SERVICE MANUAL

HIGH RESOLUTION DISPLAY MONITOR

NSH1117SKTKW

MITSUBISHI ELECTRIC CORPORATION
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CBB-S5691A

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1. Circuit description

1.1 Power circuit

1.1.1 Outline

(1) The power block is compatible with 100 to 120VAC/220 to 240VAC(50/60Hz).

(2) The active filter circuit is adopted to suppress the higher harmonic current and improve the power factor.

(3) The circuit that supplies the electric power to the secondary side is divided into two circuits that are respectively called the main power and sub power.
Though both main and sub circuits supply the power to the secondary side in the normal operation mode, the power is supplied from the sub power only in the power save mode since the main power is stopped.
The main power is the configuration used the flyback converter type switching control IC of the simulative resonant operation. Moreover, the sub power is the configuration used PWM (pulse width modulation) control IC.
In the power circuit, the voltage fluctuation from the secondary side is fed back via the photocoupler in order to suppress the voltage fluctuation caused by the load fluctuation on the secondary side.

(4) The output on the secondary side is shown in Table 1.
(Refer to the power system diagrams in Pages 1-8, 1-9 and 1-10.)

Power block	Output voltage	Application	When power save
Main power side	+190V	H. deflection circuit, video cut off circuit	OFF
	+90V	DBF circuit, high voltage circuit	OFF
	+80V	Video circuit	OFF
	+15V	H/V deflection circuit, etc.	OFF
	-15V	H/V deflection circuit, etc.	OFF
	+12V	Video circuit, H. deflection circuit, etc.	OFF
Sub power side	+6.5V	Heater	ON
	+5V	MPU, etc.	ON
	P-OFF+5V	Video circuit, etc.	OFF

Table 1

1.1.2 Rectifying circuit

(1) The AC input voltage is rectified in the full wave mode with the diode bridge in D901.

(2) In the higher harmonic circuit of the section 1.4, the AC input current becomes the sine wave form in the same phase with the AC input voltage waveform, but the interference is given to other peripheral devices since the noise of the switching current appears on the input side owing to the switching waveform. Therefore, L902 and C906 are inserted to suppress the noise that is caused by the switching current.

1.1.3 Surge current suppression

(1) TH901 (thermistor) and R930 suppress the rush current that flows when the power switch is turned ON. Moreover, D933 is added to protect D902 from the rush current.

1.1.4 Higher harmonic circuit

(1) The pulsating waveform rectified in the full wave mode by D901 is switched throughout the full cycle by the frequency of several tens kHz or more. Through this, the input current waveform becomes an average of the switching currents of the partial cycles, thus becoming the sine waveform in the macro. (See Fig.1)

(2) For the AC input voltage, the AC input current of the sine wave type in the same phase flows to achieve the power circuit of improved power factor and reduced higher harmonic wave component.

(3) L903 is the choke coil, Q901 is MOS FET, D902 is the rectifying diode, C911 is the block capacitor, and IC901 is the power factor improved controller. The power factor improved controller uses MC33262P of Motorola. (See Fig. 2)

(4) After the sub power starts, P-SUS signal becomes HI when +5V voltage is supplied to the MPU. Then, Q902 is turned ON, the voltage of approx. +18V is supplied to Pin 8 (VCC terminal) of IC901 through D932 from Pin 2 of T902, and the following operation is started.

(5) The pulsating voltage waveform rectified in the full wave mode by D901 is divided with R904, R905, R906, R907 and R908 (100VAC : 1.1Vp-p and 240VAC: 2.9Vp-p), and is input to Pin 3 of IC901 (Multiplier input). Moreover, the output (+side of C911: 400VDC) of the higher harmonic circuit is divided with R913, R914, R915, R916 and R917 (2.5VDC), and is input to Pin 1 of IC901 (error amplifier input).

(6) The output of the error amplifier and the divided waveform of the pulsating voltage input to Pin 3 of IC901 sets the threshold voltage of the current sense comparator to control the Q901 flowing current from zero to the peak line of the AC input voltage in the sine wave pattern.

(7) When Q901 is turned ON, the drain current of Q901 flows to R910 and R937 to drop the voltage, and the voltage generated by the voltage drop is input to Pin 4 (current sense input) of IC901. When the voltage reaches the threshold voltage of the current sense comparator, Q901 is turned OFF.

(8) When Q901 is turned OFF, the accumulated energy of L903 starts to be supplied to the load through D902.

(9) As the accumulated energy of L903 drops, the auxiliary coil voltage (Pin 10 of L903) also drops. When it reaches the threshold voltage of *zero current detector, Q901 will be turned ON again.

* Pin 5 of IC901 is the zero current detection terminal to input the auxiliary coil voltage of Pin 10 of L903. The zero current detector monitors that the auxiliary coil voltage drops beyond the thresh old voltage. Thus, the accumulated energy of L903 is indirectly detected.

(10) The above operation is repeated to continue the oscillating operation. Thus, the DC voltage (L903, Q901, D902 and C911 compose the voltage rise circuit.) is gained on the output, and the AC input current of the sine wave in the same phase with the AC input voltage is gained on the input side.

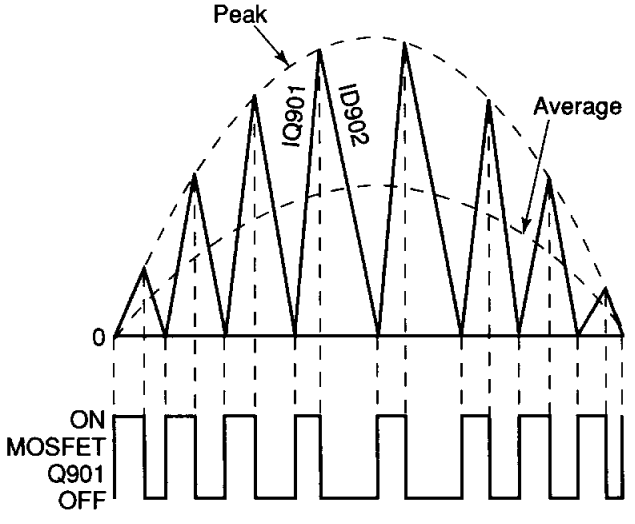


Figure 1. L903 coil current

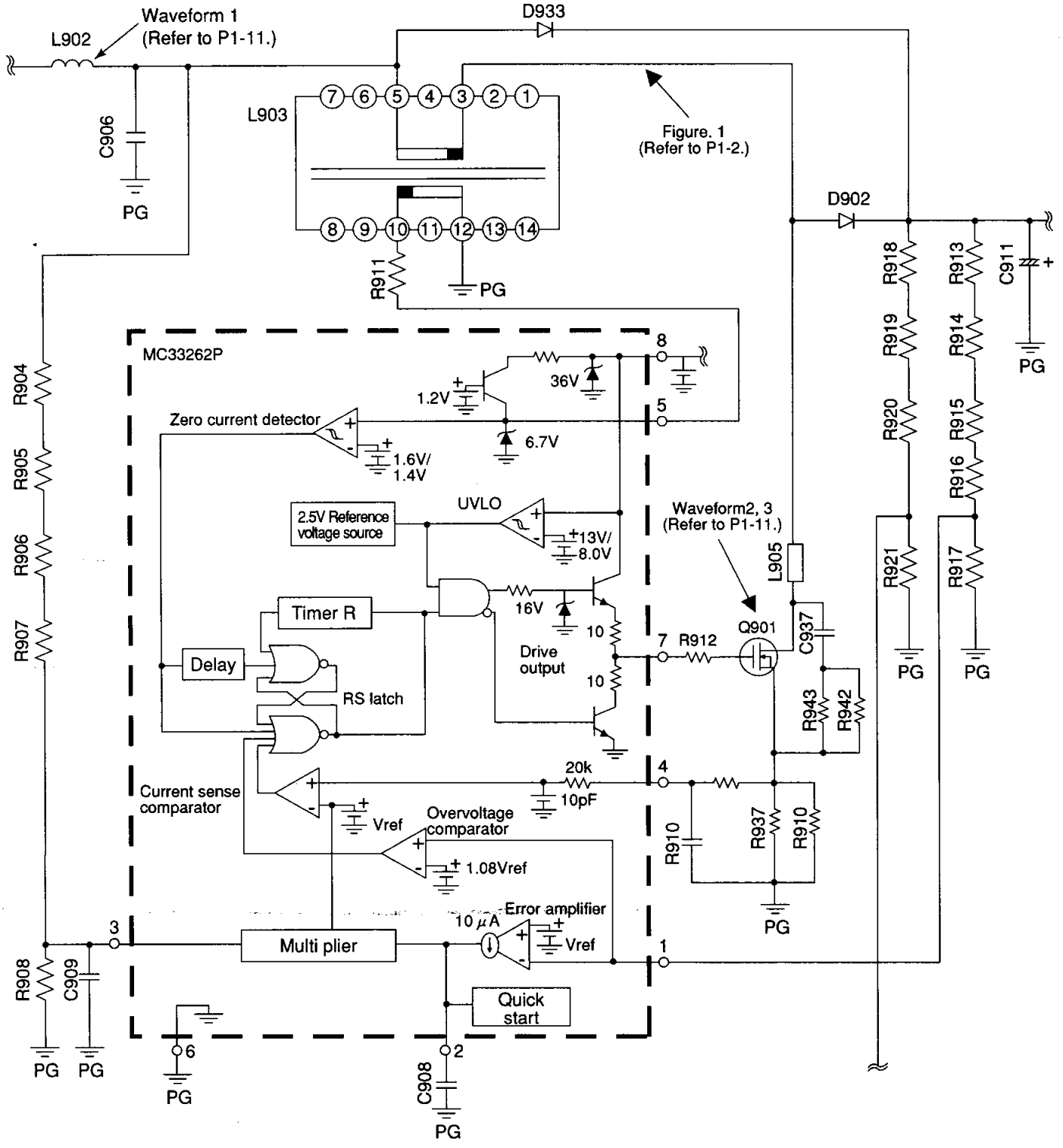


Figure 2. High harmonic waveform circuit

1.1.5 Sub power circuit

(1) The sub power uses the self-excited type regulator MIP0223SYproduced by Panasonic. (See Fig.3)

(2) When the power switch is turned ON, the rectified and smoothened DC voltage (AC voltage x $\sqrt{2}$) is supplied to Pin 3 of IC903, and is charged to C932 through Pin 1. When Pin 1 reaches 5.7V, the current supply from Pin 3 is cut off to start oscillation (approx. 100kHz) in IC903, and the output FET is put into operation. (Since Q902 is OFF, IC902 and IC 903 do not operate.)

(3) This also induces the voltage at Pin 2 of T902 and on the secondary side. These outputs are respectively rectified, and are used as the power for control on the primary side and the power for the MPU and heater.

(4) The voltage induced on the secondary side is fed back to the primary side through IC912 (photocoupler) from the constant voltage circuit that uses IC922 (shunt regulator).
The circuit supplies and controls the power for control on the primary side to Pin 1 of IC903 via R935 in order to suppress the voltage fluctuation on the secondary side.

(5) When the voltage on the secondary side starts, the MPU will be put into operation and the P-SUS signal line will become HIGH.

(6) This information is transmitted to the primary side via IC913 to turn ON Q902.
When Q902 is turned ON, the power for control on the primary side will be supplied to IC901 and IC902 to operate the higher harmonic circuit. Thus, the main power circuit will be put into operation.

1.1.6 Main power circuit

(1) The main power circuit adopts the flyback type switching power of pseudo-reosonance operation. This is composed of a Sanken brand hybrid IC (STR-F6676) that integrates the power MOS-FET and control IC.
The circuit operation is described as follows. (See Fig. 4.)

(2) The timing at that the power MOS-FET is turned ON is consistent with the bottom point of the voltage resonant waveform after the transformer (T901) discharges the energy to the secondary side, that is, a half cycle of the resonant frequency determined by Lp value (primary coil inductor value) of T901, and C914 (resonant capacitor). This is called pseudo-reosonance operation. The advantage of such an effect is that the switching loss is reduced by turning it ON when the voltage between the drain sources of the power MOS-FET becomes the lowest.

(3) Like the higher harmonic circuit, voltage of approx. +18V is supplied to the Vcc terminal (Pin 4) of IC902 (STR-F6676) via D932 from Pin 2 of T902 when Q902 is turned ON by the P-SUS signal from the MPU.
When the voltage of Pin 4 of IC902 reaches 16V, the control circuit will be put into operation to turn ON the integrated MOS-FET.

(4) When MOS-FET is turned ON, the capacitor C1 in IC will be charged to approx. 6.5V. On the other hand, the drain current flows to R928, and the voltage generated by the voltage drop is applied to Pin 1 (OCP/FB terminal) of IC902.
When the voltage of Pin 1 reaches approx. 0.73V, the comparator (Comp. 1) in IC will be activated to turn OFF MOS-FET.

(5) The voltage between both ends of C1 drops to approx. 3.7V. the oscillator output will be reversed again to turn ON MOS-FET.
The above is repeated to continue the oscillation operation.

(6) Here, IC902 monitors +190V of the output on the secondary side with IC921 (error amplifier) and feeds back it to Pin 1 of IC902 with IC911 (photocoupler), thus suppressing the voltage fluctuation of the primary side.

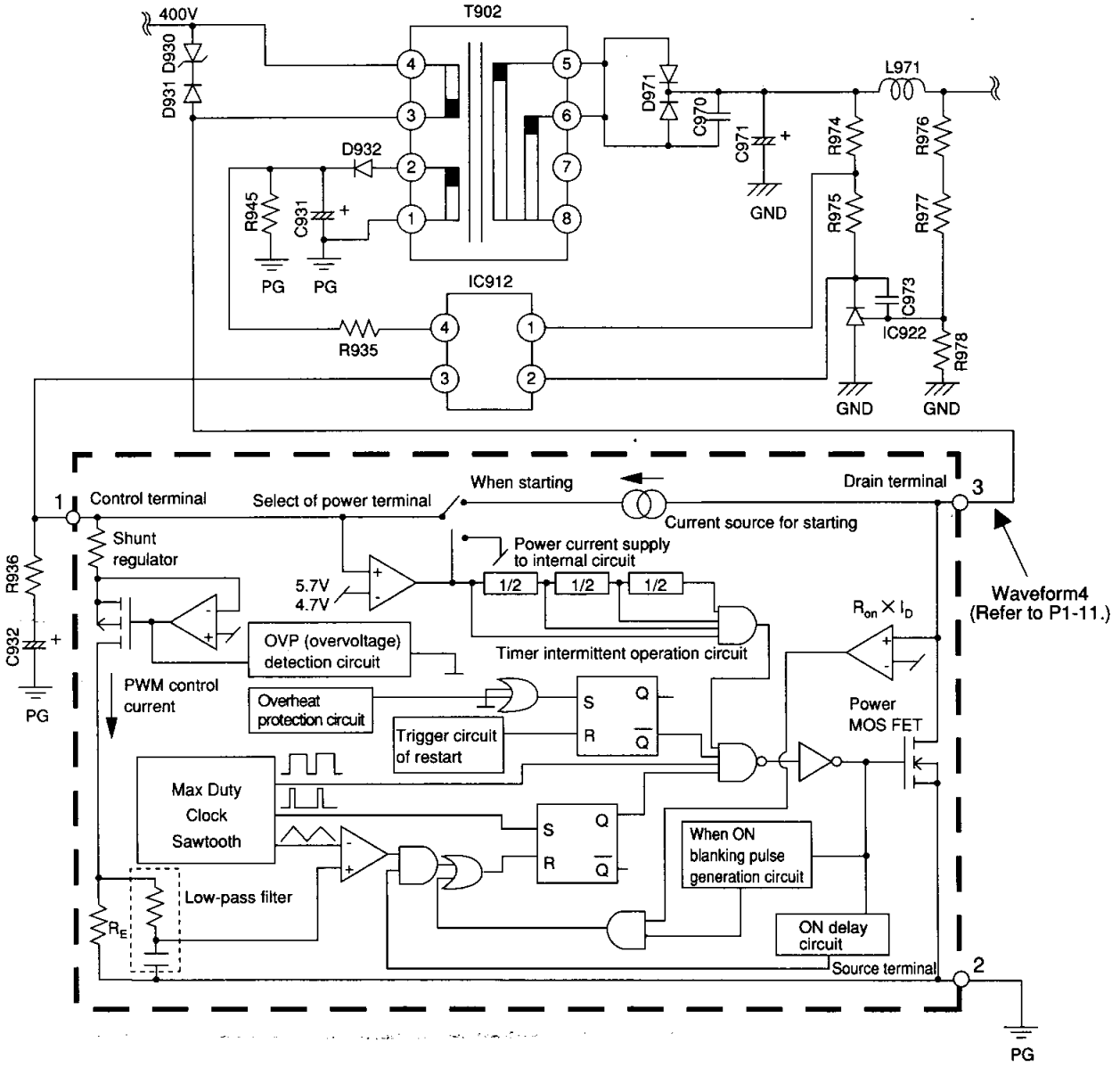


Figure 3. IC903 (MIP0223Y) block diagram and peripheral circuit

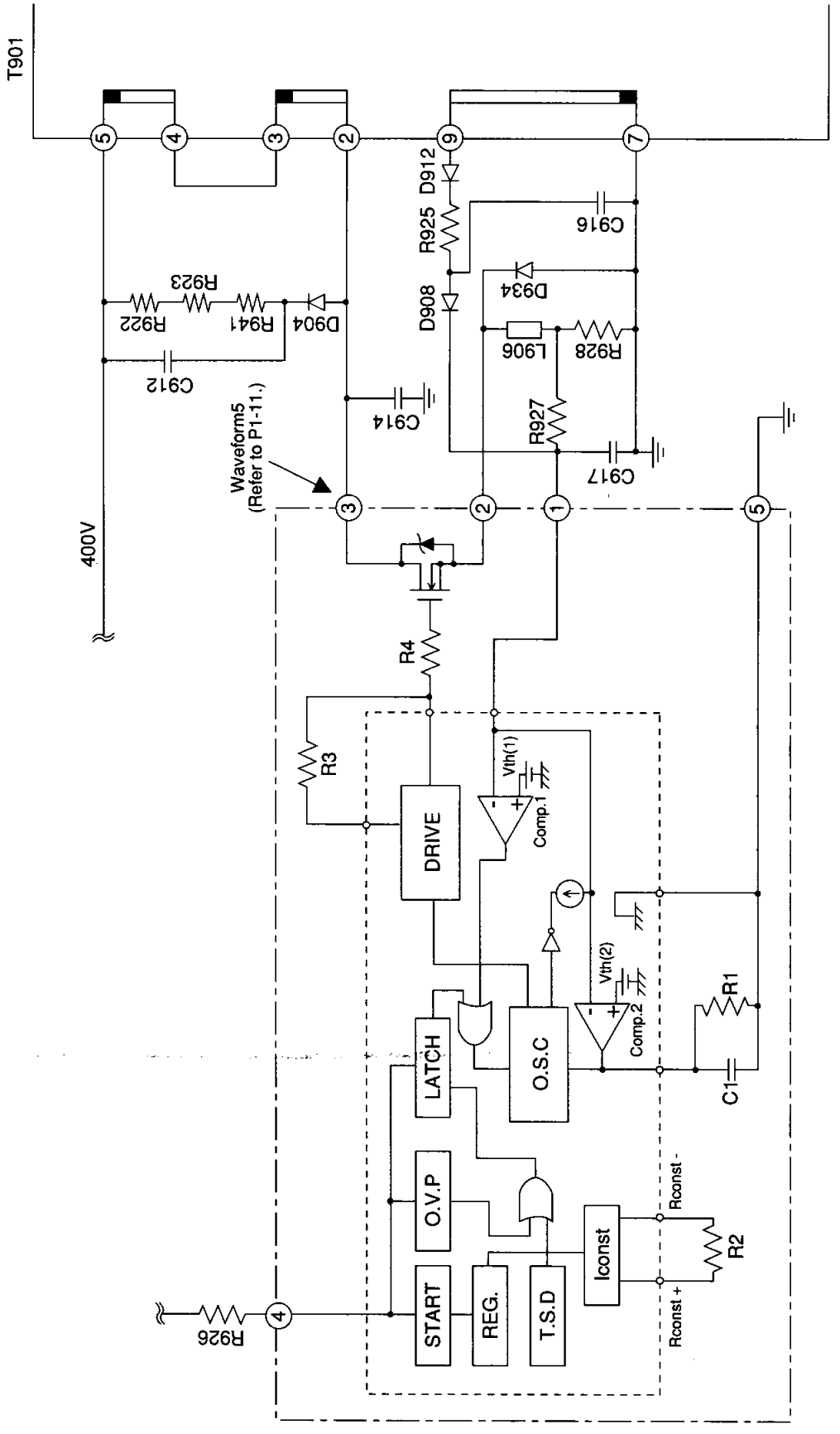


Figure 4. IC902 (STR-F6676) block diagram and peripheral circuit

1.1.7 Demagnetizing circuit

(1) The automatic and manual demagnetizing circuit is provided.
The circuit prevents the picture from dropping its quality due to the magnetization on CRT, and operates as follows.

(2) When powering ON, Q963 flows to activate RY901 by DG signal output by the MPU.
This will make the current flow through the demagnetizing coil for demagnetization. The demagnetizing time is approximately 5 seconds.
Manual demagnetization becomes possible by selecting the demagnetizing menu on the OSD picture.

1.1.8 Power management circuit

Turn ON the power management setting on the menu picture of OSD, and the energy saving mode shown in Table 2 will be ready depending on whether the horizontal/vertical sync. signal is present or not.

	H-sync	V-sync	Video	Power consumption	Recovery time	LED indicator
OFF	On	On	Active	140W	—	Green
ON	Off	On	Blank	≦5W	3秒	Amber
	On	Off	Blank			
	Off	Off	Blank			

Table 2

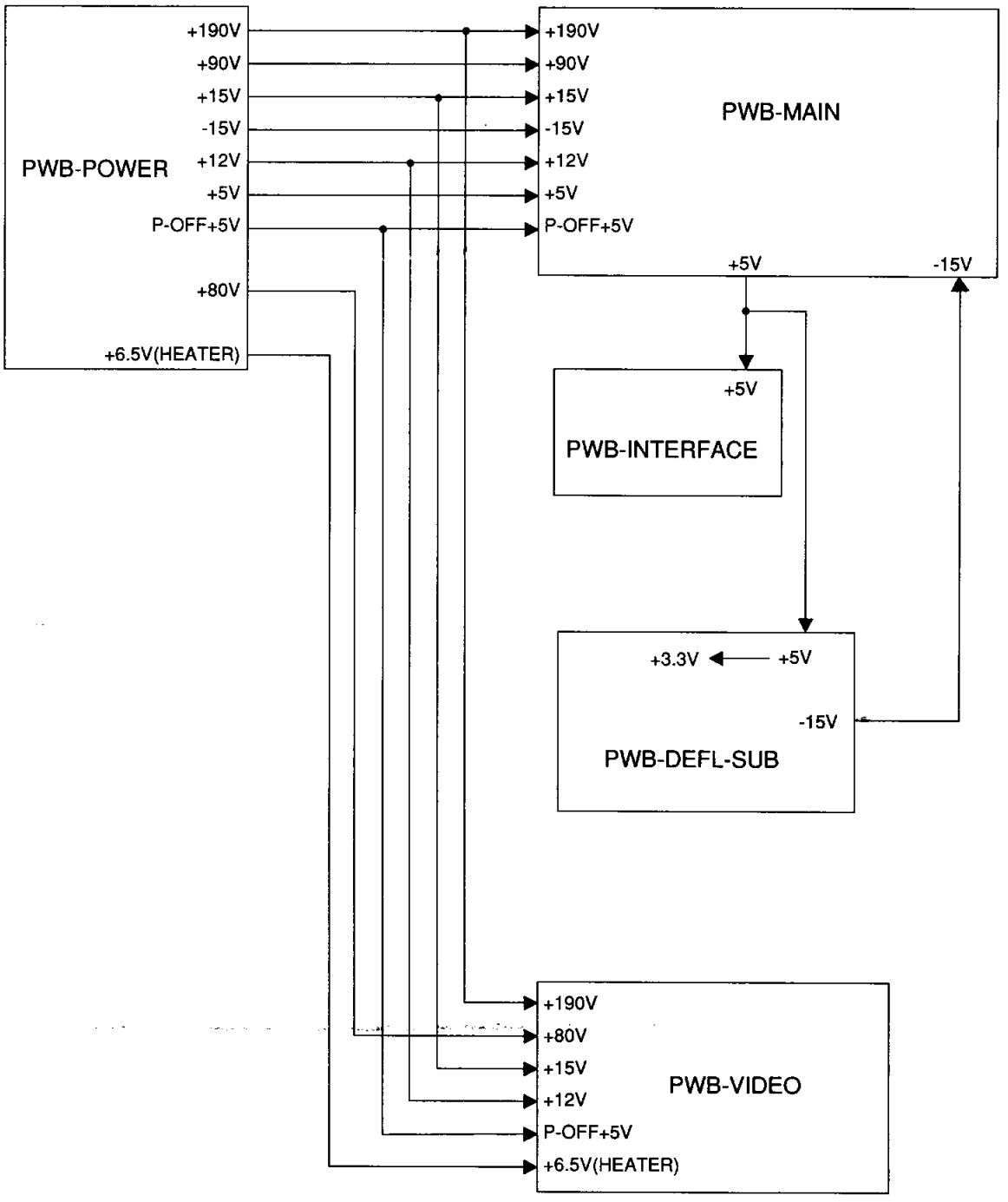
1.1.9 Protective circuit

(1) Overcurrent protective circuit (primary side)
IC902 is provided with an overcurrent protective circuit. The voltage drop generated by the drain current that flows into R928 is input to Pin 1 (OCP/FB terminal) of IC902. When the voltage reaches 0.73V, the overcurrent protective circuit will be activated.

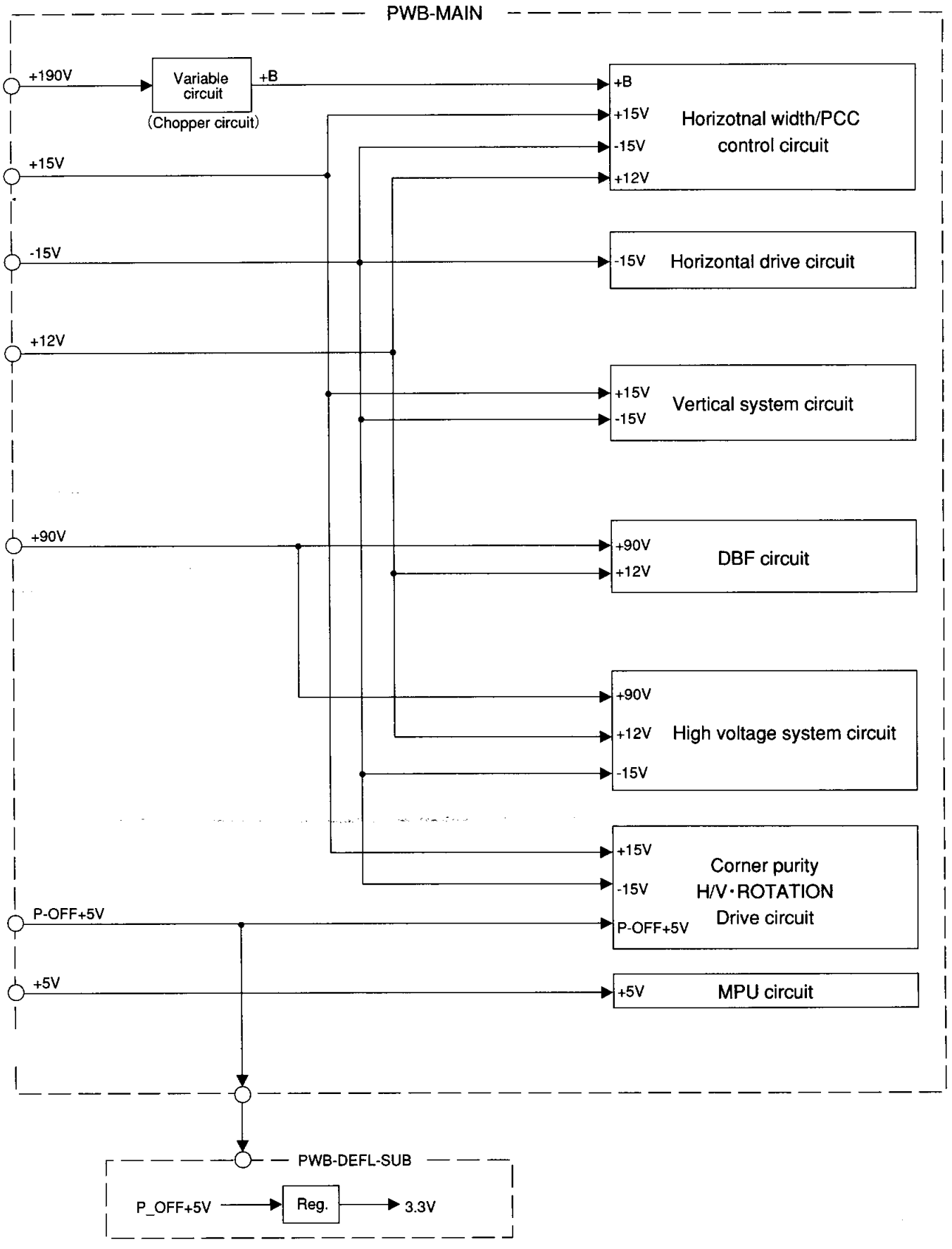
(2) Overcurrent protective circuit (secondary side)
To protect the parts on the secondary side, the short-circuit detection circuit is provided on the secondary side output (+190V, +90V, +80V, +/-15V), one for each. As an example of +190V, the output line of +190V is monitored with R964, R965, D968 and Q961. If it drops beyond +150V for any reason, Q961 will be turned ON to transmit the information to the MPU. Then, since the MPU sets P-SUS signal at LOW, Q902 will be turned OFF to cut off the power to IC902 in order to stop IC902. (IC901 will be also stopped at the same time.)
The overcurrent protective circuit is designed to be activated when the output voltage drops approx. 20 to 30%.
The circuit takes the role of the FUSE that is used on the conventional model.

(3) Overvoltage protective circuit
R918, R919, R920 and R921 are used to detect the overvoltage in the higher harmonic circuit, and the tertiary coil (Pin 9) of T901 is used to detect the overvoltage of the voltage on the secondary side. They are both connected to the overvoltage protective circuit (Q904, Q905) on the primary side. If any overvoltage results for any reason, Q905 will be turned ON to turn ON Q904. Since the base potential of Q903 then drops beyond 0.7V to stop it, Q902 will be stopped. Since the power is cut off for IC901 and IC902 as Q902 is stopped, the switching operation will be stopped.

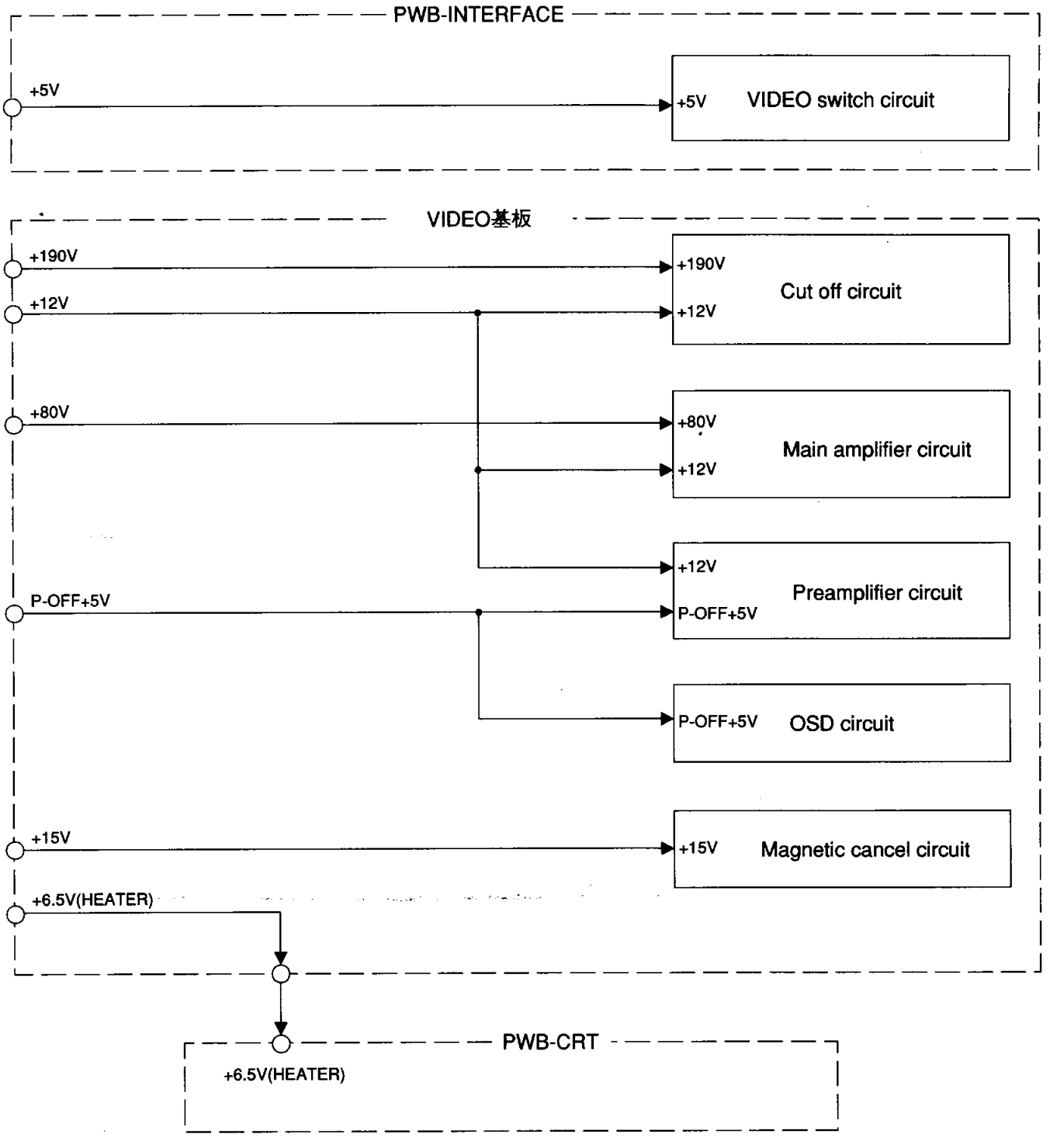
~Power system diagram 1~

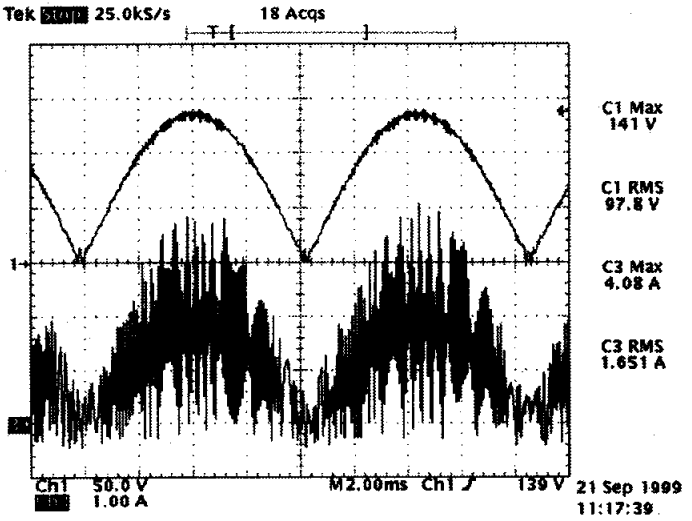


~Power system diagram 2~

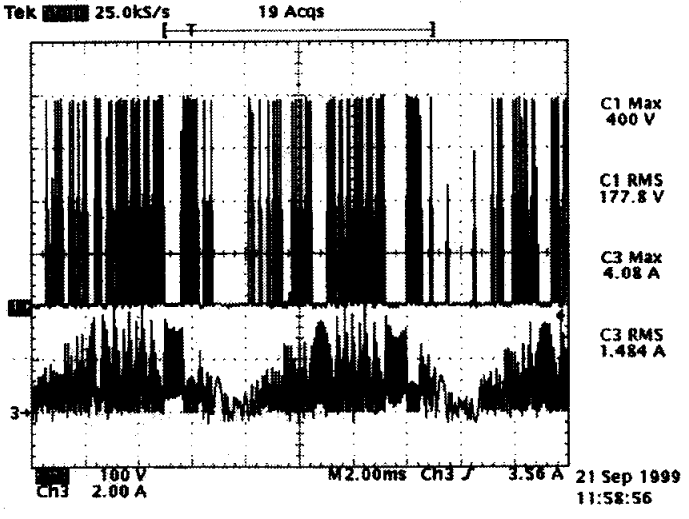


~Power system diagram 3~

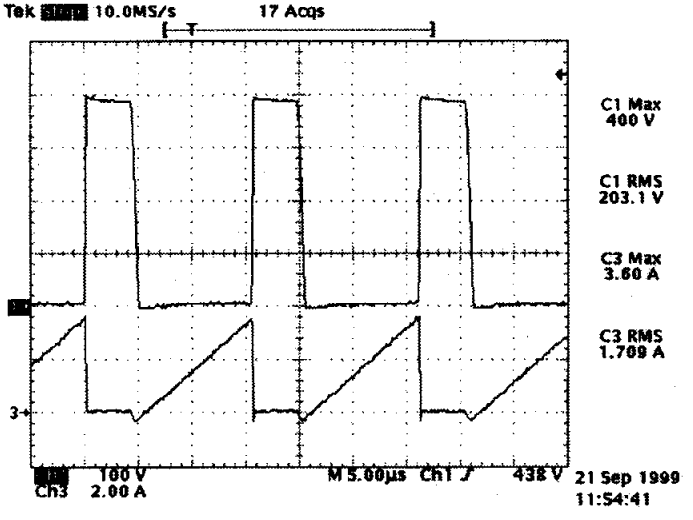




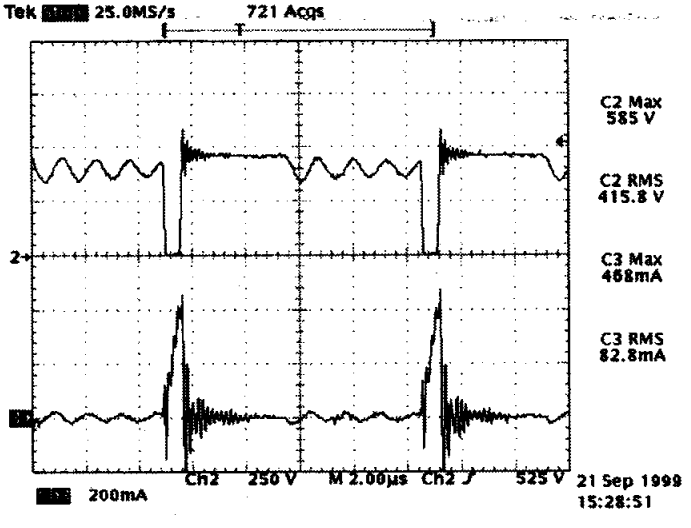
Waveform 1. Top :AC input voltage
Bottom :AC input current



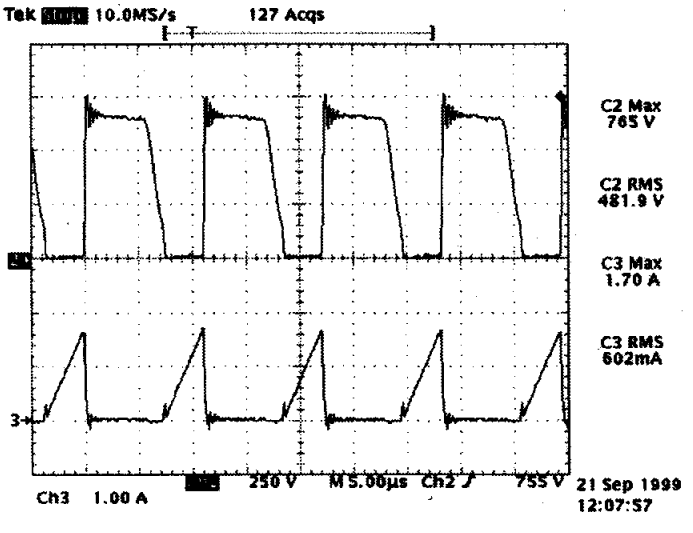
Waveform 2. Top :Q901 drain voltage
Bottom :Q901 drain current



Waveform 3. Top :Q901 drain voltage
Bottom :Q901 drain current



Waveform 4. Top :IC903 drain voltage
Bottom :IC903 drain current



Waveform 5. Top :IC902 drain voltage
Bottom :IC902 drain current

1.2 Deflection circuit block

1.2.1 Horizontal deflection circuit

The operational principle of the horizontal deflection circuit is shown as follows.
Q502 and D503 operate as the horizontal output and damper diode respectively.
IC502, Q511 and RY501 are switched according to the horizontal frequency to compensate the horizontal linearity.

In Fig. 5, the horizontal output transistor Q502 is turned ON and OFF through the drive transformer T501, drive transistor Q501 or Q7A0, Q7A1, Q7A2 and so on by the drive pulse of Pin 25 of IC700 on the PWB-DEFL-SUB.
While Q502 is ON, the deflection current Idy increases to the maximum Ip according to the following formula.

$$Idy = (Vcc/Ldy) \times Ton$$

The maximum Ip at the chassis is approximately 8A in case of full scan at fh=106k.

Here, Vcc: Q504 output voltage
Ldy: Parallel value of Lh value (=62μH) of DY and horizontal output transformer (=5mH)
Ton: Time for that Q502 is ON

When the drive pulse becomes a negative polarity, Q502 will be turned OFF, and it will flow to charge C502 and C503 until the maximum value Vcp of the collector voltage reaches the value of the following formula.

$$Vcp = Vccx\{1 + (\pi/2)x(Ts/Tr)\}$$

When Vcp reaches the maximum value, the electric charge accumulated in C502 and C503 will flow into DY as the discharge current.
The charged/discharged current is called the retrace time, being expressed with the following formula.

$$Tr = \pi\sqrt{(Ldy \cdot Cr)}$$

At the chassis, the retrace time is set at approx. 2μs.
Here, it becomes the total of the values of Cr:C502, C503. Moreover, Ts is called the trace time, being expressed by the following formula with the horizontal cycle of T.

$$T = Ts + Tr$$

When Vcp becomes 0, the damper diode D503 is turned ON, and Idy decreases from -Ip to 0 ampere. Since the ON term of Q502 and the ON term of the damper diode are made to be overlapped at the 0 ampere point of Idy, cross over distortion at the 0 ampere point of Idy is prevented from occurring. D503 flows the transient current with the high speed damper diode. The horizontal output transformer T502 is connected to the power in parallel with the deflection yoke, working as the choke coil. Figs. 6 and 7 show the image of the circuit operation and the waveform at the monitor.

The width of the horizontal picture and side PCC are controlled with IC5J1, IC5J2, Q503 and Q504. The horizontal width signal applied to Pin 5 of IC5J2 by Pin 64 of IC700, and distortion compensation signals are compared with the signal that is converted to the voltage from the current value of the horizontal deflection circuit by T503 and is fed back to Pin 13 of IC5J2 via IC5J1. Then, it is compared with the sawtoothed wave of the constant inclination type that is synchronized with the horizontal frequency generated in IC, and is converted to the PWM signal of the rectangular wave. The PWM signal is output to Pin 9 of IC5J2, and the above control is done by driving the gate of Q504. Fig. 8 shows the block diagram of IC5J2, and Fig. 9 indicates the image waveform of the operation.

Moreover, as the operation of Q5J1 and Q5J2 connected to Pin 11 of IC5J2, Q5J1 is normally turned OFF since Q5J2 is turned ON. However, as the 15V line lowers when the power is turned OFF, and Q5J2 is turned OFF, Q5J1 is turned ON and Pin 11 of IC5J2 is pulled to GND. Since Pin 11 of IC5J2 controls the ON term of PWM to 1.2μs when 0V is applied, it works to lower the output voltage of Q504 as the result in order to prevent breakage from occurring due to the abnormal pulse during the transient time of Q502 (H-OUT Tr).

Q503 works as the ripple filter of the 190V line to keep the emitter voltage of Q503 constant even if the collector voltage of Q503 slightly fluctuates. Though the voltage of 190V is applied to the collector of Q503, the emitter output is stabilized at 187V. It is mainly effective for dynamic regulation.

The horizontal raster position is adjusted with Q5A1, Q5A2, VR5A1 and T502. The reference voltage is taken at the connection point of Cs, and is input to Pin 2 of T502. As the DC level of the emitter voltage of Q5A1 and Q5A2 is raised by adjusting VR5A1, the current will flow into the DY side to move the raster leftward. On the contrary, the current flows to the Q5A2 side to move the raster rightward as the DC level of the emitter is lowered. For adjustment, the emitter voltage of Q5A1 and Q5A2 are varied with VR5A1 by the timing signal of 106k85Hz to adjust the DC level of Idy in order to position the raster position at the center of CRT. Fig. 10 shows the operation image.
This is executed only in the factory adjustment but it is not accessible for user adjustment.

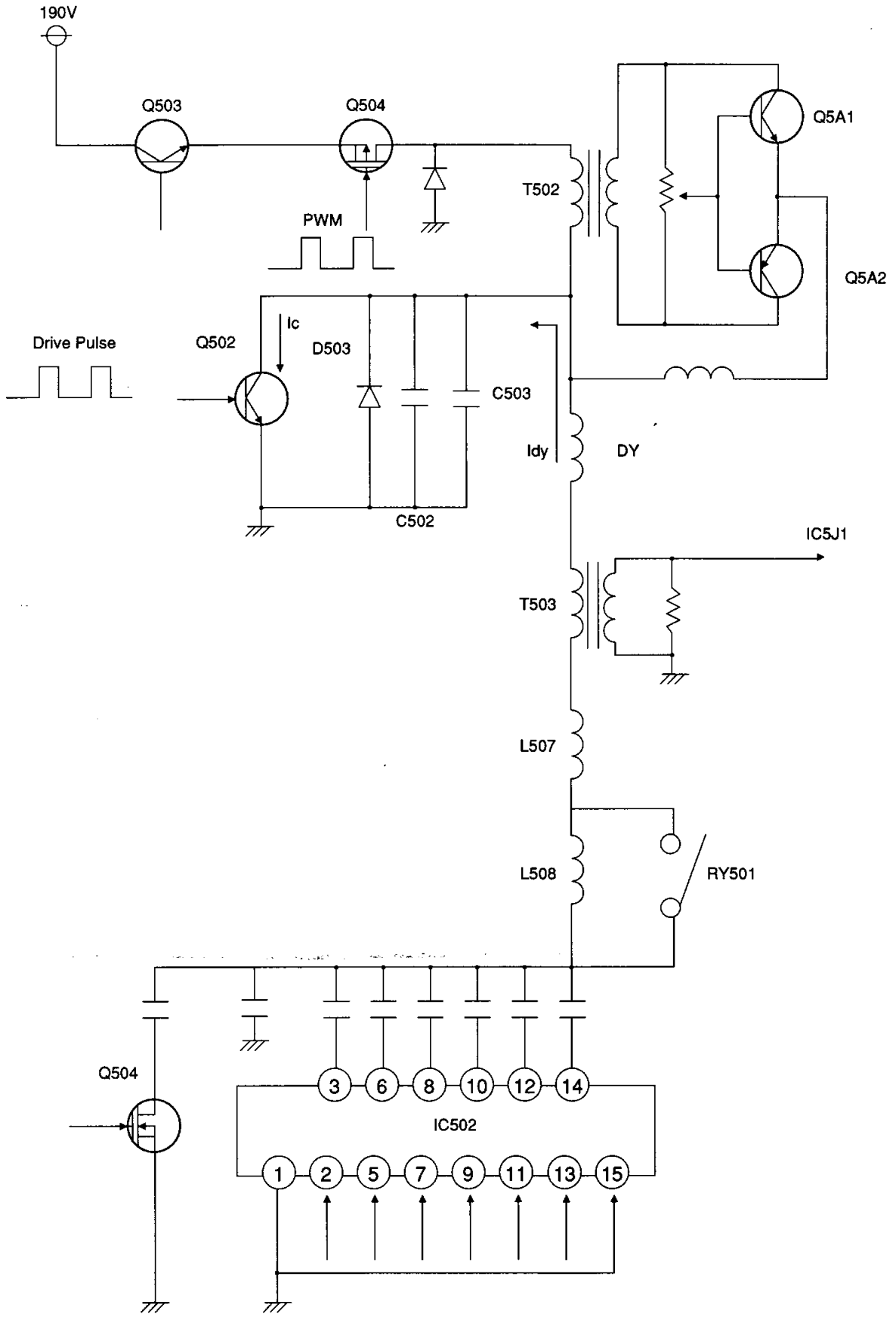

190V
Q503
Q504
PWM
T502
Q5A1
Q5A2
Drive Pulse
Q502
Ic
D503
C503
C502
Idy
DY
IC5J1
T503
L507
L508
RY501
Q504
3
6
8
10
12
14
IC502
1
2
5
7
9
11
13
15

Figure 5

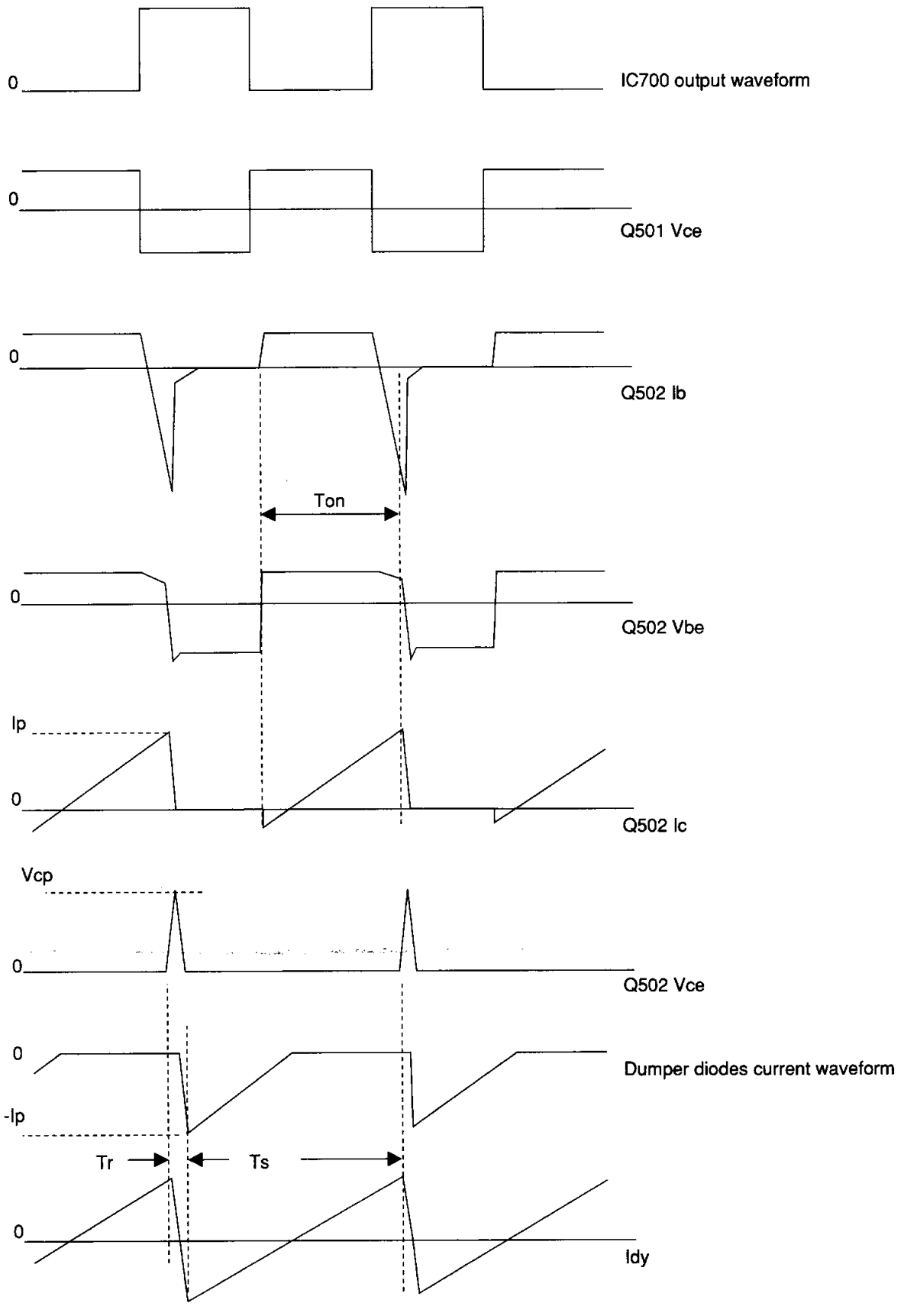
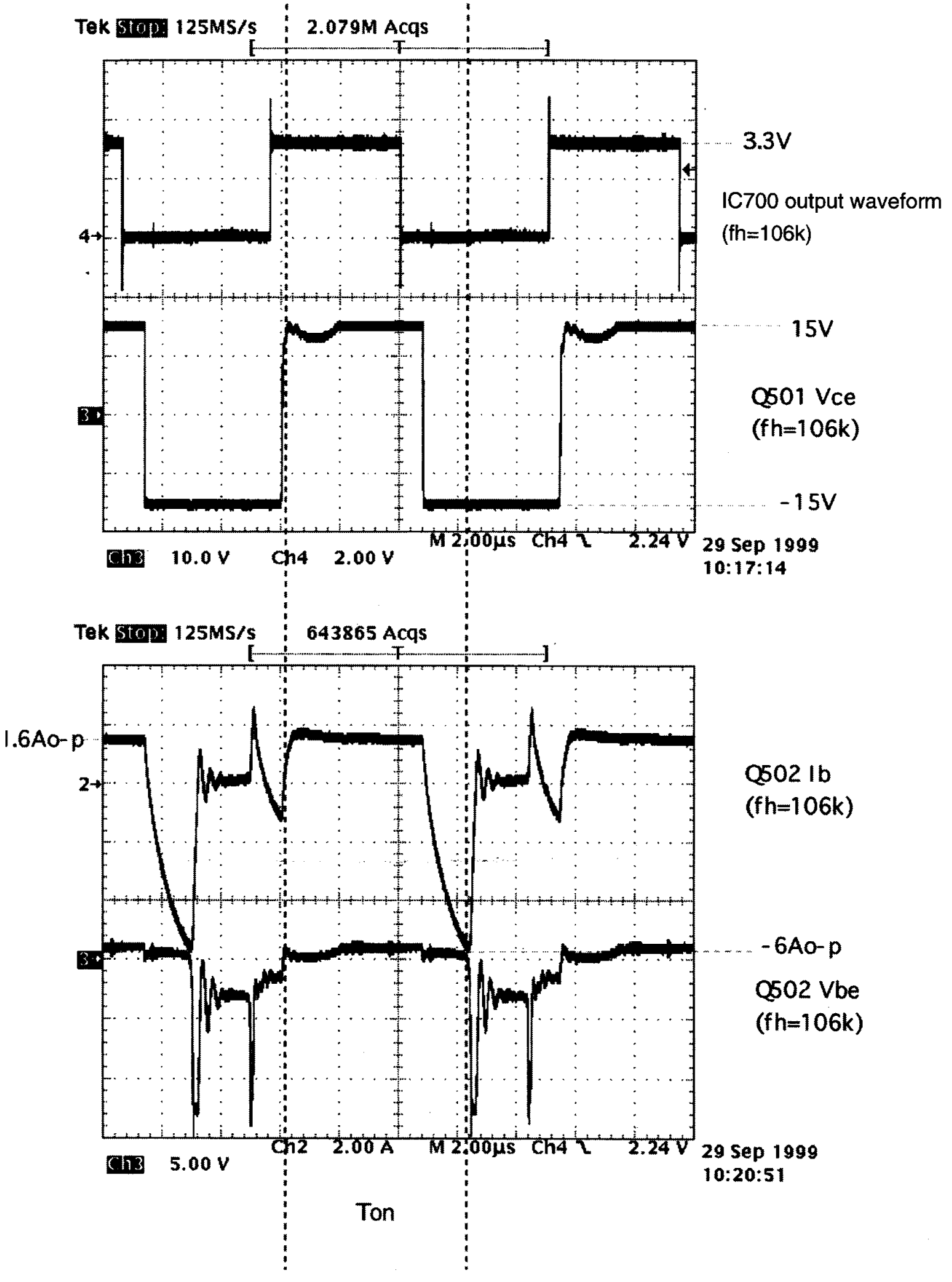
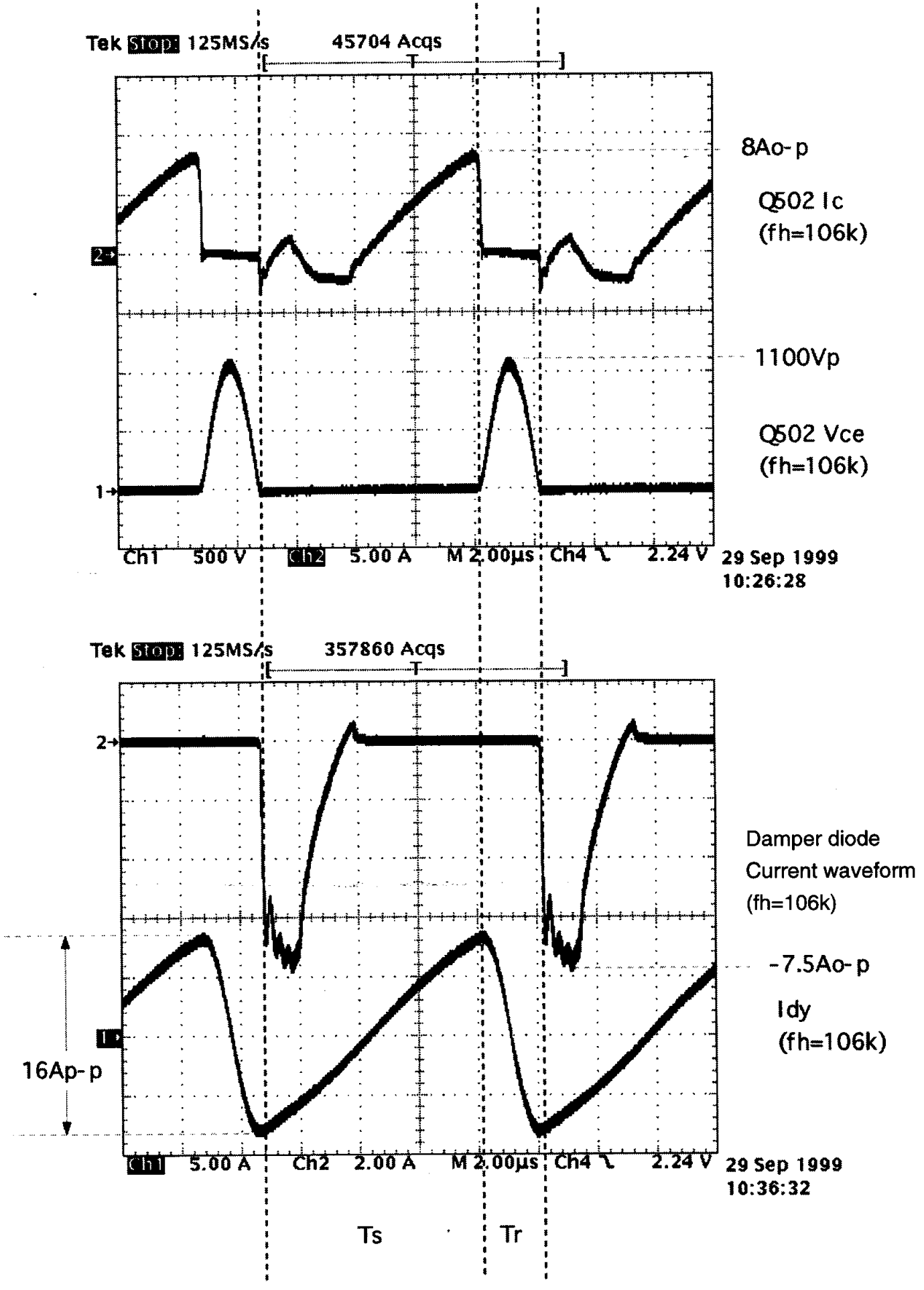

0
IC700 output waveform
0
Q501 Vce
0
Q502 Ib
Ton
0
Q502 Vbe
Ip
0
Q502 Ic
Vcp
0
Q502 Vce
0
Dumper diodes current waveform
-Ip
Tr
Ts
0
Idy

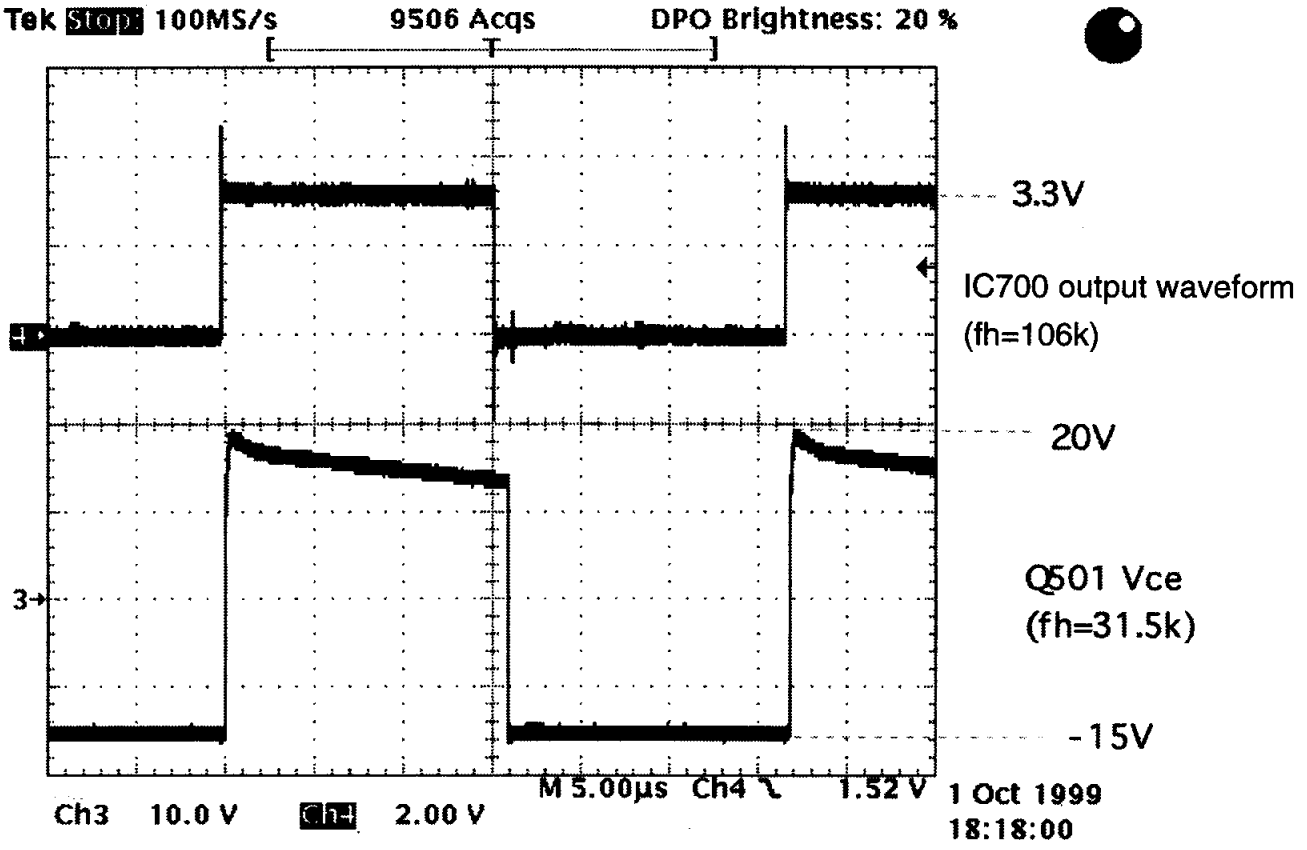
Figure 6

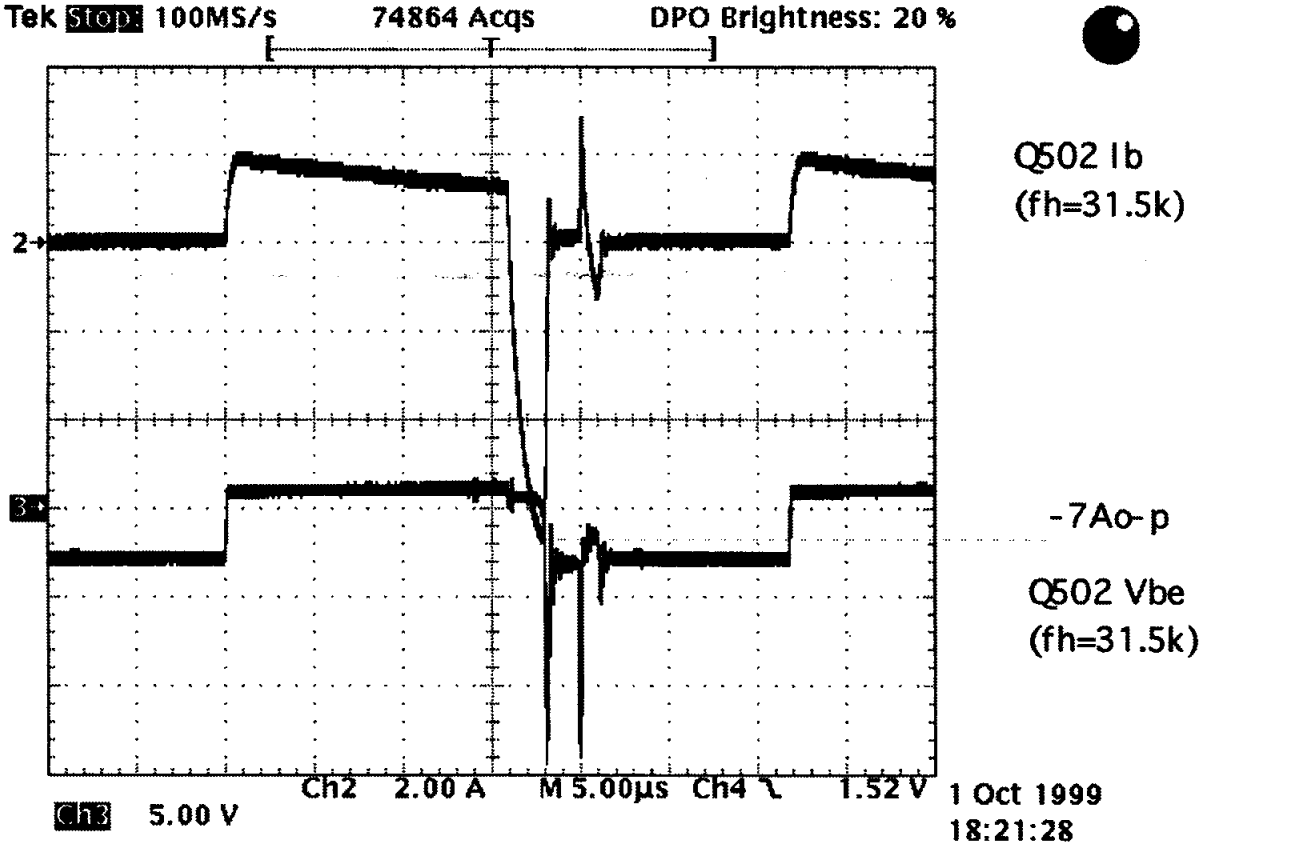
Figure 7. Deflection circuit waveform while fh=106k

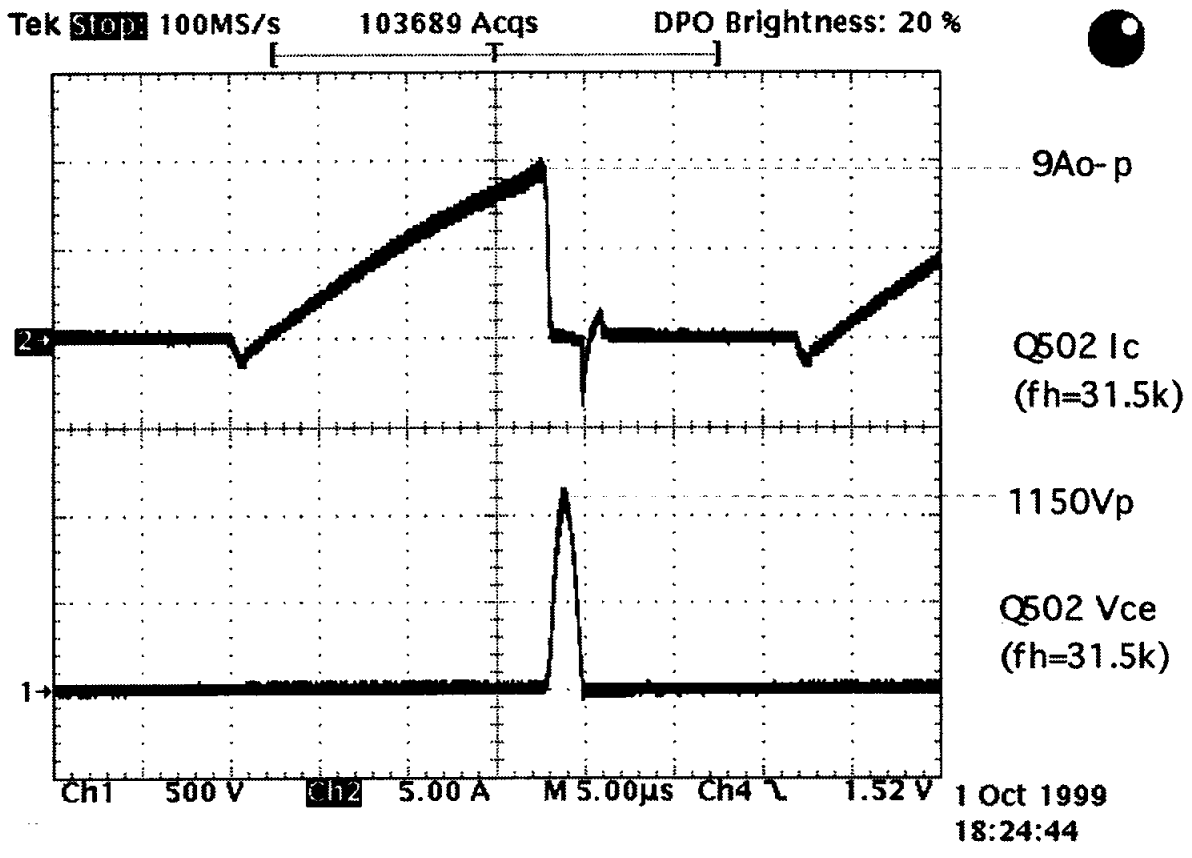


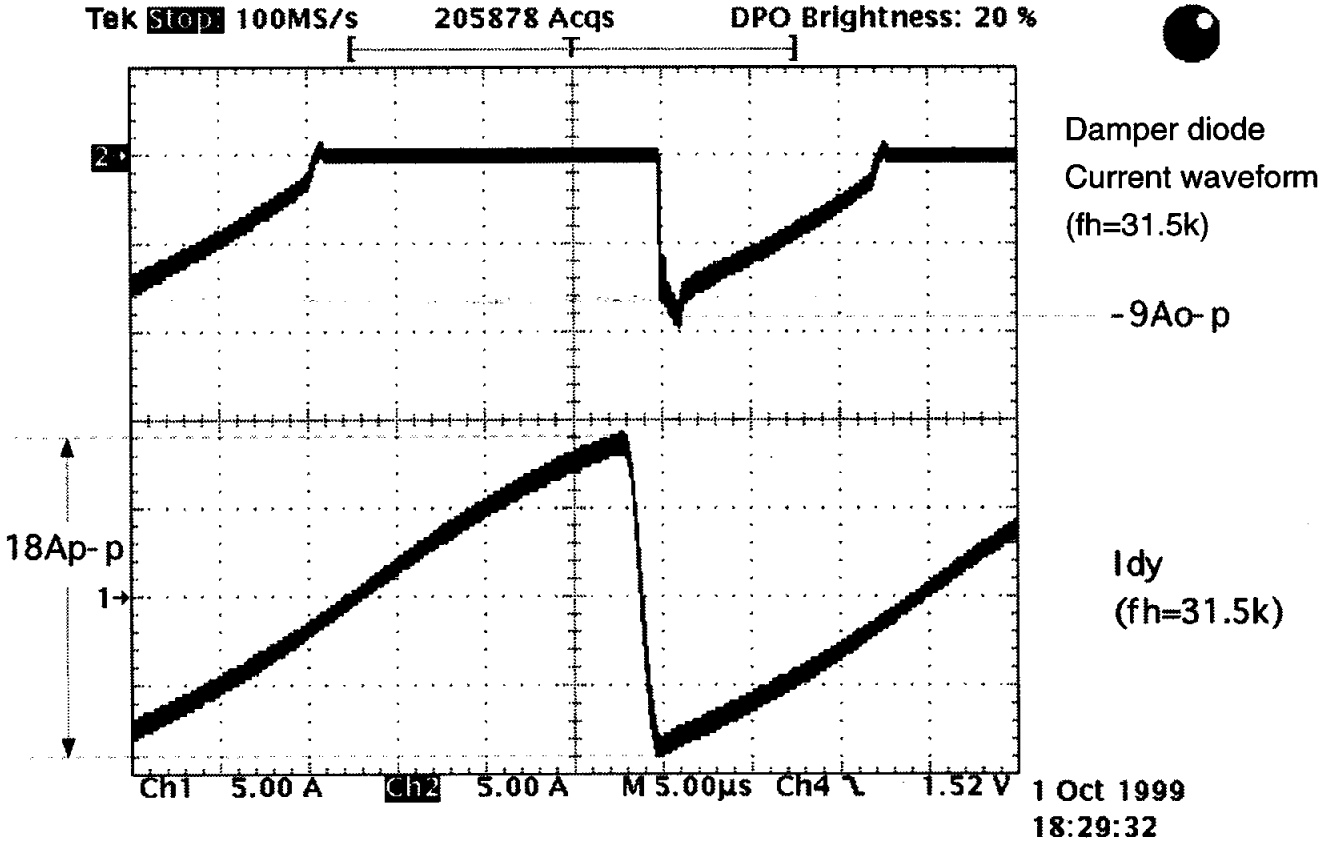

Tek Stop: 125MS/s 45704 Acqs
8Ao-p
Q502 Ic
(fh=106k)
1100Vp
Q502 Vce
(fh=106k)
Ch1 500 V Ch2 5.00 A M 2.00µs Ch4 2.24 V
29 Sep 1999
10:26:28
Tek Stop: 125MS/s 357860 Acqs
Damper diode
Current waveform
(fh=106k)
-7.5Ao-p
Idy
(fh=106k)
16Ap-p
Ch1 5.00 A Ch2 2.00 A M 2.00µs Ch4 2.24 V
29 Sep 1999
10:36:32
Ts
Tr

Deflection circuit waveform while fh=31.5k






Tek Stop: 100MS/s 103689 Acqs DPO Brightness: 20 %
9Ao-p
Q502 Ic
(fh=31.5k)
1150Vp
Q502 Vce
(fh=31.5k)
Ch1 500 V Ch2 5.00 A M 5.00µs Ch4 1.52 V
1 Oct 1999
18:24:44


Tek Stop: 100MS/s 205878 Acqs DPO Brightness: 20 %
Damper diode
Current waveform
(fh=31.5k)
-9Ao-p
18Ap-p
Idy
(fh=31.5k)
Ch1 5.00 A Ch2 5.00 A M 5.00µs Ch4 1.52 V
1 Oct 1999
18:29:32

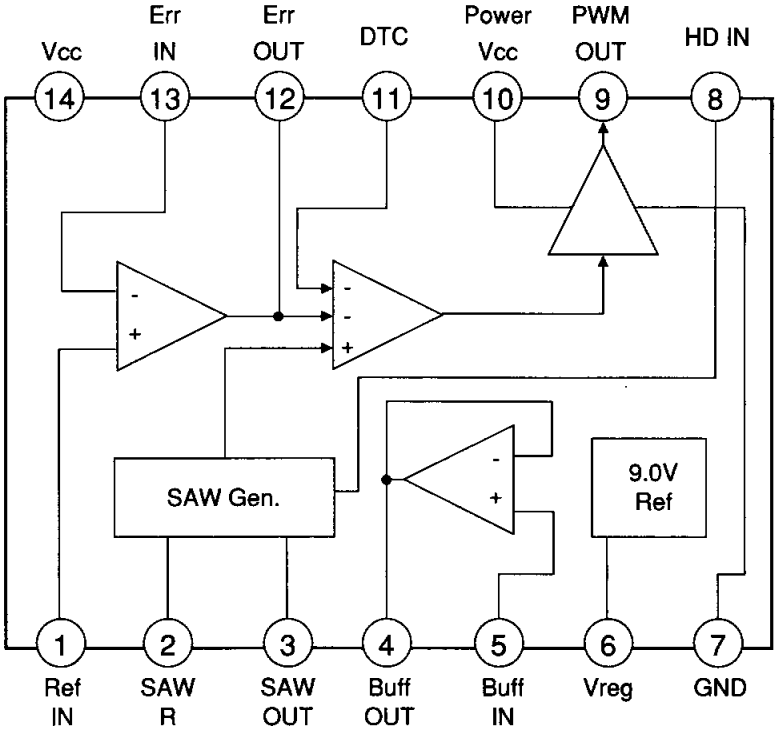


Figure 8. IC5J2 block diagram

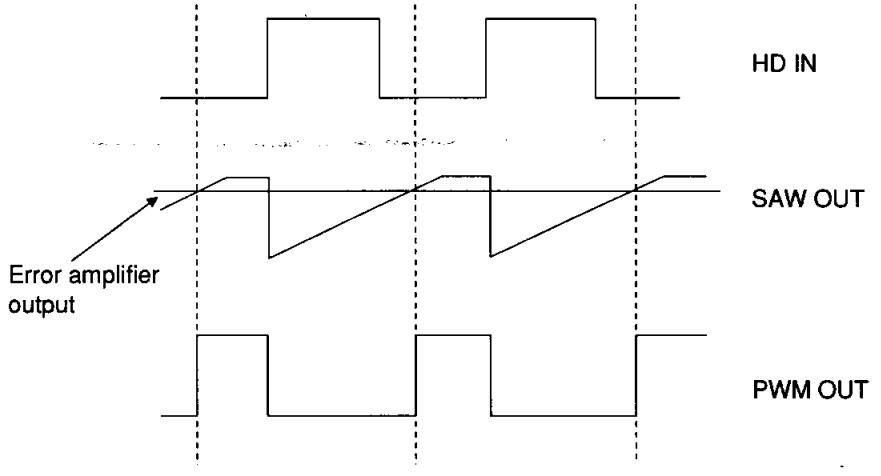


Figure 9. Operation image

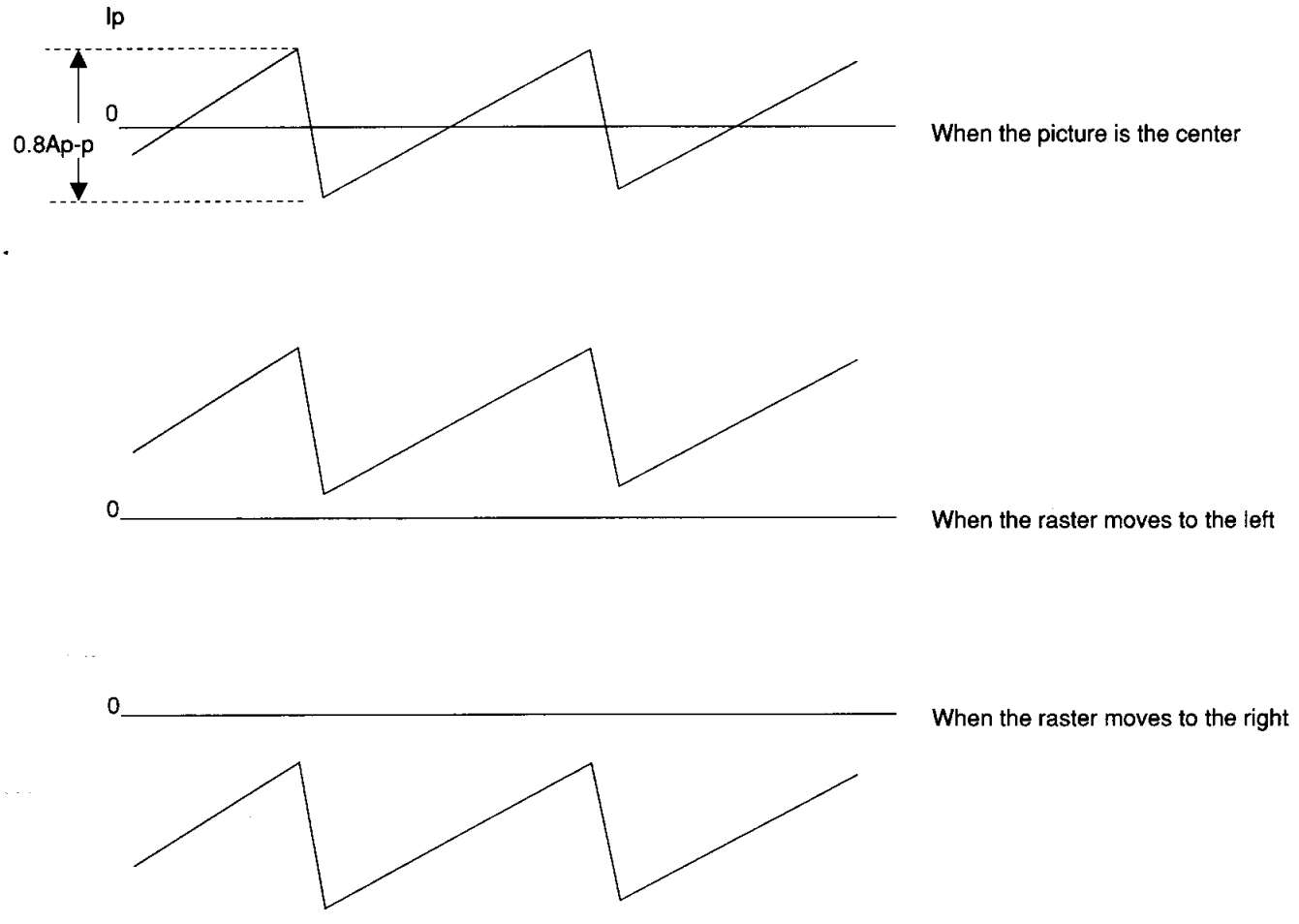

Ip
0
0.8Ap-p
When the picture is the center
0
When the raster moves to the left
0
When the raster moves to the right

Figure 10

1.2.2 Deflection current compensation circuit

As the picture becomes flatter, the arrival distance of the deflected electronic beam becomes more different between the center and both ends of the picture. Therefore, there is a tendency for the image to be contracted at the center of the picture and expanded at both ends of the picture. Moreover, the left side of the picture is more expanded than the right side of the picture owing to the characteristics of the circuit. CS applies S type compensation to the deflection current with the resonant effect of the deflection yoke and contracts at both ends of the horizontal axis. The linearity coil increases the inductance of the starting section of the deflection current with the supersaturated reactor, and works to contract the left side of the horizontal axis.

As the frequency is lower, the capacity of CS is generally increased and the linearity coil with a larger impedance value is used. In the practical circuit, seven CS capacitors are prepared, and are combined as desired. Two linearity coils are prepared, and whether one coil or the other is used is switched.

(1) S type compensation with CS

CS is switched in seven steps by FET. IC502 element with six FETs included and Q511 with one FET are used. On IC502, Pins 2, 5, 7, 9, 11 and 13 are used as the gate, and Pins 3, 6, 8, 10, 12 and 14 are used as the drain. Pins 1 and 15 are used as the ground, and each source are grounded to the earth. The binary value signal of HIGH (5V) or LOW (0V) is input to each gate by IC102. In case of HIGH, FET is turned ON. In case of LOW, FET is turned OFF. The correspondence to the signals from the capacitor and IC102 are as follows.

	G	D	Capacitor	Signal
FET1	2	3	C518	CS3
FET2	5	6	C517	CS2
FET3	7	8	C516	CS6
FET4	9	10	C515	CS7
FET5	11	12	C514	CS4
FET6	13	14	C525	CS5
FET7	—	—	C512	CS1

The column of G and D is Pin No.

(2) Compensation with linearity coil

The linearity coil is a special coil in which the magnet is used as the core of the coil and the inductance value varies depending on the flowing current. In the practical circuit, L507 and L508 are relevant. L507 is used with all frequencies but L508 is used at low frequencies only. To switch whether L508 is used or not, the relay RY501 of one pole type is used. Like CS, the binary value signal of HIGH (5V) or LOW (0V) is input to the base of Q505 by IC102. In case of HIGH, RY501 turns ON since Q505 turns ON. At this time, the deflection current does not flow through L508 but through RY501. On the other hand, RY501 also turns OFF as Q505 turns OFF in case of LOW. Therefore, the deflection current flows through L508 and L507.

As shown in the table below, CS is switched on the horizontal frequency bands, and the linearity coil is switched. 1/0 in the table express the signals from IC102 with 1 for HIGH and 0 for LOW. Here, the column of the frequency expresses the lower limit value.

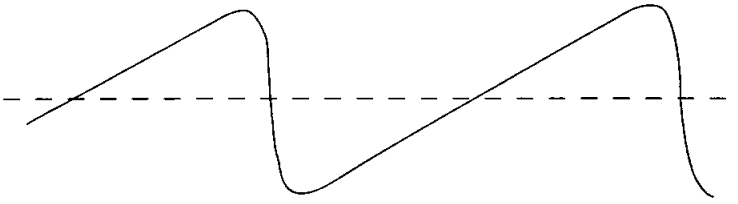
Frequency (kHz)	Lin-coil	CS7 C515	CS6 C516	CS5 C525	CS4 C514	CS3 C518	CS2 C517	CS1 C512
30	0	1	1	1	1	1	1	1
34	0	0	1	1	1	1	0	1
36.5	0	0	0	0	1	1	0	1
39	0	0	1	1	0	1	1	0
45	0	0	1	1	1	0	1	0
47.5	1	0	1	1	1	0	1	0
49	1	1	1	1	1	1	0	0
52	1	1	1	1	1	1	0	0
55	1	1	1	0	1	1	0	0
59	1	0	0	0	1	1	0	0
61	1	0	0	0	1	1	0	0
63	1	1	0	1	0	1	0	0
66	1	1	0	1	1	0	0	0
70	1	1	0	1	1	0	0	0
73	1	0	0	1	1	0	0	0
76	1	1	1	0	1	0	0	0
78.5	1	1	0	0	1	0	0	0
81.5	1	1	0	0	1	0	0	0
83	1	0	1	1	0	0	0	0
86.5	1	1	0	1	0	0	0	0
89	1	1	0	1	0	0	0	0
92	1	0	0	1	0	0	0	0
94	1	1	1	0	0	0	0	0
97	1	1	1	0	0	0	0	0
104	1	1	0	0	0	0	0	0
108	1	1	0	0	0	0	0	0

Here, the following timing is exceptional.

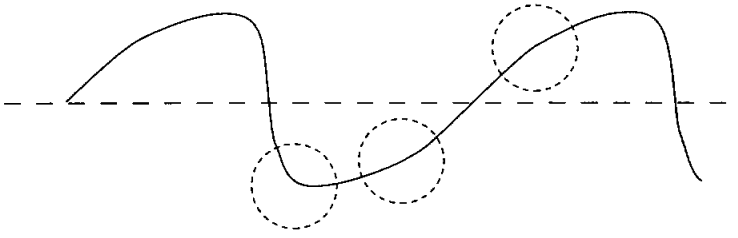
ap21 (68k/75)	1	1	1	1	1	0	0	0
80k/75	1	1	1	0	1	0	0	0

The waveform of the deflection current is compensated from Fig. (a) to Fig. (b) through the above. The starting section of the current is smoothened, and the linear section becomes the S type.

図(a)



図(b)



1.2.3 Vertical output circuit

The vertical deflection circuit controls the vertical width and vertical position with IC700 on the DEFL_SUB substract, and IC701 controls the linearity. Moreover, the signal output from IC701 is input to the vertical deflection output IC401.

1.3 High voltage circuit vlock

The high voltage circuit is composed of the high-voltage regulator H-IC601, flyback transformer (FBT) T601, operation amplifier IC602 and their peripheral circuits.

1.3.1 High voltage control

IC601 is an FBT drive H-IC unitized of the output MOS-FET (Q1) and its control section. Fig. 1 shows the block diagram. As the high voltage control system, the OFF trigger PWM control system is adopted. The OFF trigger control system turns OFF Q1 at the same time that when the horizontal sync. signal (hereafter called SYNC signal) input to Pin 13 (SYNC) of IC 601 is switched to Hi, in order to control the horizontal synchronization. The feedback signal (IC601 Pin 9) from FBT is compared with high voltage value setting voltage (IC601 Pin 10) from the MPU IC103 in the ErrAMP section in order to control the ON timing of Q1 (PWM control). Since the high-voltage detection voltage also drops when the high-voltage output voltage drops, the voltage of the capacitor CT of the ErrAMP section drops beyond the threshold value earlier than steady. Though Q1 is turned ON when it drops beyond the threshold value, the ON term of Q1 becomes longer than steady to increase the energy that generates the flyback pulse since the OFF timing of Q1 is synchronized with SYNC signal. (See Fig. 2.) As the result, the wave height value of the flyback pulse generated on the primary side of FBT increases to compensate for the dropped part of the high-voltage output voltage in order to achieve the stabilization. (27kV as normal)

1.3.2 Protective function

(1) Start and stop of high-voltage regulator IC601
When Vcc voltage (power voltage applied to Pin 8) reaches 10.4Vmin, IC601 outputs the drive pulse of Q1 to start the oscillation operation. Moreover, the drive pulse is fixed at Low to stop the oscillation operation when Vcc voltage (power voltage applied to Pin 8) becomes lower than 9.9Vmax (Vcc(La-off) voltage).

(2) IC601 pulse-by-pulse overcurrent protective (OCP) function
The peak value of drain current of MOS-FET (Q1) in IC601 is detected every pulse. When the voltage of Pin 17 of IC601 that detects both-end voltage of the source resistors (R607-R628) exceeds 0.75V, the DRIVE will be stopped until the next SYNC signal is input.

(3) IC601 overload protective (OLP) function
The function stops latching when it is continuously overloaded to continuously activate OCP. The time constant is generated by C609. When OCP is activated, C609 will be charged. When both-end voltage of C609 exceeds 5V, IC601 will come into the latch mode to stop the control operation. This state will not be released until the power SW is turned OFF (the voltage at Pin 8 of IC601 drops beyond Vcc (La-off) voltage).

(4) IC601 heat protective (TSD) function
When the frame temperature of the control IC section in IC601 exceeds 140°C (MIN), IC601 will come into the latch mode to stop the control operation. The state will not be released until the power SW is turned OFF (the voltage at Pin 8 of IC601 drops beyond Vcc (La-off) voltage).

(5) Overvoltage protective function of anode voltage (X-ray protector)
Voltage that is proportional to the high voltage value is generated in Pin 5 of T601 according to the coil ratio of the secondary coil and tertiary in FBT. The voltage is rectified by D612 and C621. Then, the voltage that is then divided by R636 and R637 is input to Pin 3 (+ terminal) of the operation amplifier IC602 in order to be compared with the X-PRO set voltage applied to Pin 2 (- terminal) from the MPU IC103. Though Pin 1 (output terminal) of IC602 is ordinarily Low (-15V output), Pin 1 (output terminal) becomes Hi (+12V output)

when the voltage at Pin 3 (+ terminal) of IC602 exceeds the voltage at Pin 2 (- terminal). Then, it is output to Pin 15 (X_PRO terminal) of IC601 via D605. When the voltage at Pin 15 of IC601 exceeds +5V, IC601 will come into the latch mode to stop the oscillation operation. The state will not be released until the power SW is turned OFF (the voltage at Pin 8 of IC601 drops beyond Vcc (La-off) voltage).

The overvoltage protective function is set to be activated when the high voltage value reaches 30.5kV.

(6) Beam current overcurrent protective function (beam protector)

The beam current is supplied through R617 from +12V power. Since the both-end voltage of R617 varies depending on the beam current value, the voltage drop caused by R617 becomes larger as the beam current increases. The voltage fluctuation is detected by Pin 6 of IC602, and is compared with the Beam-PRO set voltage that is input to Pin 5. The voltage of Pin 7 (output terminal) is linearly output against the voltage fluctuation caused by R619 and R620. However, IC601 comes into the latch mode to stop the oscillation operation when the terminal voltage of Pin 15 (X-PRO terminal) of IC601 exceeds +5V. The state will not be released until the power SW is turned OFF (the voltage at Pin 8 of IC601 drops beyond Vcc (La-off).)

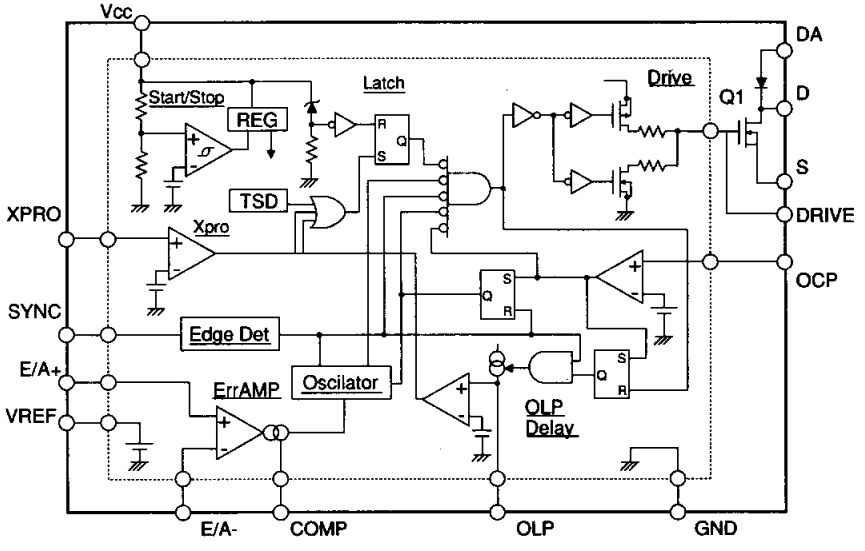
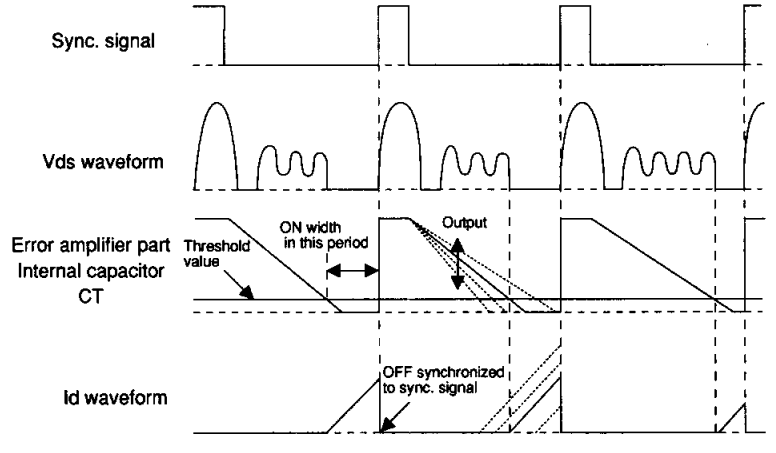


Figure 11. High voltage regulator IC601 block diagram



* The inclination of the capacitor CT changes with the output of error amplifier.
Q1 is turned ON when the capacitor voltage is lower than the threshold value.

Figure 12. OFF trigger PWM control system timing chart

1.3.3 DBF (Dynamic Beam Focus) circuit

Since the display is flattened, the focus becomes unequal between the center and circumference of the picture. To compensate for it, it is necessary to superimpose the parabola voltage of 370Vp-p in the horizontal cycle with the static focus and the parabola voltage of 145Vp-p in the vertical cycle. The slight voltage that is generated from the parabola voltage generating circuit is amplified and reversed to generate the high voltage in order to keep the focus equal. This circuit is called DBF circuit.

As shown in Fig. (b), the circuit is composed of the parabola voltage generating circuit IC700, amplifier section IC7A0 in the front step, Q6E1 to Q6E6 of amplifier section in the rear step, T6E1, and so on.

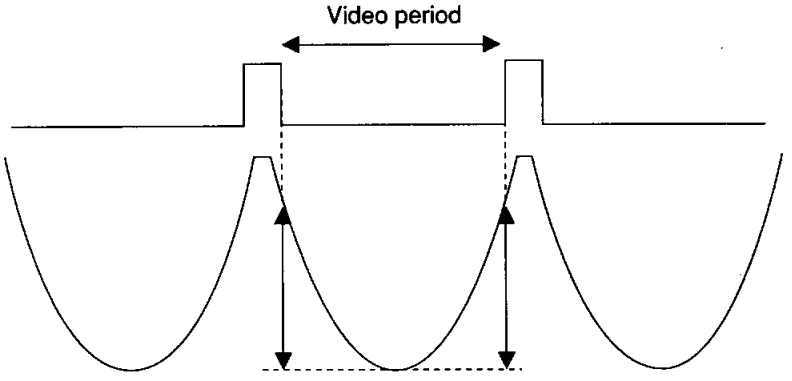


Figure (a)

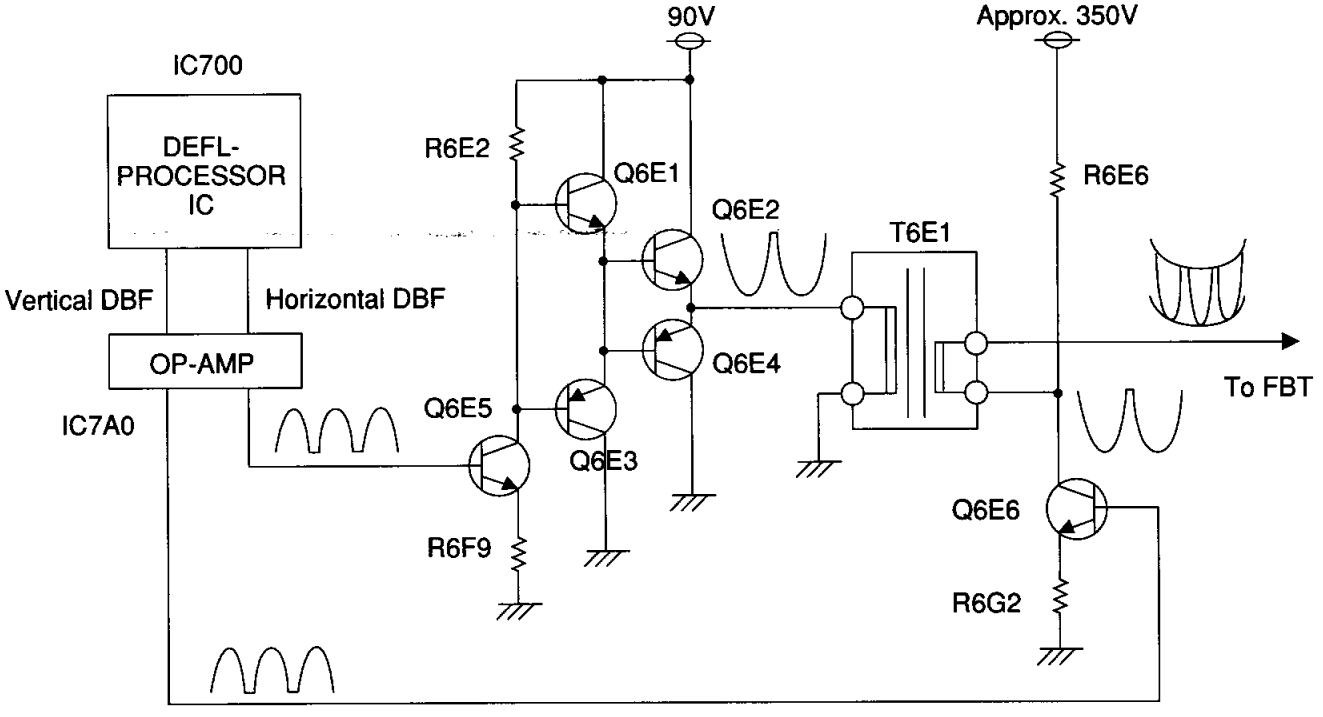


Figure (b)

After the horizontal and vertical DBF voltage are separately generated, they are amplified and are finally composed.

<Horizontal section>

The voltage (approx. 0.5Vp-p) of the parabola waveform shown in Fig. (a) is output from the deflection processor IC (IC700), and is amplified approx. 16 times by OP-AMP (IC7A0). Thereafter, it is amplified to 50 to 60Vp-p by the transistor (Q6E1 to Q6E5). The amplification ratio is determined by the ratio between the resistors R6E2 and R6F9, being approx. 8 times. Moreover, the waveform is reversed as shown in Fig. (b) at this time. Then, it is amplified to approx. 500Vp-p by DBF transformer (T6E1). The coil ratio between the primary and secondary coils of the DBF transformer is 1: 10, being the amplification ratio of approx. 10 times.

<Vertical section>

The voltage (approx. 0.6Vp-p) of the parabola waveform shown in Fig. (a) is output from the deflection processor IC (IC700), and is amplified approx. 13 times by OP-AMP (IC7A0). Thereafter, it is amplified to approx. 160Vp-p by the transistor (Q6E6). The amplification ratio this time is determined by the ratio between R6E6 and R6G2, being approx. 100 times.

The horizontal and vertical DBF voltages amplified and reversed are composed by applying vertically synchronous modulation to the output on the secondary side as shown in Fig. (c). The composed voltage is input to Pin 12 of the flyback transformer (T601).

Figure (a)

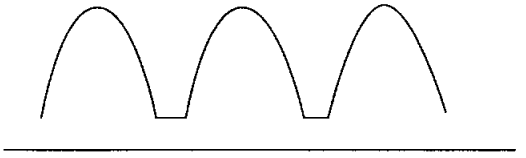


Figure (b)

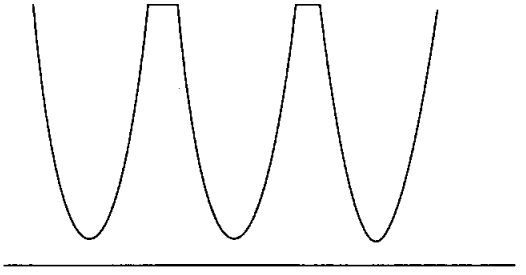
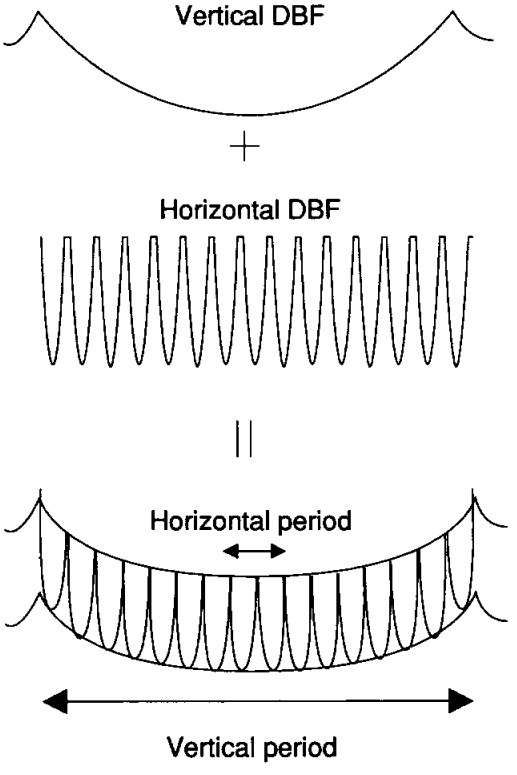


Figure (c)



1.4 Control circuit block

1.4.1 Rotation circuit

The rotation circuit is a circuit to compensate the picture inclination caused by the earth magnetism by letting DC current flow to the rotation coil wound on the front side of DY for adjustment. It is controlled to 0 to 5V with the reference of 2.5V by IC103#4(PWM_DAC), and DC current of +/-110mA (max) is made to flow to the rotation coil by IC8A4#2.

1.4.2 Corner purity circuit

The corner purity circuit is a circuit to compensate for the color shade and color deviation of the picture corner. On the rear side of CRT, it is adjusted by DC current flowing to the corner purity coils installed in the four corners on the display surface.

The compensation circuit is composed of the following three functions of (1) User (automatic adjuster) adjustment (OSD display), (2) Aging variation compensation and (3) High/low temperature drift compensation.

(1) User (automatic adjuster) adjustment (OSD display)
The user (automatic adjuster) causes DC current of +/-60mA (max.) to flow to the purity coil of each corner according to the value displayed on OSD.

(2) Aging variation compensation
As the electronic beam collides with the aperture grille, it is thermally expanded and contracted. The thermal expansion/contraction is varied according to the elapse of the power ON/OFF time of the monitor. The color shade and deviation of the picture corner thus generated are automatically adjusted.
The voltage of the beam current supply pin (FBT #10) is detected with R629/R630, and the voltage that detects the time elapse of the power ON/OFF of the monitor is read from the CR charge (integration) circuit composed of C127 and R141 and Cr discharge circuit (integration) circuit through IC100 (buffer amplifier) by IC103#15(CPU_ADC), and the DC current of +/-19mA(max) flows to the purity coil on each corner according to the specified control program.

(3) High/low temperature drift compensation
The front panel (glass) is thermally expanded and contracted as the temperature varies in the installation environments of the monitor. The color shade and deviation of the picture corner are automatically adjusted. The voltage that detects the temperature variation of the installation environments of the monitor is read from the environment temperature detection circuit composed of TH100 (thermistor) arranged near the front panel (glass) by IC103#13(CPU_ADC), and DC current of +/-11mA (max) is made to flow to the purity coil on each corner according to the specified control program.

- The left upper corner on the display surface is controlled with 0 to 5V of 2.5V reference by IC8A0#1(I2C control_DAC), and the DC current of the above value is made to flow to the purity coil on the left upper corner by IC8A3#2.
- The right upper corner on the display surface is controlled with 0 to 5V of 2.5V refer ence by IC8A0#2(I2C control_DAC), and the DC current of the above value is made to flow to the purity coil on the right upper corner by IC8A3#8.
- The left lower corner on the display surface is controlled with 0 to 5V of 2.5V reference by IC8A0#3(I2C control_DAC), and the DC current of the above value is made to flow to the purity coil on the left lower corner by IC8A2#2.
- The right lower corner on the display surface is controlled with 0 to 5V of 2.5V reference by IC8A0#4(I2C control_DAC), and the DC current of the above value is made to flow to the purity coil on the right lower corner by IC8A2#8.

1.4.3 Earth magnetism canceler circuit

The earth magnetism canceler circuit is divided into the south-north horizontal magnetic field canceling function and vertical magnetic field canceling function.

IC303 (earth magnetism sensor unit) detects the voltage and direction of the south-north horizontal magnetic field (IC303#2) and vertical magnetic field (IC303#1), and IC103#14 and 18(CPU_ADC) read the detected voltage to automatically control the following canceling function according to the specified control program.

Here, the output voltage of IC303 (earth magnetism sensor unit) operates as follows.

- South-north horizontal magnetic field (IC303#2): 0.5V(-0.04mT) to 2.5V(+/-0.00mT) to 4.0V(+0.04mT)
- Vertical magnetic field (IC303#1): 3.3V(-0.04mT) to 2.5V(+/-0.00mT) to 0.1V(+0.10mT)

<South-north horizontal magnetic field canceling function>

(a) Horizontal magnetic field landing cancel

The horizontal magnetic field landing cancel circuit is a circuit to compensate for the color shade and deviation that appear in the horizontal direction that becomes the opposite direction at the upper and lower ends on the monitor display surface, and the automatic adjustment is done by DC current flowing to the purity coil that is wound around the display surface. It is controlled to 0 to 5V of 2.5V reference by IC103#5(PWM_DAC) in order to cause the DC current of +/-90mA(max.) to flow to the purity coil from IC8A1#4.

(b) Horizontal magnetic filed convergence cancel

The horizontal magnetic field convergence cancel circuit is the circuit to compensate for the misconvergence that results after the vertical convergence of RED and BLUE in the whole display area of the monitor deteriorates, and it is automatically adjusted by DC current flowing to the 4V convergence compensation coil mounted on DY. It is controlled with the DC component (V-CONVERGENCE) by IC700#60(4V_SC), and DC current of +/-30mA (max) is flowen to the 4V convergence compensation coil by IC800#6 (PowerOpamp).

<Vertical magnetic field canceling function>

(a) Vertical magnetic field landing cancel

The vertical magnetic field landing cancel circuit is the circuit to compensate for the color shade and deviation that reaches its maximum at the center in the horizontal axis direction and its minimum at the upper and lower ends on the monitor display surface, and the automatic adjustment is done by DC current flowing to the speed modulating coil installed in the neck part of CRT.

It is controlled with 0 to 5V of 2.5V reference by IC103#6(PWM_DAC), and DC current of +/-140mA (max) is made to flow to the speed modulating coil by IC8A4#8.

(b) Vertical magnetic filed convergence cancel

The vertical magnetic field convergence cancel circuit is the circuit to compensate for the misconvergence that results after the vertical convergence of RED and BLUE reversed at the upper and lower ends on the whole display area of the monitor deteriorates, and it is automatically adjusted by the saw-toothed waveform (vertical frequency) current flowing to the 4V convergence compensation coil mounted on DY. It is controlled with the AC component (YVJT & YVJB, vertical frequency saw-toothed waveform) by IC700#60(4V_SC), and saw-toothed waveform (vertical frequency) current of +/-45mA (peak) is made to flow to the 4V convergence compensation coil by IC800#6(PowerOpamp).

1.4.4 Digital dynamic convergence clear (DDCD) circuit

In the digital dynamic convergence clear (hereafter called DDCC) circuit, the convergence compensating current waveform is produced and amplified, and the convergence is compensated by the compensation current flowing to the sub yoke that is installed as the rear unit of the deflection yoke.

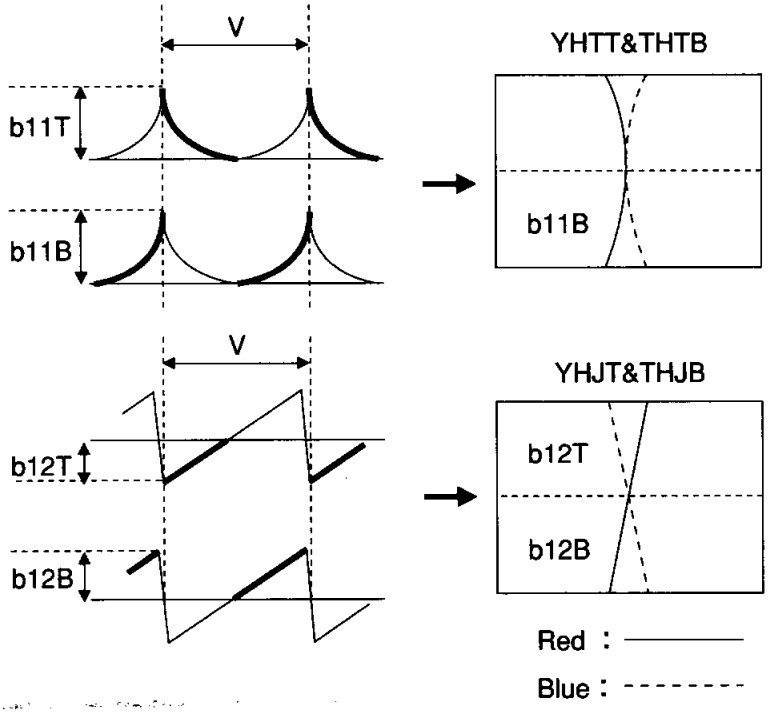
Though the principle of the convergence compensation with the sub yoke is same as the CP ring, the CP ring is used for the static variation with the parallel movement in the whole picture in the uniform magnetic field with the permanent magnet but the sub yoke is used for dynamic variation that compensates a desired position on the picture by controlling the current waveform that flows to the coil of the electric magnet.

(See Fig. 13)

(1) Production of compensation current waveform

There are 18 kinds of compensation elements, and they are programmed in IC700(μPD61882) one by one by using the functions. The amplitude of the current is controlled by inputting the compensation coefficient into the function.

YHTT= b11T·y^2
YHTB= b11B·y^2
YHJT= b12T·y
YHJB= b112B·y
YHT=b11T·y^2+b11B·y^2
YHJ=b12T·y+b12B·y
↓
4H_SC=all·(YHT+YHJ)



Examples of the functions and current waveform/compensation operation of YH(YHTT, YHTB, YHJT, YHJB) are shown as follows.

In the above formulas, b11T, b11B, b12T and b12B express the compensation coefficients, and y and y^2 express the primary and secondary functions of the vertical frequencies. The other parts except the compensation coefficients are programmed, and desired amplitudes (= compensation amount) are gained by varying the coefficients.

YHTT and YHTB compensate the upper and lower parts of the picture of the characteristic components of their DYs to compensate the upper and lower parts of the picture of the axis deviation component. The component gained by adding YHT and YHJ is multiplied by the offset compensation coefficient a11. The resultant component is regarded as 4H_SC, and is output from IC700(μPD61882)#61.

(2) Waveform, and operation on the picture

The case in which the currents flow through 4H coils of the sub yoke is explained. Regarding YHT (secondary function in the vertical frequency), in case of Fig. 1 as an example, the current is large in the same direction at the start (upper end of the picture) and the end (lower end of the picture) of the vertical frequency, and is zeroed on the X axis of the picture. Therefore, the magnetic field that is proportional to it is generated, and RED and BLUE vary in the same direction only at the upper and lower ends of the picture. As aforementioned, YHT can be independently controlled at the upper part (b11T.y^2) and lower part (b11B.y^2).

Moreover, regarding YHJ (vertical frequency primary function), if the flowing direction of the current is opposite at the start (upper end of the picture) and the end (lower end of the picture) of the vertical frequency as an example, RED and BLUE vary in the opposite direction only at the upper and lower ends of the picture. Compensation in the vertical direction can be done by making the current flow to the 4V coil.

Fig. 14 shows the image of each adjustment item of the DDCC adjustment.

(3) Adjustment method

Before the adjustment with the compensation circuit, it is necessary that they are properly adjusted at the center (H-STATIC and V-STATIC), on the X axis (XH slider, B-Bow 4P, XV differential coil) and on the Y axis (YH volume, YV volume).

Though DC current is superimposed on the sub yoke, H-STATIC and V-STATIC are pushed to the greatest possible extent by the adjustment with CP ring in order to reduce the stress of the driver IC800 (STK39-110).

Moreover, since 4H and 4V coils alone are installed on the chassis, it is first necessary that the convergence of RED, BLUE and GREEN (6H, 6V) satisfy the specifications for the performance of ITC(CRT&DY).

As the adjustment procedure, the adjustment values of 18 elements are not respectively zeroed but they are adjusted to nearest to zero with a total balance in good order.

In other words, the balance (compromise) adjustment with each adjustment item is applied.

The correspondence of the names of DDCC adjustment mode to the coefficients of all 18 elements is shown below.

<Factory mode>

4H Coil	b11T	YHTT	y^2	b11B	YHTB	y^2	b12T	YHJT	y	b12B	YHJB	y
	b21	4HTL	x^2·y^2	b31	4HTR	x^2·y^2	b41	4HBL	x^2·y^2	b51	4HBR	x^2·y^2
4V Coil	c11T	YVTT	y^2	c11B	YVTB	y^2	c12T	YVJT	y	c12B	YVJB	y
	c21	4VTL	x^2·y^2	c31	4VTR	x^2·y^2	c41	4VBL	x^2·y^2	c51	4VBR	x^2·y^2

<User & Factory mode>

4H Coil	a11	H-CONVERGENCE	DC
4V Coil	a12	V-CONVERGENCE	DC

(4) Block diagram

Fig. 15 shows the block diagram of the DDCC circuit.

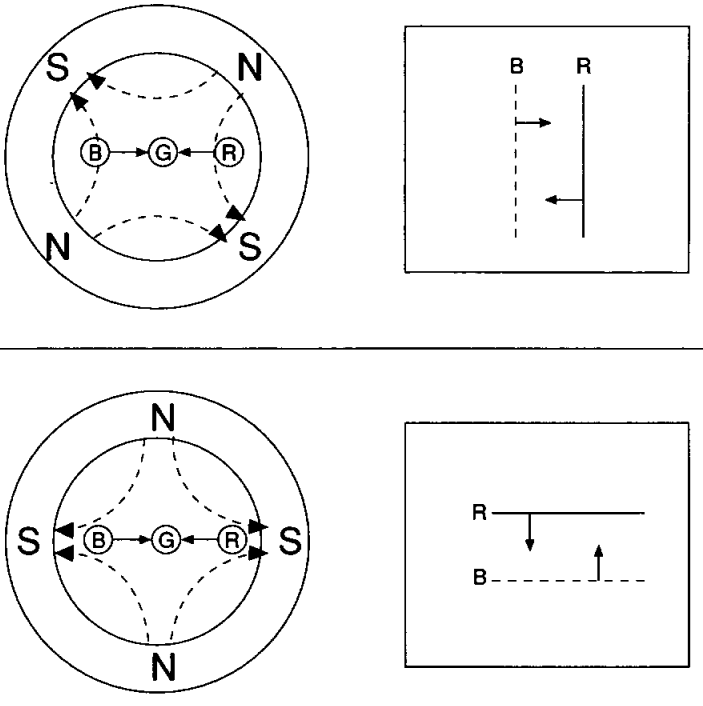
The components 4H_DC(#6), 4H_SC(#61), 4V_DC(#8) and 4V_SC(#60) supplied from IC700(μPD61882) to 4H-Coil and 4V-Coil are output, the dynamic component (4H_DC, 4V_DC) is amplified with IC7A0(TL084), and the static component (4H_SC, 4V_SC) is amplified with IC7A2(KIA4588).

DCC(#7) output from IC700(μPD61882) and DEFL_+3.3V(#3) output from IC702 (TA48M033F) are respectively the reference voltage of Op-Amp(IC7A0:TL084) that amplifies the above dynamic component (4H_DC, 4V_DC) and the reference voltage of Op-Amp(IC7A2:KIA4558) that amplifies the static component (4H_SC, 4V_SC).

On each of 4H and 4V, the waveform added with the dynamic component and static component is input to IC800#3 and 4(STK391-110) allow the specified current to flow to each convergence compensation coil.

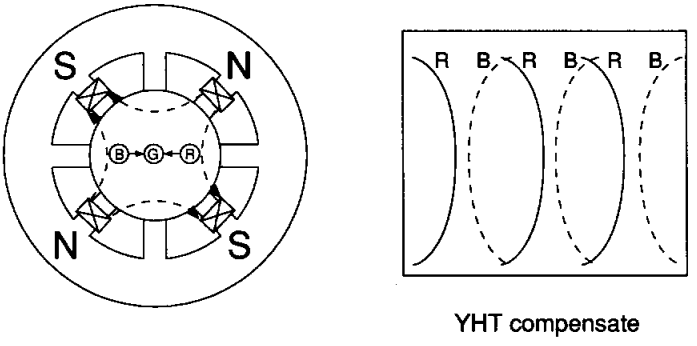
For four poles magnetic field

Static change by
the eternal magnetic field
(Parallel shifting totally)



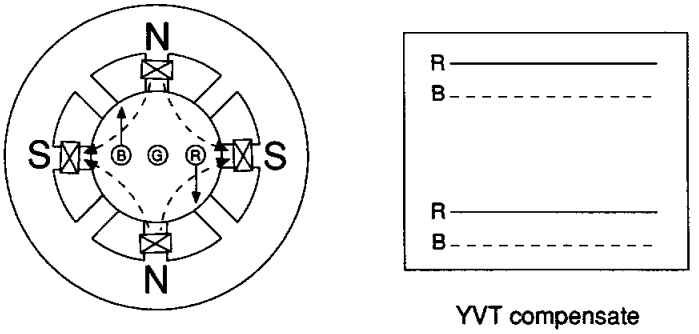
Dynamic change by
electromagnet
(Compensate at the
optional position on the picture.)

4H coils



YHT compensate

4V coils



YVT compensate

Figure 13

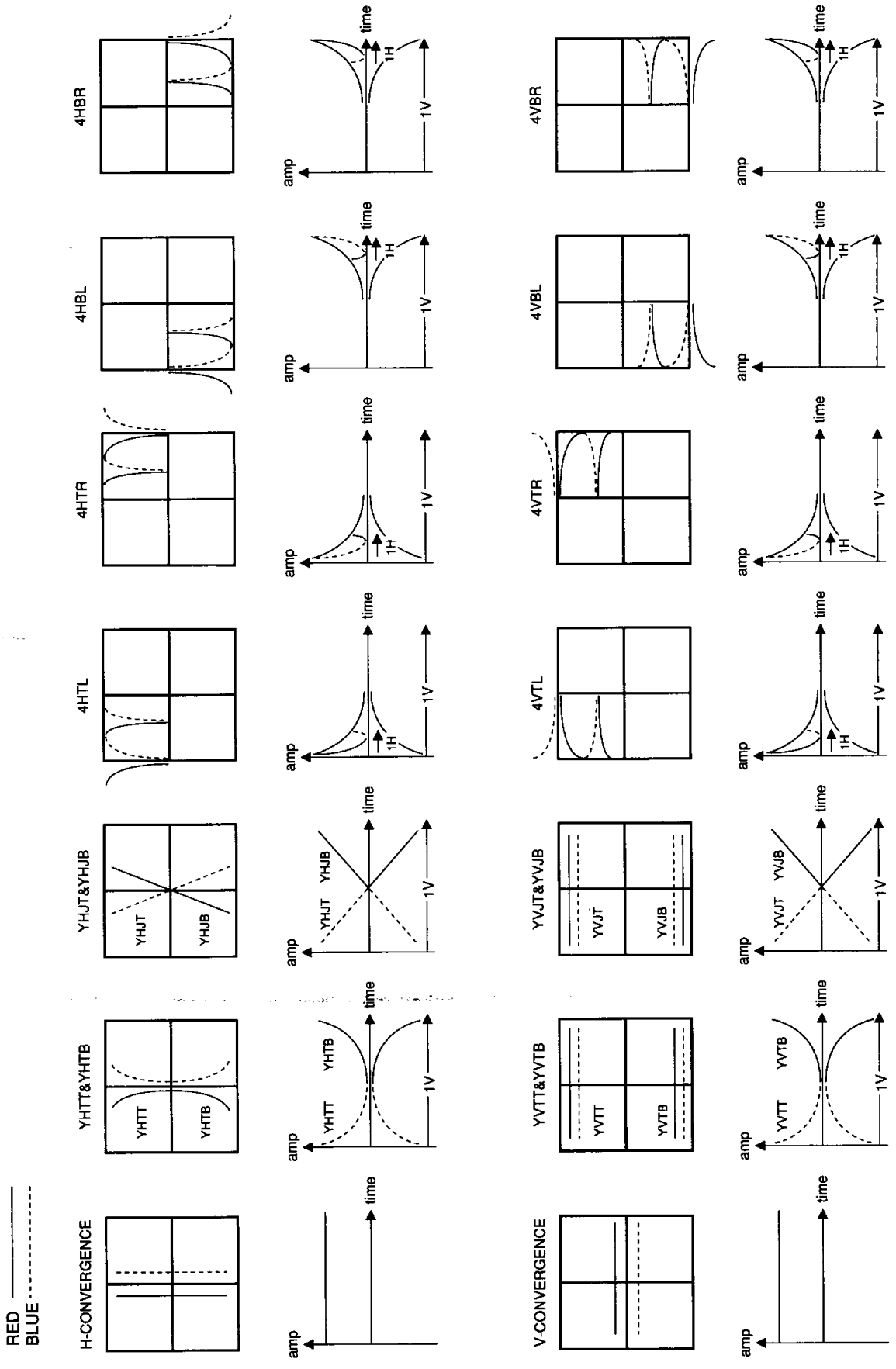

RED
BLUE
H-CONVERGENCE
YHTT&YHTB
YHJT&YHJB
4HTL
4HTR
4HBL
4HBR
V-CONVERGENCE
YVTT&YVTB
YVJT&YVJB
4VTL
4VTR
4VBL
4VBR
YHTT
YHTB
YHJT
YHJB
YVTT
YVTB
YVJT
YVJB
amp
time
1H
1V

Figure 14

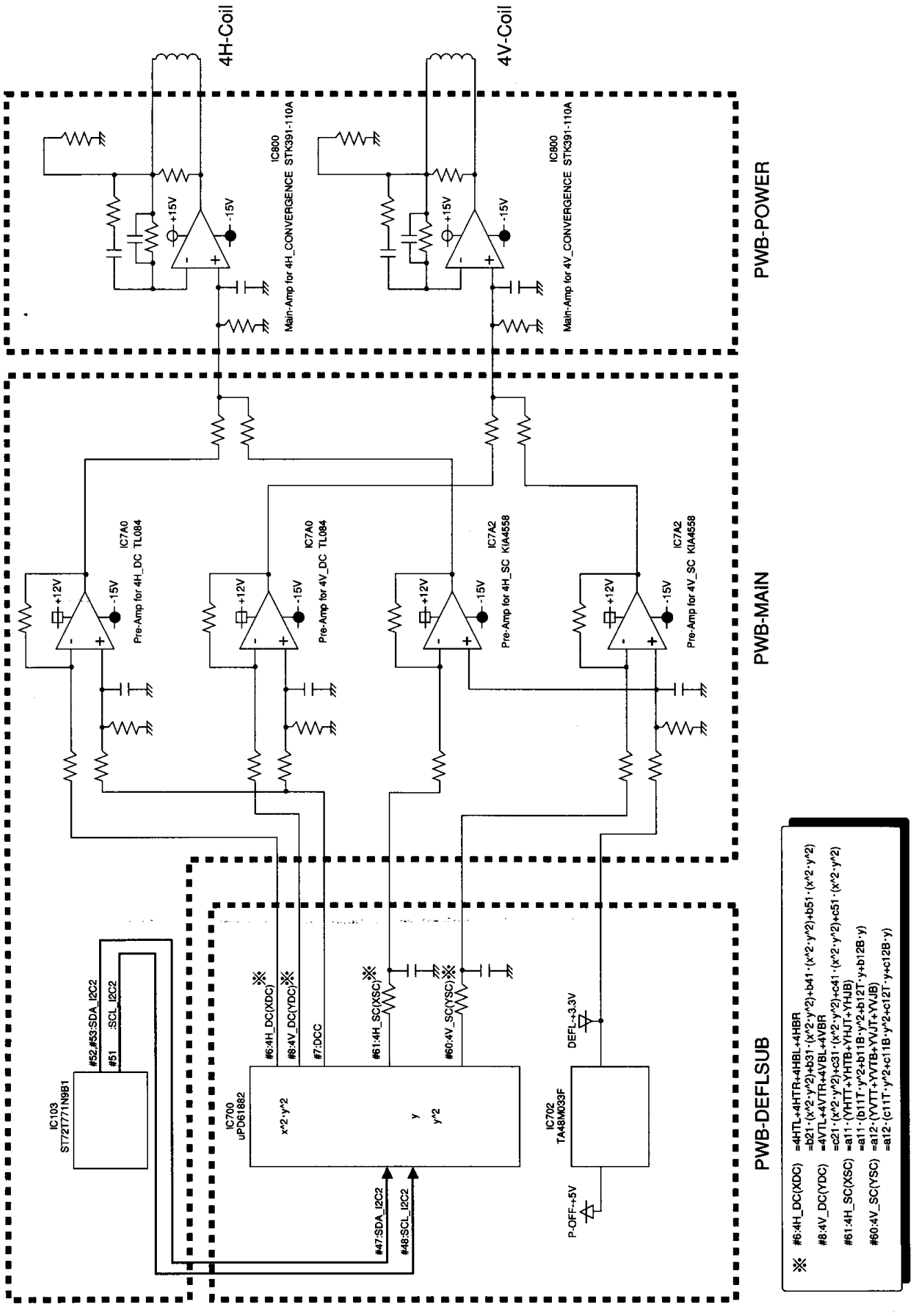

4H-Coil
4V-Coil
IC800
Main-Amp for 4H_CONVERGENCE STK391-110A
Main-Amp for 4V_CONVERGENCE STK391-110A
+15V
-15V
PWB-POWER
IC7A0
Pre-Amp for 4H_DC TL084
Pre-Amp for 4V_DC TL084
IC7A2
Pre-Amp for 4H_SC KIA4558
Pre-Amp for 4V_SC KIA4558
+12V
PWB-MAIN
IC103
ST72T771N9B1
#52,#53:SDA_I2C2
#51 :SCL_I2C2
IC700
uPD61882
#6:4H_DC(XDC)
#8:4V_DC(YDC)
#7:DCC
#61:4H_SC(XSC)
#60:4V_SC(YSC)
x^2·y^2
y
y^2
#47:SDA_I2C2
#48:SCL_I2C2
DEFL+3.3V
IC702
TA48M033F
P-OFF-+5V
PWB-DEFLSUB
※ #6:4H_DC(XDC) =4HTL+4HTR+4HBL+4HBR
=b21·(x^2·y^2)+b31·(x^2·y^2)+b41·(x^2·y^2)+b51·(x^2·y^2)
#8:4V_DC(YDC) =4VTL+4VTR+4VBL+4VBR
=c21·(x^2·y^2)+c31·(x^2·y^2)+c41·(x^2·y^2)+c51·(x^2·y^2)
#61:4H_SC(XSC) =a11·(YHTT+YHTB+YHJT+YHJB)
=a11·(b11T·y^2+b11B·y^2+b12T·y+b12B·y)
#60:4V_SC(YSC) =a12·(YVTT+YVTB+YVJT+YVJB)
=a12·(c11T·y^2+c11B·y^2+c12T·y+c12B·y)

Figure 15

1.5 Control block

The control block is composed of the following:
Monitor MPU IC103 to process the sync. signals, control the inside of the monitor and communicate with the external, EEPROM IC105 to memorize the picture adjustment values, etc., I/O expander IC102 to convert the serial data of I2C bus to the CS switch signal, and others.

1.5.1 Sync. signal process

When GSYNC of the separated image signals is input from the interface board to the MPU #30 as HSYNC or composite SYNC and to #20 as VSYNC, the frequency/polarity of SYNC will be discriminated. Then, HS_OUT will be output from #27 for beam deflection and OSD display and VS_OUT will be output from #26 as the polarity POSI.
If Separate, Composite and Sync on Green are input at the same time, they will be recognized in the sequence of Composite, Separate and Sync on Green from the highest priority.
If SYNC is not input or abnormal SYNC is input, the MPU will output simulative SYNC. The frequency of the simulative SYNC is near that of the previously input SYNC.
(Initial values: FH:31KHz and FV:75Hz)
If anything other than GSYNC is input, S/GSEL signal of #25 will be set at LOW and GSYNC input will be cut.

1.5.2 Front button

When a tact switch SW100 on the front panel is pressed, the voltage of +5V will be divided with the resistor according to the button.
The signal is converted into the digital value with the A/D converter of the MPU #12 to discriminate which button is pressed.

1.5.3 I2C bus control

For IC control in the monitor, I2C bus of two systems of I2C_1(#36:SCL, #37:SDA) and I2C_2 (#51:SCL, #52:SDA) is used. The adjustment data is read from EEPROM according to the input timing, and is sent to each IC.

Slave address list

[I2C-1]

Item	Source	ADR(BIN)
Preamplifier	IC301	10001000
OSD	IC300	01111100
DAC (Cut off)	IC305	10011000

[I2C-2]

Item	Source	ADR(BIN)
E2PROM	IC105	1010000*
Dflection processor	IC700	11011100
I/O expander (CS)	IC102	01110000
DAC(CPURITY)	IC8A0	10011000

1.5.4 Power control

The normal state and power management state are switched according to #17 P-OFF signal and #21 P-SUS signal.
"Power save" of the OSD adjustment item is turned to "ON", and the power management is activated when either H/VSYNC goes out.
In the power management mode, P-OFF+5V is turned OFF by setting #17 P-OFF signal at LOW, other power supplies except +5V and heater are turned OFF by setting #21 P-SUS signal at LOW.

Moreover, if #19 PRO signal is at H1 1 second or more, it will be regarded as a short circuit of the power of the secondary side to forcibly turn ON POWER SAVE in order to prevent trouble from being escalated.

1.5.5 CRT support

The voltage conversion signal is output from the earth magnetism sensor IC303: horizontal magnetic field from #2 and vertical magnetic field from #1. It is relayed through the reversal buffer: the horizontal magnetic field signal is input to A/D converter of the MPU IC103 #14 and the vertical magnetic field is input to the A/D converter of IC103 #18. The signal is converted to the digital value to detect the earth magnetism around the monitor.
The signal generated by dividing +5V with the thermistor TH100 and R111, R112 is input to A/D converter of IC103 #13, and is converted to the digital value. This detects the temperature in the monitor.
The monitor energization time signal is relayed through the buffer of IC100, is input to the A/D converter of IC103 #15, and is converted to the digital value. This detects the monitor energization time.
To cancel the purity and convergence from degradation due to the above earth magnetism, temperature and aging, the cancel current is flowen to H_PURITY, V_PURITY, C_PURITY and 4V coil.
H_PURITY is controlled by the signal that is gained by smoothening PWM DAC output of IC103 #5 with R119 and C110.
V_PURITY is controlled by PWM DAC output of IC103 #6. C_PURITY is controlled by the signal of the analog voltage that IC8A0 converts from the digital signal sent from the MPU to 4-channel DAC IC8A0 through the 12C bus.
The convergence 4V is controlled by the #60 output signal of the analog voltage that IC700 converts from the digital signal sent to the deflection processor IC700 through 12C bus from the MPU.

1.5.6 High voltage control

The high-voltage output voltage is controlled by the signal HV-ADJ that is passed through the buffer of IC104 after PWM DAC output of the MPU IC103 #2 is smoothened with R116 and C109.
Similarly, X ray protect voltage is controlled by the signal X-PRO_ADJ that is gained by passing PWM DAC output of IC103 #3 through the buffer of IC104.

1.5.7 Display Data Channel

Both SIGNAL A/B support DDC1/2B.
The DDC function of SIGNAL A is supported by IC201(EEPROM for DDC) on the interface board. EDID written in IC201 is output according to the clock that is input to #6 SCL or #7 VCLK of IC201.
The DDC function of SIGNAL B is supported by IC103 (MPU). Soon after the power of the monitor is turned ON, the MPU reads EDID from IC105. According to the clock input to #34 SCL or #20 VSYNC(VCLK), EDID is output.

1.5.8 USB monitor control

The serial data bus of J1A3(USB connector B) is connected to #41 DATA- #42 DATA+ of IC103 (MPU).
The MPU IC103 #43 is +3.3V power output for USB, and DATA- is pulled up with +3.3V.

This makes the MPU communicate with the personal computer in the direct USB mode. For the monitor control, it is necessary to install the application Diamond Control for USB version 4.0.3 or more on the personal computer.

IC103(MPU)Pin assingnment

PIN#	FUNCTION	ASSIGNMENT	PIN#	FUNCTION	ASSIGNMENT
1	DA0	SUB_BRT	56	VPP/TEST	GND
2	DA1	HV_ADJ	55	IRIN	GND
3	DA2	X-PRO_ADJ	54	RESET	RESET
4	DA3	ROTATION	53	PA0	SDA_I2C2
5	DA4	HCANCEL	52	PA1	SDA_I2C2
6	DA5	VCANCEL	51	PA2	SCL_I2C2
7	DA6	SW_LIN2	50	PA3	HSK
8	DA7	not used	49	PA4	WC
9	DA8	not used	48	PA5	not used
10	VSSA	GND(A)	47	PA6	not used
11	VDDA	+5V(A)	46	PA7/BLANKO	not used
12	PB7	KEY	45	OSCIN	OSCIN
13	PB6	THERM	44	OSCOUT	OSCOUT
14	PB5	X_OUT	43	USBVCC	USBVCC(3.3V)
15	PB4	BEAM	42	USBDP	USBDP
16	PB3	ACC	41	USBDM	USBDM
17	PB2	P-OFF	40	USBGND	USBGMD
18	PB1	Y_OUT	39	PC7/TDO(SCI)	SW_LIN1
19	PB0/VFBACK	PRO	38	PC6/RDI(SCI)	SDA_I2C1
20	VSYNCI1	VSYNC	37	PC5/SDAI(I2C)	SDA_I2C1
21	PD7/VSYNCI2/ITD	P_SUS	36	PC4/SCLI(I2C)	SCL_I2C1
22	PD6/CLAMPO	CLP	35	PC3/SDAD(DDC)	SDA_DDC
23	PD5/ITA	SPARK	34	PC2/SCLD(DDC)/RX	SCL_DDC
24	PD4/ITB	LOCK	33	PC1/HSYNCI2	SEL
25	PD3/ITC	S/G_SEL	32	PC0/OCMP/HFBACK	DEG
26	PD2/VSYNCO	VS_OUT	31	VDD	+5V(D)
27	PD1/HSYNCO	HS_OUT	30	HSYNCI1	HSYNC
28	PD0/CSYNCI	GSYNC	29	VSS	GND(D)

IC102(I/O expander) pin assignment

Signal name	PIN#
CS1	10
CS2	11
CS3	5
CS4	6
CS5	9
CS6	7
CS7	12
LIN	4

IC8A0(Corner purity DAC) pin assignment

Signal name	PIN#
CP-TL	1
CP-TR	2
CP-BL	3
CP-BR	4

1.5.9 LED

J100 #1 is connected to the anode of the green LED, J100 #3 is connected to the anode of the amber LED, and #2 is connected to the cathodes of both. Since +12V is normally supplied, the current flows to J100 #1 to turn OFF Q100. Therefore, any current does not flow to J100 #3. (The green LED only is lit.)

Since +12V is turned OFF in the power management mode, no current is not flowed to J100 #1 to turn ON Q100. Therefore, the current flows to J100 #3. (The amber LED only is lit.)

1.5.10 Clamp pulse

The clamp pulse signal CLP is output from #22 of the MPU IC103 #22 by the polarity POSI. When "FRONT" is selected in the OSD adjustment item "CLAMP PULS POSITION", the signal is triggered at the front edge of HSYNC, and when "BACK" is selected, the signal is triggered at the rear edge.

1.5.11 SPARK

If it is electrically discharged in the CRT tube, the GND level of the high-voltage system circuit is considerably varied. GND of this high-voltage system is connected to the MPU IC103 #23 via C137. The voltage level of IC103 #23 is normally set at HI. If GND in the high-voltage system varies since it is electrically discharged in the CRT tube, the current will flow to R168 to set IC103 #23 at the LO level. #23 is the external interrupt terminal that detects the trailing edge. When the trailing edge is detected, the MPU forcibly applies S/W RESET. (It is the same as when the power SW is turned ON.)
The above operation prevents the monitor from going out of control when it is electrically discharged in the CRT tube.

1.5.12 Avoidance operation during input SYNC switching

The horizontal LOCK output signal of the deflection processor IC700 #46 is connected to the MPU IC103 #24. JC103 #24 is the external interrupt terminal of the trailing edge detection. Though the voltage level of the LOCK signal is normally set at HI, IC700 outputs LO when the horizontal deflection lock is released since the input SYNC is switched.
When the MPU detects the trailing edge, the HSK signal of IC103 #50 is set at HI, and the simulative SYNC that is near the original frequency is output from #30 and #20. HSK signal is used to set +B, H-FOCUS voltage at MIN.
This reduces the stress when the input SYNC is switched for a short time.

1.5.13 Vertical linearity switch

The frequency characteristics of the vertical linearity are compensated by #39 SW_LINI and #7 SW_LIN2 output signals of the MPU IC103.
The switching patterns are shown in the table below.

SW_LIN1, SW_LIN2 select pattern

Vertical frequency	VLIN_SW1 #39	VLIN_SW2 #7
50Hz~73Hz	LO	LO
73Hz~90Hz	HI	LO
90Hz~125Hz	LO	HI
125Hz~160Hz	HI	HI

1.5.14 H/W RESET

The +5V power is connected to #2 of the voltage detector IC101, and IC101 #1 output is connected to the MPU IC103 #54.
On the voltage detector, #1 is the open drain output, being turned OFF when #2 voltage is 4.5V or more, and ON when it is 4.5V or less. When the power switch is turned ON, IC101 #1 is turned ON and the MPU #54 level is set at 0V since +5V has not started up.
When the voltage of IC101 #2 becomes 4.5V or more, IC101 #1 will be turned OFF, and the voltage of the MPU #54 rises with the time constants of R107 and C106.
When the voltage of the MPU #54 becomes 3.5V or more, the MPU will start operating.

1.5.15 Oscillation circuit

The crystal oscillator X100 is connected to the MPU IC103 #45 and #44. #45 is the clock input, and #44 is the amplification circuit output in the MPU. The operation frequency of the crystal oscillator is 24MHz. The basic clock is divided in the MPU to operate the program and circuits of the MPU.

1.6 Software

1.6.1 Outline

(1) Input frequency
- •Horizontal : 30KHz to 108KHz (Lower limit : 29.5KHz, Upper limit: 110KHz)
- •Vertical : 50KHz to 160Hz (Lower limit: 45Hz Upper limit: 162Hz)

(2) Memory timing number
- •Preset timing : 9 timing (22 timing max.)
- •User timing : 15 timings can be memorized.

1.6.2 Frequency variation detection function

When the normal signal is input, the input frequency and polarity are checked every input of VSYNC. If they satisfy the conditions a, b and c, it is judged that the input signal varies. When input signal variation is detected, the directory data written in EEPROM and the directory data of the input signal are compared with each other in the following sequence, and the picture data are read and output.

(1) If the input signals satisfy conditions a, b and c, they are judged to be the same as the signals registered in the directory, and the timing data are read from EEPROM and are output.
Condition a: The polarities of the input sync. signal are the same in both horizontal and vertical directions.
Condition b: Horizontal frequency difference is 0.6KHz
Condition c: Vertical frequency difference is 0.6Hz.

The sequence of the compared directories is as follows:
PRESETO–>PRESET1–>•••–>PRESET21–>USER0–>USER1–>•••–>USER14
f the same timing is judged on the way, the comparison work is stopped there, and the adjustment value for each corresponding timing is read out from EEPROM.

(2) If the conditions of (1) are not satisfied (when the new timing is input), the horizontal frequency reads the backup picture data of the nearest preset timing and outputs it.

1.6.3 Memory of user timing

The new timing is input. When the picture adjustment is executed, the directory data (frequency and polarity) and picture data will be memorized in EEPROM.
If 15 user timings (MAX) are memorized, the memory of the oldest user timing (directory data and picture data) is deleted, and the new timing information is memorized there.
USER0–>USER1–>•••–>USER14–>USER0–>USER1–>•••

1.6.4 Picture adjustment

(1) The monitor has the function to do the picture adjustment with OSD and communication.
The function has the following adjustment modes.
a: Normal mode
b: Factory mode
For entry into each adjustment mode, refer to Item "Adjustment method".

(2) High voltage adjustment supplement
The high voltage of the normal time is determined with "HVAD" setting value of OSD adjustment item and the X-ray protect voltage is determined with "XPRO" setting value of the OSD adjustment item. To adjust the X ray protect voltage, it is necessary to raise the high voltage to 30KV once.
To temporarily raise the high voltage, "HVTP" of OSD adjustment item is used. Since "HVTP" is not memorized in EEPROM, the high voltage will return to the normal ("HVAD" setting value) when the power is turned OFF once. Even if the page of the high voltage adjustment of OSD is skipped with the Ø button, it will similarly return to the normal high voltage.

(3) If XRAY-PROTECT activates even in the normal state because XRAY-PROTECT is excessively lowered by mistake, the XRAY-PROTECT and HV-ADJUST adjustment values can be initialized using the following procedure.

(a) Input the image signal to the monitor.

(b) Keeping both + and - buttons pressed, turn ON the power.

(c) Keep both + and - buttons pressed 20 seconds or more. (Approx. 30 seconds)

(d) Release - button only.

(e) Keep the + button only pressed 10 seconds or more.

(f) When it is successfully completed, the monitor will drop to POWER SAVE approx. 10 seconds. (LED becomes amber.)

(g) Turn OFF the power, and turn it ON again, and the XTRAY-PROTECT adjustment value will become 254 and HV-ADJUST adjustment value will become 0.

(4) Vertical position adjustment supplement
The adjustment data that displays OSD adjustment item "VERT-POSITION" is different between the normal mode and factory mode. Therefore, even if "VERT-POSITION" is set at 127 (middle) in the factory mode, "VERT-POSITION" does not always show 50% when it is returned to the normal mode.
Operation of "VERT-POSITION" is not followed up in the factory mode though the trapezoidal distortion compensation is automatically followed up in the normal mode.

1.6.5 Power management

The function reduces the power consumption of the monitor when the connected computer is not used.
The function is turned ON and OFF from the adjustment picture.

The monitor has only one kind of the power management function.

(1) Conditions to enter power management mode
a: "POWER SAVE" of the picture adjustment item is left ON.
b: Neither HSYNC nor VSYNC are input.
* Not that if the image signal GREEN is input when neither HSYNC nor VSYNC is input, the power management can not be activated since it wrongly recognizes that Sync On Green is input.

(2) Power management operation
When the power management is activated,
(i) P_SUS signal is turned to LO to stop the power output on the secondary side except CRT heater, P-OFF+5V, +5V line.
(ii) P-OFF signal is turned to LO to stop the power output of P-OFF+5V line.
(iii) The front LED is lit amber.

1.6.6 Automatic switch function of input connector

The monitor has two input systems of SIGNAL A/B that can be switched.
The switch function works as follows.

(1) When power is supplied,
The input connector that was previously displayed is selected.

(2) Switching with SIGNAL A/B switch button.
When SIGNAL A/B switch button is pressed, the connector that is opposite the input connector now selected will be selected.

(3) When SYNC is not normally input.
(i) If any input SYNC is present,
The input connector is kept.
(a) If the input SYNC is OUT OF RANGE,
OSD of OUT OF RANGE is displayed.
(b) If not so,
The self diagnosis OSD is displayed or power management mode is entered.
(ii) If any input SYNC is not present at all,
It is switched to the other input connector at the interval of one second, and if any input SYNC is present, the input connector is continuously selected.
If no input SYNC is present in the other input connector either, switching will be continued at intervals of 1 second with the self-diagnosis OSD displayed or power management mode entered.

1.6.7 Circuit protective operation

If any circuit operation abnormality is detected, the monitor will forcibly enter power management mode to protect the circuit. (At this time, the picture is not displayed but LED is lit amber even if the sync. signal.)

(1) Power short-circuit detection on the secondary side
If PRO signal becomes H1 for one second or more, the power on the secondary side will be regarded as a short circuit to forcibly activate power management.

(2) EEPROM memory value error
The high-voltage adjustment HV-ADJUST and XRAY-PROJECT have respectively the backup data. When the power is supplied, the adjustment values are read from EEPROM. If this is not consistent with the backup data, it will be regarded as an EEPROM memory error to forcibly activate power management.

(3) I2C bus error
If the data line (SDA) of 12C bus (I2C1 and I2C2) that controls IC in the monitor is kept at LO 2 seconds or more, it will be regarded as I2C bus error to forcibly activate power management.

1.7 Deflection processor block

1.7.1 Outline

The deflection processor block mainly composed of deflection processor IC generates and controls a variety of the following compensation waveform that are produced by this IC.
The deflection processor IC is a Pin 64 IC of uPD61882 of IC700.
The following eight points are generated and controlled by the deflection processor IC.
(Refer to the block diagram of IC700 in the figure.)

(1)Vertical deflection waveform generating circuit
(2)Horizontal deflection drive waveform generating circuit
(3)Distortion compensation waveform generating circuit
(4)DBF compensation waveform generating circuit
(5)Convergence compensation waveform generating circuit
(6)Blanking waveform generating circuit
(7)Moire canceling circuit
(8)V-PARABOLA waveform generating circuit (VCANCEL)

Moreover, the block is provided with a small both-face board (PWB-DEFL-SUB) of 60mm X 70mm.
The power of the deflection processor block is +3.3V that is converted from P-OFF+5V by the regulator of IC702, and the power and GND are divided into the digital system and analog system in the inner circuit of IC700 in order to prevent noise interference for the waveforms.
OP amplifier of IC701 uses the power of +5V and -15V, and works as the trace filter and voltage amplification of the amplitude of the saw-toothed waveform for vertical deflection.

1.7.2 Vertical deflection waveform generating circuit

The deflection processor IC (IC700) does 10-bit DAC output of the saw-toothed wave for vertical deflection that is synchronized with the vertical frequency input to Pin 42, from Pins 1 and 11 at both polarities (approx. 1.2V.p-p). Moreover, the center voltage IMID (approx. 1.6VDC) of the saw-toothed wave is output from Pin 2.
To remove the noise, the OP amplifier (Pins 1, 2 and 3) of the front step of IC701 removes the difference between the waveforms of both polarities of the saw-toothed wave for vertical deflection, using the center voltage IMID of the saw-toothed wave as the reference. From the output of the amplifier, the digital gradation component of the saw-toothed wave is removed with the low pass filter that is made of R713 and C738. Moreover, Pins 62 and 63 of IC700 are the analog switch turning ON the retrace term, prevents the waveform deformation that is produced by the low pass filter, and prevents the degradation of the linearity and the fluctuation of the scanning line.
Moreover, the saw-toothed wave for vertical deflection is controlled to adjust the vertical picture width, vertical phase and linearity.
R715, R758, R760 and R762 connected to pair GND on the filter output composed of R712 and C738 are the resistor to improve the linearity of the saw-toothed wave for input vertical deflection, and switches the resistance into four steps with the transistor switch of Q703 and Q704 according to the vertical frequency. (Refer to the switch table in the next page.)
The saw-toothed wave for vertical deflection is output to the low output impedance with the OP amplifier (Pins 5, 6 and 7) of the rear step of IC701.

Vertical frequency	Q703	Q704
50~72.9Hz	OFF	OFF
73~89.9Hz	ON	OFF
90~124.9Hz	OFF	ON
125~160Hz	ON	ON

Vertical linearity compensation resistance select transistor ON/OFF

1.7.3 Horizontal deflection drive waveform generating circuit

The rectangular wave for horizontal deflection drive are output at the amplitude 3.3Vp-p and approx. 45% Duty from Pin 25 of IC700 with the delay of the transistor taken into account in order to make the Duty become 50% at the output of Q501 of the horizontal deflection circuit. Here, the simulative horizontal sync. signal (5V pulse) from the horizontal flyback pulse (AFC, 5V pulse) input to Pin 27 of IC700 and IC103 (MPU) input to Pin 44 of IC700 is passed through the invertor of IC7A1 to produce the edges of these waveforms. This prevents the noises of the jitter , etc. from generating.

Moreover, the circuit composed of Q700, Q702 , etc. connected to Pin 13 of IC700 prevents the rapid frequency variation of the horizontal output when the horizontal input signal becomes no signal. Pin 13 of IC700 is a phase comparator filter terminal to phase-lock the horizontal input sync. signal and the oscillation in IC700. When the horizontal input sync. signal becomes no signal, the terminal voltage rapidly varies from approx. 0.8V of the phase lock time to 0V, and the frequency of the horizontal output rapidly varies according to this. The circuit is added to compress the rapid frequency variation width by smoothening the variation of the terminal voltage of Pin 13 by C719 when it becomes unlocked. This prevents the horizontal collector pulse from jumping in order to prevent overvoltage against the horizontal output transistor (Q502).

The terminals Pin 13 to Pin 20 of IC700 become the control filter terminal of horizontal PLL.

1.7.4 Distortion compensation waveform generating circuit

The deflection distortion compensating waveform is output from Pin 64 of IC700. The waveform is output from 1-bit DAC, and 3.3V pulse waveform of resolution power of 25MHz is output at Pin 64 direct. The pulse waveform is smoothened with the low pass filter of R709 and C705 to gain the compensation waveform of the vertical frequency. The amplitude is approximately 1.0 to 1.2Vp-p, and is connected to Pin 5 of IC5J2.

The horizontal size, trapezoid compensation, side pin compensation, upper/lower compensation of the side pin, S type compensation of the side pin and W compensation of the side pin are applied. (Refer to the compensation image figure.)

The deflection compensation waveform in the horizontal phase system is output from Pin 57 of IC700. Pin 57 is the 1-bit DAC output, and outputs the pulse waveform of 3.3V of resolution power of 25MHz. The pulse waveform is smoothened with the low pass filter of R704, R753, C700 and C737, and the waveform of the vertical frequency is current-added to the filter (Pin 20 of IC700) of the horizontal system PLL to compensate for the deflection distortion of the horizontal phase system. The parallel rectangular distortion compensation and the side pin balance (upper and lower) compensation are executed. (Refer to the compensation image.)

1.7.5 DBF compensation waveform generating circuit

The horizontal system DBF compensation waveform is output in 8-bit DAC mode from Pin 10 of IC700. The amplitude is approximately 0.5Vp-p. It is connected to Pin 5 of IC7A0.

The vertical system DBF compensation waveform is output from Pin 58 in the 1-bit DAC mode. Pin 58 direct outputs the pulse waveform of the resolution power of 25MHz. The pulse waveform is smoothened with the low pass filter of R705 and C701 to gain the DBF compensation waveform of the vertical frequency. The amplitude is approximately 0.6Vp-p. It is connected to Pin 3 of IC7A0.

1.7.6 Convergence compensation waveform generation circuit

The horizontal dynamic convergence compensation waveform is output from Pin 6 of IC700 in the 8-bit DAC mode. The amplitude is approximately 0V to 0.5V. The vertical dynamic convergence compensation waveform is output from Pin 8 in the 10-bit DAC mode. The amplitude is approximately 0V to 0.5V. The dynamic convergence compensation waveform center voltage (approx. 1.6V) is output from Pin 7.
In the 1-bit DAC mode, the horizontal static convergence compensation waveform is output from Pin 61, and the vertical static convergence compensation waveform is output from Pin 60. In Pins 60 and 61 direct, the pulse waveform of the resolution power of 25MHz is output. The pulse waveform is smoothened through the low pass filter to gain the horizontal static convergence compensation waveform and vertical static convergence compensation waveform of the vertical frequency.

1.7.7 Blanking waveform generation circuit

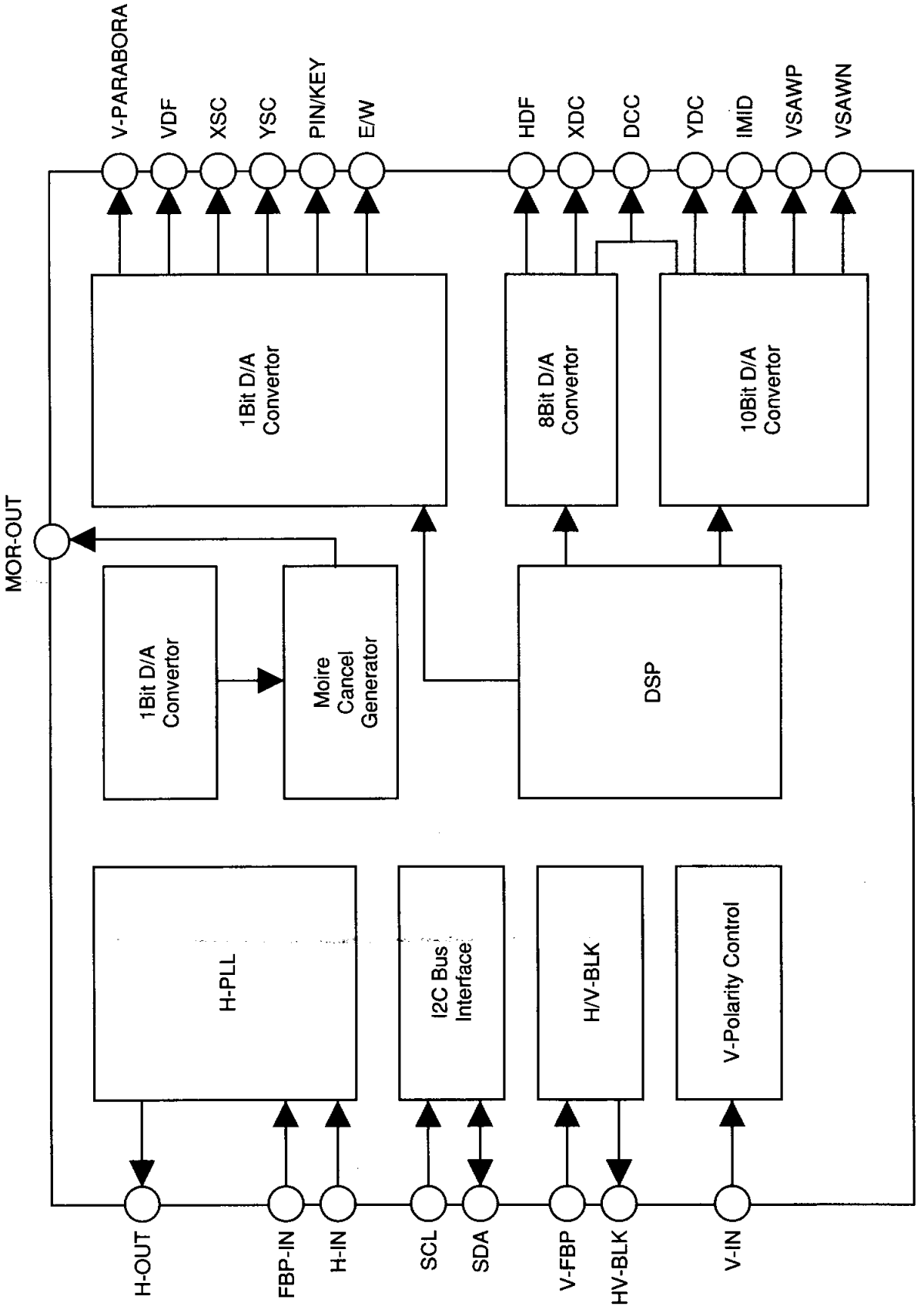
The horizontal blanking pulse and vertical blanking pulse are generated in IC700, and these two waveforms are mixed and output at 3.3Vp-p from Pin 40 of IC700.
The reference of the phase of the vertical blanking pulse is determined at the leading edge of VFLY (vertical flyback pulse, 5V pulse) of Pin 39 input of IC700, and the phase can be variably controlled to output the optimal waveform of the blanking pulse.
The horizontal blanking pulse is a pulse that is synchronized with H-IN (horizontal sync. signal, 5V pulse) of Pin 44 input of IC700, and can be also variably controlled.
The waveform is connected to Pin 22 of the preamplifier (IC301) of the video board.

1.7.8 Moire canceling circuit

The moire canceling circuit outputs the waveform that is reversed every line of the horizontal frequency and every 1 frame of the vertical frequency. The vertical frequency waveform is output from Pin 23, and these two waveforms are added to the horizontal PLL through the filter of R736 and C723 to achieve the moire canceling function.

1.7.9 V-PARABORA waveform generation circuit (VCANCEL)

V-PARABOLA waveform is output in the 1-bit DAC mode from Pin 59 of IC700. The pulse waveform of 3.3V of the resolution power of 25MHz is output at Pin 59 direct. The pulse waveform is smoothened with a low pass filter to gain V-PARABOLA waveform of the vertical frequency.
Pin 30 of IC700 is a terminal to detect the drop of the power voltage (+3.3V), and the detection voltage is approximately 1.0V. When a power voltage drop is detected, Pin 32 of IC700 varies from Hi level (5V) to Lo level (0V) but is not used now.
Pin 46 is a terminal to detect whether the horizontal PLL is locked and HD output from Pin 25 is normal or not. It is output at the Hi level (5V) when it is locked, and at the Lo level (0V) when it is unlocked. It is connected to IC103 (MPU).
Pin 49 is the reset terminal of IC700. The reset IC of IC703 resets IC700 when P-OFF+5V drops to approx. 2.7V.

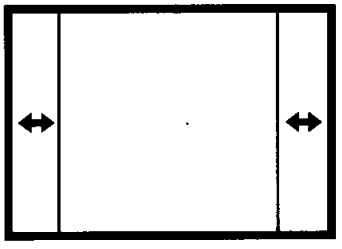


IC700 block diagram (uPD61882)

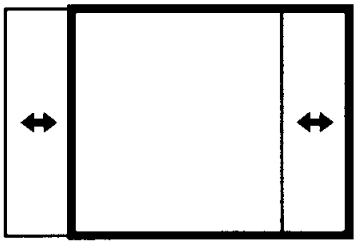
1.7.10 Distortion compensating operation

The followings are the operation image figures on the picture of the distortion compensstion.

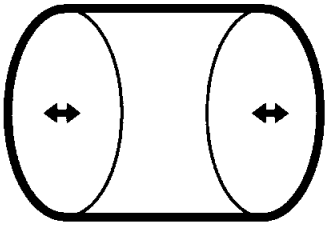
HORIZE-SIZE



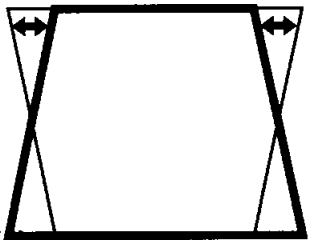
HORIZE-PHASE



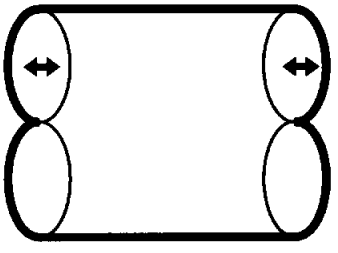
PINCUSHION



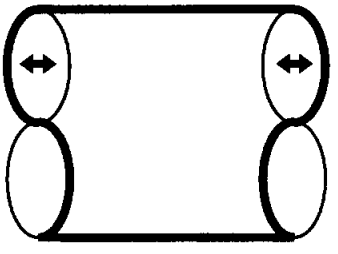
KEYSTONE



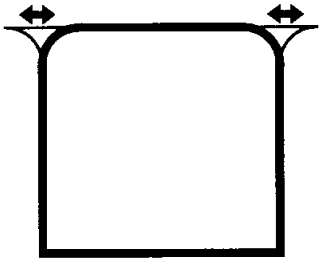
PIN-CENTER



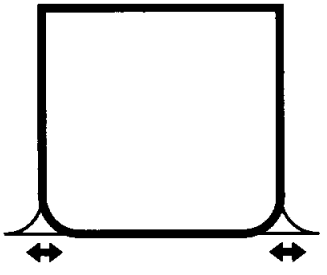
PCC-SINE



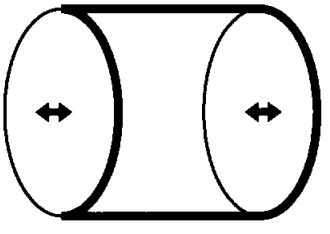
TOP-PIN



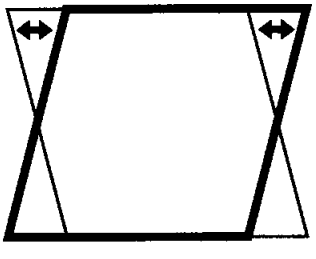
BOTTOM-PIN



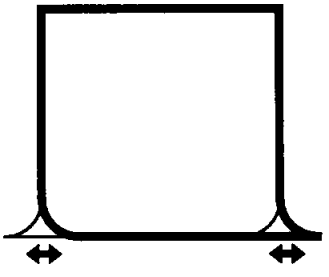
PIN-BALANCE



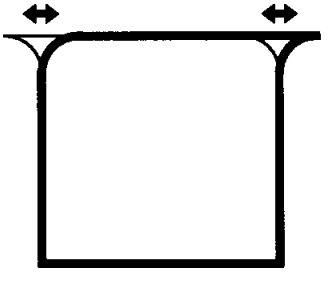
KEYBALANCE



BOTTOM-PIN



TOP-PIN



1.8 Video Block

1.8.1 Image signal amplifying circuit

The video circuit is composed of the same circuit structure for each of R, G and B. This item explains the G (green) video circuit.

The video input terminal is provided with 2 systems of SIGNAL-A and B, and are both the D-SUB connectors.

SIGNAL-A is input from Pin 2 of D-SUB connector (J201) to Pin 4 of the analog switch (IC200). Similarly, SIGNAL-B is input from Pin 2 of D-SUB connector (J200) to Pin 12 of the analog switch (IC200). (See Point A.)

The analog switch (IC200) is used for signal selection when SIGNAL-A and B are input at the same time.

As the signal selection method, the input signal SIGNAL-A is selected when Pin 13 (SELECT SW) of the analog switch (IC200) is LOW, and the input signal SIGNAL-B is selected when it is HIGH (See Point B.), and it is output from Pin 28 of the analog switch (IC200).

The video signal that is output from Pin 28 of the analog switch (IC200) is input to Pin 6 of Pre-AMP (IC301) on the video board through the flat cable. (See Point C.)

Pre-AMP (IC301) is a pre-amplifier that amplifies the voltage of the video signal (GAIN: 4 to 5 magnifications). Moreover, Pre-AMP (IC301) composes the adjustment picture (OSD) video signal output from IC300 and the blanking signals output from IC700. Moreover, the MPU (IC103) detects the current that flows through the flyback transformer on the main board, and the amplitude control (ABL) of the output voltage of the Pre-AMP (IC301) is applied to prevent the picture brightness from exceeding the constant value. The video signal processed through the voltage amplitude, composition and amplification control is output from Pin 31 of Pre-AMP (IC301), and is input to Pin 8 of MAIN-AMP (IC302) (See Point D.).

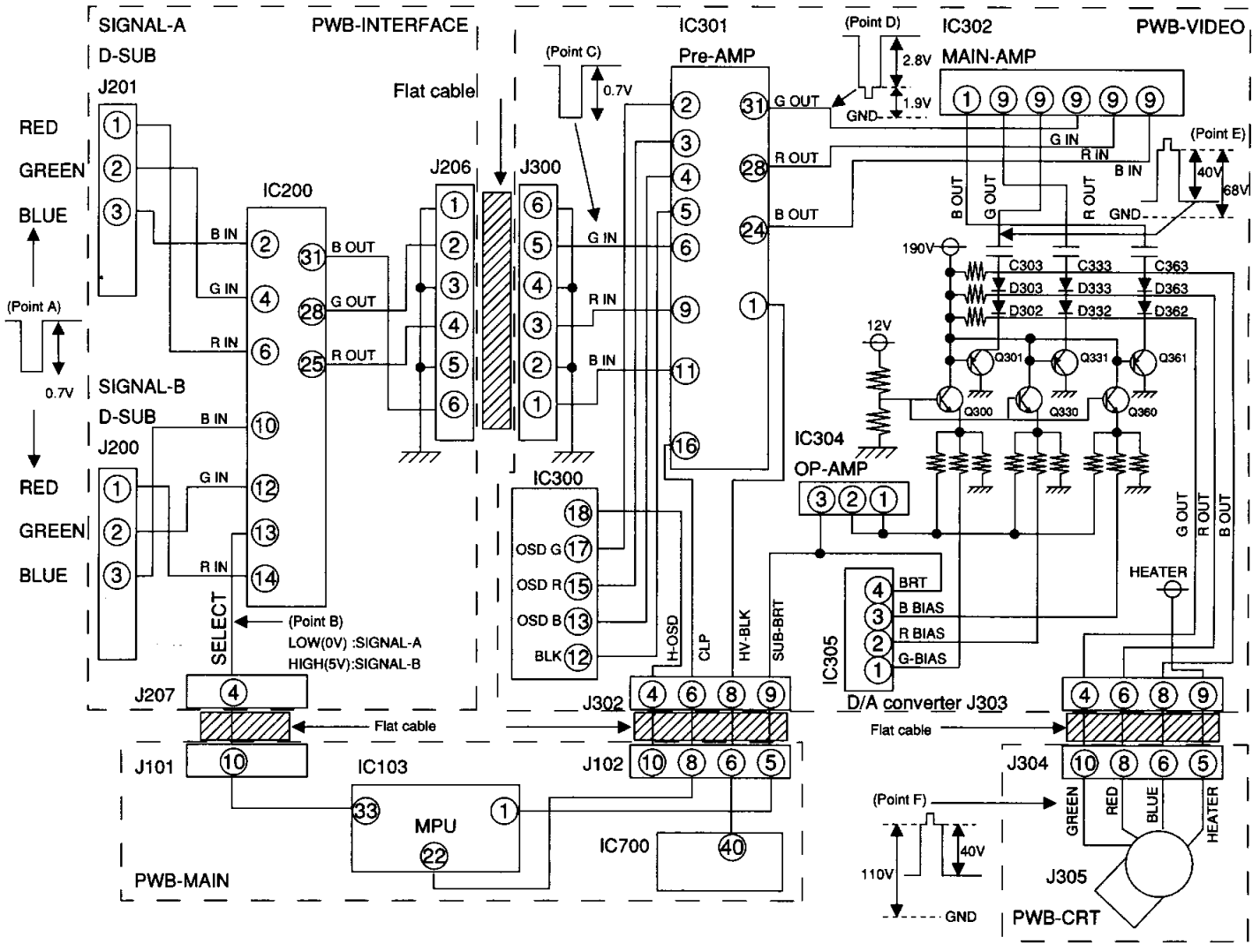
MAIN-AMP (IC302) is the main amplifier that amplifies the voltage of the video signal (GAIN: 13 to 15 magnifications). The video signal processed through the voltage amplification is output from Pin 5 of MAIN-AMP (IC302) (See Point E.). After it is AC-coupled by C303, it is DC-reproduced by the cutoff (diode clamp) circuit that is composed of D302, D303, Q300 and Q301.

The cutoff (DC bias control) voltage varies the back raster brightness (brightness) and chromaticity (bias) with the brightness control signal and bias control signal.

The brightness control signal is superimposed with SUB-BRT signal (for factory adjustment) output from Pin 1 of the MPU (IC103) and BRT signal (for user adjustment) output from Pin 4 of the D/A converter (IC305) by OP-AMP (IC304), and is output from Pin 1 of OP-AMP (IC304). The back raster brightness (brightness) is varied by applying the superimposed brightness control signal to the emitter of the base ground transistor (Q300).

The bias control signal is output from Pin 1 of the D/A converter (IC305). The bias control signal is also applied to the emitter of the base ground transistor (Q300) like the brightness control signal in order to vary the back raster chromaticity (bias).

The video signal that is AC-coupled with the above cutoff voltage is input to the CRT socket (J305) on the CRT board through the flat cable, and is supplied to the cathode of CRT. (See Point F.)



Video signal amplification circuit diagram

1.8.2 Input switch circuit

The sync. signal input terminal has two systems of SIGNAL-A and B like the video input terminal, and are both the D-SUB connectors. Since the input terminal and circuit operation are different every sync. signal (separate, composite, image composite), this item explains their sync. signals.

1.8.2.1 Separate sync. signal (Separate Sync)

The horizontal sync. signal input from SIGNAL-A is input from Pin 13 of D-SUB connector (J201) to Pin 7 of the analog switch (IC200), and the vertical sync. signal is input from Pin 14 of D-SUB connector (J201) to Pin 8 of the analog switch (IC200). Moreover, the horizontal sync. signal input from SIGNAL-B is input from Pin 13 of D-SUB connector (J201) to Pin 15 of the analog switch (IC200), and the vertical sync. signal is input from Pin 14 of D-SUB connector (J201) to Pin 16 of the analog switch (IC200). (See Point A.)

Like the video signal, the analog switch (IC200) selects the signal (2 input switch) when SIGNAL-A and B are input at the
same time.

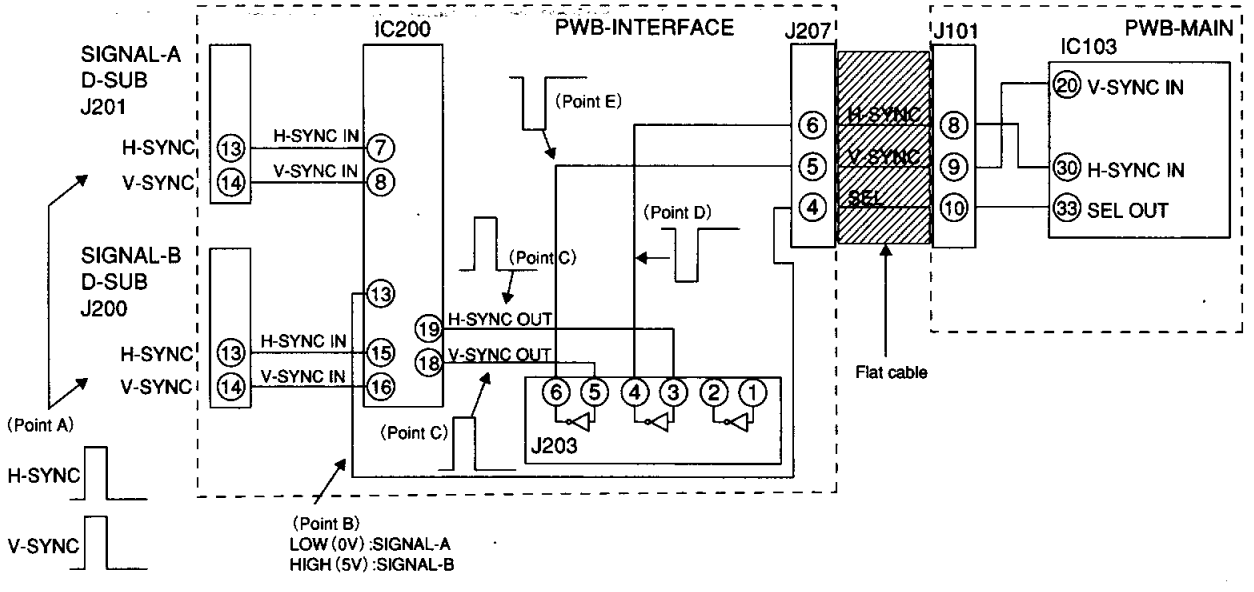
Like the video signal, the signal selection method is that the input signal of SIGNAL-A is selected when Pin 13 (SELECT SW) of the analog switch (IC200) is set at LOW by SELECT signal of Pin 33 of the MPU (IC103), and the input signal of SIGNAL-B is selected when it is HIGH (See Point B.), and the signal is output from Pin 19 (horizontal sync. signal) and Pin 18 (vertical sync. signal) of the analog switch (IC200). (See Point C.)

The horizontal sync. signal output from Pin 19 of the analog switch (IC200) is input to Pin 3 of the invertor (IC203), and is output from Pin 4 of the invertor (IC203) after the polarity of the horizontal sync. signal is reversed. (See Point D.) The vertical sync. signal output from Pin 18 of the analog switch (IC200) is input to Pin 5 of the invertor (IC203), and is output from Pin 6 of the invertor (IC203) after the polarity is reversed like the horizontal sync. signal. (See Point E.)

The reason the polarity is reversed by the invertor (IC203) is to remove the jitter (sizzling noise) on the picture displayed on the monitor.

The horizontal sync. signal and vertical sync. signal output from the invertor (IC203) are supplied through the flat cable to Pin 30 (horizontal) and Pin 20 (vertical) of the MPU (IC103) on the main board.

Though the positive polarity (POS) and negative polarity (NEG) are provided as the polarities of the separate sync. signal, the following figure shows that the positive polarity (POS) is input.



1.8.2.2 Composite sync. signal (Composite Sync)

The composite sync. signal input from SIGNAL-A is input from Pin 13 of D-SUB connector (J201) to Pin 7 of the analog switch (IC200). Moreover, the composite sync. signal input from SIGNAL-B is input from Pin 13 of D-SUB connector (J201) to Pin 15 of the analog switch (IC200). (See Point A.)

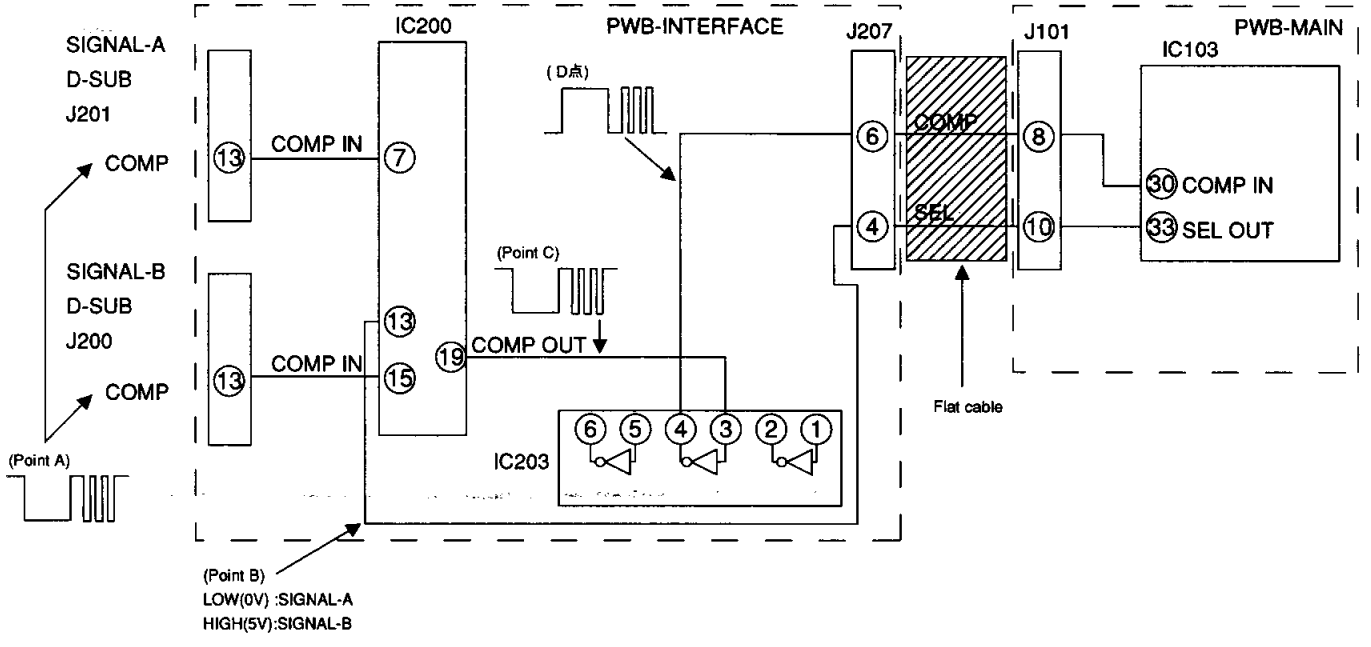
Like the separate sync. signal, the analog switch (IC200) selects the signal (2 input switch) when SIGNAL-A and B are input at the same time.

Like the separate sync. signal, the signal selection method is that the input signal of SIGNAL-A is selected when Pin 13 (SELECT SW) of the analog switch (IC200) is set at LOW by the SELECT signal of Pin 33 of the MPU (IC103), and the input signal of SIGNAL-B is selected when it is HIGH (See Point B.), and the signal is output from Pin 19 of the analog switch (IC200). (See Point C.)

The composite sync. signal output from Pin 19 of the analog switch (IC200) is input to Pin 3 of the invertor (IC203), and is output from Pin 4 of the invertor (IC203) after the polarity of the composite sync. signal is reversed. (See Point D.)

The reason the polarity is reversed by the invertor (IC203) is to remove the jitter (sizzling noise) on the picture displayed on the monitor like the separate sync. signal.

The composite sync. signal output from the invertor (IC203) is supplied through the flat cable to Pin 30 of the MPU (IC103) on the main board, and is processed through synchronous separation by the MPU (IC103).



1.8.2.3 Video composite sync. signal (Sync on Green)

The image (green video) composite sync. signal input from SIGNAL-A is input from Pin 2 of D-SUB connector (J201) to Pin 4 of the analog switch (IC200). Moreover, the image (green video) composite sync. signal input from SIGNAL-B is input from Pin 2 of D-SUB connector (J201) to Pin 12 of the analog switch (IC200). (See Point A.)

Like the separate sync. signal and composite sync. signal, the analog switch (IC200) selects the signal (2 input switch) when SIGNAL-A and B are input at the same time.

Like the separate sync. signal and composite sync. signal, the signal selection method is that the input signal of SIGNAL-A is selected when Pin 13 (SELECT SW) of the analog switch

(IC200) is set at LOW by the SELECT signal of Pin 33 of the MPU (IC103), and the input signal of SIGNAL-B is selected when it is HIGH (See Point B.), and the video signal is output from Pin 28 of the analog switch (IC200) (See Point C.) and the composite sync. signal is output from Pin 21 of the analog switch (IC200). (See Point D.)

The image composite sync. signal must be separated into the video signal and composite sync. signal.

As the separation method of the image signal and composite sync. signal, the S/G-SEL signal of the MPU (IC103) becomes HIGH (5V) when the MPU (IC103) detects the image (green video) composite sync. signal. Then, the transistor (Q200) is turned OFF to output the image (green video) composite sync. signal from Pin 23 of the analog switch (IC200). The image (green video) composite sync. signal output from Pin 23 of the analog switch (IC200) is input to Pin 22 of the analog switch (IC200), and after it is separated into the image signal and composite sync. signal in the analog switch (IC200), the composite sync. signal only is output from Pin 21.

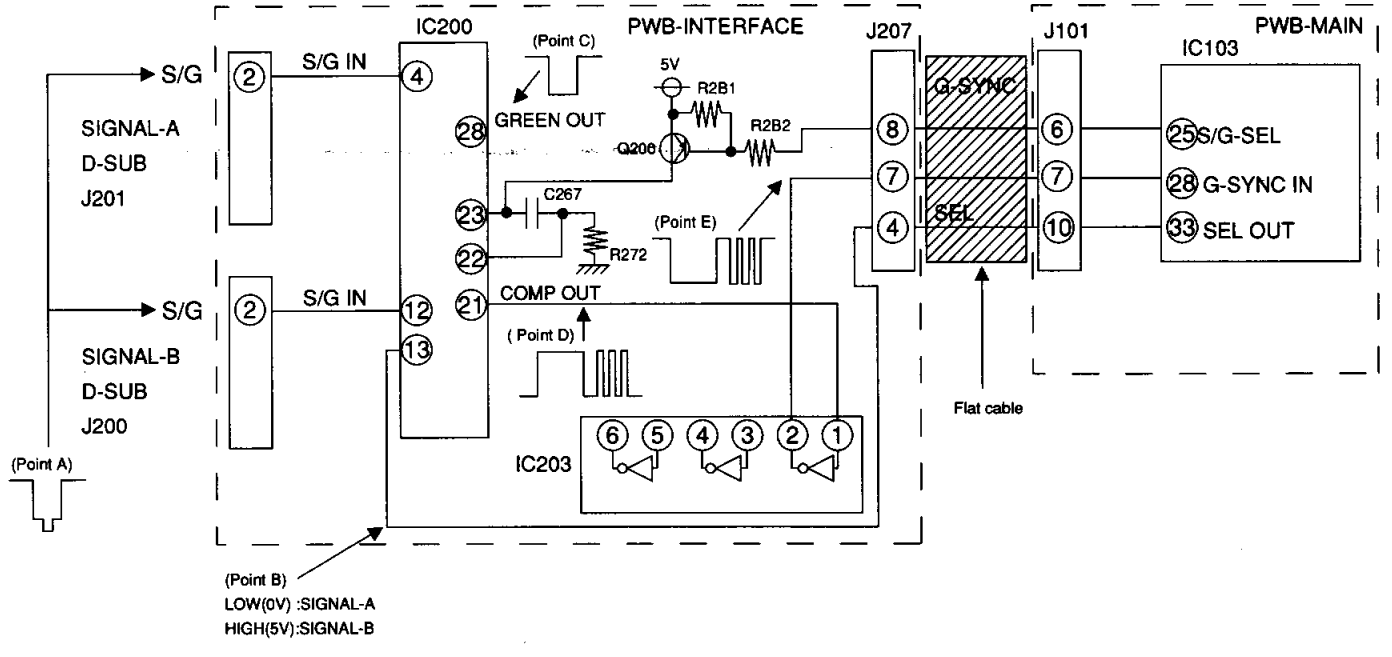
The composite sync. signal output from Pin 21 of the analog switch (IC200) is input to Pin 1 of the invertor (IC203), and is output from Pin 1 of the invertor (IC203) after the polarity of the composite sync. signal is reversed. (See Point D.)

The reason the polarity is reversed by the invertor (IC203) is to remove the jitter (sizzling noise) on the picture displayed on the monitor like the separate sync. signal and composite sync. signal.

The composite sync. signal output from the invertor (IC203) is supplied through the flat cable to Pin 28 of the MPU (IC103) on the main board, and is processed through synchronous separation by the MPU (IC103).

1.8.3 On Screen Display circuit

The control signal of the adjustment picture (OSD) is input to Pin 5 (CLK), Pin 6 (DATA), Pin 18 (H-BLK), and Pin 19 (V-BLK) of IC300. IC300 outputs Pin 12 (BLK), Pin 13 (OSD-B), Pin 15 (OSD-R), and Pin 17 (OSD-G), and they are synthesized with the video signal by IC301.



2. Adjustment procedure

2.1 Scope

These are the specified adjustment and inspection methods for the NSH1117STTKW.

2.2 Application

The applicable models are as follow.

Model	Rating label	Destination	Remarks
1	NSH1117STTKW	For own domestic use	

(Note) When degaussing this monitor with the hand demagnetizer, use the following procedure.

(1)Turn the monitor power OFF, and degauss with the hand demagnetizer.

(2)Degauss with the hand demagnetizer in the power management state.

(3)Degauss with the hand demagnetizer during automatic demagnetization of monitor unit.

2.3 Measuring instruments

(1) Signal generator A: Astro Design VG-812 or equivalent

(2) Signal generator B: Astro Design VG-829 or equivalent

(3) DC voltmeter: 150V 0.5 Class or digital voltmeter

(4) High voltage meter: 0.5 Class that can measure 30KV

(5) Luminance meter: Minolta color analyzer CA-100 or equivalent

(6) AC voltmeter: 150V/300V 0.5 Class

(7) Oscilloscope: Scope with band of 100MHz or more

(8) Landing measuring device: Felmo product

(9) Double scale: For width and distortion measurement

(10) Withstand voltage meter: Kikusui Model TOS8650 or equivalent

(11) Grounding conductivity measuring instrument: CLARE U.K. product