NEC

Service Manual

15-inch LCD Monitor
NEC-FA150ATUA

Service Manual Versions and Revision

No.	Version	Release Date	Revision
1.	1.0	October 2, 2001	Original release
2	1.1	October 11, 2001	Circuit Description 9 (3) -- page 7 Trouble Shooting 4 -- page 6 6 -- page 8 14.3 -- page 20
3	1.2	October 16, 2001	Circuit Description 1.1 -- page 1 5 -- page 3 9.2.1 (2) -- page 6 9.2.1 (3) -- page 7 9.4.1 -- page 8 Trouble Shooting 3 -- page 5 13 -- page 17

NEC FA150ATUA Service Manual.

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1. Audio circuit (Circuit diagrams Main PWB) KT

1.1 Audio input

The audio signal input received from the audio input terminal (J301) is applied to the amplifier I314 of 4 (L-CH) and 9 (R-CH) through the low-pass filter consisting of R374, R376, R378, R379, C464 and C465.
In this amplifier, controls of Volume, and mute are conducted. The audio signal controlled at the pin 6 determines the attenuation of output of the amplifiers. Since then, the signal is output to the jack P307.

1.2 Audio output

The audio signal is output from the jack output terminal (P307) of the jack board to the internal speaker system.

2. Power supply (Circuit daigrams MAIN PWB)

1. Line filter consists of C801, T801, C803, C804. It eliminates high frequency interference to meet EMI's requirement.

2. Rec & Filter

Bridge diode D801 converts AC source into pulsed DC. This pulsed DC is smoothed and filtered by C805.
R802 is an NTC (negative thermal coefficient) resistor, used to reduce inrush current to be within safe range.

3. Power transformer :

T802 converts energy from power source C805 to secondary side to generate +12V and +5V.

4. Output :

When driver Q803 is driven on and off by I801, pin 6 and pin 9 of T802 induce a square wave. This square wave is rectified by D809, D810, then filtered by C817, C822 to generate +12V and +5V respectively.

5. Driver : Q803

If the electrical potential of gate is larger than source by about 10 volts, Q803 turns on.

6. FB :

Negative feedback CKT consists of photo coupler I802 and adjustable regulator I803. It can maintain output voltages +5V and +12V at a stable level.

7. PWM :

7.1 Start : When power is turned on, Q801 conducts due to bias from C805 and R808. Q801 supplies a 17 volt and a starting current about 0.3mA to pin 7 of I801. I801 starts to oscillate (R816, C813) and outputs a pulse train through pin 6 to drive Q808.

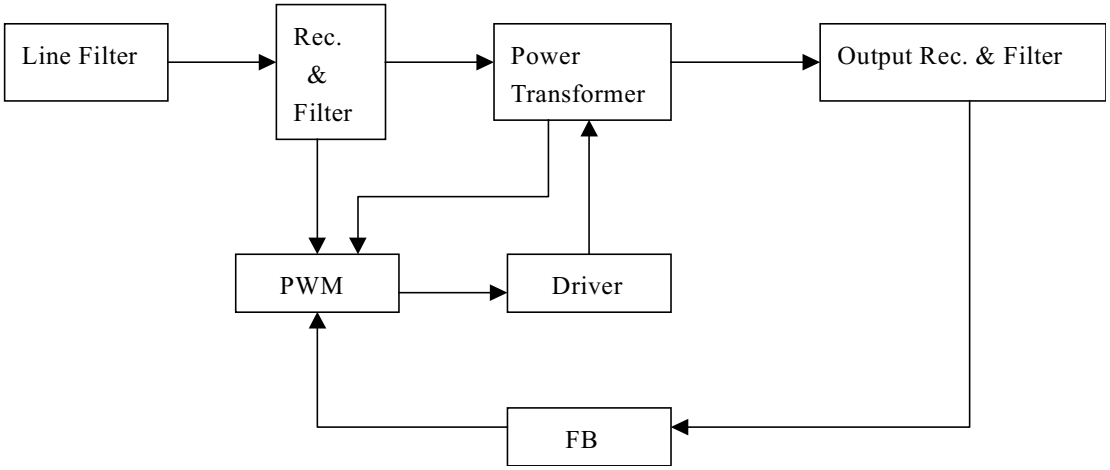
7.2 OPP : When Q808 turns on, C805 supplies a linearly increasing triangle current through the primary inductance of T802 to the driver Q808, once the peak value of this current multiplied by R811 exceeds1 volt, pulse train will be shut down immediately to protect Q808, T802 from being burned out.

7.3 Regulation : If output voltage +5V goes up, the R terminal of I808 gets more bias, accordingly photo transistor and photo diode flows more current. The voltage of pin 2 goes up too, making the pulse width of pin 6 to become narrower. So the output voltage +5V will be pulled down to a stable value.

7.4 *OVP* : If +5V goes up too much, the induced voltage on pin 4 of T802 becomes large also. Suppose that it is over 22 volts, ZD808 conducts, Q806 is triggered on, pin 1 of IC801 is pulled down to ground, the pulse train at pin 6 goes down to zero, shutting Q808 off completely.

7.5 *SCP* : If output terminal is short to ground, photo transistor does not conduct, hence Q805 does not conduct neither. The reference voltage +5V at pin 8 begins to charge on C829 and activates Q806 to conduct, pulling pin 1 down to ground, shutting Q808 off completely.

LCD 1550M Power Board Block Diagram



3. On-screen circuit (Circuit diagrams Main PWB 3/6)

I305 (M66611) Embeded function.

OSD (character pattern display controller) is a module by which the character data beforehand prepared on the normal display data is inserted (display) in an arbitrary position. SRAM can be built into internally for the character storage and it is possible to compose the flexible data of the user side.

The outline is shown in Table 1.1.

Table 1.1 Outline for OSD

Item	Outline
Screen Composition	24 digits x 12 lines x 1 page
Number of display characters	Max. 288 characters
Character composition	12 x 180 dots
Kind of character	64 kinds
Character size	4 (Ver. Direction) x 2 kind (Hor. Direction)
Blinking	Character unit (32/64 viding frequency of vertical synchronization, duty: 25, 50 and 75%)
Coloring	Character color (character unit)/ Character background color (character unit)
Blanking	Character size / Border size / Matrix-outline size / All blanking
Function of deletion of batch of display RAM	Built-in (field memory)

4. Video input circuit (Circuit diagram MAIN PWB 2/6)

RAIN Analog Input for RED Channel

GAIN Analog Input for GREEN Channel

BAIN Analog Input for BLUE Channel

High-impedance inputs that accept the RED, GREEN, and BLUE channel graphics signals, respectively. (The three channels are identical, and can be used for any colors, but colors are assigned for convenient reference.)

They accommodate input signals ranging from 0.5V to 1.0V full scale. Signals should be ac-coupled to these pins to support clamp operation.

5. Definition converter LSI peripheral circuit (Circuit diagram MAIN PWB)

I305 M66611FP is the definition converter LSI.

DESCRIPTION

M66611FP Series is a picture processor for the flat panel displays, it have unique picture processing function that high quality picture scaling and color coversion with keeping white balance. Low cost chip-set solution is provided.

FEATURES

● *Input and output format compatibility:*

-16.7 million colors in all formats

-VGA to SXGA inputs

-SXGA output (Available for B grade ver.)

● *Input port:*
-Up to 135 Mpixels/sec (Available for B grade ver.)
-24/48-bit RGB programmable, (one or two pixel-per-clock respectively)
-Seperate / composite syncs
-Glue-less interface to analog front end IC's
-TMDS receiver interface
-Interface to NTSC-digital decode IC's (YUV to RGB conversion, simplified inter less processing.)

●*Display port:*
-Up to 135 Mpixels/sec (by 48bit RGB port/B grade ver.)
-24/48-bit RGB programmable. (one or two pixel-per-clock LCD panel respectively)
-Supports 18-bit and 24-bit display
-Programmable timing generator

● *PICT clock rate conversion:*
-50Hz to 75Hz input refresh rates for VGA to SXGA
-50Hz to 75Hz output refresh rate (must be the same as input rate)
-No extermal frame memory required

● *Programmable picture processing:*
-High quality picture scaling
-Up/down scaling from VGA, SVGA, XGA, or SXGA to XGA
-Indenpendent horizontal and vertical scaling
-Edge enhancement / smoothing (M66611)
-Color conversion with keeping white balance (M66611)
-Color space expanding to 24-bit full color for 18-bit LCD panel
-1024-extry gamma table for each R,G, B color (M66611)

6. System reset, LED control circuit (Circuit diagram MAIN PWB 4/6)

6.1 System reset

System reset is performed by detecting the rising and falling of the 3.3V source voltage at I309.
There are two kinds of resets;hardware and software. In both cases, operation is the same after the reset. (See "Software Reset" for details of software resets.) This section explains on hardware resets.
When the supply voltage is in the range where operation is guaranteed, a reset is effected by holding the reset pin level "L" (0.2Vcc max.) for at least 20 cycles. When the reset pin level is then returned to the "H" level while main clock is stable, the reset status is cancelled and program execution resumes from the address in the reset vector table.
Figure 6.1 showns the example reset circuit. Figure 6.2 shows the reset sequence.

6.2 LED control circuit

Green / amber is lit with the control signal of the LED GREEN and LED AMBER signal pin 66, 65 from I306 (Circuit diagram MAIN PWB 4/6).

Figure 6.1 Example reset circuit

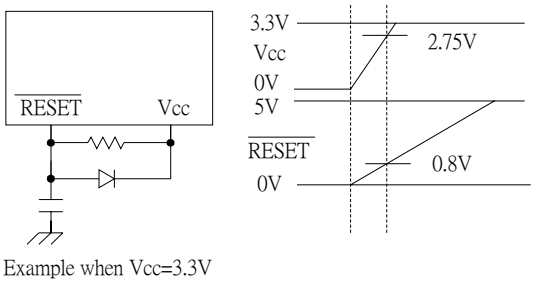
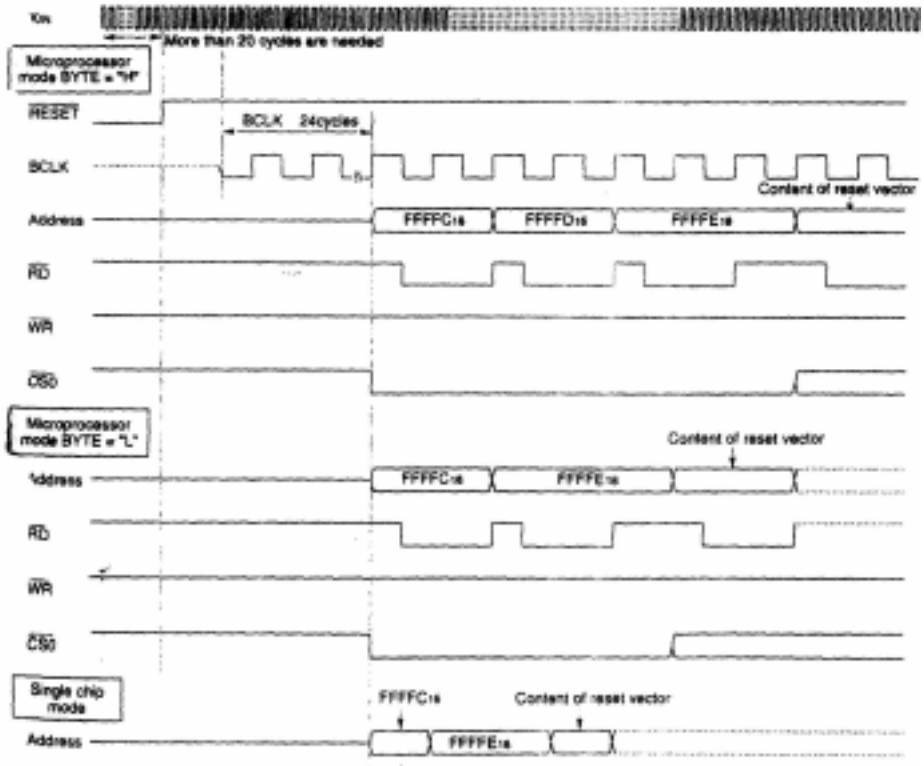


Figure 6.2 RESET sequence



7. E²PROM for PnP (Circuit diagram MAIN PWB)

Data transfer between I304 and host.

There are two forms of communications protocal. In both, display capabilities are retrieved by the system software during the boot-up and configuration time.

For the PC platform, this software layer is defined in the VESA BIOS Extension / Display Data Channel, VBE/DDC, standard.

8. E²PROM (Circuit diagram MAIN PWB 4/6)

Data transfer between I308 (24LC32) and CPU (I306) is effected through the IIC bus SCL (pin 80) and SDA (pin 81) of I306. The data to be transferred to each device are stored in I308.

- I303 control data.

9. CPU circuit (Circuit diagram MAIN PWB 4/6)

I306 (M30620FGMGP) functions as the CPU.

The source voltage for the device is 3.3V and the system clock frequency is 10MHz.

9.1 Detection of POWER switch status

The CPU identifies the ON status of the two power supplies. The identification is made when the power supply is turned off. For example, if the power supply is turned off with the POWER switch, the POWER switch must be turned on when activating the power supply again. If the power supply is turned off by pulling out the power cord, then this power supply can be turned on by connecting the power cord, without pressing the POWER switch.

9.2 Display mode identification

9.2.1 Functions

(1) Display mode identification

- The display mode of input signal is identified based on Table 1, and according to the frequency and polarity (HPOL, VPOL) of horizontal or vertical sync signal, presence of the horizontal or vertical sync signal, and the discrimination signal (HSYNC_DETECT, VSYNC_DETECT).
- When the mode has been identified through the measurement of horizontal and vertical frequencies, the total number of lines is determined with a formula of " Horizontal frequency / Vertical frequency = Total number of lines. "Final identification can be made by examining the coincidence of the obtained figure with the number of lines for the mode identified from the frequency.
- When the detected frequency if the sync signal has changed, the total number of lines should be counted even through it identified frequency in the same mode. Then, it is necessary to examine whether the preset value for the vertical display position has exceeded the total number of lines. If exceeded, a maximum value should be set up.

(2) Power save mode.

The power save mode is assumed when the horizontal / vertical signals are as specified below.

- If there is no horizontal sync signal input or below 10KHz.
- If there is no vertical sync signal input or below 10Hz.

Table 1 Preset Timing Chart

Preset	Resolution	H-freq (KHz)	Band Width (MHz)	Polarity	
				H	V
0	Non-interlaced PAL*	31.25	27	-	-
1	VGA 720 x 350 70Hz	31.47	28.322	+	-
2	PC98 640 x 400 56Hz *	24.83	21.053	+/-	+/-
3	VGA 720 x 400 70Hz	31.47	28.322	-	+
4	VGA 640 x 480 60Hz	31.47	25.175	+/-	+/-
5	MAC 640 x 480 66Hz	35	30.24	+/-	+/-
6	VESA 640 x 480 72Hz	37.86	31.5	+/-	+/-
7	VESA 640 x 480 75Hz	37.5	31.5	-	-
8	VESA 800 x 600 56Hz	35.16	36	+/-	+/-
9	VESA 800 x 600 60Hz	37.88	40	+/-	+/-
10	VESA 800 x 600 75Hz	46.88	49.5	+/-	+/-
11	VESA 800 x 600 72Hz	48.08	50	+/-	+/-
12	MAC 832 x 624 75Hz	49.72	57.283	+/-	+/-
13	VESA 1024 x 768 60Hz	48.36	65	+/-	+/-
14	SUN 1024 x 768 65Hz	52.45	70.49	+/-	+/-
15	VESA 1024 x 768 70Hz	56.48	75	+/-	+/-
16	VESA 1024 x 768 75Hz	60.02	78.75	+/-	+/-

(3) Out of range

When resolution beyond 1024 x 768 is inputted, resolution is lowered with Down scaling to 1024 x 768, and indicated, and OSD should indicate OUT of Range.

- If the horizontal sync signal is outside the measuring range 31.5KHz - 60KHz
- If the vertical syna signal is outside the measuring range 56.2Hz - 75.1Hz

9.3 User Control

General Key Description

Exit: Turn off OSM menu, Exit sub menu.

Control: Move the green cursor amd select control items.

Adjust: Change the value of each function / Enter to submenu / Proceed auto adjust / Proceed reset

Next: Move the NEXT tag

Reset: Reset the select item (Open reset warning before reset) / Mute the speaker / headphone sound (short cut: when no OSM menu is shown)

9.3.1 Related ports of I306

Port	Pin No.	I/O	Signal name	Function	Remarks
P3.5	55	1	RESET / Mute	RESET switch input MUTE switch input	The set value is returned to the initial value
P3.1	59	1	EXIT	EXIT switch input	Withdraw from OSD
P3.4	56	1	DOWN	- switch input	(-) key
P3.3	57	1	UP	+ switch input	(+) key
P3.2	58	1	LEFT	◀ switch input	(◀) key
P3.6	54	1	RIGHT	▶ switch input	(▶) key
P3.7	53	1	NEXT	NEXT switch input	

9.3.2 Functions

Control is effected for the push-switches to be used when the user changes the parameters, in order to modify the respective setting values. Whether the switch has been pressed is identified with the switch input level that is turned “L”.

Each switch input port is pulled up at outside of MCU.

Each parameter is stored in the EEPROM, the contents of which are updated as required.

9.4 Control of definition converter MCU I306.

9.4.1 Ports related to control

Pin No.	I/O	Signal name	Function
33	O	SSI	Serial data Input to M66611
34	I	SSO	Serial data Output to M66611
35	O	SCK	Serial clock Input to M66611
36	O	SCSB	Chip select to M66611
37	I	SRDYB	Ready output

9.4.2 Functions

Major function of I305 are as follows:

(1) Expansion of the display screen.

(2) Timing control for various signal types.

(3) Power-supply sequence (LCD panel).

9.5 I^2C bus control

9.5.1 Related ports of I306

Port	Pin No.	I/O	Signal name	Function
P0.6	80	I	IICCLK	IIC bus clock
P0.5	81	I/O	IICDATA	IIC bus data

9.5.2 I^2C-controlled functions

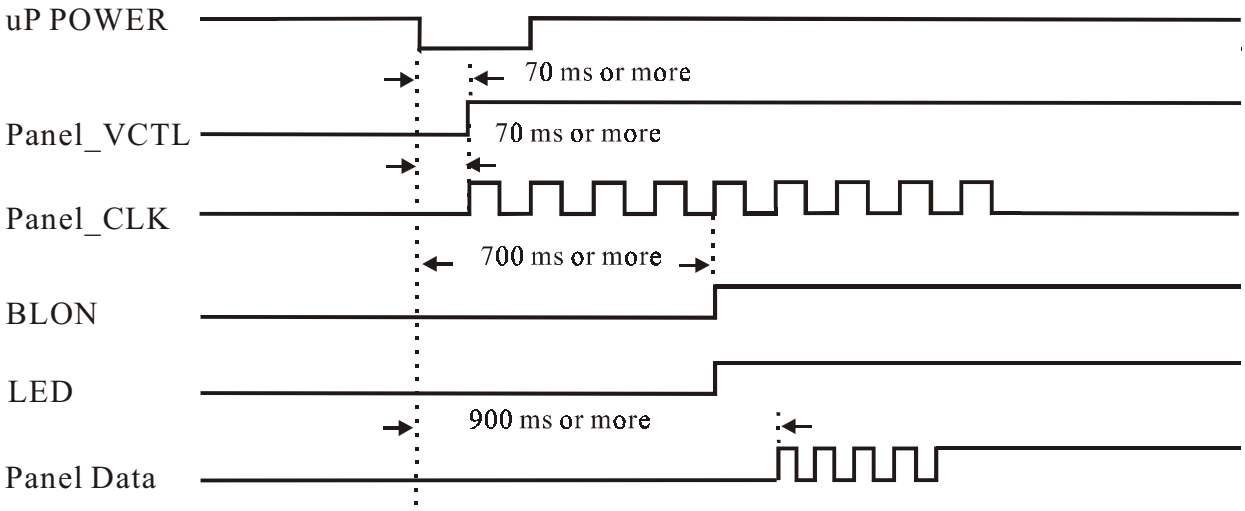
The following functional controls are effected by I^2C.

(1) Control of EEPROM I308f for parameter setting.

(2) Control of audio preamplifier.

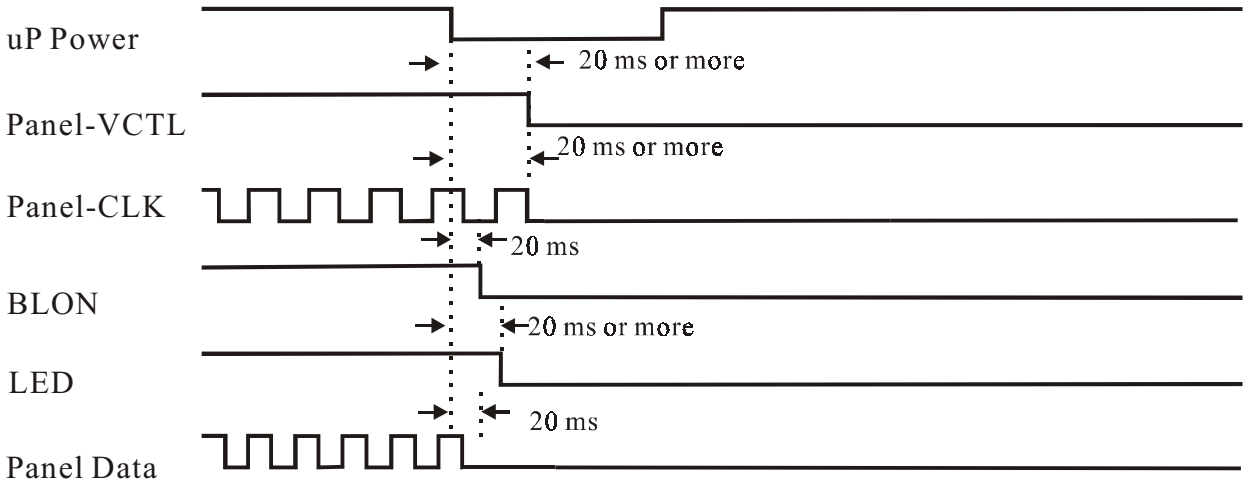
9.6 Power ON sequence

When the POWER switch is pressed, the POWER OFF signal is turned “H”. When this “H” potential is detected, the CPU begins to establish the respective power supplies according to the sequence shown below.



9.7 Power OFF sequence

When the POWER switch is pressed while the power supply is ON, the POWER ON signal is turned “H”. When tshown below.his “H” potential is detected, the CPU begins to turn off the respective power supplies according to the sequence



9.8 List of CPU Pin Assignments

Port	Pin No	Signal Name	Initial Seeting	Function	Remark
P9.4	1	Bright	~	Inverter Luminance Control	
P9.3	2	Volume	~	Audio Volume Control	
P9.2	3	Nc	~	~	
P9.1	4	Nc	~	~	
P9.0	5	Nc	~	~	
	6	Byte	~	ISP Byte Function	
	7	CNVss	~	Switches change between processor mode	
P8.7	8	Nc	~	~	
P8.6	9	Nc	~	~	
	10	Reset	L	Reset Signal at Lower Level with 20 Clock	Active L
	11	Xout	~	uP Clock Output	
	12	Vss	~	GND	
	13	Xin	~	uP Clock Input	
	14	Vcc	~	uP_Vcc 3.3V	
P8.5	15	NMI	~	uP Interrupt generator When Hi to Low	
P8.4	16	Nc	~	~	
P8.3	17	V1_Detect	~	VS_ASIC	
P8.2	18	Nc	~	~	
P8.1	19	H1_Detect	~	HS_ASIC	
P8.0	20	NC	~	~	
P7.7	21	DE_Detect	~	DDC_GND	
P7.6	22	BLON	H	Inverter Enable Control	
P7.5	23	Nc	~	~	
P7.4	24	Nc	~	~	
P7.3	25	Nc	~	~	
P7.2	26	Nc	~	~	
P7.1	27	DDC_SCL	~	uP_DDC_SCL	
P7.0	28	DDC_SDA	~	uP_DDC_SDA	
P6.7	29	TXD	~	ISP TXD	
P6.6	30	RXD	~	ISP RXD	
P6.5	31	SCLK	~	ISP SCLK	
P6.4	32	BUSY	~	ISP BUSY	
P6.3	33	SSI	~	uP_Clock Serial Data Input	
P6.2	34	SSO	~	uP_Clock Serial Data Output	
P6.1	35	SCK	~	uP_Clocled Serial clock Input	

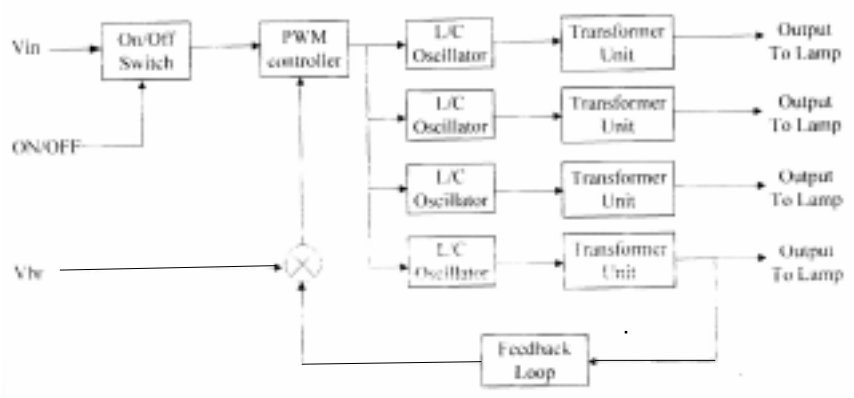
Port	Pin No	Signal Name	Initial Seeting	Function	Remark
P6.0	36	SCSB	~	uP_Clocked Serial Chip Selecet Input	
P5.7	37	SRDYB	~	uP_Clocked Serial RDY Output	
P5.6	38	Nc	~	~	
P5.5	39	EPM	~	ISP EPM Function	
P5.4	40	Soundsel	~	~	
P5.3	41	Nc	~	~	
P5.2	42	Nc	~	~	
P5.1	43	Nc	~	~	
P5.0	44	CE	~	ISP CE Function	
P4.7	45	Nc	~	~	
P4.6	46	Nc	~	~	
P4.5	47	Nc	~	~	
P4.4	48	Nc	~	~	
P4.3	49	Nc	~	~	
P4.2	50	SUSP	L	Audio Suspand Function	Active H
P4.1	51	Wprt_0	L	Serial EEPROM Write Protection	Active H
P4.0	52	Mute	L	Audio Mute Function	Active H
P3.7	53	Proceed	H	uP_Proceed	Active L
P3.6	54	Right	H	uP_Right	Active L
P3.5	55	Reset_46	H	uP_Reset_46	Active L
P3.4	56	Down	H	uP-Down	Active L
P3.3	57	UP	H	uP_UP	Active L
P3.2	58	Left	H	uP_Left	Active L
P3.1	59	Exit	H	uP_Exit	Active L
	60	Vcc	H	uP_Vcc 3.3V	Active L
P3.0	61	Power	H	uP_Power	Active L
	62	Vss	~	~	
P2.7	63	Nc	~	~	
P2.6	64	Nc	~	~	
P2.5	65	LED_A	L	Amber Color LED Enable	Active H
P2.4	66	LED_G	H	Green Color LED Enable	Active H
P2.3	67	Pixelsel	~	~	
P2.2	68	Nc	~	~	
P2.1	69	Nc	~	~	
P2.0	70	Nc	~	~	

Port	Pin No	Signal Name	Initial Seeting	Function	Remark
P1.7	71	Nc	H	Green Color LED Enable	
P1.6	72	Nc	~	~	
P1.5	73	Nc	~	~	
P1.4	74	Nc	~	~	
P1.3	75	Nc	~	~	
P1.2	76	Nc	~	~	
P1.1	77	Nc	~	~	
P1.0	78	Nc	~	~	
P0.7	79	Nc	~	~	
P0.6	80	IIC_SCL	~	uP_SCL	
P0.5	81	IIC_SDA	~	uP_SDA	
P0.4	82	Nc	~	~	
P0.3	83	Nc	~	~	
P0.2	84	Nc	~	~	
P0.1	85	Nc	~	~	
P0.0	86	Nc	~	~	
P10.7	87	Nc	~	~	
P10.6	88	Nc	~	~	
P10.5	89	Nc	~	~	
P10.4	90	Nc	~	~	
P10.3	91	Nc	~	~	
P10.2	92	Nc	~	~	
P10.1	93	Nc	~	~	
	94	Avss	~	uP_A-D Analog GND	
P10.0	95	Nc	~	~	
	96	Vref	~	uP_A-D Reference Voltage	
	97	Avcc	~	uP_Analog Vcc 3.3V	
P9.7	98	Nc	~	~	
P9.6	99	Panel_VCTL	H	Panel Power Supply Enable	Active H
P9.5	100	Reset_Out	L	Reset Signal at Lower Level with 20 Clock	Active L

10. Inverter

10.1 Circuit Diagram

TAD617 BLOCK DIAGRAM



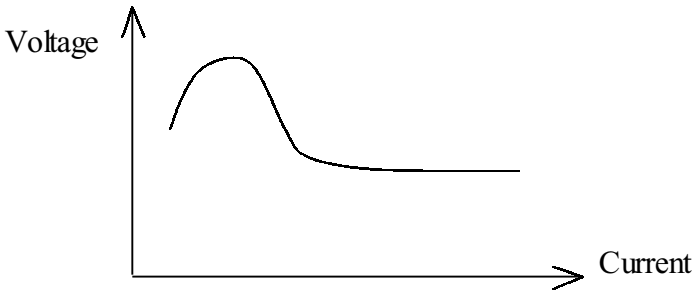
10.2 Inverter basic function

The used loading are CCFL, brightness and electric characteristic will be influence by difference Lamp length, Lamp radius and difference air in the Lamp or ambient temperature. So we explain the principle on the list.

(1) Step 1.: We light the lamp by input about 900~1800V ac voltage on the electrode of lamp, at this time we named starting voltage.

(2) Stup 2.: After light up the lamp, cause by the current, impedance of the lamp will goes down so the voltage on the lamp will also decrease to a satble state, at this time we call the voltage on the lamp named working voltage. For keeping the lihgting, that need current flow on the lamp, at this time we named the current to be output current.

(3) Stup 3.: Voltage-Current characteristic



10.3 Circuit explain

(1) ON/OFF control:

We use electric switch to control O2 IC`s Vcc voltage

ON state: Vcc ¡Ö5V

OFF state: Vcc ¡Ö0V

(2) PWM control:

For the wide range to control brightness, it is necessary to put on a DC/DC converter circuit, this circuit use O2 OZ965 control IC (list on Fig 2.)

- The lamp current is ac current, we use integral circuit to transform ac voltage to dc voltage, and then input to differential amplifier of control IC.
- Change the brightness will also change the output of DC/DC converter, then make the output current to the set value.
- The detailed application circuit can refer to OZ965 data book.

(3)L/C oscillator control:

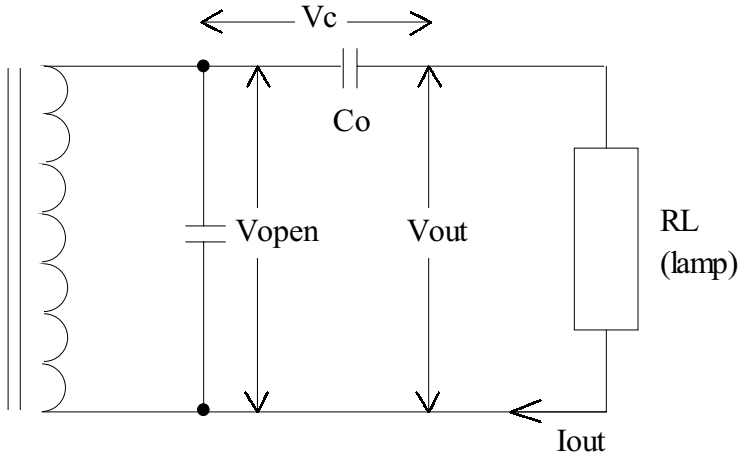
- Use O2 circuit frame, let N- P- power MOSFET switch on and off, get up to L/C resonance.
- Frequency: $\frac{1}{2\sqrt{k\,Lp(Cp+Co`)}}$

Lp: transformer leaking inductance
Cp:resonance capacitor
Co`:the value of secondary ballast capacitor distancement to primary.

(4)Transformer:

Use turn ratio to produce a high voltage, cause of the hight voltage it is important to take care of reliability and safty.

(5)Output:



The loading of lamp before lighting up=∞, the loading after lighting

$$up = \frac{Vout}{Iout}$$

Before lighting up: Vout=Vopen, Vc=0

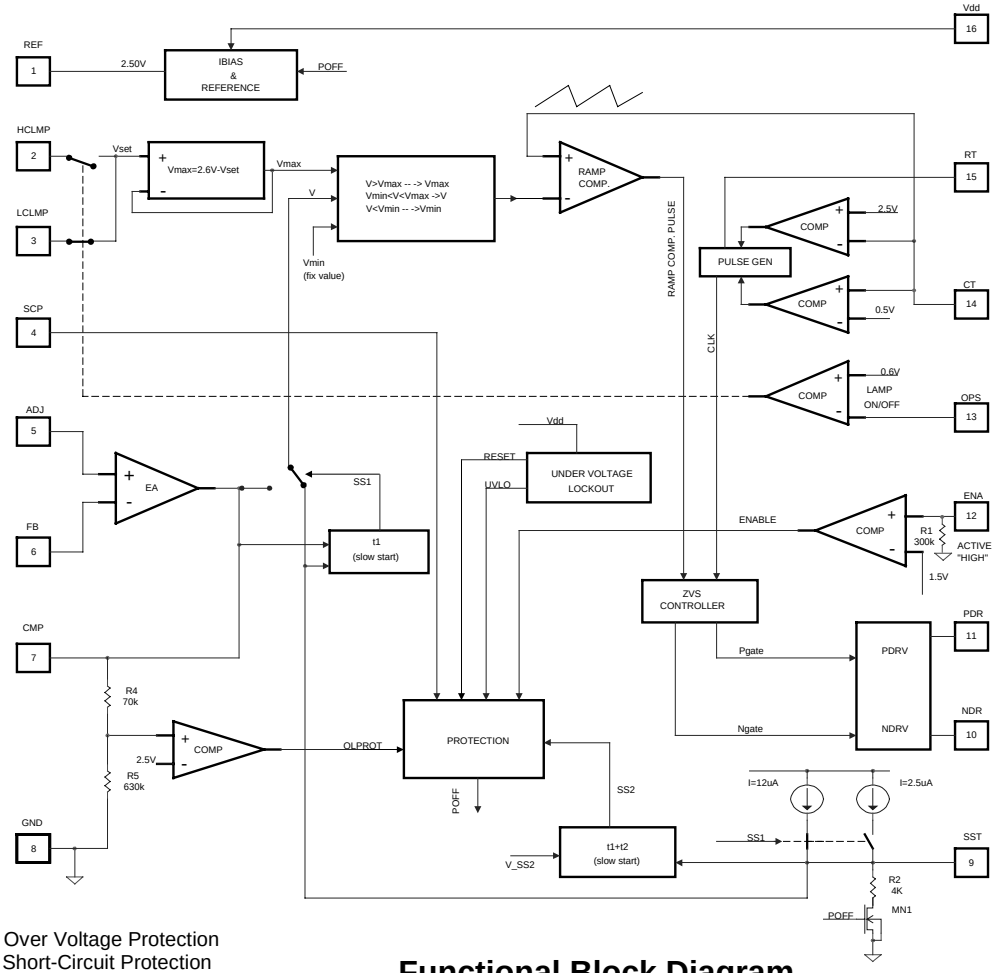
After lighting up: Vout=lamp voltage

Vc=Vopen-Vout

- The output current was decide by Co capacitor and CCFL equivalent impedance.

(6) Feedback loop:

For sensor output current, we change the ac voltage to dc voltage and connector to error amplifier of control IC, to stable the output current.



Note:
OVP – Over Voltage Protection
SCP – Short-Circuit Protection
UVL – Under Voltage Lockout

Functional Block Diagram

11. USB circuit

11.1 USB description

The USB IC AT43301 (I201), port 0 (pin 14, 15) is a full speed port. A 1.5K ohm (R201) pull-up resistor to the 3.3V regulator output CEXT (I201, pin 3) is required for proper operation. the downstream ports support both full-speed as well as low-speed devices, 15K ohm (ex. R217) pull down resistors are required at their input (I201 pin 16 ~ pin 23). Full speed signal requirments demand controlled rise/fall times and impedance matching of the USB ports to meet these requirements 22 ohm (ex: R209) resistor must be inserted in series between the USB data pins (I201 pin 14 - pin 23) and the USB connectors.

Note:$\overline{\text{OVC}}$. The overcurrent signal control circuit (D201, Q201, Q205) is read through the I201 pin 9. A logic low at OVC is interperted as an overcurrent condition. This could be caused by an circuit overload, or a short states.

11.2 USB hub control circuit

I203 is a reset IC, and I201 is a USB hub control IC made by ATMEL.

NOTE: When the monitor power circuit is turned on, a 5V power is fed to I203. Upon the detection of about 4. 5V, I203 begins to generate a reset signal of 450msec. Than control Q204 to turn on Q203 input Vcc to I201when I201 enables communication with a higher port when UD+ and UD- from the USB connector are applied to pin 14 and pin 15, respectively. Pin 16, 17, 18, 19, 20, 21, 22 and 23 are connected to the USB connector of the lower port. They function as a communication interface between lower and higher ports. If an overcurrent is generated in the lower port, it is transferred to the higher port.

X201 is a crystal oscillator that supplies a 6MHz clock signal to the USB hub control IC (I201).

11.3 Lower port circuit

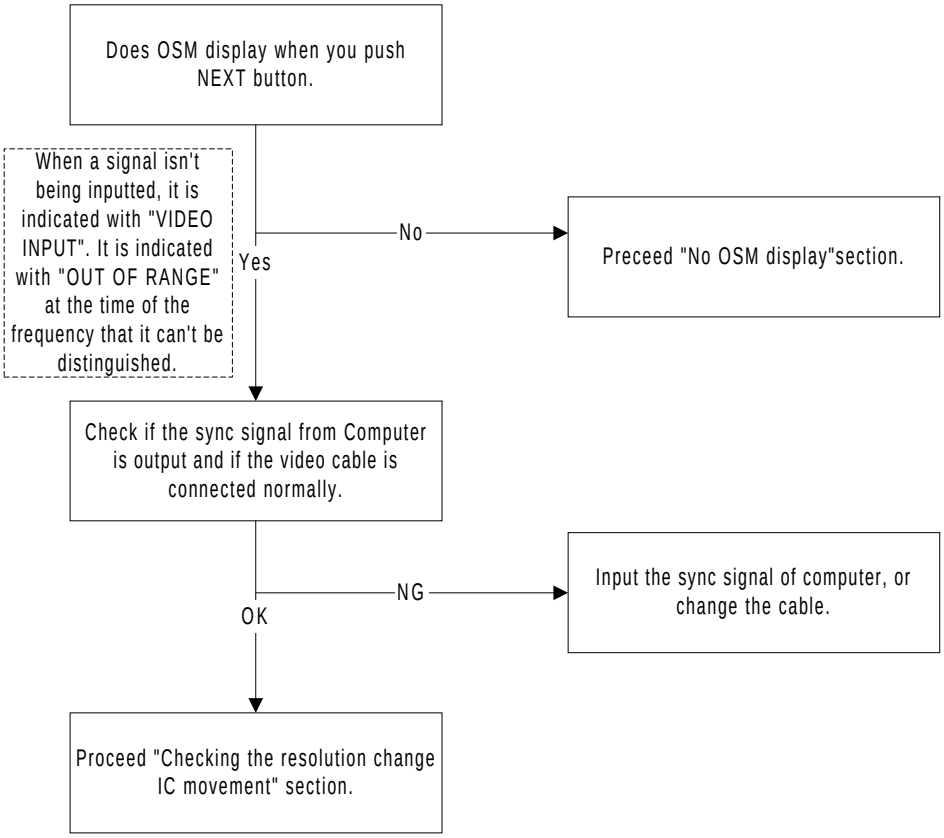
J203, J204, J205 and J206 are the USB lower-port connector.

The 5V output from the power supply passes through the poly-switches of R202, R205, R206 and R225, and is led to the power supply pins (pin 1 of each connector) of the USB lower-port connector.

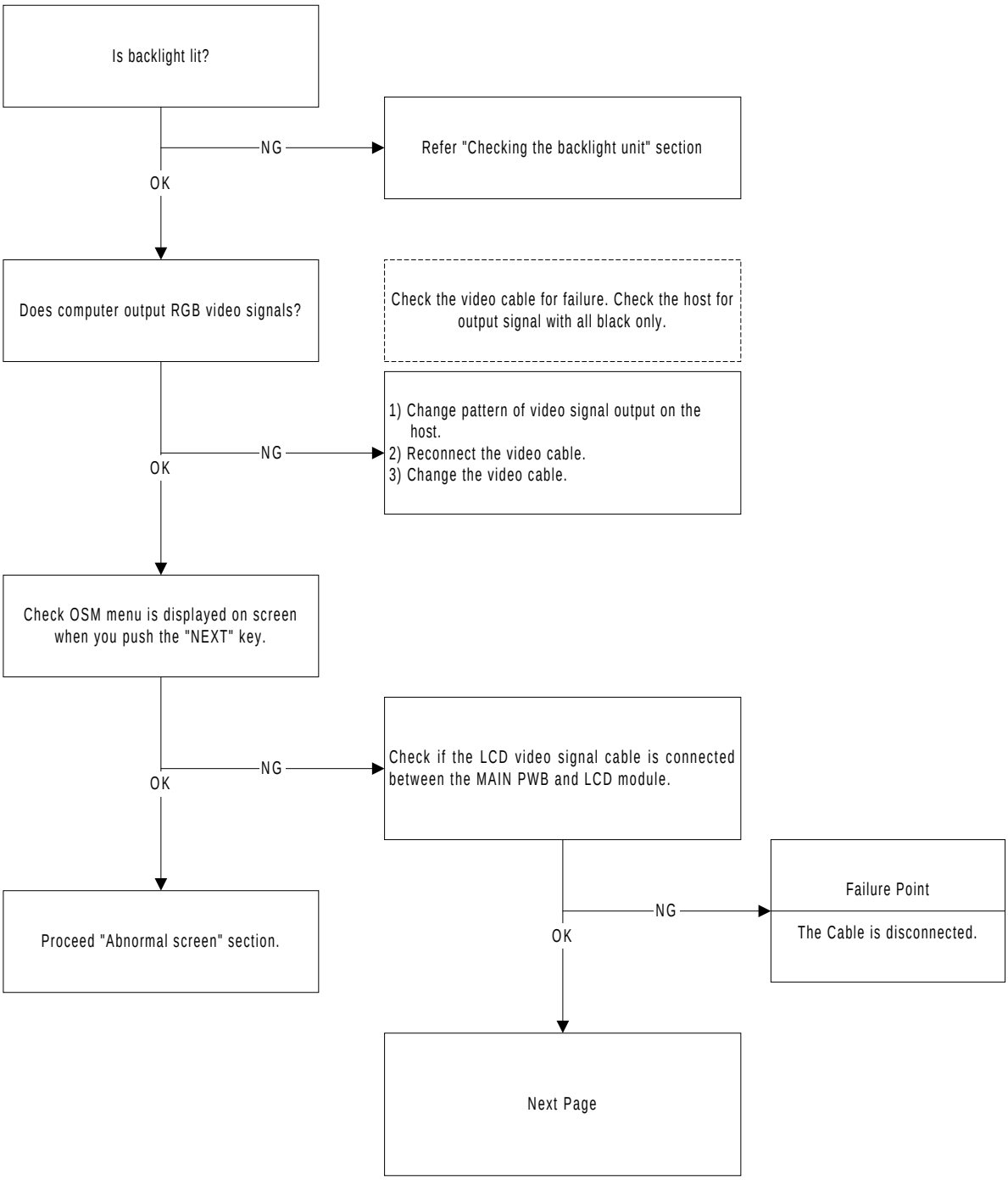
An overcurrent signal is given from the poly-switch - USB lower-port connector line to I201 overcurrent has been generated in the lower port.

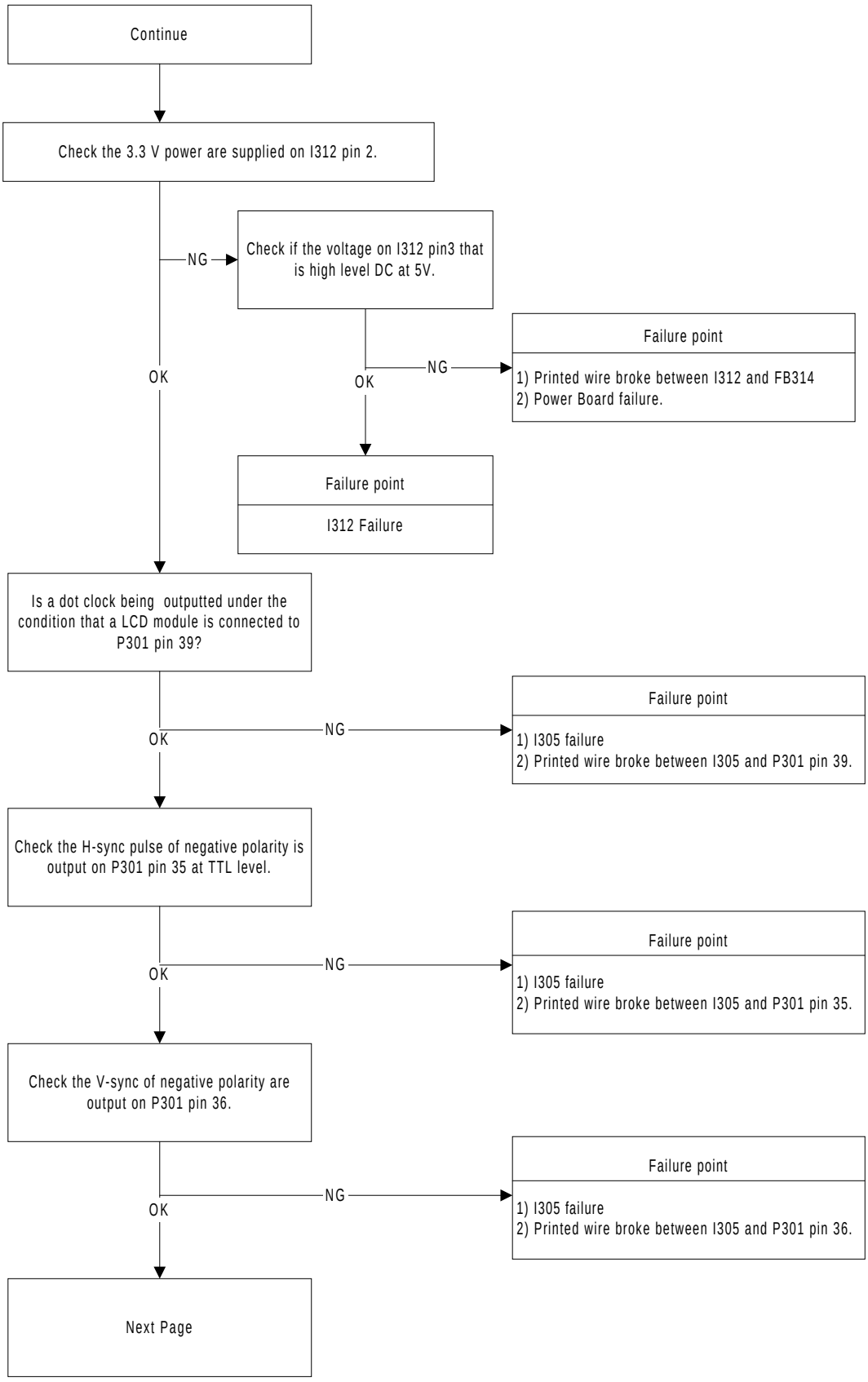
Table of Contents

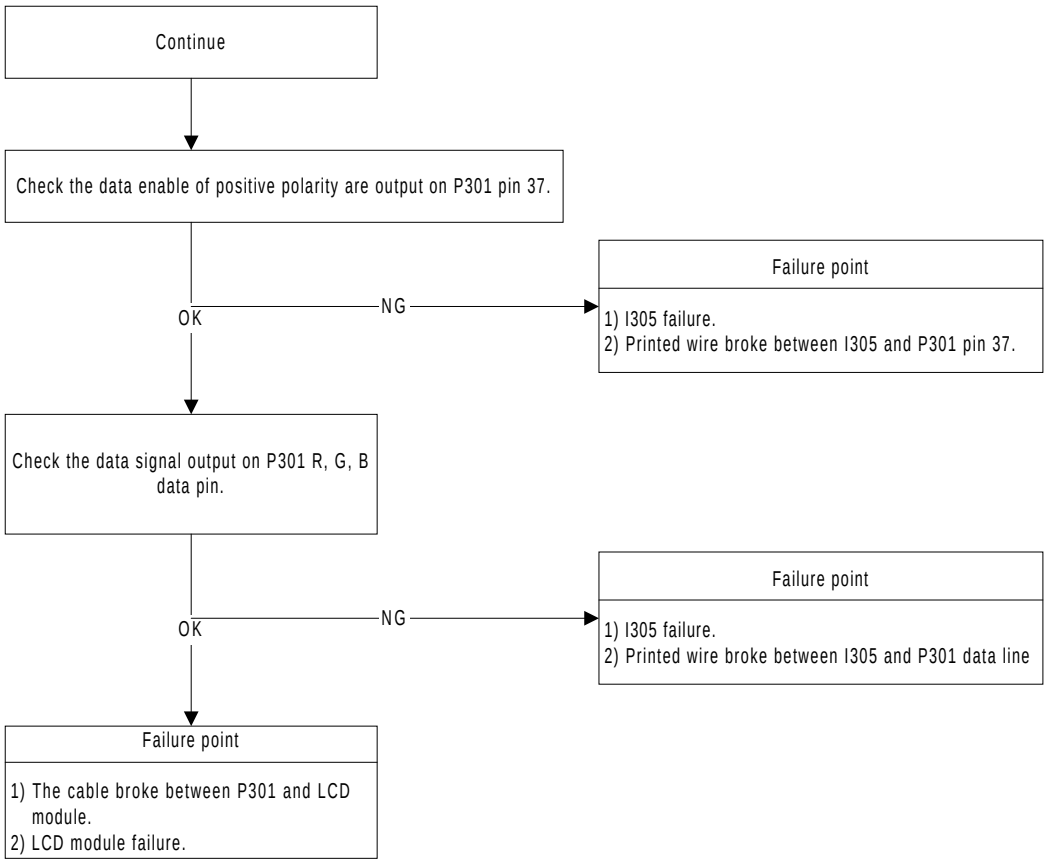
1. No display of screen (Screen is black, color of LED is amber)



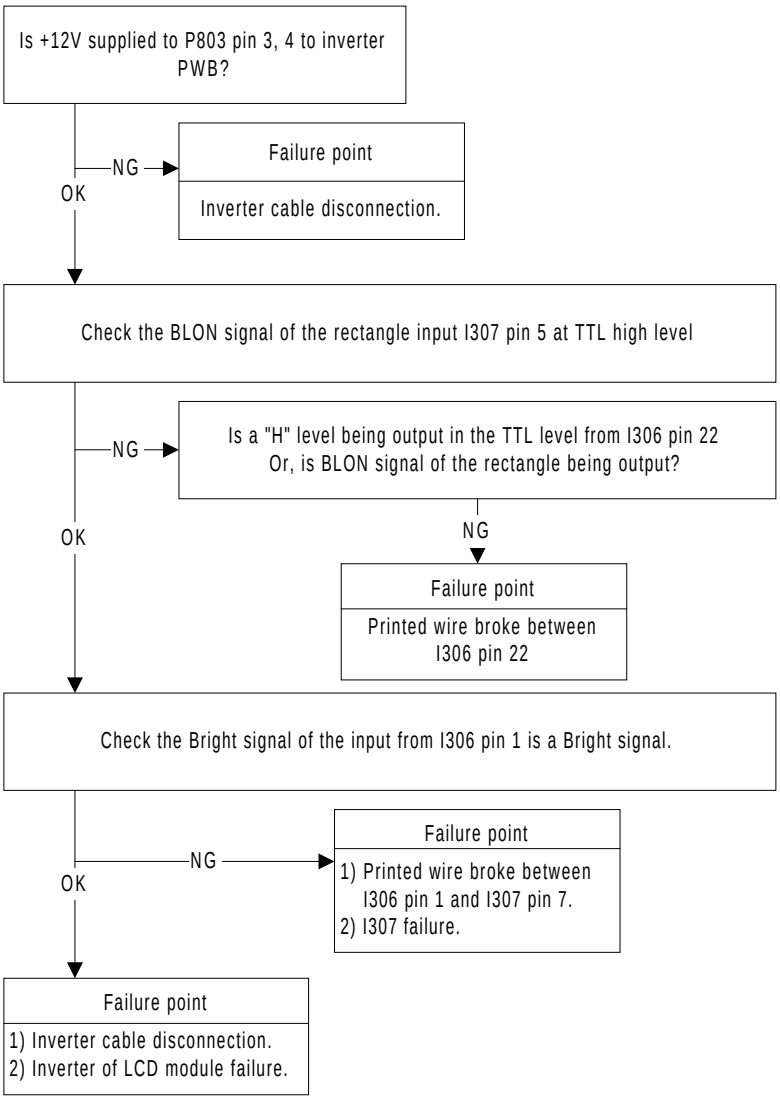
2. Nothing displays on screen (Screen is black, color of LED is green)



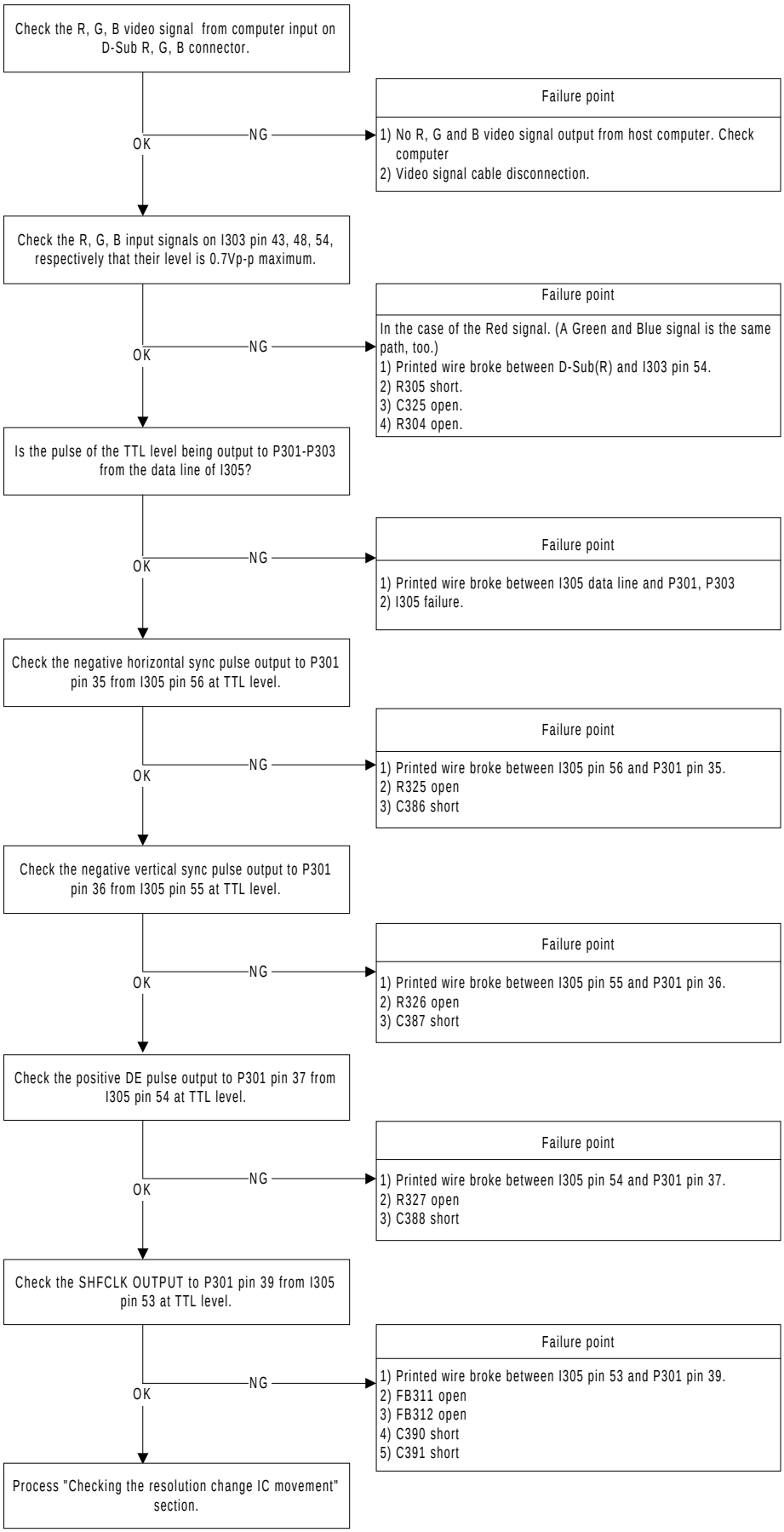

Continue
Check the 3.3 V power are supplied on I312 pin 2.
NG
Check if the voltage on I312 pin3 that is high level DC at 5V.
OK
NG
OK
Failure point
1) Printed wire broke between I312 and FB314
2) Power Board failure.
Failure point
I312 Failure
Is a dot clock being outputted under the condition that a LCD module is connected to P301 pin 39?
OK
NG
Failure point
1) I305 failure
2) Printed wire broke between I305 and P301 pin 39.
Check the H-sync pulse of negative polarity is output on P301 pin 35 at TTL level.
OK
NG
Failure point
1) I305 failure
2) Printed wire broke between I305 and P301 pin 35.
Check the V-sync of negative polarity are output on P301 pin 36.
OK
NG
Failure point
1) I305 failure
2) Printed wire broke between I305 and P301 pin 36.
Next Page


Continue
Check the data enable of positive polarity are output on P301 pin 37.
OK
NG
Failure point
1) I305 failure.
2) Printed wire broke between I305 and P301 pin 37.
Check the data signal output on P301 R, G, B data pin.
OK
NG
Failure point
1) I305 failure.
2) Printed wire broke between I305 and P301 data line
Failure point
1) The cable broke between P301 and LCD module.
2) LCD module failure.

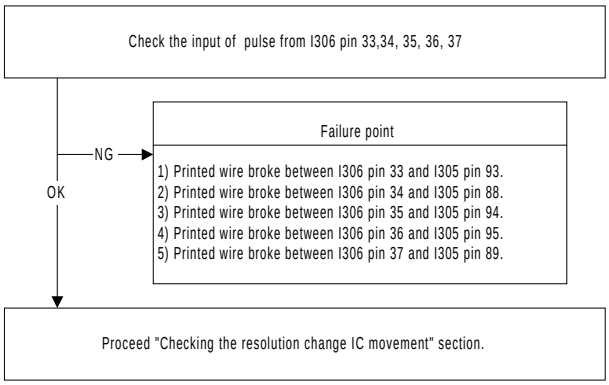
3. Checking the back light unit



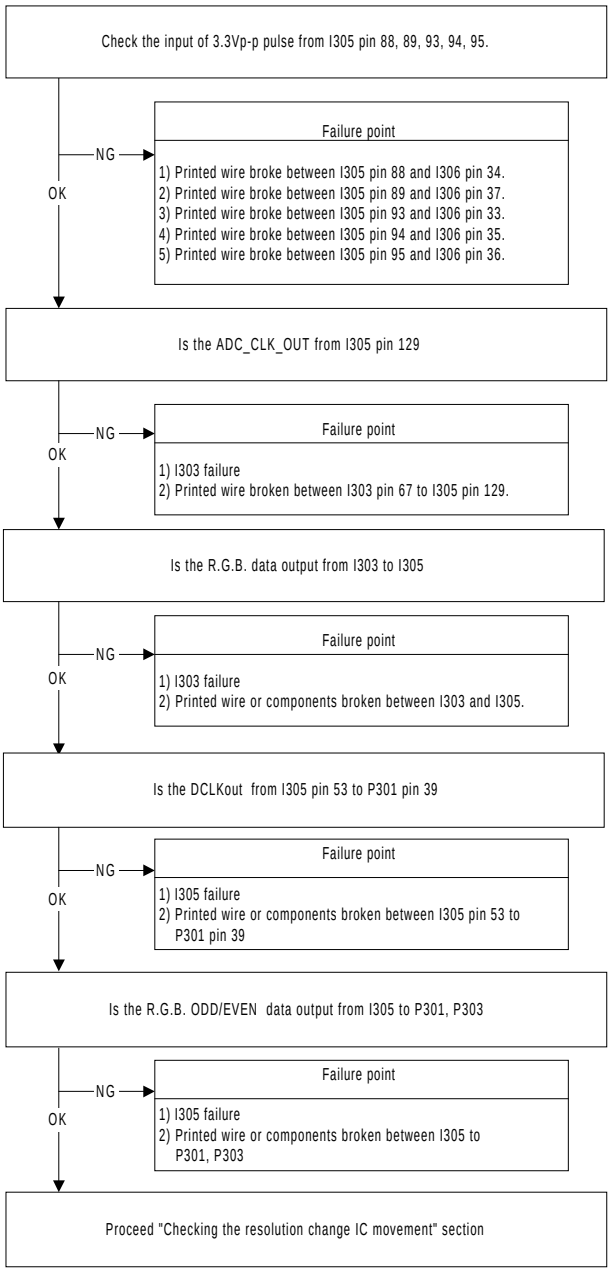
4. Abnormal screen



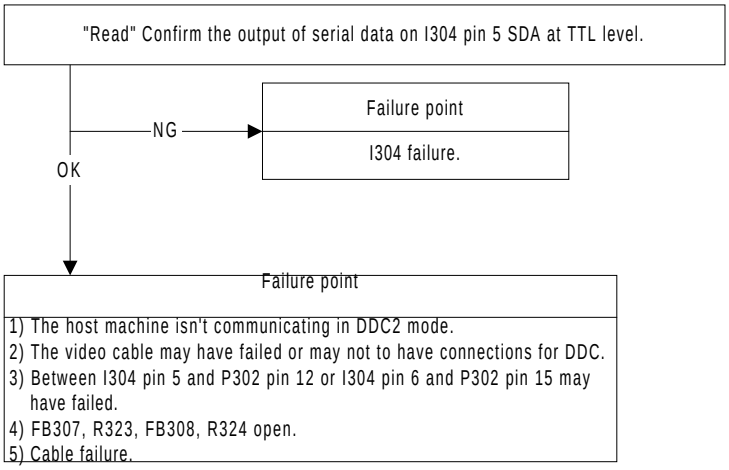
5. No OSM display

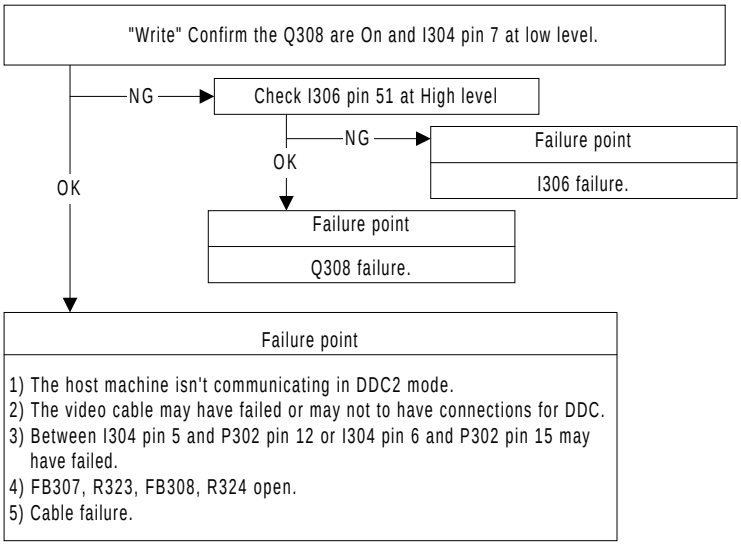


6. Abnormal auto adjustment



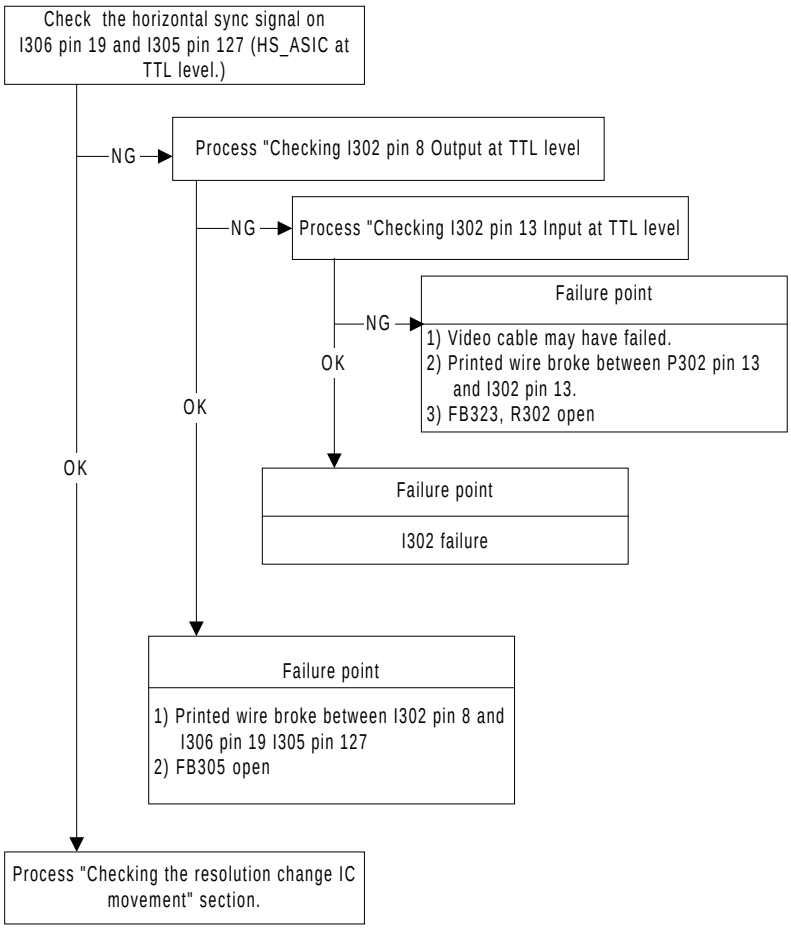
7. Abnormal plug and play operation (*Abnormal DDC2*)



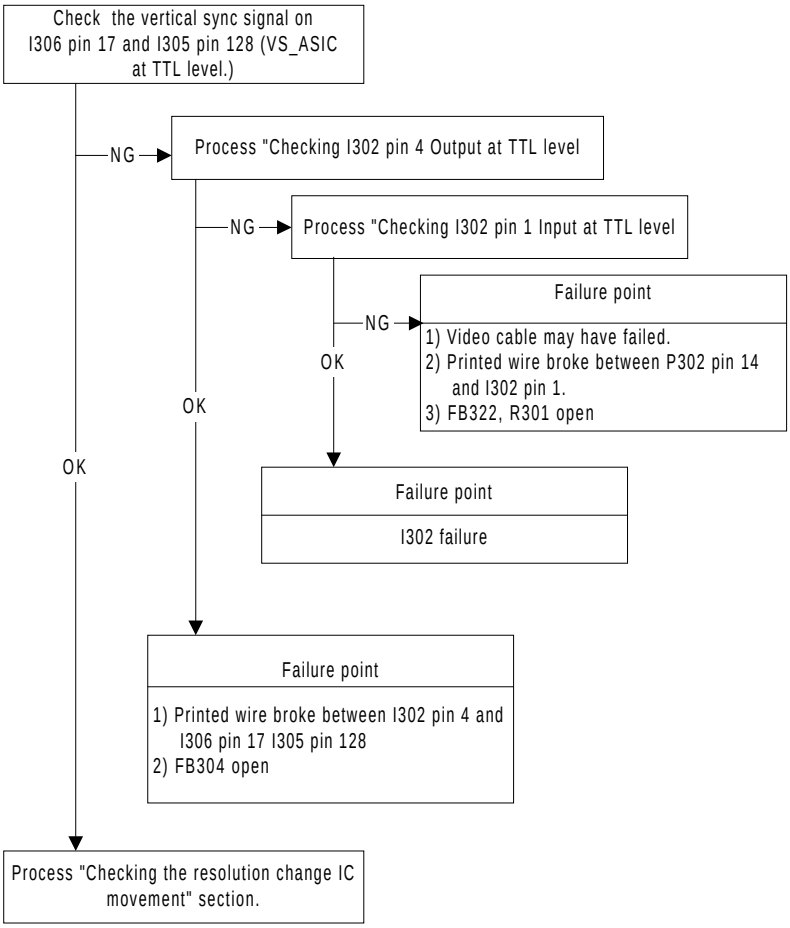


8. Checking the interface circuit of sync signal

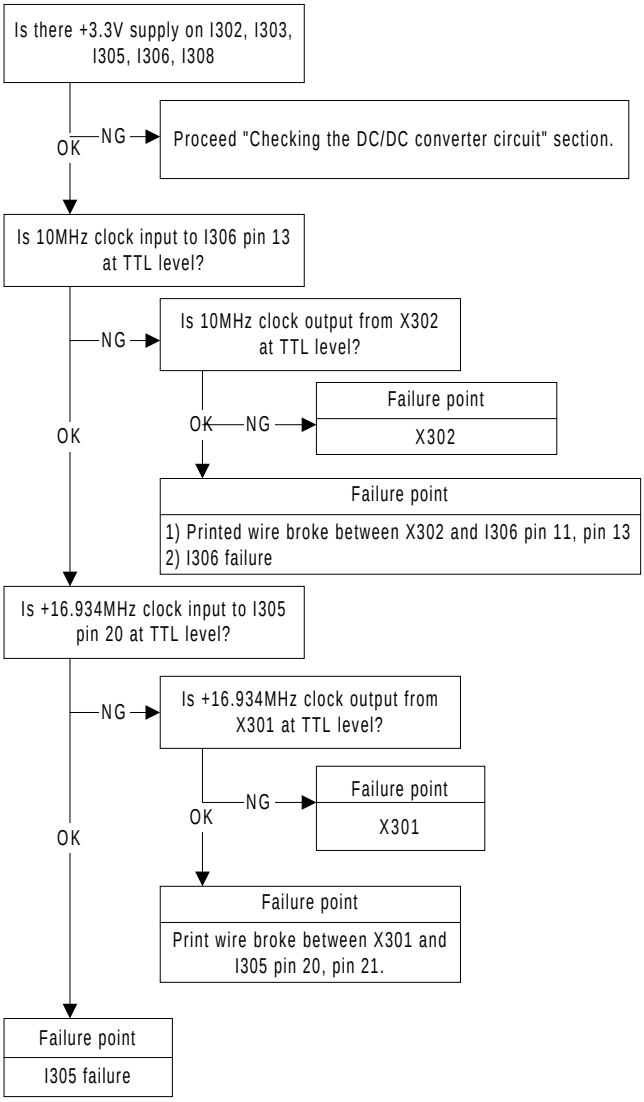
8.1 Checking the control circuit of horizontal sync pulse



8.2 Checking the control circuit of Vertical sync pulse

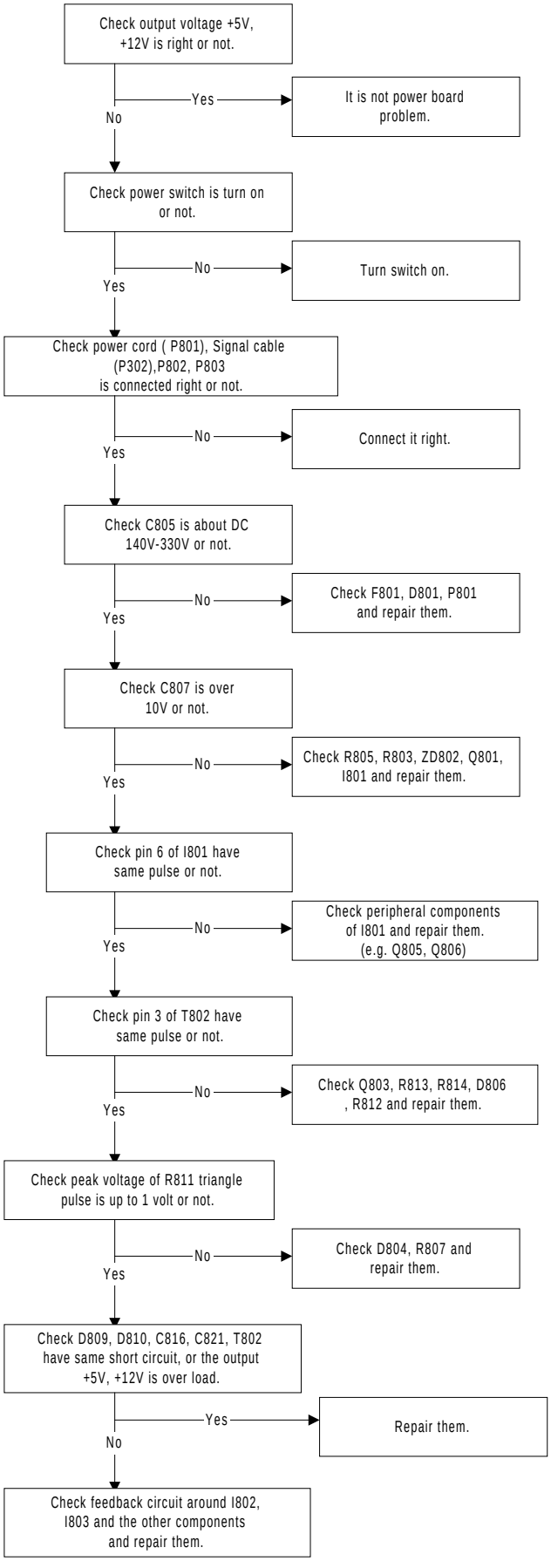


9. Checking the resolution change IC movement

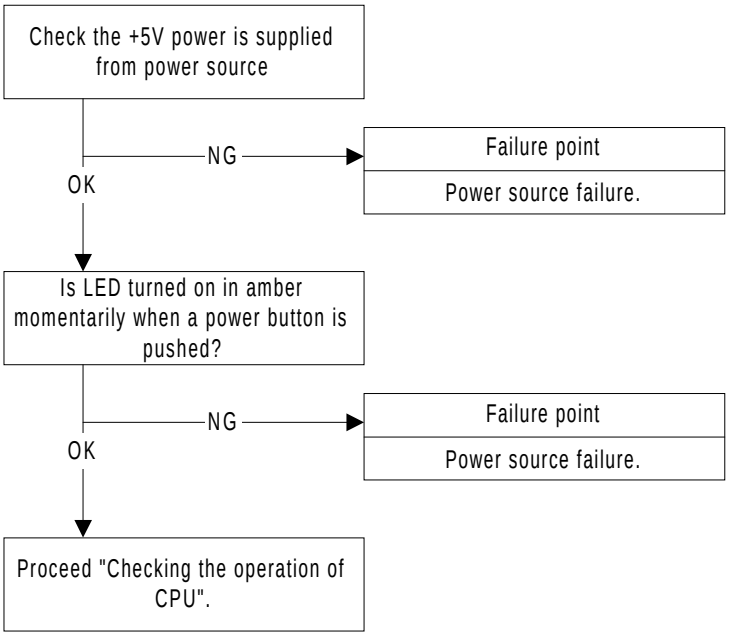


10. No power on

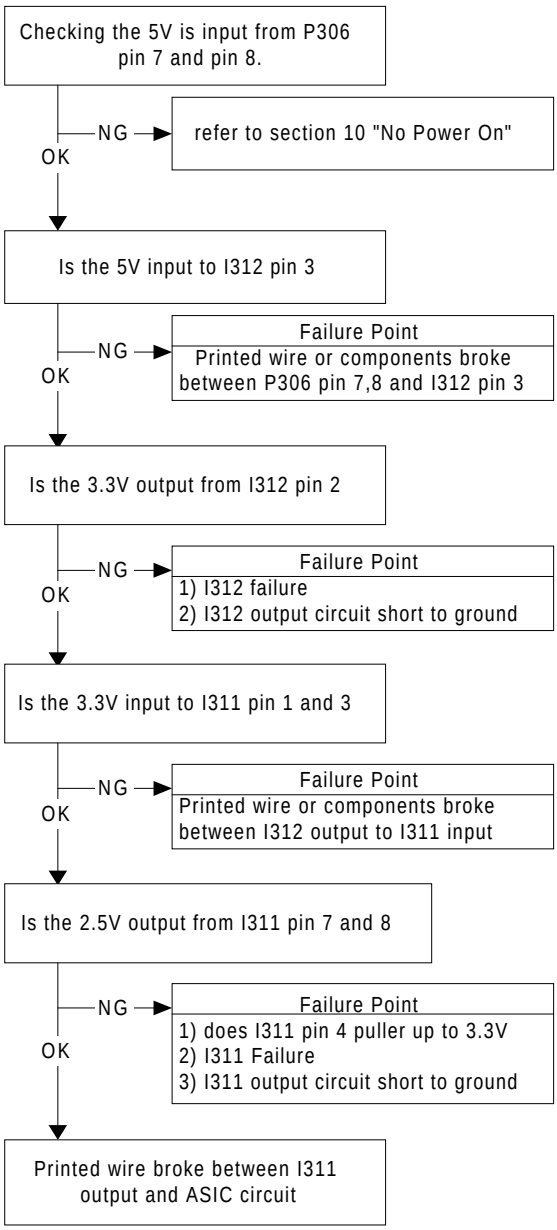
10.1 No power on (I)



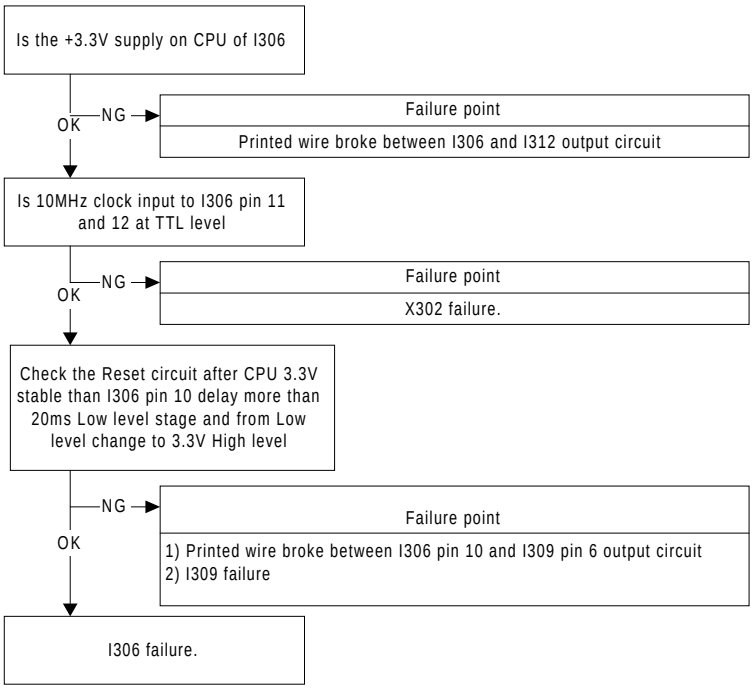
10.2 No power on (II)



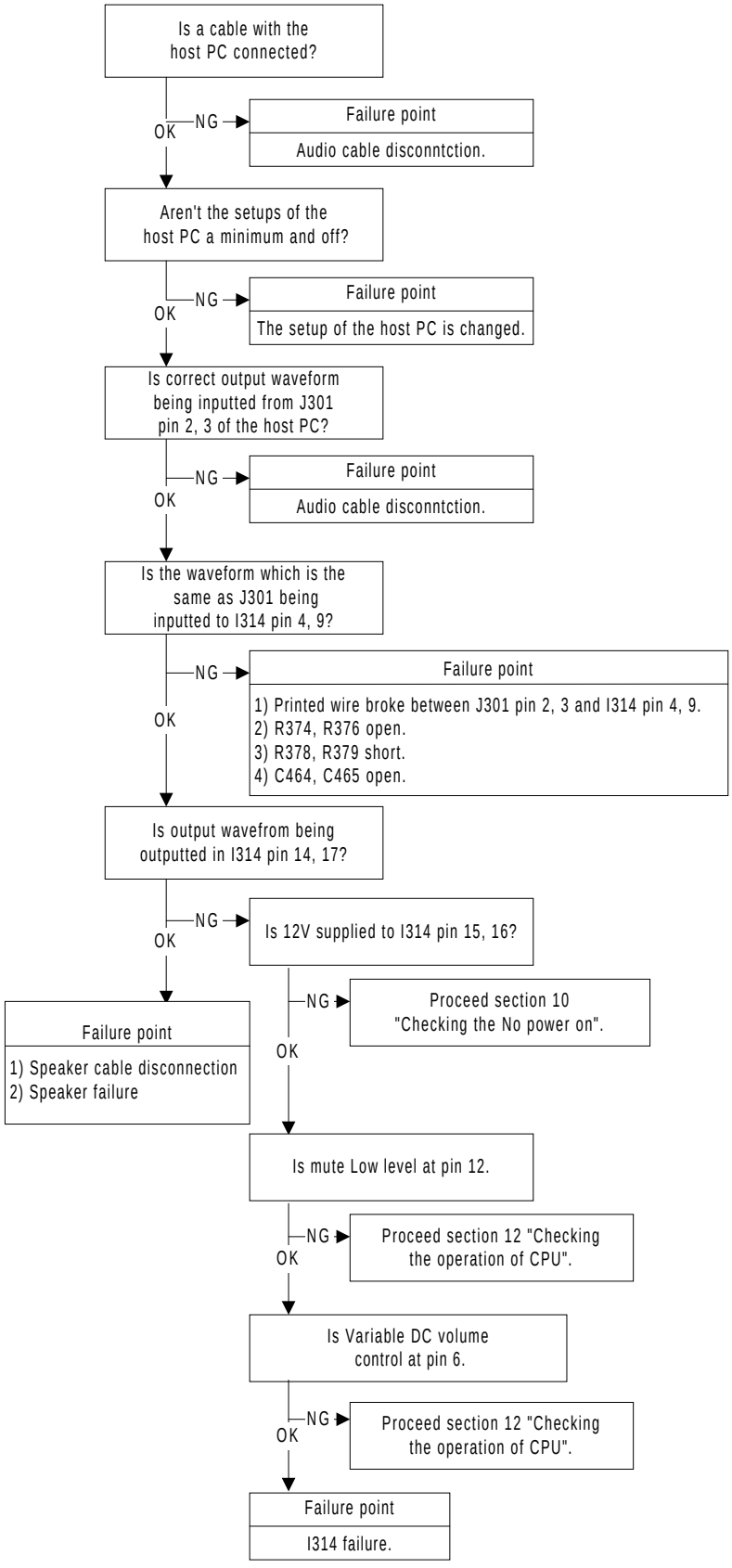
11. Checking the DC/DC converter circuit



12. Checking the operation of CPU

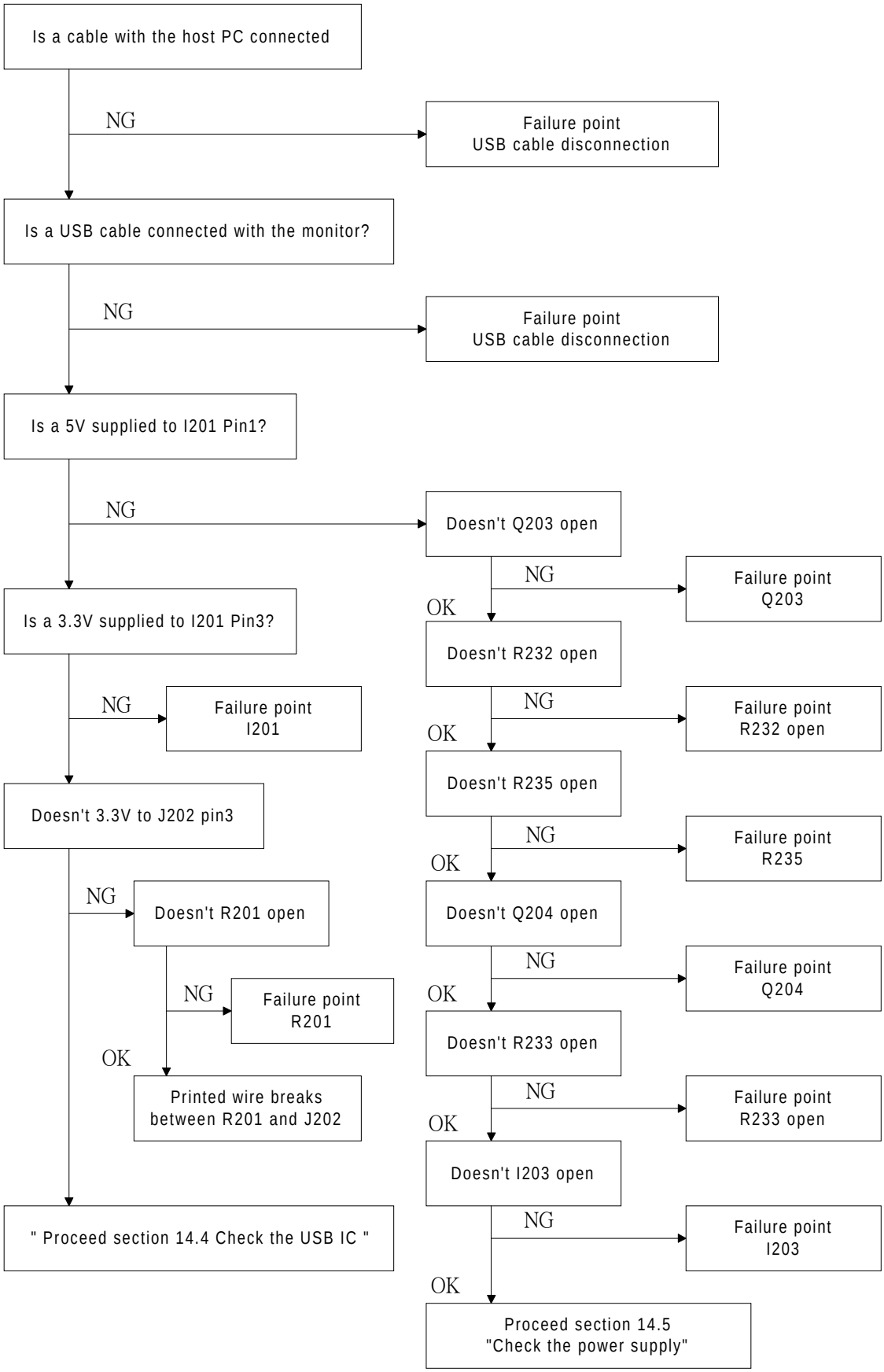


13. Checking the audio circuit

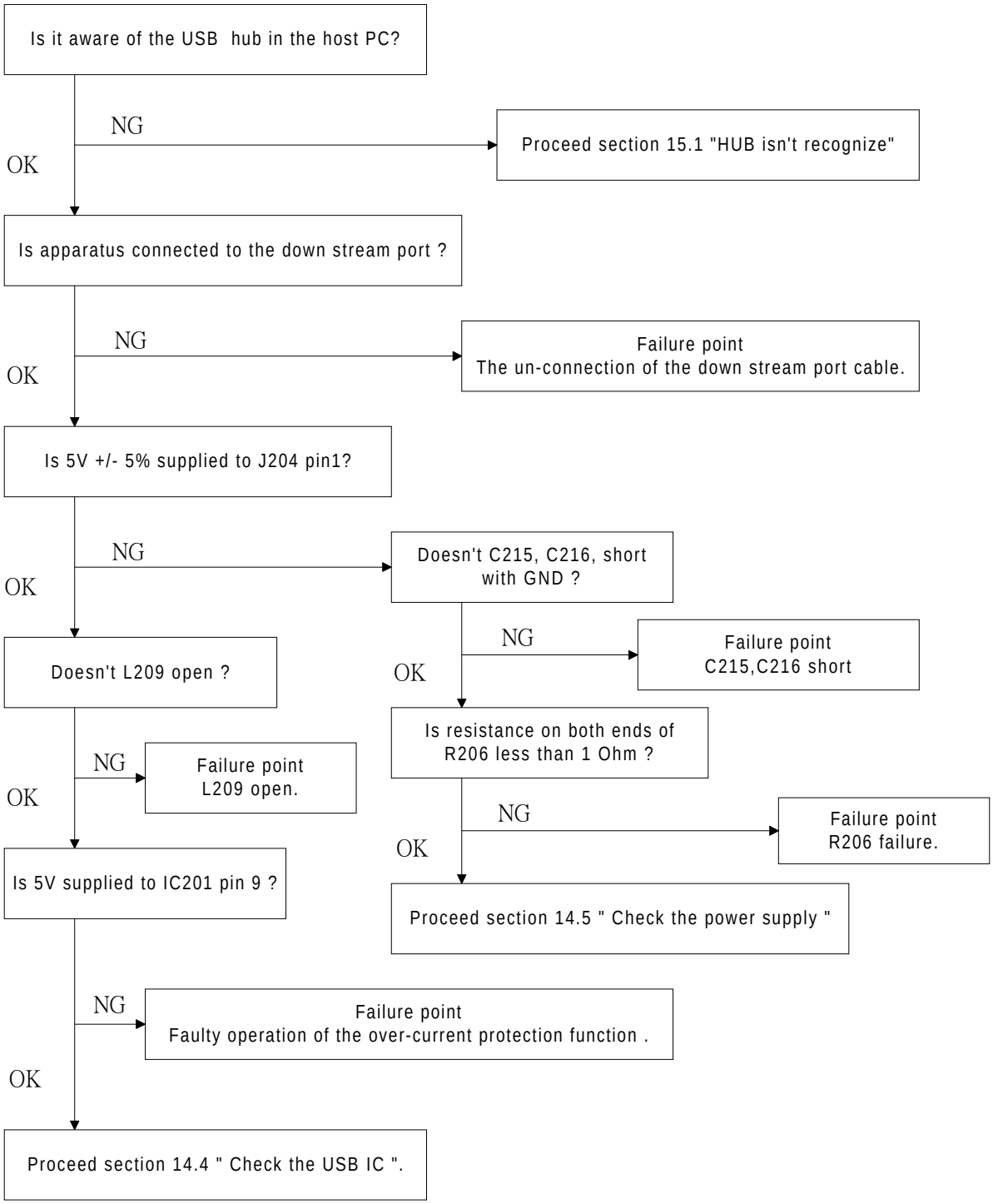


14. Check the USB hub circuit

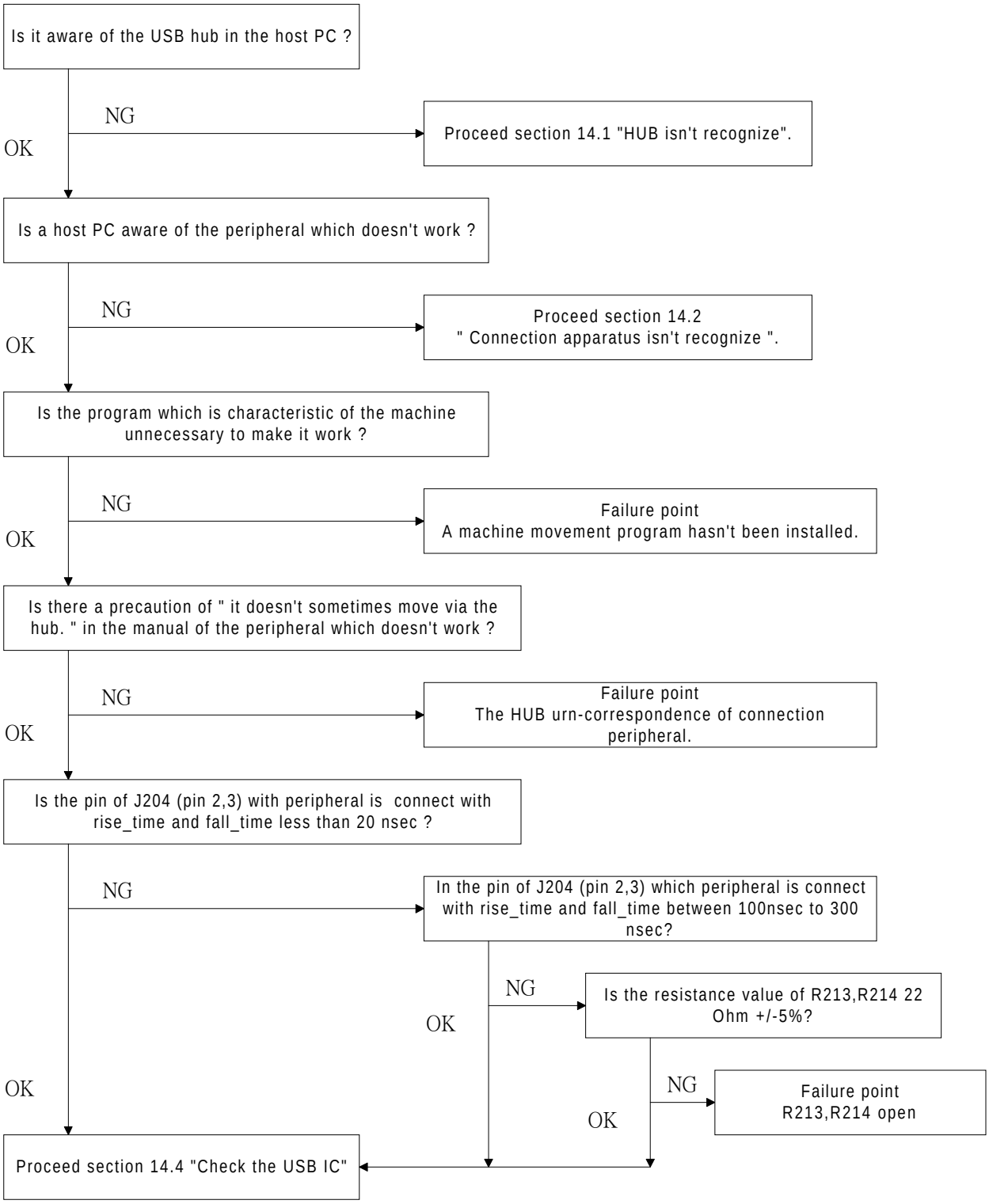
14.1 Hub isn't recognize



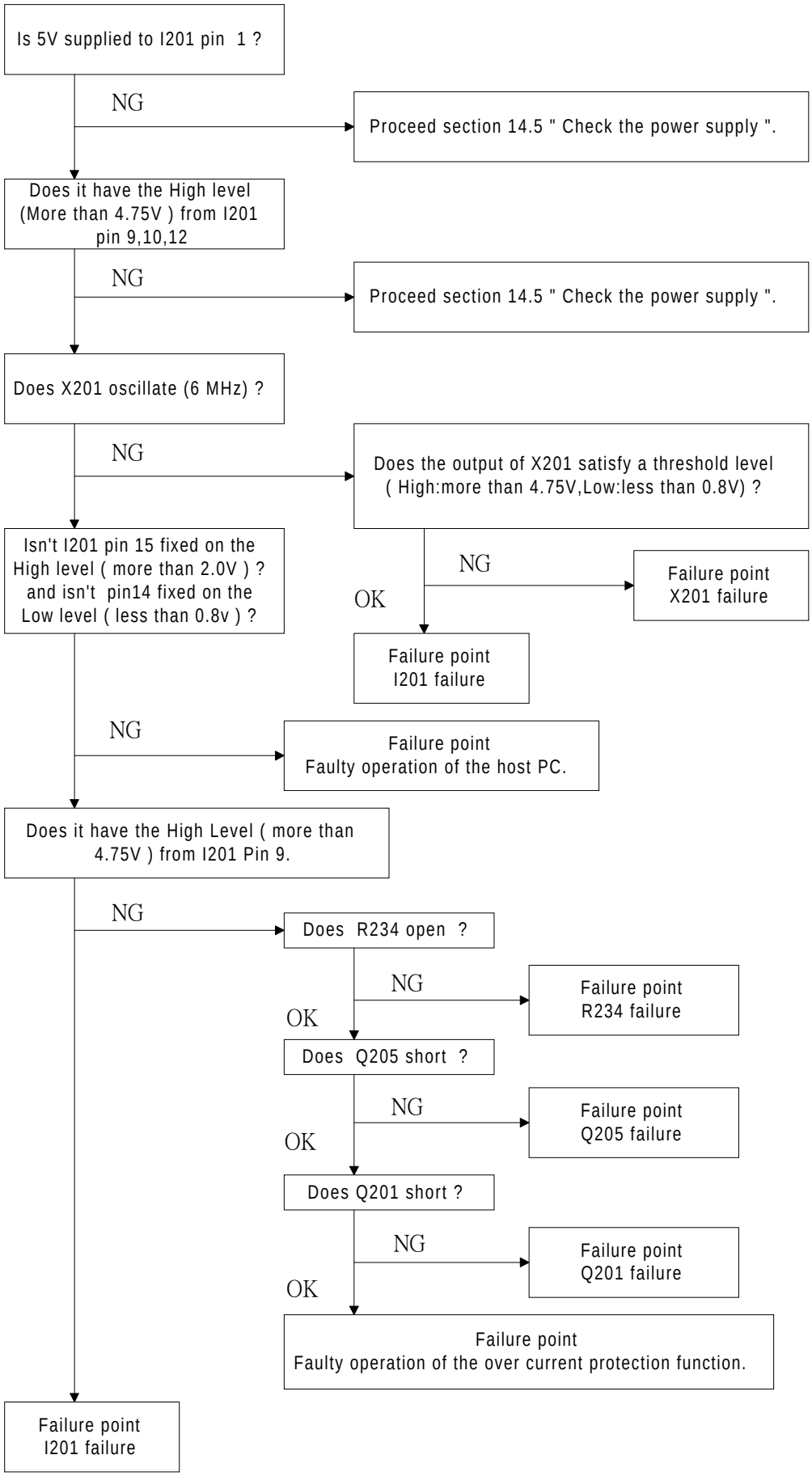
14.2 Connection apparatus isn't recongnize



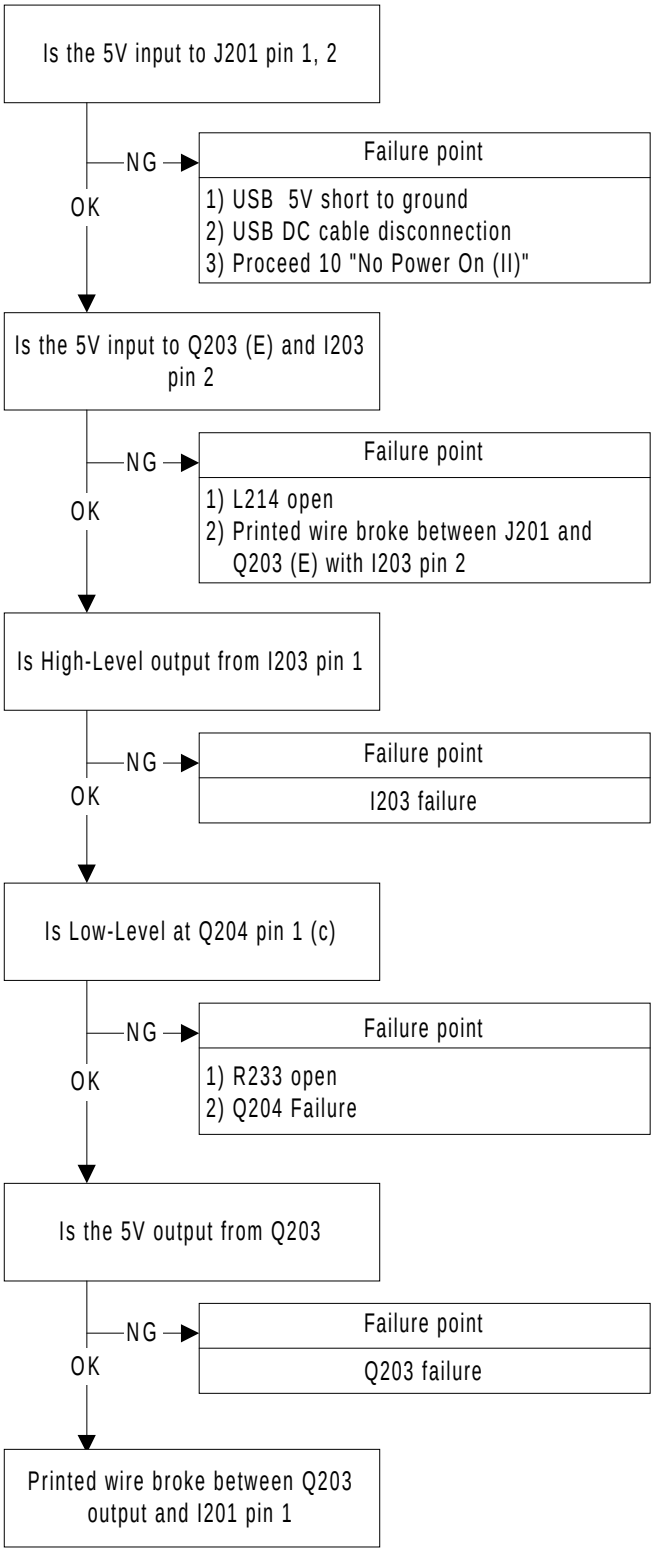
14.3 Connection apparatus doesn't work



14.4 Check the USB IC



14.5 Check the power supply



1. Recommended Parts List

Note: 1. The components identified by " ⚠ " mark are critical for X-ray safety. Replace these with only the same parts specified.

2. There is only OTP IC at the model beginning (FPR stage or before). When it put in mass production and there must be Mask coming out. Please refer BOM to get the last release part number and related information.

No.	Location	Part Number	Description
1 ⚠	INVA	6716009300	INVERTER-DC-AC 12V TAD-617-TDK
2 ⚠	0000	5113300151	INTERFACE BD-NMV-FA150ATUA(99)
3	D308	6412019508	DIODE DAN217 SMD3 T146 ROH
4	D309	6412001738	DIODE RLS4148 LL-34 SMD RO
5	D310	6413040128	DIODE-SCHOTTKY-SS14-1A/40V-SMD
6	D311	6414056038	DIODE-ZNR-RLZ TE-11 5.6B LL-34
7	D312	6412019418	DIODE RLS-73 TE-11 LL-34
8	I301	6442023338	IC-Linear-AIC1086-33CY-3P-SOT-
9	I302	6446006218	IC-TTL-74LVC14-14P-TSSOP-TI
10	I303	6444009508	IC-CMOS-AD9883-80P-MQFP-AD
11	I304	6448018208	IC-24LC02B-8PIN-SOP-MICROCHIP
12	I305	6444009608	IC-CMOS-M66611FP 44P6Q-A-MIT
13	I306	6448017908	IC-CPU-M30620FGMGP-100P-6Q-A-M
14	I307	6442001908	IC-LM358DT-8P-SOP-ST-
15	I308	6448018308	IC-24LC32A-8P-SOP-MICROCHIP-0.33
16	I309	6442028608	IC-Linear-M51957AFP-8P-SOP-MIT
17	I311	6442028308	IC-Linear-SI3025LS-8P-SOP-SANK
18	I312	6442023326	IC-Linear-AIC1084-33CM-3P-TO26
19	Q303	6428000208	FET-N&P-CHNL-2SK3018 ROHM
20	Q306	6422007308	TRANSISTOR-NPN-SST3904-T116 S
21	Q307	6427002508	FET-P-CHNL-SI2305DS-VISHAY
22	Q310	6423002308	TRANSISTOR-PNP-2SA1037AK-T146/
23	I314	6442023100	IC-Linear-TDA7496L-20P-PDIP-SG
24	X301	6449002550	CRYSTAL-16.9344MHz TOPIC-30pp

No.	Location	Part Number	Description
25	X302	6449006108	CRYSTAL-10MHz-49S-TOPIC-16PF
26 ⚠	00000	5113700005	CONRTOL BD-USB BD-NEC-FA150ATU
27	I201	6448015808	IC-CPU/PROM-AT43301-24P-SOIC-A
28	0I203	6444006810	IC-MOS-MCP130-450DI TO92-MICR
29	0Q201	6423000708	TRANSISTOR-PNP-SST3906-T116
30	0X201	6449006800	CRYSTAL-6.0MHz-49S-TOPICS-20pF
31 ⚠	00000	5114300004	CONTROL BD-POWER-NEC-FA150ATUA
32	D801	6417001000	DIODE BRIDGE TS4B05G 01 TSC
33	D802	6412001704	DIODE 1N4148 T26 NS
34	D803	6412007924	DIODE SWITCHING FUF4006AMP 1A
35	D804	6412004347	DIODE FUF4002AMP 1A/100V T52
36	D809	6412015210	DIODE YG902C 02 10A/200V FU
37	D810	6417000720	DIODE BRIDGE YG802C04 FUJI
38	I801	6442022010	IC-Linear KA3842AE S 8P PDIP F
39	I802	6442014000	IC-Linear LTV 817D 4P PDIP LIT
40	I803	6442001340	IC-Linear ka431az 3P TO 92 Vre
41	Q801	6421005800	TRANSISTOR NPN KSP44 TO 92 FA1
42	Q802	6421006005	TRANSISTOR NPN KRC102M VI=30V
43	Q803	6426006700	FET N CHEL SSS7N60A SAMSUNG
44	Q805	6421006005	TRANSISTOR NPN KRC102M VI =30V
45	Q806	6410000105	THYRISTOR 5V/400V 126 BT169

NEC

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