## MITSUBISHI

# SERVICE MANUAL 

## color monitor Diamond Plus 74SB

## MODELS DPLUS 74SB -BK(A)/(B)

NEC-MITSUBISHI ELECTRIC VISUAL SYSTEMS CORPORATION MAY 2002

The SERVICE PERSONNEL should have the appropriate technical training, knowledge and experience necessary to:

- Be familiar with specialized test equipment, and
- Be careful to follow all safety procedures associated with high voltage CRT circuit designs to minimize danger to themselves and their coworkers.

To avoid electrical shocks, this equipment should be used with an appropriate power code and be connected only to a properly grounded AC outlet.

This equipment utilized a micro-gap power switch. Turn off the set by first pushing the front panel power switch. Next, remove the power cord from the AC outlet.

To prevent fire or shock hazards, do not expose this unit to rain or moisture.


This symbol warns the personnel that un-insulated voltage within the unit may have sufficient magnitude to cause electric shock.
This symbol alerts the personnel that important literature concerning the operation and maintenance of this unit has been included.
Therefore, it should be read carefully in order to avoid any problems.

1. When parts replacement is required for servicing, always use the manufacturer's specified replacement.
2. Comply with all caution and safety-related notes on the product display chassis and picture tube.
3. When replacing the component, always be certain that all the components are put back in the place.
4. When servicing display monitor unit, it is required that the provided lead dress is used in the high voltage circuit area.
5. It is also recommended that shatter proof goggles are worn, when removing installing and handling the picture tube. People not equipped with the proper precautionary measures mentioned should keep the picture tube away from body while handling.
6. As for a connector, pick and extract housing with fingers properly since a disconnection and improper contacts may occur, when wires of the connector are led.
7. Use a proper screwdriver. If you use screwdriver that does not fit, you may damage the screws.
8. X-radiation precaution

This product contains critical electrical and mechanical parts essential for X-ray protection.
Normal anode voltage is 25.5 kV at zero beam picture tube current under AC 100-120V/220-240V input, and anode voltage must not exceed the voltages shown below under any operation condition.
To measure anode voltage set brightness for very dim picture, and use a high impedance volt meter between chassis and anode lead and measure high voltage.
If high voltage exceeds the specifications on the chassis schematic diagram, take the necessary corrective action.

Table MAXIMUM ANODE VOLTAGE

| beam current | at 0 mA | at 0.6 mA | at 1.2 mA |
| :---: | :---: | :---: | :---: |
| A/B Ver. | 31.0 kV | 30.5 kV | 30.5 kV |

9. When you degauss the set with an external degaussing coil, you must keep strictly item " * Notes about degaussing method " of ADJUSTMENT Procedures.

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## User's Manual

## 1. A Version

## $\therefore$ MITSUBISHI

USER'S MANUAL


16" Viewable Image Size
www.mitsubishidisplay.com

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## 4 CAUTION <br> RISK OF ELECTRIC SHOCK • DO NOT OPEN <br> CAUTION: TO REDUCE THE RISK OF ELECTRIC SHOCK, DO NOT REMOVE COVER (OR BACK). NO USER SERVICEABLE PARTS INSIDE. REFER SERVICING TO QUALIFIED SERVICE PERSONNEL.

This symbol warns user that uninsulated voltage within the unit may have sufficient magnitude to cause electric shock. Therefore, it is dangerous to make any kind of contact with any part inside this unit.
This symbol alerts the user that important literature concerning the operation and maintenance of this unit has been included. Therefore, it should be read carefully in order to avoid any problems.

## Canadian Department of Communications Compliance Statement

DOC: This Class B digital apparatus meets all requirements of the Canadian Interference-Causing Equipment Regulations.
C-UL: Bears the C-UL Mark and is in compliance with Canadian Safery Regulations according to C.S.A. C22. 2 No. 950.

## FCC Information

1. Use the attached specified cables with the Diamond Plus $74^{\text {SB }}$ color monitor so as not to interfere with radio and television reception.
(1) Please use the supplied power cord or equivalent to ensure FCC compliance.
(2) Shielded captive type signal cable.

Use of other cables and adapters may cause intereference with radio and television reception.
2. This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy, and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment offand on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult your dealer or an experienced radio/TV technician for help.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.
If necessary, the user should contact the dealer or an experienced radio/television technician for additional suggestions. The user may find the following booklet, prepared by the Federal Communications Commission, helpful: "How to Identity and Resolve Radio-TV Interference Problems." This booklet is available from the U.S. Government Printing Office, Washington, D.C., 20402, Stock No. 004-000-00345-4.

## Contents

Your new Diamond Plus $74^{\text {SB }}$ monitor box* should contain the following:

- Diamond Plus $74^{\text {SB }}$ Monitor with tilt/swivel base
- Power Cord
- Captive Signal Cable
- User's Manual


Captive Signal Cable


* Remember to save your original box and packing material to transport or ship the monitor.

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## Quick Start

To attach the Diamond Plus monitor to your system, follow these instructions:

1. Turn off the power to your computer.
2. If necessary, install the display card into your system. For more information, refer to the display card manual
3. For the PC: Connect the 15-pin mini D-SUB of the captive signal cable to the connector of the display card in your system (Figure A.1). Tighten all screws.
For the Mac: Connect the Diamond Plus Macintosh cable adapter (not included) to the monitor connector on the Macintosh (Figure B.1). Attach the 15 -pin mini D-SUB end of the captive signal cable to the Diamond Plus Macintosh cable adapter on the computer (Figure B.1). Tighten all screws.

## NOTE: To obtain the Diamond Plus $74^{\text {SB }}$ Macintosh cable adapter, call

 NEC-Mitsubishi Electronics Display of America, Inc. at (800) 632-4662.4. For download information on the Windows ${ }^{\circledR} 95 / 98 / \mathrm{Me} / 2000 / X P$ INF file for your Diamond Plus monitor, refer to the References section of this User's Manual.
5. Connect one end of the power cord to the Dimond Plus monitor and the other end to the power outlet (Figure C.1).
6. Turn on the monitor (Figure D.1) and the computer.

NOTE: If you have any problems, please refer to the Troubleshooting section of this User's Manual.


## Quick Start -continued



Figure D. 1

## Controls

$\mathrm{OSM}^{\text {m＂}}$（On－Screen Manager）control buttons on the front of the monitor function as follows：

| EXIT | Main Menu <br> Exits the OSM menu． |
| :--- | :--- |
| CONTROLMoves the highlighted <br> area left／right to select <br> one of the sub－menus． | Sub－Menu <br> Exits to the OSM controls <br> main menu． <br> Moves the highlighted area <br> left／right to select one of the <br> controls． |
| －／＋ |  |

## ：

Brightness：Adjusts the overall image and background screen brightness． Contrast：Adjusts the image brightness in relation to the background． Degauss：Eliminates the buildup of stray magnetic fields which alter the correct scan of the electron beams and affect the purity of the screen colors，focus and convergence．When activated，your screen image will jump and waver a bit as the screen is demagnetized．
Caution：Please allow a minimum of $\mathbf{2 0}$ minutes to elapse between uses of the Degauss Control．

## 田が Size and Position Controls

Left／Right：Moves the image horizontally（left or right）．
Down／Up：Moves the image vertically（up or down）．
Narrow／Wide：Decreases or increases the horizontal size of the image．
Short／Tall：Decreases or increases the vertical size of the image．

## Controls -continued

## R(R1B) Color Control/AccuColor ${ }^{\bullet}$ Control System

Color presets selects the desired color setting. The bar is replaced by the color setting choice. Each color setting is adjusted at the factory to the stated Kelvin. If a setting is adjusted, the name of the setting will change from Kelvin to Custom except sRGB mode.
Red, Green, Blue: AccuColor Control System decreases or increases the monitor's red, green or blue color guns depending upon which is selected. The change in color will appear on screen and the direction (decrease or increase) will be shown by the bars.
sRGB mode: sRGB mode provides the suitable color managed picture image. You can not change Red, Green and Blue colors, brightness and contrast individually. Color Temperature Adjustment: Adjusts the color temperature of the screen image.

## $\square \square$ Geometry Controls

Geometry Controls Menu
The Geometry controls allow you to adjust the curvature or angle of the sides of your display.
Sides In/Out (pincushion): Decreases or increases the curvature of the sides either inward or outward.
Sides Left/Right (pincushion balance): Decreases or increases the curvature of the sides either to the left or right.
Sides Tilt (parallelogram): Decreases or increases the tilt of the sides either to the left or right.
Sides Align (trapezoidal): Decreases or increases the bottom of the screen to be the same as the top.
Rotate (raster rotation): Rotates the entire display clockwise or counterclockwise.

## Tools 1

Moiré Canceler: Moiré is a wavy pattern which can sometimes appear on the screen. The pattern is repetitive and superimposed as rippled images. When running certain applications, the wavy pattern is more evident than in others. To reduce moiré, adjust the level by using -/+ CONTROL buttons.

## Tools 2

Language: OSM controls menus are available in 6 languages.
OSM Position: You can choose where you would like the OSM controls menu to appear on your screen. Selecting OSM Position allows you to manually adjust the OSM controls menu position from among Center, Top left, Top right, Bottom left and Bottom right.
OSM Turn Off: The OSM controls menu will stay on as long as it is in use. In the OSM Turn Off sub-menu, you can select how long the monitor waits after the last touch of a button for the OSM controls menu to disappear. The preset choices are 5 thru 120 seconds.

## Controls -continued

OSM Lock Out: This control completely locks out access to all OSM controls functions except Brightness and Contrast. When attempting to activate OSM controls while in the lock out mode, a screen will appear indicating that OSM controls are locked out. To activate the OSM Lock Out function, press SELECT and hold + down simultaneously. To deactivate the OSM Lock Out, press SELECT and hold + down simultaneously.
IPM ${ }^{m "}$ System Off Mode: Enable: The IPM System works normally and all stages of energy savings are utilized.
Disable: The Off Mode of the IPM
System is not used.
NOTE: For standard systems and graphics boards, keep the factory setting at ENABLE.
Factory Preset: Selecting Factory Preset allows you a reset most OSM ${ }^{\text {mw }}$ control settings back to the factory settings. A warning statement will appear to confirm that you do want to reset ALL settings. Individual settings can be reset by highlighting the control to be reset and pressing the RESET button.

## 1 Information

Display Mode: Indicates the current mode and frequency setting of the monitor. Monitor Info: Indicates the model and serial numbers of your monitor.
Refresh Notifier: A message will advise you if the refresh rate of the signal being applied to the monitor by the computer is too low. For further information, please refer to your display card or system manual.

## Recommended Use

## Safety Precautions and Maintenance

## FOR OPTIMUM PERFORMANCE, PLEASE NOTE THE FOLLOWING WHEN SETTING UP AND USING THE DIAMOND PLUS COLOR MONITOR:

- DO NOT OPEN THE MONITOR. There are no user serviceable parts inside and opening or removing covers may expose you to dangerous shock hazards or other risks. Refer all servicing to qualified service personnel
- Do not spill any liquids into the cabinet or use your monitor near water.
- Do not insert objects of any kind into the cabinet slots, as they may touch dangerous voltage points, which can be harmful or fatal or may cause electric shock, fire or equipment failure.
- Do not place any heavy objects on the power cord. Damage to the cord may cause shock or fire.
- Do not place this product on a sloping or unstable cart, stand or table, as the monitor may fall, causing serious damage to the monitor.
- Keep the monitor away from high capacity transformers, electric motors and other devices such as external speakers or fans, which may create strong magnetic fields.
- If possible, position the monitor so that it is facing the east to minimize the effects of the earth's magnetic field.
- Changing the direction of the monitor while it is powered on may cause image discoloration. To correct this, turn the monitor off for 20 minutes before powering it back on.
- When operating the Diamond Plus $74^{\mathrm{SB}}$ with its $\mathrm{AC} 220-240 \mathrm{~V}$ worldwide power supply, use a power supply cord that matches the power supply voltage of the AC power outlet being used. The power supply cord you use must have been approved by and comply with the safety standards of your country. (Type H05VV-F should be used except in UK)
- In UK, use a BS-approved power cord with molded plug having a black (5A) fuse installed for use with this monitor. If a power cord is not supplied with this monitor, please contact your supplier.


## Cleaning Your Monitor

A special coating is provided on the glass (CRT) surface of this monitor to reduce a reflection and static electricity on the glass surface. Due to the delicate coating on the glass surface, use a lint-free, non-abrasive cloth (cotton or equivalent) and a non-alcohol, neutral, non-abrasive cleaning solution to minimize dust. If the screen requires more than a light cleaning, apply a soft neutral detergent and water directly to a soft cloth and use it upon wringing water, to clean the glass surface. Clean your monitor regularly
CAUTION: The following agents will cause damage to the CRT when cleaning the glass surface: Benzene, thinner, acid/alkaline detergent, alcohol detergent, detergent with abrasive powder, detergent with anti-static agent, detergent for cleaning

Immediately unplug your monitor from the wall outlet and refer servicing to qualified service personnel under the following conditions:

- When the power supply cord or plug is damaged.
- If liquid has been spilled, or objects have fallen into the monitor.
- If the monitor has been exposed to rain or water.
- If the monitor has been dropped or the cabinet damaged.
- If the monitor does not operate normally by following operating instructions.
- Allow adequate ventilation around the monitor so that heat can properly dissipate. Do not block ventilated openings or place the monitor near a radiator or other heat sources. Do not put anything on top of monitor.
The power cable connector is the primary means of detaching the system from the power supply. The monitor should be installed close to a power outlet which is easily accessible.
- Handle with care when transporting. Save packaging for transporting.


## Recommended Use -continued

CORRECT PLACEMENT AND ADJUSTMENT OF THE MONITOR CAN REDUCE EYE, SHOULDER AND NECK FATIGUE. CHECK TH FOLLOWING WHEN YOU POSITION THE MONITOR:

- Adjust the monitor height so that the top of the screen is at or slightly below eye level. Your eyes should look slightly downward when viewing the middle of the screen.
- Position your monitor no closer than 16 inches and no further away than 24 inches from your eyes. The optimal distance is 20 inches.
- Rest your eyes periodically by focusing on an object at least 20 feet away. Blink often.
- Position the monitor at a $90^{\circ}$ angle to windows and other light sources to minimize
 glare and reflections. Adjust the monitor tilt so that ceiling lights do not reflect on your screen.
- If reflected light makes it hard for you to see your screen, use an anti-glare filter.
- Clean your monitor regularly. Use a lint-free, non-abrasive cloth and a non-alcohol, neutral, non-abrasive cleaning solution or glass cleaner to minimize dust.
- Adjust the monitor's brightness and contrast controls to enhance readability.
- Use a document holder placed close to the screen.
- Position whatever you are looking at most of the time (the screen or reference material) directly in front of you to minimize turning your head while you are typing.
- Get regular eye checkups.

Ergonomics
To realize the maximum ergonomics benefits, we recommend the following:

- Adjust the Brightness until the background raster disappears
- Do not position the Contrast control to its maximum setting
- Use the preset Size and Position controls with standard signals
- Use the preset Color Setting and Sides Left/Right controls
- Use non-interlaced signals with a vertical refresh rate between $75-120 \mathrm{~Hz}$
- Do not use primary color blue on a dark background, as it is difficult to see and may produce eye fatigue due to insufficient contrast
For more detailed information on setting up a healthy work environment, call NEC Mitsubishi Electronics Display of America at (888) NEC-MITS, FastFactss" information at (800) 366-0476 and request document \#900108 or write the American National Standard for Human Factors Engineering of Visual Display Terminal Workstations - ANSIHFS Standard No. 100-1988 - The Human Factors Society, Inc. P.O. Box 1369, Santa Monica, California 90406.


## Specifications



## Features

SuperBright ${ }^{\text {TM }}$ Diamondtron ${ }^{\otimes}$ CRT: This patented flat aperture grille CRT delivers an exceptional viewing experience with unprecedented brightness and contrast and a virtually flat image that reduces distortion and glare so that what you see on-screen is what you get on your printed output. The state-of-the-art Mitsubishi PX-DBFTM electron gun and tight 0.25 mm grille pitch delivers precise focus for crisp, clear text and images.

SuperBright ${ }^{T M}$ Mode: With the simple touch of a button, the brightness level of the Diamondron CRT doubles. This function enhances the crispness of images for clarity-conscious applications such as graphics, animation and video
OptiClear® Screen Surface: Further reduces reflection and glare and increases contrast without sacrificing focus level, clarity or brightness.

Dual Dynamic Beam Focus: Provides precise, continuous focus adjustments of the electron beams and optimum image quality, even to the far edges of the screen.

AccuColor ${ }^{\bullet}$ Control System with sRGB: Allows you to change between five color settings on your display to match your personal preference. The sRGB-enabled color matching setting found within AccuColor helps achieve a consistent color environment with other sRGB-enabled hardware and soffware applications.
On Screen Manager (OSM ${ }^{T M}$ ) Controls: Allows you to quickly and easily adjust all elements of your screen image via simple to use on-screen menus.
ErgoDesign ${ }^{\circledR}$ Features: Enhances human ergonomics to improve the working environment, protect the health of the user and save money. Examples include OSM controls for quick and easy image adjustments, tilt/swivel base for preferred angle of vision, space-conscious cabinet design and compliance with MPRII guidelines for lower emissions.
Plug and Play: The Microsoff ${ }^{\oplus}$ solution with the Windows ${ }^{\oplus} 95 / 98 / \mathrm{Me} / 2000 / X P$ operating system facilitates setup and installation by allowing the monitor to send its capabilities (such as screen size and resolutions supported) directly to your computer, automatically optimizing display performance.

Intelligent Power Manager (IPM ${ }^{\text {TM }}$ ) System: Provides innovative power-saving methods that allow the monitor to shift to a lower power consumption level when on but not in use, saving two-thirds of your monitor energy costs, reducing emissions and lowering the air conditioning costs of the workplace.
Reduced Magnetic Field ${ }^{\text {TM }}$ Technology: Reduces magnetic and alternating electric field emissions and static electricity, addressing ergonomic concerns regarding potential risks from extended computer monitor use.

## Features -continued

Multiple Frequency Technology: Automatically adjusts monitor to the display card's scanning frequency, thus displaying the resolution required.
FullScan ${ }^{\text {TM }}$ Capability: Allows you to use the entire screen area in most resolutions, significantly expanding image size.

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## Troubleshooting

## No picture

- Display card should be completely seated in its slot.
- Power Button and computer power switch should be in the ON position.
- Signal cable should be completely connected to display card/computer.
- Check connector for bent or pushed-in pins.


## Image is scrolling or unstable

- Signal cable should be completely attached to the computer.
- Check pin assignments and signal timings of the monitor and your display card with respect to recommended timings and pin assignments.
- If the Macintosh cable adapter is used, check for proper connection or make sure the display card is Macintosh compatible and that the card is properly seated in the computer.
LED on monitor is not lit (no green, orange color can be seen)
- Power Switch should be in the ON position and power cord should be connected.


## LED on monitor is flashing and/or dissapears

- Contact Customer Service at (800) 462-4662.

Picture is fuzzy or color looks blotchy

- Adjust Brightness and Contrast Controls or adjust the Moiré Canceler control.
- Access the Degauss Control through OSM $^{\top M}$ controls. Activate the Degauss Control. CAUTION: A minimum interval of 20 minutes should elapse before the Deguass Control is used a second time when not switching between modes.
Picture bounces or a wavy pattern is present in the picture
- Move electrical devices that may be causing electrical interference away from the monitor.
- See inside cover of User's Manual for FCC information.

Edges of the display image are not square

- Use the OSM Geometry Controls to straighten the edges
- If possible, position the front of the monitor facing east.

Display image is not centered, too small, or too large

- Use the OSM Size and Position Controls to adjust the image.


## Thin lines appear on your screen

- Thin lines are normal for an aperture grille CRT and are not a malfunction. These are shadows from the damper wires used to stabilize the aperture grille and are most noticeable when the screen's background is light (usually white).


## Black vertical lines are visible on the screen

- Thin vertical black lines on one or both sides of the screen. This minor condition is caused by grille element overlap which can occur during shipping.
- Position an open white window over the affected area of the screen and maximize the brightness and contrast controls. This will cause localized heating of the overlap which will clear in a few minutes. Be sure to readjust the brightness and contrast controls back to the normal viewing level after this procedure.


## References

- BBS
(978) 742-8706

NEC-Mitsubishi Electronics Display of America Remote Bulletin Board System is an electronic service accessible with your system and a modem. Communication parameters are: 300/1200/2400/9600/14.4k/28.8k/33.6k bps, no parity, 8 -data bits, 1 stop bit

- Customer Service/ Technical Support
(800) 632-4662 Fax
(978) 742-7049
- Electronic Channels: Internet e-mail: Internet ftp site: World Wide Web: Product Registration: European Operations:
tech-suppor@@necmitsubishi.com
ftp.necmitsubishi.com
http://www.necmitsubishi.com
http://www.necmitsubishi.com/productregistration http://www.nec-monitors.com
Windows $95 / 98 / \mathrm{Me} / 2000 / \mathrm{XP}$ INF File: http://support.necmitsubishi.com/soffware. htm

| - FastFacts ${ }^{\text {TM }}$ Information | (800) 366-0476 <br> INFORMATION | DESCRIPTION |
| :--- | :--- | ---: |$\quad$ DOCUMENT \#

## Limited Warranty

NEC-Mitsubishi Electronics Display of America, Inc. (hereinafter "NMD-A") warrants this Product to be free from defects in material and workmanship and, subject to the conditions set forth below, agrees to repair or replace (at NMD-A's sole option) any part of the enclosed unit which proves defective for a period of three (3) years from the date of first consumer purchase. Spare parts are warranted for ninety (90) days. Replacement parts or unit may be new or refurbished and will meet specifications of the original parts or unit.
This warranty gives you specific legal rights and you may also have other rights, which vary from state to state. This warranty is limited to the original purchaser of the Product and is not transferable. This warranty covers only NMD-A-supplied components. Service required as a result of third party components is not covered under this warranty. In order to be covered under this warranty, the Product must have been purchased in the U.S.A. or Canada by the original purchaser. This warranty only covers Product distribution in the U.S.A. or Canada by NMD-A No warranty service is provided outside of the U.S.A. or Canada. Proof of Purchase will be required by NMD-A to substantiate date of purchase. Such proof of purchase must be an original bill of sale or receipt containing name and address of seller, purchaser, and the serial number of the product.
It shall be your obligation and expense to have the Product shipped, freight prepaid, or delivered to the authorized reseller from whom it was purchased or other facility authorized by NMD-A to render the services provided hereunder in either the original package or a similar package affording an equal degree of protection. All Products returned to NMD-A for service MUST have prior approval, which may be obtained by calling 1-800-632-4662. The Product shall not have been previously altered, repaired, or serviced by anyone other than a service facility authorized by NMD-A to render such service, the serial number of the product shall not have been altered or removed. In order to be covered by this warranty the Product shall not have been subjected to displaying of fixed images for long periods of time resulting in image persistence (afterimage effects), accident, misuse or abuse or operated contrary to the instructions contained in the User's Manual. Any such conditions will void this warranty
NMD-A SHALL NOT BE LIABLE FOR DIRECT, INDIRECT, INCIDENTAL, CONSEQUENTIAL, OR OTHER TYPES OF DAMAGES RESULTING FROM THE USE OF ANY NMD-A PRODUCT OTHER THAN THE LIABILITY STATED ABOVE. THESE WARRANTIES ARE IN LIEU OF ALL OTHER WARRANTIES EXPRESS OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE MPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE SOME STATES DO NOT ALLOW THE EXCLUSION OF IMPLIED WARRANTIES OR THE LIMITATION OR EXCLUSION OF LIABILITY FOR INCIDENTAL OR CONSEQUENTIAL DAMAGES SO THE ABOVE EXCLUSIONS OR LIMITATIONS MAY NOT APPLY TO YOU,
This Product is warranted in accordance with the terms of this limited warranty. Consumers are cautioned that Product performance is affected by system configuration, software, the application, customer data, and operator control of the system, among other factors. While NMD-A Products are considered to be compatible with many systems, specific functional implementation by the customers of the Product may vary. Therefore, suitability of a Product for a specific purpose or application must be determined by consumer and is not warranted by NMD-A.
For the name of your nearest authorized NEC-Mitsubishi Electronics Display of America service facility, contact NEC-Mitsubishi Electronics Display of America at 1-800-632-4662.

## TCO'95

## Diamond Plus 74 ${ }^{\text {SB }}$ Black Model

Congratulations! You have just purchased a TCO'95 approved and labeled product! Your choice has provided you with a product developed for professional use. Your purchase has also contributed to reducing the burden on the environment and also, to the further development of environmentally adapted electronics products.

## Why do we have environmentally labelled computers?

In many countries, environmental labelling has become an established method for encouraging the adaptation of goods and services to the environment. The main problem, as far as computers and other electronics equipment are concerned, is that environmentally harmful substances are used both in the products and during the manufacturing. Since it has not been possible for the majority of electronics equipment to be recycled in a satisfactory way, most of these potentially damaging substances sooner or later enter Nature.
There are also other characteristics of a computer, such as energy consumption levels, that are important from the viewpoints of both the work (Internal) and natural (external) environments. Since all methods of conventional electricity generation have a negative effect on the environment (acidic and climate-influencing emissions, radioactive waste, etc.), it is vital to conserve energy. Electronics equipment in offices consume an enormous amount of energy since they are offen leff running continuously.

## What does labelling involve?

This product meets the requirements for the TCO' 95 scheme which provides for international and environmental labelling of personal computers. The labelling scheme was developed as a joint effort by the TCO (The Swedish Confederation of Professional Employees), Naturskyddsforeningen (The Swedish Society for Nature Conservation) and NUTEK (The National Board for Industrial and Technical Development in Sweden).
The requirements cover a wide range of issues: environment, ergonomics, usability, emission of electrical and magnetic fields, energy consumption and electrical and fire safery.
The environmental demands concern restrictions on the presence and use of heavy metals, brominated and chlorinated flame retardants, CFCs (freons) and chlorinated solvents, among other things. The product must be prepared for recycling and the manufacturer is obliged to have an environmental plan which must be adhered to in each country where the company implements its operational policy. The energy requirements include a demand that the computer and/or display, after a certain period of inactivity, shall reduce its power consumption to a lower level in one or more stages. The length of time to reactivate the computer shall be reasonable for the user. Labelled products must meet strict environmental demands, for example, in respect of the reduction of electric and magnetic fields, physical and visual ergonomics and good usability.
TCO'95 is a co-operative project between TCO (The Swedish Confederation of Professional Employees), Naturskyddsforeningen (The Swedish Society for Nature Conservation) and NUTEK (The National Board for Industrial and Technical Development in Sweden).

## Environmental Requirements

## Brominated flame retardants

Brominated flame retardants are present in printed circuit boards, cables, wires, casings and housings. In turn, they delay the spread offire. Up to thirty percent of the plastic in a computer casing can consist of flame retardant substances. These are related to another group of environmental

## TCO'95 -continued

toxins, PCBs, which are suspected to give rise to similar harm, including reproductive damage in fisheating birds and mammals, due to the bio-accumulative* processes. Flame retardants have been found in human blood and researchers fear that disturbances in foetus development may occur.
TCO'95 demand requires that plastic components weighing more than 25 grams must not contain organically bound chlorine and bromine.

## Lead**

Lead can be found in picture tubes, display screens, solders and capacitors. Lead damages the nervous system and in higher doses, causes lead poisoning.
TCO'95 requirement permits the inclusion of lead since no replacement has yet been developed.

## Cadmium**

Cadmium is present in rechargeable batteries and in the colourgenerating layers of certain computer displays. Cadmium damages the nervous system and is toxic in high doses.
TCO'95 requirement states that batteries may not contain more than 25 ppm (parts per million) of cadmium. The colourgenerating layers of display screens must not contain any cadmium.

## Mercury**

Mercury is sometimes found in batteries, relays and switches, Mercury damages the nervous system and is toxic in high doses.
TCO'95 requirement states that batteries may not contain more than 25 ppm (parts per million) of mercury. It also demands that no mercury is present in any of the electrical or electronics components concerned with the display unit. Mercury is, for the time being, permitted in the back light system of flat panel monitors as there today is no commercially available alternative. TCO aims on removing this exception when a mercury free alternative is available.

## CFCs (freons)

CFCs (freons) are sometimes used for washing printed circuit boards and in the manufacturing of expanded foam for packaging. CFCs break down ozone and thereby damage the ozone layer in the stratosphere, causing increased reception on Earth of ultraviolet lightwith consequent increased risks of skin cancer (malignant melanoma).
The relevantTCO' 95 requirement; Neither CFCs nor HCFCs may be used during the manufacturing of the product or its packaging.
*Bio-accumulative is defined as substances which accumulate within living organisms.
**Lead, Cadmium and Mercury are heavy metals which are Bio-accumulative.
To obtain complete information on the environmental criteria document, order from:
TCO Development Unit
SE-114 94 Stockholm
SWEDEN
FAX Number: +46 87829207
E-mail (Internet): development@tco.se
You may also obtain current information on TCO'95 approved and labelled products by visiting their website at: http://www.tco-info.com/

## Declaration of the Manufacturer

We hereby certify that the color monitor Diamond Plus $74^{\text {SB }}$ is in compliance with
Council Directive 73/23/EEC:

- EN 60950

Council Directive 89/336/EEC:
EN 55022

- EN 61000-3-2
- EN 61000-3-3
- EN 55024
and marked with


NEC-Mitsubishi Electric Visual Systems Corporation 686-1, Nishioi Oi-Machi Ashigarakami-gun
Kanagawa 258-8533, Japan

## Mitsubish Dicmond Plus74ss

## PROPRIETARY NOTICE AND LIABILITY DISCLAIMER

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The NEC-Mitsubishi Electronics Display of America product(s) discussed in this document are warranted in accordance with the terms of the Limited Warranty Statement accompanying each product. However, actual performance of each such product is dependent upon factors such as system configuration, customer data and operator control. Since mplementation by customers of each product may vary, the suitability of specific product configurations and application must be determined by the customer and is not warranted by NEC-Mitsubishi Electronics Display of America.
o allow for design and specification improvements, the information in this document is subject to change at any time without notice. Reproduction of this document or portions thereof without prior approval of NEC-Mitsubishi Electronic Display of America is prohibited.

## DECLARATION OF CONFORMITY

This device complies with Part 15 of FCC Rules. Operation is subject to the following two conditions. (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

| U.S. Responsible Party: | NEC-Mitsubishi Electronics Display of America, Inc. <br> Address: <br>  <br> Tel. No.: |
| :--- | :--- |
| Itasca, IIlinois 60143 |  |
|  | (630) 467-3000 |


| Type of Product: | Computer Monitor |
| :--- | :--- |
| Equipment Classification: | Class B Peripheral |
| Models: | N1702 |

We hereby declare that the equipment specified above conforms to the technical standards as specified in the FCC Rules.

[^0]
# $\therefore$ MITSUBISHI 

USER'S MANUAL

www.nec-mitsubishi.com

## Declaration of the Manufacturer

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Council Directive 73/23/EEC:

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NEC-Mitsubishi Electric Visual Systems Corporation 686-1, Nishioi Oi-Machi Ashigarakami-gun Kanagawa 258-8533, Japan

## EnergyStar Product

As an EnergyStar Partner, NEC-Mitsubishi Electronics Display of America, Inc. has determined that this product meets the EnergyStar guidelines for energy efficiency. The EnergyStar emblem does not represent EPA endorsement of any product or service.

## WARNING



TO PREVENT FIRE OR SHOCK HAZARDS, DO NOT EXPOSE THIS UNITTO RAIN OR MOISTURE. ALSO, DO NOT USE THIS UNIT'S POLARIZED PLUG WITH AN EXTENSION CORD RECEPTACLE OR OTHER OUTLETS UNLESS THE PRONGS CAN BE FULLY INSERTED.
EFRAIN FROM OPENING THE CABINETAS THERE ARE HIGH VOLTAGE COMPONENTS INSIDE. REFER SERVICING TO QUALIFIED SERVICE PERSONNEL.


CAUTION: TO REDUCE THE RISK OF ELECTRIC SHOCK, DO NOT REMOVE COVER (ORBACK). NO USER SERVICEABLE PARTS INSIDE. REFER SERVICING TO QUALIFIED SERVICE PERSONNEL.

This symbol warns user that uninsulated voltage within the unit may have sufficient magnitude to cause electric shock. Therefore, it is dangerous to make any kind of contact with any part inside this unit.

This symbol alerts the user that important literature concerning the operation and maintenance of this unit has been included. Therefore, it should be read carefully in order to avoid any problems.

## Canadian Department of Communications Compliance Statement

DOC: This Class B digital apparatus meets all requirements of the Canadian Interference-Causing Equipment Regulations.
C-UL: Bears the C-UL Mark and is in compliance with Canadian Safety Regulations according to C.S.A. C22.2 No. 950.

## FCC Information

1. Use the attached specified cables with the Diamond Plus $744^{\text {SB }}$ colour monitor so as not to interfere with radio and television reception.
(1) Please use the supplied power cord or equivalent to ensure FCC compliance.
(2) Shielded captive type signal cable.

Use of other cables and adapters may cause intereference with radio and television reception.
2. This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy, and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult your dealer or an experienced radio/TV technician for help.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.
If necessary, the user should contact the dealer or an experienced radio/television technician for additional suggestions. The user may find the following booklet, prepared by the Federal Communications Commission, helpful: "How to Identify and Resolve Radio-TV Interference Problems." This booklet is available from the U.S. Government Printing Office, Washington, D.C., 20402, Stock No. 004-000-00345-4.

## Contents

Your new Diamond Plus $74^{\text {SB }}$ monitor box* should contain the following:

- Diamond Plus $74^{\text {SB }}$ Monitor with tilt/swivel base
- Power Cord
- Captive Signal Cable
- User's Manual
- CD ROM with Setup Software, complete User's Manual and other helpful files. To see the User's Manual, Acrobat Reader 4.0 must be installed on your PC.

* Remember to save your original box and packing material to transport or ship the monitor.


## Quick Start

To attach the Diamond Plus $74{ }^{\text {SB }}$ monitor to your system, follow these instructions:

1. Turn off the power to your computer.
2. If necessary, install the display card into your system. For more information, refer to the display card manual.
3. For the PC: Connect the 15-pin mini D-SUB of the captive signal cable to the connector of the display card in your system (Figure A.1). Tighten all screws.
For the Mac: Connect the Diamond Plus $74^{\text {SB }}$ Macintosh cable adapter (not included) to the monitor connector on the Macintosh (Figure B.1). Attach the 15-pin mini D-SUB end of the captive signal cable to the Diamond Plus $74{ }^{\text {SB }}$ Macintosh cable adapter on the computer (Figure B.1). Tighten all screws.
4. Connect one end of the power cord to the Diamond Plus $74^{\mathrm{SB}}$ monitor and the other end to the power outlet (Figure C.1).
5. Turn on the monitor (Figure D.1) and the computer

NOTE: If you have any problems, please refer to the Troubleshooting section of this User's Manual.

Figure A. 1


Figure B. 1


## Quick Start -continued



Figure C. 1


Figure D. 1

## Controls

OSM (On-Screen Manager) control buttons on the front of the monitor function as follows:

|  | Main Menu | Sub-Menu |
| :---: | :---: | :---: |
| EXIT | Exits the OSM menu. | Exits to the OSM controls main menu. |
| CONTROL | Moves the highlighted area left/right to select one of the sub-menus. | Moves the highlighted area left/right to select one of the controls. |
| $\begin{aligned} & \text { CONTROL } \\ & -/+ \end{aligned}$ | Has no function. | Moves the bar in the - or + direction to decrease or increase the adjustment. |
| SELECT/ SBMODE | Without OSD, switches SuperBright Mode ON/OFF With OSD, enters sub menu | Has no function. |
| RESET | Resets all the controls within the highlighted menu to the factory setting. | Resets the highlighted control to the factory setting. |
|  | When RESET is pressed in the main and sub-menu, a warning window will appear allowing you to cancel the reset function. |  |
|  | In SB MODE (SuperBright M the OSM is not displayed. | FF is functional when |

## 演 (9) Brightness/Contrast Controls

Brightness: Adjusts the overall image and background screen brightness.
Contrast: Adjusts the image brightness in relation to the background.
Degauss: Eliminates the buildup of stray magnetic fields which alter the correct scan of the electron beams and affect the purity of the screen colours, focus and convergence. When activated, your screen image will jump and waver a bit as the screen is demagnetized.
Caution: Please allow a minimum of $\mathbf{2 0}$ minutes to elapse between uses of the Degauss Control.

## 田 Size and Position Controls

Left/Right: Moves the image horizontally (left or right).
Down/Up: Moves the image vertically (up or down).
Narrow/Wide: Decreases or increases the horizontal size of the image.
Short/Tall: Decreases or increases the vertical size of the image.

## Controls - continued

## (RGB) Color Control System

Colour presets selects the desired colour setting. The bar is replaced by the colour setting choice. Each colour setting is adjusted at the factory to the stated Kelvin. If a setting is adjusted, the name of the setting will change from Kelvin to Custom except sRGB mode.
Red, Green, Blue: Color Control System decreases or increases the monitor's red, green or blue colour guns depending upon which is selected. The change in colour will appear on screen and the direction (decrease or increase) will be shown by the bars.
sRGB mode: sRGB mode provides the suitable colour managed picture image. You can not change Red, Green and Blue colours, brightness and contrast individually.
Colour Temperature Adjustment: Adjusts the colour temperature of the screen image.
$\square$ Geometry Controls

## Geometry Controls Menu

The Geometry controls allow you to adjust the curvature or angle of the sides of your display.
Sides In/Out (pincushion): Decreases or increases the curvature of the sides either inward or outward.
Sides Left/Right (pincushion balance): Decreases or increases the curvature of the sides either to the left or right.
Sides Tilt (parallelogram): Decreases or increases the tilt of the sides either to the left or right.
Sides Align (trapezoidal): Decreases or increases the bottom of the screen to be the same as the top.
Rotate (raster rotation): Rotates the entire display clockwise or counterclockwise.

Tools 1

Moiré Canceler: Moiré is a wavy pattern which can sometimes appear on the screen. The pattern is repetitive and superimposed as rippled images. When running certain applications, the wavy pattern is more evident than in others. To reduce moiré, adjust the level by using -/+ CONTROL buttons.

Tools 2

Language: OSM controls menus are available in 6 languages.
OSM Position: You can choose where you would like the OSM controls menu to appear on your screen. Selecting OSM Position allows you to manually adjust the OSM controls menu position from among Center, Top left, Top right, Bottom left and Bottom right.
OSM Turn Off: The OSM controls menu will stay on as long as it is in use. In the OSM Turn Off sub-menu, you can select how long the monitor waits after the last touch of a button for the OSM controls menu to disappear. The preset choices are 5 thru 120 seconds.

## Controls - continued

OSM Lock Out: This control completely locks out access to all OSM controls functions except Brightness and Contrast. When attempting to activate OSM controls while in the lock out mode, a screen will appear indicating that OSM controls are locked out. To activate the OSM Lock Out function, press SELECT and hold + down simultaneously. To deactivate the OSM Lock Out, press SELECT and hold + down simultaneously.

IPM System Off Mode: Enable: The IPM System works normally and all stages of energy savings are utilized.

Disable: The Off Mode of the IPM System is not used.
NOTE: For standard systems and graphics boards, keep the factory setting at ENABLE.
Factory Preset: Selecting Factory Preset allows you a reset most OSM control settings back to the factory settings. A warning statement will appear to confirm that you do want to reset ALL settings. Individual settings can be reset by highlighting the control to be reset and pressing the RESET button.

## 1 Information

Display Mode: Indicates the current mode and frequency setting of the monitor.
Monitor Info: Indicates the model and serial numbers of your monitor.
Refresh Notifier: A message will advise you if the refresh rate of the signal being applied to the monitor by the computer is too low. For further information, please refer to your display card or system manual.

## Recommended Use

## Safety Precautions and Maintenance

## FOR OPTIMUM PERFORMANCE, PLEASE NOTE THE FOLLOWING WHEN SETTING UP AND USING THE DIAMOND PLUS $74{ }^{\text {SB }}$ COLOUR MONITOR:

- DO NOT OPEN THE MONITOR. There are no user serviceable parts inside and opening or removing covers may expose you to dangerous shock hazards or other risks. Refer all servicing to qualified service personnel.
- Do not spill any liquids into the cabinet or use your monitor near water.
- Do not insert objects of any kind into the cabinet slots, as they may touch dangerous voltage points, which can be harmful or fatal or may cause electric shock, fire or equipment failure.
- Do not place any heavy objects on the power cord. Damage to the cord may cause shock or fire.
- Do not place this product on a sloping or unstable cart, stand or table, as the monitor may fall, causing serious damage to the monitor.
- Keep the monitor away from high capacity transformers, electric motors and other devices such as external speakers or fans, which may create strong magnetic fields.
- If possible, position the monitor so that it is facing the east to minimize the effects of the earth's magnetic field.
- Changing the direction of the monitor while it is powered on may cause image discolouration. To correct this, turn the monitor off for 20 minutes before powering it back on.
- When operating the Diamond Plus $74^{\mathrm{SB}}$ with its AC 220-240 V worldwide power supply, use a power supply cord that matches the power supply voltage of the AC power outlet being used. The power supply cord you use must have been approved by and comply with the safety standards of your country. (Type H05VV-F should be used except in UK)
- In UK, use a BS-approved power cord with molded plug having a black (5A) fuse installed for use with this monitor. If a power cord is not supplied with this monitor, please contact your supplier.


## Cleaning Your Monitor

A special coating is provided on the glass (CRT) surface of this monitor to reduce a reflection and static electricity on the glass surface. Due to the delicate coating on the glass surface, use a lint-free, non-abrasive cloth (cotton or equivalent) and a non-alcohol, neutral, non-abrasive cleaning solution to minimize dust. If the screen requires more than a light cleaning, apply a soft neutral detergent and water directly to a soft cloth and use it upon wringing water, to clean the glass surface. Clean your monitor regularly.
CAUTION: The following agents will cause damage to the CRT when cleaning the glass surface: Benzene, thinner, acid/alkaline detergent, alcohol detergent, detergent with abrasive powder, detergent with anti-static agent, detergent for cleaning.
Immediately unplug your monitor from the wall outlet and refer servicing to qualified service personnel under the following conditions:

- When the power supply cord or plug is damaged.
- If liquid has been spilled, or objects have fallen into the monitor.
- If the monitor has been exposed to rain or water.
- If the monitor has been dropped or the cabinet damaged.
- If the monitor does not operate normally by following operating instructions.
- Allow adequate ventilation around the monitor so that heat can properly dissipate. Do not block ventilated openings or place the monitor near a radiator or other heat sources. Do not put anything on top of monitor.

- The power cable connector is the primary means of detaching the system from the power supply. The monitor should be installed close to a power outlet which is easily accessible.
- Handle with care when transporting. Save packaging for transporting.


## Recommended Use - continued

## 0

## CORRECT PLACEMENTAND ADJUSTMENT OF THE MONITOR CAN REDUCE EYE, SHOULDER AND NECK FATIGUE. CHECK THE FOLLOWING WHEN YOU POSITION THE MONITOR:



- Adjust the monitor height so that the top of the screen is at or slightly below eye level. Your eyes should look slightly downward when viewing the middle of the screen.
- Position your monitor no closer than 40 cm and no further away than 60 cm from your eyes. The optimal distance is 50 cm .
- Rest your eyes periodically by focusing on an object at least 6 meter away. Blink often.
- Position the monitor at a $90^{\circ}$ angle to windows and other light sources to minimize glare and reflections. Adjust the monitor tilt so that ceiling lights do not reflect on your screen.
- If reflected light makes it hard for you to see your screen, use an anti-glare filter.

- Clean your monitor regularly. Use a lint-free, non-abrasive cloth and a non-alcohol, neutral, non-abrasive cleaning solution or glass cleaner to minimize dust.
- Adjust the monitor's brightness and contrast controls to enhance readability.
- Use a document holder placed close to the screen.
- Position whatever you are looking at most of the time (the screen or reference material) directly in front of you to minimize turning your head while you are typing.
- Get regular eye checkups.


## Ergonomics

To realize the maximum ergonomics benefits, we recommend the following:

- Adjust the Brightness until the background raster disappears
- Do not position the Contrast control to its maximum setting
- Use the preset Size and Position controls with standard signals
- Use the preset Colour Setting and Sides Left/Right controls
- Use non-interlaced signals with a vertical refresh rate between $75-120 \mathrm{~Hz}$
- Do not use primary colour blue on a dark background, as it is difficult to see and may produce eye fatigue due to insufficient contrast


## Specifications

| Monitor Specifications | Diamond Plus 74 ${ }^{\text {SB }}$ Monitor | Notes |
| :---: | :---: | :---: |
| Picture Tube Diagonal: <br>  Viewable Image Size: | $43 \mathrm{~cm} / 17$ inch 406 mm/16 inch | $90^{\circ}$ deflection, 0.25 mm grille pitch, medium short persistence phosphor, aperture grille CRT, multi-layered, antistatic screen coating, dark-tint screen and OptiClear screen. |
| $\begin{array}{lr}\text { Input Signal } & \text { Video: } \\ & \text { Sync: }\end{array}$ | ANALOG $0.7 \mathrm{Vp}-\mathrm{p} / 75$ Ohms Separate sync. TTL Level Horizontal sync. Positive/Neg Vertical sync. Positive/Negat Composite sync. (Positive/N | L Level) |
| Display Colours Analog input: | Unlimited number of Colours | Depends on display card used. |
| Synchronization Horizontal: <br> Range Vertical: | 30 kHz to 70 kHz <br> 50 Hz to 120 Hz | Automatically <br> Automatically |
| Resolutions Supported Resolution based on horizontal and vertical frequencies only | $640 \times 480$ @ 60 to 120 Hz $800 \times 600$ @ 50 to 110 Hz $832 \times 624$ @ 50 to 106 Hz $1024 \times 768$ @ 50 to 87 Hz . $1152 \times 864$ @ 50 to 77 Hz $1280 \times 1024 @ 50$ to 66 Hz | Some systems may not support all modes listed. <br> .NEC-Mitsubishi Electronics Display cites recommended resolution at 85 Hz for optimal display performance |
| Active Display Area Horizontal: <br> (Factory Setting) Vertical: | 315 mm/12.4 inches 236 mm/9.3 inches | Dependent upon signal timing used, and does not include border area. |
| Active Display Area (Full Scan) | 325 mm/12.8 inches 244 mm/9.6 inches | Dependent upon signal timing used, and does not include border area. |
| Power Supply | AC 100-240 V, 50-60 Hz |  |
| Current Rating | 1.5A @ 100-240 V |  |
| Dimensions | $\begin{aligned} & 397 \mathrm{~mm}(\mathrm{~W}) \times 392 \mathrm{~mm}(\mathrm{H}) \times 415.5 \mathrm{~mm}(\mathrm{D}) \\ & 15.6 \text { inches }(\mathrm{W}) \times 15.4 \text { inches }(\mathrm{H}) \times 16.4 \text { inches (D) } \end{aligned}$ |  |
| Weight | $\begin{aligned} & 16.8 \mathrm{~kg} \\ & 37.0 \mathrm{lbs} \end{aligned}$ |  |
| Environmental Considerations <br> Operating Temperature: Humidity: <br> Feet: <br> Storage Temperature: <br> Humidity: <br> Feet: | $\begin{aligned} & +5{ }^{\circ} \mathrm{C} \text { to }+35{ }^{\circ} \mathrm{C} \\ & 10 \% \text { to } 90 \% \\ & 0 \text { to } 3,000 \\ & -20{ }^{\circ} \mathrm{C} \text { to }+60^{\circ} \mathrm{C} \\ & 10 \% \text { to } 90 \% \\ & 0 \text { to } 15,000 \text { Feet } \end{aligned}$ |  |

NOTE: Technical specifications are subject to change without notice.

## Features

SuperBright Diamondtron CRT: This patented flat aperture grille CRT delivers an exceptional viewing experience with unprecedented brightness and contrast and a virtually flat image that reduces distortion and glare so that what you see on-screen is what you get on your printed output. The state-of-the-art Mitsubishi PX-DBF electron gun and tight 0.25 mm grille pitch delivers precise focus for crisp, clear text and images.
SuperBright Mode: With the simple touch of a button, the brightness level of the Diamondtron CRT doubles. This function enhances the crispness of images for clarity-conscious applications such as graphics, animation and video

OptiClear Screen Surface: Further reduces reflection and glare and increases contrast without sacrificing focus level, clarity or brightness.
Dual Dynamic Beam Focus: Provides precise, continuous focus adjustments of the electron beams and optimum image quality, even to the far edges of the screen.

Color Control System with sRGB: Allows you to change between five colour settings on your display to match your personal preference. The SRGB-enabled colour matching setting found within Color Control helps achieve a consistent colour environment with other sRGB-enabled hardware and software applications.
On Screen Manager (OSM) Controls: Allows you to quickly and easily adjust all elements of your screen image via simple to use on-screen menus.

ErgoDesign Features: Enhances human ergonomics to improve the working environment, protect the health of the user and save money. Examples include OSM controls for quick and easy image adjustments, tilt/swivel base for preferred angle of vision, space-conscious cabinet design and compliance with MPRII guidelines for lower emissions.
Plug and Play: The Microsoft solution with the Windows 95/98/Me/2000/XP operating system facilitates setup and installation by allowing the monitor to send its capabilities (such as screen size and resolutions supported) directly to your computer, automatically optimizing display performance.

Intelligent Power Manager (IPM) System: Provides innovative power-saving methods that allow the monitor to shift to a lower power consumption level when on but not in use, saving two-thirds of your monitor energy costs, reducing emissions and lowering the air conditioning costs of the workplace.

Reduced Magnetic Field Technology: Reduces magnetic and alternating electric field emissions and static electricity, addressing ergonomic concerns regarding potential risks from extended computer monitor use.
Multiple Frequency Technology: Automatically adjusts monitor to the display card's scanning frequency, thus displaying the resolution required.
FullScan Capability: Allows you to use the entire screen area in most resolutions, significantly expanding image size.

## Troubleshooting

## No picture

- Display card should be completely seated in its slot.
- Power Button and computer power switch should be in the ON position.
- Signal cable should be completely connected to display card/computer.
- Check connector for bent or pushed-in pins.


## Image is scrolling or unstable

- Signal cable should be completely attached to the computer.
- Check pin assignments and signal timings of the monitor and your display card with respect to recommended timings and pin assignments.
- If the Macintosh cable adapter is used, check for proper connection or make sure the display card is Macintosh compatible and that the card is properly seated in the computer.

LED on monitor is not lit (no green, orange colour can be seen)

- Power Switch should be in the ON position and power cord should be connected.


## Picture is fuzzy or colour looks blotchy

- Adjust Brightness and Contrast Controls or adjust the Moiré Canceler control.
- Access the Degauss Control through OSM controls. Activate the Degauss Control. CAUTION: A minimum interval of 20 minutes should elapse before the Deguass Control is used a second time when not switching between modes.


## Picture bounces or a wavy pattern is present in the picture

- Move electrical devices that may be causing electrical interference away from the monitor.
- See inside cover of User's Manual for FCC information.

Edges of the display image are not square

- Use the OSM Geometry Controls to straighten the edges.
- If possible, position the front of the monitor facing east.

Display image is not centered, too small, or too large

- Use the OSM Size and Position Controls to adjust the image.

Thin lines appear on your screen

- Thin lines are normal for an aperture grille CRT and are not a malfunction.

These are shadows from the damper wires used to stabilize the aperture grille and are most noticeable when the screen's background is light (usually white).

## Black vertical lines are visible on the screen

- Thin vertical black lines on one or both sides of the screen. This minor condition is caused by grille element overlap which can occur during shipping.
- Position an open white window over the affected area of the screen and maximize the brightness and contrast controls. This will cause localized heating of the overlap which will clear in a few minutes. Be sure to readjust the brightness and contrast controls back to the normal viewing level after this procedure.


## TCO'99

## Diamond Plus 74 ${ }^{\text {SB }}$

Congratulations! You have just purchased a TCO'99 approved and labeled product! Your choice has provided you with a product developed for professional use. Your purchase has also contributed to reducing the burden on the environment and also to the further development of environmentally adapted electronics products.

## Why do we have environmentally labelled computers?

In many countries, environmental labelling has become an established method for encouraging the adaptation of goods and services to the environment. The main problem, as far as computers and other electronics equipment are concerned, is that environmentally harmful substances are used both in the products and during the manufacturing. Since it has not been possible for the majority of electronics equipment to be recycled in a satisfactory way, most of these potentially damaging substances sooner or later enter Nature.

There are also other characteristics of a computer, such as energy consumption levels, that are important from the viewpoints of both the work (Internal) and natural (external) environments. Since all methods of conventional electricity generation have a negative effect on the environment (acidic and climate-influencing emissions, radioactive waste, etc.), it is vital to conserve energy. Electronics equipment in offices consume an enormous amount of energy since they are often left running continuously.

## What does labelling involve?

This product meets the requirements for the TCO'99 scheme which provides for international and environmental labelling of personal computers. The labelling scheme was developed as a joint effort by the TCO (The Swedish Confederation of Professional Employees), Svenska Naturskyddsforeningen (The Swedish Society for Nature Conservation) and Statens Energimyndighet (The Swedish National Energy Administration).

The requirements cover a wide range of issues: environment, ergonomics, usability, emission of electrical and magnetic fields, energy consumption and electrical and fire safety.

The environmental demands concern restrictions on the presence and use of heavy metals, brominated and chlorinated flame retardants, CFCs (freons) and chlorinated solvents, among other things. The product must be prepared for recycling and the manufacturer is obliged to have an environmental plan which must be adhered to in each country where the company implements its operational policy. The energy requirements include a demand that the computer and/or display, after a certain period of inactivity, shall reduce its power consumption to a lower level in one or more stages. The length of time to reactivate the computer shall be reasonable for the user.

Labelled products must meet strict environmental demands, for example, in respect of the reduction of electric and magnetic fields, physical and visual ergonomics and good usability.

## Environmental Requirements

## Flame retardants

Flame retardants are present in printed circuit boards, cables, wires, casings and housings. In turn, they delay the spread of fire. Up to thirty percent of the plastic in a computer casing can consist of flame retardant substances. Most flame retardants contain bromine or chloride and these are related to another group of environmental toxins, PCBs, which are suspected to give rise to severe health effects, including reproductive damage in fisheating birds and mammals, due to the bioaccumulative* processes. Flame retardants have been found in human blood and researchers fear that disturbances in foetus development may occur.

## TCO'99 - continued

TCO'99 demand requires that plastic components weighing more than 25 grams must not contain flame retardants with organically bound chlorine and bromine. Flame retardants are allowed in the printed circuit boards since no substitutes are available.

## Lead**

Lead can be found in picture tubes, display screens, solders and capacitors. Lead damages the nervous system and in higher doses, causes lead poisoning.

TCO'99 requirement permits the inclusion of lead since no replacement has yet been developed.

## Cadmium**

Cadmium is present in rechargeable batteries and in the colourgenerating layers of certain computer displays. Cadmium damages the nervous system and is toxic in high doses.

TCO'99 requirement states that batteries, the colourgenerating layers of display screens and the electrical or electronics components must not contain any cadmium.

## Mercury**

Mercury is sometimes found in batteries, relays and switches, Mercury damages the nervous system and is toxic in high doses.

TCO'99 requirement states that batteries may not contain any Mercury. It also demands that no mercury is present in any of the electrical or electronics components associated with the display unit.

## CFCs (freons)

CFCs (freons) are sometimes used for washing printed circuit boards. CFCs break down ozone and thereby damage the ozone layer in the stratosphere, causing increased reception on Earth of ultraviolet light with consequent increased risks of skin cancer (malignant melanoma).

The relevant TCO'99 requirement; Neither CFCs nor HCFCs may be used during the manufacturing and assembly of the product or its packaging.

* Bio-accumulative is defined as substances which accumulate within living organisms.
** Lead, Cadmium and Mercury are heavy metals which are Bio-accumulative.

To obtain complete information on the environmental criteria document, order from:
TCO Development Unit
SE-114 94 Stockholm SWEDEN
FAX Number: +46 87829207
E-mail (Internet): development@tco.se
You may also obtain current information on TCO'99 approved and labelled products by visiting their website at: http://www.tco-info.com/

## Serial Number Information

Refer to the serial number information shown below.


## DISASSEMBLY

- Before you disassemble the set, turn off power and pull out the power plug.
- Use the appropriate screwdrivers that first the screws. If you use screwdriver that does not fit, you may break the screws.
- Assembly is the opposite process of Disassembly.
- Carefully discharge the CRT anode potential by grounding to coating dag before removing Anode Cap.


## Revolving Stand ASSY

1. Turn the monitor CRT face down on a clean static free surface to prevent scratching CRT face.
2. Remove with pulling up a Hooks and lifting a Revolving stand Assy to the upside.


## Cabinet Back

1. Remove the two screws (\#2CBRITS*4*12*15BF).


## CRT BOARD

1. Five terminals are removed, and six solder is removed.

2. Disconnect the connectors "S201", "S202", "S203" and "GND".
3. Unsolder the wires "White wire", "Red wire" and "Gray wire".


## MAIN BOARD

1. Disconnect the connectors "S102", "S701" and "CRT PWB (GND)".
2. Remove the screw (PL-CPTS*3*8*15BF).

3. Remove the two screws (PL-CPTS*3*8*15BF) and screw (PL-CPIMS*4*10*15BF).

4. Cut the three Ties and disconnect the connectors "TPC" and "S301".
5. Remove the screw (PL-CPTS*3* $8^{*} 15 B F$ ).
6. Remove the Anode cap from CRT.

NOTE: Carefully discharge the CRT anode by shorting it to ground before removing anode cap.

7. Remove the two screws (\#2CBRITS*4*12*15BF) and remove the Chassis Base from Cabinet Front ASSY.

screw (\#2CBRITS*4*12*15BF)
8. Remove the eight screws (PL-CPTS*3*8*15BF) and remove the Main Board from Chassis Base.

screw (PL-CPTS*3*8*15BF)

## ADJUSTMENT PROCEDURES

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## 1. Adjustment \& Inspection Tools

(A) Color Analyzer
(B) Signal Generator CHROMA 2135 or compatible
(C) Multi Meter
(D) Hi-Voltage Probe
(E) Convergence Meter
(F) Degaussing Probe
(G) Power Meter
(H) Automatic Alignment system
2. Timing Table (Factory Mode -20 Modes)

| MODE | RESOLUTION | H-SYNC EREQ. | V-SYNC FREQ | H. POLARITY | V. POLARITY |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | VGA350 | 31.5 KHz | 70 Hz | + | - |
| 2 | VGA400 | 31.5 KHz | 70 Hz | - | + |
| 3 | VGA480 | 31.5 KHz | 60 Hz | - | - |
| 4 | MACII35K | 35.0 KHz | 66 Hz | - | - |
| 5 | 800*600(56) | 35.2 KHz | 56 Hz | + | + |
| 6 | 8514A | 35.5 KHz | 87 Hz | + | + |
| 7 | 640*480(75) | 37.5 KHz | 75 Hz | - | - |
| 8 | EVGA400 | 37.8 KHz | 84 Hz | - | + |
| 9 | 800*600(60) | 37.8 KHz | 60 Hz | + | + |
| 10 | 640*480 | 43.3 KHz | 85 Hz | - | - |
| 11 | 800*600(75) | 46.8 KHz | 75 Hz | + | + |
| 12 | 1024*768(60) | 48.3 KHz | 60 Hz | - | - |
| 13 | MACII 49K | 49.7 KHz | 74 Hz | - | - |
| 14 | 800*600(85) | 53.6 KHz | 85 Hz | + | + |
| 15 | 1024*768(70) | 56.4 KHz | 70 Hz | - | - |
| 16 | 1024*768(75) | 60.0 KHz | 75 Hz | + | + |
| 17 | 640*480(120) | 63.7 KHz | 120 Hz | - | - |
| 18 | 1280*1024(60) | 64.0 KHz | 60 Hz | + | + |
| 19 | 800*600(100) | 64.0 KHz | 100 Hz | + | + |
| 20 | 1024*768(85) | 68.6 KHz | 85 Hz | + | + |

## 3. Normal Condition Definition

(A) Input AC Voltage $110 \mathrm{~V} / 60 \mathrm{~Hz}$.
(B) Warm up time minimum 30 minutes.
(C) Full White Pattern.
(D) All VR's adjust to Center Position.
(F) Color temp 9300K

## 4．Hot Key Operation

（A）Factory Mode：power on＋＇＋＇key＋＇－＇key．
＊To hide the Factory menu temporary in Factory mode：
Push＂RESET＂key once while Menu is displayed，then Menu disappears．
Push＂RESET＂key once more，then Menu reappears．
（B）Auto Alignment Mode：power on＋＇－＇key．
（C）Diagnosis Mode ：no sync power on＋＇Reset＇key．
（D）Factory Menu
TAB 1）BRIGHTNESS／CONTRAST


嫁：Brightness
O ：Contrast

TAB 2）POSITION／SIZE


TAB 3）COLOR ADJUST


| 1： 9300 K | 嫁：Brightness |
| :--- | :--- |
| 2： 8200 K | ：Contrast |
| 3：7500K | R G：Red Gain |
| sRGB：sRGB | G G：Green Gain |
| 5： 5000 K | B G：Blue Gain |
| 6：N／A | R B：Red Bias |
|  |  |
|  | G B：Green Bias |
|  |  |
|  | B B：Blue Bias |
|  |  |

TAB 4）DISTORTION

$\square:$ In／Out（Side Pincushion）
$\square:$ Left／Right（Pin Balance）
$\square:$ Tilt（Parallelogram）
$\square$ ：Align（Trapezoid）
$\square:$ Rotate
$\square:$ Top／Bottom Corner
氖：Vertical Linearity
目：Vertical Linearity Balance

TAB 5) TOOLS 1


Đ: Vertical Focus

TAB 7) INFORMATION



国 $x^{2}$ : Burnin Type Select
E: MCU Version
Wex : Destination
$\triangle$ : Hours Running
5. B+Check
(A) Mode: No. 12.
(B) Pattern: Full White. (Brightness set to cut off)
(C) Check other power sources are: $82 \mathrm{~V} \pm 2 \mathrm{~V}, 13.6 \mathrm{~V} \pm 0.3 \mathrm{~V}, 6.2 \mathrm{~V} \pm 0.3 \mathrm{~V}, 49 \mathrm{~V} \pm 1.5 \mathrm{~V},-11.5 \mathrm{~V} \pm 0.5 \mathrm{~V}$.
6. X-RAY Test
(A) Mode: No. 12
(B) Pattern: Normal Crosshatch (Brightness just cut off)
(C) Test

Apply a resistor(39K, 1/4W, 1\%) between TP3 and TP4 then power on, Monitor should be active in X-Ray protector.

## 7. H. V. B+ Confirmation

(A) Mode: No. 12
(B) Pattern: Full Black(Brightness just cut off)
(C) Check that the high voltage is $25.5 \mathrm{kV} \pm 0.7 \mathrm{kV}$.

## 8. H-Raster Center Adjustment

(A) Mode: No. 18
(B) Pattern: Crosshatch Reverse
(C) Adjust the Brightness Control so that the background is visible.
(D) Change SW301 position to center background raster.

## 9. Preset Picture Size and position Adjustment

(A) Factory mode setting
(B) Signal: All signals Pattern: Cross hatch

* Perform the preset picture size and position adjustment for above all signals.
(C) Select the " $\Theta$ " icon, then set to $70 \%$.

(E) Adjust the picture size and position as listed below by " - " and " + " SW.


## Picture size

$\mathrm{H}: 315 \pm 2 \mathrm{~mm}$
V: $236 \pm 2 \mathrm{~mm}$

Picture position
$\mathrm{H}:\left|\left(\mathrm{X}_{\text {тор }}-\mathrm{X}_{\text {воттом }}\right)\right| \leq 3 \mathrm{~mm}$


V: $\left.\mid \mathrm{X}_{\text {LEFT }}-\mathrm{X}_{\text {RIGHT }}\right) \mid \leq 3 \mathrm{~mm}$

## 10. White Balance adjustment

(A) Setting

Enter Factory Mode,
Mode: No.20, Pattern: Full White.
Warm up 60 min .
Make External Degauss.
(B) Cut Off Adjustment

1. Select the color Mode 9300K.
2. Cut Off Adjustment : Video Signal Off(0.Vp-p),Bright Control set to Max.
3. R.Bias, G.Bias and B.Bias set to $34.9 \%$.
4. Adjust the VR307, at the Brightness $3.4 \sim 5.1 \mathrm{~cd} / \mathrm{m}^{2}$, setting.
5. 9300K (Select color Mode 9300)

Adjust R.Bias, B.Bias to make $\mathrm{x}=283, \mathrm{y}=297$, with readjusting G 2 to keep the brightness between $3.4 \sim 5.1 \mathrm{~cd} / \mathrm{m}^{2}$.
(C) "9300K, $8200 \mathrm{~K}, 7500 \mathrm{~K}, 5000 \mathrm{~K}$ MODE" White Balance Adjustment

1. 9300 K (Select color Mode 9300K)
1) $50 * 50 \mathrm{~mm}$ Green block Pattern, Brightness Control set to Max., Contrast Control set to Max, Adjust G. Gain control to $Y=154 \mathrm{~cd} / \mathrm{m}^{2}$.
2) Video signal off ( $0 . V \mathrm{p}-\mathrm{p}$ ), Brightness control set to $0.2 \mathrm{~cd} / \mathrm{m}^{2}$.
3) Adjust R.Gain control and B.Gain control to $x=283, y=297$ (Pattern: Full White).
2. 8200 K (Select color Mode 8200 K )
1) $50 * 50 \mathrm{~mm}$ Green block Pattern, Brightness Control set to Max., Contrast Control set to Max, Adjust G. Gain control to $Y=154 \mathrm{~cd} / \mathrm{m}^{2}$.
2) Video signal off $0 . V p-p$ ), Brightness control set to $0.2 \mathrm{~cd} / \mathrm{m}^{2}$.
3) Adjust R.Gain control and B.Gain control to $x=290, y=313$ (Pattern: Full White).
3. 7500 K (Select color Mode 7500K)
1) $50 * 50 \mathrm{~mm}$ Green block Pattern, Brightness Control set to Max., Contrast Control set to Max, Adjust G. Gain control to $Y=154 \mathrm{~cd} / \mathrm{m}^{2}$.
2) Video signal off ( $0 . V p-p$ ), Brightness control set to $0.2 \mathrm{~cd} / \mathrm{m}^{2}$.
3) Adjust R.Gain control and B.Gain control to $x=300, y=315$ (Pattern: Full White).
4. 5000K (Select color Mode 5000K)
1) $50 * 50 \mathrm{~mm}$ Green block Pattern, Brightness Control set to Max., Contrast Control set to Max, Adjust G. Gain control to $Y=154 \mathrm{~cd} / \mathrm{m}^{2}$.
2) Video signal off ( $0 \mathrm{Vp}-\mathrm{p}$ ), Brightness control set to $0.2 \mathrm{~cd} / \mathrm{m}^{2}$.
3) Adjust R.Gain control and B.Gain control to $x=345, y=359$ (Pattern: Full White).
5. ABL Adjustment and Brightness Preset
1) Color set to 9300K. Pattern is Full White.
2) Brightness, contrast control to max., Adjust "AB" to $Y=103 \mathrm{~cd} / \mathrm{m}^{2}$.
3) Brightness preset: set to 1.2) position -40 steps.
(D) "sRGB MODE" White Balance Adjustment (Select color Mode sRGB)
4) Contrast set to Max., Adjust Brightness to Max.
5) Change Pattern to $50 * 50 \mathrm{~mm}$ Green block, Adjust G.Gain control to $Y=154 \mathrm{~cd} / \mathrm{m}^{2}$.
6) Video Signal off ( $0 . V p-p$ ), Adjust Brightness to $0.1 \mathrm{~cd} / \mathrm{m}^{2}$.
7) Change Pattern to $50 * 50 \mathrm{~mm}$ White block, Adjust R.Gain and B.Gain to control to $x=313, y=329$.
8) Adjust contrast control to $Y=96 \mathrm{~cd} / \mathrm{m}^{2}$.

Note: Do not readjust the Contrast control at sRGB mode after W/B adjustment finish.
(E) "SB MODE" White Balance Adjustment (Select the color Mode SB MODE)

1) Select the color mode "SB Mode".
2) Video signal off ( $0 V p-p$ ), Adjust brightness to $0.1 \mathrm{~cd} / \mathrm{m}^{2}$, contrast to Max.
3) Change pattern to $50 * 50$ green block, Adjust G.Gain control to $Y=223 \mathrm{~cd} / \mathrm{m}^{2}$.
4) Change pattern to $50 * 50$ white block, Adjust R.Gain and B.Gain to $x=283, y=297$.
5) Change pattern to Full white, Brightness to Max.

Adjust "AB" of SB Mode to $Y=103 \mathrm{~cd} / \mathrm{m}^{2}$.
6) Brightness preset : Video Signal off (0Vp-p), Adjust Brightness to $0.1 \mathrm{~cd} / \mathrm{m}^{2}$.

## 11. Focus Adjustment

(A) Mode: No. 16 (VESA 1024*768(75))
(B) Pattern: Green Crosshatch, Brightness just cut off, Contrast maximum.
(C) Adjust F1 VR of FBT (lower side VR) for the vertical line to become fine line.
(D) Adjust F2 VR of FBT (higher side VR) for the horizontal line to become fine line.
(E) Receive Focus adjustment pattern.
(F) Adjust F1 VR if vertical black line is not fall out.
(G) Adjust F2 VR if horizontal black line is not fall out.
(H) Use the video card "Trio64+", and receive Microsoft Excel "Work sheet" (1024*768(85)).

Make sure that there is no double line for horizontal at the center.
*Note: Focus adjustment must be finished at F1 VR.



Focus VR

## 12. Purity Adjustment

(1) Receive signal 14 (Cross hatch pattern).
(2) The CRT face should be facing east and degauss the entire unit by external degaussing coil.
(3) Make sure the single color purity.

If not, readjust CPC magnet and touch up using correction magnets.

## 13. Convergence Adjustment

CH : Convergence error of horizontal direction
CV : Convergence error of vertical direction
(1) Receive signal 14 (Cross hatch pattern).

(2) Measure convergence error. If it is out of spec, adjust convergence by 4 -pole magnets and 6 -pole magnets.


A Zone (A circle 236 mm in the center of the CRT face center)
CH, CV : Within 0.25 mm

B Zone (Areas outside of zone A within the rectangle of $315 \mathrm{~mm} x 236 \mathrm{~mm}$ )
CH, CV : Within 0.35 mm

## 14. Power Saving Function Inspection

(A) Mode: No. 20
(B) Pattern: Full white
(C) Input voltage: AC240V/50Hz
(D) Inspection

1. It should be into power off Mode when the both horizontal sync and vertical sync are disable after 8 seconds. Check the LED color "Orange" and the power consumption must be less than 5W.
2. It should be recovered the normal Mode when the both horizontal sync and vertical sync are enable. Check the picture is normal and LED color "Green".

## 15. Distortion Adjustment

Factory mode setting

* After completion of adjustment exit the factory mode and data will be saved.


## Signal: All signals Cross hatch

Perform the adjust for signal No. 14 in step $1 \sim 3$.
Perform the adjust for above all signal in step $4 \sim 5$.

1. Rotation Adjustment
(1) Receive signal 14 (Cross hatch)
(2) Select the " [] " icon in OSM TAB 4.
(3) Make sure that the picture tilt meets the following standards.

2. Pincushion Balance Adjustment
(1) Select the " $\square$ " icon in OSM TAB 4.
(2) Make sure that the Pincushion Balance meets the following standards.

$$
A-B \leq 0.5 \mathrm{~mm}
$$



A B
3. Parallelogram distortion Adjustment
(1) Select the " $\square$ " icon in OSM TAB 4.
(2) Adjust "+", "-" SW so that the vertical line and horizontal line at the screen's center fall at right angles. (less than $90 \pm 0.5$ degree)

$\times$

$\square$

$\times$
4. Side Pincushion Adjustment
(1) Select the " $\square$ " icon in OSM TAB 4.
(2) Make sure that the side pincushion distortion meets the following standards.


## 5. Trapezoid Distortion Adjustment

(1) Select the " $\square$ " icon in OSM TAB 4.
(2) Make sure that the trapezoid distortion meets the following standards.


## 16. Setting Before Shipment

(A) Do Factory Preset in OSM TAB 6.
(B) Set to following.

TAB: Language ... English
OSM Lock ... OFF
IPM OFF MODE ... Enable

## 17. Adjustment Magnetic Field

Vertical: +40uT, Horizontal: $\pm 0 \mathrm{uT}$ (Neutral)

* Notes About Degaussing Method

Follow the degaussing procedure as below. (For prevent intertwinement of aperture grille.)

1) Use stick type degaussing probe at demagnetizing CRT.

Do not use ring type degaussing probe.
2) In order to remove a magnetization from front, top, bottom and side of CRT, and bottom chassis.

Do not switch off the degaussing probe abruptly. Move the degaussing probe slowly when degaussing.
Note: If switch off the degaussing probe near the set, the set will be magnetized.
3) Degaussing method

When switch on the degaussing probe, keep distance between panel surface and degaussing probe more than 50 cm . Move the degaussing probe vertically facing to the panel surface.

## Keep distance of panel surface and degaussing probe to more than 15 mm .

Starting from edge of CRT, move the degaussing probe toward CRT center in circular motion, spending 6 to 7 seconds. (Rounding about 4 or 5 times.)



Vertical



Horizontal
4) After sufficiently degaussing the CRT, move the degaussing probe slowly away from the panel surface while rotating from corner to center, taking more than 3 seconds. Turn off SW more than 1 m away from the CRT. Degauss again if the unit is magnetized.


## 18. TIMING SHEET

Rev1. 0

| Preset Mode No. | 1 | 2 | 3 | 4 | 5 | 6 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Signal Name | VGA350 | VGA400 | VGA480 | MACII (35k) | 800*600 <br> (56) | $\begin{gathered} \text { 8514/A } \\ \text { XGA } \end{gathered}$ |
| Resolution | 640*350 | 640*400 | 640*480 | 640*480 | 800*600 | 1024*768 |
| Dot Clock (MHz) | 25.175 | 25.175 | 25.175 | 30.240 | 36.000 | 44.900 |
| fh (kHz) | 31.47 | 31.47 | 31.47 | 35.00 | 35.16 | 35.52 |
| fv ( Hz ) | 70.09 | 70.09 | 59.94 | 66.67 | 56.25 | 86.96 |
| Total <br> (dot) <br> (uS) | 800 31.78 | 800 31.78 | 800 31.78 | $\begin{array}{r} 864 \\ 28.57 \end{array}$ | $\begin{array}{r} 1024 \\ 28.44 \\ \hline \end{array}$ | $\begin{array}{r} 1264 \\ 28.15 \\ \hline \end{array}$ |
| Disp (dot) <br>  $(\mathrm{uS})$ | $\begin{array}{r} 640 \\ 25.42 \end{array}$ | 640 25.42 | 640 25.42 | 640 21.16 | 800 22.22 | 1024 22.81 |
| Front (dot) <br>  (uS) | 16 0.64 | $\begin{array}{r}16 \\ 0.64 \\ \hline\end{array}$ | $\begin{array}{r}16 \\ 0.64 \\ \hline\end{array}$ | 64 2.12 | 24 0.67 | $\begin{array}{r}8 \\ 0.18 \\ \hline\end{array}$ |
| Sync Pulse (dot) <br> (uS) | 96 3.18 | $\begin{array}{r}96 \\ 3.81 \\ \hline\end{array}$ | $\begin{array}{r}96 \\ 3.81 \\ \hline\end{array}$ | $\begin{array}{r}64 \\ 2.12 \\ \hline\end{array}$ | $\begin{array}{r}72 \\ 2.00 \\ \hline\end{array}$ | $\begin{array}{r}176 \\ 3.92 \\ \hline\end{array}$ |
| Back $(\mathrm{dot})$ <br>  $(\mathrm{uS})$ | 48 1.91 | 48 1.91 | 48 1.91 | 96 3.17 | 128 3.56 | $\begin{array}{r}56 \\ 1.25 \\ \hline\end{array}$ |
| Total $(\mathrm{H})$ <br>  $(\mathrm{mS})$ | $\begin{array}{r} 449 \\ 14.268 \end{array}$ | 449 14.268 | 525 16.683 | 525 15.000 | 625 17.778 | $\begin{array}{r}408.5 \\ 11.500 \\ \hline\end{array}$ |
| Disp $(\mathrm{H})$ <br>  $(\mathrm{mS})$ | $\begin{array}{r} 350 \\ 11.122 \end{array}$ | $\begin{array}{r} 400 \\ 12.711 \end{array}$ | $\begin{array}{r} 480 \\ 15.253 \end{array}$ | 480 13.714 | $\begin{array}{r} 600 \\ 17.067 \end{array}$ | 384 10.810 |
| Front $(\mathrm{H})$ <br>  $(\mathrm{mS})$ | 37 1.176 | 12 0.381 | 10 0.318 | 3 0.086 | 1 0.028 | 0 0.000 |
| Sync Pulse $(\mathrm{H})$ <br>  $(\mathrm{mS})$ | 2 0.064 | 2 0.064 | 2 0.064 | 3 0.086 | 2 0.057 | 4 0.113 |
| Back $(\mathrm{H})$ <br>  $(\mathrm{mS})$ | $\begin{array}{r} 60 \\ 1.907 \\ \hline \end{array}$ | 35 1.112 | 33 1.049 | 39 1.114 | 22 0.626 | 20 0.563 |
| Interlace | NON | NON | NON | NON | NON | YES |
| Polarity (H/V) | POS/NEG | NEG/POS | NEG/NEG | NEG/NEG | POS/POS | POS/POS |
| Composite Sync |  |  |  | NEG |  |  |
| Composite Video |  |  |  |  |  |  |
| Character Font | 7*9 | 7*9 | 7*9 | 7*9 | 7*9 | 7*9 |
| Serration | OFF | OFF | OFF | ON | OFF | OFF |
| EQP | OFF | OFF | OFF | OFF | OFF | OFF |


| Preset Mode No. | 7 | 8 | 9 | 10 | 11 | 12 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Signal Name | $640 * 480$ <br> (75) | $\begin{gathered} \text { EVGA400 } \\ \text { (VESA) } \\ \hline \end{gathered}$ | $\begin{gathered} 800 * 600 \\ (60) \\ \hline \end{gathered}$ | $\begin{gathered} 640 * 480 \\ (85) \\ \hline \end{gathered}$ | 800*600 <br> (75) | $10 * 7(60)$ <br> (VESA) |
| Resolution | 640*480 | 640*400 | 800*600 | 640*480 | 800*600 | 1024*768 |
| Dot Clock (MHz) | 31.500 | 31.5000 | 40.000 | 36.000 | 49.500 | 65.000 |
| fh (kHz) | 37.50 | 37.86 | 37.88 | 43.27 | 46.88 | 48.36 |
| fv ( Hz ) | 75.00 | 84.13 | 60.32 | 85.01 | 75.00 | 60.00 |
| Total <br>  | $\begin{array}{r} 840 \\ 26.67 \\ \hline \end{array}$ | $\begin{array}{r} 832 \\ 26.41 \\ \hline \end{array}$ | $\begin{array}{r} 1056 \\ 26.40 \\ \hline \end{array}$ | $\begin{array}{r} 832 \\ 23.11 \\ \hline \end{array}$ | $\begin{array}{r} 1056 \\ 21.33 \\ \hline \end{array}$ | $\begin{array}{r} 1344 \\ 20.68 \\ \hline \end{array}$ |
| Disp (dot) <br>  (uS) | 640 20.32 | $\begin{array}{r} 640 \\ 20.32 \end{array}$ | $\begin{array}{r} 800 \\ 20.00 \end{array}$ | $\begin{array}{r} 640 \\ 17.78 \end{array}$ | $\begin{array}{r} 800 \\ 16.16 \end{array}$ | $\begin{array}{r} 1024 \\ 15.75 \end{array}$ |
| Front(dot)  <br>  (uS) | 16 0.51 | 24 0.76 | $\begin{array}{r} 40 \\ 1.00 \end{array}$ | $\begin{array}{r}56 \\ 1.56 \\ \hline\end{array}$ | 16 0.32 | $\begin{array}{r}24 \\ 0.37 \\ \hline\end{array}$ |
| Sync Pulse (dot) <br>  $(\mathrm{uS})$ | 64 2.03 | $\begin{array}{r}40 \\ 1.27 \\ \hline 128\end{array}$ | 128 3.20 | $\begin{array}{r}56 \\ 1.56 \\ \hline\end{array}$ | $\begin{array}{r}80 \\ 1.62 \\ \hline 160\end{array}$ | $\begin{array}{r}136 \\ 2.09 \\ \hline\end{array}$ |
| Back <br>  <br>  <br>  <br> (dot) <br> (uS) | 120 3.81 | 128 4.06 | 88 2.20 | 80 2.22 | 160 3.23 | $\begin{array}{r}160 \\ 2.46 \\ \hline\end{array}$ |
| Total $(\mathrm{H})$ <br>  $(\mathrm{mS})$ | $\begin{array}{r} 500 \\ 13.333 \end{array}$ | $\begin{array}{r} 450 \\ 11.886 \end{array}$ | $\begin{array}{r} 628 \\ 16.579 \end{array}$ | $\begin{array}{r} 509 \\ 11.76 \\ \hline \end{array}$ | $\begin{array}{r} 625 \\ 13.333 \end{array}$ | $\begin{array}{r}806 \\ 16.666 \\ \hline\end{array}$ |
| Disp $(\mathrm{H})$ <br>  $(\mathrm{mS})$ | $\begin{array}{r} 480 \\ 12.800 \end{array}$ | $\begin{array}{r} 400 \\ 10.565 \end{array}$ | $\begin{array}{r} 600 \\ 15.840 \end{array}$ | $\begin{array}{r} 480 \\ 11.093 \end{array}$ | $\begin{array}{r} 600 \\ 12.800 \end{array}$ | $\begin{array}{r}768 \\ 15.880 \\ \hline\end{array}$ |
| Front$(\mathrm{H})$  <br>  $(\mathrm{mS})$ | 1 0.027 | 9 ${ }^{9}$ | $\begin{array}{r} 1 \\ 0.026 \end{array}$ | 1 1 | 1 0.021 | $\begin{array}{r}3 \\ 0.062 \\ \hline\end{array}$ |
| $\begin{array}{lc}\text { Sync Pulse } & (\mathrm{H}) \\ & (\mathrm{mS})\end{array}$ | 3 0.080 | $\begin{array}{r} 3 \\ 0.079 \end{array}$ | $\begin{array}{r} 4 \\ 0.106 \end{array}$ | 3 0.069 | 3 0.064 | $\begin{array}{r}6 \\ 0.124 \\ \hline\end{array}$ |
| Back $(\mathrm{H})$ <br>  $(\mathrm{mS})$ | $\begin{array}{r} 16 \\ 0.427 \end{array}$ | $\begin{array}{r} 38 \\ 1.004 \end{array}$ | $\begin{array}{r} 23 \\ 0.607 \end{array}$ | $\begin{array}{r} 25 \\ 0.578 \end{array}$ | $\begin{array}{r} 21 \\ 0.448 \end{array}$ | $\begin{array}{r} 29 \\ 0.600 \end{array}$ |
| Interlace | NON | NON | NON | NON | NON | NON |
| Polarity (H/V) | NEG/NEG | NEG/POS | POS/POS | NEG/NEG | POS/POS | NEG/NEG |
| Composite Sync |  |  |  |  |  |  |
| Composite Video |  |  |  |  |  |  |
| Character Font | 7*9 | 7*9 | 7*9 | 7*9 | 7*9 | 7*9 |
| Serration | OFF | OFF | OFF | OFF | OFF | OFF |
| EQP | OFF | OFF | OFF | OFF | OFF | OFF |


| Preset Mode No. | 13 | 14 | 15 | 16 | 17 | 18 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Signal Name | $\begin{aligned} & \text { MACII } \\ & (49.7 \mathrm{k}) \end{aligned}$ | $\begin{gathered} 800 * 600 \\ (85) \\ \hline \end{gathered}$ | 10*7(70) <br> (VESA) | $10 * 7(75)$ <br> (VESA) | $\begin{gathered} 640 * 480 \\ (120) \\ \hline \end{gathered}$ | $\begin{gathered} 12 * 10(60) \\ (\text { VESA }) \end{gathered}$ |
| Resolution | 832*624 | 800*600 | 1024*768 | 1024*768 | 640*480 | 1280*1024 |
| Dot Clock (MHz) | 57.286 | 56.250 | 75.000 | 78.750 | 55.00 | 108.000 |
| fh (kHz) | 49.73 | 53.67 | 56.48 | 60.02 | 63.66 | 63.98 |
| fv ( Hz ) | 74.55 | 85.06 | 70.07 | 75.03 | 120.11 | 60.02 |
| Total (dot) <br> (uS) | $\begin{array}{r} 1152 \\ 20.11 \\ \hline \end{array}$ | $\begin{array}{r} 1048 \\ 18.63 \\ \hline \end{array}$ | $\begin{array}{r} 1328 \\ 17.71 \end{array}$ | $\begin{array}{r} 1312 \\ 16.66 \end{array}$ | $\begin{array}{r} 864 \\ 15.71 \end{array}$ | $\begin{array}{r} 1688 \\ 15.63 \end{array}$ |
| Disp (dot) <br>  (uS) | 832 14.52 | $\begin{array}{r} 800 \\ 14.22 \end{array}$ | $\begin{gathered} 1024 \\ 13.65 \end{gathered}$ | $\begin{array}{r} 1024 \\ 13.00 \end{array}$ | $\begin{array}{r} 640 \\ 11.645 \end{array}$ | $\begin{gathered} 1280 \\ 11.85 \end{gathered}$ |
| Front(dot)  <br>  (uS) | 32 0.56 | $\begin{array}{r}32 \\ 0.57 \\ \hline\end{array}$ | 24 0.32 | 16 0.20 | 32 0.582 | $\begin{array}{r}48 \\ 0.44 \\ \hline\end{array}$ |
| $\begin{array}{lr}\text { Sync Pulse } & \text { (dot) } \\ & \text { (uS) }\end{array}$ | $\begin{array}{r}64 \\ 1.12 \\ \hline\end{array}$ | 64 1.14 | $\begin{array}{r} 136 \\ 1.81 \end{array}$ | $\begin{array}{r}96 \\ 1.22 \\ \hline\end{array}$ | $\begin{array}{r}96 \\ 1.745 \\ \hline\end{array}$ | $\begin{array}{r}112 \\ 1.04 \\ \hline\end{array}$ |
| Back <br>  <br>  <br>  <br> (dot) <br> (uS) | 224 3.91 | 152 2.70 | 144 1.92 | 176 2.23 | 96 1.745 | $\begin{array}{r}248 \\ 2.30 \\ \hline\end{array}$ |
| Total $(\mathrm{H})$ <br>  $(\mathrm{mS})$ | $\begin{array}{r} 667 \\ 13.413 \end{array}$ | $\begin{array}{r} 631 \\ 11.756 \end{array}$ | $\begin{array}{r} 806 \\ 14.272 \end{array}$ | 800 13.328 | $\begin{array}{r} 530 \\ 8.325 \\ \hline \end{array}$ | $\begin{array}{r}1066 \\ 16.661 \\ \hline\end{array}$ |
| Disp $(\mathrm{H})$ <br>  $(\mathrm{mS})$ | $\begin{array}{r} 624 \\ 12.548 \end{array}$ | $\begin{array}{r} 600 \\ 11.179 \end{array}$ | $\begin{array}{r} 768 \\ 13.599 \end{array}$ | $\begin{array}{r} 768 \\ 12.795 \end{array}$ | $\begin{array}{r} 480 \\ 7.540 \end{array}$ | $\begin{array}{r}1024 \\ 16.005 \\ \hline\end{array}$ |
| Front$(\mathrm{H})$  <br>  $(\mathrm{mS})$ | 1 0.020 | 1 ${ }^{1}$ | 3 0.053 | 1 1 | 8 0.126 | $\begin{array}{r}1 \\ 0.016 \\ \hline\end{array}$ |
| $\begin{array}{lc}\text { Sync Pulse } & (\mathrm{H}) \\ & (\mathrm{mS})\end{array}$ | 3 0.060 | $\begin{array}{r} 3 \\ 0.056 \end{array}$ | $\begin{array}{r} 6 \\ 0.106 \end{array}$ | 3 0.050 | 6 0.094 | $\begin{array}{r}3 \\ 0.047 \\ \hline\end{array}$ |
| Back $(\mathrm{H})$ <br>  $(\mathrm{mS})$ | $\begin{array}{r} 39 \\ 0.784 \end{array}$ | $\begin{array}{r} 27 \\ 0.503 \end{array}$ | $\begin{array}{r} 29 \\ 0.513 \end{array}$ | $\begin{array}{r} 28 \\ 0.466 \end{array}$ | $\begin{array}{r} 36 \\ 0.566 \end{array}$ | $\begin{array}{r} 38 \\ 0.594 \end{array}$ |
| Interlace | NON | NON | NON | NON | NON | NON |
| Polarity (H/V) | NEG/NEG | POS/POS | NEG/NEG | POS/POS | NEG/NEG | POS/POS |
| Composite Sync | NEG |  |  |  |  |  |
| Composite Video |  |  |  |  |  |  |
| Character Font | 7*9 | 7*9 | 7*9 | 7*9 | 7*9 | 7*9 |
| Serration | ON | OFF | OFF | OFF | OFF | OFF |
| EQP | OFF | OFF | OFF | OFF | OFF | OFF |



## INSPECTION

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## 1.Scope

### 1.1 Introduction

This document defines the design and performance requirements for a 17 inch (16 inch Viewable), color display monitor. This monitor shall use a 17 inch Flat Aperture Grille type CRT. This monitor is capable of maximum resolution of $1280 \times 1024$ pixels at 66 Hz non-interlaced mode, and is capable of horizontal frequencies between 30 kHz and 70 kHz .

The following list shows the model name, Cabinet color, Audio function, and market.

| CODE NAME | MODEL NAME | Cabinet <br> color | Audio <br> Base | MARKET | Ver. |
| :--- | :--- | :--- | :--- | :--- | :--- |
| Dplus74SB-BK(A) | Diamond Plus 74SB-BK | Black | No | USA/Canada | A ver. |
| Dplus74SB(B) | Diamond Plus 74SB | White | No | Europe | B ver. |

### 1.2 General Description

### 1.2.1 Display Part

MODEL:1702

| NO | Item |  |  | Spec. | REMARKS |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | CRT | Vendor / Model No. |  | Mitsubishi / M41LRY61X22 |  |
|  |  | Type |  | Diamondtron M2 (Aperture Grille) |  |
|  |  | Size |  | $43 \mathrm{~cm} / 406 \mathrm{~mm}$ Diagnonal Viewable Image (17" / 16" Diaqonal Viewable Image) |  |
|  |  | Grille pitch(Phosphor pitch) |  | Approx.0.25mm (Approx.0.26mm) | Aperture Grille |
|  |  | Phosphor Type |  | P22 |  |
|  |  | Face-plate |  | AR-film(Anti-reflection and Anti-static) |  |
|  |  | Electron Gun Type |  | PX-DBF |  |
|  |  | Face-plate Transmission |  | approx.38\% |  |
| 2 | SCANNING | Horizontal Freq |  | $30.0-70.0 \mathrm{kHz}$ |  |
|  |  | Vertical Freq. |  | $50-120 \mathrm{~Hz}$ |  |
| 3 | SIGNAL INPUT | Video Sync |  | Analog | 0.7Vp-p |
|  |  |  |  | Composite Sync | TTL Pos / Neg |
|  |  |  |  | Separate Sync | TTL Pos / Neg |
|  |  | Termination (Impedance) | Video | 75 ohm to GND |  |
|  |  |  | Sync. | 2.2K ohm to GND or more |  |
| 4 |  VIDEO <br> CHARACTERISTICS  | Clock frequency |  | 120 MHz |  |
| 5 |  | Display Resolution(Maximum) |  | $\begin{array}{\|l\|} \hline 1280 \times 1024(66 \mathrm{~Hz}) \text { (Maximum) } \\ 1024 \times 768(85 \mathrm{~Hz}) \text { (recommend) } \\ \hline \end{array}$ |  |
|  |  | Display Size | Preset | $315 \mathrm{~mm}(\mathrm{H})$ * 236 mm (V) |  |
|  |  |  | FullScan | $325 \mathrm{~mm}(\mathrm{H}){ }^{*} 244 \mathrm{~mm}$ (V) |  |
|  |  | Misconvergence |  | Center: 0.25 mm , Corner : 0.35 mm |  |
|  |  | Brightness (Full White) |  | 90cd/m ${ }^{2}$ (typ.) at 9300K |  |
| 6 | CONTROL (User Controls) | Front  <br>  OSM |  | Power SW <br> Exit, Left, Right, "-", "+", Select, Reset <br> Note: User can change Super Bright Mode by pressing a Select key. | 7 control buttons |
|  |  |  |  | Brightness, Contrast, Degauss <br> H.Size, H.Position, V.Size, V.Position, <br> Color Control (9300K, 8200K, 7500K, sRGB 5000K) <br> ColorTemperature Control, RGB Gain Control(USER) <br> SidePin In/Out, Side Pin Left/Right, Parallelogram, Trapezoid, Rotation, <br> Moire Cancel(Horizontal) <br> Language, OSM Position, OSM Turn off, OSM Lock, IPM OFF mode, <br> Factory Preset <br> URL indication, Display Mode, Monitor info, Refresh Notifier Diagnosis Indication | Micro-processor control |
| 7 | CONNECTOR | Power Input Signal Input |  | Power Cord (Length:1.8m, Color: Haze gray) |  |
|  |  |  |  | Mini 15pin D-sub (Length:1.8m, Color:Haze gray) |  |
| 8 | POWER SUPPLY | Operating Range |  | AC100-240V, $50-60 \mathrm{~Hz}$ |  |
|  |  | Power Consumption (Max.) |  | 70W 1.5A@100-240VAC $\text { Power save } \leq 5 \mathrm{~W}$ |  |
| 9 | ENVIRONMENTAL CONDITION | Operating Temperature |  | $5-35{ }^{\circ} \mathrm{C}$ |  |
|  |  | Operating Humidity |  | 10-90\% (without condensation) |  |
| 10 | WEIGHT |  |  | Net : $16.8 \mathrm{~kg} / 37.0 \mathrm{lbs}$, Gross : $19.8 \mathrm{~kg} / 43.7 \mathrm{l}$ bs |  |
| 11 | DIMENSIONS | Cabinet with Tilt / Swivel stand Carton |  | Net : W 397.0mm(15.6"), H $392.0 \mathrm{~mm}\left(15.4^{\prime \prime}\right)$, D $415.5 \mathrm{~mm}\left(16.4^{\prime \prime}\right)$ Gross(Aver): W 530mm(20.9"), H $520 \mathrm{~mm}\left(20.5^{\prime \prime}\right)$, D 565mm(22.2") Gross(B/Jver): W $510 \mathrm{~mm}\left(20.1^{\prime \prime}\right)$, H $513 \mathrm{~mm}\left(20.2^{\prime \prime}\right)$, D $565 \mathrm{~mm}\left(22.2^{\prime \prime}\right)$ |  |
| 12 | REGULATION | Safety |  | UL1950(UL), CSA C22.2 No.950(C-UL), EN60950(TUV-GS), PCBC, GOST, PSB |  |
|  |  | EMC |  | FCC-B, DOC-B, EN55022-B, EN61000-3-2,-3-3, EN55024(IEC61000-4-2,-4-3,-4-4,-4-5,-4-6,-4-8,-4-11), C-tick |  |
|  |  | X-Ray |  | DHHS, Red Act, PTB |  |
|  |  | VLF / ELF |  | pr EN50279(MPR-III), TCO'99(Exceept Aver Black), TCO'95(For Aver Black) |  |
|  |  | Power Management |  | Energy Star, TCO99 (Except Aver Black), TCO'95 (For Aver Black) |  |
|  |  | Ergonomics |  | $\begin{aligned} & \hline \text { (ISO9241-3, ISO9241-7, ISO9241-8), } \\ & \text { TCO'99 (Except Aver Black), TCO'95 (For Aver Black) } \end{aligned}$ |  |
|  |  | Miscellaneous |  | TCO'99 (Except Aver Black), TCO'95 (For Aver Black), CE marking |  |
|  |  | Others |  | WHQL (Win ME, Win 2000, Win XP) DDC/CI |  |
| 13 | OTHERS | Plug \& Play |  | DDC2B,DDC/Cl (Support 9pin-5V) |  |
| 14 | FEATURE |  |  | $\begin{array}{\|l\|} \hline \begin{array}{l} \text { Self Diagnosis } \\ \text { Super Bright Mode } \end{array} \\ \hline \end{array}$ |  |

### 1.3 Regulations

| GEOGRAPHICAL | REGULATIONS |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| REGION | SAFETY | EMC | X-RAY | ELF/VLF | Power <br> Management | Ergonomics | Miscellaneous <br> And others |
| Dplus74SB-BK(A) | UL C-UL TUV/GS | FCC-B | DHHS <br> Red Act | $\begin{aligned} & \text { MPR-III } \\ & \text { TCO'99 } \\ & \text { (White) } \\ & \begin{array}{l} \text { TCO'95 } \\ \text { (Black) } \end{array} \end{aligned}$ | Energy Star TCO'99 (White) TCO'95 (Black) | TUV-GS (IS9241-3 IS9241-7 IS9241-8) TCO'99 (White) TCO'95 (Black) | CE Marking <br> WHQL <br> (Win ME, <br> Win 2000, <br> Win XP) |
| Dplus74SB(B) | UL C-UL TUV-GS PCBC <br> Gost <br> PSB | C-tick <br> EN55022-B <br> EN55024 <br> EN61000-3-2 <br> EN61000-3-3 | PTB | $\begin{aligned} & \text { MPR-IIII } \\ & \text { TCO'99 } \end{aligned}$ | $\begin{aligned} & \text { Energy Star } \\ & \text { TCO'99 } \end{aligned}$ | TUV-GS (IS9241-3 IS9241-7 IS9241-8) TCO'99 | CE Marking <br> WHQL <br> (Win ME, <br> Win 2000, <br> Win XP) |

*: This model is applied these regulations in case of including the audio base.

### 1.4 Regulation Information \& Marking Location

| Marking Location | Regulation | Information |
| :---: | :---: | :---: |
| (1) | UL | UL1950 3rd Edition (or UL60950 $3^{\text {rd }}$ edition) |
| (1) | C-UL | CAN/CSA-C22.2 NO.950:1995 (or CAN/CSA-C22.2 No.60950:2000) |
| (1), (2) | TUV-GS | EN60950 : 1992 \& AD1/AD2/AD3/AD4/AD11, (or EN60950:2000) EK1-ITB 2000,ISO9241-3: 1992, ISO9241-7: 1998, ISO9241-8: 1997 |
| (1) | PSB | Singapore Safety |
| (1) | CCIB | Chinese Safety \& EMI |
| (1), (2) | FCC | 47 CFR Chapter I Subpart B, Class B |
| - | DOC | Interference-Causing Equipment Standard ICES-003 Issue 3,Class B |
| - | DHHS | 21CFR Chapter I Subchapter J |
| - | Red Act | Radiation Emitting Devices Act |
| - | PTB | German X-ray |
| - | MPR-II | MPR1990:10, MPR1990:8 |
| - | MPR-III | prEN50297 |
| (1), (2), (3) | TCO'95 | Requirements for environmental labeling of personal computers |
| (1), (2), (3) | TCO'99 | Requirements and test methods for environmental labeling of display (CRT) and Ecology |
| (1), (2), (3) | CE-Marking | EN60950: 1992 \& AD1/AD2/AD3/AD4/AD11 <br> EN55022: 1998 Class B, <br> EN55024: 1998(IEC61000-4-2, -4-3, -4-4, -4-5, -4-6, -4-8, -4-11) <br> EN61000-3-2 : 1995 \& AD1/AD2, EN61000-3-3 : 1995 |
| (2) | Energy Star | International Energy Star office Equipment Program |
| (1), (2), (3) | PCBC | Poland Safety |
| (1), (2), (3) | Gost | Russian Safety |
| (1), (2) | C-tick | AS/NZS3548:1995+A1/A2:1997 |
| (2), (3) | WHQL | Microsoft Windows® Hardware Quality Labs |

Note:
(1) The mark is printed on the " Rating Label".
(2) The mark is printed on the "Carton Box".
(3) The mark is printed on the "User's Manual".
2. CRT Specifications

| Vendor | Mitsubishi |
| :---: | :---: |
| CRT Model No. | M41LRY61X22 |
| Type | Diamondtron M2 (Aperture Grille) |
| Size | 448.8 mm (17" diagonal surface) <br> 406.4 mm (16" diagonal viewable image) |
| Grille pitch (Phosphor pitch) | Approx.0.25mm (Approx. 0.26 mm ) |
| Deflection Angle | 90 degree |
| Phosphor Type | P22 |
| Electron Gun Type | PX-DBF type |
| Light Transmission at Center (Approx.) | Approx. 38\% (Include Face-plate coating) |
| Face-plate | AR-film <br> (Anti-reflection and Anti-static) |
| Useful Screen dimensions | $325.1 \mathrm{~mm} \times 243.8 \mathrm{~mm}$ |
| Face-plate Curvature | $\mathrm{H}: \mathrm{R}=50000 \mathrm{~mm}, \mathrm{~V}: \mathrm{R}=80000 \mathrm{~mm}$ |
| Phosphor Color Coordinate | $R: x=0.626 \pm 0.020, y=0.338 \pm 0.020$ <br> $G: x=0.278 \pm 0.020, y=0.601 \pm 0.020$ <br> B: $x=0.150 \pm 0.020, y=0.068 \pm 0.020$ |

## 3. Electric Specifications

### 3.1 Deflections

| Horizontal | Scanning Frequency | $30.0-70.0 \mathrm{kHz}$ |
| :--- | :--- | :--- |
|  | Back Porch | $\geq 0.2 \mu \mathrm{sec}$ |
|  | Blanking | $\geq 3.6 \mu \mathrm{sec}$ |
|  | H-sync Width | $\geq 0.8 \mu \mathrm{sec}$ |
| Vertical | Scanning frequency | $50-120 \mathrm{~Hz}$ |
|  | V-sync + V-back Porch | $\geq 500 \mu \mathrm{sec}$ |
|  | V-sync Width | $2 \mathrm{H} \leq \mathrm{Vs} \leq 8 \mathrm{H}$ |
|  | V-Total Line | $\geq 256 \mathrm{H}+\mathrm{V}$-sync Width |

### 3.2 Signal Input

| Video Input Signal | R.G.B analog |
| :--- | :--- |
| Sync. Input Signal | External composite sync :TTL (N or P) <br> External HD ND separate sync :TTL (N or P) |
| Video Input Impedance | 75 ohm to ground |
| Sync. Input Impedance | 2.2 k ohm to grand or more. |
| Signal Level | Video signal $: 0.70 \mathrm{~V}$ p-p $\pm 5 \%$ <br> Composite sync TTL level <br> Separate H $/ \mathrm{V}$-sync $:$ TTL level |

### 3.3 Video Performance

| Video Clock Frequency | 120 MHz (Input signal) |
| :--- | :--- |
| Pulse Rise and Fall time | 9.0 nsec (typ.) 10 to $90 \%$ at 40Vp-p |

The rise and fall time of the input video signal is 2.0 nsec or less.
The pulse rise or fall time is determined using the formula :

$$
\begin{aligned}
& T a=\sqrt{T m^{2}}-\left(T s^{2}+T p^{2}+T s c^{2}\right) \\
& \text { Where } \quad: \mathrm{Ta}=\text { Amplifier rise } / \text { fall time } \\
& \mathrm{Tm}=\text { Measured rise } / \text { fall time } \\
& \mathrm{Ts}=\text { Input signal rise } / \text { fall time } \\
& \mathrm{Tp}=\text { Probe effect on rise } / \text { fall time }=2.2 \times \mathrm{RI} \times \mathrm{Cp} \\
& \mathrm{RI}
\end{aligned}=\text { Amplifier output resistance }(\text { ohm }) .
$$

Tsc= Scope rise $/$ fall time $=0.35 /$ Scope bandwidth $(\mathrm{MHz})$

### 3.4 Power Supply

| Input Voltage | $100-240$ VAC $\pm 10 \%$ |
| :---: | :---: |
| Frequency | $50-60 \mathrm{~Hz} \pm 3 \mathrm{~Hz}$ |
| Power Consumption (Max.) <br> (Typical) | 70W 100 - 240VAC, 1.5A <br> Condition: <br> Input voltage:100-240VAC <br> Signal: No. 13 (1024x768(85Hz), (All white)) <br> Contrast: Max, Brightness: Max, <br> H/V size: full scan <br> Others: default position <br> 65W @ 120VAC /60Hz <br> 64W @ 230VAC /50Hz <br> Condition: <br> Signal: No. 13 (1024x768(85Hz), (All white)) <br> Contrast: Max, Brightness: Cutoff, <br> H/V size: preset <br> Others: default position |
| AC leakage current | Except Japan $\leq 3.5 \mathrm{~mA}(254 \mathrm{~V})$, Japan $\leq 0.2 \mathrm{~mA}(100 \mathrm{~V})$ |
| Inrush current | $\leq 42 \mathrm{~A} 0$-peak at 240 VAC on cold starting <br> (or $\leq 30 \mathrm{Arms}$ (half cycle) at 240VAC on cold starting) <br> $\leq 100 \mathrm{~A} 0$-peak at 240VAC on hot starting <br> (or $\leq 70 \mathrm{Arms}$ (half cycle) at 240VAC on hot starting) |

### 3.5 Power Saving

|  | H-sync | V-sync | Video | Power <br> Consumption | Recovery <br> Time | LED <br> Indicator |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ON Mode | On | On | Active | 70W (Max.) | - | Green |
| Off <br> Mode | Off | On | Blank |  |  |  |
|  | On | Off | Blank | $\leq 5 \mathrm{~W}$ | $3-5 \mathrm{sec}$ | Orange |
|  | Off | Off | Blank |  |  |  |

### 3.6 Degaussing

| Auto Degaussing | The monitor has an automatic degaussing function <br> which activates when the unit is turned on. |
| :--- | :--- |
| Manual Degaussing | This activates degaussing at the user's discretion after <br> the unit is operating |

The Monitor requires minimum 15 minutes after last degauss operation for full degauss capability.
4. Functions
4.1 Display Part
4.1.1 Front Controls

a : POWER SWITCH
b: POWER INDICATOR
c: EXIT BUTTON
d : ITEM SELECT BUTTONS
e : FUNCTION ADJUST BUTTONS
f: SELECT \& SB Mode BUTTON
g : RESET BUTTON
(While OSM is closed, User can change "Super Bright Mode" by pressing "SELECT" key.)
"Super Bright Mode" is enable to display brighter picture than "Normal Mode" by increasing video gain. )

### 4.1.2.1 OSM Menu

Tab 1


Tab 2


Tab 3


Tab 4


Tab 5


Tab 6


Tab 6 (OSM Position)


Tab 6 (OSM Lock)



Tab 6 (Language)


Tab 6 (OSM Turn off)


Tab 6 (IPM OFF Mode)


Tab 6 Factory Preset


Tab 7 (URL indication)


Tab 7 (Display Mode)


Tab 7 (Monitor info.)


Tab 7 (Refresh Notifier)


Refresh Notifier

```
    REFRESH RATE LOWER
    THAN RECOMMENDED
    REFER TO
    USER'S MANUAL FOR
    MORE INFORMATION.
    PRESS EXIT TO CLEAR
```

Item Reset


Tab Reset


Factory Preset


Others

diagnosis
INPUT CHECK H:OFF Y:ON


POWER SAYE

PLEASE CHANGE
SIGNAL TIMING
4.1.2.2 OSM Item Variability \& Default Position.

| Tab | Item |  | Default | Item | Push"+" | Push"-" |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | Brightness | 0-100\% | Adjusted | Yes | Up | Down |
|  | Contrast | 0-100\% | 100\% | Yes | Up | Down |
|  | Degauss | - | - | - | Operate | - |
| 2 | Left/Right (H. Posi) | 0-100\% | Adjusted | Yes | Right | Left |
|  | Down/Up (V. Posi) | 0-100\% | Adjusted | Yes | Up | Down |
|  | Narrow/Wide (H. Size) | 0-100\% | Adjusted | Yes | Large | Small |
|  | Short/Tall (V. Size) | 0-100\% | Adjusted | Yes | Large | Small |
| 3 | Color Number | 1 (9300K) | 1 (9300K) | Yes | - | - |
|  |  | 2 (8200K) |  | Yes | - | - |
|  |  | 3 (7500K) |  | Yes | - | - |
|  |  | sRGB |  | Yes | - | - |
|  |  | 5 (5000K) |  | Yes | - | - |
|  | Color Temperature | 5000K-9300K | 9300K | Yes | High | Low |
|  | R/G/B gain control | 0-100\% | Adjusted | Yes | Up | Down |
| 4 | In/Out (Side_Pin) | 0-100\% | Adjusted | Yes | , | $\square$ |
|  | Left/Right(Side Pin Balance) | 0-100\% | Adjusted | Yes |  |  |
|  | Tilt (Parallelogram) | 0-100\% | Adjusted | Yes | $\Gamma$ | $\square$ |
|  | Align (Trapezoidal) | 0-100\% | Adjusted | Yes | $\square$ | $\Gamma$ |
|  | Rotate | 0-100\% | Adjusted | Yes | $\square$ | - |
| 5 | Moire Canceler (Hor) | 0-100\% | 0\% | Yes | Increase | Decrease |
| 6 | Language | English / <br> German / <br> French / <br> Spanish / <br> Italian / <br> Japanese | English | No | - | - |
|  | OSM Position | 5 position | Center | Yes | Cursor move to Left/Right |  |
|  | OSM Turn off | 5-120 sec | 45 sec | Yes | Turn off Time shorter | Turn off Time longer |
|  | OSM Lock | OFF/ON | OFF | No | Lock on: "Select" + "+"key |  |
|  | IPM OFF Mode | Enable/ Disable | 1 (Enable) | No | Cursor move to Left/Right |  |
|  | Factory Preset | - | - | - | All Reset | No operate |
| 7 | URL indication | WWW.NECMITSUBISHI.COM |  |  |  |  |
|  | Display Mode | FH : Horizontal Frequency \& Polarity FV : Vertical Frequency \& Polarity |  |  |  |  |
|  | Monitor Info. | Mitsubishi Brand:"DPLUS74SB" \& Serial Number |  |  |  |  |
|  | Refresh Notifier | OFF/ON | OFF | Yes | Cursor move to Left/Right |  |
| others | Super Bright Mode | OFF/ON | OFF | No | Can switch "OFF/ON" by "SERECT" key |  |

* Default show factory shipping condition.
*The detail function of OSM is written at "2002 model OSM specification".


### 4.1.3 Back Panel

a: AC POWER CONNECTOR (3P IEC Plug)
b: SIGNAL INPUT CONNECTOR pig-tail type (D-SUB 15P)
Signal Cable: Length:1800 $\pm 50 \mathrm{~mm}$, Color: Hazegray (NEC\#8508)


### 4.1.4 Connector Pin Assignment

1) Signal Input Connector (mini D-sub 15P pig-tail cable)

| Pin | Signal |
| :---: | :---: |
| 1 | Red-video |
| 2 | Green-video |
| 3 | Blue-video |
| 4 | Gnd |
| 5 | DDC Gnd |
| 6 | Red Gnd |
| 7 | Green Gnd |
| 8 | Blue Gnd |
| 9 | DDC +5V |
| 10 | Sync Gnd |
| 11 | Gnd |
| 12 | Serial data |
| 13 | H-sync or Composite sync |
| 14 | V-sync |
| 15 | Serial clock |



Signal Cable Connector

### 4.1.5 DDC (Display Data Channel) Functions

VESA DDC 2B (EDID data only), (Support 9 pin - 5V)
VESA DDC/CI (The details is written at "DDC/CI Command \& VCP for NPG design model" )

### 4.1.6 Preset Timing

Factory-presets: 13 (See Appendix 1 for detail timing parameters.)
(Signal Nos.3,7,10,13 are adjustment Signals and Signal Nos.2, 4, 5, 6, 8, 9, 11, 12 are rough adjustment Signals.)
User-presets : 7
Preset Timing Discrimination

| Horizontal Frequency | $\geq 1 \mathrm{kHz}$ |
| :--- | :--- |
| Vertical Frequency | $\geq 1 \mathrm{~Hz}$ |
| Sync Signal Polarity | H or V-sync signal polarity is different |

* The monitor is able to discriminate input signals by at least one of above parameters.


### 4.1.7 Self Diagnosis Function

Monitor show the abnormal condition by Blinking LED.

| Contents of Information | LED Blink |
| :---: | :---: |
| X-ray protector operate | $\bigcirc \bigcirc$ |
| Beam protector circuit operate | $\mathrm{OO} \longrightarrow$ |
| High voltage circuit no operate | $\bigcirc \bigcirc \bigcirc \bigcirc \bigcirc \bigcirc$ |
| High voltage value is abnormal | $\bigcirc \bigcirc \bigcirc \bigcirc$ |
| Oscillation circuit no operate | $\bigcirc \bigcirc \bigcirc \bigcirc \bigcirc \bigcirc$ |
| Internal I2C bus line is abnormal | $\bigcirc \bigcirc \bigcirc \bigcirc \bigcirc \bigcirc \bigcirc \bigcirc \bigcirc \bigcirc$ |
| No H/V sync | Turn on orange LED continually |

Notes: ○ LED off (0.5sec)
$\bigcirc$ LED orange on ( 0.5 sec ) $\bigcirc$ LED orange on ( 2 sec )
"Blinking LED" is repeated until the monitor is turned off.

## 5. Display Quality

### 5.1 Basic Test Conditions

| AC Voltage | 120VAC 60 Hz or 220 VAC 50 Hz |
| :--- | :--- |
| Video Signal | No. $13,1024 \times 768(85 \mathrm{~Hz})(\mathrm{fH}=68.7 \mathrm{kHz} \mathrm{fV}=85 \mathrm{~Hz})$ <br> Video signal $0.70 \pm 0.01 \mathrm{Vp}-\mathrm{p}$ |
| Picture | Reverse cross hatch pattern |$|$| More than 30 min . with full white picture |  |
| :--- | :--- |
| Temperature | $20-25$ degree C |
| Relative Humidity | $40-80 \%$ |
| Magnetic Field | $\mathrm{BH}=0.000 \mathrm{mT}, \mathrm{BV}=0.040 \mathrm{mT}$ (Northern Hemisphere) <br> BH=0.000mT, BV=-0.040mT (Southern Hemisphere) |
| Contrast \& Brightness | Contrast maximum and Brightness default position |
| Display Size | $315 \times 236 \mathrm{~mm}$ for 4:3 aspect ratio |
| Ambient light | $200 \pm 50 \mathrm{~lx}$ |
| Luminance Meter | Minolta CA100 or Equivalent |

If no description, the test below are applied under the Basic Test Condition.
Unless specified, the monitor is set at the factory default setting.

### 5.2 Picture Size and Position

| Adjustment Signal: <br> Signal No.3, 7, 10, 13 | Size <br> Position | Horizontal : $315 \mathrm{~mm} \pm 3.0 \mathrm{~mm}$ <br> Vertical $: 236 \mathrm{~mm} \pm 3.0 \mathrm{~mm}$ <br> Horizontal : \| XLef $\mathrm{t}-$ Xright $\mid \leq 3.0 \mathrm{~mm}$ <br> Vertical $\quad: \mid$ XTop - XBottom $\mid \leq 3.0 \mathrm{~mm}$ <br> The picture should adjust underscan. |
| :---: | :---: | :---: |
| Rough Adjustment Signal: <br> Signal No.2, 4, 5, 6, 8, 9, 11, 12 | Size <br> Position | Horizontal : $315 \mathrm{~mm} \pm 6.0 \mathrm{~mm}$ <br> Vertical : $236 \mathrm{~mm} \pm 6.0 \mathrm{~mm}$ <br> Horizontal : \|XLeft - XRight $\mid \leq 6.0 \mathrm{~mm}$ <br> Vertical $\quad:\|X T o p-X B o t t o m ~\| \leq 6.0 m m$ <br> The picture should adjust underscan. |
| Signal No. 1 (VGA350) | Adjust the vertical size to maximum. |  |
| Figure | 236 mm |  |

### 5.2.1 Size and Position Control Ranges

| Signal No.2 to 13 <br> Size Control Ranges | The horizontal and vertical size control should be <br> controllable to "FullScan" at the maximum position. <br> * Except MAC Signal (Signal No. 4, 9) |
| :--- | :--- |
| Signal No. 1 to 13 <br> Position Control Ranges | Image position can be controlled to the center <br> position of the bezel opening. |

### 5.3 Luminance (Brightness)

Signal No. 13 (1024*768@85Hz)

| 5.3.1 Luminance at CRT center (Full white pattern) | Contrast : Max. <br> Brightness : Set to cut off $76 \mathrm{~cd} / \mathrm{m}^{2} \leq \text { Full White } \leq 110 \mathrm{~cd} / \mathrm{m}^{2}$ <br> (at 9300K +8 M.P.C.D.) <br> * When Brightness control to MAX, the luminance should be over $90 \mathrm{~cd} / \mathrm{m}^{2}$ |
| :---: | :---: |
| 5.3.2 Luminance at CRT center (Window pattern) (H:33\%,V:33\%) | ```Contrast : Max. Brightness : Set to cut off \(120 \mathrm{~cd} / \mathrm{m}^{2} \leq\) Window pattern \(\leq 160 \mathrm{~cd} / \mathrm{m}^{2}\) (at \(9300 \mathrm{~K}+8\) M.P.C.D.) SB Mode : ON Contrast: :Max. Brightness :Set to cut off Window pattern \(=300 \mathrm{~cd} / \mathrm{m}^{2}+30 /-0\) (at \(9300 \mathrm{~K}+8\) M.P.C.D.)``` |
| 5.3.3 <br> Luminance Variation <br> (Full white pattern) <br> Contrast : MAX <br> Brightness : <br> Adjust to $90 \mathrm{~cd} / \mathrm{m}^{2}$ | $125 \% \geq \frac{B i}{A} \times 100 \geq 75 \% \begin{array}{lll} \text { B1 } & & \text { B4 } \\ & \text { A } & \\ \text { B2 } & & \text { B3 } \\ \hline \end{array}$ |
| 5.3.4 <br> Back Raster <br> Luminance <br> (Full black pattern) | Brightness : default position <br> Raster $\leq 0.20 \mathrm{~cd} / \mathrm{m}^{2}$ <br> Raster must not visible at minimum Brightness control. <br> Brightness : MAX position <br> $2.0 \mathrm{~cd} / \mathrm{m}^{2} \leq$ Raster $\leq 8.0 \mathrm{~cd} / \mathrm{m}^{2}$ |

### 5.4 Color

Signal No. 13 (1024*768@85Hz)

| 5.4.1 Color Temperature (Window pattern) (H:33\%,V:33\%) <br> Contrast: Max. Brightness : Cut off | Color-1: $9300 \mathrm{~K}+8$ M.P.C.D.Xref $=0.283 \pm 0.015$Yref $=0.297 \pm 0.015$ |  |  |
| :---: | :---: | :---: | :---: |
|  | $\begin{aligned} \text { Color-2: } 8200 \mathrm{~K} \\ \mathrm{X}=0.290 \pm 0.015 \\ \mathrm{Y}=0.313 \pm 0.015 \end{aligned}$ |  |  |
|  | $\begin{aligned} & \text { Color-3: } 7500 \mathrm{~K} \\ & \mathrm{X}=0.300 \pm 0.015 \\ & \mathrm{Y}=0.315 \pm 0.015 \end{aligned}$ |  |  |
|  | $\begin{gathered} \text { Color-4: sRGB (Luminance: } \left.80+20 /-10 \mathrm{~cd} / \mathrm{m}^{2}\right) \\ \mathrm{X}=0.313 \pm 0.015 \\ \mathrm{Y}=0.329 \pm 0.015 \end{gathered}$ |  |  |
|  | $\begin{aligned} \hline \text { Color-5: } 5000 \mathrm{~K} \\ \mathrm{X}=0.345 \pm 0.015 \\ \mathrm{Y}=0.359 \pm 0.015 \\ \hline \end{aligned}$ |  |  |
| 5.4.2 Color Tracking of Contrast control (Window pattern) ( $\mathrm{H}: 33 \%, \mathrm{~V}: 33 \%$ ) | $\begin{aligned} & X=\text { Xref } \pm 0.020 \\ & Y=\text { Yref } \pm 0.020 \end{aligned}$ <br> Color setting : 9300K Contrast Control: from $20 \mathrm{~cd} / \mathrm{m}^{2}$ to MAX. Brightness : Cut off |  |  |
| 5.4.3 Color Tracking of brightness control (Window pattern) ( $\mathrm{H}: 33 \%, \mathrm{~V}: 33 \%$ ) | $\begin{aligned} & X=\text { Xref } \pm 0.020 \\ & Y=\text { Yref } \pm 0.020 \end{aligned}$ <br> Color setting : 9300K <br> Contrast Control: $50 \mathrm{~cd} / \mathrm{m}^{2}$ (at Brightness cut off) Brightness : from Max. to Min. |  |  |
| 5.4.4 sRGB color quality (Full white pattern) |  |  |  |
| 5.4.2 White Uniformity (Full white pattern) | White color temperature(x,y) at $\mathrm{B} 1, \mathrm{~B} 2, \mathrm{~B} 3, \mathrm{~B} 4$ is as follows. |  |  |
| Contrast : MAX Brightness : Adjust to $90 \mathrm{~cd} / \mathrm{m}^{2}$ | $\begin{aligned} & \text { A(x ref, y ref) } \\ & x \leq x \text { ref } \pm 0.015 \\ & y \leq y \text { ref } \pm 0.015 \end{aligned}$ | B2 | $\begin{aligned} & \text { B4 } \\ & \text { B3 } \end{aligned}$ |


5.6 Linearity

| Linearity | $\mathrm{H}: \leq 20 \%(30-43 \mathrm{k}), \leq 12 \%(43-55 \mathrm{k}), \leq 10 \%(55-70 \mathrm{k})$, adjacent: $\leq 7 \%$ |
| :--- | :--- |
|  | $\mathrm{~V}: \leq 10 \%$, adjacent: $\leq 7 \%$ |

* at preset timings
* With Green-Crosshatch (17 lines horizontally by 13 lines vertically ) applied.
* The formula used to calculate linearity is:
$\frac{X \max -X \min }{(X \max +X \min ) / 2} \times 100 \% \quad \frac{Y \max -Y \min }{(Y \max +Y \min ) / 2} \times 100 \%$



### 5.7 Misconvergence

| Misconvergence | Zone $\mathrm{A}: \mathrm{X}, \mathrm{Y} \leq 0.25 \mathrm{~mm}$ within the 236 mm diameter circle |
| :--- | :--- |
|  | Zone $\mathrm{B}: \mathrm{X}, \mathrm{Y} \leq 0.35 \mathrm{~mm}$ within $315 \mathrm{~mm} \times 236 \mathrm{~mm}$ |

* With White Crosshatch (17 lines horizontally by 13 lines vertically ) applied.
* Zone A is a circular area with 236 mm diameter at the center.
* Zone $B$ is a rectangular area ( $315 \mathrm{~mm} \times 236 \mathrm{~mm}$ ) outside of the Zone A.
* Use worst case horizontal/vertical misconvergence between any two primary colors.




### 5.9 Halo



### 5.10 Raster Regulation

| Raster Size |  |
| :--- | :--- |
| Regulation |  |
| (Full White pattern) | Judgment: <br> 1.The picture size should not vary more than following spec. <br> by luminance change from $100 \mathrm{~cd} / \mathrm{m}^{2}$ to $30 \mathrm{~cd} / \mathrm{m}^{2}$. <br> 2. The picture size should not vary more than following spec. <br> by input voltage change in $90-132 \mathrm{VAC}$ and 198-264VAC. <br> Size Change Spec. <br> Signal No.13 <br> $\frac{\|H 1-H 2\|}{H 2} \leq 0.5 \%$ |
| $\frac{\|V 1-V 2\|}{V 2} \leq 0.5 \%$ |  |

## 6. CRT Screen and Faceplate Blemish Limits

### 6.1 CRT Face Plate Defect

### 6.1.1 Inspection Condition

(1) In the operating condition, observe the defect on the screen under following condition.
$9,300 \mathrm{~K}(x=0.283, y=0.297)$ white raster or the element monochrome raster which its brightness is $34 \mathrm{~cd} / \mathrm{m}^{2}(10 \mathrm{ft} \cdot \mathrm{L})$ on the screen center surrounding light is about 10 Lux.
(2) In the non-operating condition, observe the defect of the screen under light of about 200 Lux, measured at the faceplate.
(3) Inspection shall be made more than 45 cm away from the screen.
(4) Observe the screen on white raster and each monochrome color of red, green and blue.

### 6.1.2 Division of Zone

A screen is divided into following 2 zones.
zone A : Area inside the rectangle that its size measures the followings in the center of screen.

$$
\mathrm{H}: 300 \mathrm{~mm}, \mathrm{~V}: 225 \mathrm{~mm}
$$

zone $B$ : Area outside the above rectangle

### 6.1.3 Limits

(1) CRT face defect
(a) Distance (minimum distance )

(b) Average diameter

Turn of $\frac{a+b}{2} \quad$ (a: length, b : width)
b

(c) Limit

* Dark spot, Blocked aperture

| Average diameter (mm) | A | $B$ | $A+B$ | minimum distance |
| :---: | :---: | :---: | :---: | :---: |
| $0.51 \sim$ | 0 | 0 | 0 | - |
| $0.31 \sim 0.50$ | 0 | 0 | 0 | - |
| $0.15 \sim 0.30$ | 6 (note 1) | 6 (note 1) | 10 (note 1) | 10 mm |

* Discoloration, stain, Missing phosphor, etc.

| Average diameter (mm) | A | B | A + B | minimum distance |
| :---: | :---: | :---: | :---: | :---: |
| $0.51 \sim 0.75$ | 0 | 1 | - | 20 mm |
| $0.15 \sim 0.50$ | 2 | 3 | - | 20 mm |

Note 1 : No missing spot larger than specified are allowed in Zone A.
Note 2 : The spec applies to each color.
(2) Face plate defect
(a) Blisters, opaque spots and elongated closed blisters

| Average diameter <br> $(\mathrm{mm}) ~ \# 1$ | Allowable number (pcs) |  |  | Minimum Separation <br> $(\mathrm{mm})$ |
| :---: | :---: | :---: | :---: | :---: |
|  | Zone A | Zone B | Total |  |
| $0.76 \sim$ | 0 | 0 | 0 | 30 |
| $0.51 \sim 0.75$ | 0 | 1 | 1 |  |
| $0.26 \sim 0.50$ | 2 | 3 | 5 | $\# 2$ |
| $0.11 \sim 0.25$ | - | - | - |  |

\#1: Mean diameter shall be either one of the following values, which is smaller. $(a+b) / 2$ or $a / 20+2 b$ ( $a$ : length, $b$ : width)
\#2:Maximum 5 pcs. In area of $\phi 10 \mathrm{~mm}$.
(b) Scratch

| Width (mm) | Allowable Length (mm) |
| :---: | :---: |
| $0.16 \sim$ | rejected |
| $0.11 \sim 0.15$ | 3 |
| $0.06 \sim 0.10$ | 26 |
| $\sim 0.05$ | unlimited |

(c) Other glass defects

Flaw, crack and lack cannot be distinguish easily by naked eye.
Iron rust conforms to limited sample.

### 6.2 AR-film's Surface Defect

### 6.2.1 Inspection Condition

(1) Put a valve on an inspective stand and Illuminate it from the top with white fluorescent light.
(2) Valve surface Illuminance is more than 1000Lux and less than 1000Lux.
(3) Observe from distance of 40 cm from surface, disregard flaws which can not be distinguished from this distance.

### 6.2.2 Division of Zone

A screen is divided into following 3 zones.
zone A: Area inside the rectangle that its size measures the followings in the center of screen.

$$
\mathrm{H}: 300 \mathrm{~mm}, \mathrm{~V}: 225 \mathrm{~mm}
$$

zone B: Area outside zone A and inside the fluorescent surface edge.
zone C: Area outside the fluorescent surface edge.


### 6.2.3 Limits

(1) Scratch

| Width (mm) | Allowable Length (mm)(Zone A + Zone B) |
| :---: | :---: |
| $0.16 \sim$ | reject |
| $0.11 \sim 0.15$ | 13 |
| $0.06 \sim 0.10$ | 26 |
| $\sim 0.05$ | unlimited |

NOTE 1 : Even though width of scratch is more than 0.16 mm , regard scratch whose contrast is weak extremely as stain and apply standard of 6.2.3(2).

NOTE 2 : Do not recognize flaws which injures goods prices though it is not especially stipulated as for zone $C$.
(2) Opaque flaws (ex. Stain) and coating peeling

Do not apply the following standard to zone C.
Classify flaws by contrast and judge it by size every the contrast.

## Definition of a contrast

High contrast : The foreign substance which shuts off light from fluorescence surface.
Middle contrast: A semitransparent foreign substance and stain.
(ex. coating material which has been changed)
Low contrast: stain and dust which do not reflect light from fluorescence surface and can be distinguished by its appearance.

Note : Ignore the light spot with no interference color.
(However, Non of them with its size in excess of 3.75 mm is acceptable, that damages the product quality.)

Standard

| Average diameter classified by a contrast <br> $($ Note 1) $(\mathrm{mm})$ |  |  | Allowable number |  | Allowable Length <br> $(\mathrm{mm})$ |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| High contrast | Middle <br> contrast | Low contrast | zone A | zone B |  |  |
| $\sim 0.10$ | $\sim 0.20$ | $\sim 0.50$ | Ignore | Ignore |  |  |
| $0.11 \sim 0.25$ | $0.21 \sim 0.50$ | $0.51 \sim 1.25$ | $2[4]$ | $4[5]$ | 20 |  |
| $0.26 \sim 0.50$ | $0.51 \sim 1.00$ | $1.26 \sim 2.50$ | $1[4]$ | $2[4]$ | 40 |  |
| $0.51 \sim 0.75$ | $1.01 \sim 1.50$ | $2.51 \sim 3.75$ | $0[4]$ | $1[4]$ | 80 |  |

Values inside [ ] represent acceptable number in low contrast.
See the table in the next page for total defect number, which is acceptable in low contrast.
NOTE 1 : Convert $(\mathrm{a}+\mathrm{b}) / 2$ or $\mathrm{a} / 20+2 \mathrm{~b}$ small value into average diameter.
(a: length, b: width)

| total number of a low contrast flaws | zone A | zone B |
| :---: | :---: | :---: |
| Standard classified by zones | 6 | 8 |
| Total ( zone A + zone B ) | 10 |  |

NOTE 1 : Acceptable interval shall be larger one in the case that defects have different interval.
NOTE 2 : There is no standard regarding zone C. Therefore, no defect is accepted that may deteriorate the value of products. Defect level by consultation. Discuss is necessary.
NOTE 3 Tolerance of defect size is approx. 10\%.

## 7. Inspection of PLUG \& PLAY Communication and OSM "MONITOR INFORMATION" for Model Name/ Serial Number

### 7.1 A System Construction

This system should be connected as shown below.


### 7.2 Input Signal

Horizontal sync frequency: Not specified.
Vertical sync frequency: Not specified.

### 7.3 Programs Required

CN8701.EXE
DP74SB.BAT
DP74SB.TXT

### 7.4 Inspection Procedures

a. Power on pressing "-" button.
b. Copy the above-mentioned programs in an adequate directory.
c. Set up the MO-DOS mode. (DOS Prompt of Windows95/98 is also acceptable.)
d. Execute the DP74SB.BAT from the command line.
e. "MONITOR INFO." of the OSM is indicated, and a model name and a serial number are confirmed. When the model name and the serial number are not written in or it differs, $h$ or later is performed.
f. Press the F1 key to start the inspection of DDC1.

As a result of inspection, when EDID data is not written in or it differs, h or later is performed.
g. Press the F2 key to start the inspection of DDC2B.

As a result of inspection, when EDID data is not written in or it differs, h or later is performed..
h. Check the serial number of the set and enter an input of the following code from the keyboard. *08109691 Serial Number* (*+Model Code +3 Spaces + Serial No. + ${ }^{*}$ )

Example: *08109693...2150001YB*
i. Press the Enter key. Then, the EDID data, OSM model name, and the serial number begin to be written in.

j. Display "MONITOR INFO." of the OSM, and confirm that the model name and serial number have been correctly written.


```
    MIDE
            HzO
    MONITOR INFO.
    MODEL:DPLUS74SB
    SERIAL NUMBER:
        XXXXXXXXXXX
```

k. Press the F1 key to start the inspection of DDC1.

After the completion of inspection, the contents of EDID are displayed. If an error should occur, the related error message will be displayed in the bottom area of the screen. Refer to Paragraph 7.5 in regard to the meaning of this error message.
I. Press the F2 key to start the inspection of DDC2B.

After the completion of inspection, the contents of EDID are displayed. If an error should occur, the related error message will be displayed in the bottom area of the screen. Refer to Paragraph 7.5 in regard to the meaning of this error message.


### 7.5 Error Messages

- IIC Communication Error

Communication disabled

- EDID Check Sum Error

Entry of false EDID

- DDC1 Does Not Find Head Data

DDC1 Communication disabled

- DDC2 Does Not Find Head Data

DDC2 Communication disabled

### 7.6 EDID Data File

The EDID data file text is shown below. When you write or inspect EDID for this monitor, the following table can be used.

File name : DP74SB.TXT

|  | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 00 | 00 | FF | FF | FF | FF | FF | FF | 00 | 34 | AC | 23 | 46 | 01 | 01 | 01 | 01 |
| 10 | $\begin{aligned} & 30 \\ & { }_{*} \end{aligned}$ | $\begin{aligned} & \hline 0 \mathrm{~B} \\ & { }^{*} 2 \end{aligned}$ | 01 | 03 | 0C | 21 | 18 | 78 | EA | 67 | A8 | A0 | 56 | 47 | 99 | 26 |
| 20 | 11 | 48 | 4C | FF | FE | 00 | 31 | 59 | 45 | 59 | 61 | 59 | 71 | 4F | 81 | 40 |
| 30 | 81 | 80 | 01 | 01 | 01 | 01 | EA | 24 | 00 | 60 | 41 | 00 | 28 | 30 | 30 | 60 |
| 40 | 13 | 00 | 3B | EC | 10 | 00 | 00 | 1E | 00 | 00 | 00 | FD | 00 | 32 | 78 | 1 E |
| 50 | 46 | OC | 00 | OA | 20 | 20 | 20 | 20 | 20 | 20 | 00 | 00 | 00 | FC | 00 | 44 |
| 60 | 50 | 6C | 75 | 73 | 37 | 34 | 53 | 42 | OA | 20 | 20 | 20 | 00 | 00 | 00 | FF |
| 70 | 00 | $\begin{aligned} & \hline 31 \\ & * 3 \\ & \hline \end{aligned}$ | $\begin{aligned} & \hline \text { 5A } \\ & * 3 \end{aligned}$ | $\begin{aligned} & \hline 30 \\ & \text { *3 } \end{aligned}$ | $\begin{aligned} & \hline 30 \\ & * 3 \end{aligned}$ | $\begin{aligned} & \hline 30 \\ & * 3 \end{aligned}$ | $\begin{array}{\|l\|} \hline 30 \\ * 3 \\ \hline \end{array}$ | $\begin{array}{\|l\|} \hline 31 \\ * 3 \\ \hline \end{array}$ | $\begin{aligned} & \hline 59 \\ & * 3 \end{aligned}$ | $\begin{array}{\|l\|} \hline 41 \\ * 3 \\ \hline \end{array}$ | $$ | $\begin{aligned} & 20 \\ & * 3 \end{aligned}$ | $\begin{array}{r} 20 \\ \times 3 \\ \hline \end{array}$ | $\begin{aligned} & 20 \\ & * 3 \end{aligned}$ | 00 | 11 $*$ 4 |

Table 7.6 Data list
*1 : address 10h
*2 : address 11h
*3 : address 71h~7Dh
*4 : address 7Fh

Manufactured month x 4
Manufactured year - 1990
Input serial number (ASCII code)
Add OAh after serial number.
Add 20th remaining address.
Checksum. The sum of entire 128byte shall be equal to 00 h .

Appendix 1 Preset Timing Chart


Preset Signal

| No | Signal Name | $\left\|\begin{array}{c} \text { Clock } \\ (\mathrm{MHz}) \end{array}\right\|$ | $\begin{gathered} \mathrm{Fh} \\ (\mathrm{kHz}) \end{gathered}$ | $\begin{gathered} \mathrm{Fv} \\ (\mathrm{~Hz}) \end{gathered}$ | $\begin{array}{\|c\|} \hline \text { Th } \\ \text { (uSec) } \\ \text { (dot) } \end{array}$ | Tsh (uSec) (dot) | $\begin{array}{\|c\|} \hline \text { Tfh } \\ \text { (uSec) } \\ \text { (dot) } \\ \hline \end{array}$ | $\begin{gathered} \text { Tbh } \\ (\mathrm{uSec}) \\ (\mathrm{dot}) \end{gathered}$ | $\begin{gathered} \text { Tdh } \\ \text { (uSec) } \\ \text { (dot) } \\ \hline \end{gathered}$ | $\begin{array}{\|c\|} \hline \text { Tv } \\ (\mathrm{mSec}) \\ (\text { line }) \\ \hline \end{array}$ | $\begin{array}{\|c\|} \hline \text { Tsv } \\ (\mathrm{mSec}) \\ \text { (line) } \end{array}$ | $\begin{gathered} \text { Tfv } \\ (\mathrm{mSec}) \\ (\text { line }) \end{gathered}$ | $\begin{gathered} \text { Tbv } \\ (\mathrm{mSec}) \\ (\text { line }) \end{gathered}$ | $\left\lvert\, \begin{gathered} \mathrm{Tdv} \\ (\mathrm{mSec}) \\ (\text { line }) \end{gathered}\right.$ | Hs | Vs |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | $\begin{aligned} & \text { VGA } \\ & 720^{*} 350(70) \end{aligned}$ | 28.322 | 31.469 | 70.087 | $\begin{gathered} 31.777 \\ (900) \end{gathered}$ | $\begin{aligned} & 3.813 \\ & (108) \end{aligned}$ | $\begin{gathered} 0.636 \\ (18) \end{gathered}$ | $\begin{gathered} 1.907 \\ (54) \end{gathered}$ | $\begin{gathered} 25.422 \\ (720) \end{gathered}$ | $\begin{gathered} 14.268 \\ (449) \end{gathered}$ | $0.064$ <br> (2) | $\begin{gathered} 1.176 \\ (37) \end{gathered}$ | $\begin{gathered} 1.907 \\ (60) \end{gathered}$ | $\begin{gathered} 11.122 \\ (350) \end{gathered}$ | + | - |
| 2 | $\begin{aligned} & \text { VGA } \\ & 720^{*} 400(70) \end{aligned}$ | 28.322 | 31.469 | 70.087 | $\begin{aligned} & 31.777 \\ & (900) \end{aligned}$ | $\begin{aligned} & 3.813 \\ & (108) \end{aligned}$ | $\begin{gathered} 0.636 \\ (18) \end{gathered}$ | $\begin{gathered} 1.907 \\ (54) \end{gathered}$ | $\begin{gathered} 25.422 \\ (720) \end{gathered}$ | $\begin{gathered} 14.268 \\ (449) \end{gathered}$ | $0.064$ <br> (2) | $\begin{gathered} 0.381 \\ (12) \end{gathered}$ | $\begin{gathered} 1.112 \\ (35) \end{gathered}$ | $\begin{gathered} 12.711 \\ (400) \end{gathered}$ | - | + |
| 3 | $\begin{aligned} & \text { VGA } \\ & 640^{*} 480(60) \\ & \hline \end{aligned}$ | 25.175 | 31.469 | 59.940 | $\begin{gathered} 31.778 \\ (800) \end{gathered}$ | $\begin{gathered} 3.813 \\ (96) \\ \hline \end{gathered}$ | $\begin{gathered} 0.636 \\ (16) \end{gathered}$ | $\begin{gathered} 1.907 \\ (48) \\ \hline \end{gathered}$ | $\begin{gathered} 25.422 \\ (640) \end{gathered}$ | $\begin{gathered} 16.683 \\ (525) \\ \hline \end{gathered}$ | $0.064$ <br> (2) | $\begin{gathered} 0.318 \\ (10) \end{gathered}$ | $\begin{gathered} 1.049 \\ (33) \\ \hline \end{gathered}$ | $\begin{gathered} 15.253 \\ (480) \end{gathered}$ | - |  |
| 4 | Mac640*480 | 30.240 | 35.000 | 66.667 | $\begin{gathered} 28.571 \\ (864) \\ \hline \end{gathered}$ | $\begin{gathered} 2.116 \\ (64) \\ \hline \end{gathered}$ | $\begin{gathered} 2.116 \\ (64) \\ \hline \end{gathered}$ | $\begin{gathered} 3.175 \\ (96) \end{gathered}$ | $\begin{gathered} 21.164 \\ (640) \end{gathered}$ | $\begin{gathered} 15.000 \\ (525) \\ \hline \end{gathered}$ | $\begin{gathered} 0.086 \\ (3) \end{gathered}$ | $\begin{gathered} 0.086 \\ (3) \end{gathered}$ | $\begin{gathered} 1.114 \\ (39) \\ \hline \end{gathered}$ | $\begin{gathered} 13.714 \\ (480) \end{gathered}$ | - |  |
| 5 | $\begin{aligned} & \text { VESA } \\ & 640 * 480(75) \\ & \hline \end{aligned}$ | 31.500 | 37.500 | 75.000 | $\begin{array}{\|c} 26.667 \\ (840) \\ \hline \end{array}$ | $\begin{gathered} 2.032 \\ (64) \end{gathered}$ | $\begin{gathered} 0.508 \\ (16) \end{gathered}$ | $\begin{aligned} & 3.810 \\ & (120) \\ & \hline \end{aligned}$ | $\begin{gathered} 20.317 \\ (640) \\ \hline \end{gathered}$ | $\begin{gathered} 13.333 \\ (500) \\ \hline \end{gathered}$ | $\begin{array}{\|c\|} \hline 0.080 \\ (3) \\ \hline \end{array}$ | $\begin{array}{\|c\|} \hline 0.027 \\ (1) \\ \hline \end{array}$ | $\begin{array}{r} 0.427 \\ (16) \\ \hline \end{array}$ | $\left\lvert\, \begin{gathered} 12.800 \\ (480) \end{gathered}\right.$ | - | - |
| 6 | $\begin{aligned} & \text { VESA } \\ & 800^{*} 600(75) \\ & \hline \end{aligned}$ | 49.500 | 46.875 | 75.000 | $\begin{aligned} & 21.333 \\ & (1056) \end{aligned}$ | $\begin{gathered} 1.616 \\ (80) \end{gathered}$ | $\begin{gathered} 0.323 \\ (16) \end{gathered}$ | $\begin{aligned} & 3.232 \\ & (160) \\ & \hline \end{aligned}$ | $\begin{gathered} 16.162 \\ (800) \\ \hline \end{gathered}$ | $\begin{gathered} 13.333 \\ (625) \\ \hline \end{gathered}$ | $\begin{array}{\|c} 0.064 \\ (3) \\ \hline \end{array}$ | $\begin{gathered} 0.021 \\ (1) \\ \hline \end{gathered}$ | $\begin{gathered} 0.448 \\ (21) \\ \hline \end{gathered}$ | $\begin{gathered} 12.800 \\ (600) \\ \hline \end{gathered}$ | + | + |
| 7 | $640 * 480(85)$ | 36.000 | 43.269 | 85.008 | $\begin{gathered} 23.111 \\ (832) \\ \hline \end{gathered}$ | $\begin{gathered} 1.556 \\ (56) \end{gathered}$ | $\begin{gathered} 1.556 \\ (56) \\ \hline \end{gathered}$ | $\begin{gathered} 2.222 \\ (80) \\ \hline \end{gathered}$ | $\begin{gathered} 17.778 \\ (640) \\ \hline \end{gathered}$ | $\begin{gathered} 11.764 \\ (509) \\ \hline \end{gathered}$ | $\begin{array}{\|c} 0.069 \\ (3) \\ \hline \end{array}$ | $\begin{gathered} 0.023 \\ (1) \\ \hline \end{gathered}$ | $\begin{gathered} 0.578 \\ (25) \\ \hline \end{gathered}$ | $\begin{gathered} 11.093 \\ (480) \\ \hline \end{gathered}$ | - | - |
| 8 | $\begin{array}{\|l\|} \hline \text { VESA } \\ 1024^{\star} 768(60) \\ \hline \end{array}$ | 65.000 | 48.363 | 60.004 | $\begin{aligned} & 20.677 \\ & (1344) \end{aligned}$ | $\begin{aligned} & 2.092 \\ & (136) \\ & \hline \end{aligned}$ | $\begin{array}{\|c} 0.369 \\ (24) \\ \hline \end{array}$ | $\begin{array}{r} 2.462 \\ (160) \\ \hline \end{array}$ | $\begin{array}{r} 15.754 \\ (1024) \\ \hline \end{array}$ | $\begin{aligned} & 16.666 \\ & (806) \\ & \hline \end{aligned}$ | $0.124$ <br> (6) | $\begin{gathered} 0.062 \\ (3) \\ \hline \end{gathered}$ | $\begin{gathered} 0.600 \\ (29) \\ \hline \end{gathered}$ | $\begin{gathered} 15.880 \\ (768) \\ \hline \end{gathered}$ | - | - |
| 9 | MAC832*624 | 57.283 | 49.725 | 74.550 | $\begin{aligned} & 20.111 \\ & (1152) \end{aligned}$ | $\begin{gathered} 1.117 \\ (64) \\ \hline \end{gathered}$ | $\begin{array}{\|c} 0.559 \\ (32) \\ \hline \end{array}$ | $\begin{aligned} & 3.910 \\ & (224) \\ & \hline \end{aligned}$ | $\begin{gathered} 14.524 \\ (832) \end{gathered}$ | $\begin{gathered} 13.414 \\ (667) \\ \hline \end{gathered}$ | $\begin{array}{\|c} 0.060 \\ (3) \\ \hline \end{array}$ | $\begin{gathered} 0.020 \\ (1) \\ \hline \end{gathered}$ | $\begin{gathered} 0.784 \\ (39) \\ \hline \end{gathered}$ | $\begin{gathered} 12.549 \\ (624) \end{gathered}$ | - |  |
| 10 | $\begin{aligned} & \text { VESA } \\ & 800 * 600(85) \\ & \hline \end{aligned}$ | 56.250 | 53.674 | 85.061 | $\begin{array}{\|} 18.631 \\ (1048) \end{array}$ | $\begin{gathered} 1.138 \\ (64) \end{gathered}$ | $\begin{gathered} 0.569 \\ (32) \\ \hline \end{gathered}$ | $\begin{aligned} & 2.702 \\ & (152) \\ & \hline \end{aligned}$ | $\begin{gathered} 14.222 \\ (800) \\ \hline \end{gathered}$ | $\begin{gathered} 11.756 \\ (631) \end{gathered}$ | $\begin{array}{\|c} 0.056 \\ (3) \\ \hline \end{array}$ | $\begin{array}{\|c\|} \hline 0.019 \\ (1) \\ \hline \end{array}$ | $\begin{gathered} 0.503 \\ (27) \\ \hline \end{gathered}$ | $\begin{array}{\|c\|} \hline 11.179 \\ (600) \\ \hline \end{array}$ | + | + |
| 11 | $\begin{array}{\|l\|} \hline \text { VESA } \\ 1024^{\star} 768(75) \\ \hline \end{array}$ | 78.750 | 60.023 | 75.029 | $\begin{aligned} & 16.660 \\ & (1312) \end{aligned}$ | $\begin{gathered} 1.219 \\ (96) \end{gathered}$ | $\begin{array}{\|c} 0.203 \\ (16) \end{array}$ | $\begin{aligned} & 2.235 \\ & (176) \\ & \hline \end{aligned}$ | $\begin{aligned} & 13.003 \\ & (1024) \end{aligned}$ | $\begin{array}{\|c\|} 13.328 \\ (800) \\ \hline \end{array}$ | $\begin{array}{\|c\|} \hline 0.050 \\ (3) \\ \hline \end{array}$ | $\begin{array}{\|c\|} \hline 0.017 \\ (1) \\ \hline \end{array}$ | $\begin{gathered} 0.466 \\ (28) \\ \hline \end{gathered}$ | $\left\lvert\, \begin{gathered} 12.795 \\ (768) \end{gathered}\right.$ | + | + |
| 12 | $\begin{array}{\|l\|} \hline \text { VESA } \\ 1280 * 1024(60) \\ \hline \end{array}$ | 108.00 | 63.981 | 60.020 | $\begin{aligned} & 15.630 \\ & (1688) \end{aligned}$ | $\begin{aligned} & 1.037 \\ & (112) \\ & \hline \end{aligned}$ | $\begin{array}{\|c} 0.444 \\ (48) \\ \hline \end{array}$ | $\begin{array}{r} 2.296 \\ (248) \\ \hline \end{array}$ | $\begin{aligned} & 11.852 \\ & (1280) \\ & \hline \end{aligned}$ | $\begin{aligned} & 16.661 \\ & (1066) \end{aligned}$ | $0.047$ <br> (3) | $\begin{gathered} 0.016 \\ (1) \\ \hline \end{gathered}$ | $\begin{gathered} 0.594 \\ (38) \\ \hline \end{gathered}$ | $\begin{array}{\|l\|} \hline 16.005 \\ (1024) \\ \hline \end{array}$ | + | + |
| 13 | $\begin{aligned} & \text { VESA } \\ & 1024^{*} 768(85) \\ & \hline \end{aligned}$ | 94.500 | 68.677 | 84.997 | $\begin{aligned} & 14.561 \\ & (1376) \end{aligned}$ | $\begin{gathered} 1.016 \\ (96) \end{gathered}$ | $\begin{array}{\|c} 0.508 \\ (48) \end{array}$ | $\begin{aligned} & 2.201 \\ & (208) \\ & \hline \end{aligned}$ | $\begin{aligned} & 10.836 \\ & (1024) \end{aligned}$ | $\begin{gathered} 11.765 \\ (808) \end{gathered}$ | $\begin{gathered} 0.044 \\ (3) \\ \hline \end{gathered}$ | $\begin{array}{c\|} 0.015 \\ (1) \end{array}$ | $\begin{gathered} 0.524 \\ (36) \end{gathered}$ | $\begin{gathered} 11.183 \\ (768) \end{gathered}$ | + | + |

## TROUBLE SHOOTING

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Refer to User's Manual trouble shooting section before using this chart.
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## 1. NO OPERATION, POWER LED FLASH


2. NO OPERATION, POWER LED OFF

3. VIDEO NOISE, UNSYNCHRONOUS

4. NO VIDEO


## 5. NO RASTER


6. TROUBLE IN H. V SYNC

7. POOR PINCUSHION


## CIRCUIT DESCRIPTION

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## 1. Power supply circuit

### 1.1 Outline

This power supply unit uses switching mode technology, and is an off-line mode type unit that provides several different DC outputs. The scanning frequency is available in different values ranging from 31 kHz to 69 kHz . Moreover, it is capable of operating at an AC input voltage of $100 \mathrm{~V} \sim 240 \mathrm{~V}$ and an AC frequency of $50-60 \mathrm{~Hz} \pm 3 \mathrm{~Hz}$.
The block diagram is the functional construction schematics, that shows the major functions of this power supply unit.

### 1.2 Harmonics (OPTION)

L107 is a harmonic choke circuit that reduces the harmonic peak currents, for the purpose of fulfilling the requirement items of IEC 1000-3-2.

### 1.3 EMI

The EMI circuit has a 2-stage construction, with the first stage consisting of the common mode choke unit and one X -capacitor, and the second stage consisting of the common mode choke unit and four Y capacitors.
R101 is the X-capacitor bleed resistor. When the power supply switch is turned OFF, this resistor carries out the emergency charging of the capacitor C101.

The EMI is the circuit that prevents monitor switching noise from being generated, there by minimizing the negative influence on other electronic equipment.

### 1.4 AC rectifier and smoothing capacitor

The AC input is rectified by means of the full-bridge rectifier, that consists of the diodes D101 to D104. The AC voltage is converted into the DC voltage by passing through the next stage, that consists of the smoothing capacitor C105.
TH101 is a NTC thermistor for the power supply at the in-rush current limit.

### 1.5 Degaussing circuit

The degaussing circuit consists of the PTC thermistor TH102, the degaussing coil and relay RL101. The relay is controlled by means of the +12 V control signal coming from the CPU.

### 1.6 Transformer and energy induction

1) When the PWM controls IC KA3842A chip, a driving pulse is generated at the gate of the transistor Q101, and Q101 turns ON. The current returns from the "plus" (+) side of the energy-supplying capacitor C105 to the "minus" (-) side of the same capacitor C105, passing through the transformer Q101 D-S. During the ON cycle, the energy is stored in the transformer T101. The transistor Q101 turns OFF when the driving pulse disappears from Q101. As a result, all voltages of the dot ends of the winding flow to the positive direction and reach the fly-back rectifier. At that point of time, the diodes of the rectifier of the secondary side turn ON, a temporary energy is induced at the secondary side, and the ON cycle of the driving pulse is repeated.
2) The power supply MOS FET Q101 carries out the ON/OFF operation of the control unit, by means of U101 KA3842A. KA3842A is a PWM (pulse width modulation) IC chip, with 16 V starting voltage and 10 V cut-off voltage.
The following list shows the pin layout of KA3842A pulse width modulation IC chip.

| Pin 1: | Feedback | Pin 2: | Compensation |
| :--- | :--- | :--- | :--- |
| Pin 3: | Current sensor | Pin 4: | Oscillator |
| Pin 5: | Ground (GND) | Pin 6: | Pulse output |
| Pin 7: | VCC | Pin 8: | VREF $(5.1 \mathrm{~V})$ |

3) Overcurrent protection

R111 is a sensor resistor, and it has the function of increasing the current of this loop when the output of the secondary side is either in the overloaded state or is insufficient.
Since the current passing through the R111 sensor resistor has a voltage dropping effect, the operation of the output pulse is stopped when a voltage lower than 1 Volt is detected at pin number 3 of KA3842A 3chip, and the switch of the power supply MOS FET is kept in the "break" state until the VCC voltage is charged up to 16 Volts, and the operation of U101 KA3842A resumes. When it is not clearly known whether there is voltage shortage or not, however, this circuit repeats the ON/OFF switching, and the power supply LED lights up.
4) Starting circuit

The resistors R122 and R123 and the transistor U103 and diode D131 and resistor R169 and zener diode ZD101 are for operation starting. When the circuit starts its operation, the power supply transformer T101 supplies the auxiliary 12 Volt power to the control IC chip U101 via pins 6 and 7 of the winding transformer T101.
5) Synchronization circuit

The synchronization signal is induced from the fly-back transformer (FBT), and carries out the synchronization with the power supply frequency. The frequency range is from 31 kHz to 70 kHz , and the component elements of the synchronization circuit are D124, R116, D109, R115 and R117.
6) Feedback circuit

The feedback circuit loop induces the 12 V voltage through the pin 6 and the pin 7 of the power supply transformer. This voltage is connected with the pin 3 of the IC chip U101 by passing through U103, R135, R136 and passing next through is a regular loop.
7) Snubber circuit

The snubber circuit has the function of clamping the ON/OFF spikes of the power supply MOS-FET, and its component elements D105, C106, R106 make up a snubber that turns OFF the power supply MOS-FET.
8) Secondary rectifier and smoothing rectifier

The secondary rectifier is a harmonic rectifier consisting of D111, C124 and R128, and it works as a snubber circuit as well. The capacitors C120 and C138 are smoothing rectifiers working on the 49 Volt DC output. There are also other DC outputs, such as 80 Volt (D110), 13.5 Volt (D112) and 6.3 Volt (D113).

### 1.7 Power saving

Suspend mode : Every DC voltage operation of the CRT is turned OFF. The color of the power LED101 switches from green to orange.
OFF mode $\quad:$ This is the mode in which the CPU control unit turns OFF the power supply, but the power turns ON when the user touches the keyboard. The power LED switches to dark orange color.

1) When the power switch is turned $O N$, and there is no sync pulses to the video cable, the video shifts from the free-run mode to the suspend mode. Transistor Q107 turns OFF and the operation returns to the OFF mode within a few seconds.
2) As for the sequence of steps that turn the operation to the OFF mode, if the keyboard is not touched for a given period of time that a preset in advance, the CPU outputs the LOW level signal to transistor Q107, then Q105 turns OFF, transistor Q108 and Q104 turn OFF. As a result the power is shut out at that state.
3) When the user touches the keyboard in the OFF mode, the operation resumes, the video signals $V$ SYNC and H-SYNC turn ON the CPU via resistors R129 and R173, then the transistors Q105 and Q107 turn ON, transistors Q104 and Q108 turn ON. As a result the operation returns to the ON state.

### 1.8 DC/DC

The DC/DC voltage is DC 49 volts, and since the set-up voltage is variable from 62 volts to 160 volts, it is variable depending on the horizontal sync. The frequency band is variable from 31 kHz to 69 kHz . The voltage is fed back from the fly-back transformer (FBT). The DC/DC output voltage is used as highvoltage input of FBT T301.

1) DC/DC is a step-up circuit, and consists mainly of the choke L304, the transistor Q319, the diode D335 and U302.
2) PWM controls U302 IC TDA4857, a driving pulse is generated at the gate of transistor Q319 turning it ON. During the ON cycle, the energy is stored in the choke L304.
Transistor Q319 turns OFF when the driving pulse disappears from the gate.
As a result, the voltage at the dot terminal of the winding flows in the positive direction and goes to the fly-back rectifier. The energy stored in the choke L304 enters the FBT, passing through choke L304, diode D335 and capacitor C373.
3) The feedback is detected by the FBT via diode D310, capacitor C326, resistor R349, variable resistor VR102 and fixed resistor R382, and is connected to U302 pin 5.
This is loop is the regular type one.
4) The frequency of the sync signal coming from video H-SYNC is variable from 31 kHz to 69 kHz . The circuit consists of the R30X.
5) The soft start circuit consists of resistor R30P, capacitor C309, diode D303 and Q326.

## 2. MCU

## Monitor MCU Specification

Frequency Specification
H-freq. : $29.5 \mathrm{~K}-70 \mathrm{kHz}$
V-freq. : $43-160 \mathrm{~Hz}$
Judge polarity only when horizontal frequency is 31.5 kHz and 37.8 kHz
Support composite sync detection

## System Architecture

1. MCU - Weltrend WT6260, 60K bytes ROM size
2. EEPROM -24 C 08 series, 8 K bit, with ID code for identify initialization.
3. OSD - Myson MTV030N-46

Input

1. Sync input $\quad-2$ pins for H -sync \& V -sync frequency inverted input.
2. Key input -2 pins for A/D key input (SELECT. UP, DOWN and RECALL).
3. Burn-in ID input - 1 pins for Burn-in ID input.
4. Reset input - low pulse for reset MCU
5. Crystal input -2 pins using 8 MHz crystal.

Output - MCU digital pin

1. Degauss - Active high pulse for 2.5 sec when in degauss. MCU will activate degauss while power on.
2. CS output - 3 pins (CS2, CS1, CS0) for CS control

| H-sync | CS2 | CS1 | CS0 |
| :---: | :---: | :---: | :---: |
| H -sync $<33.25 \mathrm{kHz}$ | 0 | 0 | 0 |
| $33.25 \mathrm{kHz}<\mathrm{H}-$ sync $<36.50 \mathrm{kHz}$ | 0 | 1 | 0 |
| $36.50 \mathrm{kHz}<\mathrm{H}-$ sync $<40.50 \mathrm{kHz}$ | 0 | 1 | 1 |
| $40.50 \mathrm{kHz}<\mathrm{H}-$ sync $<45.10 \mathrm{kHz}$ | 1 | 0 | 0 |
| $45.10 \mathrm{kHz}<\mathrm{H}-$ sync $<51.60 \mathrm{kHz}$ | 1 | 0 | 1 |
| $51.60 \mathrm{kHz}<\mathrm{H}-$ sync $<55.10 \mathrm{kHz}$ | 1 | 1 | 0 |
| $55.10 \mathrm{kHz}<\mathrm{H}-$-sync $<62.15 \mathrm{kHz}$ | 1 | 1 | 0 |
| $62.15 \mathrm{kHz}<\mathrm{H}$-sync | 1 | 1 | 1 |
| Mode change | 0 | 0 | 0 |

3. Power saving - 2 pins (PMUS, PMUO) for power saving control

- if $\mathrm{Hf}>70 \mathrm{kHz}$ or $\mathrm{Hf}<23 \mathrm{kHz}$, enter power saving mode (suspend).
- enter power saving mode after 3 sec when condition is met.
- enter suspend mode first for 3 sec before enter off mode if off mode condition is met.

| Mode | H-sync freq. | V-sync freq. | Burn-in ID | PMUS | PMUO |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Normal | Yes | Yes | --- | 1 | 1 |
| Stand By | No | Yes | --- | 0 | 1 |
| Suspend | Yes | No | --- | 0 | 1 |
| Off | No | No | Low | 0 | 0 |
| Burn-in | No | No | High | 1 | 1 |

4. Mute -2 pins for screen mute

Mute1 - active low pulse for about 0.6 sec when mode change.
Mute2 - active low pulse for about 1.0 sec when mode change, active with mute 1 simultaneously.
5. D/A - 14 pins (PWM output) are Brightness, Contrast, H-phase, H-size, V-center, V-size,

Pincushion, Trapezoid, Rotation, Parallel, Pin-balance, R-gain, G-gain and B-gain.

- DAC value 255 means the maximum output volts except Parallel PWM.
- All D/A except Rotation, Brightness, Contrast, R-gain G-gain B-gain are mode dependent functions.
- Parallel is voltage inverter function.

6. Sync output - 2 pins for H -sync and V -sync negative output, normal high.
7. DDC - 2 pins (DDC SDA/DDC SCL) for DDC1/DDC2B or auto alignment control.

- In auto alignment mode, all keys and OSD are disabled.

8. SDA/SCL - 2 pins for EEPROM and OSD control.
9. WP - 1 pin, high for EEPROM write protect.

Control Panel Operation


1. Key arrangement - 7 keys for OSD control.
2. Hot key operation

Factory Mode: SELECT Key + UP (+) Key if pressed when the power SW on.

## GENERALDESCRIPTION

The WT62P2 is a microcontroller for digital controlled monitor with Universal Serial Bus (USB) interface. It contains an 8 -bit CUP, 60K bytes Flash memory, 1024 bytes RAM, 256 bits bit-addressable RAM, 14 PWMs, parallel I/Os, SYNC signal processor, timer, DDC1/2B interface, master/slave IC interface, low speed USB device module, 6-bit A/D converter and watch-dog timer.

## FEATURES

- 8-bit 6502 compatible CPU with 6 MHz operating frequency
- 60 K bytes flash memory, 1024 bytes SRAM, 256 bits bit-addressable SRAM
- 12 MHz crystal oscillator
- 14 channels 8 -bit PWM outputs
- Sync signal processor with $\mathrm{H}+\mathrm{V}$ separation, $\mathrm{H} / \mathrm{V}$ frequency counter, $\mathrm{H} / \mathrm{V}$ polarity detection/control and clamp pulse output
- Six free-running sync signal outputs (Horizontal frequency up to $106 \mathrm{kHz} 85 \mathrm{~Hz} @ 1600 \times 1200$ )
- Self-test pattern
- DDC1/2B module for EDID1.3, EDID2.0 and Enhance EDID
- Fast mode master/slave $\mathrm{I}^{2} \mathrm{C}$ interface (up to 400 kHz )
- Embedded USB function with endpoint 0 and endpoint 1
- Built-in 3.3 V regulator for USB transceiver
- Watch-dog timer
- Maximum 28 programmable I/O pins
- One 8-bit programmable timer
- 6 -bit A/D converter with 4 selectable inputs
- One external interrupt request input
- Low VDD reset


## ORDERING INFORMATION

| Package Type | Part Number |
| :---: | :---: |
| 42-pin PDIP | WT62P2-N42 |
| 42-pin Shrink PDIP | WT62P2-K42 |
| 40-pin PDIP | WT62P2-N40 |
| 44-pin SOP | WT62P2-S44 |
| 44-pin PLCC | WT62P2-L44 |



## PIN ASSIGNMENT AND PACKAGE TYPE

| Pin No. |  |  |  | Pin Name | I/O | Descriptions |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| L40 | S44 | 42 | 40 |  |  |  |
| 1 | 1 | 1 | - | D+ | I/O | USB D+ signal. |
| 2 | 2 | 2 | 1 | PWM2 | 0 | PWM2 output (10V open-drain). |
| 3 | 3 | 3 | 2 | PWM1 | 0 | PWM1 output (5V open-drain). |
| 4 | 4 | 4 | 3 | PWM0 | 0 | PWM0 output (5V open-drain). |
| 5 | 5 | 5 | 4 | /RESET/3V3 | 1 | Reset input and +3.3 V regulator output for USB tranceiver power supply. |
| 6 | - | - | - | NC |  | No Connection. |
| 7 | 6 | 6 | 5 | VDD |  | +5V power supply. |
| - | 7 | - | - | NC |  | No Connection. |
| 8 | 8 | 7 | 6 | GND |  | Ground. |
| 9 | 9 | 8 | 7 | OSCO | I/O | 12 MHz oscillator output. |
| 10 | 10 | 9 | 8 | OSCI | 1 | 12 MHz oscillator input. |
| 11 | 11 | 10 | 9 | PB5/SDA2 | I/O | Port B 5 or $I^{2} \mathrm{C}$ interface data line. |
| 12 | 12 | 11 | 10 | PB4/SCL2 | I/O | Port B4 or $\mathrm{I}^{2} \mathrm{C}$ interface clock line. |
| 13 | 13 | 12 | 11 | PB3/PAT | I/O | Port B3 or test pattern output. |
| 14 | 14 | 13 | 12 | PB2 | I/O | Port B2. |
| 15 | 15 | 14 | 13 | PB1/HFI | I/O | Port B1 or half frequency divider input. |
| 16 | 16 | 15 | 14 | PB0/HFO | I/O | Port B0 or half frequency divider output. |
| 17 | 17 | 16 | 15 | /IRQ | 1 | Interrupt request input, A low level on this can generate interrupt. |
| 18 | 18 | 17 | 16 | PC7/SOGIN | I/O | Port C7 or Sync on Green input. |
| 19 | 19 | 18 | 17 | PC6 | I/O | Port C6. |
| 20 | 20 | 19 | 18 | PC5 | I/O | Port C5. |
| 21 | 21 | 20 | 19 | PC4 | I/O | Port C4. |
| 22 | 22 | 21 | 20 | PC3/AD3 | I/O | Port C3 or ADC input 3. |
| 23 | 23 | 22 | 21 | PC2/AD2 | I/O | Port C2 or ADC input 2. |
| 24 | 24 | 23 | 22 | PC1/AD1 | I/O | Port C1 or ADC input 1. |
| 25 | 25 | 24 | 23 | PCO/AD0 | I/O | Port CO or ADC input 0. |
| 26 | 26 | 25 | 24 | PA0/SDA1 | I/O | Port A0 or DDC interface SDA pin. |
| 27 | 27 | 26 | 25 | PA1/SCL1 | I/O | Port A1 or DDC interface SCL pin. |
| 28 | 28 | 27 | 26 | PA2/PWM8 | I/O | Port A2 or PWM8 output. |
| 29 | 29 | 28 | 27 | PA3/PWM9 | I/O | Port A3 or PWM9 output. |
| 30 | 30 | 29 | 28 | PA4/PWM10 | I/O | Port A4 or PWM10 output. |
| 31 | 31 | 30 | 29 | PA5/PWM11 | I/O | Port A5 or PWM11 output. |
| 32 | 32 | 31 | 30 | PA6/PWM12 | I/O | Port A6 or PWM12 output. |
| 33 | 33 | 32 | 31 | PA7/PWM13/ CLAMP | I/O | Port A7 or PWM13 output or clamp pulse output. |
| 34 | 34 | 33 | 32 | PDO/VOUT | I/O | Port D0 or Vsync output. |
| 35 | 35 | 34 | 33 | PD1/HOUT | I/O | Port D1 or Hsync output. |
| 36 | 36 | 35 | 34 | PD2/PWM7 | I/O | Port D2 or PWM7 output. |
| 37 | 37 | 36 | 35 | PD3/PWM6 | I/O | Port D3 or PWM6 output. |
| - | 38 | - | - | NC |  | No Connection. |
| 38 | 39 | 37 | 36 | PD4/PWM5 | I/O | Port D4 or PWM5 output. |
| 39 | 40 | 38 | 37 | PD5/PWM4 | I/O | Port D5 or PWM4 output. |


| 40 | 41 | 39 | 38 | PWM3 | I/O | PWM3 output (10V open-drain) |
| :--- | :---: | :---: | :---: | :--- | :---: | :--- |
| 41 | 42 | 40 | 39 | HIN | I | Hsync input. |
| 42 | 43 | 41 | 40 | VIN | I | Vsync input. |
| 43 | - | - | - | NC |  | No Connection. |
| 44 | 44 | 42 | - | D- | I/O | USB D-signal. |

## PIN DESCRIPTION

## FUNCTIONALDESCRIPTION

## CPU

8 -bit 6502 compatible CPU wiht 16 -bit address bus and 8 -bit data bus operates at 6 MHz . The nonmaskable interrupt (/NMI) of 6502 is modified to be maskable and is defined as INT0 with higher priority. The interrupt request (/IRQ) of 6502 is defined as INT1 with lower priority.

Please refer the 6502 reference menu for more detail.

## RAM

The 1024 bytes SRAM include:
128 bytes SRAM are from $\$ 0080 \mathrm{H}$ to $\$ 00 \mathrm{FFH}$
256 bytes SRAM are from $\$ 0100 \mathrm{H}$ to $\$ 01 \mathrm{FFH}$
256 bytes SRAM are from $\$ 0200 \mathrm{H}$ to $\$ 02 \mathrm{FFH}$
256 bytes SRAM are from $\$ 0300 \mathrm{H}$ to $\$ 03 \mathrm{FFH}$
128 bytes SRAM are from $\$ 0400 \mathrm{H}$ to $\$ 047 \mathrm{FH}$

The 256 bits bit-addressable SRAM are from $\$ 0500 \mathrm{H}$ to $\$ 05 F F H$

## Flash Memory

60K bytes flash memory for program. Address is located from $\$ 1000$ to $\$$ FFFFh.

The following addresses are reserved for special purpose:
\$FFFAh (low byte) and \$FFFBh (high byte): INT0 interrupt vector.
\$FFFCh (low byte) and \$FFFDh (high byte): program reset interrupt vector.
\$FFFEh (low byte) and \$FFFFh (high byte): INT1 interrupt vector.

| $\begin{aligned} & \$ 0000 \mathrm{~h} \\ & : \\ & \$ 003 F h \end{aligned}$ | Registers |
| :---: | :---: |
| $\begin{aligned} & \text { \$0040h } \\ & : \\ & \$ 007 F h \end{aligned}$ | Reserved |
| $\begin{gathered} \text { \$0080h } \\ : \\ \text { \$00FFh } \end{gathered}$ | 128 bytes RAM |
| \$0100h <br> \$01FFh | 256 bytes RAM |
| $\begin{gathered} \text { \$0200h } \\ \vdots \\ \text { \$02FFh } \end{gathered}$ | 256 bytes RAM |
| $\begin{gathered} \$ 0300 \mathrm{~h} \\ \vdots \\ \text { \$03FFh } \end{gathered}$ | 256 bytes RAM |
| $\begin{aligned} & \text { \$0400h } \\ & : \\ & \$ 047 F h \end{aligned}$ | 128 bytes RAM |
| \$0480h <br> \$04FFh | Reserved |
| \$0500h <br> \$05FFh | Bit-addressable 256 bits RAM |
| \$0600h <br> \$0FFEh | Reserved |
| \$0FFFh | Configuration Register |
| \$1000h <br> \$FFFFh | Flash ROM |



Fig. 1 Reset Signals

## Memory Mapping

## External Reset

A low level on the RESET/3.3V pin will generate reset.

## Illegal address Reset

When the address bus of CPU goes to illegal address, a reset pulse will be generated.
The illegal address is defined as \$0040h~\$007Fh, \$0300h~\$0FFEh and \$1000h~\$7FFFh.

## Low VDD Voltage Reset

When VDD is below 3.9V, an internal reset signal is generated. The reset signal will last 2.048 ms after the voltage is higher than 3.9 V .

## Watchdog Timer Reset

If a time-out happens when watchdog timer is enabled, a reset pulse is generated. Please refer watchdog timer section for more information.

## I/O Port

## I/O Port A

Pin PA0 and PA1 are shared with DDC interface SDA1 and SCL1 When ENDDC bit is " 0 ", these two pins become an I/O port. If PAOOE bit is set, Pin PAO is an open-drain output. If PA0OE is cleared, Pin PAO is an input pin with no internal pull-up resistor. The operation of PA1 is same as PAO. Fig. 2 Shows the structure of PAO.


Fig. 2 Structure of PA0 and PA1

Pins PA2 to PA6 are shared with PWM output. When corresponding EPWMx bit is " 0 ", the pin is I/O port.

If PAxOE bit is set, it is a push-pull type output. If PAxOE bit is cleared, it is an input pin with internal pull-up resistor.
Pin PA7 is shared with PWM13 output and clamp pulse output. When both EPWM13 bit and ENCLP bit are " 0 ", this pin becomes I/O port. If PA7OE bit is set, it is a push-pull type output. If PA7OE bit is cleared, it is an input pin with internal pull-up resistor.


Fig. 3 Structure of PA2

## SYNC Processor

The functional block diagram of SYNC Processor is shown in Fig. 4. It contains H and V polarity detection circuit, H and V frequency counter, composite sync signal separation circuit, free-running H and V sync signal generator, vedio signal generation circuit for burn-in test and clamp pulse generator.


Fig. 4 Block diagram of sync signal processor

## Horizontal Polarity Detect

The horizontal polarity is detected by sampling HIN signal at 5.5~6.5us after rising and falling edge of HIN. If the result of sampling is low and lasts 192~256us with no change, the polarity is positive (HINPOL=1). If the result of sampling is high and lasts 192~256us with no change, the polarity is negative (HINPOL=0).

## Vertical Polarity Detect

Vertical polarity is detected by sampling VIN level at 2.048 ms after rising edge of VIN . If the level is low, the polarity is positive (VINPOL=1). If the level is high, the polarity is negative (VINPOL=0). But if SEPART bit is set, the VINPOL bit is " 1 " because the Vsync from composite signal separator is always positive polarity.

## Output Polarity Control

The polarities of HOUT and VOUT are controlled by HOPOL and VOPOL bites. When the bit is set, the output polarity is positive. When the bit is cleared, the output polarity is negative.

## Composite Sync Signal Separator

Composite sync signal separator extract Vsync signal from HIN or SOGIN input pin by filtering pulses which is less than 6us. The output Vsync signal will be widened about $5.5 \sim 6.5 u s$. The output Hsync will be replaced by 2us pulse during Vsync pulse.

The composite sync signal separator can handle $\mathrm{H}+\mathrm{V}$ and H exclusive $\mathrm{OR} V$ signals. Fig. 5 shows the timig relationship of the extracted H and V sync signals.

If Hsync output do not want to insert pseudo H pulses (EXTRHS signal) during Vsync pulse, set BYPASS bit can let HOUT pin output waveform same as Hsync input (Note: polarity can be controlled by HOPOL bit).


Fig. 6 Timing relationship of composite sync signal separator

Free-running sync signal and self-test pattern
The self-generated free run sync signals are output from HOUT and VOUT pins when ENFREE bit is set. Four kinds of standard VESA timings are selected by FREE1 and FREE0 bits.
Self-test pattern signal is output form PAT pin when ENPAT bit is set. PAT1 and PAT0 bits select different self-test pattern.


PAT1 $=0$, PAT0 $=0$


PAT1 $=0$, PAT0 $=1$


PAT1 $=1$, PAT0 $=0$


PAT1 $=1$, PAT0 $=1$

Fig. 7 Test Pattern

|  |  | X00 | X01 | 010 | 011 | 110 | 111 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| FH | Hot frequency | 31.496 kHz | 48 kHz | 63.83 kHz | 81.25 kHz | 90.909 kHz | 106.195 kHz |
| FV | Ver frequency | 59.993 Hz | 72.072 Hz | 59.878 Hz | 64.865 Hz | 84.8 Hz | 84.96 Hz |
| THT | Hor total time | 31.75us | 20.833us | 15.667us | 12.333us | 11us | 9.417us |
| TVT | Ver total time | 16.669 ms | 13.875 ms | 16.7 ms | 15.417 ms | 11.792 ms | 11.771 ms |
| Ths | H sync time | 3.833us | 2.417us | 1us | 1.083us | 1us | 0.833us |
| Тнв | H Back porch + <br> H Left border | 2 us | 1.417us | 2.417 us | 1.833us | 1.583us | 1.417us |
| ThF | H Front porch + H Right border | 0.708us | 1.125us | 0.542 us | 0.375us | 0.375 us | 0.292 us |
| Tvs | $V$ sync time | $2 \times$ THT | $6 \times$ Tнт | $3 \times$ THT | $3 \times$ Tнт | $3 \times$ Tнт | $3 \times$ THT |
| Tvb | V Back porch + <br> V Top border | $33 \times$ Тнт | $23 \times$ Тнт | $38 \times$ Т ${ }^{\text {¢ }}$ | $46 \times$ Тнт | $44 \times$ Тнт | $46 \times$ Тнт |
| TvF | V Front porch + <br> V Bottom border | $11 \times$ Тнт | $38 \times$ Тнт | $3 \times$ Tнт | $2 \times$ Tнт | $2 \times$ Tнт | $2 \times$ Tнт |
| Tvideo | Video pulse width | 41.67ns | 41.67ns | 41.67 ns | 41.67ns | 41.67ns | 41.67ns |



Fig. 8 Free-running sync signal and test pattern timing

## DDC Flow Chart



## Master ${ }^{2}$ C Flow Chart



## Master I ${ }^{2} \mathrm{C}$ (restart mode) Flow Chart



## Slave $I^{2} \mathrm{C}$ Flow Chart



## 3. Horizontal deflection signal processing / Vertical and geometrical compensation of the raster

$I^{2}$ C-bus autosync deflection controller for PC monitors
TDA4857

## FEATURES

## Concept features

- Full horizotal plus vertical autosync capability
- Extended horizontal frequency range from 15 to 130kHz
- Comprehensive set of $\mathrm{I}^{2} \mathrm{C}$-bus driven geometry adjustments and functions, including standby mode
- Very good vertical linearity
- Moire cancellation
- Start-up and switch-off sequence for safe operation of all power components
- X-ray protection
- Power dip recognition
- Flexible switched mode B+ supply function block for feedback and feed forward converter
- Internally stabilized voltage reference
- Drive signal for focus amplifiers with combined horizontal and vertical parabola waveforms
- DC controllable inputs for Extremely High Tension (EHT) Compensation
- SDIP32 Package


## Synchronization

- Can handle all sync signals (horizontal, vertical, composite and sync-on-video)
- Output for video clamping (leading/trailing edge selectable by the $I^{2} \mathrm{C}$-bus), vertical blanking and protection blanking
- Output for fast unlock status of horizontal synchronization and blanking on grid 1 of picture tube.


## Horizontal section

- $I^{2} C$-bus controllable wide range linear picture position, pin unbalance and parallelogram correction via horizontal phase
- Frequency-locked loop for smooth catching of horizontal frequency
- Simple frequency preset of fmin and fmax by external resistors
- Low jitter
- Soft start for horizontal and B+ control drive signals.


## Vertical section

- $I^{2} \mathrm{C}$-bus controllable vertical picture size, picture position, linearity (S-correction) and linearity balance
- Output for the $\mathrm{I}^{2} \mathrm{C}$-bus controllable vertical sawtooth and parabola (for pin unbalance and parallelogram)
- Vertical picture size independent of frequency
- Differential current outputs for DC coupling to vertical booster
- 50 to 160 Hz vertical autosync range.


## East-West (EW) section

- $I^{2} \mathrm{C}$-bus controllable output for horizontal pincushion, horizontal size, corner and trapezium correction
- Optional tracking of EW drive waveform with line frequency selectable by the $\mathrm{I}^{2} \mathrm{C}$-bus.


## Focus section

- $I^{2} \mathrm{C}$-bus controllable output for horizontal and vertical parabolas
- Vertical parabola is independent of frequency and tracks with vertical adjustments
- Horizontal parabola independent of frequency
- Adjustable pre-correction of delay in focus output stage.


## BLOCK DIAGRAM



## PINNING

| SYMBOL | PIN |  |
| :--- | :---: | :--- |
| HFLB | 1 | horizontal flyback input |
| XRAY | 2 | X-ray protection input |
| BOP | 3 | B+ control OTA output |
| BSENS | 4 | B+ control comparator input |
| BIN | 5 | B+ control OTA input |
| BDRV | 6 | B+ control driver output |
| PGND | 7 | power ground |
| HDRV | 8 | horizontal driver output |
| XSEL | 9 | select input for X-ray reset |
| VCC | 10 | supply voltage |
| EWDRV | 11 | EW waveform output |
| VOUT2 | 12 | vertical output 2 (ascending sawtooth) |
| VOUT1 | 13 | vertical output 1 (descending sawtooth) |
| VSYNC | 14 | vertical synchronization input |
| HSYNC | 15 | horizontal/composite synchronization input |
| CLBL | 16 | video clamping pulse/vertical blanking output |
| HUNLOCK | 17 | horizontal synchronization unlock/protection/vertical blanking output |
| SCL | 18 | I'C-bus clock input |
| SDA | 19 | l2C-bus data input/output |
| ASCOR | 20 | output for asymmetric EW corrections |
| VSMOD | 21 | input for EHT compensation (via vertical size) |
| VAGC | 22 | external capacitor for vertical amplitude control |
| VREF | 23 | external resistor for vertical oscillator |
| VCAP | 24 | external capacitor for vertical oscillator |
| SGND | 25 | signal ground |
| HPLL1 | 26 | external filter for PLL1 |
| HBUF | 27 | buffered f/v voltage output |
| HREF | 28 | reference current for horizontal oscillator |
| HCAP | 29 | external capacitor for horizontal oscillator |
| HPLL2 | 30 | external filter for PLL2/soft start |
| HSMOD | 31 | input for EHT compensation (via horizontal size) |
| FOCUS | 32 | output for horizontal and vertical focus |
|  |  |  |



Fig. 2 Pin configuration.

## FUNCTIONALDESCRIPTION

## Horizontal sync separator and polarity correction

HSYNC (pin 15) is the input for horizontal synchronization signals, which can be DC-coupled TTL signals (horizontal or composite sync) and AC-coupled negative-going video sync signal. Video syncs are clamped to 1.28 V and sliced at 1.4 V . This results in a fixed absolute slicing level of 120 mV related to top sync.

For DC-coupled TTL signals the input clamping current is limited. The slicing level for TTL signals is 1.4 V .

The separated sync signal (either video or TTL) is integrated on an internal capacitor to detect and normalize the sync polarity.

Normalized horizontal sync pulses are used as input signals for the vertical sync integrator, the PLL1 phase detector and the frequency-locked loop.

## Vertical sync integrator

Normalized composite sync signals from HSYNC are integrated on an internal capacitor in order to extract vertical sync pulses. The integration time is dependent on the horizontal oscillator reference current at HREF (pin 28). The integrator output directly triggers the vertical oscillator.

## Vertical sync slicer and polarity correction

Vertical sync signals (TTL) applied to VSYNC (pin 14) are sliced at 1.4 V . The output signal of the sync slicer is integrated on an internal capacitor to detect and normalize the sync polarity. The output signals of vertical sync integrator and sync normalizer are disjuncted before they are fed to the vertical oscillator.

## Video clamping/vertical blanking generator

The video clamping/vertical blanking signal at CLBL (pin 16) is a two-level sandcastle pulse which is especially suitable for video ICs such as the TDA488x family, but also for direct applications in video output stages.

The upper level is the video clamping pulse, which is triggered by the horizontal sync pulse. Either the leading or trailing edge can be selected by setting control bit CLAMP via the $I^{2} \mathrm{C}$-bus. The width of the video clamping pulse is determined by an internal single-shot multivibrator.

The lower level of the sandcastle pulse is the vertical blanking pulse, which is derived directly from the internal oscillator waveform. It is started by the vertical sync and stopped with the start of the vertical scan. This results in optimum vertical blanking. Two different vertical blanking times are accessible, by control bit VBLK, via the $I^{2} C$-bus.

Blanking will be activated continuously if one of the following conditions is true:

Soft start of horizontal and B+ drive [voltage at HPLL2 (pin 30) pulled down externally or by the $I^{2} \mathrm{C}$-bus] PLL1 is unlocked while frequency-locked loop is in search mode
No horizontal flyback pulses at HFLB (pin 1)
X -ray protection is activated
Supply voltage at Vcc (pin 10) is low

Horizontal unlock blanking can be switched off, by control bit BLKDIS, via the $I^{2} \mathrm{C}$-bus while vertical blanking is maintained.

## $1^{2}$ C-bus autosync deflection controller for PC monitors

## Frequency-locked loop

The frequency-locked loop can lock the horizontal oscillator over a wide frequency range. This is achieved by a combined search and PLL operation. The frequency range is preset by two external resistors and the
recommended maximum ratio is $\frac{f \max }{f_{\max }}=\frac{6.5}{1}$
This can, for instance, be a range from 15.625 to 90 kHz with all tolerance included.

Without a horizontal sync signal the oscillator will be freerunning at $\mathrm{f}_{\text {min }}$. Any change of sync conditions is detected by the internal coincidence detector. A deviation of more than $4 \%$ between horizontal sync and oscillator frequency switches the horizontal section into search mode. This means that PLL1 control currents are switched off immediately. The internal frequency detector then starts tuning the oscillator. Very small DC currents at HPLL1 (pin 26) are used to perform this tuning with a well defined change rate. When coincidence between horizontal sync and oscillator frequency is detected, the search mode is first replaced by a soft-lock mode which lasts for the first part of the next vertical period.
The soft-lock mode is then replaced by a normal PLL operation. This operation ensures smooth tuning and avoids fast changes of horizontal frequency during catching.

In this concept it is not allowed to load HPLL1.
The frequency dependent voltage at this pin is fed internally to HBUF (pin 27) via a sample-and-hold and buffer stange. The sample-and-hold stage removes all disturbances caused by horizontal sync or composite vertical sync from the buffered voltage. An external resistor connected between pins HBUF and HREF defines the frequency range.

## Out-of-lock indication (pin HUNLOCK)

Pin HUNLOCK is floating during search mode, or if a protection condition is true. All this can be detected by the microcontroller if a pull-up resistor is connected to its own supply voltage.

For an additional fast vertical blanking at grid 1 of the picture tube a 1 V signal referenced to ground is available at this output. The continuous protection blanking (see Section "Video clamping/vertical blanking generator") is also available at this pin. Horizontal unlock blanking can be switched off, by control bit BLKDIS via the $I^{2} \mathrm{C}$-bus while vertical blanking is maintained.

## Horizontal oscillator

The horizontal oscillator is of the relaxation type and requires a capacitor of 10 nF at HCAP (pin 29).
For optimum jitter performance the value of 10 nF must not be changed.

The minimum oscillator frequency is determined by a resistor from HREF to ground. A resistor connected between pins HREF and HBUF defines the frequency range.

The reference current at pin HREF also defines the integration time constant of the vertical sync integration.

## Calculation of line frequency range

The oscillator frequencies fmin and fmax must first be calculated. This is achieved by adding the spread of the relevant components to the highest and lowest sync frequencies $f_{\text {sync(min) }}$ and $f_{\text {sync(max) }}$. The oscillator is driven by the currents in $R_{\text {HREF }}$ and $R_{\text {HBUF }}$.

The following example is a 31.45 to 90 kHz application:

Table 1 Calculation of total spread

| spread of | for $f_{\max }$ | for $f_{\min }$ |
| :--- | :---: | :---: |
| IC | $\pm 3 \%$ | $\pm 5 \%$ |
| CHCAP | $\pm 2 \%$ | $\pm 2 \%$ |
| RHREF, RHBUF | $\pm 2 \%$ | $\pm 2 \%$ |
| Total | $\pm 7 \%$ | $\pm 9 \%$ |

Thus the typical frequency range of the oscillator in this example is:
$f_{m a x}=$ fsync $\left.^{(m a x}\right) \times 1.07=96.3 \mathrm{kHz}$

$$
f_{\min }=\frac{f_{\text {sync }}(\min )}{1.09}=28.4 \mathrm{kHz}
$$

The resistors Rhref and Rhbuf par can be calculated using the following formulae:

$$
\begin{aligned}
& R_{\text {HREF }}=\frac{78 \times \mathrm{kHz} \times \mathrm{k} \Omega}{\mathrm{f}_{\min }+0.0012 \times \mathrm{f}_{\min }^{2}[\mathrm{kHz}]}=2.61 \Omega \\
& R_{\text {HBUFpar }}=\frac{78 \times \mathrm{kHz} \times \mathrm{k} \Omega}{\mathrm{f}_{\text {max }}+0.0012 \times \mathrm{f}_{\text {max }}^{2}[\mathrm{kHz}]}=726 \Omega
\end{aligned}
$$

The resistor Rhbuf $_{\text {par }}$ os calculated as the value to RhRef and Rhbuf in parallel.

## $I^{2} \mathrm{C}$-bus autosync deflection controller for PC monitors

The formulae for $\mathrm{R}_{\text {HBUF }}$ also takes into account the voltage swing across this resistor:
$R_{\text {HBUF }}=\frac{R_{\text {HREF }} \times R_{\text {HBUFpar }}}{R_{\text {HREF }}-R_{\text {HBUFpar }}} \times 0.8=805 \Omega$

## PLL1 phase detector

The phase detector is a standard type using switched current sources, which are independent of horizontal frequency. It compares the middle of horizontal sync with a fixed point on the oscillator sawtooth voltage. The PLL1 loop filter is connected to HPLL1 (pin 26).

See also Section "Horizontal position adjustment and corrections".

## Horizontal position adjustment and corrections

Alinear adjustment of the relative phase between the horizontal sync and the oscillator sawtooth (in PLL1 loop) is achieved via register HPOS. Once adjusted, the relative phase remains constant over the whole frequency range.

Correction of pin unbalance and parallelogram is achieved by modulating the phase between oscillator sawtooth and horizontal flyback (in loop PLL2) via registers HPARAL and HPINBAL. If those asymmetric EW corrections are performed in the deflection stage, both registers can be disconnected from the horizontal phase via control bit ACD. This does not change the output at pin ASCOR.

## Horizontal moire cancellation

To achieve a cancellation of horizontal moire (also known as 'video moire'), the horizontal frequency is divided-bytwo to achieve a modulation of the horizontal phase via PLL2. The amplitude is controlled by register HMOIRE. To avoid a visible structure on screen the polarity changes with half of the vertical frequency.
Control bit MOD disables the moire cancellation function.

## PLL2 phase detector

The PLL2 phase detector is similar to the PLL1 detector and compares the line flyback pulse at HFLB (pin 1) with the oscillator sawtooth voltage. The control currents are independent of the horizontal frequency. The PLL2 detector thus compensates for the delay in the external horizontal deflection circuit by adjusting the phase of the HDRV (pin 8) output pulse.

An external modulation of the PLL2 phase is not allowed, because this would disturb the pre-correction of the horizontal focus parabola.

## Soft start and standby

If HPLL2 is pulled to ground, either by an external DC current or by resetting register SOFTST, the horizontal output pulses and $B+$ control driver pulses will be inhibited. This means that HDRV (pin 8) and BDRV (pin 6) are floating in this state. In both cases PLL2 and the frequency-lock loop are disabled, and CLBL (pin 16) provides a continuous blanking signal and HUNLOCK (pin 17) is floating.

This option can be used for soft start, protection and powerdown modes. When pin HPLL2 is released again, an automatic soft start sequence on the horizontal drive as well as on the B-drive output will be performed.

A soft start can only be performed if the supply voltage for the IC is a minimum of 8.6 V .

The soft start timing is determined by the filter capacitor at HPLL2 (pin 30), which is charged with a constant current during soft start. In the beginning the horizontal driver stage generates very small output pulses. The width of these pulses increases with the voltage at HPLL2 until the final duty cycle is reached. The voltage at HPLL2 increases further and performs a soft start at BDRV (pin 6) as well. After BDRV has reached full duty cycle, the voltage at HPLL2 continues to rise until HPLL2 enters its normal operating range. The internal charge current is now disabled. Finally PLL2 and the frequency-locked loop are activated. If both functions reach normal operation, HUNLOCK (pin 17) switches from the floating status to normal vertical blanking, and continuous blanking at CLBL (pin 16) is removed.

## Output stage for line drive pulses [HDRV (pin 8)]

An open-collector output stage allows direct drive of an inverting driver transistor because of a low saturation voltage of 0.3 V at 20 mA . To protect the line deflection transistor, the output stage is disabled (floating) for a low supply voltage at Vcc.

The duty cycle of line drive pulses is slightly dependent on the actual horizontal frequency. This ensures optimum drive conditions over the whole frequency range.

## $1^{2}$ C-bus autosync deflection controller for PC monitors

## X-ray protection

The X-ray protection input XRAY (pin 2) provides a voltage detector with a precise threshold. If the input voltage at XRAY exceeds this threshold for a certain time, then control bit SOFTST is reset, which switches the IC into protection mode. In this mode several pins are forced into defined states:

HUNLOCK (pin 17) is floating
The capacitor connected to HPLL2 (pin 30) is discharged Horizontal output stage (HDRV) is floating $B+$ control driver stage (BDRV) is floating CLBL provides a continuous blanking signal.

There are two different methods of restarting ways the IC:

1. XSEL (pin 9) is opeb-circuit or connected to ground. The control bit SOFTST must be set to logic 1 via the $I^{2} \mathrm{C}$ bus. Then the IC returns to normal operation via soft start.
2. XSEL (pin 9) is connected to Vcc via an external resistor. The supply voltage of the IC must be switched off for a certain period of time, before the IC can be restarted again using the standard power-on procedure.

## Vertical oscillator and amplitude control

This stage is designed for fast stabilization of vertical size after changes in sync frequency conditions.
The free-running frequency $f_{f r(v)}$ is determined by the resistor Rvref connected to pin 23 and the capacitor Cvcap connected to pin 24. The value of RVREF is not only optimized for noise and linearity performance in the whole vertical and EW section, but also influences several internal reference. Therefore the value of RVREF must not be changed. Capacitor Cvcap should be used to select the freerunning frequency of the vertical oscillator in accordance with the following formula:
$f_{f r(V)}=\frac{1}{10.8 \times R_{V R E F} \times C_{V C A P}}$
To achieve a stabilized amplitude the free-running frequency ffr(v), without adjustment, should be at least $10 \%$ lower than the minimum trigger frequency.
The contributions shown in Table 2 canbe assumed.

Table 2 Calculation of $f_{\text {fr(v) }}$ total spread

| Contributing elements |  |
| :--- | :--- |
| Minimum frequency offset between $\mathrm{ffr}_{\mathrm{f}(\mathrm{v})}$ and | $10 \%$ |
| lowest trigger frequency |  |
| Spread of IC | $\pm 3 \%$ |
| Spread of RVREF | $\pm 1 \%$ |
| Spread of CVCAP | $\pm 5 \%$ |
| Total | $19 \%$ |

Result for 50 to 160 Hz application:
$f_{f r(V)}=\frac{50 \mathrm{~Hz}}{1.19}=42 \mathrm{~Hz}$
The AGC of the vertical oscillator can be disabled by setting control bit AGCDIS via the $I^{2} C$-bus. Aprecise external current has to be injected into VCAP (pin 24) to obtain the correct vertical size. This special application mode can be used when the vertical sync pulses are serrated (shifted); this condition is found in some display modes, e.g. when using a 100 Hz up converter for video signals.

Application hint: VAGC (pin 22) has a high input impedance during scan. Therefore, the pin must not be loaded externally otherwise non-linearities in the vertical output currents may occur due to the changing charge current during scan.

## Adjustment of vertical size, VGA overscan and EHT compensation

There are four different ways to adjust the amplitude of the differential output currents at VOUT1 and VOUT2.
1 Register VGIN changes the vertical size without affecting any other output signal of the IC. This adjustment is meant for factory alignments.
2 Register VSIZE changes not only the vertical size, but also provides the correct tracking of all other related waveforms (see section"Tracking of vertical adjustments"). This register should be used for user adjustments.
3 For the VGA350 mode register VOVSCN can activate a $+17 \%$ step in vertical size.
4 VSMOD (pin 21) can be used for a DC controlled EHT compensation of vertical size by correcting the differential output currents at VOUT1 and VOUT2. The EW waveforms, vertical focus, pin unbalance and parallelogram corrections are not affected by VSMOD.

Adjustment of vertical position, vertical linearity and vertical linearity balance
Register VOFFS provides a DC shift at the sawtooth outputs VOUT1 and VOUT2 (pin 13 and 12) without affecting any other output waveform. This adjustment is meant for factory alignments.

Register VPOS provides a DC shift at the sawtooth output VOUT1 and VOUT2 with correct tracking of all other related waveforms (see Section "Tracking of vertical adjustments"). This register should be used for user adjustments. Due to the tracking the whole picture moves vertically while maintaining the correct geometry.

Register VLIN is used to adjust the amount of the vertical S -correction in the output signal. This function can be switched off by control bit VSC.

Register VLINBAL is used to correct the unbalance of vertical S-correction in the output signal.

## Tracking of vertical adjustments

The adjustments via registers VSIZE, VOVSCN and VPOS also affect the waveforms of horizontal pincushion, vertical linearity (S-correction), vertical linearity balance, focus parabola, pin unbalance and parallelogram correction. The result of this interaction is that no readjustment of these parameters is necessary after an user adjustment of vertical picture size and vertical picture position.

## Adjustment of vertical moire cancellation

To achieve a cancellation of vertical moire (also known as 'scan moire') the vertical picture position can be modulated by half the vertical frequency. The amplitude of the modulation is controlled by register VMOIRE and can be switched off via control bit MOD.

Horizontal pincushion (including horizontal size, corner correction and trapezium correction)

EWDRV (pin 11) provides a complete EW drive waveform. The components horizontal pincushion, horizontal size, corner correction and trapezium correction are controlled by the registers HPIN, HSIZE, HCORT, HCORB and HTRAP.

The corner correction can be adjusted separately for the top (HCORT) and bottom (HCORB) part of the picture.

The pincushion (EW parabola) amplitude, corner and trapezium correction track with the vertical picture size (VSIZE) and also with the adjustment for vertical picture position (VPOS). The corner correction does not track with the horizontal pincushion (HPIN).
Further the horizontal pincushion amplitude, corner and trapezium correction track with the horizontal picture size, which is adjusted via register HSIZE and the analog modulation input HSMOD. If the DC component in the EWDRV output signal is increased via HSIZE or Ihsmod, the pincushion, corner and trapezium component of the EWDRV output will be reduced by a factor of


The value 14.4 V is a virtual voltage for calculation only. The output pin can not reach this value, but the gain (and DC bias) of the external application should be such that the horizontal deflection is reduced to zero when EWDRV reaches 14.4 V .
HSMOD (pin 31) can be used for a DC controlled EHT compensation by correcting horizontal size, horizontal pincushion, corner and trapezium. The control range at this pin tracks with the actual value of HSIZE. For an increasing DC component VHSIZE in the EWDRV output signal, the DC component Vheht caused by lhsmod will be reduced by a
factor of $1-\frac{\mathrm{V}_{\mathrm{HSIZE}}}{14.4 \mathrm{~V}}$ as shown in the equation above.
The whole EWDRV voltage is calculated as follows:

$$
\begin{aligned}
& V_{\text {EWDRV }}=1.2 \mathrm{~V}+\left[\mathrm{VHSIZE}+\mathrm{V}_{\text {HEHT }} \times \mathrm{f}(\mathrm{HSIZE})+(\mathrm{V} \text { HPIN }+\right. \\
& \left.\left.V_{\text {HCOR }}+\mathrm{V}_{\text {HTRAP }}\right) \times \mathrm{g}(\mathrm{HSIZE}, \mathrm{HSMOD})\right] \mathrm{h}(\text { IHREF }) \text { where: } \\
& \mathrm{V}_{\text {HEHT }}=\frac{\mathrm{I}_{\text {HSMOD }}}{120 \mu 2} \times 0.69 \\
& \mathrm{f}(\mathrm{HSIZE})=1-\frac{\mathrm{V}_{\text {HSIZE }}}{14.4 \mathrm{~V}} \\
& \mathrm{~g}(\mathrm{HSIZE}, \mathrm{HSMOD})=1-\frac{V_{\text {HSIZE }}+V_{\text {HEHT }}\left(1-\frac{V_{\text {HSIZE }}}{14.4 \mathrm{~V}}\right)}{14.4 \mathrm{~V}} \\
& \mathrm{~h}\left(\mathrm{l}_{\text {HREF }}\right)=1-\frac{\mathrm{I}_{\text {HREF }}}{I_{\text {HREFf }}=70 \mathrm{kHz}}
\end{aligned}
$$

## Two different modes of operation can be chosen for the EW output waveform via control bit FHMULT:

## 1. Mode 1

Horizontal size is controlled via register HSIZE and causes a DC shift at the EWDRV output. The complete waveform is also multiplied internally by a signal proportional to the line frequency [which is detected via the current at HREF (pin 28)]. This mode is to be used for driving EW diode modulator stage which require a voltage proportional to the line frequency.

## 2. Mode 2

The EW drive waveform does not track with the line frequency. This mode is to be used for driving EW modulators which require a voltage independent of the line frequency.

## Output stage for asymmetric correction waveforms [ASCOR (pin 20)]

This output is designed as a voltage output for superimposed waveforms of vertical parabola and sawtooth. The amplitude and polarity of both signals can be change by registers HPARAL and HPINBAL via the $I^{2} \mathrm{C}$-bus.

Application hint: The TDA4856 offers two possibilities to control registers HPINBAL and HPARAL.

1. Control bit $\mathrm{ACD}=1$

The two registers now control the horizontal phase by means of internal modulation of the PLL2 horizontal phase control. The ASCOR output (pin 20) can be left unused, but it will always provide an output signal because the ASCOR output stage is not influenced by the control bit ACD.
2. Control bit $\mathrm{ACD}=0$

The internal modulation via PLL2 is disconnected. In order to obtain the required effect on the screen, pin ASCOR must now be fed to the DC amplifier which controls the DC shift of the horizontal deflection. This option is useful for applications which already use a DC shift transformer.

If the tube does not need HPINBAL and HPARAL, then pin ASCOR can be used for other purposes, i.e. for a simple dynamic convergence.

Dynamic focus section [FOCUS (pin 32)]

This section generates a complete drive signal for dynamic focus applications. The amplitude of the horizontal parabola is internally stabilized, thus it is independent of the horizontal frequency. The amplitude can be adjusted via register HFOCUS. Changing horizontal size may require a correction of HFOCUS. To compensate for the delay in external focus amplifiers a 'pre-correction' for the phase of the horizontal parabola has been implemented. The amount of this pre-correction can be adjusted via register HFOCAD. The amplitude of the vertical parabola is independent of frequency and tracks with all vertical adjustments. The amplitude can be adjusted via register VFOCUS.

FOCUS (pin 32) is designed as a voltage output for the superimposed vertical and horizontal parabolas.

## B+ control function block

The B+ control function block of the TDA4856 consists of an Operational Transconductance Amplifier (OTA), a voltage comparator, a flip-flop and a discharge circuit. This configuration allows easy applications for differnet $\mathrm{B}+$ control concepts. See also Application Note AN96052: "B+ converter Topologies for Horizontal Deflection and EHT with TDA4855/58".

## General description

The non-inverting input of the OTA is connected internally to a high precision reference voltage. The inverting input is connected to BIN (pin 5). An internal clamping circuit limits the maximum positive output voltage of OTA.
The output itself is connected to BOP (pin 3) and to the inverting input of the voltage comparator.
The non-inverting input of the voltage comparator can be accessed via BSENS (pin 4).

B+ drive pulses are generated by an internal flip-flop and fed to BDRV (pin 6) via an open-collector output stage. This flip-flop is set at the rising edge of the signal at HDRV (pin 8). The falling edge of the output signal at BDRV has a defined delay of $\mathrm{t}_{\mathrm{d}(\mathrm{BDRV})}$ to the rising edge of the HDRV pulse. When the voltage at BSENS exceeds the voltage at BOP, the voltage comparator output resets the flip-flop and, therefore, the open-collector stage at BDRV is floating again.

## $I^{2} \mathrm{C}$-bus autosync deflection controller for PC monitors

An internal discharge circuit allows a well defined discharge of capacitors at BSENS. BDRV is active at a LOWlevel output voltage (see Fig. 22), thus it requires an external inverting driver stage.

The $\mathrm{B}+$ function block can be used for $\mathrm{B}+$ deflection modulators in many different ways. Two popular application combinations are as follows:

- Boost converter in feedback mode (see Fig. 22)

In this application the OTA is used as an error amplifier with a limited output voltage range. The flip-flop is set on the rising edge of the signal at HDRV. A reset will be generated when the voltage at BSENS, taken from the current sense resistor, exceeds the voltage at BOP.
If no reset is generated within a line period, the rising edge of the next HDRV pulse forces the flip-flop to reset. The flip-flop is set immediately after the voltage at BSENS has dropped below the threshold voltage VRESTART(BSENS).

- Buck converter in feed forward mode

This application uses an external RC combination at BSENS to provide a pulse width which is independent from the horizontal frequency. The capacitor is charged via an external resistor and discharged by the internal discharge circuit. For normal operation the discharge circuit is activated when the flip-flop is reset by the internal voltage comparator. The capacitor will now be discharged with a constant current until the internally controlled stop level Vstop(bSENs) is reached. This level will be maintained until the rising edge of the next HDRV pulse sets the flip-flop again and disables the discharge circuit.
If no reset is generated within a line period, the rising edge of the next HDRV pulse automatically starts the discharge sequence and resets the flip-flop. When the voltage at BSENS reaches the threshold voltage $V_{\text {RESTART(BSENS }}$ ), the discharge circuit will be disabled automatically and the flip-flop will be set immediately. This behaviour allows a definition of the maximum duty cycle of the $B+$ control drive pulse by the relationship of charge current to discharge current.

## Supply voltage stabilizer, references, start-up procedures and protection functions

The TDA4857 provides an internal supply voltage stabilizer for excellent stabilization of all internal references. An internal gap reference, especially designed for low-noise, is the reference for the internal horizontal and vertical supply voltages. All internal reference currents and drive current for the vertical output stage are derived from this voltage via external resistors.

If eithr the supply voltage is below 8.3 V or no data from the $I^{2} \mathrm{C}$-bus has been received after power-up, the internal soft start and protection functions fo not allow any of those outputs [HDRV, BDRV, VOUT1, VOUT2 and HUNLOCK] to be active.

For supply voltages below 8.3 V the internal $\mathrm{I}^{2} \mathrm{C}$-bus will not generated an acknowledge and the IC is in standby mode. This is because the internal protection circuit has generated a reset signal for the soft start register SOFTST. Above 8.3 V data is accepted and all registers can be loaded. If the register SOFTST has received a set from the $I^{2} \mathrm{C}$-bus, the internal soft start procedure is released, which activates all above mentioned outputs.

If during normal operation the supply voltage has dropped below 8.1 V , the protection mode is activated and HUNLOCK (pin 17) changes to the protection status and is floating. This can be detected by the microcontroller.

This protection mode has been implemented in order to protect the deflection stages and the picture tube during start-up, shut-down and fault conditions. This protection mode can be activated as shown is Table 3.

## $I^{2}$ C-bus autosync deflection controller for PC monitors

Table 3 Activation of protection mode

| ACTIVATION | RESET |
| :--- | :--- |
| Low supply voltage at <br> pin10 | increase supply voltage; <br> reload registers; <br> soft start via I ${ }^{2} \mathrm{C}$-bus |
| Power dip, below 8.1 V | reload registers; <br> soft start via I ${ }^{2} \mathrm{C}$-bus or via <br> supply voltage |
| X-ray protection XRAY <br> (pin 2) triggered | reload registers; <br> soft start via I ${ }^{2} \mathrm{C}$-bus |
| HPLL2 (pin 30) externally <br> pulled to ground | release pin 30 |

When the protection mode is active, several pins of the TDA4857 are forced into a defined state:

HDRV (horizontal driver output) is floating
BDRV ( $B+$ control driver output) is floating
HUNLOCK (indicates, that the frequency-to-voltage converter is out of lock) is floating (HIGH-level via external pull-up resistor)
CLBL provides a continuous blanking signal The capacitor at HPLL2 is discharged.

If the soft start procedure is activated via the $I^{2} \mathrm{C}$-bus, all of these actions will be performed in a well defined sequence.

## Power dip recognition

In standby mode the $\mathrm{I}^{2} \mathrm{C}$-bus will only answer with an acknowledge, when data is sent to control register with subaddress 1AH. This register contains the standby and soft start control bit.

If the $I^{2} \mathrm{C}$-bus master transmits data to another register, an aknowledge is given after the chip address and the subaddress; an acknowledge is not given after the data. This indicates that only in soft start mode data can be stored into normal registers.

If the supply voltage dips under 8.1 V the TDA4857 leaves normal operation mode and changes into standby mode. The microcontroller can check this state by sending data into a register with the subaddress 0XH. The acknowledge will only be given on the data if the TDA4857 is active.

Due to this behavior the start-up of the TDA4857 is defined as follows. The first data that is transferred to the TDA4857 must be sent to the control register with subaddress 1AH. Any other subaddress will not lead to an acknowledge. This is a limitation in checking the $I^{2} \mathrm{C}$ busses of the monitor during start-up.

## APPLICATION INFORMATION



For $\mathrm{f}<50 \mathrm{kHz}$ and $\mathrm{C} 2<47 \mathrm{nF}$ calculation formulas and behaviour of the OTA are the same as for an OP. An exception is the limited output current at BOP (pin 3). See Chapter "Characteristics", Row Head "B+ control section; see Figs 22 and $23^{\circ}$.
(1) The recommended value for $R 6$ is $1 \mathrm{k} \Omega$.
a. Feedback mode application.

b. Waveforms for normal operation.

c. Waveforms for fault condition.

Fig. 22 Application and timing for feedback mode.

## 4. Horizontal drive and power supply output



## Circuit Diagram

## Description of the circuit:

1) R1, T1 and Q2 compose the horizontal driving circuit, and transistor Q1 generates a horizontal output through the driving signal.

$$
\begin{aligned}
& \mathrm{IB} 1=I_{\text {CPMAX }} / \text { Q1 }_{\text {femin }} \\
& \mathrm{I}_{\mathrm{B} 2}=3 \mathrm{I}_{\mathrm{B} 1} \\
& \mathrm{di} / \mathrm{dt}=3.3 \mathrm{~A} / \mathrm{us}
\end{aligned}
$$

2) Resistor R2 corrects the current IB1, resistor R3 works as a damping resistor and leak resistor and diode D2 works as a discharging device and polar body.
As long as transistor Q1 is OFF, the discharge is accelerated and the storage time (Tstg) is shortened.
3) H-OUT circuit wavefor


Time 5uS/div

## 5. Horizontal amplitude control

## Circuit Diagram

Circuit Description:


1) Diodes $D 1$ and $D 2$ compose the bipolar modulation circuit, and have the function of controlling the currents of the coils $\mathrm{DY}(\mathrm{Ipp})$ and $\mathrm{Lm}(\mathrm{Im})$ through voltage modulation carried out by utilizing VM .
$\mathrm{B}+=\mathrm{Vm}+\mathrm{Vcs} \quad$ Therefore, $\mathrm{Vcs}=(\mathrm{ly} * \mathrm{Ly}) / \mathrm{ts} \rightarrow \mathrm{ly}=(\mathrm{Vcs} *$ ts $) / \mathrm{Ly}$, with $\mathrm{B}+$ fixed.
Such being the case, the horizontal width decreases when $\mathrm{Vm} \uparrow \rightarrow \mathrm{Vc} \downarrow \rightarrow \mathrm{ly} \downarrow$ Inversely, the horizontal width decreases when $\mathrm{Vm} \downarrow \rightarrow \mathrm{Vcs} \uparrow \rightarrow \mathrm{ly} \uparrow$

$$
\left(B+=\left(V p^{*} 2 T r\right) /\left(\pi^{*} T s\right), T r=\sqrt{L y C t}, T m=\sqrt{L m C m}\right)
$$

2) Q2, Q3 and U1 compose the control circuit of H-WIDTH. Of those devices, the transistors Q2 and Q3 compose the Darlington current amplifier, and the operational amplifier U1 composes the emitter-coupled circuit, that stabilizes the voltage and controls the current.
3) The horizontal width broadens when $\mathrm{Va} \uparrow \rightarrow \mathrm{VbI} \downarrow \rightarrow \mathrm{I} \uparrow \rightarrow \mathrm{I} 2 \uparrow \rightarrow \mathrm{Vm} \downarrow \rightarrow$. An inference in the opposite sense is also possible.

## Test points for maintenance:

1) $\mathrm{C}_{\mathrm{T}}=31$ to $37 \mathrm{kHz}=3.2$ us

48 to $64 \mathrm{kHz}=3.0 \mathrm{us}$
$\mathrm{Cm} \div 2.8$ us
2) $\mathrm{V}_{\mathrm{A}}$ CENTER: 31 to $64 \mathrm{kHz}=1.91$ to 4.06 V
$\mathrm{V}_{\mathrm{m}}$ CENTER: 31 to $64 \mathrm{kHz}=11.6$ to 27.4 V

## 6. Blanking and spot killer

## Circuit Diagram



## Circuit Description:

1) The vertical blanking circuit is composed of Q1, Q2, Q3 and peripheral circuit. The vertical sync pulse applied to R3, R12 connected to Q5 base. Q5 is invert amplifier, then mixed with Q1 base together for vertical retrace compensation time of the blanking pulse.
2) The vertical amplifier output waveform through D1, C2, R1, R2 make waveform forming and clamp. Then applied to Q1 base, the vertical blanking amplifier of Q1, the output connected to buffer Q2, through C3 coupling to G1 control circuit. D4, D5 are for over voltage protect.
$3)$ The Q6 is spot killer protect circuit, in normal power on stage.
$\mathrm{V} 1=\mathrm{V} 2$ and ZD 1 , so Q 6 off. The CRT G1 voltage is fixed at $-45 \sim-67 \mathrm{VDc}$ with vertical blanking pulse 12Vpp VG1 = $-(\mathrm{V} \times \mathrm{R} 11) /(\mathrm{R} 10+\mathrm{R} 11),(\mathrm{V}=\mathrm{V} 1-\mathrm{V} 3)$.

When power off the voltage $\mathrm{V} 1>\mathrm{V} 2$, then Q 6 turn on pulling VG 1 to -180 V to protect CR .
4) When Mute set to lower the Q3 off G1 $=-180 \mathrm{~V}$ screen cut off no picture display, this mute circuit is active, at power ON/OFF and when mode change stage.
5) Q4 bias set up by MCU to control the Vce bias of Q3, then control G1 voltage output.

## Test points for maintenance:

1) Check D1, R3 and Q1 collector
2) G1 voltage control range $=-45 \sim-67 \mathrm{VDC}$

G1 off momentary voltage $=-180 \mathrm{VAC}$

## 7. Video amplifier system

## LM1269

## 110 MHz I²$^{2} \mathrm{C}$ RGB Video Amplifier System with OSD \& DACs

## General Description

The LM1269 pre-amp is an integrated CMOS CRT pre-amp. The IC is I2C compatible, and allows control of all the parameters necessary to direct setup and adjust the gain and contrast in the CRT display. Brightness and bias can be controlled through the DAC outputs, and is well matched to the LM2479 and LM2480 integrated bias clamp IC.
The LM1269 pre-amp is designed to work in cooperation with the LM246X high gain driver family.
Black level clamping of the signal is carried out directly on the AC coupled input signal into the high impedance preamplifier input, thus eliminating the need for the additional black level clamp capacitors.
The IC is packaged in an industry standard 24-lead DIP molded plastic package.

## Features

- $I^{2} \mathrm{C}$ compatible interface to micro-controller
- 110 MHz bandwidth preamplifier with full video signal parametric control
- 4 external 8-bit DACs for bus controlled Bias and Brightness
- Suitable for use with discrete or integrated clamp, with software configurable Brightness mixer
- Power Save (Green) Mode, 80\% power reduction
- Matched to LM246X driver


## Applications

- Low end 14 ", 15 ", and 17 " bus controlled monitors with OSD
- $1024 \times 768$ displays up to 70 Hz requiring OSD capability
- Very low cost system with LM246X driver


## Block and Connection Diagram

## Timing Diagrams



FIGURE 1.

## Pin Descriptions



FIGURE 3. OSD Output Skew

## Pin Descriptions

| Pin No. | Pin Name | Schematic | Description |
| :---: | :---: | :---: | :--- |
| 1 | Red OSD Input | These inputs accept standard TTL or |  |
| 2 | Green OSD Input |  | CMOS input. Each color is either fully on <br> 3 |
| Blue OSD Input |  |  |  |
| logic high) or fully off (logic low). Unused |  |  |  |
| pins should be connected to ground with a |  |  |  |
| 47k resistor. |  |  |  |

## Pin Descriptions

| Pin No. | Pin Name | Red Video Input <br> Green Video Input <br> Blue Video Input |  |
| :---: | :---: | :---: | :--- | :--- |

## Function Description

| Pin No. | Pin Name | Red Video Out <br> Green Video Out <br> Blue Video Out |  |
| :---: | :---: | :---: | :--- |

All functions of the LM1269 are controlled through the $I^{2} \mathrm{C}$ Bus. Details on the internal registers are covered in the $\mathrm{I}^{2} \mathrm{C}$ Interface

Registers Section. Figure 1 shows the block diagram of the LM1269. The $I^{2} \mathrm{C}$ signals come in on pins 11 and 12 and go to the $I^{2} \mathrm{C}$ Interface. Both the internal blocks with an " R " and the four external DACs are controlled by the $I^{2} \mathrm{C}$ Interface. The video and OSD block are shown for the red channel in Figure 1. The blocks for both the green and blue channels are not shown; however, they are identical to the red channel.
Proper operation of the LM1269 does require a very accurate reference voltage. This voltage is generated in the $\mathrm{V}_{\text {Ref }}$ block. To insure an accuate voltage over temperature, an external resistor is used to set the current in the $\mathrm{V}_{\text {Ref }}$ stage. The external resistor is connected to pin 10 . This resistor should be $1 \%$ and have a temperature coefficient under $100 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$. ALL VIDEO SIGNALS MUST BE KEPT AWAY FROM PIN 10. This pin has a very high input impedance and will pick up any high frequency signals routed near it. The board layout shown in Figure 10 is a good example of trace routing near pin 10 . The output of the $V_{\text {Ref }}$ stage goes to a number of blocks in the video section and also to pin 21. This pin allows capacitor filtering on the $\mathrm{V}_{\text {Ref }}$ output and offers an accurate external reference. A buffer must be used with this reference, the maximum current loading should be only $100 \mu \mathrm{~A}$. Note: Any noise injected into pin 21 will appear on the video. The voltage reference must be kept very clean for best performance of the LM1269.
The video inputs are pins 5,6 , and 7 . Looking at the red channel (pin 5) note that the "Clamp DC Restore Amp" is connected to this pin. Since the video must be AC coupled to the LM1269, the coupling cap is also used to store the reference voltage for DC restoration. The "Clamp DC Re-store Amp" block charges the input capacitor to the correct voltage when the clamp pulse (pin 23) is active. The "Hi Z Input Buffer Amp" buffers the video signal for internal processing. Input impedance to this stage is typically 20 MW . With such a high impedance the DC restoration can appear to be working for a number of minutes after the clamp pulse in removed.
The output of the Buffer Amp goes to the Contrast stage. The 7 bit contrast register (03h) sets the contrast level through the $I^{2} \mathrm{C}$ bus. This register controls the Contrast stage in each video channel. Contrast adjustment range is up to -20 dB . Loading all zeros in the contrast register gives -20 dB attenuation. All ones will give no attenuation. The output of this stage is used as the feedback for the DC restoration loop. "Auto Beam Limit Amp" or ABL is the next block in the video path. This is a voltage controlled gain stage which gives no attenuation with 5 V at pin 22 and gives about -10 dB attenuation with 2 V at pin 2 . ABL is covered in more detail later in this section.
Next in the video path is the "OSD Mixer". The OSD Select signal at pin 4 controls this stage, selecting OSD with a high at pin 4 , and video with a low at pin 4 . Since the DC restoration feedback is at the Contrast output, the video black level will match the OSD black level. The OSD signal is mixed with the video signal at the output of this stage.

The OSD goes through the "OSD Contrast" stage before entering the "OSD Mixer" block. Bits 3 and 4 of register 08 h control the

OSD contrast giving four video levels for the OSD window. Maximum video level for the OSD window occurs with both bits set to one. Minimum video level will occur with both bits set to a zero. Following the "OSD Mixer" is the "Gain" block. Each video channel has its own independent control of this block so the user can balance the color of the CRT display. Registers 00h, 01h, 02h are used for the gain attenuation. These registers are 7 bits with the maximum attenuation of -10 dB occurring when all zeros are loaded.
The final block in the video path is the "Output Buffer Amp". This stage provides the drive needed for the inputs of a CRT driver. The recommended driver for this pre-amp is one of the LM246X family. Horizontal blanking is also added to the video signal from the "H Blank" stage. This block is covered in more detail below. DC offset of the output is set by the "DC DACs Offset" stage. Bits 0 through 2 in register 08 control this stage. This gives 8 different black levels ranging from 0.75 V to 1.55 V . When using one of the LM246X CRT driver family it is recommended that the black level be set to 1.25 V .
ABL: The Auto Beam Limit control reduces the gain of the video amplifiers in response to a control voltage proportional to the CRT beam current. The ABL acts on all three channels in an identical manner. This is required for CRT life and X-ray protection. The beam current limit circuit application is as shown in Figure 4: when no current is being drawn by the EHT supply, current flows from the supply rail through the ABL resistor and into the ABL input of the IC. The IC clamps the input voltage to a low impedance voltage source (the 5 V supply rail).
When current is drawn from the EHT supply, some of the current passing through the ABL resistor goes to the EHT supply, which reduces the current flowing into the ABL input of the IC. When the EHT current is high enough, the current flowing into the ABL input of the IC drops to zero. This current level determines the ABL threshold and is given by:

$$
I_{A B L}=\frac{V_{S}-V_{A B L T H}}{R_{A B L}}
$$

Where:
$V_{S}$ is the external supply (usually the CRT driver supply rail, about 80 V )
$\mathrm{V}_{\text {ABL TH }}$ is the threshold ABL voltage of the IC
$R_{A B L}$ is the ABL resistor value
$I_{A B L}$ is the ABL limit
When the voltage on the ABL input drops below the ABL threshold of the pre-amp the gain of the pre-amp reduces, which reduces the beam current. A feedback loop is thus established which acts to prevent the average beam current exceeding $I_{A B L}$. H Flyback: H Flyback is an analog signal input from the monitor horizontal scan. The "H Blank" section uses this signal to add

Typical Monitor H Flyback


## FIGURE 5. H Flyback Input Pulse

a logic input. It is necessary for the current flow into pin 24 to reverse for proper operation. Therefore the logic signal must be AC coupled into pin 24 . Figure 6 shows the recommended circuit for a logic signal input. The blank signal must be a positive pulse. Power Save Mode: There are two modes of power save:

1. Blanking the video
2. Turning off most of the power for maximum power savings.


FIGURE 6. Standard Logic H Blank
In the first mode the video is completely blanked. By setting bit0 in register 90 to a 1 the video will be completely blanked. This gives some power saving since there is no beam current in the monitor. Maximum power saving is obtained in the second mode. Bits 0 and 1 in register 9 should be set to a 1 . Bit 1 in register 9 turns off the video output stage of the LM1269, giving a high impedance at the output pin. After bits 0 and 1 of register 9 are set to a 1 , the power supplies to the CRT driver and CRT can be turned off.
Note: The 5 V supply must remain on for proper operation. Since the LM1269 is a CMOS device its power consumption will be minimal.
External DACs: Four DACs with external outputs are provided in the LM1269. Normally these DACs will be used for color bal-
ance and brightness control. If the brightness control is done at G1, then three DACs would be used for color balance and the last DAC would be used for controlling the G 1 voltage.
There is also a provision to set the brightness at the cathodes. DAC 4 can be set to vary the outputs of the other three DACs after the color balance is completed. This is accomplished by adding the output of DAC 4 to the other 3 DACs. Bits 3 and 4 of register 9 are set to a 1 for brightness control at the cathodes. Bit 3 sets the output range of DAC $1-3$ to $50 \%$ of their full range. Bit 4 adds $50 \%$ of DAC 4 to the other three DACs. These two adjustments keeps the overall output voltage of DAC 1-3 in the proper range and still allows brightness control. For either mode of brightness control, the DACs are ideally set to work with the LM2479 or LM2480 for DC restoration at the cathodes of the CRT.

## ESD and Arc-Over Protection

The LM1269 incorporates full ESD protection with special consideration given to maximizing arc-over robustness. The monitor designer must still use good circuit design and PCB layout techniques. The human body model ESD susceptibility of the LM1269 is 3.5 kV , however many monitor manufacturers are now testing their monitors to the level 4 of the IEC 801-2 specification which requires the monitor to survive an 8 kV discharge. External ESD protection is needed to survive this level of ESD. The LM1269 provides excellent protection against both ESD and arc-over, but this is not a substitute for good PCB layout. Figure 7 shows the recommended input protection for the LM1269. This provides the best protection against ESD. When this protection is combined with good PCB layout the LM1269 will easily survive the IEC $801-2$ level 4 testing ( 8 kV ESD). It is strongly recommended that the protection diodes be added as shown in Figure 7. The 1 N 4148 diode has a maximum capacitance of 4 pF , which will have little effect on the response of the video system due to the low impedance of the input video.

The ESD cells of the LM1269 also provide good protection against arc-over, however good PCB layout is necessary. The LM1269 should not be exposed directly to the voltages that may occur during arc-over. The main vulnerability of the LM1269 to arc-over is though the ground traces on the PCB. For proper protection all ground connections associated with the LM1269, including the grounds to the bypass capacitors, must have short returns to the ground pins. A significant ground plane should be used to connect all the LM1269 grounds which shows the demo board layout, is an excellent example of an effective ground plane. The list below should be followed to ensure a PCB with good grounding:
All grounds associated with the LM1269 should be connected together through a large ground plane.
CRT driver ground is connected to the video pre-amp group at one point.
CRT and arc protection grounds are connected directly to the chassis or main ground. There is no arc-over current flow from these grounds through the LM1269 grounds.
Input signal traces for SDA, SCL, H Flyback, and Clamp should be kept away from the CRT driver and all traces that could carry the arc current.
Output signal traces of the LM1269 should be kept away from the traces that carry the output signals of the CRT driver. If any one of the above suggestions is not followed the LM1269 may become more vulnerable to arc-over. Improper grounding is by far the most common cause of video pre-amp failure during arc-over.


FIGURE 7. Recommended Video Input ESD Protection

## 8. 9nS Hight Gain CRT Driver

## LM2469

## Monolothic Triple 9nS High Gain CRT Driver

## Gerenral Description

The LM2469 is an integrated high voltage CRT driver circuit designed for use in color monitor applications. The IC contains three high input impedance wide band amplifiers, which directly drive the RGB cathodes of a CRT. Each channel has its gain internally set to -20 and can drive CRT capacitive loads as well as resistive loads present in other applications, limited only by the package's power dissipation. The IC is packaged in an industry standard 9 lead TO-220 molded plastic package.

## Features

- Higher gain to match LM126X CMOS preamplifiers
- 0 V to 3.75 V input range
- Stable with 0-20pF capacitive loads and inductive peaking networks
- Maintains standard LM243X Family Pinout which is designed for easy PCB layout
- Convenient TO-220 staggered lead package style


## Applications

- Up to $1024 \times 768$ at 70 Hz
- Pixel clock frequencies up to 75 MHz
- Monitors using video blanking


## Schematic Diagram



FIGURE 1. Simplified Schematic Diagram (One Channel)

## Schematic Diagram



Note: Tab is at GND.

FIGURE 2. Top View Order Number: LM2469TA N\$ package Number: TA09A

## THEORY OF OPERATION

The LM2469 is high voltage monolithic three channel CRT driver suitable for color monitor applications. The LM2469 operates with 80 V and 12 V power supplies. The part is housed in the industry standard 9-lead TO-220 molded plastic power package. The circuit diagram of the LM2469 is shown in Figure 1. The PNP emitter follower, Q5, provides input buffering. Q1 and Q2 form a fixed gain cascode amplifier with resistors R1 AND R2 setting the gain at -20 . Emitter followers Q3 and Q4 isolate the high output impedance of the amplifier, decreasing the sensitivity of the device to changes in load capacitance. Q6 provides biasing to the output emitter follower stage to reduce crossover distortion at low signal levels.
Figure 3 shows a typical test circuit for evaluation of the LM2469. This circuit is designed to allow testing of the LM2469 in a 50W environment without the use of an expensive FET probe. In this test circuit, two low inductance resistors in series totaling 4.95KW form a 200:1 wideband, low capacitance probe when connected to a 50 W load (such as 50 W oscilloscope input). The input signal from the generator is AC coupled to the base of Q5.

## APPLICATION HINTS

## INTRODUCTION

National Semiconductor (NSC) is committed to provide application information that assists our customers in obtaining the best performance possible from our products. The following information is provided in order to support this commitment. The reader should be aware that the optimization of performance was done using a specific printed circuit board designed at NSC. Variations in performance can be realized due to physical changes in the printed circuit board and the application. Therefore, the designer should know that component value changes might be required in order to optimize performance in a given application. The values shown in this document can be used as a starting point for evaluation purposes. When working with high bandwidth circuits, good layout practices are always critical to achieving maximum performance.

## IMPORTANT INFORMATION

The LM2469 performance is targeted for the VGA ( $640 \times 480$ ) to ( $1024 \times 768,70 \mathrm{~Hz}$ refresh) resolution market. It is designed to be a replacement for discrete CRT drivers. The application circuits shown in this document to optimize performance and to protect against damage from CRT arc-over are designed specifically for the LM2469. If another member of the LM246X family is used, pleased refer to its datasheet.

## POWER SUPPLY BYPASS

Since the LM2469 is a wide bandwith amplifier, proper power supply bypassing is critical for optimum performance. Improper power supply bypassing can result in large overshoot, ringing or oscillation. A 0.1 uF capacitor should be connected from the supply pin, $\mathrm{V}_{\mathrm{cc}}$ to ground, as close to the supply and ground pins as is practical. Additionally, a 10 uF to 100 uF electrolytic capacitor should be connected from the supply pin to ground. The electrolytic capacitor should also be placed reasonably close to the LM2469's supply and ground pins. A 0.10 uF capacitor should be
connected from the bias pin $\left(\mathrm{V}_{\mathrm{bb}}\right)$ to the ground, as close as is practical to the part.

## ARC PROTECTION

During normal CRT operation, internal arcing may occasionally occur. Spark gaps, in the range of 200 V , connected from the CRT cathodes to CRT ground will limit the maximum voltage, but to a value that is much higher than allowable on the LM2469. This fast, high voltage, high energy pulse can damage the LM2469 output stage. The application circuit shown in Figure 4 is designed to help clamp the voltage at the output of the LM2469 to a safe level. The clamp diodes, D1 and D2, should have a fast transient response, high peak current rating, low series impedance and low shunt capacitance. FDH400 or equivalent diodes are recommended. Do not use 1N4148 diodes for the clamp diodes. D1 and D2 should have short, low impedance connections to $\mathrm{V}_{C C}$ and ground respectively. The cathode of D1 should be located very close to a separately decoupled bypass capacitor (C3 in Figure 4). The ground connection of D2 and the decoupling capacitor should be very close to the LM2469 ground. This will significantly reduce the high frequency voltage transients that the LM2469 would be subjected to during an arcover condition. Resistor R2 limits the arcover current that is seen by the diodes while R1 limits the current into the LM2469 as well as the voltage stress at the outputs of the device. R2 should be a $1 / 2 \mathrm{~W}$ solid carbon type resistor. R1 can be a $1 / 4 \mathrm{~W}$ metal or carbon film type resistor. Having large value resistors for R1 and R2 would be desirable, but has the effect of increasing rise and fall times. Inductor L1 is critical to reduce the initial high frequency voltage levels that the LM2469 would be subjected to. The inductor will not only help protect the device, but will also help optimize rise and fall times as well as minimize EMI. For proper arc protection, it is important to not omit any of the arc protection components shown in Figure 4.


FIGURE 4. One Video Channel of the LM2469 with the Recommended Arc Protection Circuit

## OPTIMIZINGTRANSIENTRESPONSE

Referring to Figure 4, there are three components (R1, R2 and L1) that can be adjusted to optimize the transient response of the application circuit. Increasing the values of R1 and R2 will slow the circuit down while decreasing overshoot. Increasing the value of L1 will speed up the circuit as well as increase overshoot. It is very important to use inductors with very high self-resonant frequencies, preferably above 300 MHz . Ferrite core inductors from J.W. Miller Magnetics (part \#78FR39K) were used for optimizing the performance of the device in the NSC application board. The values shown in Figure 4 can be used as a good starting point for the evaluation of the LM2469. Using variable resistors for R1 and the parallel resistor will simplify finding the values needed for optimum performance in a given application. Once the optimum values are determined, the variable resistors can be replaced with fixed values.

## Effect of Load Capacitance

Figure 13 shows the effect of increased load capacitance on the speed of the device. This demonstrates the importance of knowing the load capacitance in the application. Note that the fall time stayed fairly constant while the rise time increased approximately $1.8 \%$ per pF .

## Effect of Offset

Figure 11 shows the variation in rise and fall times when the output offset of the device is varied from 40VDC to 50VDC. The rise time shows a maximum variation relative to the center data point (45VDC) of less than $1.3 \%$. The fall time shows a variation of about $3.9 \%$ relative to the center data points.

## THERMAL CONSIDERATIONS

Figure 10 shows the performance of the LM2469 video amplifiers in the test circuit shown in Figure 3 as a function of case temperature. The figure shows that the rise time of the LM2469 increases by approximately $9 \%$ as the case temperature increases from $30^{\circ} \mathrm{C}$ to $100^{\circ} \mathrm{C}$. This corresponds to a speed degradation of $1.3 \%$ for very $10^{\circ} \mathrm{C}$ rise in case temperature.
Figure 9 shows the maximum power dissipation of the LM2469 vs. Frequency when all three channels of the device are driving an 8 pF load with a $40 \mathrm{~V}_{\mathrm{p-p}}$ signal alternating one pixel on, one pixel off. The graph assumes a $72 \%$ active time (device operating at the specified frequency) which is typical in a monitor application. The other $28 \%$ of the time the device is assumed to be sitting at the black level ( 65 V in this case). This graph gives the designer the information needed to determine the heat sink requirement for his application. The designer should note that if the load capacitance is increased, the AC component of the total power dissipation will also increase.
The LM2469 case temperature must be maintained below $100^{\circ} \mathrm{C}$. If the maximum expected ambient temperature is $70^{\circ} \mathrm{C}$ and the maximum power dissipation is 3.85 W (from Figure $9,50 \mathrm{MHz}$ bandwith), then a maximum heat sink thermal resistance can be calculated:
$R_{T H}=\frac{100^{\circ} \mathrm{C}-70^{\circ}}{3.85 \mathrm{~W}}=7.8^{\circ} \mathrm{C} / \mathrm{W}$
This example assumes a capacitive load of 8 pF and no resistive load.

## TYPICALAPPLICATION

The typical application of the LM2469 is shown in Figure 5 \& 6 . Used in conjunction with an LM126X and an LM2479/2480 bias clamp, a complete video channel from monitor input to CRT cathode can be achieved. Performance is ideal for $1024 \times 768$ resolution displays with pixel clock frequencies up top 75 MHz . Figure 6 are the schematic for the NSC demonstration board that can be used to evaluate the LM126X/246X/2480 combination in a monitor.

## PC Board Layout Considerations

For optimum performance, an adequate ground plane, isolation between channels, good supply bypassing and minimizing unwanted feedback are necessary. Also, the length of the signal traces from the preamplifier to the LM2469 and from the LM2469 to the CRT cathode should be as short as possible. The following references are recommended:
Ott, Henry W., "Noise Reduction Techniques in Electronic Systems", John Wiley \& Sons, New York, 1976.
"Video Amplifier Design for Computer Monitors", National Semiconductor Application Note 1013.
Pease, Robert A., "Troubleshooting Analog Circuits", Butterworth-Heinemann, 1991.
Because of its high small signal bandwith, the part may oscillate in a monitor if feedback occurs around the video channel through the chassis wiring. To prevent this, leads to the video amplifier input circuit should be shielded, and input wiring should be spaced as far as possible from output circuit wiring.

## NSC Demonstration Board

Figure 7 shows the routing and component placement on the NSC LM126X/246X demonstration board. The schematic of the board is shown in Figure 6. This board provides a good example of a layout that can be used as a guide for future layouts. Note the location of the following components:

- C16, C19 - V ${ }_{\text {cc }}$ bypass capacitor, located very close to pin 4 ground pins.
- $\mathrm{C} 17, \mathrm{C} 20-\mathrm{V}_{\mathrm{BB}}$ bypass capacitors, located close to pin 8 and ground.
- C46, C47, C48 - $V_{c c}$ bypass capacitors near LM2469 V clamp diodes. Very important for arc protection.
The routing of the LM2469 video outputs to the CRT is very critical to achieving optimum performance. It shows the routing and component placement from pin 3 of the LM2469 to the blue cathode. Note that the components are placed so that they almost line up from the output pin of the LM2469 to the blue cathode pin of the CRT connector. This is done to minimize the length of the video path between these two components. Note also that D8, D9, R24, and D6 are placed to minimize the size of the video nodes that they are attached to. This minimizes parasitic capacitance in the video path and also enhances the effectiveness of the protection diodes. The anode of protection diode D8 is connected directly to a section of the ground plane that has a short and direct path to the LM2469 ground pins. The cathode of D9 is connected to $V_{c c}$ very close to decoupling capacitor C48 which is connected to the same section of the ground plane as D8. The diode placement and routing is very important for minimizing the voltage stress on the LM2469 video outputs during an arc over event. Lastly, notice that S 3 is placed very close to the blue cathode and is tied directly to the ground under the CRT connector.



## 9. Bias Clamp

## LM2480

## 80V Triple Bias Clamp

## General Description

The LM2480 driver is an integrated 80V triple bias clamp circuit for DC recovery of each of the AC coupled outputs of a CRT driver. It is well matched with the DAC outputs of the LM126/x family of preamplifiers. Each amplifier has its gain internally set to -18 . The IC is package.

- High input impedance
- Single supply operation
- Matched to the LM126X family of preamplifiers


## Recommended Applications

- CRT monitor requiring DC restoration at the cathodes


## Features

- Wide range integrated triple bias clamp


## Block Diagrams



FIGURE 1. Simplified Schematic (One Channel)

Package Pinout


FIGURE 2. LM2480 Package Pinout Order Number LM2480NA NS Package Number: N08E

## Typical Performance Characteristics

(VCC $=+80 \mathrm{~V}$ ), Test Circuit - Figure 3 unless otherwise specified.


## THEORY OF OPERATION

The circuit diagram of the LM2480 is shown in Figure 1. The DC clamp circuit amplifies the input signal by -18 and the gain is set by the resistor ratio of 18 R and R . The output requires pull-up resistor to 80 V . Figure 2 shows the test circuit used for evaluation of the LM2480 Clamp Amplifier. A high impedance voltmeter (100MW) is used for DC measurements at the output. The DC transfer function is shown in Figure 4.

## APPLICATION HINTS

## Power Supply Bypass

The LM2480 should have proper power supply bypassing for optimum performance. A 0.1 mF capacitor should be connected from the supply pin, $\mathrm{V}_{\mathrm{cc}}$ to ground, as close to the supply and ground pins as is practical. Additionally, a 1.0 mF electrolytic capacitor should be connected from the supply pin to ground. The
electrolytic capacitor should also be placed reasonably close to the LM2480's supply and ground pins.

## Application Circuit

The application circuit shown in Figure 5 is designed to help clamp the voltage at the output of the driver to the desired level. Capacitor $\mathrm{C}_{4}$ stabilizes the entire node at the anode of the clamp diode, $\mathrm{D}_{3}$, by creating a low impedance at high frequencies. Figure 5 also shows the standard application circuit topology when used with an LM246X CRT driver. It shows all the components necessary to optimize performance as well as to protect against damage from a CRT arc event. No additional components are required to protect the LM2480 from arc damage.


FIGURE 5. One Channel of the LM2480 and LM246X Application Circuit

## Demonstration Hardware

National Semiconductor has designed a demonstration neckboard for the LM126X, LM246X, and the LM2480 chipset. To obtain demonstration board contact the National Semiconductor Sales Office in your region.

## 10. On Screen Display

## MTV030

## On-Screen Display with Auto-Sizing Controller

## FEATURES

- Horizontal SYNC input up to 150 kHz .
- On-chip PLL circuitry up to 150 MHz .
- Minimum timing measurement among HFLB, VFLB, RIN, GIN and BIN for auto sizing.
- Full screen self-test pattern generator.
- Programmable Hor. resolutions up to 1524 dots per line.
- Full-screen display consists of 15 (rows) by 30 (columns)
- Two font size $12 \times 16$ or $12 \times 18$ dot matrix per character.
- True totally 512 mask ROM fonts including 496 standard fonts and 16 multi-color fonts.
- Double character height and/or width control.
- Programmable positioning for display screen center.
- Character bordering, shadowing and blinking effect.
- Programmable character height (18 to 71 lines) control.
- Row to row spacing control to avoid expansion distortion.
- 4 programmable windows with multi-level operation.
- Shadowing on windows with programmable shadow width/ height/color.
- Programmable adaptive approach to handle H, V sync collision automatically by hardware.
- Software clears bit for full-screen erasing.
- Fade-in/fade-out or blending-in/blending-out effects.
- 5-channel/8-bit PWM D/A converter output.
- Compatible with SPI bus or $\mathrm{I}^{2} \mathrm{C}$ interface with slave address 7AH/7BH (slave address is mask option).
- 16-pin, 20-pin or 24-pin PDIP package.


## GENERALDESCRIPTION

MTV030 is designed for monitor applications to display built-in characters or fonts onto monitor screen. The display operation occurs by transferring data and control information from the micro-controller to RAM through a serial data interface. It can execute full-screen display automatically, as well as specific functions such as character background, bordering, shadowing, blinking, double height and width, font by font color control, frame positioning, frame size control by character height and row to row spacing, horizontal display resolution, full-screen erasing, fade-in/fade-out effect, ndowing effect, shadowing on window and full-screen self-test pattern generator.
MTV030 provides true 512 fonts including 496 standard fonts and 16 multi-color fonts and 2 font sizes, $12 \times 16$ or $12 \times 18$ for more efficacious applications. So each one of the 512 fonts can be displayed at the same time. The full OSD menu is formed by 15 rows $\times 30$ columns, which can be positioned anywhere on the monitor screen by changing vertical or horizontal delay. The auto sizing video measurement module measure the timing relationship among HFLB, VFLB, and R, G, BIN at the speed related to the OSD resolution. MCU can get the measurement data, active video, front porth and back porth, through $I^{2} \mathrm{C}$ bus read/write operation to keep the appropriate display size and center.

## BLOCK DIAGRAM



* MTV030N16 is used in this Model.



### 2.0 PIN DESCRIPTIONS

| Name | I/O | Pin No. |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :--- |
|  |  | N201 | N202 | N24 |  |  |
| VSSA | - | 1 | 1 | 1 | 1 | Analog ground. This ground pin is used to internal analog <br> circuitry. |
| VCO | I/O | 2 | 2 | 2 | 2 | Voltage Control Oscillator. This pin is used to control the <br> internal oscillator frequency by DC voltage input from <br> external low pass filter. |
| RP | I/O | 3 | 3 | 3 | 3 | Bias Resistor. The bias resistor is used to regulate the <br> appropriate bias current for internal oscillator to resonate at <br> specific dot frequency. |
| VDDA | - | 4 | 4 | 4 | 4 | Analog power supply. Positive 5 V DC supply for internal <br> analog circuitry. And a 0.1 $\mu$ F decoupling capacitor should be <br> connected across to VDDA and VSSA. |
| HFLB | I | 5 | 5 | 5 | 5 | Horizontal input. This pin is used to input the horizontal <br> synchronizing signal. It is a leading edge triggered and has <br> an internal pull-up resistor. |


| Name | I/O | Pin No. |  |  |  | Descriptions |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | N16 | N201 | N202 | N24 |  |
| SSB | 1 | 6 | 6 | 6 | 6 | Serial interface enable. It is used to enable the serial data and is also used to select the operation of $I^{2} \mathrm{C}$ or SPI bus. If this pin is left floating, $I^{2} \mathrm{C}$ bus is enabled, otherwise the SPI bus is enabled. |
| SDA | 1 | 7 | 7 | 7 | 7 | Serial data input. The external data transfer through this pin to internal display registers and control registers. It has an internal pull-up resistor. |
| SCK | 1 | 8 | 8 | 8 | 8 | Serial clock input. The clock-input pin is used to syn-chronize the data transfer. It has an internal pull-up resistor. |
| RIN | 1 | - | - | 9 | 9 | Red video input. It is used for auto sizing measurement and this signal is came from video pre-amp red output. |
| GIN | 1 | - | - | 10 | 10 | Green video input. It is used for auto sizing measurement and this signal is came from video pre-amp green output. |
| BIN | 1 | - | - | 11 | 11 | Blue video input. It is used for auto sizing measurement and this signal is came from video pre-amp blue output. |
| NC | - | - | - | 12 | - | No connection. |
| PWM0 | 0 | - | 9 | - | 12 | Open-Drain PWM D/A converter 0. The output pulse width is programmable by the register of Row 15 , column 23. |
| PWM1 | 0 | - | 10 | - | 13 | Open-Drain PWM D/A converter 1. The output pulse width is programmable by the register of Row 15 , column 24. |
| PWM2 | 0 | - | 11 | - | 14 | Open-Drain PWM D/A converter 2. The output pulse width is programmable by the register of Row 15 , column 25. |
| PWM3 | O | - | 12 | - | 15 | Open-Drain PWM D/A converter 3. The output pulse width is programmable by the register of Row 15 , column 26. |
| PWM4 | 0 | - | - | - | 16 | Open-Drain PWM D/A converter 4. The output pulse width is programmable by the register of Row 15, column 27. |
| VDD | - | 9 | 13 | 13 | 17 | Digital power supply. Positive 5 V DC supply for internal digital circuitry and a 0.1 uF decoupling capacitor should be connected across to VDD and VSS. |
| VFLB | 1 | 10 | 14 | 14 | 18 | Vertical input. This pin is used to input the vertical synchronizing signal. It is leading triggered and has an internal pull-up resistor. |
| INT | O | 11 | 15 | 15 | 19 | Intensity color output. 16-color selection is achievable by combining this intensity pin with R/G/B output pins. |
| FBKG | O | 12 | 16 | 16 | 20 | Fast Blanking output. It is used to cut off external R, G, B signals of VGA while this chip is displaying character or windows. |
| BOUT | O | 13 | 17 | 17 | 21 | Blue color output. It is a blue color video signal output. |
| GOUT | 0 | 14 | 18 | 18 | 22 | Green color output. It is a green color video signal output. |
| ROUT | 0 | 15 | 19 | 19 | 23 | Red color output. It is a red color video signal output. |
| VSS | - | 16 | 20 | 20 | 24 | Digital ground. This ground pin is used to internal digital circuitry. |

## REPLACEMENT PARTS LIST

The components specified for Model DPlus74SB/DPlus74SB-BK
*** CRT BOARD ***

| Part No. for NPG | Part No. for NMV | DESCRIPTION | LOCATION | Q'TY | ALT | REMARK |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| HC006002 | 79PQ1104 | BEAD 3.5X4.7/T | B201 | 1 |  |  |
| HC005003 | 79PQ1594 | BEAD 3.5X8/T | B202 | 1 |  |  |
| 80000561 | 79PQ1232 | BEAD 3.5x6x0.8/T | B203 | 1 |  |  |
| 80000561 | 79PQ1232 | BEAD 3.5x6x0.8/T | B204 | 1 |  |  |
| GE210352 | 79PQ0245 | PLASTIC PEI/T 0.01u/50V J | C202 | 1 |  |  |
| GE210352 | 79PQ0245 | PLASTIC PEI/T 0.01u/50V J | C203 | 1 |  |  |
| GB910358 | 79PQ0242 | CERAMIC Z5V(F)/T 0.01u/50V Z | C205 | 1 |  |  |
| GA310655 | 79PQ0198 | ELECT 85oC/T 10u/50V M | C206 | 1 |  |  |
| GB910358 | 79PQ0242 | CERAMIC Z5V(F)/T 0.01u/50V Z | C207 | 1 |  |  |
| GA310655 | 79PQ0198 | ELECT 85oC/T 10u/50V M | C209 | 1 |  |  |
| GB910358 | 79PQ0242 | CERAMIC Z5V(F)/T 0.01u/50V Z | C210 | 1 |  |  |
| GB910358 | 79PQ0242 | CERAMIC Z5V(F)/T 0.01u/50V Z | C211 | 1 |  |  |
| GA410575 | 79PQ0213 | ELECT NP/T 1u/100V M | C212 | 1 |  |  |
| GAA10575 | 79PQ1744 | ELECT 850C/A 1u/100V M | C213 | 1 |  |  |
| GB910358 | 79PQ0242 | CERAMIC Z5V(F)/T $0.01 \mathrm{u} / 50 \mathrm{~V}$ Z | C230 | 1 |  |  |
| GB910358 | 79PQ0242 | CERAMIC Z5V(F)/T 0.01u/50V Z | C231 | 1 |  |  |
| GA410575 | 79PQ0213 | ELECT NP/T 1u/100V M | C232 | 1 |  |  |
| GAA10575 | 79PQ1744 | ELECT 850C/A 1u/100V M | C233 | 1 |  |  |
| GB910358 | 79PQ0242 | CERAMIC Z5V(F)/T 0.01u/50V Z | C250 | 1 |  |  |
| GB910358 | 79PQ0242 | CERAMIC Z5V(F)/T 0.01u/50V Z | C251 | 1 |  |  |
| GA410575 | 79PQ0213 | ELECT NP/T 1u/100V M | C252 | 1 |  |  |
| GAA10575 | 79PQ1744 | ELECT 850C/A 1u/100V M | C253 | 1 |  |  |
| GB656052 | 79PQ1087 | CERAMIC SL/T 56P/50V J | C270 | 1 |  |  |
| GA347625 | 79PQ0210 | ELECT 850C/T 47u/16V M | C272 | 1 |  |  |
| GB910358 | 79PQ0242 | CERAMIC Z5V(F)/T 0.01u/50V Z | C273 | 1 |  |  |
| GB7102F3 | 79PQ0234 | CERAMIC Y5P(B)/T 1000P/500V K | C274 | 1 |  |  |
| GB7222F3 | 79PQ1717 | CERAMIC Y5P(B)/T 2200P/500V K | C275 | 1 |  |  |
| GAA10575 | 79PQ1744 | ELECT 850C/A 1u/100V M | C277 | 1 |  |  |
| GB7102F3 | 79PQ0234 | CERAMIC Y5P(B)/T 1000P/500V K | C278 | 1 |  |  |
| GB910358 | 79PQ0242 | CERAMIC Z5V(F)/T 0.01u/50V Z | C279 | 1 |  |  |
| GB618152 | 79PQ2233 | CERAMIC SL/T 180P/50V J | C27A | 1 |  |  |
| GB618152 | 79PQ2233 | CERAMIC SL/T 180P/50V J | C27E | 1 |  |  |
| GB7102F3 | 79PQ0234 | CERAMIC Y5P(B)/T 1000P/500V K | C280 | 1 |  |  |
| GA310555 | 79PQ0196 | ELECT 850C/T 1u/50V M | C282 | 1 |  |  |
| GB210458 | 79PQ0228 | CERAMIC Y5V/T 0.1u/50V Z | C283 | 1 |  |  |
| GB7102F3 | 79PQ0234 | CERAMIC Y5P(B)/T 1000P/500V K | C284 | 1 |  |  |
| GB910358 | 79PQ0242 | CERAMIC Z5V(F)/T 0.01u/50V Z | C287 | 1 |  |  |
| GF210462 | 79PQ0253 | MEF CAP BOX $0.1 \mathrm{u} / 63 \mathrm{~V}$ J | C288 | 1 |  |  |
| GF210452 | 79PQ0752 | MEF CAP BOX 0.1u/50V J | C288 | OR |  |  |
| GA347625 | 79PQ0210 | ELECT 850C/T 47u/16V M | C289 | 1 |  |  |
| GB910358 | 79PQ0242 | CERAMIC Z5V(F)/T 0.01u/50V Z | C290 | 1 |  |  |
| GB622152 | 79PQ0230 | CERAMIC SL/T 220P/50V J | C292 | 1 |  |  |
| 72000623 | --- | NM17S CRT BOARD (M) | CRT BOARD | 1 |  |  |
| EJAC0018 | 79PQ1251 | DIODE/T 1A 1N4937 | D203 | 1 |  |  |
| 80000451 | 79PQ0043 | DIODE/T 1/2W 1SS83 | D212 | 1 |  |  |




| GB9332H8 | 79PQ1381 | CERAMIC Z5V(F)/T 3300P/1KV Z | C285 | 1 |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| GB8472H5 | 79PQ2450 | CERAMIC Z5U(E)/T 4700/1KV M | C286 | 1 |  |  |
| R0224070 | --- | SINGLE PIN 1P L=14mm 2.36 mm | CRT GND | 1 |  |  |
| 12600112 | --- | HEAT SINK (VIDEO) | FOR U204 | 1 |  |  |
| 14000041 | --- | SCREW (P-\#2CBRITS*3*8*15BF) | FOR U204 | 1 |  |  |
| HB000008 | 79PQ0276 | CHOKE COIL 100uH 8X10 | L201 | 1 |  |  |
| HB000008 | 79PQ0276 | CHOKE COIL 100uH 8X10 | L202 | 1 |  |  |
| 15201381 | --- | LABEL (S.NO.) | LABEL(S/N) | 1 |  |  |
| 80001991 | 79PQ0732 | RESISTOR FUSEABLE 1/4W 47 ohm J | R218 | 1 |  |  |
| 80001991 | 79PQ0732 | RESISTOR FUSEABLE 1/4W 47 ohm J | R238 | 1 |  |  |
| 80001991 | 79PQ0732 | RESISTOR FUSEABLE 1/4W 47 ohm J | R258 | 1 |  |  |
| R0224132 | --- | XH-BASE PIN 9P P=2.5mm | S201 | 1 |  |  |
| R0224129 | --- | BASE PIN 6P+HOUSING P=2.5mm | S202 | 1 |  |  |
| R0224130 | --- | BASE PIN 7P+HOUSING P=2.5mm | S203 | 1 |  |  |
| 80002391 | --- | SIGLE PIN L=15.5mm D=1.57mm | TP-G2 | 1 |  |  |
| 80010871 | 79PQ1729 | IC LM1269 | U201 | 1 |  |  |
| 80016551 | 79PQ2472 | OSD IC MTV030N-046 FOR E70,E75 | U202 | 1 |  |  |
| 80010891 | 79PQ1731 | IC LM2480 | U203 | 1 |  |  |
| 80010881 | 79PQ1730 | IC LM2469 | U204 | 1 |  |  |
| 80005711 | 79PQ1363 | IN CHANGE ISDW02S41 CRT SOCKET | CRT SOCKET | 1 |  |  |

## *** MAIN BOARD ***



| GAJ10825 | 79PQ2343 | ELECT CAP 105oC/T 1000u/16V M PF | C121 | OR |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| GB7101H3 | 79PQ1089 | CERAMIC Y5P(B)/T 100P/1KV K | C127 | 1 |  |  |
| GA347725 | 79PQ0851 | ELECT 850C/T 470u/16V M | C136 | 1 |  |  |
| GA347625 | 79PQ0210 | ELECT 850C/T 47u/16V M | C137 | 1 |  |  |
| GAH47725 | 79PQ1986 | ELECT CAP 105oC/T 470u/16V M TK | C139 | 1 |  |  |
| GAJ47725 | --- | ELECT CAP 105oC/T 470u/16V M PF | C139 | OR |  |  |
| GB747153 | 79PQ0238 | CERAMIC Y5P(B)/T 470P/50V K | C141 | 1 |  |  |
| GE210352 | 79PQ0245 | PLASTIC PEI/T 0.01u/50V J | C142 | 1 |  |  |
| GA322555 | 79PQ0202 | ELECT 85oC/T 2.2u/50V M | C143 | 1 |  |  |
| GA310655 | 79PQ0198 | ELECT 85oC/T 10u/50V M | C145 | 1 |  |  |
| GA310655 | 79PQ0198 | ELECT 850C/T 10u/50V M | C150 | 1 |  |  |
| GB910358 | 79PQ0242 | CERAMIC Z5V(F)/T 0.01u/50V Z | C301 | 1 |  |  |
| GB7331H3 | 79PQ0237 | CERAMIC Y5P(B)/T 330P/1KV K | C304 | 1 |  |  |
| GE210452 | 79PQ0915 | PLASTIC PEI/T 0.1u/50V J | C306 | 1 |  |  |
| GA310745 | 79PQ0848 | ELECT 85oC/T 100u/35V M | C308 | 1 |  |  |
| GA347555 | 79PQ0208 | ELECT 85oC/T 4.7u/50V M | C309 | 1 |  |  |
| GF215252 | 79PQ2238 | MEF CAP BOX 0.0015u/50V J | C312 | 1 |  |  |
| GF215262 | --- | MEF CAP BOX 0.0015u/63V J | C312 | OR |  |  |
| GA347655 | 79PQ1267 | ELECT 850C/T 47u/50V M | C313 | 1 |  |  |
| GF210452 | 79PQ0752 | MEF CAP BOX 0.1u/50V J | C314 | 1 |  |  |
| GF210462 | 79PQ0253 | MEF CAP BOX 0.1u/63V J | C314 | OR |  |  |
| GF210252 | 79PQ0748 | MEF CAP BOX 0.001u/50V J | C315 | 1 |  |  |
| GF210262 | 79PQ0749 | MEF CAP BOX 0.001u/63V J | C315 | OR |  |  |
| GE247352 | 79PQ2236 | PLASTIC PEI/T 0.047u/50V J | C316 | 1 |  |  |
| GE210452 | 79PQ0915 | PLASTIC PEI/T 0.1u/50V J | C317 | 1 |  |  |
| GE233252 | 79PQ0247 | PLASTIC PEI/T 0.0033u/50V J | C320 | 1 |  |  |
| GE233252 | 79PQ0247 | PLASTIC PEI/T 0.0033u/50V J | C327 | 1 |  |  |
| GA347455 | 79PQ0207 | ELECT 85oC/T 0.47u/50V M | C328 | 1 |  |  |
| GA347725 | 79PQ0851 | ELECT 85oC/T 470u/16V M | C330 | 1 |  |  |
| GB9103F8 | 79PQ1271 | CERAMIC Z5V(F)/T 0.01u/500V Z | C331 | 1 |  |  |
| GA347625 | 79PQ0210 | ELECT 850C/T 47u/16V M | C335 | 1 |  |  |
| GA310555 | 79PQ0196 | ELECT 850C/T 1u/50V M | C336 | 1 |  |  |
| GA310655 | 79PQ0198 | ELECT 850C/T 10u/50V M | C337 | 1 |  |  |
| GA310655 | 79PQ0198 | ELECT 850C/T 10u/50V M | C338 | 1 |  |  |
| GA322555 | 79PQ0202 | ELECT 850C/T 2.2u/50V M | C339 | 1 |  |  |
| GA310555 | 79PQ0196 | ELECT 85oC/T 1u/50V M | C340 | 1 |  |  |
| GB7471F3 | 79PQ0854 | CERAMIC Y5P(B)/T 470P/500V K | C341 | 1 |  |  |
| GE247352 | 79PQ2236 | PLASTIC PEI/T 0.047u/50V J | C343 | 1 |  |  |
| GA347585 | 79PQ0746 | ELECT 85oC/T 4.7u/250V M | C344 | 1 |  |  |
| GB210458 | 79PQ0228 | CERAMIC Y5V/T 0.1u/50V Z | C346 | 1 |  |  |
| GE210252 | 79PQ1272 | PLASTIC PEI/T 0.001u/50V J | C347 | 1 |  |  |
| GE222352 | 79PQ0246 | PLASTIC PEI/T 0.022u/50V J | C348 | 1 |  |  |
| GB210458 | 79PQ0228 | CERAMIC Y5V/T 0.1u/50V Z | C350 | 1 |  |  |
| GA310555 | 79PQ0196 | ELECT 85oC/T 1u/50V M | C352 | 1 |  |  |
| GB633152 | 79PQ0232 | CERAMIC SL/T 330P/50V J | C353 | 1 |  |  |
| GA347645 | 79PQ0212 | ELECT 850C/T 47u/35V M | C354 | 1 |  |  |
| GE210452 | 79PQ0915 | PLASTIC PEI/T 0.1u/50V J | C358 | 1 |  |  |
| GF215452 | 79PQ1098 | MEF CAP BOX 0.15u/50V J | C360 | 1 |  |  |
| GF215462 | 79PQ1587 | MEF CAP BOX 0.15u/63V J | C360 | OR |  |  |
| GE210452 | 79PQ0915 | PLASTIC PEI/T 0.1u/50V J | C361 | 1 |  |  |
| GF282252 | 79PQ2312 | MEF CAP BOX 0.0082u/50V J | C362 | 1 |  |  |
| GF282262 | 79PQ1941 | MEF CAP BOX 0.0082u/63V J | C362 | OR |  |  |



| EJAC0017 | 79PQ0068 | DIODE/T 1A 1N4936 | D132 | 1 |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| EJ044148 | 79PQ0065 | DIODE "T" 1N4148 | D303 | 1 |  |  |
| EJ044148 | 79PQ0065 | DIODE "T" 1N4148 | D304 | 1 |  |  |
| EJA05819 | 79PQ1644 | DIODE STKY/T 1A/40V 1N5819 | D305 | 1 |  |  |
| EJAC0017 | 79PQ0068 | DIODE/T 1A 1N4936 | D310 | 1 |  |  |
| EJ044148 | 79PQ0065 | DIODE "T" 1N4148 | D311 | 1 |  |  |
| EJAC0018 | 79PQ1251 | DIODE/T 1A 1N4937 | D312 | 1 |  |  |
| EJ044148 | 79PQ0065 | DIODE "T" 1N4148 | D313 | 1 |  |  |
| EJAC0018 | 79PQ1251 | DIODE/T 1A 1N4937 | D318 | 1 |  |  |
| EJ044148 | 79PQ0065 | DIODE "T" 1N4148 | D319 | 1 |  |  |
| EJ044148 | 79PQ0065 | DIODE "T" 1N4148 | D320 | 1 |  |  |
| EJAC0018 | 79PQ1251 | DIODE/T 1A 1N4937 | D321 | 1 |  |  |
| EJAC0018 | 79PQ1251 | DIODE/T 1A 1N4937 | D322 | 1 |  |  |
| EJ044148 | 79PQ0065 | DIODE "T" 1N4148 | D323 | 1 |  |  |
| EJAC0018 | 79PQ1251 | DIODE/T 1A 1N4937 | D324 | 1 |  |  |
| EJ044148 | 79PQ0065 | DIODE "T" 1N4148 | D325 | 1 |  |  |
| EJ044148 | 79PQ0065 | DIODE "T" 1N4148 | D327 | 1 |  |  |
| EJAC0018 | 79PQ1251 | DIODE/T 1A 1N4937 | D328 | 1 |  |  |
| EJAC0018 | 79PQ1251 | DIODE/T 1A 1N4937 | D329 | 1 |  |  |
| EJAC0018 | 79PQ1251 | DIODE/T 1A 1N4937 | D331 | 1 |  |  |
| EJ044148 | 79PQ0065 | DIODE "T" 1N4148 | D332 | 1 |  |  |
| EJ044148 | 79PQ0065 | DIODE "T" 1N4148 | D333 | 1 |  |  |
| EJ044148 | 79PQ0065 | DIODE "T" 1N4148 | D334 | 1 |  |  |
| EJ044148 | 79PQ0065 | DIODE "T" 1N4148 | D336 | 1 |  |  |
| EJ044148 | 79PQ0065 | DIODE "T" 1N4148 | D337 | 1 |  |  |
| EJ044148 | 79PQ0065 | DIODE "T" 1N4148 | D338 | 1 |  |  |
| R0319110 | --- | JUMPER WIRE AI/T 10mm | D339 | 1 |  |  |
| EJ044148 | 79PQ0065 | DIODE "T" 1N4148 | D340 | 1 |  |  |
| EJ044148 | 79PQ0065 | DIODE "T" 1N4148 | D341 | 1 |  |  |
| EJAC0018 | 79PQ1251 | DIODE/T 1A 1N4937 | D343 | 1 |  |  |
| EJ044148 | 79PQ0065 | DIODE "T" 1N4148 | D345 | 1 |  |  |
| EJAC0018 | 79PQ1251 | DIODE/T 1A 1N4937 | D403 | 1 |  |  |
| EJ044148 | 79PQ0065 | DIODE "T" 1N4148 | D601 | 1 |  |  |
| EJ044148 | 79PQ0065 | DIODE "T" 1N4148 | D604 | 1 |  |  |
| EJ044148 | 79PQ0065 | DIODE "T" 1N4148 | D605 | 1 |  |  |
| EJ044148 | 79PQ0065 | DIODE "T" 1N4148 | D60A | 1 |  |  |
| EJA05819 | 79PQ1644 | DIODE STKY/T 1A/40V 1N5819 | D702 | 1 |  |  |
| EJ044148 | 79PQ0065 | DIODE "T" 1N4148 | D703 | 1 |  |  |
| EJ044148 | 79PQ0065 | DIODE "T" 1N4148 | D704 | 1 |  |  |
| EJ044148 | 79PQ0065 | DIODE "T" 1N4148 | D705 | 1 |  |  |
| EJA05819 | 79PQ1644 | DIODE STKY/T 1A/40V 1N5819 | D706 | 1 |  |  |
| EJ044148 | 79PQ0065 | DIODE "T" 1N4148 | D709 | 1 |  |  |
| EJ044148 | 79PQ0065 | DIODE "T" 1N4148 | D70A | 1 |  |  |
| EJ044148 | 79PQ0065 | DIODE "T" 1N4148 | D70F | 1 |  |  |
| EJ044148 | 79PQ0065 | DIODE "T" 1N4148 | D710 | 1 |  |  |
| R0319110 | --- | JUMPER WIRE AI/T 20 mm | J1 | 1 |  |  |
| R0319110 | --- | JUMPER WIRE AI/T 10 mm | J10 | 1 |  |  |
| R0319110 | --- | JUMPER WIRE AI/T 10mm | J100 | 1 |  |  |
| R0319110 | --- | JUMPER WIRE AI/T 15 mm | J101 | 1 |  |  |
| R0319110 | --- | JUMPER WIRE AI/T 10mm | J102 | 1 |  |  |
| R0319110 | --- | JUMPER WIRE AI/T 20 mm | J103 | 1 |  |  |
| R0319110 | --- | JUMPER WIRE AI/T 12.5mm | J104 | 1 |  |  |




| R0319110 | --- | JUMPER WIRE AI/T 12.5 mm | J77 | 1 |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| R0319110 | --- | JUMPER WIRE AI/T 12.5 mm | J78 | 1 |  |  |
| R0319110 | --- | JUMPER WIRE AI/T 20 mm | J79 | 1 |  |  |
| R0319110 | --- | JUMPER WIRE AI/T 7.5 mm | J8 | 1 |  |  |
| R0319110 | --- | JUMPER WIRE AI/T 20 mm | J80 | 1 |  |  |
| R0319110 | --- | JUMPER WIRE AI/T 15 mm | J81 | 1 |  |  |
| R0319110 | --- | JUMPER WIRE AI/T 15 mm | J82 | 1 |  |  |
| R0319110 | --- | JUMPER WIRE AI/T 10 mm | J83 | 1 |  |  |
| R0319110 | --- | JUMPER WIRE AI/T 12.5 mm | J84 | 1 |  |  |
| R0319110 | --- | JUMPER WIRE AI/T 12.5 mm | J85 | 1 |  |  |
| R0319110 | --- | JUMPER WIRE AI/T 10 mm | J86 | 1 |  |  |
| R0319110 | --- | JUMPER WIRE AI/T 12.5 mm | J87 | 1 |  |  |
| R0319110 | --- | JUMPER WIRE AI/T 17.5 mm | J88 | 1 |  |  |
| R0319110 | --- | JUMPER WIRE AI/T 7.5 mm | J89 | 1 |  |  |
| R0319110 | --- | JUMPER WIRE AI/T 20 mm | J9 | 1 |  |  |
| R0319110 | --- | JUMPER WIRE AI/T 20 mm | J90 | 1 |  |  |
| R0319110 | --- | JUMPER WIRE AI/T 17.5 mm | J91 | 1 |  |  |
| R0319110 | --- | JUMPER WIRE AI/T 20 mm | J92 | 1 |  |  |
| R0319110 | --- | JUMPER WIRE AI/T 10 mm | J93 | 1 |  |  |
| R0319110 | --- | JUMPER WIRE AI/T 12.5 mm | J94 | 1 |  |  |
| R0319110 | --- | JUMPER WIRE AI/T 10 mm | J95 | 1 |  |  |
| R0319110 | --- | JUMPER WIRE AI/T 17.5 mm | J96 | 1 |  |  |
| R0319110 | --- | JUMPER WIRE AI/T 12.5 mm | J97 | 1 |  |  |
| 80000561 | 79PQ1232 | BEAD 3.5x6x0.8/T | J98 | 1 |  |  |
| R0319110 | --- | JUMPER WIRE AI/T 7.5 mm | J99 | 1 |  |  |
| R0319110 | --- | JUMPER WIRE AI/T 12.5 mm | JP1 | 1 |  |  |
| R0319110 | --- | JUMPER WIRE AI/T 12.5 mm | JP2 | 1 |  |  |
| R0319110 | --- | JUMPER WIRE AI/T 20 mm | JP6 | 1 |  |  |
| R0319110 | --- | JUMPER WIRE AI/T 7.5 mm | L308 | 1 |  |  |
| JB000761 | --- | N1702 MAIN BOARD PCB V01 | MAIN PCB | 1 |  |  |
| EAA18157 | 79PQ0734 | TR NPN 2SC1815GR TO-92(T) (T.P.S.) | Q105 | 1 |  |  |
| EAA09456 | 79PQ0056 | TR NPN 2SC945P TO-92(T) (N.P.S.) | Q105 | OR |  |  |
| EAA23285 | 79PQ2475 | TR NPN KSC2328A TO-92(T) | Q106 | 1 |  |  |
| EAA32055 | --- | TR NPN KTC2305-Y TO-92L/T | Q106 | OR |  |  |
| EAA22355 | 79PQ0058 | TR NPN 2SC2235Y TO-92(T) (TOSHIBA) | Q106 | OR |  |  |
| EAA18157 | 79PQ0734 | TR NPN 2SC1815GR TO-92(T) (T.P.S.) | Q107 | 1 |  |  |
| EAA09456 | 79PQ0056 | TR NPN 2SC945P TO-92(T) (N.P.S.) | Q107 | OR |  |  |
| EBA09281 | 79PQ1247 | TR PNP KSA 928A TO-92(T) (SAMSUNG) | Q108 | 1 |  |  |
| EBA10205 | 79PQ1685 | TR PNP 2SA1020Y TO-92(T) | Q108 | OR |  |  |
| 80002631 | 79PQ0997 | TR PNP KTA1273-Y TO-92L/T | Q108 | OR |  |  |
| EAA18157 | 79PQ0734 | TR NPN 2SC1815GR TO-92(T) (T.P.S.) | Q110 | 1 |  |  |
| EAA09456 | 79PQ0056 | TR NPN 2SC945P TO-92(T) (N.P.S.) | Q110 | OR |  |  |
| EBA04230 | 79PQ0061 | TR PNP BF423 TO-92(T)(T.P.) | Q112 | 1 |  |  |
| EAA23690 | 79PQ0059 | TR NPN PH2369 TO-92(T) (PHILIPS) | Q301 | 1 |  |  |
| EAA40020 | 79PQ0812 | TR NPN 2SC4002 TO-92(T) (SANYO) | Q303 | 1 |  |  |
| EBA04230 | 79PQ0061 | TR PNP BF423 TO-92(T)(T.P.) | Q305 | 1 |  |  |
| EAA18157 | 79PQ0734 | TR NPN 2SC1815GR TO-92(T) (T.P.S.) | Q306 | 1 |  |  |
| EAA09456 | 79PQ0056 | TR NPN 2SC945P TO-92(T) (N.P.S.) | Q306 | OR |  |  |
| EFA29610 | 79PQ1249 | TR 2SK2961 FET TOSHIBA | Q308 | 1 |  |  |
| EBA10157 | 79PQ0735 | TR PNP 2SA1015GR TO-92(T) (T.P.S.) | Q310 | 1 |  |  |
| EBA07336 | 79PQ0062 | TR PNP 2SA733P TO-92(T) (N.P.S.) | Q310 | OR |  |  |
| EBA09281 | 79PQ1247 | TR PNP KSA 928A TO-92(T) (SAMSUNG) | Q317 | 1 |  |  |


| EBA10205 | 79PQ1685 | TR PNP 2SA1020Y TO-92(T) | Q317 | OR |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 80002631 | 79PQ0997 | TR PNP KTA1273-Y TO-92L/T | Q317 | OR |  |  |
| EAA18157 | 79PQ0734 | TR NPN 2SC1815GR TO-92(T) (T.P.S.) | Q320 | 1 |  |  |
| EAA09456 | 79PQ0056 | TR NPN 2SC945P TO-92(T) (N.P.S.) | Q320 | OR |  |  |
| EAA09456 | 79PQ0056 | TR NPN 2SC945P TO-92(T) (N.P.S.) | Q321 | 1 |  |  |
| EAA18157 | 79PQ0734 | TR NPN 2SC1815GR TO-92(T) (T.P.S.) | Q321 | OR |  |  |
| EAA18157 | 79PQ0734 | TR NPN 2SC1815GR TO-92(T) (T.P.S.) | Q323 | 1 |  |  |
| EAA09456 | 79PQ0056 | TR NPN 2SC945P TO-92(T) (N.P.S.) | Q323 | OR |  |  |
| EAA18157 | 79PQ0734 | TR NPN 2SC1815GR TO-92(T) (T.P.S.) | Q324 | 1 |  |  |
| EAA09456 | 79PQ0056 | TR NPN 2SC945P TO-92(T) (N.P.S.) | Q324 | OR |  |  |
| EBA07336 | 79PQ0062 | TR PNP 2SA733P TO-92(T) (N.P.S.) | Q325 | 1 |  |  |
| EBA10157 | 79PQ0735 | TR PNP 2SA1015GR TO-92(T) (T.P.S.) | Q325 | OR |  |  |
| EBA07336 | 79PQ0062 | TR PNP 2SA733P TO-92(T) (N.P.S.) | Q326 | 1 |  |  |
| EBA10157 | 79PQ0735 | TR PNP 2SA1015GR TO-92(T) (T.P.S.) | Q326 | OR |  |  |
| EAA09456 | 79PQ0056 | TR NPN 2SC945P TO-92(T) (N.P.S.) | Q327 | 1 |  |  |
| EAA18157 | 79PQ0734 | TR NPN 2SC1815GR TO-92(T) (T.P.S.) | Q327 | OR |  |  |
| EAA09456 | 79PQ0056 | TR NPN 2SC945P TO-92(T) (N.P.S.) | Q329 | 1 |  |  |
| EAA18157 | 79PQ0734 | TR NPN 2SC1815GR TO-92(T) (T.P.S.) | Q329 | OR |  |  |
| EAA09456 | 79PQ0056 | TR NPN 2SC945P TO-92(T) (N.P.S.) | Q401 | 1 |  |  |
| EAA18157 | 79PQ0734 | TR NPN 2SC1815GR TO-92(T) (T.P.S.) | Q401 | OR |  |  |
| EAA18157 | 79PQ0734 | TR NPN 2SC1815GR TO-92(T) (T.P.S.) | Q603 | 1 |  |  |
| EAA09456 | 79PQ0056 | TR NPN 2SC945P TO-92(T) (N.P.S.) | Q603 | OR |  |  |
| EBA10157 | 79PQ0735 | TR PNP 2SA1015GR TO-92(T) (T.P.S.) | Q604 | 1 |  |  |
| EBA07336 | 79PQ0062 | TR PNP 2SA733P TO-92(T) (N.P.S.) | Q604 | OR |  |  |
| EAA18157 | 79PQ0734 | TR NPN 2SC1815GR TO-92(T) (T.P.S.) | Q605 | 1 |  |  |
| EAA09456 | 79PQ0056 | TR NPN 2SC945P TO-92(T) (N.P.S.) | Q605 | OR |  |  |
| EAA18157 | 79PQ0734 | TR NPN 2SC1815GR TO-92(T) (T.P.S.) | Q606 | 1 |  |  |
| EAA09456 | 79PQ0056 | TR NPN 2SC945P TO-92(T) (N.P.S.) | Q606 | OR |  |  |
| EBA07336 | 79PQ0062 | TR PNP 2SA733P TO-92(T) (N.P.S.) | Q701 | 1 |  |  |
| EBA10157 | 79PQ0735 | TR PNP 2SA1015GR TO-92(T) (T.P.S.) | Q701 | OR |  |  |
| EBA07336 | 79PQ0062 | TR PNP 2SA733P TO-92(T) (N.P.S.) | Q703 | 1 |  |  |
| EBA10157 | 79PQ0735 | TR PNP 2SA1015GR TO-92(T) (T.P.S.) | Q703 | OR |  |  |
| EAA12133 | 79PQ0057 | TR NPN 2SC1213AC TO-92(T) | Q704 | 1 |  |  |
| EAA20015 | --- | TR NPN KSC2001Y TO-92(T) (SAMSUNG | Q704 | OR |  |  |
| EAA02005 | --- | TR NPN KTC200-Y TO-92(T) (KEC) | Q704 | OR |  |  |
| FA330684 | 79PQ0156 | CARBON 1/2W(T) 5\% 680Kohm | R101 | 1 |  |  |
| FA040331 | 79PQ1020 | CARBON 1/8W(T) 5\% 3300hm | R102 | 1 |  |  |
| FA240330 | 79PQ1645 | CARBON 1/4W(T) 5\% 33 ohm | R104 | 1 |  |  |
| FA240564 | 79PQ0328 | CARBON 1/4W(T) 5\% 560Kohm | R107 | 1 |  |  |
| FA240334 | 79PQ1034 | CARBON 1/4W(T) 5\% 330Kohm | R108 | 1 |  |  |
| FA040470 | 79PQ0322 | CARBON 1/8W(T) 5\% 47ohm | R109 | 1 |  |  |
| FA040103 | 79PQ0083 | CARBON 1/8W(T) 5\% 10Kohm | R110 | 1 |  |  |
| FA040102 | 79PQ0082 | CARBON 1/8W(T) 5\% 1Kohm | R112 | 1 |  |  |
| FA040272 | 79PQ0100 | CARBON 1/8W(T) 5\% 2.7Kohm | R113 | 1 |  |  |
| FA330104 | 79PQ0826 | CARBON 1/2W(T) 5\% 100Kohm | R114 | 1 |  |  |
| FA040470 | 79PQ0322 | CARBON 1/8W(T) 5\% 47ohm | R115 | 1 |  |  |
| FA240271 | 79PQ0132 | CARBON 1/4W(T) 5\% 270ohm | R116 | 1 |  |  |
| FA240390 | 79PQ1372 | CARBON 1/4W(T) 5\% 39ohm | R117 | 1 |  |  |
| FA240203 | 79PQ0128 | CARBON 1/4W(T) 5\% 20Kohm | R118 | 1 |  |  |
| FA040224 | 79PQ0097 | CARBON 1/8W(T) 5\% 220Kohm | R119 | 1 |  |  |
| FA330104 | 79PQ0826 | CARBON 1/2W(T) 5\% 100Kohm | R120 | 1 |  |  |
| FA040223 | 79PQ0096 | CARBON 1/8W(T) 5\% 22Kohm | R121 | 1 |  |  |





| FA040101 | 79PQ0081 | CARBON 1/8W(T) 5\% 100ohm | R761 | 1 |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| FA040101 | 79PQ0081 | CARBON 1/8W(T) 5\% 1000hm | R762 | 1 |  |  |
| FA330621 | 79PQ2441 | CARBON 1/2W(T) 5\% 6200hm | R768 | 1 |  |  |
| FA040471 | 79PQ0113 | CARBON 1/8W(T) 5\% 470ohm | R771 | 1 |  |  |
| R0319110 | --- | JUMPER WIRE AI/T 5 mm | VR102 | 1 |  |  |
| R0319110 | --- | JUMPER WIRE AI/T 5mm | VR103 | 1 |  |  |
| EKA01201 | 79PQ0077 | ZEN DIODE 1/2W(T) HZS12A2 (HITACHI) | ZD102 | 1 |  |  |
| EKC01201 | 79PQ0816 | ZEN DIODE 1/2W(T) BZX79F12 (PHLIPS) | ZD102 | OR |  |  |
| EKA0180B | 79PQ0078 | ZEN DIODE 1/2W(T) HZS 18-2 (HITACHI) | ZD106 | 1 |  |  |
| EKC0180B | 79PQ0817 | ZEN DIODE 1/2W(T) BZX79F18 (PHILIPS | ZD106 | OR |  |  |
| EKA00507 | 79PQ0075 | ZEN DIODE 1/2W(T) HZS5C2 (HITACHI) | ZD701 | 1 |  |  |
| EKC00507 | 79PQ0814 | ZEN DIODE 1/2W(T) BZX79F5V1 (PHILIP | ZD701 | OR |  |  |
| EKA00507 | 79PQ0075 | ZEN DIODE 1/2W(T) HZS5C2 (HITACHI) | ZD702 | 1 |  |  |
| EKC00507 | 79PQ0814 | ZEN DIODE 1/2W(T) BZX79F5V1 (PHILIP | ZD702 | OR |  |  |
| EKA00507 | 79PQ0075 | ZEN DIODE 1/2W(T) HZS5C2 (HITACHI) | ZD703 | 1 |  |  |
| EKC00507 | 79PQ0814 | ZEN DIODE 1/2W(T) BZX79F5V1 (PHILIP | ZD703 | OR |  |  |
| EKA00507 | 79PQ0075 | ZEN DIODE 1/2W(T) HZS5C2 (HITACHI) | ZD704 | 1 |  |  |
| EKC00507 | 79PQ0814 | ZEN DIODE 1/2W(T) BZX79F5V1 (PHILIP | ZD704 | OR |  |  |
| EKA00601 | 79PQ2477 | ZEN DIODE 1/2W(T) HZS6A2 HITACHI | ZD705 | 1 |  |  |
| EKA00607 | 79PQ0292 | ZEN DIODE 1/2W(T) HZS6C2 (HITACHI) | ZD706 | 1 |  |  |
| EKC00607 | 79PQ0815 | ZEN DIODE 1/2W(T) BZX79F6V2 (PHILIP | ZD706 | OR |  |  |
| HC006002 | 79PQ1104 | BEAD 3.5X4.7/T | B309 | 1 |  |  |
| HC006002 | 79PQ1104 | BEAD 3.5X4.7/T | B32A | 1 |  |  |
| GB7102H3 | 79PQ0235 | CERAMIC Y5P(B)/T 1000P/1KV K | C334 | 1 |  |  |
| GE210352 | 79PQ0245 | PLASTIC PEI/T 0.01u/50V J | C363 | 1 |  |  |
| EJA00018 | 79PQ1526 | DIODE 1A UF4006 | D31A | 1 |  |  |
| EJA00160 | 79PQ1250 | DIODE STKY/T 1A/60V SB160 | D330 | 1 |  |  |
| EJAE0001 | 79PQ0069 | DIODE/T 1A SR106 | D330 | OR |  |  |
| EJA00160 | 79PQ1250 | DIODE STKY/T 1A/60V SB160 | D346 | 1 |  |  |
| EJAE0001 | 79PQ0069 | DIODE/T 1A SR106 | D346 | OR |  |  |
| FA040154 | 79PQ0091 | CARBON 1/8W(T) 5\% 150Kohm | R319 | 1 |  |  |
| FB242742 | 79PQ2454 | MATAL 1/4W (T)5\% 27.4Kohm | R344 | 1 |  |  |
| FB245361 | 79PQ2224 | METAL 1/4W (T) 1\%5.36Kohm | R348 | 1 |  |  |
| FA240102 | 79PQ0125 | CARBON 1/4W(T) 5\% 1Kohm | R350 | 1 |  |  |
| FB243302 | 79PQ1053 | METAL 1/4W(T) 1\% 33Kohm | R35E | 1 |  |  |
| FB242493 | 79PQ2498 | METAL 1/4W(T) 1\% 249Kohm | R366 | 1 |  |  |
| FB245490 | 79PQ2269 | METAL 1/4W(T) 1\% 549ohm | R388 | 1 |  |  |
| FA040103 | 79PQ0083 | CARBON 1/8W(T) 5\% 10Kohm | R705 | 1 |  |  |
| R0319110 | --- | JUMPER WIRE AI/T 5mm | VR307 | 1 |  |  |
| 14000051 | --- | SCREW (\#2CBRITS*4*8*15BF) | AC SOCKET | 2 |  |  |
| 80000991 | 79PQ1233 | BEAD WBR6H-3T-R7K-B5 | B102 | 1 |  |  |
| GJ033404 | 79PQ2481 | SAFETY X-CAP 0.33u/275V M(ISKRA) | C101 | 1 |  |  |
| GJ033407 | --- | SAFETY X-CAP 0.33u/275V M(OKAYA) | C101 | OR |  |  |
| GJ033405 | --- | SAFETY X-CAP 0.33u/275V M(PHILIPS) | C101 | OR |  |  |
| GJ033409 | --- | SAFETY X-CAP 0.33u/275V M(PILKOR) | C101 | OR |  |  |
| GJ033406 | --- | SAFETY X-CAP 0.33u/275V M(EPCOS) | C101 | OR |  |  |
| GJC102E5 | 79PQ1982 | SAFETY Y-CAP/D 1000P/400V M | C102 | 1 |  |  |
| GJH102E5 | 79PQ0274 | SAFETY Y-CAP/S 1000P/400V M | C103 | 1 |  |  |
| GJH102E5 | 79PQ0274 | SAFETY Y-CAP/S 1000P/400V M | C104 | 1 |  |  |
| GKA227E5 | 79PQ1103 | POWER ELECT 85oC 220u/400V M | C105 | 1 |  |  |
| GAI10775 | 79PQ1984 | ELECT 105oC/A 100u/100V M TK | C120 | 1 |  |  |
| 80011091 | --- | ELECT LOW ESR 100u/100V M 10X30(10 | C120 | OR |  |  |


| GA310815 | 79PQ1658 | ELECT 85oC/T 1000u/10V M | C122 | 1 |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| GAI10775 | 79PQ1984 | ELECT 105oC/A 100u/100V M TK | C138 | 1 |  |  |
| 80011091 | --- | ELECT LOW ESR 100u/100V M 10X30(10 | C138 | OR |  |  |
| GJH102E5 | 79PQ0274 | SAFETY Y-CAP/S 1000P/400V M | C146 | 1 |  |  |
| GJH102E5 | 79PQ0274 | SAFETY Y-CAP/S 1000P/400V M | C154 | 1 |  |  |
| GFC622J2 | 79PQ1987 | PLASTIC PPS/A 6200P/2KV J | C318 | 1 |  |  |
| GFB22482 | 79PQ0889 | PLASTIC MPP/A 0.22u/250V J | C325 | 1 |  |  |
| GFA15482 | 79PQ0262 | PLASTIC MPE/A 0.15u/250V J | C329 | 1 |  |  |
| GFA10572 | 79PQ2451 | PLASTIC MPE/A 1u/100V J | C333 | 1 |  |  |
| GFA10582 | 79PQ0261 | PLASTIC MPE/A 1u/250V J | C333 | OR |  |  |
| GFB15482 | 79PQ0265 | PLASTIC MPP/A 0.15u/250VJ | C351 | 1 |  |  |
| GFD47482 | 79PQ2271 | PLASTIC MPPS/A 0.47u/250V J (MYLAR) | C373 | 1 |  |  |
| GB210458 | 79PQ0228 | CERAMIC Y5V/T 0.1u/50V Z | C712 | 1 |  |  |
| 80003561 | 79PQ1238 | DIODE 600V/1.6A RG2A SANKEN | D110 | 1 |  |  |
| 80003581 | --- | DIODE 600V/2A UF2005 CHENMKO | D110 | OR |  |  |
| 12800021 | 79PQ1335 | HEAT SINK 22.5*56.5*1.3t | D111 | 1 |  |  |
| 80011291 | 79PQ2036 | DIODE/A 3A/400V RG4 | D111 | 1 |  |  |
| 80003551 | 79PQ1237 | DIODE 200V/1.6A RG2Z SANKEN | D112 | 1 |  |  |
| 80003571 | --- | DIODE 200V/2A UF2003 CHENMKO | D112 | OR |  |  |
| 80003551 | 79PQ1237 | DIODE 200V/1.6A RG2Z SANKEN | D113 | 1 |  |  |
| 80003571 | --- | DIODE 200V/2A UF2003 CHENMKO | D113 | OR |  |  |
| EJ044148 | 79PQ0065 | DIODE "T" 1N4148 | D115 | 1 |  |  |
| 80003551 | 79PQ1237 | DIODE 200V/1.6A RG2Z SANKEN | D118 | 1 |  |  |
| 80003571 | --- | DIODE 200V/2A UF2003 CHENMKO | D118 | OR |  |  |
| EJ044148 | 79PQ0065 | DIODE "T" 1N4148 | D126 | 1 |  |  |
| 14300071 | --- | SCREW (PL-CPTS*3*8*15BF) | D307 | 1 |  |  |
| 80016491 | 79PQ2437 | DIODE/A BY329X-1500S | D307 | 1 |  |  |
| 80001171 | --- | DIODE/A 5TUZ47C (TOSHIBA) | D307 | OR |  |  |
| 80009541 | 79PQ1631 | DIODE FAGOR FUF5406 (A+K) | D308 | 1 |  |  |
| 80001131 | 79PQ0794 | DIODE/A 2A/600V RG4A | D308 | OR |  |  |
| 80009261 | 79PQ1958 | DIODE/A RP3F(A+K) SANKEN | D316 | 1 |  |  |
| 80010981 | --- | DIODE TOSHIBA 3TH41(A+K) | D316 | OR |  |  |
| 80011471 | --- | DIODE FUJI ERD07-15L(A+K) | D316 | OR |  |  |
| EJ000215 | 79PQ2487 | DIODE 0.1A/1400V PR 1400 | D326 | 1 |  |  |
| 80003561 | 79PQ1238 | DIODE 600V/1.6A RG2A SANKEN | D335 | 1 |  |  |
| 80001521 | 79PQ0799 | FUSE 3.15A/250V 50T T3.15A | F101 | 1 |  |  |
| 18000481 | --- | EDGE SADDLE (BLACK) (SB-31B) | FOR CHASSING | 2 |  |  |
| 18000561 | --- | MINI CLIP (WC-15A) | FOR FBT H.S | 1 |  |  |
| R0180028 | 79PQ1198 | FUSE HOLDER 5X20mm | FOR FUSE | 2 |  |  |
| 80000781 | --- | SINGLE PIN L=12.0 D=1.5 | FOR TH101 | 2 |  |  |
| JD010040 | 79PQ1105 | IC SOCKET 40P | FOR U701 | 1 |  |  |
| 12300121 | --- | PLATE SHIELDING (IC) | FOR U701 | 1 |  |  |
| 12300241 | --- | PLATE SHIELDING (EEPROM) | FOR U702 | 1 |  |  |
| HA030010 | 79PQ0275 | EMI FILTER COIL 20.45X10.2X10 | G2,G4 WIRE | 2 |  |  |
| 80003511 | --- | WIRE GND 70mm Y/G 1015 18AWG | L100 | 1 |  |  |
| 80000111 | 79PQ0019 | LINE FILTER ET24 10mH MIN | L101 | 1 |  |  |
| HB000015 | 79PQ0277 | LINE FILTER UU10.5 1mH | L102 | 1 |  |  |
| 80009291 | 79PQ1630 | H-CENTER CHOKE | L301 | 1 |  |  |
| HB000019 | 79PQ0279 | CHOKE COIL 130uH 18X20 | L304 | 1 |  |  |
| 15201381 | --- | LABEL (S.NO.) | LABEL(S/N) | 1 |  |  |
| 80000131 | 79PQ0021 | LED L-59GH/1GYC | LED701 | 1 |  |  |
| 18000331 | --- | CABLE CLIP(WC-13T) | LW101 | 1 |  |  |



| 80000251 | 79PQ0028 | TACT SW 1P 100G+-50 | SW705 | 1 |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 80000251 | 79PQ0028 | TACT SW 1P 100G+-50 | SW706 | 1 |  |
| 80000251 | 79PQ0028 | TACT SW 1P 100G+-50 | SW707 | 1 |  |
| 80011211 | 79PQ2206 | POWER X'FM ERL35 500uH FE700+ | T101 | 1 | B Ver. |
| 80000281 | 79PQ0030 | H.DRIVE X'FM 4.5mH El-19 | T302 | 1 |  |
| 80000801 | 79PQ0311 | THERMISTOR NTCR SCK054 13.3mm | TH101 | 1 |  |
| 80005821 | 79PQ1365 | THERMISTOR PTCR 4.5ohm | TH102 | 1 |  |
| R0224074 | --- | SINGLE PIN L=11.5 D=1.0 | TP-1 | 1 |  |
| R0224077 | --- | BASE PIN 1P 1.55mm | TPC | 1 |  |
| DD002600 | 79PQ0050 | IC LINEAR KA3842A 8P | U101 | 1 |  |
| 80010251 | 79PQ2205 | OP AMP LM358 / KIA358 | U301 | 1 |  |
| 80012941 | 79PQ2208 | PHILIPS IC TDA 4857 | U302 | 1 |  |
| 12800282 | --- | HEAT SINK 44*27*50 | U401 | 1 |  |
| 14000041 | --- | SCREW (P-\#2CBRITS*3*8*15BF) | U401 | 1 |  |
| 80001041 | 79PQ0793 | IC TDA8172 (N.S,SGS) | U401 | 1 |  |
| 80016251 | 79PQ2435 | E70, E75 MCU MASK | U701 | 1 |  |
| 80016261 | --- | N1702 MTP WT62P2 | U701 | OR |  |
| 80009941 | 79PQ2277 | ATMEL E2ROM AT24C08B | U702 | 1 |  |
| 80010311 | --- | MICROCHIP E²ROM 24LC08 | U702 | OR |  |
| 80016501 | --- | CATALYST EEROM CAT24WC08P | U702 | OR |  |
| 80010801 | --- | NM17S WIRE A'SSY | WIRE ASSY | 1 |  |
| EM012004 | 79PQ1735 | X'TAL 49U 12MHz | X701 | 1 |  |
| GED622M2 | 79PQ1988 | PLASTIC PPN/A 6200P/800V J | C319 | 1 |  |
| GFD274E2 | 79PQ2079 | PLASTIC 378/A 0.27u/400V J (PILKOR) | C332 | 1 |  |
| GFD27482 | --- | PLASTIC PMM/A 0.27u/250V J (MYLAR) | C332 | OR |  |
| GFA10382 | 79PQ0860 | PLASTIC MPE/A 0.01u/250V J | C345 | 1 |  |
| GFB68482 | 79PQ0267 | PLASTIC MPP/A 0.68u/250V J | C355 | 1 |  |
| GFB24482 | 79PQ2241 | PLASTIC MPP/A 0.24u/250V J | C356 | 1 |  |
| 80005801 | --- | DY WIRE | DY WIRE | 1 |  |
| 80011061 | 79PQ2179 | N0701F LINEARITY CHOKE 76uH | L302 | 1 |  |
| HB000019 | 79PQ0279 | CHOKE COIL 130uH 18X20 | L303 | 1 |  |
| 80010401 | 79PQ1702 | N0701F LINEARITY COIL | L307 | 1 |  |
| 12600371 | --- | HEAT SINK (FBT) TCO | Q307 | 1 |  |
| FB470119 | 79PQ2073 | MOF 1W/M(A) 5\% 1.10hm | R415 | 1 |  |
| 80009121 | --- | WIRE 6P-2P | ROTATION WIRE | 1 |  |
| R0224611 | --- | BASE PIN 3P+HOUSING P=2.5mm | S701 | 1 |  |
| 80015631 | 79PQ2286 | T301 FBT DV17H1 MERITON | T301 | 1 |  |
| 80009691 | 79PQ1632 | N0501 D.F X'FM El-19(1:7.5) | T303 | 1 |  |

*** SET ASSY *** DPlus74SB (White Cabinet)

| AC0M05MM | 79PQ2629 | CRT BOARD INSERT |  |  |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| AM0M05MM | 79PQ2630 | MAIN BOARD INSERT |  |  |  | A,B |
| AM0M06MM | 79PQ2631 | MAIN BOARD INSERT |  |  |  | R |
| 14000071 | --- | SCREW (PL-CPTS*3*8*15BF) | BRACKET CORD | 1 |  |  |
| 80016931 | $79 P Q 2473$ | N1702 SINGNAL CABLE | CABLE | 1 |  |  |
| 17000921 | --- | CRT BARRIER | CRT UPPER DEG | 1 |  |  |
| 80016351 | 79PQ2471 | DEGAUSSING COIL N1702 | DEGUESSING CQ | 1 |  |  |
| 14000021 | --- | SCREW (\#2CBRITS*4*12*15BF) | FOR BACK | 2 |  |  |
| 17000841 | 79PQ2430 | CUSHION PIECE (SPONG) | FOR BACK | 1 |  |  |
| 14000021 | --- | SCREW (\#2CBRITS*4*12*15BF) | FOR CHASSIS | 2 |  |  |
| 12000651 | BRACKET(CORD) | FOR CHASSIS | 1 |  |  |  |


| 14600191 | --- | SCREW SPECIAL (5*25*WASHER=16) | FOR CRT | 4 |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 18000371 | --- | FIXED CABLE CLIP(GL-115A) | FOR DEGUES | 2 |  |
| 14300031 | --- | SCREW (PL-CPIMS**10*15BF) | FOR EMI GROUN | 1 |  |
| 18000061 | --- | ANODE CLAMPER | FOR FBT WIRE | 2 |  |
| 18000321 | --- | EDGE SADDLE(SB-31) | FOR FBT WIRE | 1 |  |
| 14000071 | --- | SCREW (PL-CPTS*3**15BF) | FOR GROUND | 2 |  |
| 14000071 | --- | SCREW (PL-CPTS*3*8*15BF) | FOR MPCB | 8 |  |
| 18000581 | --- | PCB SUPPORT | FOR MPCB | 4 |  |
| 18000551 | --- | EXTENDING SHIFT | FOR P/W SW | 1 |  |
| 12300721 | --- | PLATE SHIELDING (VIDEO) | FOR VIDEO BOA月 | 1 |  |
| 80000031 | --- | GND WIRE 18AWG L=130mm | GND WIRE2 | 1 |  |
| 80016941 | --- | WIRE GND 1015 18AWG L=200mm BLAQ | GND WIRE3 | 1 |  |
| 80016881 | --- | N1702 TCO WIRE L=660mm | TCO WIRE | 1 |  |
| 17000322 | --- | CABLE TIES(GT-80M) | TIE | 10 |  |
| 12000641 | 79PQ2424 | CHASSIS BASE |  | 1 |  |
| 15200031 | 79PQ0961 | LABEL (REV.) |  | 1 |  |
| 80001631 | 79PQ0703 | POWER CORD 3P 1.8 NON-SHIELD COL | POWER CORD | 1 | A |
| 80001651 | 79PQ0869 | POWER CORD 3P 1.8M EUROPE | POWER CORD | 1 | B |
| 80002931 | 79PQ2243 | POWER CORD 3P 1.8M AUSTRALIA N-S | POWER CORD | 1 | R |
| --- | --- | CARTON BOX DP74(A VER.) |  | 1 | A |
| 13201781 | 79PQ2640 | CARTON BOX DP74(B/R VER.) |  | 1 | B,R |
| --- | --- | OWNERS MANUAL DP74 A VER |  | 1 | A |
| 15501051 | 79PQ2641 | OWNERS MANUAL DP74 B/R VER |  | 1 | B,R |
| 80015091 | 79PQ2285 | MITSUBISHI CRT M41LRY61X22 | CRT | 1 | A, B |
| JG071301 | 79PQ2499 | CRT M41LRY61X22R MITSUBISHI | CRT | 1 | R |
| 17000831 | --- | CRT PAD (T=2.5mm) O.D=16, I.D=6.8 | FOR CRT | 4 |  |
| 17000981 | --- | MALAR SHEET (MIT. TUBE) | FOR CRT | 1 |  |
| 10102331 | 79PQ2642 | CABINET FRONT ASSY,(MC-0807) |  | 1 |  |
| 10102271 | 79PQ2643 | CABINET BACK (MITSUBISHI) (PC+ABS), | ,(MC-0807) | 1 |  |
| 80016891 | --- | E75 MITSUBISHI CRT GND WIRE | GND WIRE | 1 |  |
| 11000991 | 79PQ2466 | REVOLVING STAND ASSY |  | 1 |  |
| 13400841 | 79PQ2484 | POLYLON(B) |  | 1 |  |
| 13400851 | 79PQ2485 | POLYLON(T) |  | 1 |  |
| 13700021 | 79PQ0958 | BAG POLYETHYLENE (270*370) |  | 1 |  |
| 13700031 | 79PQ2252 | BAG POLYETHYLENE (150*370) |  | 1 |  |
| 13700071 | 79PQ0959 | PE BAG (500*480*850+WARNING) |  | 1 |  |
| 15200541 | 79PQ2616 | LABEL WARNING (29KV) |  | 1 |  |
| 15201331 | 79PQ2633 | LABEL WARNING(28Kv,1000uA) |  | 1 |  |
| 15201621 | 79PQ2486 | LABEL CARTON (NE) |  | 1 | B.R |
| 19700081 | 79PQ2644 | INSTRUCTION CD-ROM FE771 |  | 1 | B,R |
| --- | --- | NAME PLATE INSTRUCTION DP74A |  | 1 | A |
| 15001491 | 79PQ2645 | NAME PLATE INSTRUCTION DP74B/R |  | 1 | B,R |
| 15200281 | 79PQ0962 | LABEL,SERIAL BARCODE (A) |  | 1 | A |
| 15201651 | 79PQ2646 | LABEL SERIAL BARCODE(B) |  | 1 | B,R |
| 15200491 | 79PQ0966 | LABEL (MANUFACTURE, NPG) |  | 1 |  |
| 15200241 | 79PQ2634 | LABEL (D8,CYAN) |  | 1 |  |

*** SET ASSY *** DPlus74SB-BK(BLACK Cabinet)

| AC0M05MM | 79PQ2629 | CRT BOARD INSERT |  |  |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| AM0M05MM | 79PQ2630 | MAIN BOARD INSERT |  |  |  |  |
| 14000071 | -- | SCREW (PL-CPTS* ${ }^{*} 8^{* 15 B F) ~}$ | BRACKET CORD | 1 |  |  |
| 80016931 | $79 P Q 2473$ | N1702 SINGNAL CABLE | CABLE | 1 |  |  |


| 17000921 | --- | CRT BARRIER | CRT UPPER DEG | 1 |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 80016351 | 79PQ2471 | DEGAUSSING COIL N1702 | DEGUESSING CQ | 1 |  |  |
| 14000021 | --- | SCREW (\#2CBRITS**12*15BF) | FOR BACK | 2 |  |  |
| 17000841 | 79PQ2430 | CUSHION PIECE (SPONG) | FOR BACK | 1 |  |  |
| 14000021 | --- | SCREW (\#2CBRITS**12*15BF) | FOR CHASSIS | 2 |  |  |
| 12000651 | --- | BRACKET(CORD) | FOR CHASSIS | 1 |  |  |
| 14600191 | --- | SCREW SPECIAL (5*25*WASHER=16) | FOR CRT | 4 |  |  |
| 18000371 | --- | FIXED CABLE CLIP(GL-115A) | FOR DEGUES | 2 |  |  |
| 14300031 | --- | SCREW (PL-CPIMS**10*15BF) | FOR EMI GROUN | 1 |  |  |
| 18000061 | --- | ANODE CLAMPER | FOR FBT WIRE | 2 |  |  |
| 18000321 | --- | EDGE SADDLE(SB-31) | FOR FBT WIRE | 1 |  |  |
| 14000071 | --- | SCREW (PL-CPTS*3*8*15BF) | FOR GROUND | 2 |  |  |
| 14000071 | --- | SCREW (PL-CPTS*3*8*15BF) | FOR MPCB | 8 |  |  |
| 18000581 | --- | PCB SUPPORT | FOR MPCB | 4 |  |  |
| 18000551 | --- | EXTENDING SHIFT | FOR P/W SW | 1 |  |  |
| 12300721 | --- | PLATE SHIELDING (VIDEO) | FOR VIDEO BOAF | 1 |  |  |
| 80000031 | --- | GND WIRE 18AWG L=130mm | GND WIRE2 | 1 |  |  |
| 80016941 | --- | WIRE GND 1015 18AWG L=200mm BLAC | GND WIRE3 | 1 |  |  |
| 80016881 | --- | N1702 TCO WIRE L=660mm | TCO WIRE | 1 |  |  |
| 17000322 | --- | CABLE TIES(GT-80M) | TIE | 10 |  |  |
| 12000641 | 79PQ2424 | CHASSIS BASE |  | 1 |  |  |
| 15200031 | 79PQ0961 | LABEL (REV.) |  | 1 |  |  |
| 80001631 | 79PQ0703 | POWER CORD 3P 1.8 NON-SHIELD COL | POWER CORD | 1 |  |  |
| 80016891 | --- | E75 MITSUBISHI CRT GND WIRE | GND WIRE | 1 |  |  |
| 13201871 | 79PQ2647 | CARTON BOX DP74(A VER.) |  | 1 |  |  |
| 15501101 | 79PQ2648 | OWNERS MANUAL DP74 A VER |  | 1 |  |  |
| 80015091 | 79PQ2285 | MITSUBISHI CRT M41LRY61X22 | CRT | 1 |  |  |
| 17000831 | --- | CRT PAD ( $T=2.5 \mathrm{~mm}$ ) O.D=16, I.D=6.8 | FOR CRT | 4 |  |  |
| 17000981 | --- | MALAR SHEET (MIT. TUBE) | FOR CRT | 1 |  |  |
| 10102531 | 79PQ2649 | CABINET FRONT ASSY,(MC-0735) |  | 1 |  |  |
| 10102521 | 79PQ2650 | CABINET BACK (MITSUBISHI) (PC+ABS), | ,(MC-0735),BK | 1 |  |  |
| 11001021 | 79PQ2651 | REVOLVING STAND ASSY(MC-0735) |  | 1 |  |  |
| 13700021 | 79PQ0958 | BAG POLYETHYLENE (270*370) |  | 1 |  |  |
| 13700031 | 79PQ2252 | BAG POLYETHYLENE (150*370) |  | 1 |  |  |
| 13700071 | 79PQ0959 | PE BAG (500*480*850+WARNING) |  | 1 |  |  |
| 15001481 | 79PQ2652 | NAME PLATE INSTRUCTION DP74A |  | 1 |  |  |
| 15201331 | 79PQ2633 | LABEL WARNING(28Kv,1000uA) |  | 1 |  |  |
| 15201541 | 79PQ2632 | LABEL WARNING(28Kv) |  | 1 |  |  |
| 13400751 | 79PQ2427 | POLYLON(B) |  | 1 |  |  |
| 13400741 | 79PQ2426 | POLYLON(T) |  | 1 |  |  |
| 15201641 | 79PQ2653 | LABEL,SERIAL BARCODE (A) |  | 1 |  |  |
| 15200491 | 79PQ0966 | LABEL (MANUFACTURE, NPG) |  | 1 |  |  |

9. BLOCK DIAGRAM


## 10. SCHEMATIC DIAGRAM (FE770/FE770M/FE771SB/DPlus 74SB)




| MODEL | FE771SB/Dplus74SB | FE770/FE770M | FE770/FE770M |
| :---: | :---: | :---: | :---: |
| CRT | MITSUBISHI M41LRY61X22 | $\begin{gathered} \text { LG } \\ \text { M41QEE903X03 } \end{gathered}$ | $\begin{gathered} \text { SAMSUNG } \\ \text { M41QCJ761X172 } \\ \text { (DFX) } \end{gathered}$ |
| R30H | NC | 750k 1/4W | 750k 1/4W |
| R30J | NC | 750k 1/4W | 750k 1/4W |
| R319 | 150k | 68k | 120k |
| R31L | NC | 51k 1/4W 1/4W | 51k 1/4W 1/4W |
| R31T | 390k 1/4W 1\% | 169k 1/4W 1\% | 133k 1/4W 1\% |
| R344 | 27.4k 1/4W 1\% | 25.5k 1/4W 1\% | 25.5k 1/4W 1\% |
| R348 | 5.36k 1/4W 1\% | 5.49k 1/4W 1\% | 5.49k 1/4W 1\% |
| R350 | 1k 1/4W | 4.7k 1/4W | 4.7k 1/4W |
| R35E | 33k 1/4W 1\% | 39k 1/4W 1\% | 39k 1/4W 1\% |
| R358 | 470k | 330k | 330k |
| R366 | 240k 1/4W 1\% | 150k 1/4W 1\% | 169k 1/4W 1\% |
| R367 | NC | 1M 1/2W | 1M 1/2W |
| R380 | NC | 1M 1/2W | 1M 1/2W |
| R381 | NC | 1M 1/2W | 1M 1/2W |
| R388 | 549 1/4W 1\% | 510 1/4 1\% | 430 1/4W 1\% |
| R415 | 1.1 1W | 1.2 1W | 1.2 1W |
| R705 | 10K | NC | NC |
| C319 | 6200P 800V PPN | 5600P 800V PPN | 5600P 800V PPN |
| C321 | NC | $0.01 \mathrm{u} 1 \mathrm{kV} \mathrm{25V}$ | 0.01u 1kV 25V |
| C322 | NC | J.W | J.W |
| C332 | . 3 u 400 V MPPS | .3u 400V MPPS | .3u 400V MPPS |
| C334 | 1000P / 1kV Y5P | 1000P / 1kV Y5P | 1000P / 1kV Y5P |
| C345 | .01u 250V MPE | .01u 250V MPE | 0.022u 250V MPE |
| C356 | .24u 250V MPP | .27u 250V MPP | .27u 250V MPP |
| C357 | NC | 1000P 1kV Y5P | 1000P 1kV Y5P |
| C363 | 0.01u PEI | NC | NC |
| C367 | NC | NC | 0.01u PEI |
| D31A | UF4006 | J.W | J.W |
| D326 | NC | BA159 | BA159 |
| D330 | SB160/SR160 | 1N4937 | 1N4937 |
| D346 | SB160/SR160 | J.W | J.W |
| B309 | 3.5X4.7/T | J.W | J.W |
| B32A | 3.5X4.7/T | J.W | J.W |
| L302 | 76uH | 130uH | 76uH |
| L303 | 130uH | 130uH | 130uH |
| L307 | 80010401 | 80010401 | 80010401 |
| Q307 | 12600251 | 12600251 | 12600251 |
| T301 | 80015631 | 80009281 | 80009281 |
| T303 | 80015651 | 80015651 | 80015651 |
| S701 | R0224611 | R0224611 | R0224611 |
| JP701 | NC | J.W | J.W |
| VR307 | J.W | 100k | 100k |
| CRT | 80015091 | JG072301 | 80013481 |
| G2 | NC | 80013121 | 80013121 |




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