SERVICE MANUAL

HIGH RESOLUTION DISPLAY MONITOR

NSH1157STTUW

MITSUBISHI ELECTRIC CORPORATION
JANUARY 2000

CBB-S5701

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SPECIFICATION
OF
51cmV (20"V) AUTO-TRACKING COLOR DISPLAY MONITOR

MODEL: NSH1157STTUW

NO.	TYPE			MITSUBISHI STANDARD	REMARKS
1	CRT	Size		55cm / 51cmV (22" / 20"V)	Diamondtron NF
		Grill Spacing(Phosphor Spacing)		0.24mm (0.25mm)	Aperture Grille
		Phosphor Type		B22 (EBU)	
		Face-plate		AR Coating with anti-static	
		Electron Gun Type		S-NX-DBF	
		Face-plate Transmission		39.8 %(Including face-plate coating)	
2	SCANNING	Horizontal Freq.		30k - 121kHz	
		Vertical Freq.		50 - 160Hz	
3	SIGNAL INPUT	Video Sync.		Analog	0.7Vp-p
				Composite Sync. with G-video	0.3Vp-p
				Composite Sync.	TTL Nega
				Separate Sync.	TTL Posi / Nega
		Termination (Impedance)	Video	75 Ω to Ground	
			Sync.	2.2k Ω to Ground	
4	VIDEO	clock frequency		240MHz	
5	SCREEN CHARACTERISTICS	Display Resolution		2048 x 1536 (addressable)	
		Display size	Horizontal	393mm	
			Vertical	295mm	
		Misconvergence		Center : 0.3 mm , Corner : 0.40 mm	
		Brightness (Full White)		100cd/m^2 at 9300K	
6	CONTROL (User Controls)	Front		Power SW, Input Connector select / OSD off Button, Select Button , Adjust Button	
			OSD	Contrast, Bright, Color No. , RGB-Gain, Color temperature, Color Reset, Horiz-Size, Horiz-Phase, Vert-Size,Vert-Position,Pincushion, Keystone, Top-Pin, Bottom-Pin, Pin-Balance, Key-Balance, Vert-Lin-Balance, Vert-Lin, Rotation, Zoom, Geometry Reset, Fine Picture Mode, Horiz-Convergence, Vert-Convergence, Corner Purity (TL/TR/BL/BR), Moire Cancel, Moire Cancel Level , Clamp Pulse Position, Video Level,Degauss, Power-Save, Control Lock, OSD Position, All Reset, GTF Auto Adjust, Diagnosis, Language	Micro-processor control. Color adjustment. (3 color preset)
7	CONNECTOR	Power Input		3P IEC Plug	Auto-select
		Signal Input		DB9 - 15P x2 USB Connectors (2 x Upstream Ports , 3 x Downstream Ports)	
8	POWER SUPPLY	Operating range		AC100 - 120V / 220 - 240V , 50 / 60 Hz	
		Power consumption (typ.)		140 W 1.40A@100-120VAC 0.65A@220-240VAC(without USB load) 155 W 1.55A@100-120VAC 0.75A@220-240VAC(with USB load)	
9	ENVIRONMENTAL CONDITION	Operating temperature		5 - 35°C	
		Relative humidity		10 - 90% (without condensation)	
10	WEIGHT			approx. 29.5kg (65lbs)	
11	CABINET	with Tilt / Swivel stand		Mitsubishi standard	
12	REGULATION	Safety		UL / C-UL TÜV (GS)	
		EMC		FCC-B CE-Marking EN60950 EN55022 - B DOC-B EN50082 - 1 EN61000 - 3 - 2, - 3 - 3	
		X - Ray		DHHS RöV HWC	
		VLF / ELF		MPR - II , TCO91	
		Power Management		International Energy Star Program .	
		Ergonomics		TCO99 , TÜV (GS)	
13	OTHERS	Plug & Play		DDC1 , 2B(EDID)	
		Digital Dynamic Convergence			
		Communication		Universal Serial Bus (Hub & Function) SELF POWERED HUB(500mA per 1 Downstream Port) & Function 3 x Downstream Port , 2 x Upstream Port	

1. Circuit description

1.1 Power circuit

1.1.1 Outline

(1) The power block is compatible with 100 to 120VAC/220 to 240VAC(50/60Hz).

(2) The active filter circuit is adopted to suppress the higher harmonic current and improve the power factor.

(3) The circuit that supplies the electric power to the secondary side is divided into two circuits that are respectively called the main power and sub power.
Though both main and sub circuits supply the power to the secondary side in the normal operation mode, the power is supplied from the sub power only in the power save mode since the main power is stopped.
The main power is the configuration used the flyback converter type switching control IC of the simulative resonant operation. Moreover, the sub power is the configuration used PWM (pulse width modulation) control IC.
In the power circuit, the voltage fluctuation from the secondary side is fed back via the photocoupler in order to suppress the voltage fluctuation caused by the load fluctuation on the secondary side.

(4) The output on the secondary side is shown in Table 1.
(Refer to the power system diagrams in Pages 1-8, 1-9 and 1-10.)

Power block	Output voltage	Application	When power save
Main power side	+190V	H. deflection circuit, video cut off circuit	OFF
	+90V	DBF circuit, high voltage circuit	OFF
	+80V	Video circuit	OFF
	+15V	H/V deflection circuit, etc.	OFF
	-15V	H/V deflection circuit, etc.	OFF
	+12V	Video circuit, H. deflection circuit, etc.	OFF
Sub power side	+6.5V	Heater	ON
	USB+6.5V	USB circuit	ON
	+5V	MPU, etc.	ON
	P-OFF+5V	Video circuit, etc.	OFF

Table 1

1.1.2 Rectifying circuit

(1) The AC input voltage is rectified in the full wave mode with the diode bridge in D901.

(2) In the higher harmonic circuit of the section 1.4, the AC input current becomes the sine wave form in the same phase with the AC input voltage waveform, but the interference is given to other peripheral devices since the noise of the switching current appears on the input side owing to the switching waveform. Therefore, L902 and C906 are inserted to suppress the noise that is caused by the switching current.

1.1.3 Surge current suppression

(1) TH901 (thermistor) and R930 suppress the rush current that flows when the power switch is turned ON. Moreover, D933 is added to protect D902 from the rush current.

1.1.4 Higher harmonic circuit

(1) The pulsating waveform rectified in the full wave mode by D901 is switched throughout the full cycle by the frequency of several tens kHz or more. Through this, the input current waveform becomes an average of the switching currents of the partial cycles, thus becoming the sine waveform in the macro. (See Fig.1)

(2) For the AC input voltage, the AC input current of the sine wave type in the same phase flows to achieve the power circuit of improved power factor and reduced higher harmonic wave component.

(3) L903 is the choke coil, Q901 is MOS FET, D902 is the rectifying diode, C911 is the block capacitor, and IC901 is the power factor improved controller. The power factor improved controller uses MC33262P of Motorola. (See Fig. 2)

(4) After the sub power starts, P-SUS signal becomes HI when +5V voltage is supplied to the MPU. Then, Q902 is turned ON, the voltage of approx. +18V is supplied to Pin 8 (VCC terminal) of IC901 through D932 from Pin 2 of T902, and the following operation is started.

(5) The pulsating voltage waveform rectified in the full wave mode by D901 is divided with R904, R905, R906, R907 and R908 (100VAC : 1.1Vp-p and 240VAC: 2.9Vp-p), and is input to Pin 3 of IC901 (Multiplier input). Moreover, the output (+side of C911: 400VDC) of the higher harmonic circuit is divided with R913, R914, R915, R916 and R917 (2.5VDC), and is input to Pin 1 of IC901 (error amplifier input).

(6) The output of the error amplifier and the divided waveform of the pulsating voltage input to Pin 3 of IC901 sets the threshold voltage of the current sense comparator to control the Q901 flowing current from zero to the peak line of the AC input voltage in the sine wave pattern.

(7) When Q901 is turned ON, the drain current of Q901 flows to R910 and R937 to drop the voltage, and the voltage generated by the voltage drop is input to Pin 4 (current sense input) of IC901. When the voltage reaches the threshold voltage of the current sense comparator, Q901 is turned OFF.

(8) When Q901 is turned OFF, the accumulated energy of L903 starts to be supplied to the load through D902.

(9) As the accumulated energy of L903 drops, the auxiliary coil voltage (Pin 10 of L903) also drops. When it reaches the threshold voltage of *zero current detector, Q901 will be turned ON again.

* Pin 5 of IC901 is the zero current detection terminal to input the auxiliary coil voltage of Pin 10 of L903. The zero current detector monitors that the auxiliary coil voltage drops beyond the thresh old voltage. Thus, the accumulated energy of L903 is indirectly detected.

(10) The above operation is repeated to continue the oscillating operation. Thus, the DC voltage (L903, Q901, D902 and C911 compose the voltage rise circuit.) is gained on the output, and the AC input current of the sine wave in the same phase with the AC input voltage is gained on the input side.

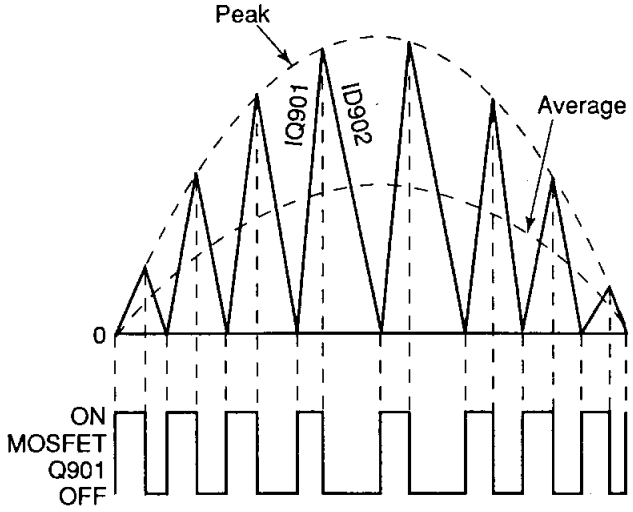


Figure 1. L903 coil current

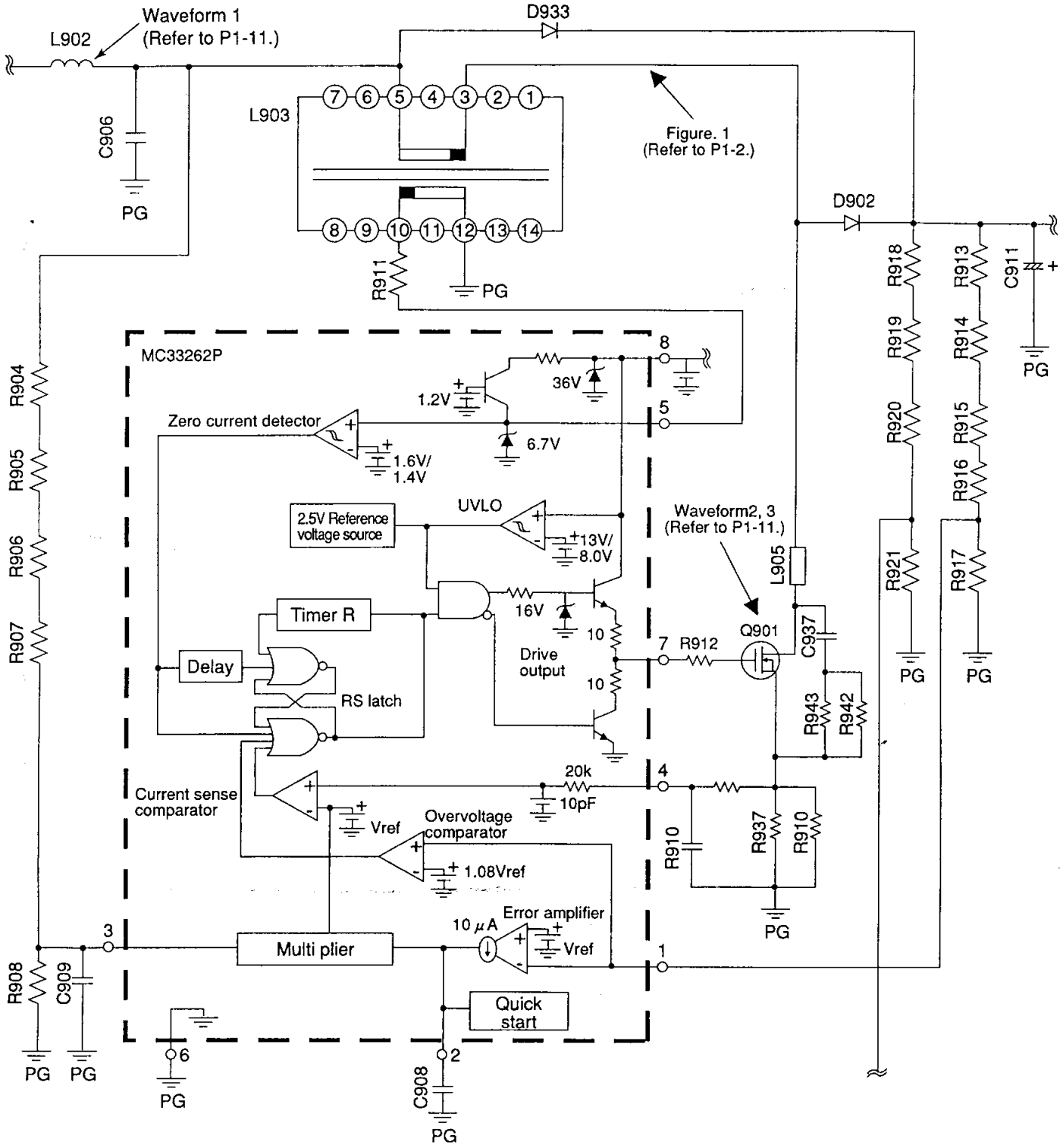


Figure 2. High harmonic waveform circuit

1.1.5 Sub power circuit

(1) The sub power uses the self-excited type regulator MIP0223SYproduced by Panasonic. (See Fig.3)

(2) When the power switch is turned ON, the rectified and smoothened DC voltage (AC voltage x $\sqrt{2}$) is supplied to Pin 3 of IC903, and is charged to C932 through Pin 1. When Pin 1 reaches 5.7V, the current supply from Pin 3 is cut off to start oscillation (approx. 100kHz) in IC903, and the output FET is put into operation. (Since Q902 is OFF, IC902 and IC 903 do not operate.)

(3) This also induces the voltage at Pin 2 of T902 and on the secondary side. These outputs are respectively rectified, and are used as the power for control on the primary side and the power for the MPU and heater.

(4) The voltage induced on the secondary side is fed back to the primary side through IC912 (photocoupler) from the constant voltage circuit that uses IC922 (shunt regulator). The circuit supplies and controls the power for control on the primary side to Pin 1 of IC903 via R935 in order to suppress the voltage fluctuation on the secondary side.

(5) When the voltage on the secondary side starts, the MPU will be put into operation and the P-SUS signal line will become HIGH.

(6) This information is transmitted to the primary side via IC913 to turn ON Q902. When Q902 is turned ON, the power for control on the primary side will be supplied to IC901 and IC902 to operate the higher harmonic circuit. Thus, the main power circuit will be put into operation.

1.1.6 Main power circuit

(1) The main power circuit adopts the flyback type switching power of pseudo-reosonance operation. This is composed of a Sanken brand hybrid IC (STR-F6676) that integrates the power MOS-FET and control IC.
The circuit operation is described as follows. (See Fig. 4.)

(2) The timing at that the power MOS-FET is turned ON is consistent with the bottom point of the voltage resonant waveform after the transformer (T901) discharges the energy to the secondary side, that is, a half cycle of the resonant frequency determined by Lp value (primary coil inductor value) of T901, and C914 (resonant capacitor). This is called pseudo-reosonance operation. The advantage of such an effect is that the switching loss is reduced by turning it ON when the voltage between the drain sources of the power MOS-FET becomes the lowest.

(3) Like the higher harmonic circuit, voltage of approx. +18V is supplied to the Vcc terminal (Pin 4) of IC902 (STR-F6676) via D932 from Pin 2 of T902 when Q902 is turned ON by the P-SUS signal from the MPU.
When the voltage of Pin 4 of IC902 reaches 16V, the control circuit will be put into operation to turn ON the integrated MOS-FET.

(4) When MOS-FET is turned ON, the capacitor C1 in IC will be charged to approx. 6.5V. On the other hand, the drain current flows to R928, and the voltage generated by the voltage drop is applied to Pin 1 (OCP/FB terminal) of IC902.
When the voltage of Pin 1 reaches approx. 0.73V, the comparator (Comp. 1) in IC will be activated to turn OFF MOS-FET.

(5) The voltage between both ends of C1 drops to approx. 3.7V. the oscillator output will be reversed again to turn ON MOS-FET.
The above is repeated to continue the oscillation operation.

(6) Here, IC902 monitors +190V of the output on the secondary side with IC921 (error amplifier) and feeds back it to Pin 1 of IC902 with IC911 (photocoupler), thus suppressing the voltage fluctuation of the primary side.

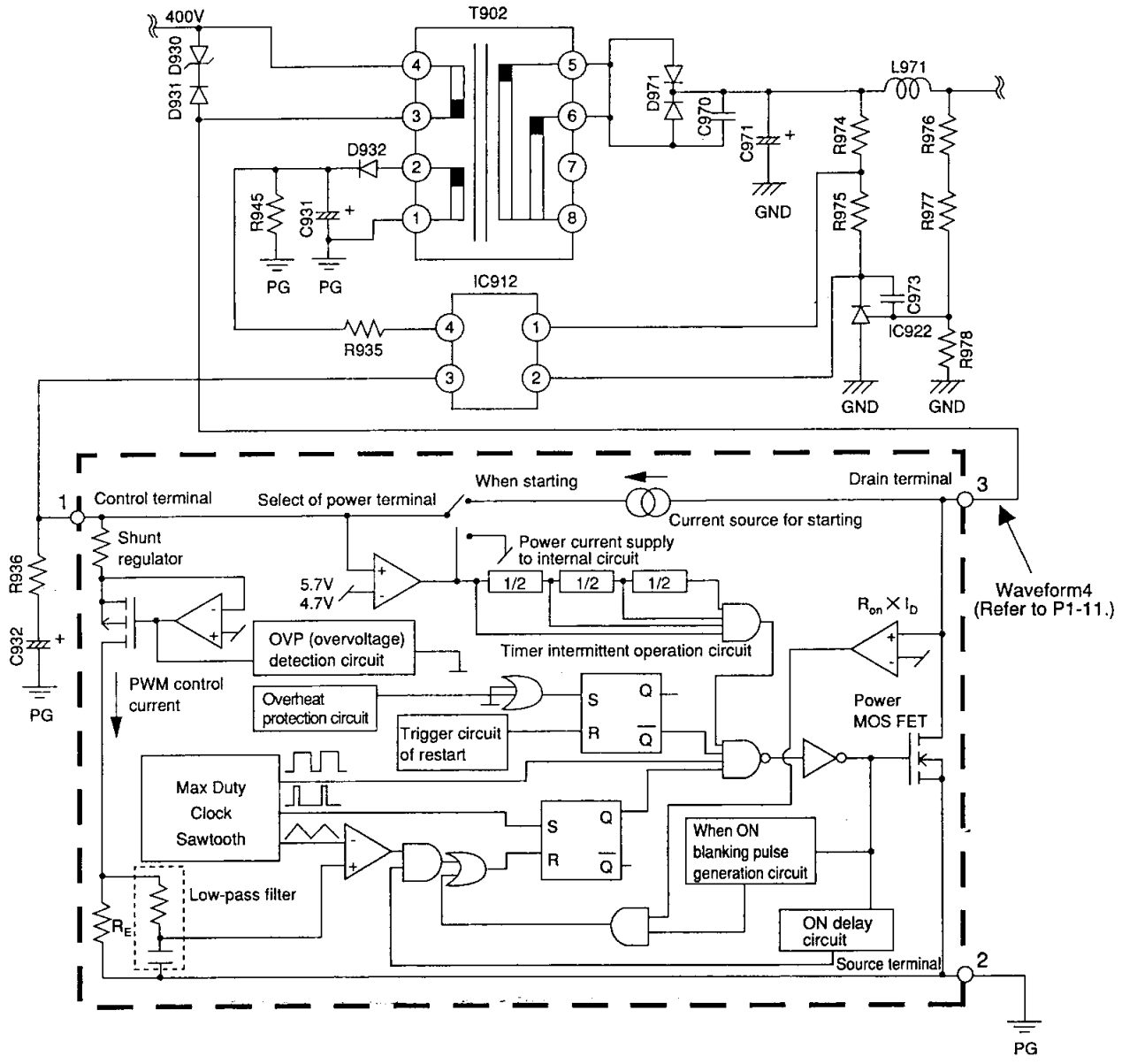


Figure 3. IC903 (MIP0223Y) block diagram and peripheral circuit

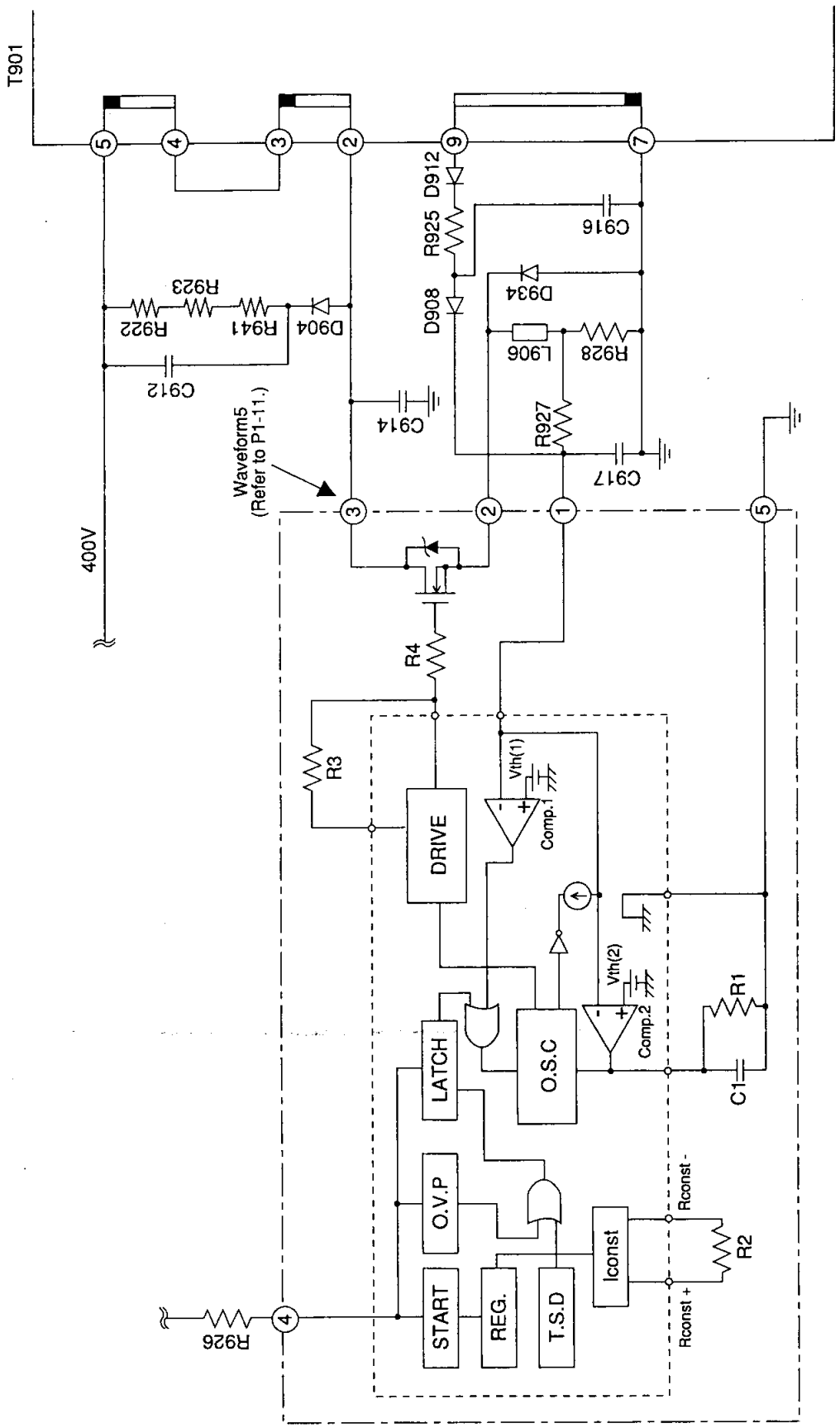


Figure 4. IC902 (STR-F6676) block diagram and peripheral circuit

1.1.7 Demagnetizing circuit

(1) The automatic and manual demagnetizing circuit is provided.
The circuit prevents the picture from dropping its quality due to the magnetization on CRT, and operates as follows.

(2) When powering ON, Q963 flows to activate RY901 by DG signal output by the MPU.
This will make the current flow through the demagnetizing coil for demagnetization. The demagnetizing time is approximately 5 seconds.
Manual demagnetization becomes possible by selecting the demagnetizing menu on the OSD picture.

1.1.8 Power management circuit

Turn ON the power management setting on the menu picture of OSD, and the energy saving mode shown in Table 2 will be ready depending on whether the horizontal/vertical sync. signal is present or not.

	H-sync	V-sync	Video	Power consumption	Recovery time	LED indicator
OFF	On	On	Active	140W	—	Green
ON	Off	On	Blank	≦5W	3秒	Amber
	On	Off	Blank			
	Off	Off	Blank			

Table 2

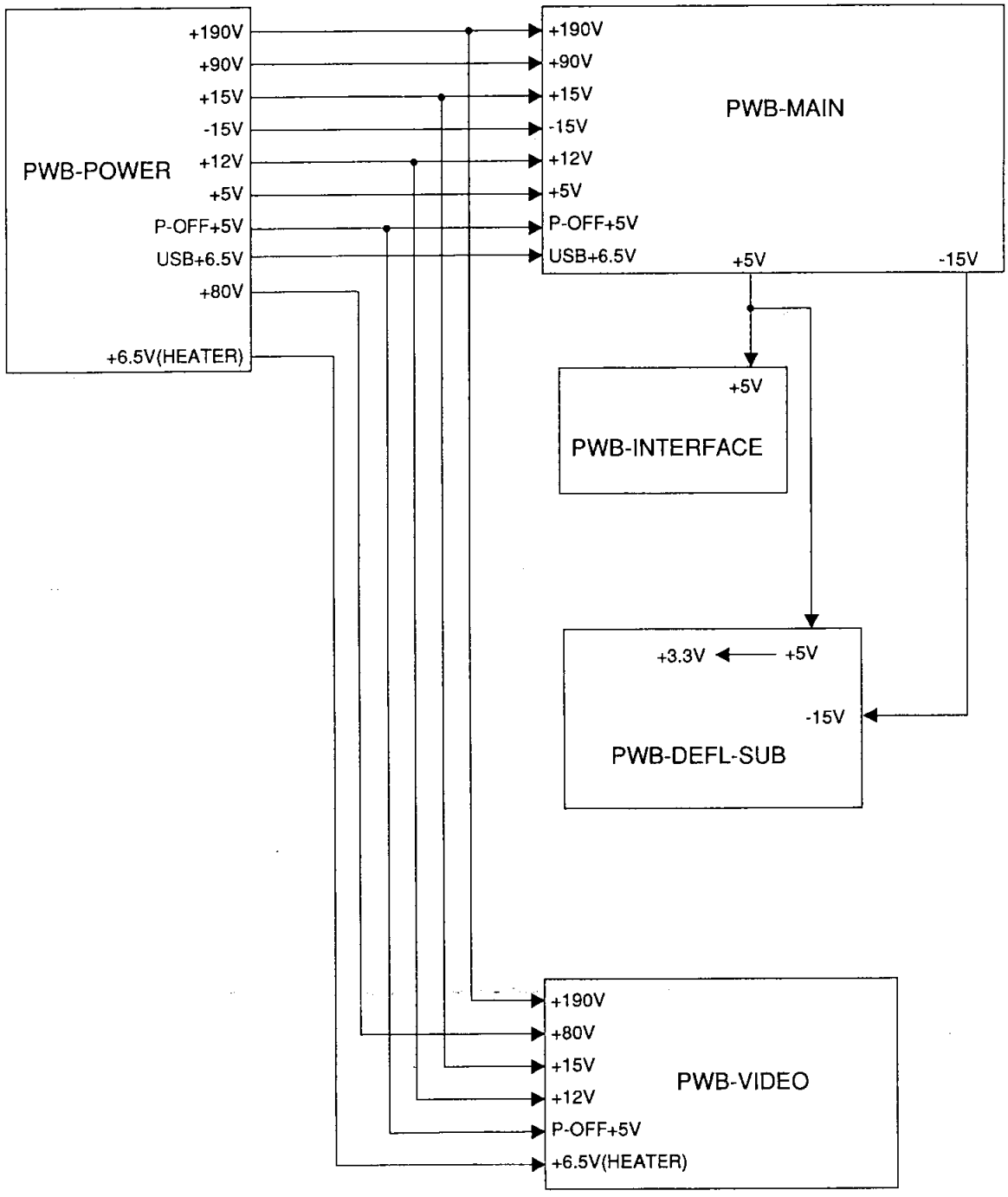
1.1.9 Protective circuit

(1) Overcurrent protective circuit (primary side)
IC902 is provided with an overcurrent protective circuit. The voltage drop generated by the drain current that flows into R928 is input to Pin 1 (OCP/FB terminal) of IC902. When the voltage reaches 0.73V, the overcurrent protective circuit will be activated.

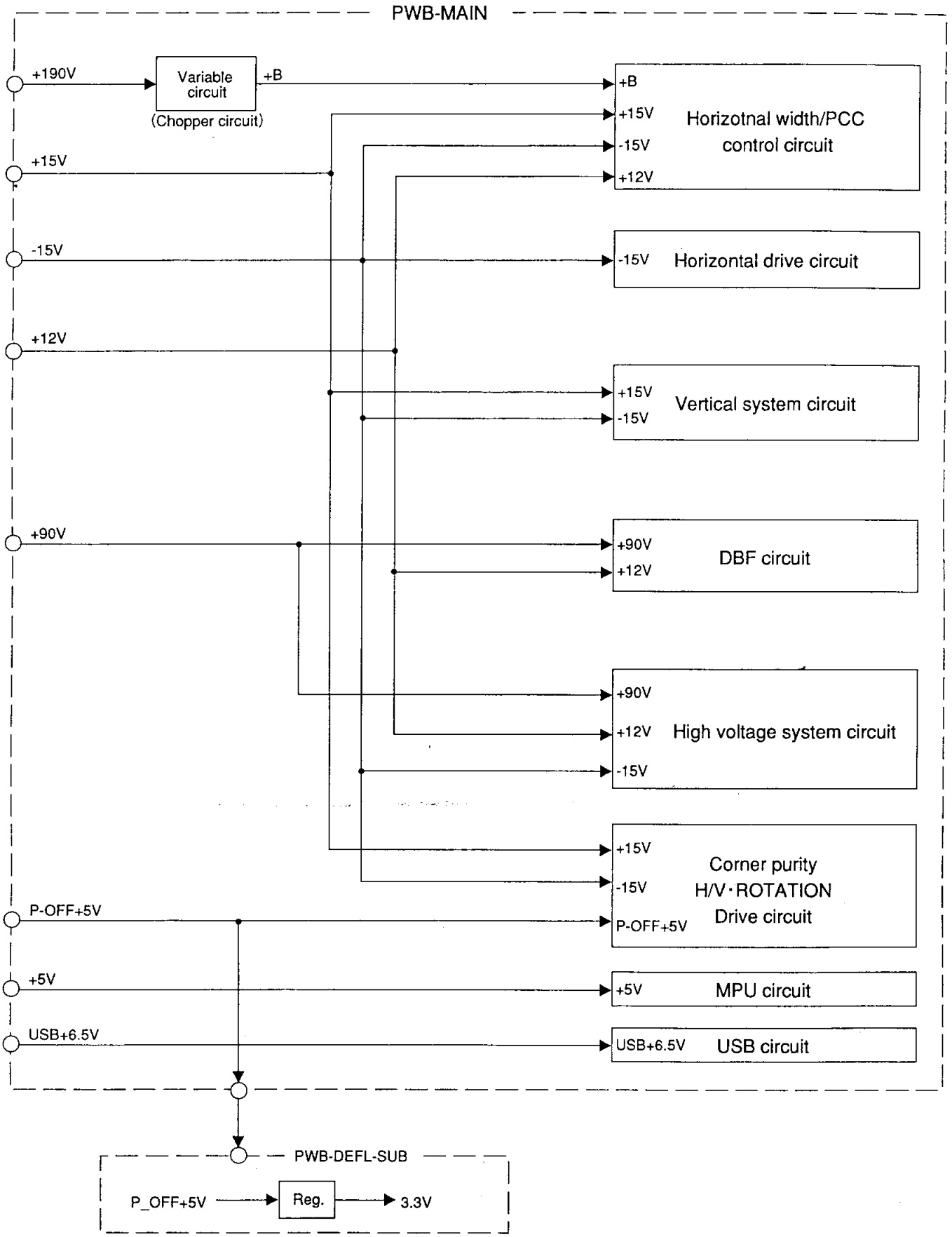
(2) Overcurrent protective circuit (secondary side)
To protect the parts on the secondary side, the short-circuit detection circuit is provided on the secondary side output (+190V, +90V, +80V, +/-15V), one for each. As an example of +190V, the output line of +190V is monitored with R964, R965, D968 and Q961. If it drops beyond +150V for any reason, Q961 will be turned ON to transmit the information to the MPU. Then, since the MPU sets P-SUS signal at LOW, Q902 will be turned OFF to cut off the power to IC902 in order to stop IC902. (IC901 will be also stopped at the same time.)
The overcurrent protective circuit is designed to be activated when the output voltage drops approx. 20 to 30%.
The circuit takes the role of the FUSE that is used on the conventional model.

(3) Overvoltage protective circuit
R918, R919, R920 and R921 are used to detect the overvoltage in the higher harmonic circuit, and the tertiary coil (Pin 9) of T901 is used to detect the overvoltage of the voltage on the secondary side. They are both connected to the overvoltage protective circuit (Q904, Q905) on the primary side. If any overvoltage results for any reason, Q905 will be turned ON to turn ON Q904. Since the base potential of Q903 then drops beyond 0.7V to stop it, Q902 will be stopped. Since the power is cut off for IC901 and IC902 as Q902 is stopped, the switching operation will be stopped.

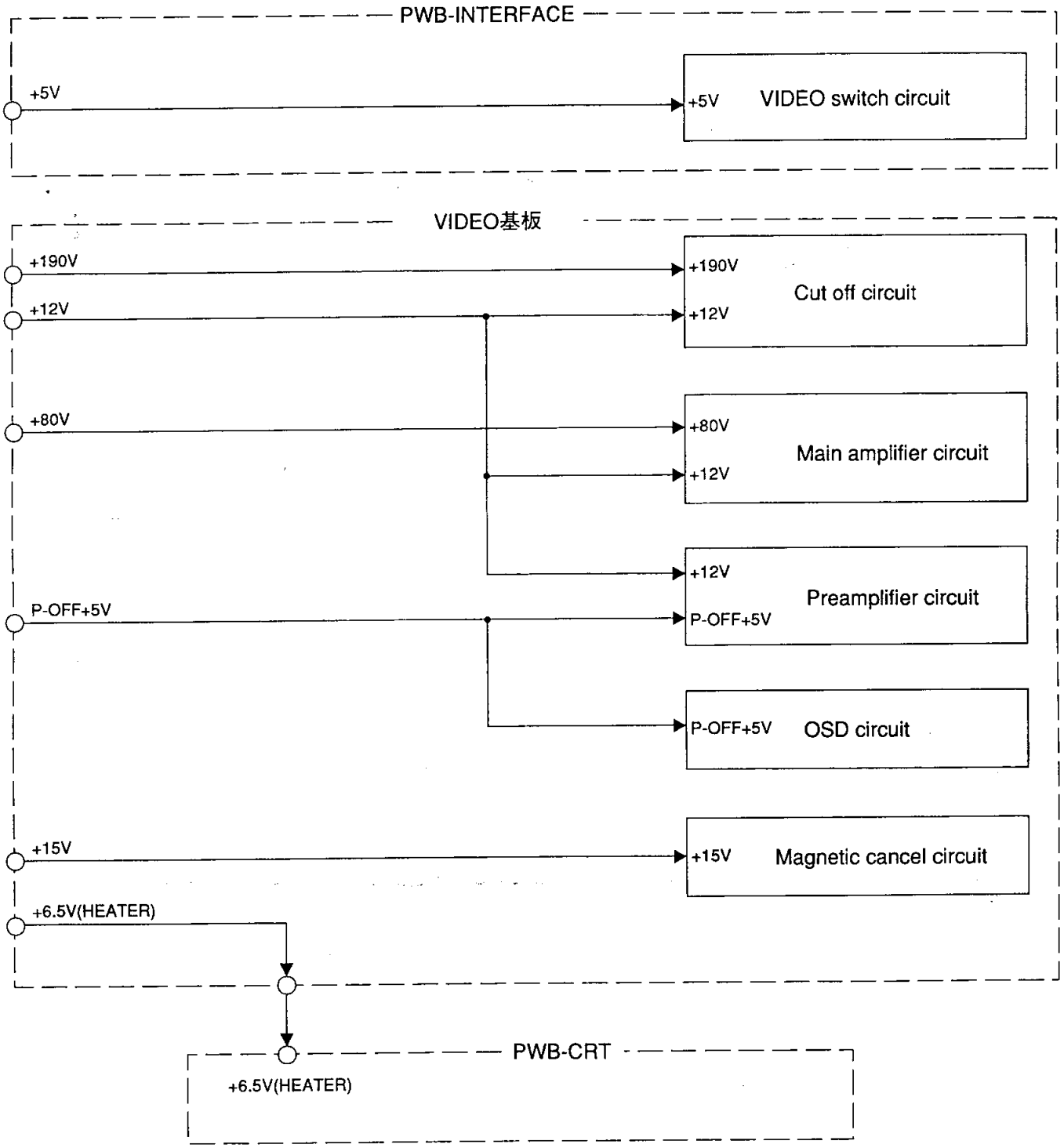
~Power system diagram 1~

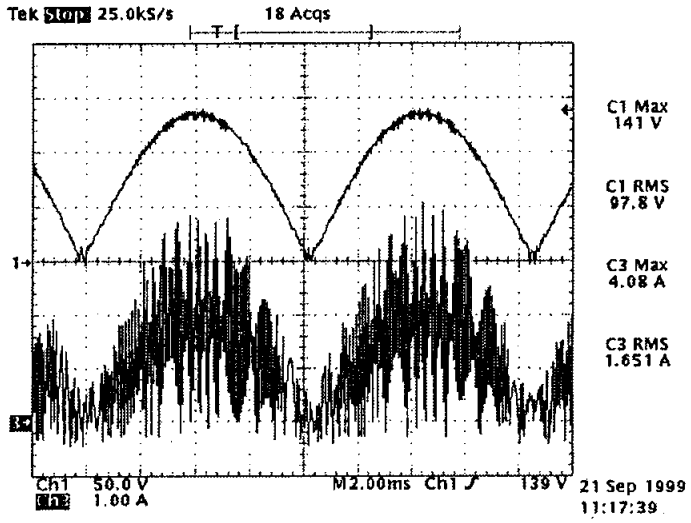


~Power system diagram 2~

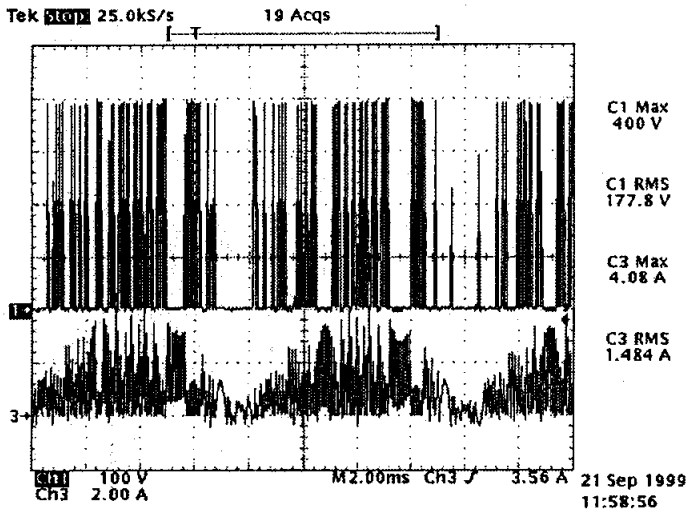


~Power system diagram 3~

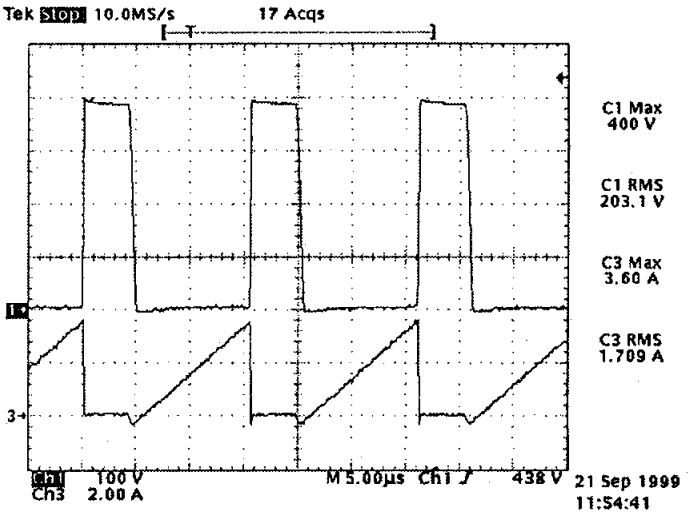




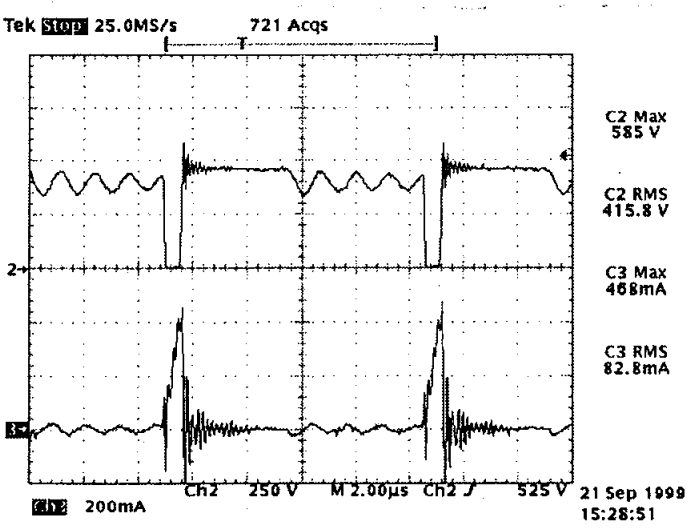
Waveform 1. Top :AC input voltage
Bottom :AC input current



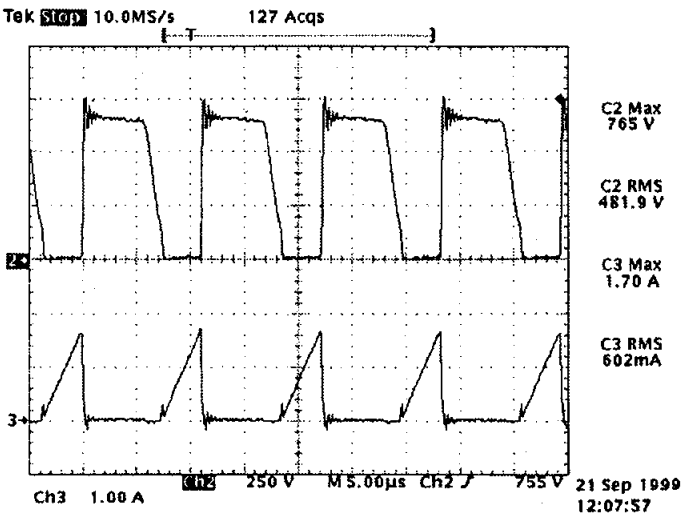
Waveform 2. Top :Q901 drain voltage
Bottom :Q901 drain current



Waveform 3. Top :Q901 drain voltage
Bottom :Q901 drain current



Waveform 4. Top :IC903 drain voltage
Bottom :IC903 drain current



Waveform 5. Top :IC902 drain voltage
Bottom :IC902 drain current

1.2 Deflection circuit block

1.2.1 Horizontal deflection circuit

The operational principle of the horizontal deflection circuit is shown as follows.
Q502 and D503 operate as the horizontal output and damper diode respectively.
IC502, Q511 and RY501 are switched according to the horizontal frequency to compensate the horizontal linearity.

In Fig. 5, the horizontal output transistor Q502 is turned ON and OFF through the drive transformer T501, drive transistor Q501 or Q7A0, Q7A1, Q7A2 and so on by the drive pulse of Pin 25 of IC700 on the PWB-DEFL-SUB.
While Q502 is ON, the deflection current Idy increases to the maximum Ip according to the following formula.

$$Idy = (Vcc/Ldy) \times Ton$$

The maximum Ip at the chassis is approximately 8A in case of full scan at fh=106k.

Here, Vcc: Q504 output voltage
Ldy: Parallel value of Lh value (=62μH) of DY and horizontal output transformer (=5mH)
Ton: Time for that Q502 is ON

When the drive pulse becomes a negative polarity, Q502 will be turned OFF, and it will flow to charge C502 and C503 until the maximum value Vcp of the collector voltage reaches the value of the following formula.

$$Vcp = Vccx\{1 + (\pi/2) \times (Ts/Tr)\}$$

When Vcp reaches the maximum value, the electric charge accumulated in C502 and C503 will flow into DY as the discharge current.
The charged/discharged current is called the retrace time, being expressed with the following formula.

$$Tr = \pi\sqrt{(Ldy \cdot Cr)}$$

At the chassis, the retrace time is set at approx. 2μs.
Here, it becomes the total of the values of Cr:C502, C503. Moreover, Ts is called the trace time, being expressed by the following formula with the horizontal cycle of T.

$$T = Ts + Tr$$

When Vcp becomes 0, the damper diode D503 is turned ON, and Idy decreases from -Ip to 0 ampere. Since the ON term of Q502 and the ON term of the damper diode are made to be overlapped at the 0 ampere point of Idy, cross over distortion at the 0 ampere point of Idy is prevented from occurring. D503 flows the transient current with the high speed damper diode. The horizontal output transformer T502 is connected to the power in parallel with the deflection yoke, working as the choke coil. Figs. 6 and 7 show the image of the circuit operation and the waveform at the monitor.

The width of the horizontal picture and side PCC are controlled with IC5J1, IC5J2, Q503 and Q504. The horizontal width signal applied to Pin 5 of IC5J2 by Pin 64 of IC700, and distortion compensation signals are compared with the signal that is converted to the voltage from the current value of the horizontal deflection circuit by T503 and is fed back to Pin 13 of IC5J2 via IC5J1. Then, it is compared with the sawtoothed wave of the constant inclination type that is synchronized with the horizontal frequency generated in IC, and is converted to the PWM signal of the rectangular wave. The PWM signal is output to Pin 9 of IC5J2, and the above control is done by driving the gate of Q504. Fig. 8 shows the block diagram of IC5J2, and Fig. 9 indicates the image waveform of the operation.

Moreover, as the operation of Q5J1 and Q5J2 connected to Pin 11 of IC5J2, Q5J1 is normally turned OFF since Q5J2 is turned ON. However, as the 15V line lowers when the power is turned OFF, and Q5J2 is turned OFF, Q5J1 is turned ON and Pin 11 of IC5J2 is pulled to GND. Since Pin 11 of IC5J2 controls the ON term of PWM to 1.2μs when 0V is applied, it works to lower the output voltage of Q504 as the result in order to prevent breakage from occurring due to the abnormal pulse during the transient time of Q502 (H-OUT Tr).

Q503 works as the ripple filter of the 190V line to keep the emitter voltage of Q503 constant even if the collector voltage of Q503 slightly fluctuates. Though the voltage of 190V is applied to the collector of Q503, the emitter output is stabilized at 187V. It is mainly effective for dynamic regulation.

The horizontal raster position is adjusted with Q5A1, Q5A2, VR5A1 and T502. The reference voltage is taken at the connection point of Cs, and is input to Pin 2 of T502. As the DC level of the emitter voltage of Q5A1 and Q5A2 is raised by adjusting VR5A1, the current will flow into the DY side to move the raster leftward. On the contrary, the current flows to the Q5A2 side to move the raster rightward as the DC level of the emitter is lowered. For adjustment, the emitter voltage of Q5A1 and Q5A2 are varied with VR5A1 by the timing signal of 106k85Hz to adjust the DC level of Idy in order to position the raster position at the center of CRT. Fig. 10 shows the operation image.
This is executed only in the factory adjustment but it is not accessible for user adjustment.

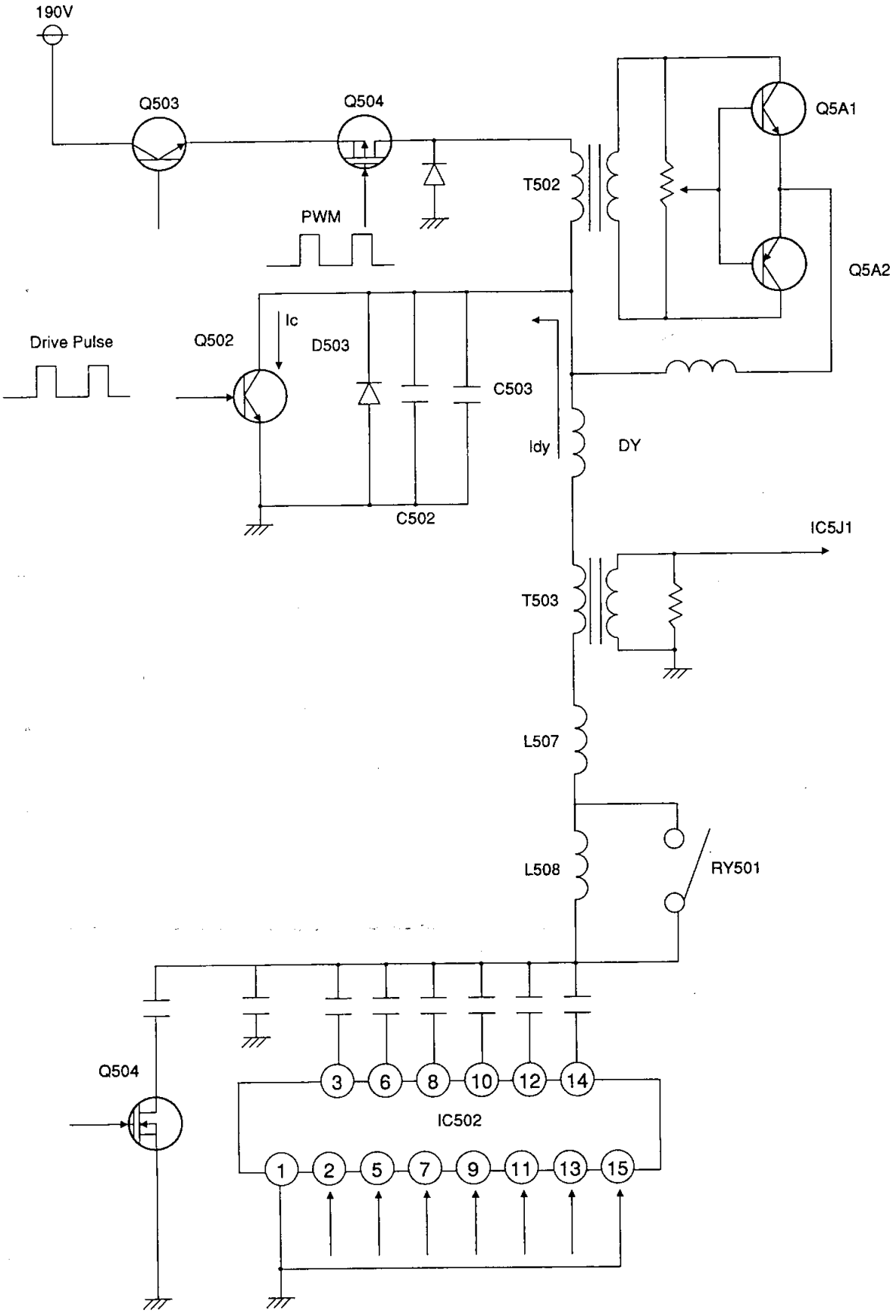

190V
Q503
Q504
T502
Q5A1
Q5A2
PWM
Drive Pulse
Q502
Ic
D503
C503
C502
Idy
DY
IC5J1
T503
L507
L508
RY501
Q504
3
6
8
10
12
14
IC502
1
2
5
7
9
11
13
15

Figure 5

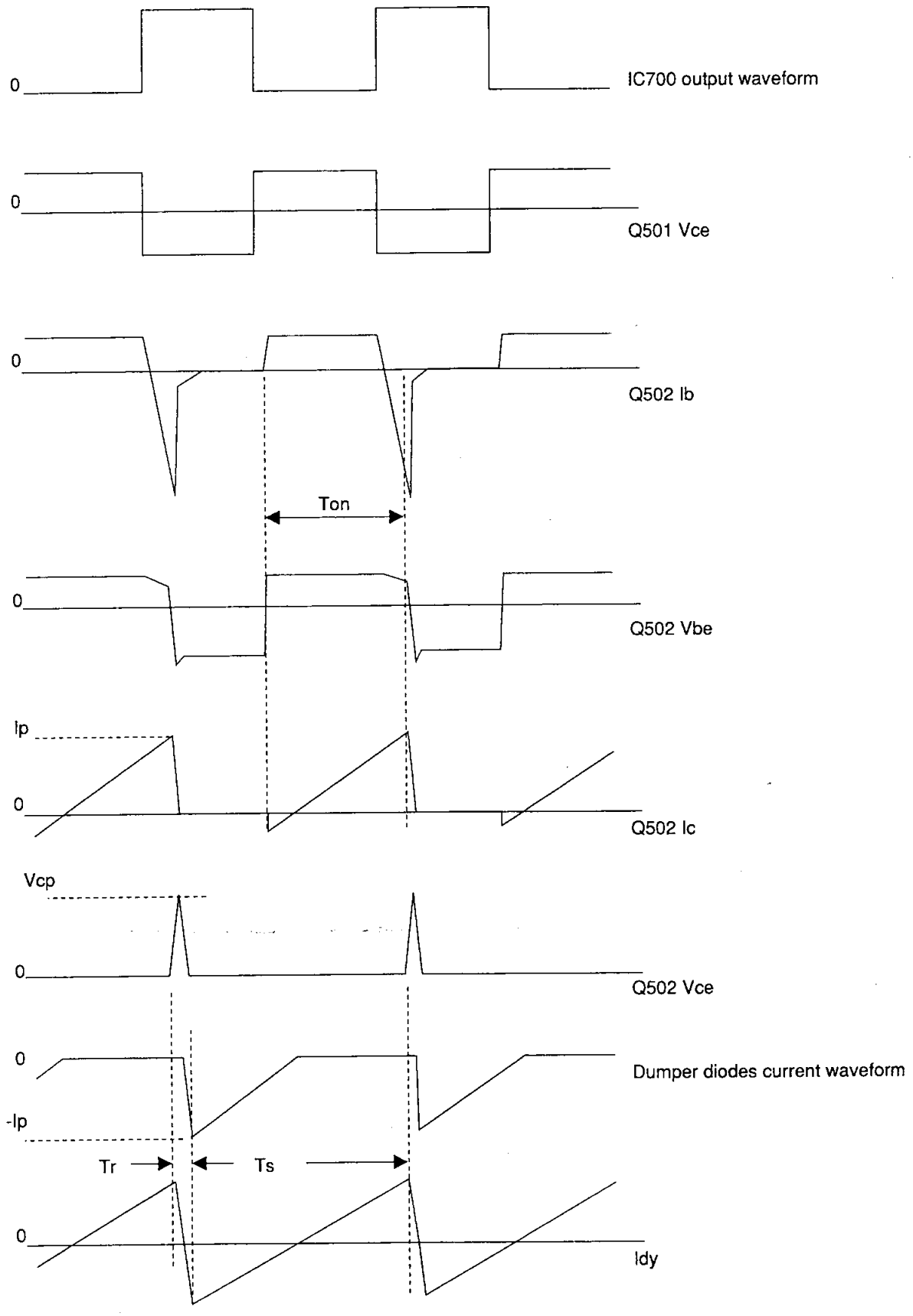
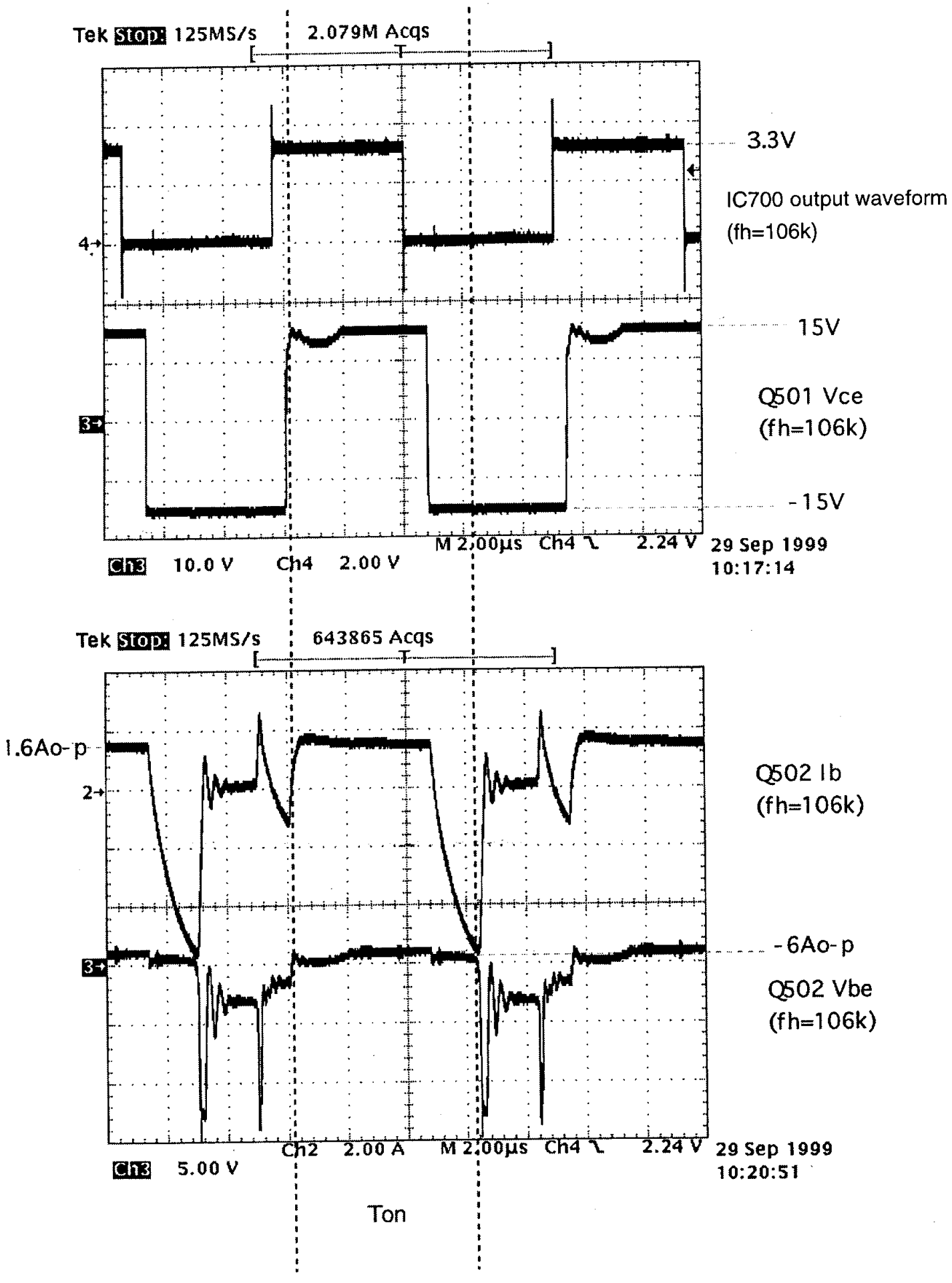
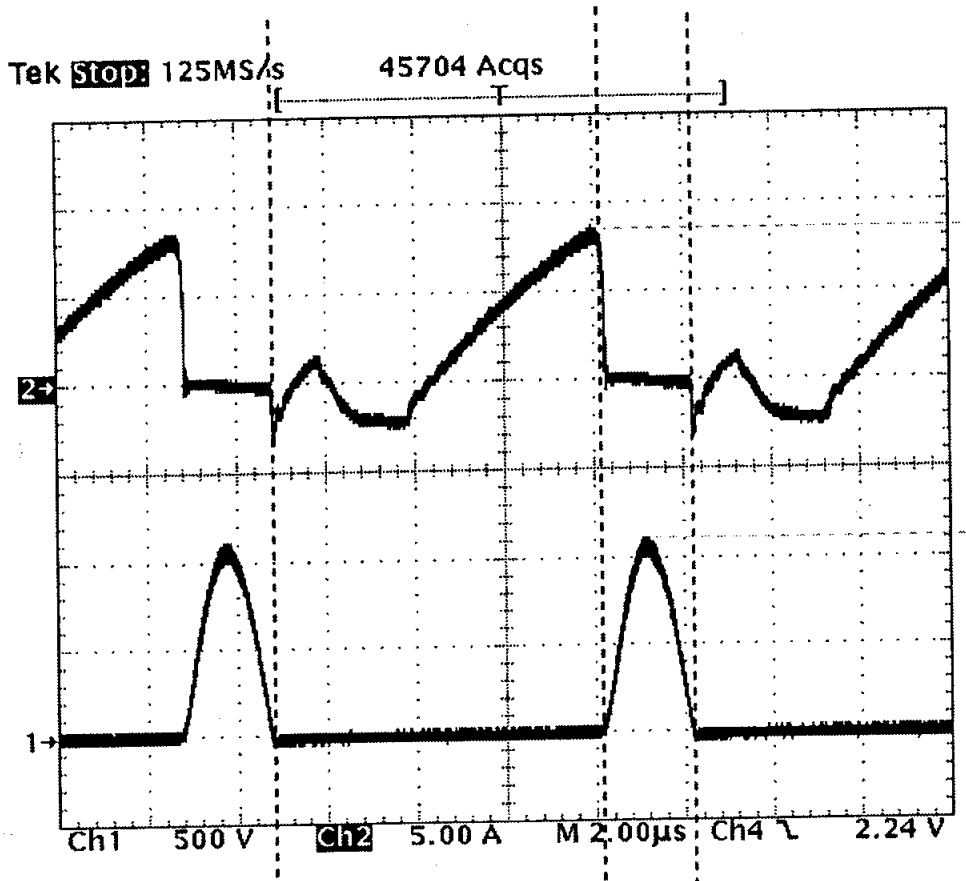
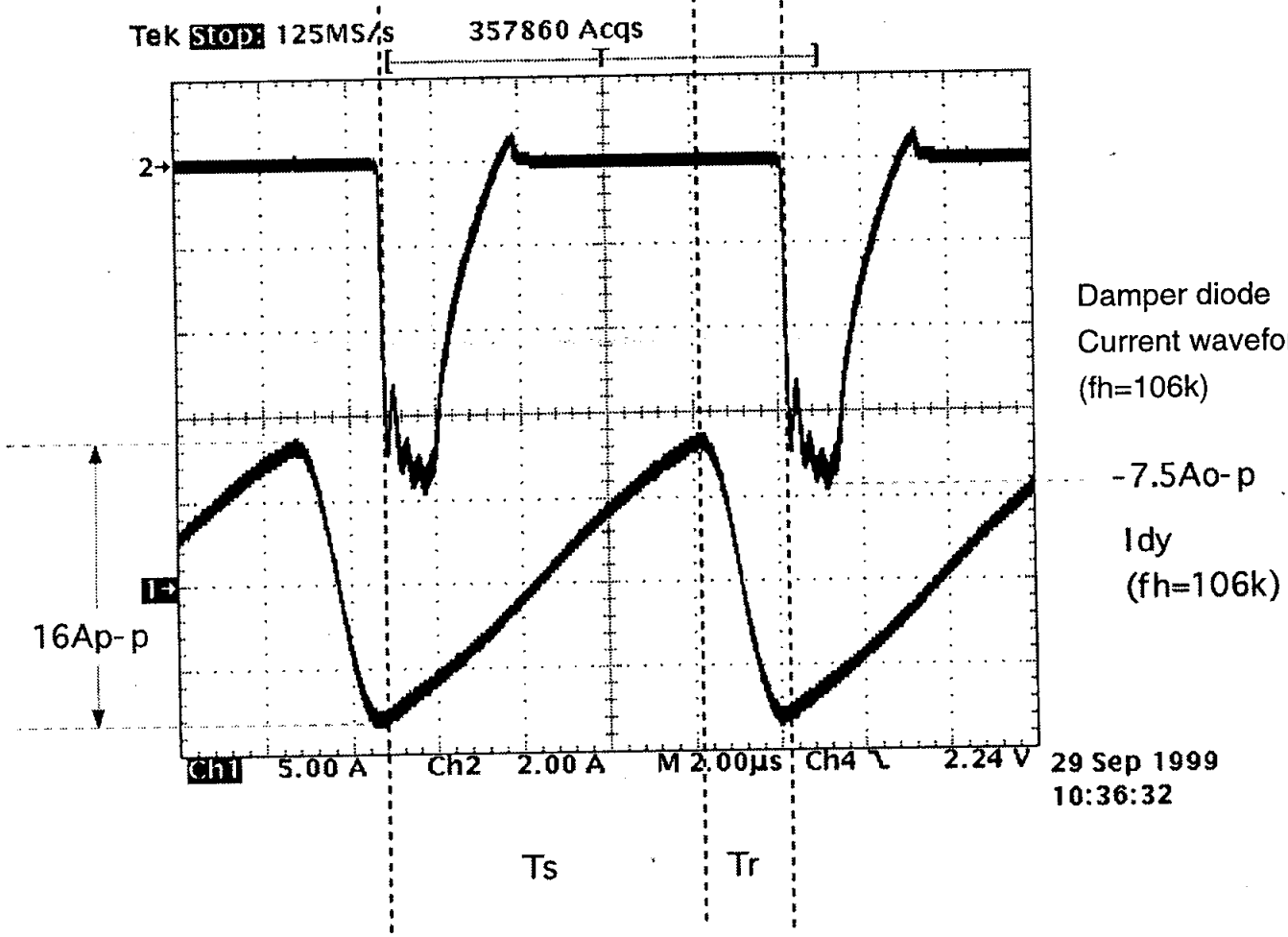

0
IC700 output waveform
0
Q501 Vce
0
Q502 Ib
Ton
0
Q502 Vbe
Ip
0
Q502 Ic
Vcp
0
Q502 Vce
0
Dumper diodes current waveform
-Ip
Tr
Ts
0
Idy

Figure 6

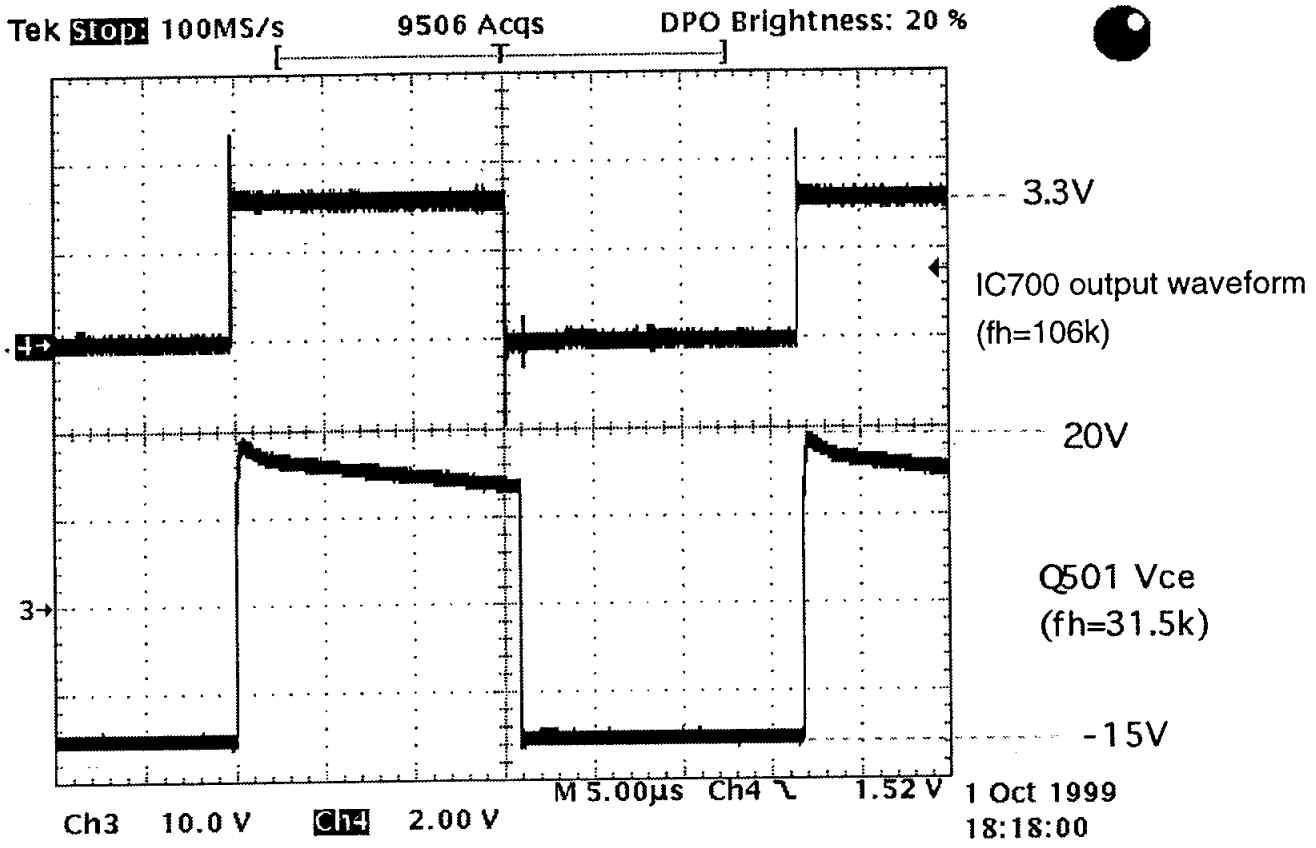
Figure 7. Deflection circuit waveform while fh=106k

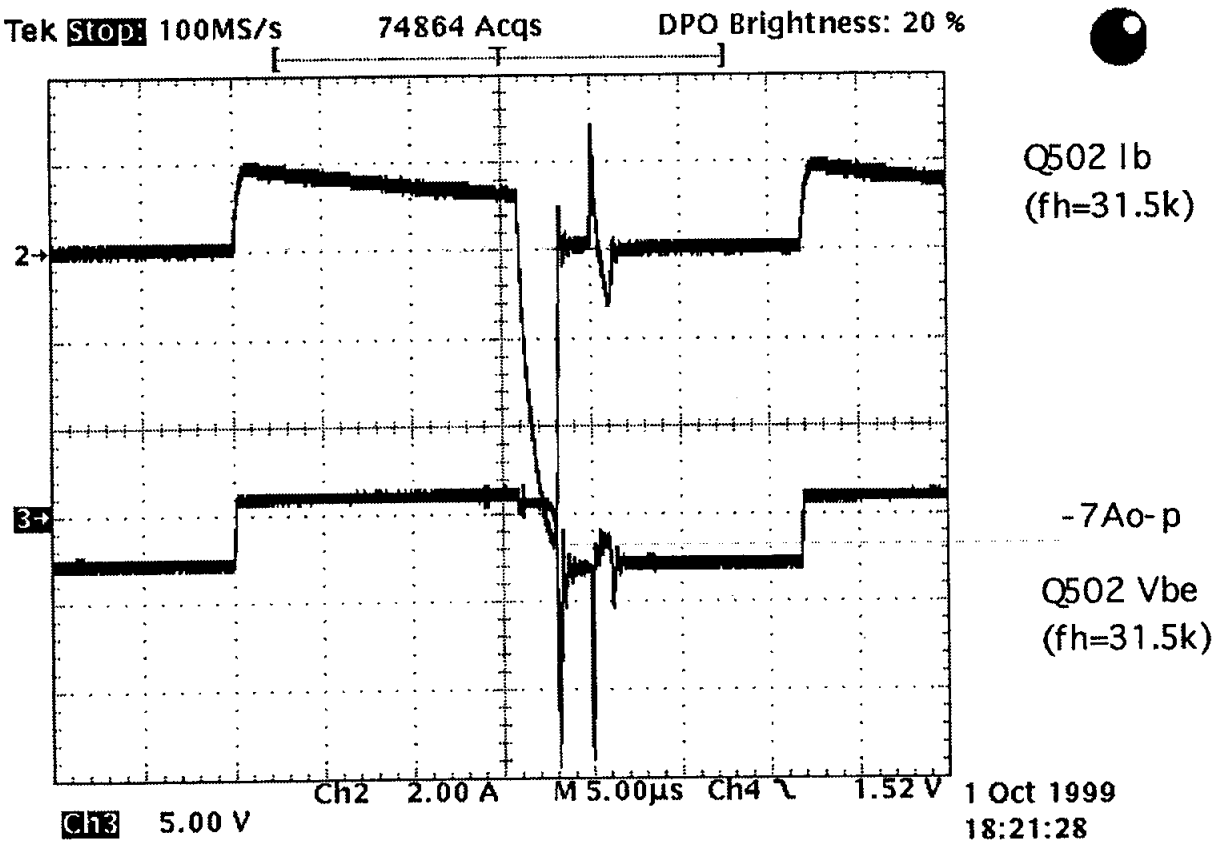


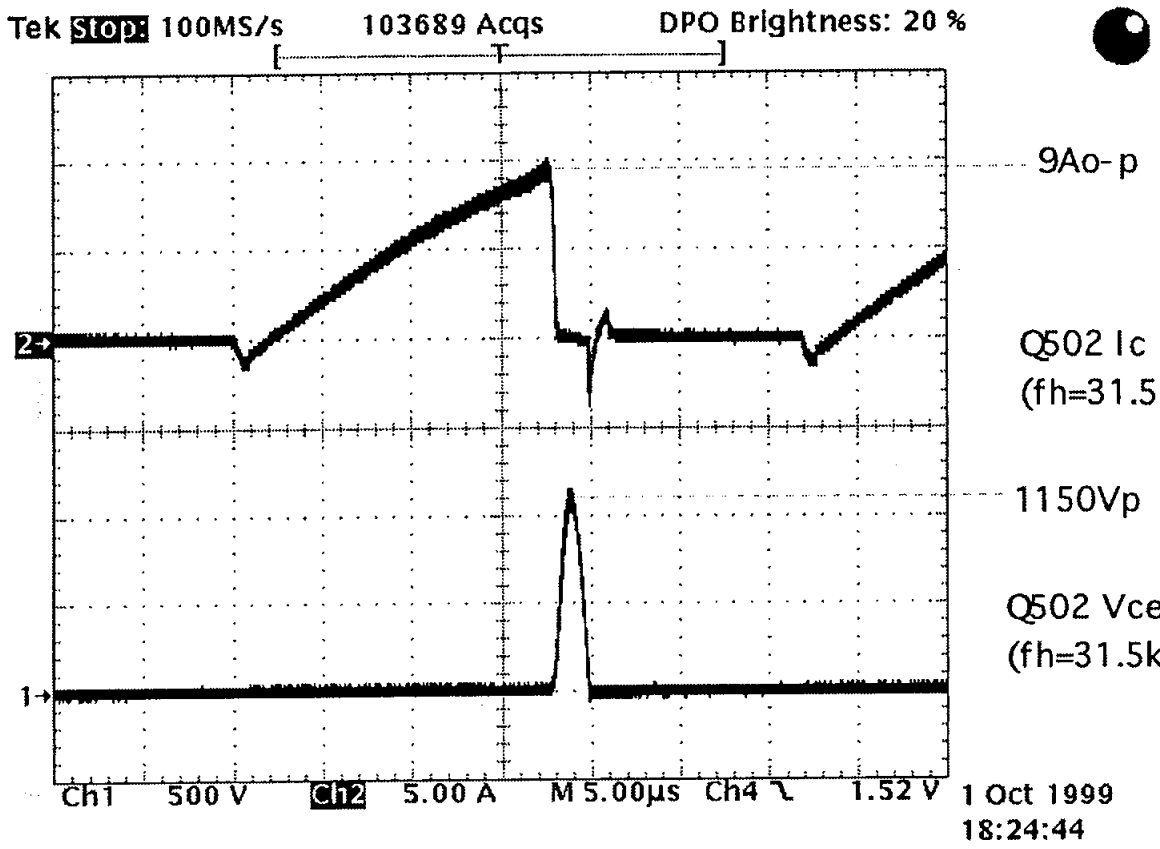

Tek Stop: 125MS/s
45704 Acqs
8Ao-p
Q502 Ic
(fh=106k)
1100Vp
Q502 Vce
(fh=106k)
Ch1 500 V
Ch2 5.00 A
M 2.00µs
Ch4 2.24 V
29 Sep 1999
10:26:28

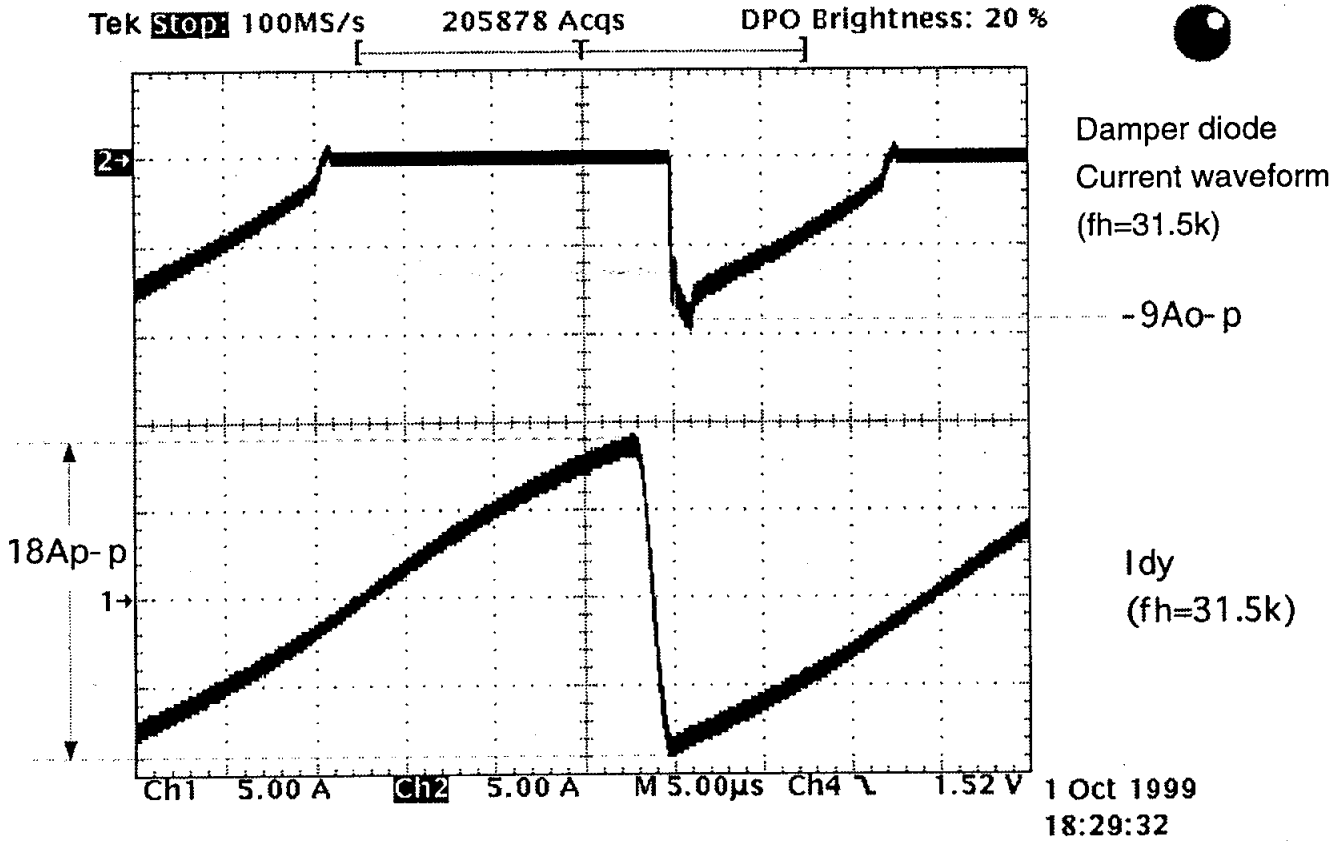

Tek Stop: 125MS/s
357860 Acqs
Damper diode
Current waveform
(fh=106k)
-7.5Ao-p
Idy
(fh=106k)
16Ap-p
Ch1 5.00 A
Ch2 2.00 A
M 2.00µs
Ch4 2.24 V
29 Sep 1999
10:36:32
Ts
Tr

Deflection circuit waveform while fh=31.5k






Tek Stop: 100MS/s 103689 Acqs DPO Brightness: 20 %
9Ao-p
Q502 Ic
(fh=31.5k)
1150Vp
Q502 Vce
(fh=31.5k)
Ch1 500 V Ch2 5.00 A M 5.00µs Ch4 1.52 V
1 Oct 1999
18:24:44


Tek Stop: 100MS/s 205878 Acqs DPO Brightness: 20 %
Damper diode
Current waveform
(fh=31.5k)
-9Ao-p
18Ap-p
Idy
(fh=31.5k)
Ch1 5.00 A Ch2 5.00 A M 5.00µs Ch4 1.52 V
1 Oct 1999
18:29:32

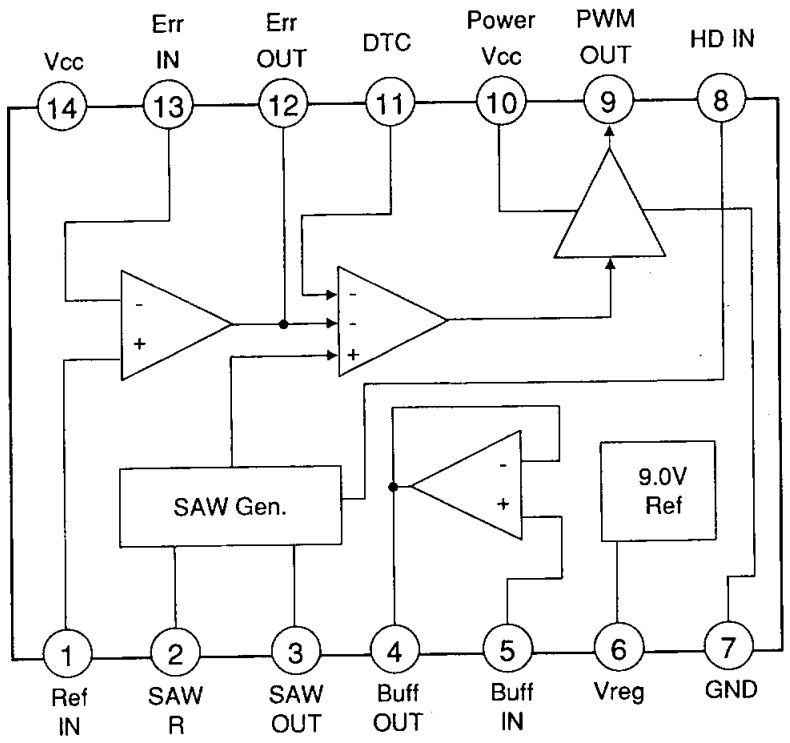


Figure 8. IC5J2 block diagram

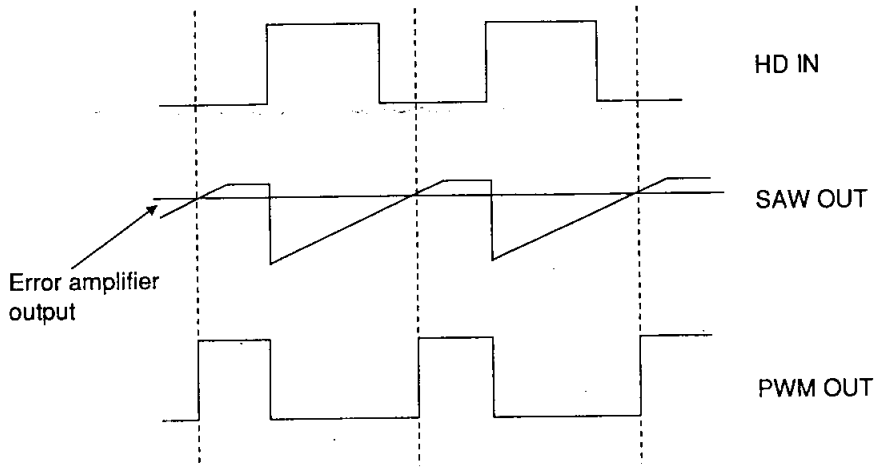


Figure 9. Operation image

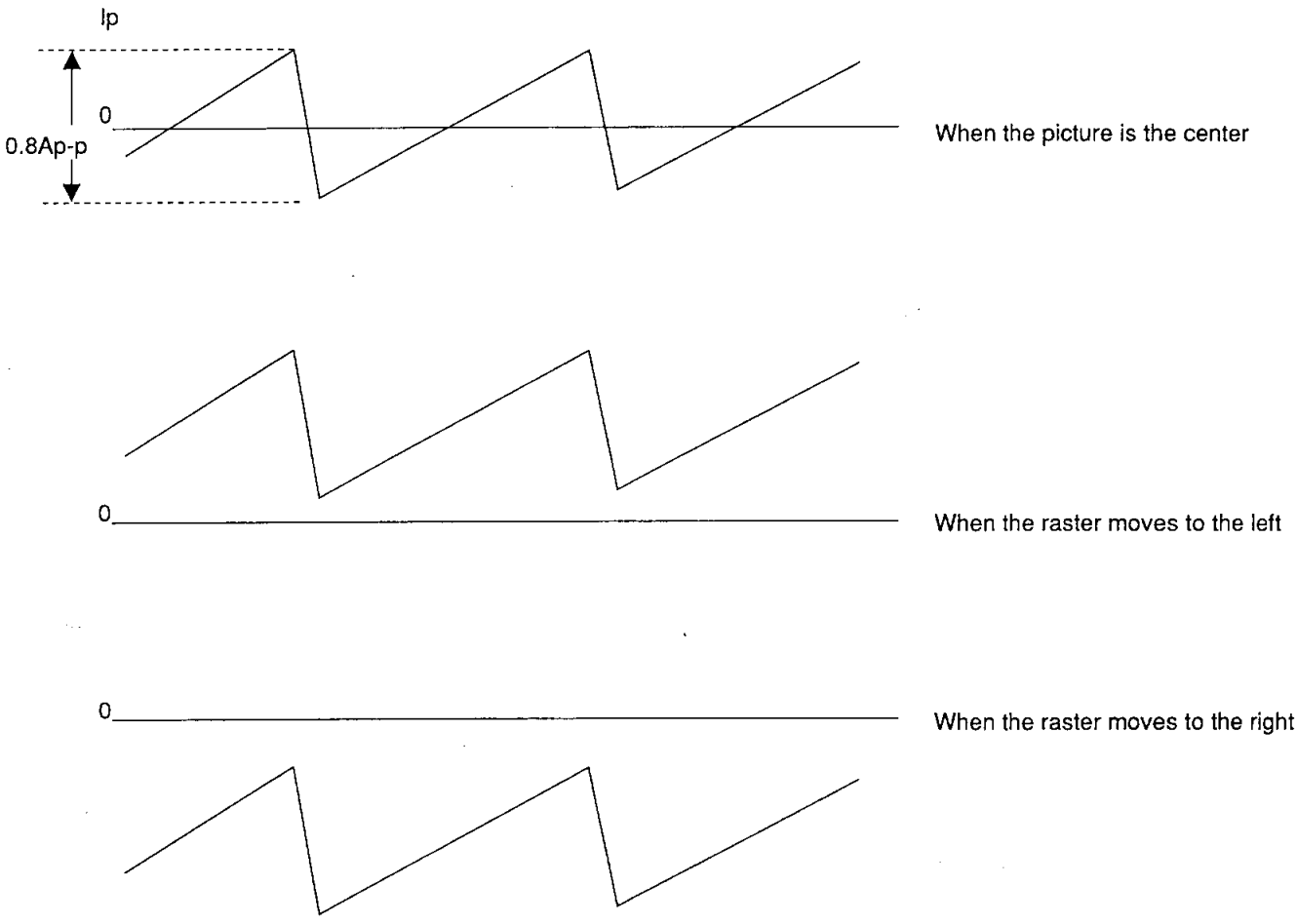

Ip
0
0.8Ap-p
When the picture is the center
0
When the raster moves to the left
0
When the raster moves to the right

Figure 10

1.2.2 Deflection current compensation circuit

As the picture becomes flatter, the arrival distance of the deflected electronic beam becomes more different between the center and both ends of the picture. Therefore, there is a tendency for the image to be contracted at the center of the picture and expanded at both ends of the picture. Moreover, the left side of the picture is more expanded than the right side of the picture owing to the characteristics of the circuit. CS applies S type compensation to the deflection current with the resonant effect of the deflection yoke and contracts at both ends of the horizontal axis. The linearity coil increases the inductance of the starting section of the deflection current with the supersaturated reactor, and works to contract the left side of the horizontal axis.

As the frequency is lower, the capacity of CS is generally increased and the linearity coil with a larger impedance value is used. In the practical circuit, seven CS capacitors are prepared, and are combined as desired. Two linearity coils are prepared, and whether one coil or the other is used is switched.

(1) S type compensation with CS

CS is switched in seven steps by FET. IC502 element with six FETs included and Q511 with one FET are used. On IC502, Pins 2, 5, 7, 9, 11 and 13 are used as the gate, and Pins 3, 6, 8, 10, 12 and 14 are used as the drain. Pins 1 and 15 are used as the ground, and each source are grounded to the earth. The binary value signal of HIGH (5V) or LOW (0V) is input to each gate by IC102. In case of HIGH, FET is turned ON. In case of LOW, FET is turned OFF. The correspondence to the signals from the capacitor and IC102 are as follows.

	G	D	Capacitor	Signal
FET1	2	3	C518	CS3
FET2	5	6	C517	CS2
FET3	7	8	C516	CS6
FET4	9	10	C515	CS7
FET5	11	12	C514	CS4
FET6	13	14	C525	CS5
FET7	—	—	C512	CS1

The column of G and D is Pin No.

(2) Compensation with linearity coil

The linearity coil is a special coil in which the magnet is used as the core of the coil and the inductance value varies depending on the flowing current. In the practical circuit, L507 and L508 are relevant. L507 is used with all frequencies but L508 is used at low frequencies only. To switch whether L508 is used or not, the relay RY501 of one pole type is used. Like CS, the binary value signal of HIGH (5V) or LOW (0V) is input to the base of Q505 by IC102. In case of HIGH, RY501 turns ON since Q505 turns ON. At this time, the deflection current does not flow through L508 but through RY501. On the other hand, RY501 also turns OFF as Q505 turns OFF in case of LOW. Therefore, the deflection current flows through L508 and L507.

As shown in the table below, CS is switched on the horizontal frequency bands, and the linearity coil is switched. 1/0 in the table express the signals from IC102 with 1 for HIGH and 0 for LOW. Here, the column of the frequency expresses the lower limit value.

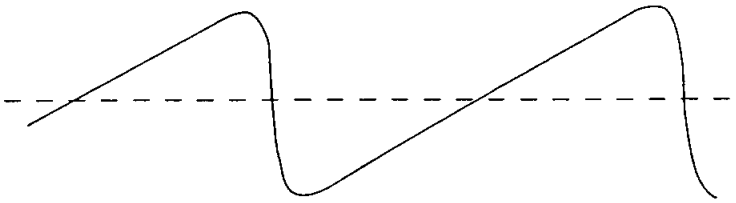
Frequency (kHz)	Lin-coil	CS7 C515	CS6 C516	CS5 C525	CS4 C514	CS3 C518	CS2 C517	CS1 C512
30	0	1	1	1	1	1	1	1
34	0	0	1	1	1	1	0	1
36.5	0	0	0	0	1	1	0	1
39	0	0	1	1	0	1	1	0
45	0	0	1	1	1	0	1	0
47.5	1	0	1	1	1	0	1	0
49	1	1	1	1	1	1	0	0
52	1	1	1	1	1	1	0	0
55	1	1	1	0	1	1	0	0
59	1	0	0	0	1	1	0	0
61	1	0	0	0	1	1	0	0
63	1	1	0	1	0	1	0	0
66	1	1	0	1	1	0	0	0
70	1	1	0	1	1	0	0	0
73	1	0	0	1	1	0	0	0
76	1	1	1	0	1	0	0	0
78.5	1	1	0	0	1	0	0	0
81.5	1	1	0	0	1	0	0	0
83	1	0	1	1	0	0	0	0
86.5	1	1	0	1	0	0	0	0
89	1	1	0	1	0	0	0	0
92	1	0	0	1	0	0	0	0
94	1	1	1	0	0	0	0	0
97	1	1	1	0	0	0	0	0
104	1	1	0	0	0	0	0	0
108	1	1	0	0	0	0	0	0

Here, the following timing is exceptional.

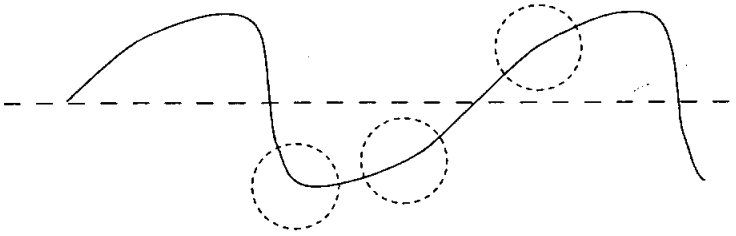
ap21 (68k/75)	1	1	1	1	1	0	0	0
80k/75	1	1	1	0	1	0	0	0

The waveform of the deflection current is compensated from Fig. (a) to Fig. (b) through the above. The starting section of the current is smoothened, and the linear section becomes the S type.

図(a)



図(b)



1.2.3 Vertical output circuit

The vertical deflection circuit controls the vertical width and vertical position with IC700 on the DEFL_SUB substract, and IC701 controls the linearity. Moreover, the signal output from IC701 is input to the vertical deflection output IC401.

1.3 High voltage circuit vlock

The high voltage circuit is composed of the high-voltage regulator H-IC601, flyback transformer (FBT) T601, operation amplifier IC602 and their peripheral circuits.

1.3.1 High voltage control

IC601 is an FBT drive H-IC unitized of the output MOS-FET (Q1) and its control section. Fig. 1 shows the block diagram. As the high voltage control system, the OFF trigger PWM control system is adopted. The OFF trigger control system turns OFF Q1 at the same time that when the horizontal sync. signal (hereafter called SYNC signal) input to Pin 13 (SYNC) of IC 601 is switched to Hi, in order to control the horizontal synchronization. The feedback signal (IC601 Pin 9) from FBT is compared with high voltage value setting voltage (IC601 Pin 10) from the MPU IC103 in the ErrAMP section in order to control the ON timing of Q1 (PWM control). Since the high-voltage detection voltage also drops when the high-voltage output voltage drops, the voltage of the capacitor CT of the ErrAMP section drops beyond the threshold value earlier than steady. Though Q1 is turned ON when it drops beyond the threshold value, the ON term of Q1 becomes longer than steady to increase the energy that generates the flyback pulse since the OFF timing of Q1 is synchronized with SYNC signal. (See Fig. 2.) As the result, the wave height value of the flyback pulse generated on the primary side of FBT increases to compensate for the dropped part of the high-voltage output voltage in order to achieve the stabilization. (27kV as normal)

1.3.2 Protective function

(1) Start and stop of high-voltage regulator IC601
When Vcc voltage (power voltage applied to Pin 8) reaches 10.4Vmin, IC601 outputs the drive pulse of Q1 to start the oscillation operation. Moreover, the drive pulse is fixed at Low to stop the oscillation operation when Vcc voltage (power voltage applied to Pin 8) becomes lower than 9.9Vmax (Vcc(La-off) voltage).

(2) IC601 pulse-by-pulse overcurrent protective (OCP) function
The peak value of drain current of MOS-FET (Q1) in IC601 is detected every pulse. When the voltage of Pin 17 of IC601 that detects both-end voltage of the source resistors (R607-R628) exceeds 0.75V, the DRIVE will be stopped until the next SYNC signal is input.

(3) IC601 overload protective (OLP) function
The function stops latching when it is continuously overloaded to continuously activate OCP. The time constant is generated by C609. When OCP is activated, C609 will be charged. When both-end voltage of C609 exceeds 5V, IC601 will come into the latch mode to stop the control operation. This state will not be released until the power SW is turned OFF (the voltage at Pin 8 of IC601 drops beyond Vcc (La-off) voltage).

(4) IC601 heat protective (TSD) function
When the frame temperature of the control IC section in IC601 exceeds 140°C (MIN), IC601 will come into the latch mode to stop the control operation. The state will not be released until the power SW is turned OFF (the voltage at Pin 8 of IC601 drops beyond Vcc (La-off) voltage).

(5) Overvoltage protective function of anode voltage (X-ray protector)
Voltage that is proportional to the high voltage value is generated in Pin 5 of T601 according to the coil ratio of the secondary coil and tertiary in FBT. The voltage is rectified by D612 and C621. Then, the voltage that is then divided by R636 and R637 is input to Pin 3 (+ terminal) of the operation amplifier IC602 in order to be compared with the X-PRO set voltage applied to Pin 2 (- terminal) from the MPU IC103. Though Pin 1 (output terminal) of IC602 is ordinarily Low (-15V output), Pin 1 (output terminal) becomes Hi (+12V output)

when the voltage at Pin 3 (+ terminal) of IC602 exceeds the voltage at Pin 2 (- terminal). Then, it is output to Pin 15 (X_PRO terminal) of IC601 via D605. When the voltage at Pin 15 of IC601 exceeds +5V, IC601 will come into the latch mode to stop the oscillation operation. The state will not be released until the power SW is turned OFF (the voltage at Pin 8 of IC601 drops beyond Vcc (La-off) voltage).

The overvoltage protective function is set to be activated when the high voltage value reaches 30.5kV.

(6) Beam current overcurrent protective function (beam protector)

The beam current is supplied through R617 from +12V power. Since the both-end voltage of R617 varies depending on the beam current value, the voltage drop caused by R617 becomes larger as the beam current increases. The voltage fluctuation is detected by Pin 6 of IC602, and is compared with the Beam-PRO set voltage that is input to Pin 5. The voltage of Pin 7 (output terminal) is linearly output against the voltage fluctuation caused by R619 and R620. However, IC601 comes into the latch mode to stop the oscillation operation when the terminal voltage of Pin 15 (X-PRO terminal) of IC601 exceeds +5V. The state will not be released until the power SW is turned OFF (the voltage at Pin 8 of IC601 drops beyond Vcc (La-off).)

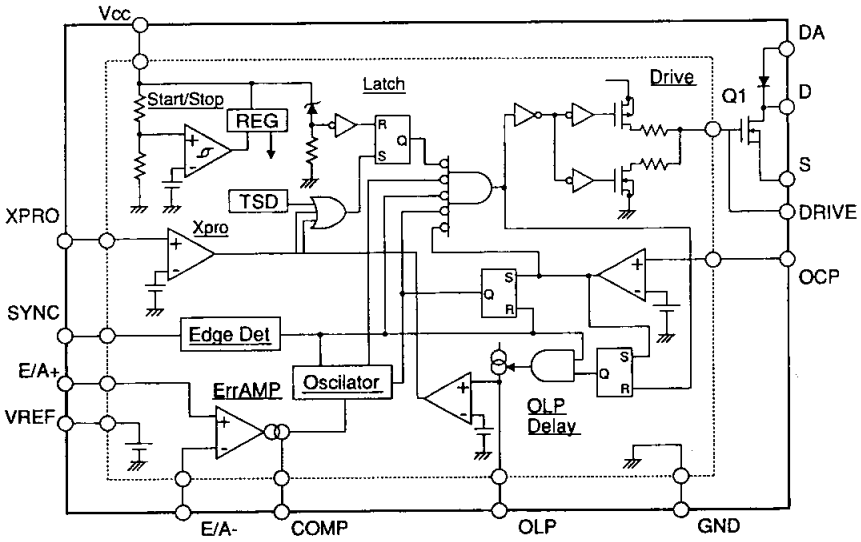
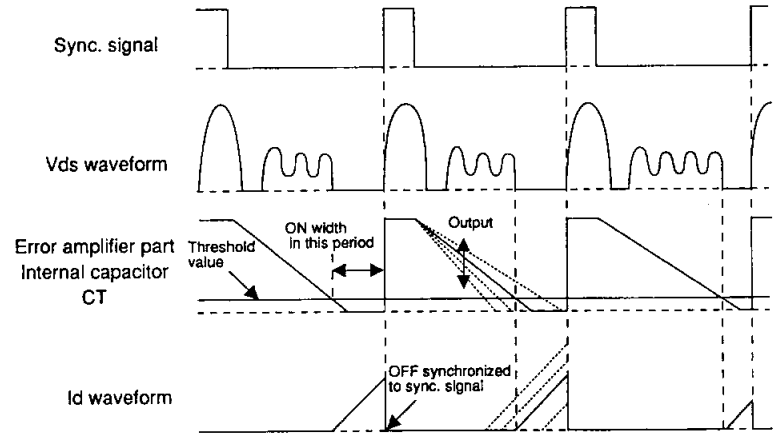


Figure 11. High voltage regulator IC601 block diagram



* The inclination of the capacitor CT changes with the output of error amplifier.
Q1 is turned ON when the capacitor voltage is lower than the threshold value.

Figure 12. OFF trigger PWM control system timing chart

1.3.3 DBF (Dynamic Beam Focus) circuit

Since the display is flattened, the focus becomes unequal between the center and circumference of the picture. To compensate for it, it is necessary to superimpose the parabola voltage of 370Vp-p in the horizontal cycle with the static focus and the parabola voltage of 145Vp-p in the vertical cycle. The slight voltage that is generated from the parabola voltage generating circuit is amplified and reversed to generate the high voltage in order to keep the focus equal. This circuit is called DBF circuit.

As shown in Fig. (b), the circuit is composed of the parabola voltage generating circuit IC700, amplifier section IC7A0 in the front step, Q6E1 to Q6E6 of amplifier section in the rear step, T6E1, and so on.

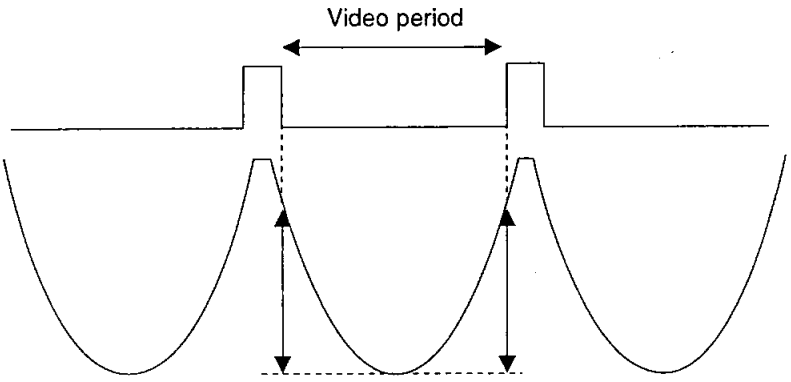


Figure (a)

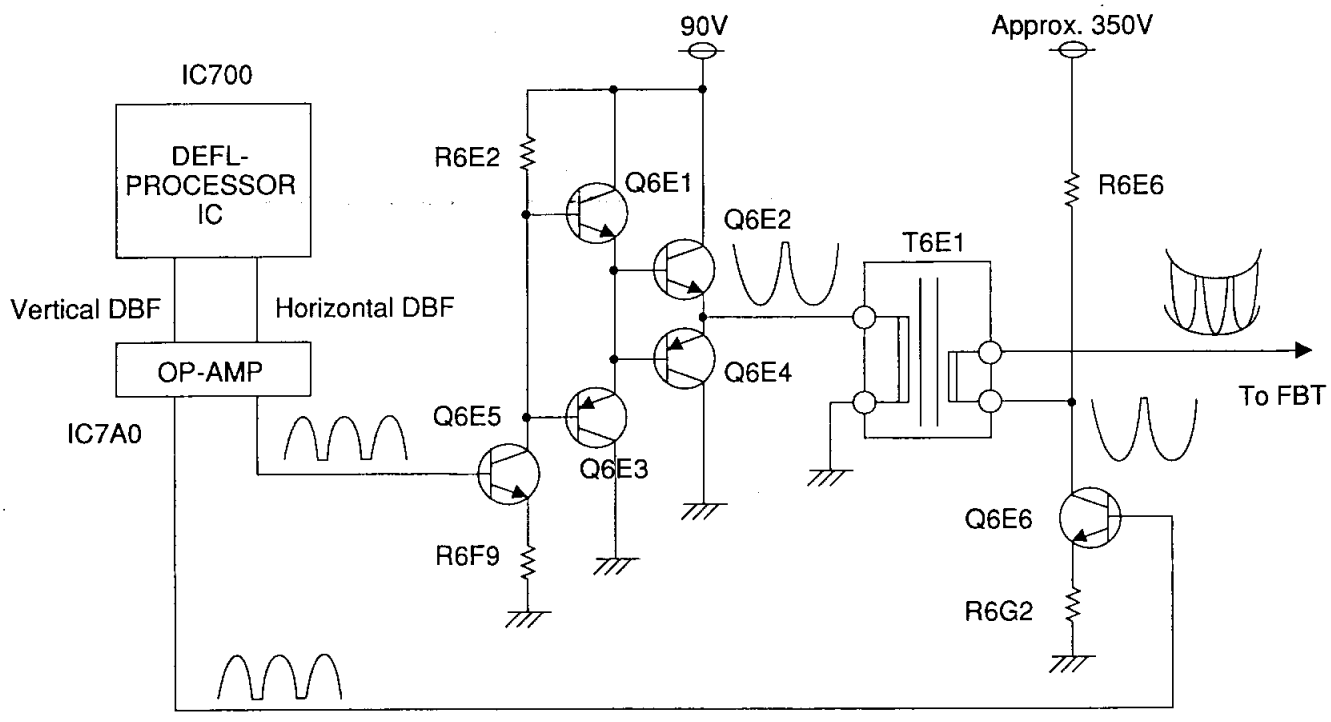


Figure (b)

After the horizontal and vertical DBF voltage are separately generated, they are amplified and are finally composed.

<Horizontal section>

The voltage (approx. 0.5Vp-p) of the parabola waveform shown in Fig. (a) is output from the deflection processor IC (IC700), and is amplified approx. 16 times by OP-AMP (IC7A0). Thereafter, it is amplified to 50 to 60Vp-p by the transistor (Q6E1 to Q6E5). The amplification ratio is determined by the ratio between the resistors R6E2 and R6F9, being approx. 8 times. Moreover, the waveform is reversed as shown in Fig. (b) at this time. Then, it is amplified to approx. 500Vp-p by DBF transformer (T6E1). The coil ratio between the primary and secondary coils of the DBF transformer is 1: 10, being the amplification ratio of approx. 10 times.

<Vertical section>

The voltage (approx. 0.6Vp-p) of the parabola waveform shown in Fig. (a) is output from the deflection processor IC (IC700), and is amplified approx. 13 times by OP-AMP (IC7A0). Thereafter, it is amplified to approx. 160Vp-p by the transistor (Q6E6). The amplification ratio this time is determined by the ratio between R6E6 and R6G2, being approx. 100 times.

The horizontal and vertical DBF voltages amplified and reversed are composed by applying vertically synchronous modulation to the output on the secondary side as shown in Fig. (c). The composed voltage is input to Pin 12 of the flyback transformer (T601).

Figure (a)

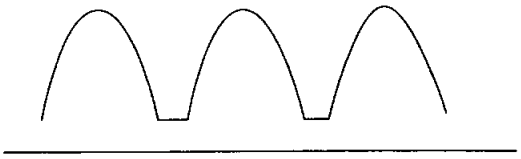


Figure (b)

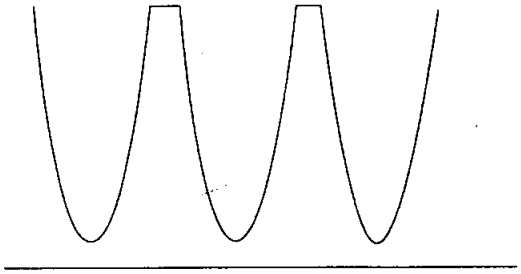
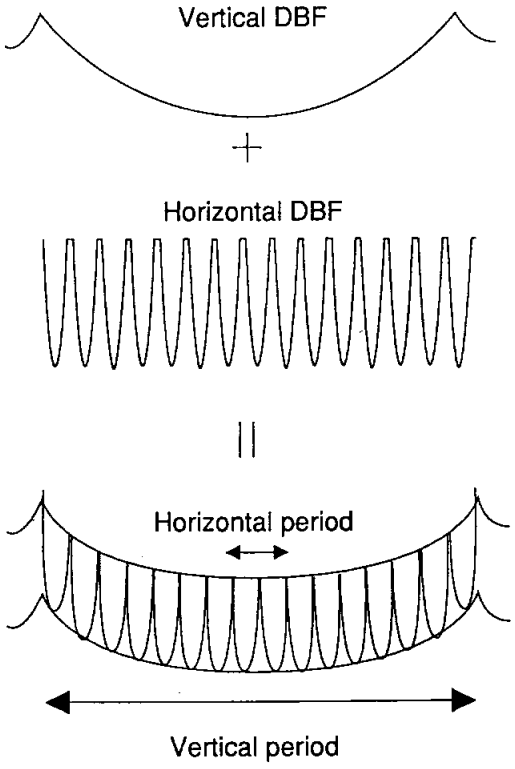


Figure (c)



1.4 Control circuit block

1.4.1 Rotation circuit

The rotation circuit is a circuit to compensate the picture inclination caused by the earth magnetism by letting DC current flow to the rotation coil wound on the front side of DY for adjustment. It is controlled to 0 to 5V with the reference of 2.5V by IC103#4(PWM_DAC), and DC current of +/-110mA (max) is made to flow to the rotation coil by IC8A4#2.

1.4.2 Corner purity circuit

The corner purity circuit is a circuit to compensate for the color shade and color deviation of the picture corner. On the rear side of CRT, it is adjusted by DC current flowing to the corner purity coils installed in the four corners on the display surface.

The compensation circuit is composed of the following three functions of (1) User (automatic adjuster) adjustment (OSD display), (2) Aging variation compensation and (3) High/low temperature drift compensation.

(1) User (automatic adjuster) adjustment (OSD display)

The user (automatic adjuster) causes DC current of +/-60mA (max.) to flow to the purity coil of each corner according to the value displayed on OSD.

(2) Aging variation compensation

As the electronic beam collides with the aperture grille, it is thermally expanded and contracted. The thermal expansion/contraction is varied according to the elapse of the power ON/OFF time of the monitor. The color shade and deviation of the picture corner thus generated are automatically adjusted.

The voltage of the beam current supply pin (FBT #10) is detected with R629/R630, and the voltage that detects the time elapse of the power ON/OFF of the monitor is read from the CR charge (integration) circuit composed of C127 and R141 and Cr discharge circuit (integration) circuit through IC100 (buffer amplifier) by IC103#15(CPU_ADC), and the DC current of +/-19mA(max) flows to the purity coil on each corner according to the specified control program.

(3) High/low temperature drift compensation

The front panel (glass) is thermally expanded and contracted as the temperature varies in the installation environments of the monitor. The color shade and deviation of the picture corner are automatically adjusted. The voltage that detects the temperature variation of the installation environments of the monitor is read from the environment temperature detection circuit composed of TH100 (thermistor) arranged near the front panel (glass) by IC103#13(CPU_ADC), and DC current of +/-11mA (max) is made to flow to the purity coil on each corner according to the specified control program.

- The left upper corner on the display surface is controlled with 0 to 5V of 2.5V reference by IC8A0#1(I2C control_DAC), and the DC current of the above value is made to flow to the purity coil on the left upper corner by IC8A3#2.
- The right upper corner on the display surface is controlled with 0 to 5V of 2.5V refer ence by IC8A0#2(I2C control_DAC), and the DC current of the above value is made to flow to the purity coil on the right upper corner by IC8A3#8.
- The left lower corner on the display surface is controlled with 0 to 5V of 2.5V reference by IC8A0#3(I2C control_DAC), and the DC current of the above value is made to flow to the purity coil on the left lower corner by IC8A2#2.
- The right lower corner on the display surface is controlled with 0 to 5V of 2.5V reference by IC8A0#4(I2C control_DAC), and the DC current of the above value is made to flow to the purity coil on the right lower corner by IC8A2#8.

1.4.3 Earth magnetism canceler circuit

The earth magnetism canceler circuit is divided into the south-north horizontal magnetic field canceling function and vertical magnetic field canceling function.
IC303 (earth magnetism sensor unit) detects the voltage and direction of the south-north horizontal magnetic field (IC303#2) and vertical magnetic field (IC303#1), and IC103#14 and 18(CPU_ADC) read the detected voltage to automatically control the following canceling function according to the specified control program.
Here, the output voltage of IC303 (earth magnetism sensor unit) operates as follows.

- South-north horizontal magnetic field (IC303#2): 0.5V(-0.04mT) to 2.5V(+/-0.00mT) to 4.0V(+0.04mT)
- Vertical magnetic field (IC303#1): 3.3V(-0.04mT) to 2.5V(+/-0.00mT) to 0.1V(+0.10mT)

<South-north horizontal magnetic field canceling function>

(a) Horizontal magnetic field landing cancel
The horizontal magnetic field landing cancel circuit is a circuit to compensate for the color shade and deviation that appear in the horizontal direction that becomes the opposite direction at the upper and lower ends on the monitor display surface, and the automatic adjustment is done by DC current flowing to the purity coil that is wound around the display surface. It is controlled to 0 to 5V of 2.5V reference by IC103#5(PWM_DAC) in order to cause the DC current of +/-90mA(max.) to flow to the purity coil from IC8A1#4.

(b) Horizontal magnetic filed convergence cancel
The horizontal magnetic field convergence cancel circuit is the circuit to compensate for the misconvergence that results after the vertical convergence of RED and BLUE in the whole display area of the monitor deteriorates, and it is automatically adjusted by DC current flowing to the 4V convergence compensation coil mounted on DY. It is controlled with the DC component (V-CONVERGENCE) by IC700#60(4V_SC), and DC current of +/-30mA (max) is flowen to the 4V convergence compensation coil by IC800#6 (PowerOpamp).

<Vertical magnetic field canceling function>

(a) Vertical magnetic field landing cancel
The vertical magnetic field landing cancel circuit is the circuit to compensate for the color shade and deviation that reaches its maximum at the center in the horizontal axis direction and its minimum at the upper and lower ends on the monitor display surface, and the automatic adjustment is done by DC current flowing to the speed modulating coil installed in the neck part of CRT.
It is controlled with 0 to 5V of 2.5V reference by IC103#6(PWM_DAC), and DC current of +/-140mA (max) is made to flow to the speed modulating coil by IC8A4#8.

(b) Vertical magnetic filed convergence cancel
The vertical magnetic field convergence cancel circuit is the circuit to compensate for the misconvergence that results after the vertical convergence of RED and BLUE reversed at the upper and lower ends on the whole display area of the monitor deteriorates, and it is automatically adjusted by the saw-toothed waveform (vertical frequency) current flowing to the 4V convergence compensation coil mounted on DY. It is controlled with the AC component (YVJT & YVJB, vertical frequency saw-toothed waveform) by IC700#60(4V_SC), and saw-toothed waveform (vertical frequency) current of +/-45mA (peak) is made to flow to the 4V convergence compensation coil by IC800#6(PowerOpamp).

1.4.4 Digital dynamic convergence clear (DDCD) circuit

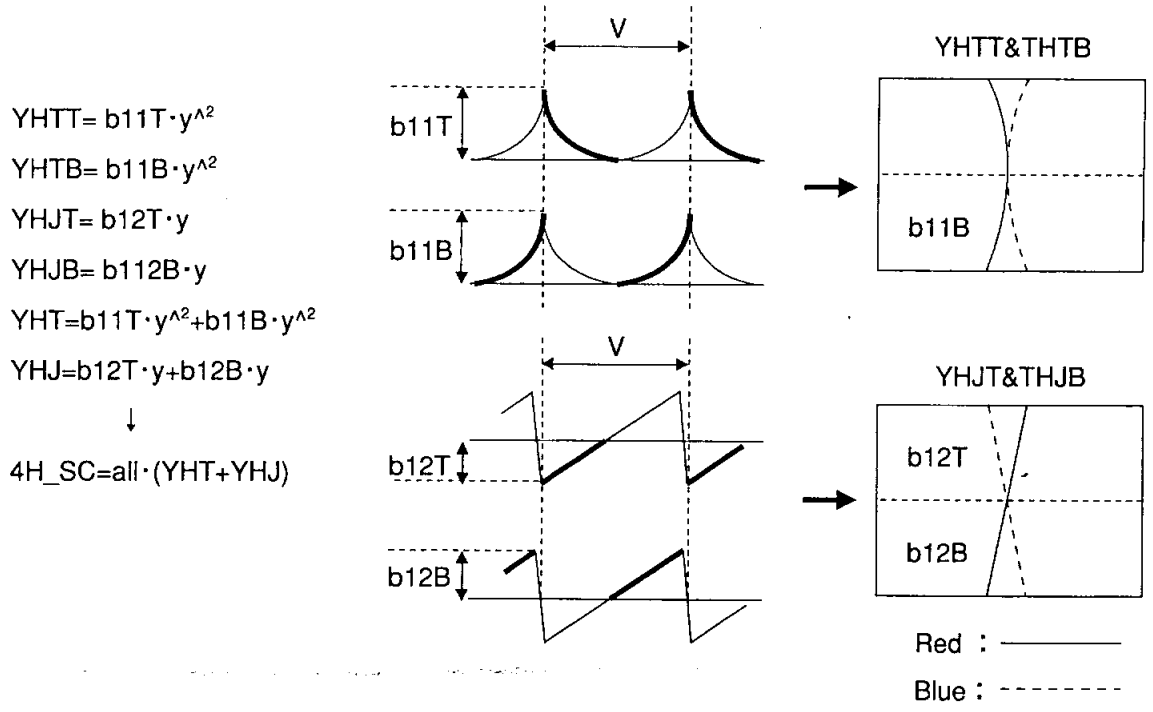
In the digital dynamic convergence clear (hereafter called DDCC) circuit, the convergence compensating current waveform is produced and amplified, and the convergence is compensated by the compensation current flowing to the sub yoke that is installed as the rear unit of the deflection yoke.

Though the principle of the convergence compensation with the sub yoke is same as the CP ring, the CP ring is used for the static variation with the parallel movement in the whole picture in the uniform magnetic field with the permanent magnet but the sub yoke is used for dynamic variation that compensates a desired position on the picture by controlling the current waveform that flows to the coil of the electric magnet.

- (See Fig. 13)

(1) Production of compensation current waveform

There are 18 kinds of compensation elements, and they are programmed in IC700(μPD61882) one by one by using the functions. The amplitude of the current is controlled by inputting the compensation coefficient into the function.



Examples of the functions and current waveform/compensation operation of YH(YHTT, YHTB, YHJT, YHJB) are shown as follows.

In the above formulas, b11T, b11B, b12T and b12B express the compensation coefficients, and y and y^2 express the primary and secondary functions of the vertical frequencies. The other parts except the compensation coefficients are programmed, and desired amplitudes (= compensation amount) are gained by varying the coefficients.

YHTT and YHTB compensate the upper and lower parts of the picture of the characteristic components of their DYs to compensate the upper and lower parts of the picture of the axis deviation component. The component gained by adding YHT and YHJ is multiplied by the offset compensation coefficient a11. The resultant component is regarded as 4H_SC, and is output from IC700(μPD61882)#61.

(2) Waveform, and operation on the picture

The case in which the currents flow through 4H coils of the sub yoke is explained. Regarding YHT (secondary function in the vertical frequency), in case of Fig. 1 as an example, the current is large in the same direction at the start (upper end of the picture) and the end (lower end of the picture) of the vertical frequency, and is zeroed on the X axis of the picture. Therefore, the magnetic field that is proportional to it is generated, and RED and BLUE vary in the same direction only at the upper and lower ends of the picture. As aforementioned, YHT can be independently controlled at the upper part (b11T.y^2) and lower part (b11B.y^2).

Moreover, regarding YHJ (vertical frequency primary function), if the flowing direction of the current is opposite at the start (upper end of the picture) and the end (lower end of the picture) of the vertical frequency as an example, RED and BLUE vary in the opposite direction only at the upper and lower ends of the picture. Compensation in the vertical direction can be done by making the current flow to the 4V coil.

Fig. 14 shows the image of each adjustment item of the DDCC adjustment.

(3) Adjustment method

Before the adjustment with the compensation circuit, it is necessary that they are properly adjusted at the center (H-STATIC and V-STATIC), on the X axis (XH slider, B-Bow 4P, XV differential coil) and on the Y axis (YH volume, YV volume).

Though DC current is superimposed on the sub yoke, H-STATIC and V-STATIC are pushed to the greatest possible extent by the adjustment with CP ring in order to reduce the stress of the driver IC800 (STK39-110).

Moreover, since 4H and 4V coils alone are installed on the chassis, it is first necessary that the convergence of RED, BLUE and GREEN (6H, 6V) satisfy the specifications for the performance of ITC(CRT&DY).

As the adjustment procedure, the adjustment values of 18 elements are not respectively zeroed but they are adjusted to nearest to zero with a total balance in good order.

In other words, the balance (compromise) adjustment with each adjustment item is applied.

The correspondence of the names of DDCC adjustment mode to the coefficients of all 18 elements is shown below.

<Factory mode>

4H Coil	b11T	YHTT	y^2	b11B	YHTB	y^2	b12T	YHJT	y	b12B	YHJB	y
	b21	4HTL	x^2·y^2	b31	4HTR	x^2·y^2	b41	4HBL	x^2·y^2	b51	4HBR	x^2·y^2
4V Coil	c11T	YVTT	y^2	c11B	YVTB	y^2	c12T	YVJT	y	c12B	YVJB	y
	c21	4VTL	x^2·y^2	c31	4VTR	x^2·y^2	c41	4VBL	x^2·y^2	c51	4VBR	x^2·y^2

<User & Factory mode>

4H Coil	a11	H-CONVERGENCE	DC
4V Coil	a12	V-CONVERGENCE	DC

(4) Block diagram

Fig. 15 shows the block diagram of the DDCC circuit.

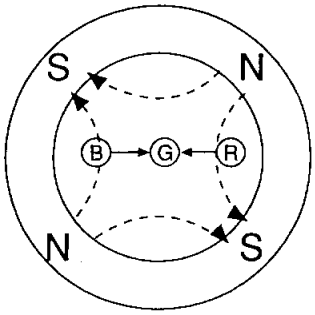
The components 4H_DC(#6), 4H_SC(#61), 4V_DC(#8) and 4V_SC(#60) supplied from IC700(μPD61882) to 4H-Coil and 4V-Coil are output, the dynamic component (4H_DC, 4V_DC) is amplified with IC7A0(TL084), and the static component (4H_SC, 4V_SC) is amplified with IC7A2(KIA4588).

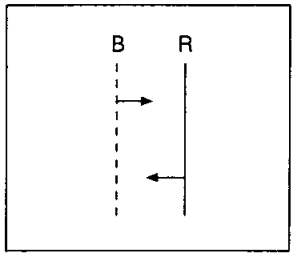
DCC(#7) output from IC700(μPD61882) and DEFL_+3.3V(#3) output from IC702 (TA48M033F) are respectively the reference voltage of Op-Amp(IC7A0:TL084) that amplifies the above dynamic component (4H_DC, 4V_DC) and the reference voltage of Op-Amp(IC7A2:KIA4558) that amplifies the static component (4H_SC, 4V_SC).

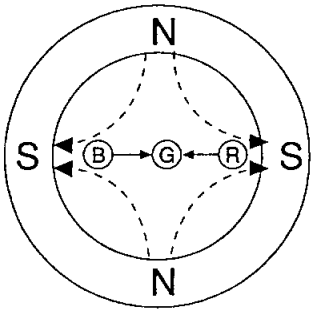
On each of 4H and 4V, the waveform added with the dynamic component and static component is input to IC800#3 and 4(STK391-110) allow the specified current to flow to each convergence compensation coil.

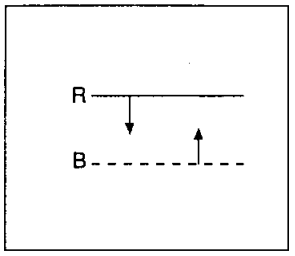
For four poles magnetic field

Static change by
the eternal magnetic field
(Parallel shifting totally)



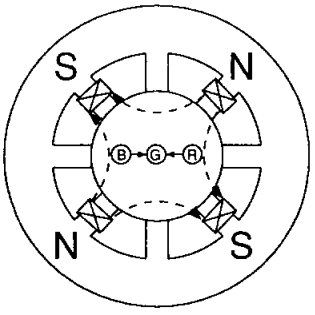


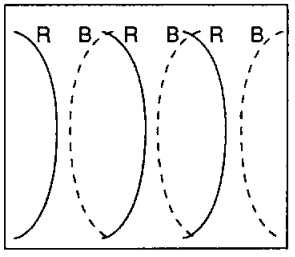




Dynamic change by
electromagnet
(Compensate at the
optional position on the picture.)

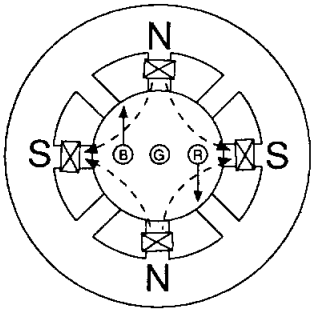
4H coils

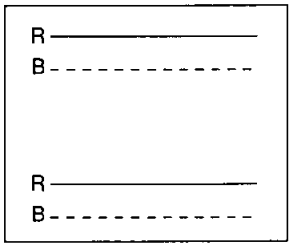




YHT compensate

4V coils





YVT compensate

Figure 13

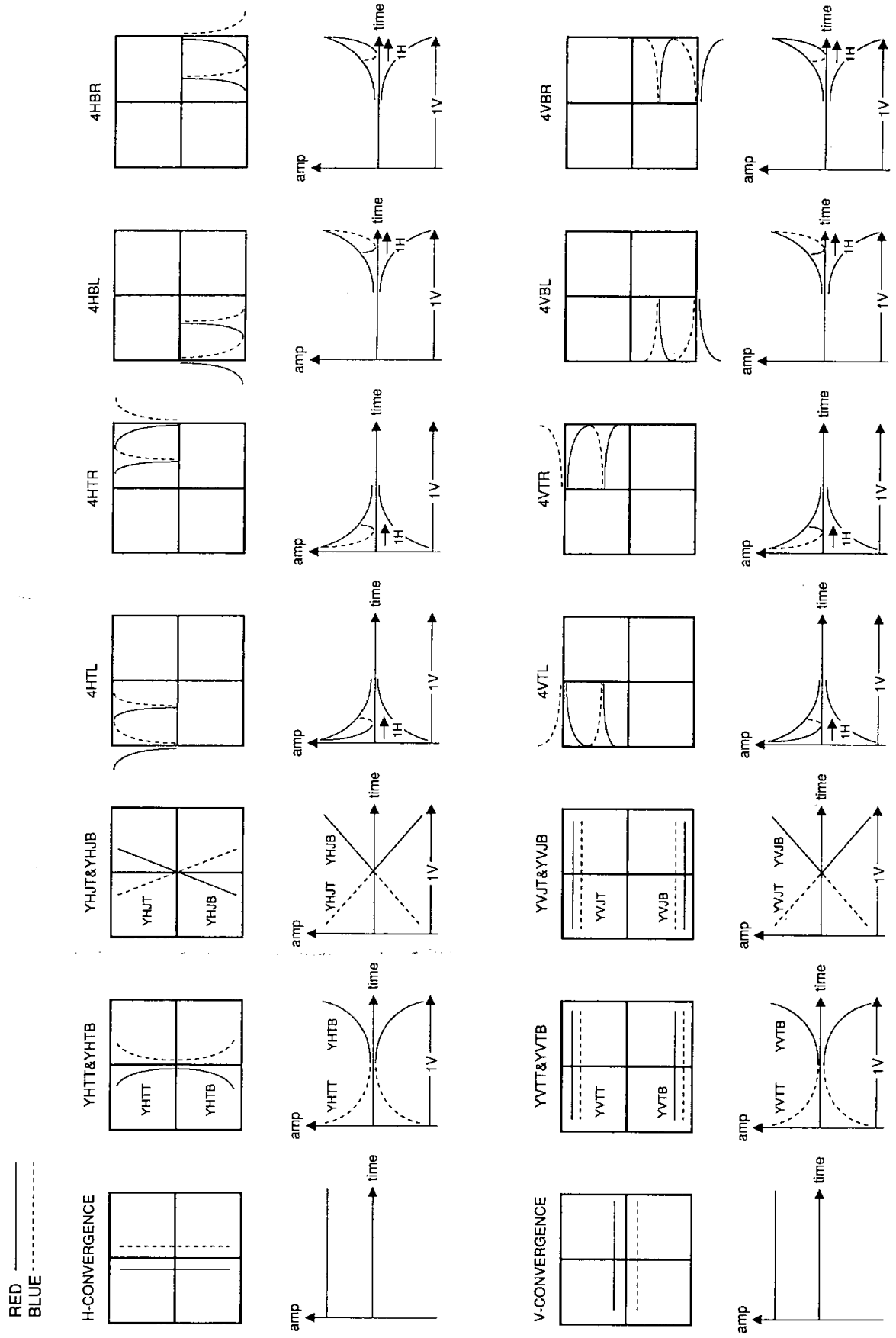

RED
BLUE
H-CONVERGENCE
YHJT&YHJB
YHJT
YHJB
YHTT&YHTB
YHTT
YHTB
4HTL
4HTR
4HBL
4HBR
V-CONVERGENCE
YVJT&YVJB
YVJT
YVJB
YVTT&YVTB
YVTT
YVTB
4VTL
4VTR
4VBL
4VBR
time
amp
1H
1V

Figure 14

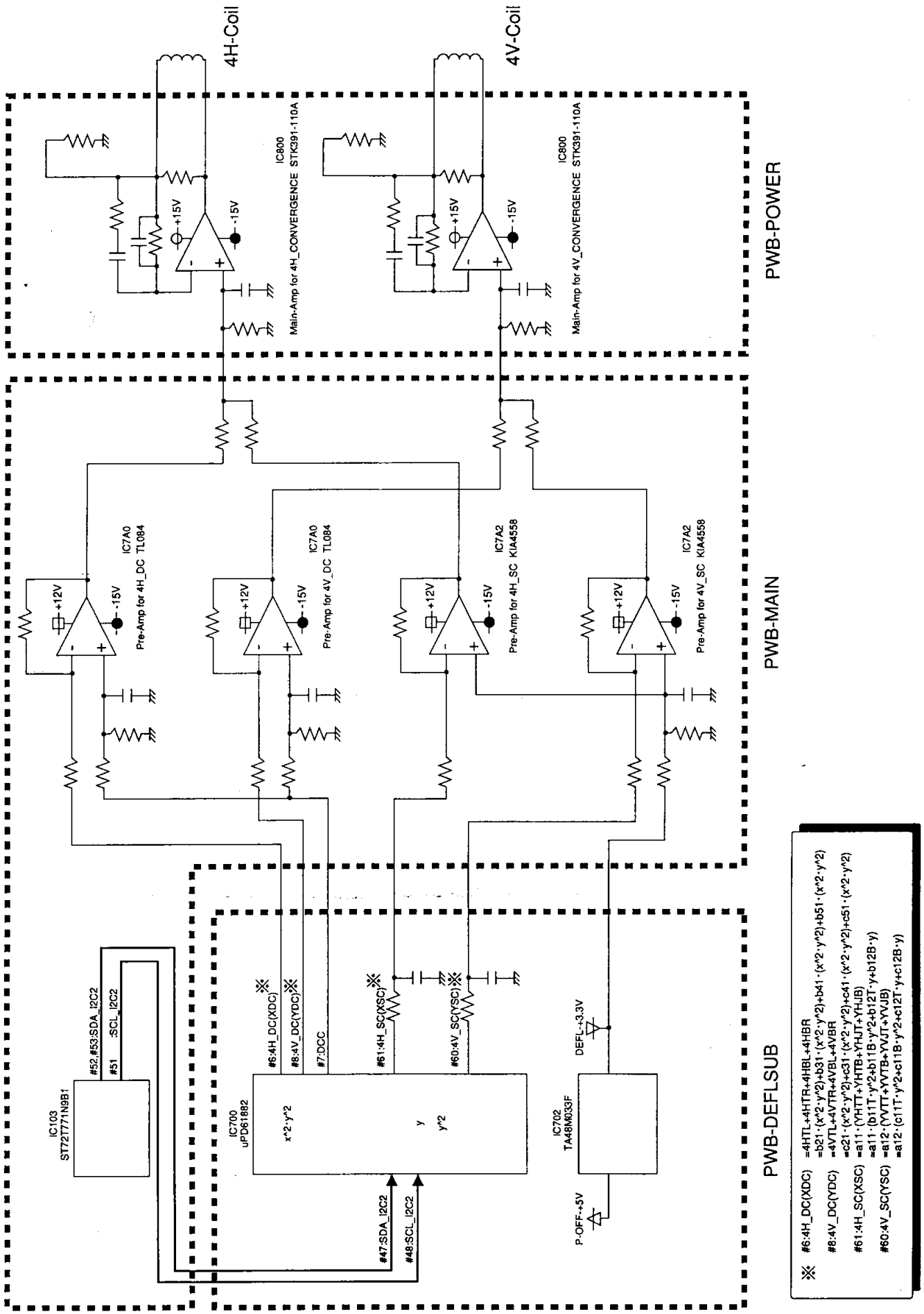

4H-Coil
4V-Coil
PWB-POWER
PWB-MAIN
PWB-DEFLSUB
IC800 STK391-110A
Main-Amp for 4H_CONVERGENCE
Main-Amp for 4V_CONVERGENCE
IC7A0 TL084
Pre-Amp for 4H_DC
Pre-Amp for 4V_DC
IC7A2 KIA4558
Pre-Amp for 4H_SC
Pre-Amp for 4V_SC
+12V
-15V
IC103 ST72T771N9B1
IC700 uPD61882
IC702 TA48M033F
DEFL-+3.3V
P-OFF-+5V
#52,#53:SDA_I2C2
#51 :SCL_I2C2
#6:4H_DC(XDC)
#8:4V_DC(YDC)
#7:DCC
#61:4H_SC(XSC)
#60:4V_SC(YSC)
#47:SDA_I2C2
#48:SCL_I2C2
x^2·y^2
y
y^2
※ #6:4H_DC(XDC) =4HTL+4HTR+4HBL+4HBR
=b21·(x^2·y^2)+b31·(x^2·y^2)+b41·(x^2·y^2)+b51·(x^2·y^2)
#8:4V_DC(YDC) =4VTL+4VTR+4VBL+4VBR
=c21·(x^2·y^2)+c31·(x^2·y^2)+c41·(x^2·y^2)+c51·(x^2·y^2)
#61:4H_SC(XSC) =a11·(YHTT+YHTB+YHJT+YHJB)
=a11·(b11T·y^2+b11B·y^2+b12T·y+b12B·y)
#60:4V_SC(YSC) =a12·(YVTT+YVTB+YVJT+YVJB)
=a12·(c11T·y^2+c11B·y^2+c12T·y+c12B·y)

Figure 15

1.5 Control block

The control block is composed of the following:
Monitor MPU IC103 to process the sync. signals, control the inside of the monitor and communicate with the external, EEPROM IC105 to memorize the picture adjustment values, etc., I/O expander IC102 to convert the serial data of I2C bus to the CS switch signal, and others.

1.5.1 Sync. signal process

When GSYNC of the separated image signals is input from the interface board to the MPU #30 as HSYNC or composite SYNC and to #20 as VSYNC, the frequency/polarity of SYNC will be discriminated. Then, HS_OUT will be output from #27 for beam deflection and OSD display and VS_OUT will be output from #26 as the polarity POSI.
If Separate, Composite and Sync on Green are input at the same time, they will be recognized in the sequence of Composite, Separate and Sync on Green from the highest priority.
If SYNC is not input or abnormal SYNC is input, the MPU will output simulative SYNC. The frequency of the simulative SYNC is near that of the previously input SYNC.
(Initial values: FH:31KHz and FV:75Hz)
If anything other than GSYNC is input, S/GSEL signal of #25 will be set at LOW and GSYNC input will be cut.

1.5.2 Front button

When a tact switch SW100 on the front panel is pressed, the voltage of +5V will be divided with the resistor according to the button.
The signal is converted into the digital value with the A/D converter of the MPU #12 to discriminate which button is pressed.

1.5.3 I2C bus control

For IC control in the monitor, I2C bus of two systems of I2C_1(#36:SCL, #37:SDA) and I2C_2 (#51:SCL, #52:SDA) is used. The adjustment data is read from EEPROM according to the input timing, and is sent to each IC.

Slave address list

[I2C-1]

Item	Source	ADR(BIN)
Preamplifier	IC301	10001000
OSD	IC300	01111100
DAC (Cut off)	IC305	10011000

[I2C-2]

Item	Source	ADR(BIN)
E2PROM	IC105	1010000*
Dflection processor	IC700	11011100
I/O expander (CS)	IC102	01110000
DAC(CPURITY)	IC8A0	10011000

1.5.4 Power control

The normal state and power management state are switched according to #17 P-OFF signal and #21 P-SUS signal.
"Power save" of the OSD adjustment item is turned to "ON", and the power management is activated when either H/VSYNC goes out.
In the power management mode, P-OFF+5V is turned OFF by setting #17 P-OFF signal at LOW, other power supplies except +5V and heater are turned OFF by setting #21 P-SUS signal at LOW.

Moreover, if #19 PRO signal is at H1 1 second or more, it will be regarded as a short circuit of the power of the secondary side to forcibly turn ON POWER SAVE in order to prevent trouble from being escalated.

1.5.5 CRT support

The voltage conversion signal is output from the earth magnetism sensor IC303: horizontal magnetic field from #2 and vertical magnetic field from #1. It is relayed through the reversal buffer: the horizontal magnetic field signal is input to A/D converter of the MPU IC103 #14 and the vertical magnetic field is input to the A/D converter of IC103 #18. The signal is converted to the digital value to detect the earth magnetism around the monitor.

The signal generated by dividing +5V with the thermistor TH100 and R111, R112 is input to A/D converter of IC103 #13, and is converted to the digital value. This detects the temperature in the monitor.

The monitor energization time signal is relayed through the buffer of IC100, is input to the A/D converter of IC103 #15, and is converted to the digital value. This detects the monitor energization time.

To cancel the purity and convergence from degradation due to the above earth magnetism, temperature and aging, the cancel current is flowen to H_PURITY, V_PURITY, C_PURITY and 4V coil.

H_PURITY is controlled by the signal that is gained by smoothening PWM DAC output of IC103 #5 with R119 and C110.

V_PURITY is controlled by PWM DAC output of IC103 #6. C_PURITY is controlled by the signal of the analog voltage that IC8A0 converts from the digital signal sent from the MPU to 4-channel DAC IC8A0 through the 12C bus.

The convergence 4V is controlled by the #60 output signal of the analog voltage that IC700 converts from the digital signal sent to the deflection processor IC700 through 12C bus from the MPU.

1.5.6 High voltage control

The high-voltage output voltage is controlled by the signal HV-ADJ that is passed through the buffer of IC104 after PWM DAC output of the MPU IC103 #2 is smoothened with R116 and C109.

Similarly, X ray protect voltage is controlled by the signal X-PRO_ADJ that is gained by passing PWM DAC output of IC103 #3 through the buffer of IC104.

1.5.7 Display Data Channel

Both SIGNAL A/B support DDC1/2B.

The DDC function of SIGNAL A is supported by IC201(EEPROM for DDC) on the interface board. EDID written in IC201 is output according to the clock that is input to #6 SCL or #7 VCLK of IC201.

The DDC function of SIGNAL B is supported by IC103 (MPU). Soon after the power of the monitor is turned ON, the MPU reads EDID from IC105. According to the clock input to #34 SCL or #20 VSYNC(VCLK), EDID is output.

IC103(MPU)Pin assingnment

PIN#	FUNCTION	ASSIGNMENT	PIN#	FUNCTION	ASSIGNMENT
1	DA0	SUB_BRT	56	VPP/TEST	GND
2	DA1	HV_ADJ	55	IRIN	GND
3	DA2	X-PRO ADJ	54	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$
4	DA3	ROTATION	53	PA0	SDA_I2C2
5	DA4	HCANCEL	52	PA1	SDA_I2C2
6	DA5	VCANCEL	51	PA2	SCL_I2C2
7	DA6	SW_LIN2	50	PA3	HSK
8	DA7	not used	49	PA4	WC
9	DA8	not used	48	PA5	not used
10	VSSA	GND(A)	47	PA6	not used
11	VDDA	+5V(A)	46	PA7/BLANKO	not used
12	PB7	KEY	45	OSCIN	OSCIN
13	PB6	THERM	44	OSCOUT	OSCOUT
14	PB5	X_OUT	43	USBVCC	USBVCC(3.3V)
15	PB4	BEAM	42	USBDP	USBDP
16	PB3	ACC	41	USBDM	USBDM
17	PB2	P-OFF	40	USBGND	USBGMD
18	PB1	Y_OUT	39	PC7/TDO(SCI)	SW_LIN1
19	PB0/VFBACK	PRO	38	PC6/RDI(SCI)	SDA_I2C1
20	VSYNCI1	VSYNC	37	PC5/SDAI(I2C)	SDA_I2C1
21	PD7/VSYNCI2/ITD	P_SUS	36	PC4/SCLI(I2C)	SCL_I2C1
22	PD6/CLAMPO	CLP	35	PC3/SDAD(DDC)	SDA_DDC
23	PD5/ITA	SPARK	34	PC2/SCLD(DDC)/RX	SCL_DDC
24	PD4/ITB	LOCK	33	PC1/HSYNCI2	SEL
25	PD3/ITC	S/G_SEL	32	PC0/OCMP/HFBACK	DEG
26	PD2/VSYNCO	VS_OUT	31	VDD	+5V(D)
27	PD1/HSYNCO	HS_OUT	30	HSYNCI1	HSYNC
28	PD0/CSYNCI	GSYNC	29	VSS	GND(D)

IC102(I/O expander) pin assignment

Signal name	PIN#
CS1	10
CS2	11
CS3	5
CS4	6
CS5	9
CS6	7
CS7	12
LIN	4

IC8A0(Corner purity DAC) pin assignment

Signal name	PIN#
CP-TL	1
CP-TR	2
CP-BL	3
CP-BR	4

1.5.8 LED

J100 #1 is connected to the anode of the green LED, J100 #3 is connected to the anode of the amber LED, and #2 is connected to the cathodes of both. Since +12V is normally supplied, the current flows to J100 #1 to turn OFF Q100. Therefore, any current does not flow to J100 #3. (The green LED only is lit.)

Since +12V is turned OFF in the power management mode, no current is not flowed to J100 #1 to turn ON Q100. Therefore, the current flows to J100 #3. (The amber LED only is lit.)

1.5.9 Clamp pulse

The clamp pulse signal CLP is output from #22 of the MPU IC103 #22 by the polarity POSI. When "FRONT" is selected in the OSD adjustment item "CLAMP PULS POSITION", the signal is triggered at the front edge of HSYNC, and when "BACK" is selected, the signal is triggered at the rear edge.

1.5.10 SPARK

If it is electrically discharged in the CRT tube, the GND level of the high-voltage system circuit is considerably varied. GND of this high-voltage system is connected to the MPU IC103 #23 via C137. The voltage level of IC103 #23 is normally set at HI. If GND in the high-voltage system varies since it is electrically discharged in the CRT tube, the current will flow to R168 to set IC103 #23 at the LO level. #23 is the external interrupt terminal that detects the trailing edge. When the trailing edge is detected, the MPU forcibly applies S/W RESET. (It is the same as when the power SW is turned ON.)
The above operation prevents the monitor from going out of control when it is electrically discharged in the CRT tube.

1.5.11 Avoidance operation during input SYNC switching

The horizontal LOCK output signal of the deflection processor IC700 #46 is connected to the MPU IC103 #24. JC103 #24 is the external interrupt terminal of the trailing edge detection. Though the voltage level of the LOCK signal is normally set at HI, IC700 outputs LO when the horizontal deflection lock is released since the input SYNC is switched.
When the MPU detects the trailing edge, the HSK signal of IC103 #50 is set at HI, and the simulative SYNC that is near the original frequency is output from #30 and #20. HSK signal is used to set +B, H-FOCUS voltage at MIN.
This reduces the stress when the input SYNC is switched for a short time.

1.5.12 Vertical linearity switch

The frequency characteristics of the vertical linearity are compensated by #39 SW_LINI and #7 SW_LIN2 output signals of the MPU IC103.
The switching patterns are shown in the table below.

SW_LIN1, SW_LIN2 select pattern

Vertical frequency	VLIN_SW1 #39	VLIN_SW2 #7
50Hz~73Hz	LO	LO
73Hz~90Hz	HI	LO
90Hz~125Hz	LO	HI
125Hz~160Hz	HI	HI

1.5.13 H/W RESET

The +5V power is connected to #2 of the voltage detector IC101, and IC101 #1 output is connected to the MPU IC103 #54.
On the voltage detector, #1 is the open drain output, being turned OFF when #2 voltage is 4.5V or more, and ON when it is 4.5V or less. When the power switch is turned ON, IC101 #1 is turned ON and the MPU #54 level is set at 0V since +5V has not started up.
When the voltage of IC101 #2 becomes 4.5V or more, IC101 #1 will be turned OFF, and the voltage of the MPU #54 rises with the time constants of R107 and C106.
When the voltage of the MPU #54 becomes 3.5V or more, the MPU will start operating.

1.5.14 Oscillation circuit

The crystal oscillator X100 is connected to the MPU IC103 #45 and #44. #45 is the clock input, and #44 is the amplification circuit output in the MPU. The operation frequency of the crystal oscillator is 24MHz. The basic clock is divided in the MPU to operate the program and circuits of the MPU.

1.6 Software

1.6.1 Outline

(1) Input frequency
- •Horizontal : 30KHz to 121KHz (Lower limit : 29.5KHz, Upper limit: 123KHz)
- •Vertical : 50KHz to 160Hz (Lower limit: 45Hz Upper limit: 162Hz)

(2) Memory timing number
- •Preset timing : 9 timing (22 timing max.)
- •User timing : 15 timings can be memorized.

1.6.2 Frequency variation detection function

When the normal signal is input, the input frequency and polarity are checked every input of VSYNC. If they satisfy the conditions a, b and c, it is judged that the input signal varies. When input signal variation is detected, the directory data written in EEPROM and the directory data of the input signal are compared with each other in the following sequence, and the picture data are read and output.

(1) If the input signals satisfy conditions a, b and c, they are judged to be the same as the signals registered in the directory, and the timing data are read from EEPROM and are output.
Condition a: The polarities of the input sync. signal are the same in both horizontal and vertical directions.
Condition b: Horizontal frequency difference is 0.6KHz
Condition c: Vertical frequency difference is 0.6Hz.

The sequence of the compared directories is as follows:
PRESETO–>PRESET1–>•••–>PRESET21–>USER0–>USER1–>•••–>USER14
f the same timing is judged on the way, the comparison work is stopped there, and the adjustment value for each corresponding timing is read out from EEPROM.

(2) If the conditions of (1) are not satisfied (when the new timing is input), the horizontal frequency reads the backup picture data of the nearest preset timing and outputs it.

1.6.3 Memory of user timing

The new timing is input. When the picture adjustment is executed, the directory data (frequency and polarity) and picture data will be memorized in EEPROM.
If 15 user timings (MAX) are memorized, the memory of the oldest user timing (directory data and picture data) is deleted, and the new timing information is memorized there.
USER0–>USER1–>•••–>USER14–>USER0–>USER1–>•••

1.6.4 Picture adjustment

(1) The monitor has the function to do the picture adjustment with OSD and communication.
The function has the following adjustment modes.
a: Normal mode
b: Factory mode
For entry into each adjustment mode, refer to Item "Adjustment method".

(2) High voltage adjustment supplement
The high voltage of the normal time is determined with "HVAD" setting value of OSD adjustment item and the X-ray protect voltage is determined with "XPRO" setting value of the OSD adjustment item. To adjust the X ray protect voltage, it is necessary to raise the high voltage to 30KV once.
To temporarily raise the high voltage, "HVTP" of OSD adjustment item is used. Since "HVTP" is not memorized in EEPROM, the high voltage will return to the normal ("HVAD" setting value) when the power is turned OFF once. Even if the page of the high voltage adjustment of OSD is skipped with the Ø button, it will similarly return to the normal high voltage.

(3) If XRAY-PROTECT activates even in the normal state because XRAY-PROTECT is excessively lowered by mistake, the XRAY-PROTECT and HV-ADJUST adjustment values can be initialized using the following procedure.

(a) Input the image signal to the monitor.

(b) Keeping both + and - buttons pressed, turn ON the power.

(c) Keep both + and - buttons pressed 20 seconds or more. (Approx. 30 seconds)

(d) Release - button only.

(e) Keep the + button only pressed 10 seconds or more.

(f) When it is successfully completed, the monitor will drop to POWER SAVE approx. 10 seconds. (LED becomes amber.)

(g) Turn OFF the power, and turn it ON again, and the XTRAY-PROTECT adjustment value will become 254 and HV-ADJUST adjustment value will become 0.

(4) Vertical position adjustment supplement
The adjustment data that displays OSD adjustment item "VERT-POSITION" is different between the normal mode and factory mode. Therefore, even if "VERT-POSITION" is set at 127 (middle) in the factory mode, "VERT-POSITION" does not always show 50% when it is returned to the normal mode.
Operation of "VERT-POSITION" is not followed up in the factory mode though the trapezoidal distortion compensation is automatically followed up in the normal mode.

1.6.5 Power management

The function reduces the power consumption of the monitor when the connected computer is not used.
The function is turned ON and OFF from the adjustment picture.

The monitor has only one kind of the power management function.

(1) Conditions to enter power management mode
a: "POWER SAVE" of the picture adjustment item is left ON.
b: Neither HSYNC nor VSYNC are input.
* Not that if the image signal GREEN is input when neither HSYNC nor VSYNC is input, the power management can not be activated since it wrongly recognizes that Sync On Green is input.

(2) Power management operation

When the power management is activated,

(i) P_SUS signal is turned to LO to stop the power output on the secondary side except CRT heater, P-OFF+5V, +5V line.

(ii) P-OFF signal is turned to LO to stop the power output of P-OFF+5V line.

(iii) The front LED is lit amber.

1.6.6 Automatic switch function of input connector

The monitor has two input systems of SIGNAL A/B that can be switched.

The switch function works as follows.

(1) When power is supplied,

The input connector that was previously displayed is selected.

(2) Switching with SIGNAL A/B switch button.

When SIGNAL A/B switch button is pressed, the connector that is opposite the input connector now selected will be selected.

(3) When SYNC is not normally input.

(i) If any input SYNC is present,

The input connector is kept.

(a) If the input SYNC is OUT OF RANGE,

OSD of OUT OF RANGE is displayed.

(b) If not so,

The self diagnosis OSD is displayed or power management mode is entered.

(ii) If any input SYNC is not present at all,

It is switched to the other input connector at the interval of one second, and if any input SYNC is present, the input connector is continuously selected.

If no input SYNC is present in the other input connector either, switching will be contin ued at intervals of 1 second with the self-diagnosis OSD displayed or power manage ment mode entered.

1.6.7 Circuit protective operation

If any circuit operation abnormality is detected, the monitor will forcibly enter power management mode to protect the circuit. (At this time, the picture is not displayed but LED is lit amber even if the sync. signal.)

(1) Power short-circuit detection on the secondary side

If PRO signal becomes H1 for one second or more, the power on the secondary side will be regarded as a short circuit to forcibly activate power management.

(2) EEPROM memory value error

The high-voltage adjustment HV-ADJUST and XRAY-PROJECT have respectively the backup data. When the power is supplied, the adjustment values are read from EEPROM. If this is not consistent with the backup data, it will be regarded as an EEPROM memory error to forcibly activate power management.

(3) I2C bus error

If the data line (SDA) of 12C bus (I2C1 and I2C2) that controls IC in the monitor is kept at LO 2 seconds or more, it will be regarded as I2C bus error to forcibly activate power management.

1.6.8 USB circuit

1.6.8.1 Outline

The H chassis USB hub has a 2-upstream/3-downstream self-powered hub (Gang Mode).
The MPU is connected to the hub's port 4 allowing the USB to be monitored and controlled.

(1) Serial data bus

The USB data bus is connected from the upstream connector (J1A0, J1A3) to the upstream port on the hub controller (IC1A0). The hub controller's downstream port is connected to the downstream connector (J1A1, J1A2) and the USB port on the MPU. The hub controller relays the data communication from the upstream side (PC) and downstream side (device).

Downstream connection of Hub controller IC1A0

Electrical port No.	Connection	Silk display
port 1	J1A1	3
port 2	J1A2 (Down)	2
port 3	J1A2 (Up)	1
port 4	MPU	

(2) 2-upstream

The H chassis has two upstream connectors (J1A0, J1A3). D+ of these data buses is connected to the analog SW (IC1A1), and D- is connected to the analog SW (IC1A4). The common terminal of each analog SW is connected to the upstream port of the hub controller.

If a USB cable is connected to J1A0 or J1A3, the data bus of that connector will be automatically connected to the hub controller.

If USB cables are connected to both J1A0 and J1A3, which cable to use can be selected with the OSD menu.

(3) Power supply to downstream

The H chassis USB hub is a batch controlled self-powered hub. The 5V 500mA (max.) power is supplied from the hub regulator IC1A6 to each downstream port.

The regulator IC1A6 has an overcurrent detection function, and if a current exceeding 500mA flows to one downstream port, the power to all downstream ports will stop automatically. (Batch control)

(4) USB monitor control

Port 4 of the hub controller (IC1A0) is connected to the USB port on the MPU. Monitoring and control using the USB can be carried out with this.

1.6.8.2 2-upstream

#1 (Vbus 5V power) of each upstream connector is connected to the MPU's input port. If this port input is HI, the MPU will determine that a USB cable is connected to that connector.
The MPU inputs the UPSEL signal (IC103 #48) to each analog SW (IC1A1, IC1A4), and either the upstream connector J1A0 or J1A3 data bus is connected to the upstream port of the hub controller (IC1A0).

UPSEL	Selected Upstream
LOW	ROOT A (J1A3)
HI	ROOT B (J1A0)

Following set conditions, the MPU carries out control are explained below.

(1) When neither the upstream A nor B is connected
When UPA (IC103 #47) and UPB (IC100 #46) are LOW, the UPSEL setting is maintained, and the OSD "USB UPSTREAM" display changes to "NO ROOT CONNECTION".

(2) When upstream A or B is connected
If UPA or UPB is HI, the MPU will control with the UPSEL signal so that the data bus of that upstream port is connected to the hub controller (IC1A0).
At this time, the OSD "USB UPSTREAM" display will show the connected upstream port in blue.

(3) When both upstream A and B are connected
When both UPA and UPB are HI, upstream A or B is connected with the OSD setting.
The OSD "USB UPSTREAM" display will show the selected upstream port in blue, and the non-selected upstream port in black.
(a)When upstream is connected with +/- button at OSD "USB UPSTREAM"
The OSD-designated (blue display) upstream is selected.
The selected state is saved in the EEPROM (IC105), and that root selection will be maintained regardless of the BNC/DSUB connector selection. The combination display at the OSD "USB PORT COMBINATION" will all appear in black.
(b)When combination with input connector is selected with +/- button at OSD "USB PORT COMBINATION"
The combination designated with the +/- button will appear in blue.
Following the OSD-designated (blue display) combination, the upstream corresponding to the DSUB connector displayed on the screen will be selected.

1.6.8.3 Power supply to USB downstream

The power supply and overcurrent detection for the H chassis downstream is carried out as a batch for the 3-downstream ports.

(1) Vbus power supply
When the hub controller (IC1A0) is recognized from the upstream side, the downstream current output enable signal will be output from the IC1A0 #33. When #1, #5 and #9 are set to HI, the power regulator =
(IC1A6) will start to supply 5V power to each downstream port (J1A2 #1 and #5, J1A1 #1).

(2) Overcurrent detection
The regulator (IC1A6) has an overcurrent detection function. When the current output at each port reaches 550mA (min) or more, the current output from that port will be automatically stopped, and the corresponding overcurrent detection flag terminal (IC1A1 #2, #6 or #10) will be grounded.
(The overcurrent detection resistor is built into the regulator.)
The overcurrent detection flag terminal is an open collector output pulled up to +5V by R1C1. LOW is input to the overcurrent detection input terminal (IC1A0 #26) of the hub controller.
When the hub controller (IC1A0) detects this signal, IC1A1 #1, #5 and #9 are set to LOW to prohibit the current output. This stops the output of current to all downstream ports.
The regulator (IC1A6) has the function to stop the overcurrent detection for a set time after starting the current output to avoid malfunctioning of the overcurrent detection caused by a rush current.
This time is controlled by the external capacitor (CIC6, CIC7 and CIC8).

(3) Hub controller power

#17 of the regulator (IC1A6) is the 3.3V output, and #14 is the 3.3V output control. The control terminal is pulled up by the USB_6.5V, and when the monitor power is turned ON, 3.3V is output from the #17. The hub controller is driven by this 3.3V power.

1.6.8.4 USB monitor control

Port 4 of the hub controller is connected to a MPU, allowing the USB to be monitored and controlled.

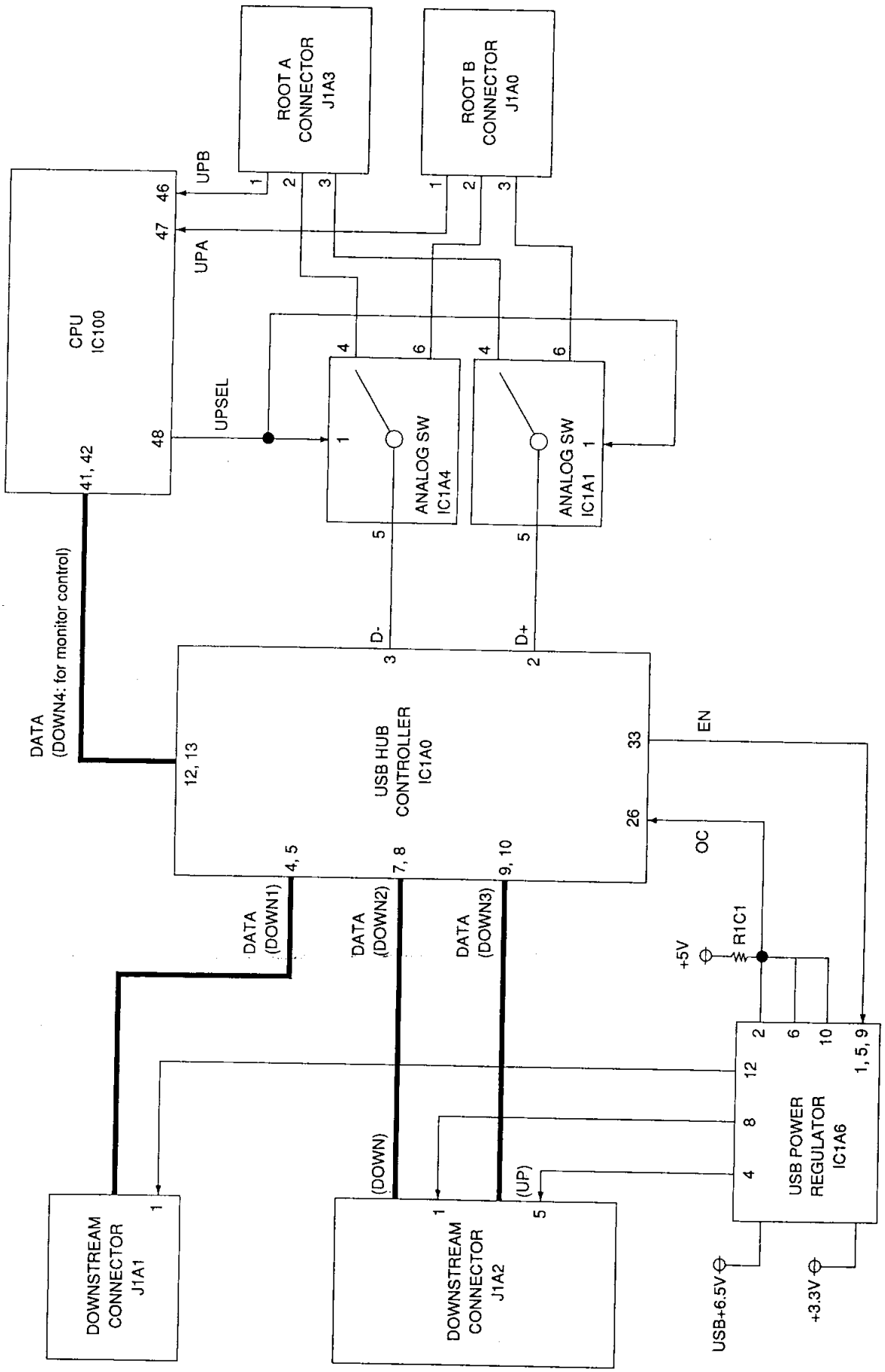
A low-speed (1.5Mbps) USB serial interface engine is built into the MPU. #43 of the MPU is 3.3V output for the USB, and by pulling up D- (IC103 #41) with this 3.3V, the hub controller recognizes that the MPU is a low-speed device.

When the USB cable is connected from the PC to the upstream port, the various descriptors will be sent to the PC.

The configuration descriptor and report descriptor are burned on the MPU's ROM. The device descriptor and string descriptor are saved in the EEPROM (IC105).

The monitor's USB interface is recognized as an HID (Human Interface Device). The required drivers can be installed from the Windows98 CD-ROM. (Refer to IB.)

A dedicated application is required for the USB monitor control.



USB circuit block diagram

1.7 Deflection processor block

1.7.1 Outline

The deflection processor block mainly composed of deflection processor IC generates and controls a variety of the following compensation waveform that are produced by this IC.
The deflection processor IC is a Pin 64 IC of uPD61882 of IC700.
The following eight points are generated and controlled by the deflection processor IC.
(Refer to the block diagram of IC700 in the figure.)

(1)Vertical deflection waveform generating circuit
(2)Horizontal deflection drive waveform generating circuit
(3)Distortion compensation waveform generating circuit
(4)DBF compensation waveform generating circuit
(5)Convergence compensation waveform generating circuit
(6)Blanking waveform generating circuit
(7)Moire canceling circuit
(8)V-PARABOLA waveform generating circuit (VCANCEL)

Moreover, the block is provided with a small both-face board (PWB-DEFL-SUB) of 60mm X 70mm.
The power of the deflection processor block is +3.3V that is converted from P-OFF+5V by the regulator of IC702, and the power and GND are divided into the digital system and analog system in the inner circuit of IC700 in order to prevent noise interference for the waveforms.
OP amplifier of IC701 uses the power of +5V and -15V, and works as the trace filter and voltage amplification of the amplitude of the saw-toothed waveform for vertical deflection.

1.7.2 Vertical deflection waveform generating circuit

The deflection processor IC (IC700) does 10-bit DAC output of the saw-toothed wave for vertical deflection that is synchronized with the vertical frequency input to Pin 42, from Pins 1 and 11 at both polarities (approx. 1.2V.p-p). Moreover, the center voltage IMID (approx. 1.6VDC) of the saw-toothed wave is output from Pin 2.
To remove the noise, the OP amplifier (Pins 1, 2 and 3) of the front step of IC701 removes the difference between the waveforms of both polarities of the saw-toothed wave for vertical deflection, using the center voltage IMID of the saw-toothed wave as the reference. From the output of the amplifier, the digital gradation component of the saw-toothed wave is removed with the low pass filter that is made of R713 and C738. Moreover, Pins 62 and 63 of IC700 are the analog switch turning ON the retrace term, prevents the waveform deformation that is produced by the low pass filter, and prevents the degradation of the linearity and the fluctuation of the scanning line.
Moreover, the saw-toothed wave for vertical deflection is controlled to adjust the vertical picture width, vertical phase and linearity.
R715, R758, R760 and R762 connected to pair GND on the filter output composed of R712 and C738 are the resistor to improve the linearity of the saw-toothed wave for input vertical deflection, and switches the resistance into four steps with the transistor switch of Q703 and Q704 according to the vertical frequency. (Refer to the switch table in the next page.)
The saw-toothed wave for vertical deflection is output to the low output impedance with the OP amplifier (Pins 5, 6 and 7) of the rear step of IC701.

Vertical frequency	Q703	Q704
50~72.9Hz	OFF	OFF
73~89.9Hz	ON	OFF
90~124.9Hz	OFF	ON
125~160Hz	ON	ON

Vertical linearity compensation resistance select transistor ON/OFF

1.7.3 Horizontal deflection drive waveform generating circuit

The rectangular wave for horizontal deflection drive are output at the amplitude 3.3Vp-p and approx. 45% Duty from Pin 25 of IC700 with the delay of the transistor taken into account in order to make the Duty become 50% at the output of Q501 of the horizontal deflection circuit. Here, the simulative horizontal sync. signal (5V pulse) from the horizontal flyback pulse (AFC, 5V pulse) input to Pin 27 of IC700 and IC103 (MPU) input to Pin 44 of IC700 is passed through the invertor of IC7A1 to produce the edges of these waveforms. This prevents the noises of the jitter , etc. from generating.

Moreover, the circuit composed of Q700, Q702 , etc. connected to Pin 13 of IC700 prevents the rapid frequency variation of the horizontal output when the horizontal input signal becomes no signal. Pin 13 of IC700 is a phase comparator filter terminal to phase-lock the horizontal input sync. signal and the oscillation in IC700. When the horizontal input sync. signal becomes no signal, the terminal voltage rapidly varies from approx. 0.8V of the phase lock time to 0V, and the frequency of the horizontal output rapidly varies according to this. The circuit is added to compress the rapid frequency variation width by smoothening the variation of the terminal voltage of Pin 13 by C719 when it becomes unlocked. This prevents the horizontal collector pulse from jumping in order to prevent overvoltage against the horizontal output transistor (Q502).

The terminals Pin 13 to Pin 20 of IC700 become the control filter terminal of horizontal PLL.

1.7.4 Distortion compensation waveform generating circuit

The deflection distortion compensating waveform is output from Pin 64 of IC700. The waveform is output from 1-bit DAC, and 3.3V pulse waveform of resolution power of 25MHz is output at Pin 64 direct. The pulse waveform is smoothened with the low pass filter of R709 and C705 to gain the compensation waveform of the vertical frequency. The amplitude is approximately 1.0 to 1.2Vp-p, and is connected to Pin 5 of IC5J2.

The horizontal size, trapezoid compensation, side pin compensation, upper/lower compensation of the side pin, S type compensation of the side pin and W compensation of the side pin are applied. (Refer to the compensation image figure.)

The deflection compensation waveform in the horizontal phase system is output from Pin 57 of IC700. Pin 57 is the 1-bit DAC output, and outputs the pulse waveform of 3.3V of resolution power of 25MHz. The pulse waveform is smoothened with the low pass filter of R704, R753, C700 and C737, and the waveform of the vertical frequency is current-added to the filter (Pin 20 of IC700) of the horizontal system PLL to compensate for the deflection distortion of the horizontal phase system. The parallel rectangular distortion compensation and the side pin balance (upper and lower) compensation are executed. (Refer to the compensation image.)

1.7.5 DBF compensation waveform generating circuit

The horizontal system DBF compensation waveform is output in 8-bit DAC mode from Pin 10 of IC700. The amplitude is approximately 0.5Vp-p. It is connected to Pin 5 of IC7A0.

The vertical system DBF compensation waveform is output from Pin 58 in the 1-bit DAC mode. Pin 58 direct outputs the pulse waveform of the resolution power of 25MHz. The pulse waveform is smoothened with the low pass filter of R705 and C701 to gain the DBF compensation waveform of the vertical frequency. The amplitude is approximately 0.6Vp-p. It is connected to Pin 3 of IC7A0.

1.7.6 Convergence compensation waveform generation circuit

The horizontal dynamic convergence compensation waveform is output from Pin 6 of IC700 in the 8-bit DAC mode. The amplitude is approximately 0V to 0.5V. The vertical dynamic convergence compensation waveform is output from Pin 8 in the 10-bit DAC mode. The amplitude is approximately 0V to 0.5V. The dynamic convergence compensation waveform center voltage (approx. 1.6V) is output from Pin 7.

In the 1-bit DAC mode, the horizontal static convergence compensation waveform is output from Pin 61, and the vertical static convergence compensation waveform is output from Pin 60. In Pins 60 and 61 direct, the pulse waveform of the resolution power of 25MHz is output. The pulse waveform is smoothened through the low pass filter to gain the horizontal static convergence compensation waveform and vertical static convergence compensation waveform of the vertical frequency.

1.7.7 Blanking waveform generation circuit

The horizontal blanking pulse and vertical blanking pulse are generated in IC700, and these two waveforms are mixed and output at 3.3Vp-p from Pin 40 of IC700.

The reference of the phase of the vertical blanking pulse is determined at the leading edge of VFLY (vertical flyback pulse, 5V pulse) of Pin 39 input of IC700, and the phase can be variably controlled to output the optimal waveform of the blanking pulse.

The horizontal blanking pulse is a pulse that is synchronized with H-IN (horizontal sync. signal, 5V pulse) of Pin 44 input of IC700, and can be also variably controlled.

The waveform is connected to Pin 22 of the preamplifier (IC301) of the video board.

1.7.8 Moire canceling circuit

The moire canceling circuit outputs the waveform that is reversed every line of the horizontal frequency and every 1 frame of the vertical frequency. The vertical frequency waveform is output from Pin 23, and these two waveforms are added to the horizontal PLL through the filter of R736 and C723 to achieve the moire canceling function.

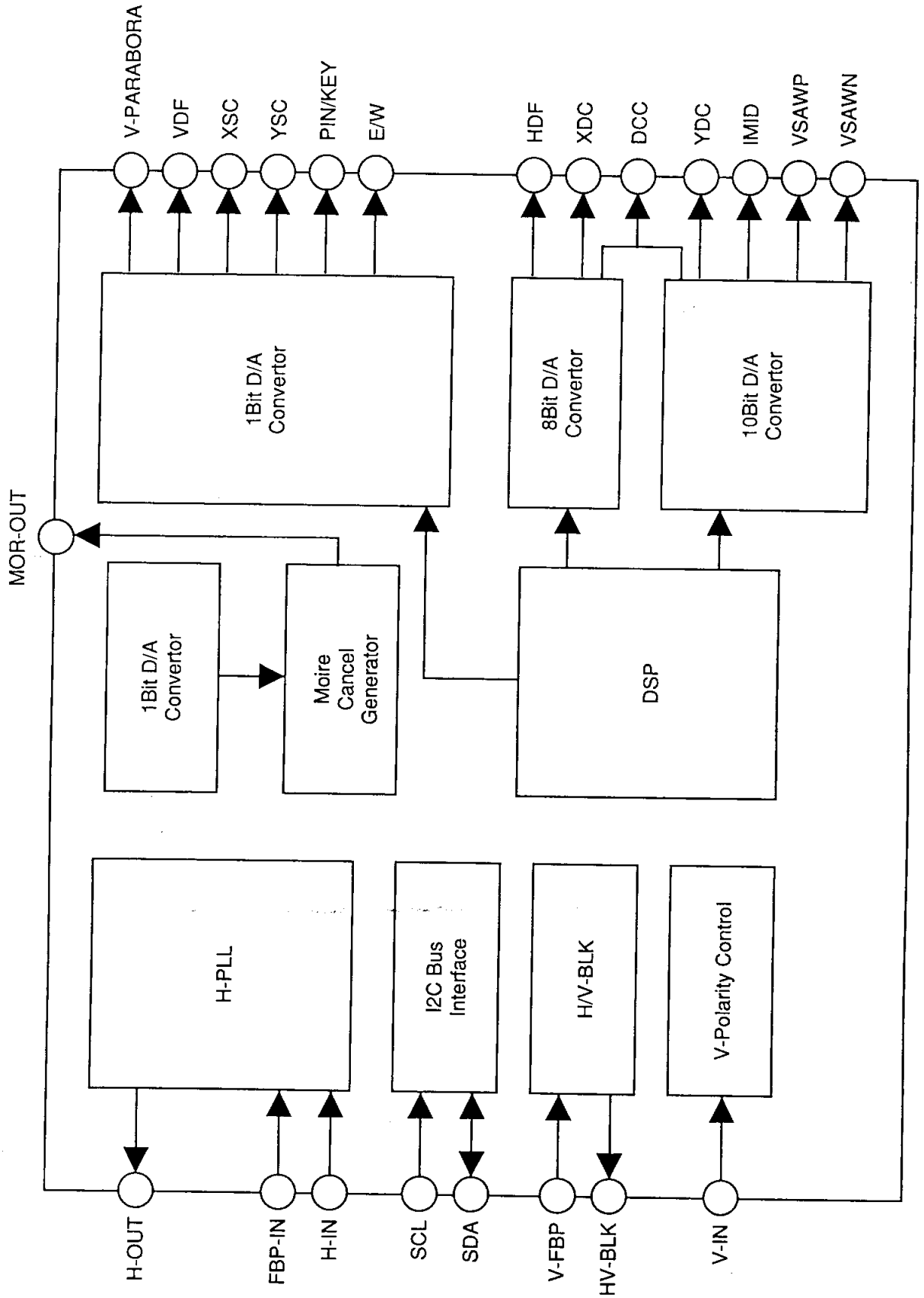
1.7.9 V-PARABORA waveform generation circuit (VCANCEL)

V-PARABOLA waveform is output in the 1-bit DAC mode from Pin 59 of IC700. The pulse waveform of 3.3V of the resolution power of 25MHz is output at Pin 59 direct. The pulse waveform is smoothened with a low pass filter to gain V-PARABOLA waveform of the vertical frequency.

Pin 30 of IC700 is a terminal to detect the drop of the power voltage (+3.3V), and the detection voltage is approximately 1.0V. When a power voltage drop is detected, Pin 32 of IC700 varies from Hi level (5V) to Lo level (0V) but is not used now.

Pin 46 is a terminal to detect whether the horizontal PLL is locked and HD output from Pin 25 is normal or not. It is output at the Hi level (5V) when it is locked, and at the Lo level (0V) when it is unlocked. It is connected to IC103 (MPU).

Pin 49 is the reset terminal of IC700. The reset IC of IC703 resets IC700 when P-OFF+5V drops to approx. 2.7V.

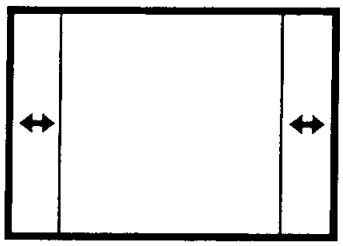


IC700 block diagram (uPD61882)

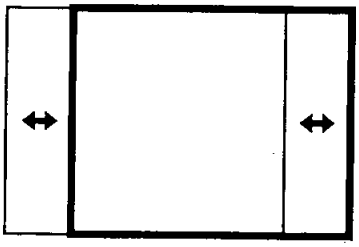
1.7.10 Distortion compensating operation

The followings are the operation image figures on the picture of the distortion compensstion.

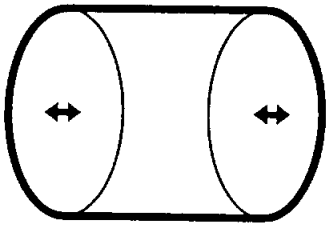
HORIZE-SIZE



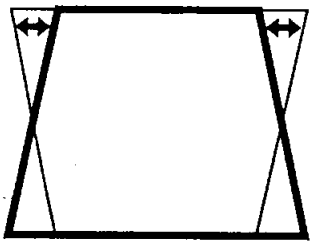
HORIZE-PHASE



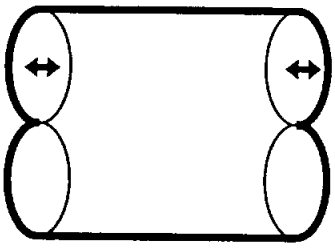
PINCUSHION



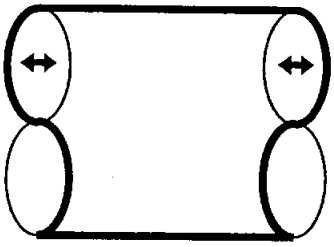
KEYSTONE



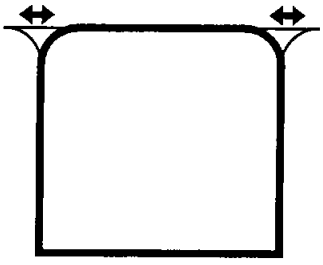
PIN-CENTER



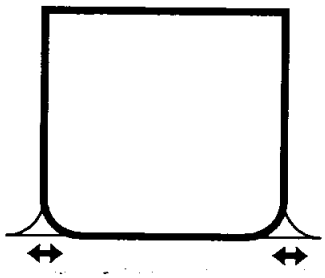
PCC-SINE



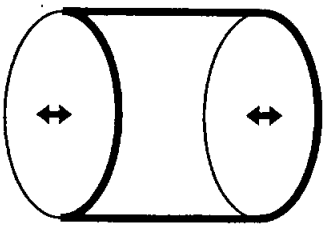
TOP-PIN



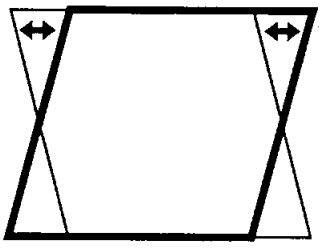
BOTTOM-PIN



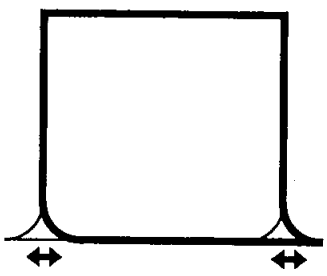
PIN-BALANCE



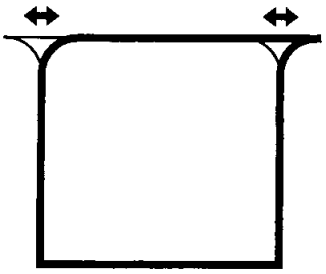
KEYBALANCE



BOTTOM-PIN



TOP-PIN



1.8 Video Block

1.8.1 Image signal amplifying circuit

The video circuit is composed of the same circuit structure for each of R, G and B. This item explains the G (green) video circuit.

The video input terminal is provided with 2 systems of SIGNAL-A and B, and are both the D-SUB connectors.

SIGNAL-A is input from Pin 2 of D-SUB connector (J201) to Pin 4 of the analog switch (IC200). Similarly, SIGNAL-B is input from Pin 2 of D-SUB connector (J200) to Pin 12 of the analog switch (IC200). (See Point A.)

The analog switch (IC200) is used for signal selection when SIGNAL-A and B are input at the same time.

As the signal selection method, the input signal SIGNAL-A is selected when Pin 13 (SELECT SW) of the analog switch (IC200) is LOW, and the input signal SIGNAL-B is selected when it is HIGH (See Point B.), and it is output from Pin 28 of the analog switch (IC200).

The video signal that is output from Pin 28 of the analog switch (IC200) is input to Pin 6 of Pre-AMP (IC301) on the video board through the flat cable. (See Point C.)

Pre-AMP (IC301) is a pre-amplifier that amplifies the voltage of the video signal (GAIN: 4 to 5 magnifications). Moreover, Pre-AMP (IC301) composes the adjustment picture (OSD) video signal output from IC300 and the blanking signals output from IC700. Moreover, the MPU (IC103) detects the current that flows through the flyback transformer on the main board, and the amplitude control (ABL) of the output voltage of the Pre-AMP (IC301) is applied to prevent the picture brightness from exceeding the constant value. The video signal processed through the voltage amplitude, composition and amplification control is output from Pin 31 of Pre-AMP (IC301), and is input to Pin 8 of MAIN-AMP (IC302) (See Point D.).

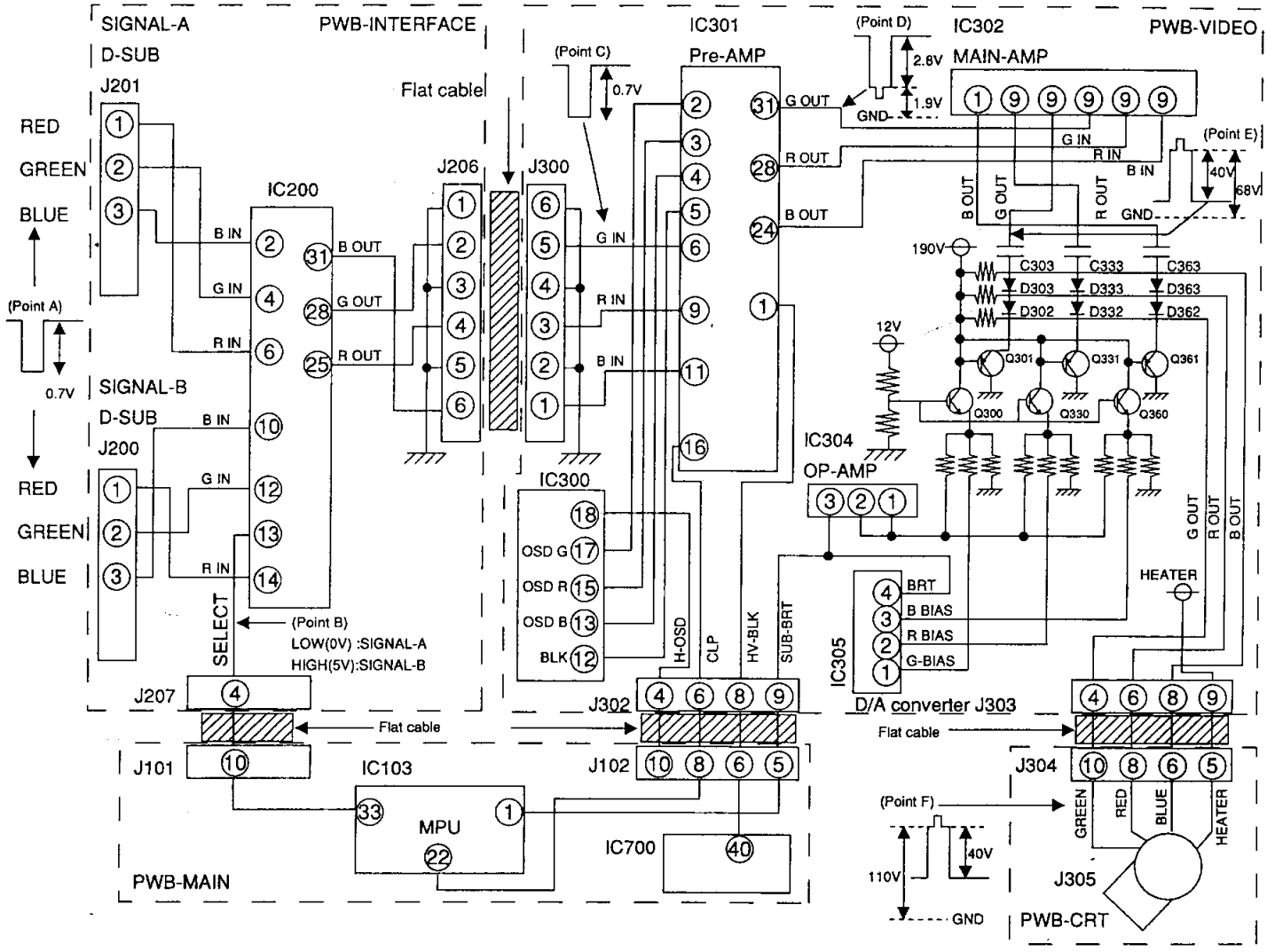
MAIN-AMP (IC302) is the main amplifier that amplifies the voltage of the video signal (GAIN: 13 to 15 magnifications). The video signal processed through the voltage amplification is output from Pin 5 of MAIN-AMP (IC302) (See Point E.). After it is AC-coupled by C303, it is DC-reproduced by the cutoff (diode clamp) circuit that is composed of D302, D303, Q300 and Q301.

The cutoff (DC bias control) voltage varies the back raster brightness (brightness) and chromaticity (bias) with the brightness control signal and bias control signal.

The brightness control signal is superimposed with SUB-BRT signal (for factory adjustment) output from Pin 1 of the MPU (IC103) and BRT signal (for user adjustment) output from Pin 4 of the D/A converter (IC305) by OP-AMP (IC304), and is output from Pin 1 of OP-AMP (IC304). The back raster brightness (brightness) is varied by applying the superimposed brightness control signal to the emitter of the base ground transistor (Q300).

The bias control signal is output from Pin 1 of the D/A converter (IC305). The bias control signal is also applied to the emitter of the base ground transistor (Q300) like the brightness control signal in order to vary the back raster chromaticity (bias).

The video signal that is AC-coupled with the above cutoff voltage is input to the CRT socket (J305) on the CRT board through the flat cable, and is supplied to the cathode of CRT. (See Point F.)



Video signal amplification circuit diagram

1.8.2 Input switch circuit

The sync. signal input terminal has two systems of SIGNAL-A and B like the video input terminal, and are both the D-SUB connectors. Since the input terminal and circuit operation are different every sync. signal (separate, composite, image composite), this item explains their sync. signals.

1.8.2.1 Separate sync. signal (Separate Sync)

The horizontal sync. signal input from SIGNAL-A is input from Pin 13 of D-SUB connector (J201) to Pin 7 of the analog switch (IC200), and the vertical sync. signal is input from Pin 14 of D-SUB connector (J201) to Pin 8 of the analog switch (IC200). Moreover, the horizontal sync. signal input from SIGNAL-B is input from Pin 13 of D-SUB connector (J201) to Pin 15 of the analog switch (IC200), and the vertical sync. signal is input from Pin 14 of D-SUB connector (J201) to Pin 16 of the analog switch (IC200). (See Point A.)

Like the video signal, the analog switch (IC200) selects the signal (2 input switch) when SIGNAL-A and B are input at the
same time.

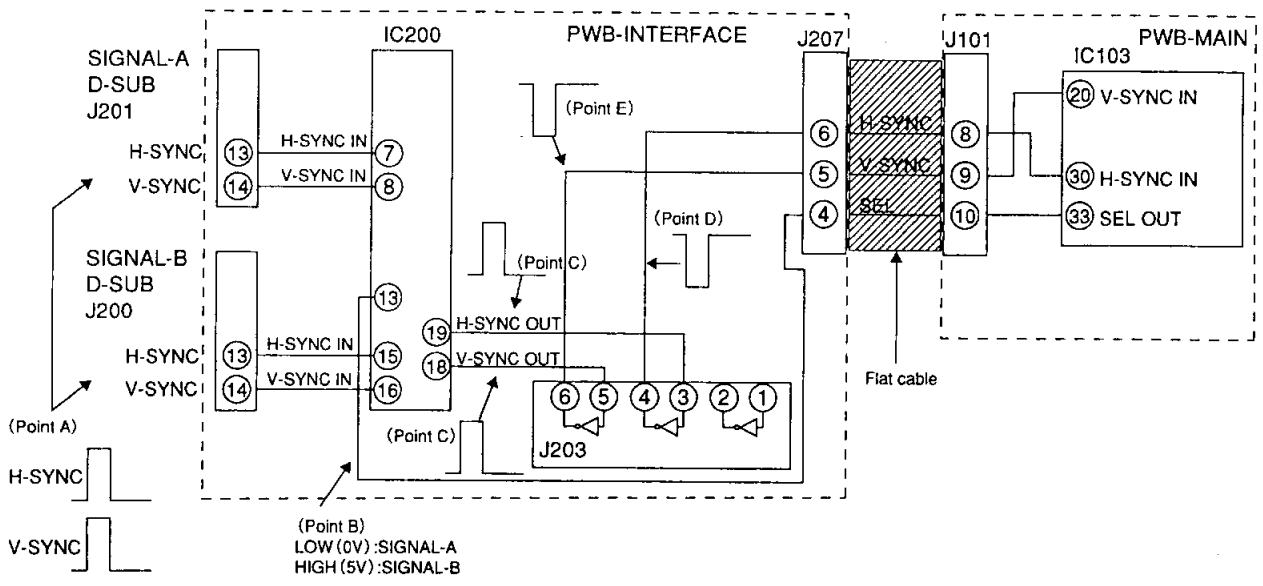
Like the video signal, the signal selection method is that the input signal of SIGNAL-A is selected when Pin 13 (SELECT SW) of the analog switch (IC200) is set at LOW by SELECT signal of Pin 33 of the MPU (IC103), and the input signal of SIGNAL-B is selected when it is HIGH (See Point B.), and the signal is output from Pin 19 (horizontal sync. signal) and Pin 18 (vertical sync. signal) of the analog switch (IC200). (See Point C.)

The horizontal sync. signal output from Pin 19 of the analog switch (IC200) is input to Pin 3 of the invertor (IC203), and is output from Pin 4 of the invertor (IC203) after the polarity of the horizontal sync. signal is reversed. (See Point D.) The vertical sync. signal output from Pin 18 of the analog switch (IC200) is input to Pin 5 of the invertor (IC203), and is output from Pin 6 of the invertor (IC203) after the polarity is reversed like the horizontal sync. signal. (See Point E.)

The reason the polarity is reversed by the invertor (IC203) is to remove the jitter (sizzling noise) on the picture displayed on the monitor.

The horizontal sync. signal and vertical sync. signal output from the invertor (IC203) are supplied through the flat cable to Pin 30 (horizontal) and Pin 20 (vertical) of the MPU (IC103) on the main board.

Though the positive polarity (POS) and negative polarity (NEG) are provided as the polarities of the separate sync. signal, the following figure shows that the positive polarity (POS) is input.



1.8.2.2 Composite sync. signal (Composite Sync)

The composite sync. signal input from SIGNAL-A is input from Pin 13 of D-SUB connector (J201) to Pin 7 of the analog switch (IC200). Moreover, the composite sync. signal input from SIGNAL-B is input from Pin 13 of D-SUB connector (J201) to Pin 15 of the analog switch (IC200). (See Point A.)

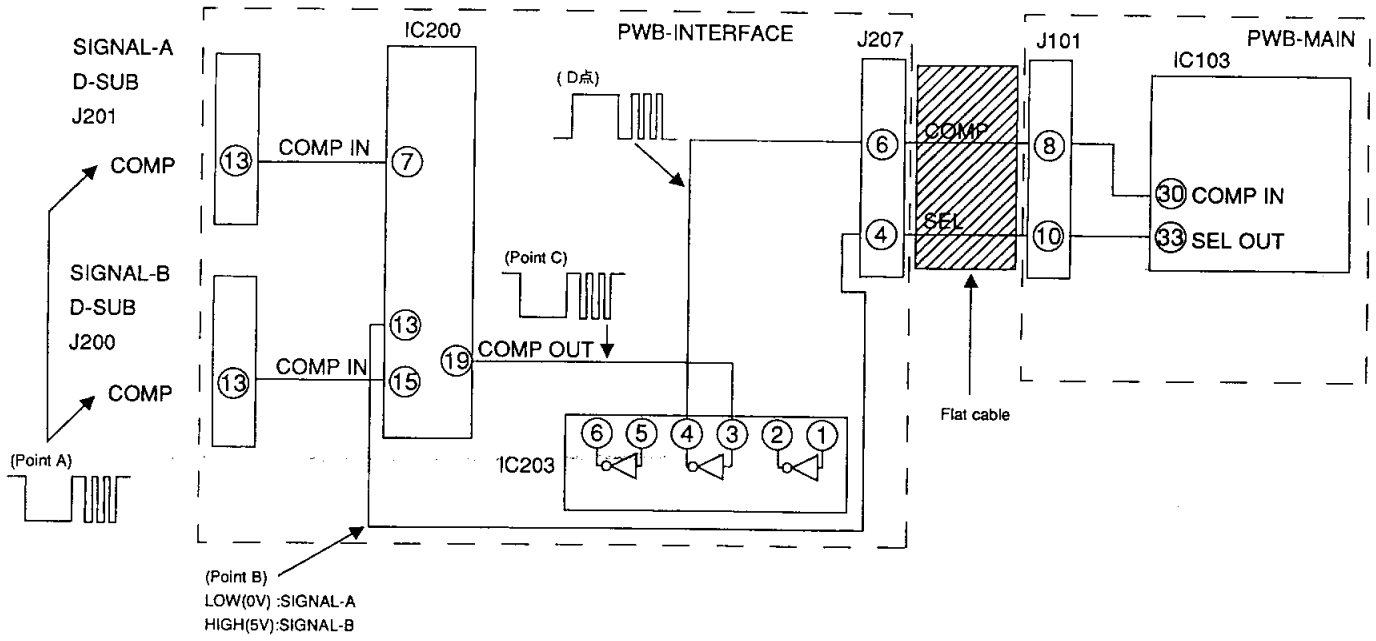
Like the separate sync. signal, the analog switch (IC200) selects the signal (2 input switch) when SIGNAL-A and B are input at the same time.

Like the separate sync. signal, the signal selection method is that the input signal of SIGNAL-A is selected when Pin 13 (SELECT SW) of the analog switch (IC200) is set at LOW by the SELECT signal of Pin 33 of the MPU (IC103), and the input signal of SIGNAL-B is selected when it is HIGH (See Point B.), and the signal is output from Pin 19 of the analog switch (IC200). (See Point C.)

The composite sync. signal output from Pin 19 of the analog switch (IC200) is input to Pin 3 of the invertor (IC203), and is output from Pin 4 of the invertor (IC203) after the polarity of the composite sync. signal is reversed. (See Point D.)

The reason the polarity is reversed by the invertor (IC203) is to remove the jitter (sizzling noise) on the picture displayed on the monitor like the separate sync. signal.

The composite sync. signal output from the invertor (IC203) is supplied through the flat cable to Pin 30 of the MPU (IC103) on the main board, and is processed through synchronous separation by the MPU (IC103).



1.8.2.3 Video composite sync. signal (Sync on Green)

The image (green video) composite sync. signal input from SIGNAL-A is input from Pin 2 of D-SUB connector (J201) to Pin 4 of the analog switch (IC200). Moreover, the image (green video) composite sync. signal input from SIGNAL-B is input from Pin 2 of D-SUB connector (J201) to Pin 12 of the analog switch (IC200). (See Point A.)

Like the separate sync. signal and composite sync. signal, the analog switch (IC200) selects the signal (2 input switch) when SIGNAL-A and B are input at the same time.

Like the separate sync. signal and composite sync. signal, the signal selection method is that the input signal of SIGNAL-A is selected when Pin 13 (SELECT SW) of the analog switch

(IC200) is set at LOW by the SELECT signal of Pin 33 of the MPU (IC103), and the input signal of SIGNAL-B is selected when it is HIGH (See Point B.), and the video signal is output from Pin 28 of the analog switch (IC200) (See Point C.) and the composite sync. signal is output from Pin 21 of the analog switch (IC200). (See Point D.)

The image composite sync. signal must be separated into the video signal and composite sync. signal.

As the separation method of the image signal and composite sync. signal, the S/G-SEL signal of the MPU (IC103) becomes HIGH (5V) when the MPU (IC103) detects the image (green video) composite sync. signal. Then, the transistor (Q200) is turned OFF to output the image (green video) composite sync. signal from Pin 23 of the analog switch (IC200). The image (green video) composite sync. signal output from Pin 23 of the analog switch (IC200) is input to Pin 22 of the analog switch (IC200), and after it is separated into the image signal and composite sync. signal in the analog switch (IC200), the composite sync. signal only is output from Pin 21.

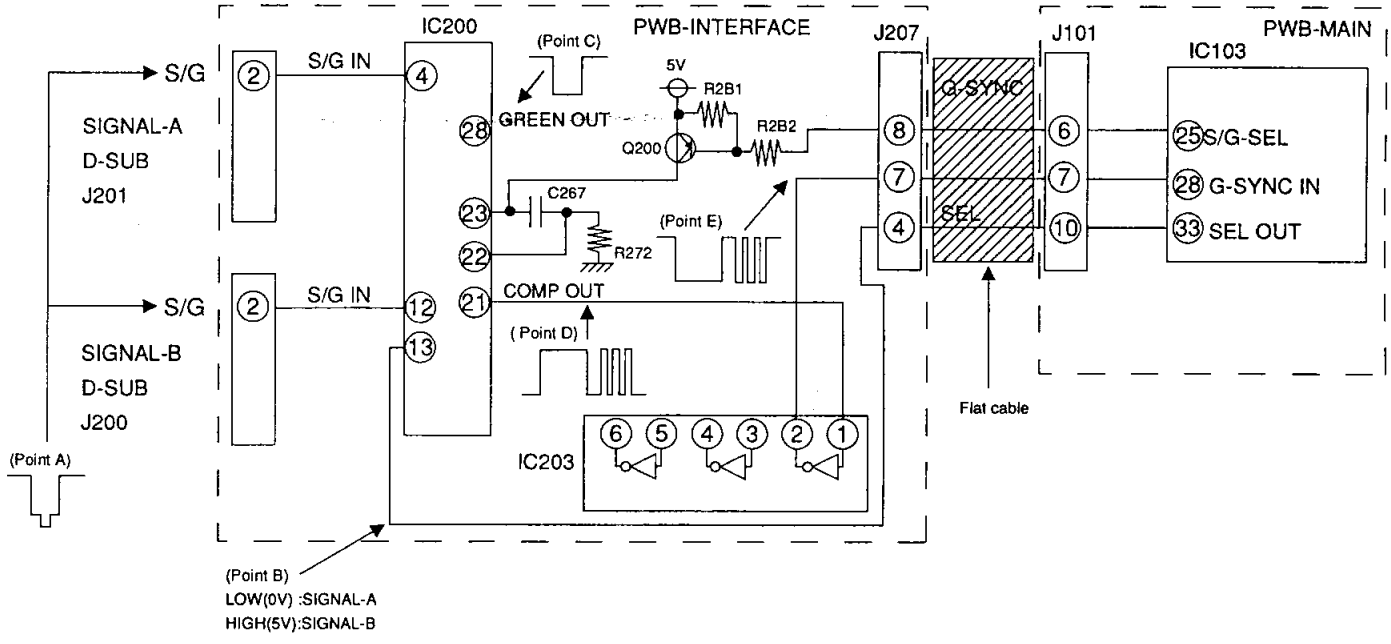
The composite sync. signal output from Pin 21 of the analog switch (IC200) is input to Pin 1 of the invertor (IC203), and is output from Pin 1 of the invertor (IC203) after the polarity of the composite sync. signal is reversed. (See Point D.)

The reason the polarity is reversed by the invertor (IC203) is to remove the jitter (sizzling noise) on the picture displayed on the monitor like the separate sync. signal and composite sync. signal.

The composite sync. signal output from the invertor (IC203) is supplied through the flat cable to Pin 28 of the MPU (IC103) on the main board, and is processed through synchronous separation by the MPU (IC103).

1.8.3 On Screen Display circuit

The control signal of the adjustment picture (OSD) is input to Pin 5 (CLK), Pin 6 (DATA), Pin 18 (H-BLK), and Pin 19 (V-BLK) of IC300. IC300 outputs Pin 12 (BLK), Pin 13 (OSD-B), Pin 15 (OSD-R), and Pin 17 (OSD-G), and they are synthesized with the video signal by IC301.



2. Adjustment procedure

2.1 Scope

These are the specified adjustment and inspection methods for the NSH1117STTKW.

2.2 Application

The applicable models are as follow.

Model	Rating label	Destination	Remarks
1	NSH1157STTUW	For own domestic use	

(Note) When degaussing this monitor with the hand demagnetizer, use the following procedure.

(1)Turn the monitor power OFF, and degauss with the hand demagnetizer.

(2)Degauss with the hand demagnetizer in the power management state.

(3)Degauss with the hand demagnetizer during automatic demagnetization of monitor unit.

2.3 Measuring instruments

(1) Signal generator A: Astro Design VG-812 or equivalent

(2) Signal generator B: Astro Design VG-829 or equivalent

(3) DC voltmeter: 150V 0.5 Class or digital voltmeter

(4) High voltage meter: 0.5 Class that can measure 30KV

(5) Luminance meter: Minolta color analyzer CA-100 or equivalent

(6) AC voltmeter: 150V/300V 0.5 Class

(7) Oscilloscope: Scope with band of 100MHz or more

(8) Landing measuring device: Felmo product

(9) Double scale: For width and distortion measurement

(10) Withstand voltage meter: Kikusui Model TOS8650 or equivalent

(11) Grounding conductivity measuring instrument: CLARE U.K. product

2.4 Standard setting state

Unless particularly designated, adjust with the state given in this section.

2.4.1 Power voltage

Model	Assembly	Aging	Adjustment	Remarks
All models	AC100V 60Hz	AC264V 60Hz	AC220V 60Hz	

2.4.2 Adjustment magnetic field

Model	Adjustment magnetic field	Remarks
All models	HORIZ. 0mT VERT. 0.04mT	Northern hemisphere
	HORIZ. 0mT VERT. 0.mT	Equator
	HORIZ. 0mT VERT. -0.04mT	Southern hemisphere

2.4.3 Signal cable

Unless particularly designated, use a D-SUB 15-PIN signal cable.

*When executing DDC IIBi communication, use SIGNAL B side unless particularly designated.

2.5 Preparatory inspections

(1) The assembly must be correctly assembled.
(2) There must be no cracks or remarkable contamination on the PWB.
(3) There must be no remarkable lifting or inclination of the parts on the PWB, and the parts must not be touching.
(4) The connectors must be securely inserted without crimping faults.
(5) The CRT socket, anode cap and focus lead must be securely mounted.
(6) The lead wires must not be pressed against the edges of the board.
(7) The lead wires must not touch the high temperature parts such as the R-METAL, R-CEMENT or TR with FIN.
(8) The board must not be bent, remarkably contaminated or scratched.
(9) The CRT has no scratch or chipping.
(10) Each potentiometer must turn smoothly.
(11) Always set each potentiometer to the following positions before turning the power ON.

Potentiometer default settings

PWB name	IC sources	Name (symbol)	Default adjustment position	Remarks
PWB-MAIN	VR5A1	H-POSI	Center	
		FOCUS1	Center	FBT
		FOCUS2	Center	FBT
		SCREEN	Completely counterclockwise	FBT

2.6 Initializing the adjustment data in the EEPROM

(1) Turn the monitor power ON to confirm that the aging raster appears.
(2) Initialize the EEPROM with serial communication. Use the designated file shown below, and initialize the adjustment data in the EEPROM. Refer to section 3.7.3 OSD display (factory mode) for details on the default values.
(3) Turn the monitor power OFF.

Adjustment data initialization file name

Model	Rating label	Date of revision	Remarks
1	H_OWN5**.DAT		

The initial data regarding the horizontal linearity is as shown below.

Frequency	LIN	CS7	CS6	CS5	CS4	CS3	CS2	CS1
30.0 -- 34.0	0	1	1	1	1	1	1	1
34.0 -- 36.5	0	0	1	1	1	1	0	1
36.5 -- 39.0	0	0	0	0	1	1	0	1
39.0 -- 45.0	0	0	1	1	0	1	1	0
45.0 -- 47.5	0	0	1	1	1	0	1	0
47.5 -- 49.0	1	0	1	1	1	0	1	0
49.0 -- 52.0	1	1	1	1	1	1	0	0
52.0 -- 55.0	1	1	1	1	1	1	0	0
55.0 -- 59.0	1	1	1	0	1	1	0	0
59.0 -- 61.0	1	0	0	0	1	1	0	0
61.0 -- 63.0	1	0	0	0	1	1	0	0
63.0 -- 66.0	1	1	0	1	0	1	0	0
66.0 -- 70.0	1	1	0	1	1	0	0	0
70.0 -- 73.0	1	1	0	1	1	0	0	0
73.0 -- 76.0	1	0	0	1	1	0	0	0
76.0 -- 78.5	1	1	1	0	1	0	0	0
78.5 -- 81.5	1	1	0	0	1	0	0	0
81.5 -- 83.0	1	1	0	0	1	0	0	0
83.0 -- 86.5	1	0	1	1	0	0	0	0
86.5 -- 89.0	1	1	0	1	0	0	0	0
89.0 -- 92.0	1	1	0	1	0	0	0	0
92.0 -- 94.0	1	0	0	1	0	0	0	0
94.0 -- 97.0	1	1	1	0	0	0	0	0
97.0 -- 104.0	1	1	1	0	0	0	0	0
104.0 -- 108.0	1	1	0	0	0	0	0	0
108.0 -- 111.0	1	1	0	0	0	0	0	0
110.0 -- 113.5	1	1	0	0	0	0	0	0
113.5 -- 116.0	1	1	0	0	0	0	0	0
116.0 -- 121.0	1	0	0	0	0	0	0	0
AP-21 (68k/75)	1	1	1	1	1	0	0	0
VESA 80k/75	1	1	1	0	1	0	0	0

The above is I/O expander IC102 output

※1 When CS or LIN-COIL is ON, the corresponding bit is "1".
When OFF, the corresponding bit is "0".

2.7 Names of each monitor part

2.7.1 Configuration of front control panel

a: Power switch
b: Power lamp
c: Connector select button (OSD OFF)
d: Adjustment item select button
e: Adjustment button

* OSD OFF functions only when the OSD is displayed.

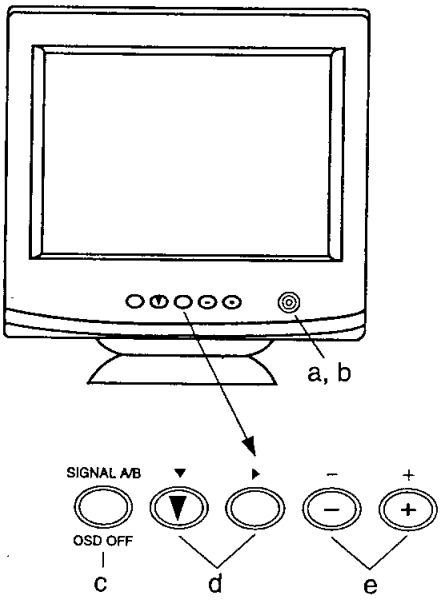


Fig. 1 Front control panel

2.7.2 Configuration of rear input connector

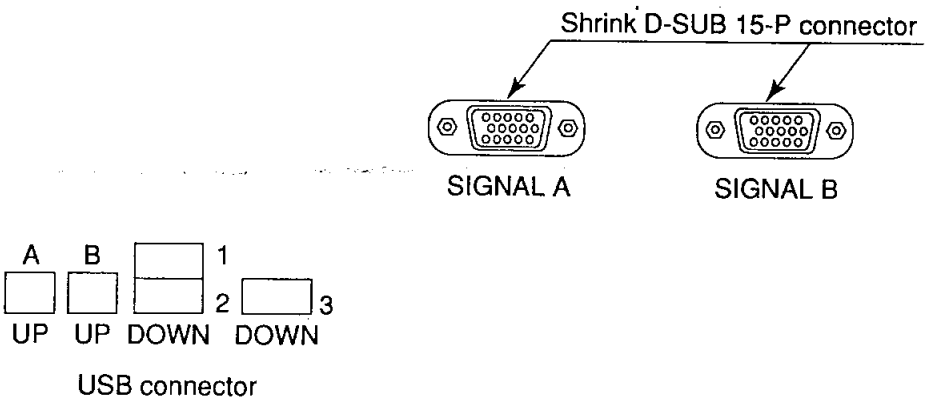


Fig. 2 Rear input connector

2.7.3 OSD display matrix

2.7.3.1 User mode

Adjustment items	Setting contents	Default setting	Setting classification	
			By timings	Common
OSD group 1				
CONTRAST	0~100%	100%		○
BRIGHT	0~100%	50%		○
COLOR NO.	COLOR No. 1,2,3	COLOR NO.1	○	
R-GAIN 1,2,3	0~100%			○
G-GAIN 1,2,3	0~100%			○
B-GAIN 1,2,3	0~100%			○
COLOR TEMPERATURE 1,2,3	5000K~9300K	COLOR 1:9300K, 2:6500K, 3:5000K		○
COLOR RESET 1,2,3	PROCEED			
OSD group 2				
H-SIZE	0~100%		○	
H-PHASE	0~100%		○	
V-SIZE	0~100%		○	
V-POSITION	0~100%	50%	○	
PIN-CUSHION	0~100%		○	
KEYSTONE	0~100%		○	
TOP-PIN	0~100%		○	
BOTTOM-PIN	0~100%		○	
PIN-BALANCE	0~100%		○	
KEY-BALANCE	0~100%		○	
VERT-LIN-BALANCE	0~100%		○	
VERT-LIN	0~100%		○	
ROTATION	0~100%	CENTER		
ZOOM	0~100%		○	
GEOMETRY-RESET	PROCEED			
				○
OSD group 3				
FINE PICTURE MODE	Normal/Text/Graphic	NORMAL	○	
H-CONVERGENCE	0~100%	CENTER		○
V-CONVERGENCE	0~100%	CENTER		○
CORNER PURITY(TL)	0~100%	CENTER		○
CORNER PURITY(TR)	0~100%	CENTER		○
CORNER PURITY(BL)	0~100%	CENTER		○
CORNER PURITY(BR)	0~100%	CENTER		○
MOIRE CANCEL ON/OFF	OFF / ON	OFF	○	
MOIRE CANCEL LEVEL	0~100%	0%	○	
CLAMP PULSE POSITION	FRONT / BACK	BACK	○	
VIDEO LEVEL	1.0V / 0.7V	0.7V	○	
OSD group 4				
DEGAUSS	PROCEED	ON		○
POWER-SAVE	OFF / ON	OFF		○
CONTROL LOCK	OFF / ON	(OSD position is the center of the picture)		○
OSD POSITION	<-- / -->			
ALL RESET	PROCEED			
GTF AUTO ADJUST	PROCEED			
DIAGNOSIS		ENG		○
LANGUAGE	ENG/ESP/ITA/GER/FRA/JAP			
OSD group 5				
USB UPSTREAM	PORT A / PORT B			○
USB PORT COMBINATION	PORT A : SIGNAL A PORT B : SIGNAL B			○

* CENTER=the factory setting value returning by pressing +, - buttons simultaneously.

2.7.3.2 Factory mode

(1)Factory mode 1 (The same section as the user mode)

Adjustment items	Setting contents	Default setting	Setting classification	
			By timings	Common
OSD group 1				
CONTRAST	0~254	254		○
BRIGHT	0~254	127		○
COLOR NO.	COLOR No. 1,2,3	COLOR NO.1	○	
R-GAIN 1,2,3	0~254			○
G-GAIN 1,2,3	0~254			○
B-GAIN 1,2,3	0~254			○
COLOR TEMPERATURE 1,2,3	0~86	COLOR1:86, 2:30, 3:0		○
COLOR RESET 1,2,3	PROCEED			
OSD group 2				
H-SIZE	0~(depend on +B adjustment)		○	
H-PHASE	0~254		○	
H-POSITION	0~254		○	
V-SIZE	0~254		○	
V-POSITION	0~254		○	
PINCUSHION	0~254		○	
KEYSTONE	0~254		○	
PIN-CENTER	0~254		○	
TOP-PIN	0~254		○	
BOTTOM-PIN	0~254		○	
S-CURVE	0~254	127	○	
PIN-BALANCE	0~254		○	
KEY-BALANCE	0~254		○	
TOP-BALANCE	0~254		○	
BOTTOM-BALANCE	0~254		○	
V-LIN	0~254		○	
ROTATION	0~254	127		○
ZOOM	0~(depend on +B adjustment)		○	
GEOMETRY-RESET	PROCEED			
OSD group 3				
FINE PICTURE MODE	Normal/Text/Graphic	Normal	○	
H-CONVERGENCE	0~254	127		○
V-CONVERGENCE	0~254	127		○
CORNER PURITY(TL)	0~254	127		○
CORNER PURITY(TR)	0~254	127		○
CORNER PURITY(BL)	0~254	127		○
CORNER PURITY(BR)	0~254	127		○
MOIRE CANCEL ON/OFF	OFF / ON	OFF	○	
MOIRE CANCEL LEVEL	0~127	0	○	
CLANP PULSE POSITION	FRONT / BACK	BACK	○	
VIDEO LEVEL	1.0V / 0.7V	0.7V	○	
OSD group 4				
DEGAUSS	PROCEED			
POWER-SAVE	OFF / ON	OFF		○
CONTROL LOCK	OFF / ON	OFF		○
OSD POSITION	<-- / -->	(OSD is the center of picture)		○
ALL RESET	PROCEED			
GTF AUTO ADJUST	PROCEED			
DIAGNOSIS				
LANGUAGE	ENG/ESP/ITA/GER/FRA/JAP	ENG		○
OSD group 5				
USB UPSTREAM	PORT A / PORT B			○
USB PORT COMBINATION	PORT A : SIGNAL A PORT B : SIGNAL B			○

(2)Factory mode 2 (The added section to the user mode)

Adjustment items	Setting contents	Default setting	Setting classification	
			By timing	Common
FACT 00				
PURITY-OFF1	0 (OFF)/1 (ON)	1 (ON)		○
PURITY-OFF2	0 (OFF)/1 (ON)	1 (ON)		○
H-PURITY	0~254	127		○
V-PURITY	0~254	127		○
DBF H AMP	0~254		○	
DBF H PHASE	0~100		○	
DBF V AMP	0~127		○	
R BIAS(COLOR1)	0~254	50		○
G BIAS(COLOR1)	0~254	50		○
B BIAS(COLOR1)	0~254	50		○
R BIAS(COLOR2)	0~254	50		○
G BIAS(COLOR2)	0~254	50		○
B BIAS(COLOR2)	0~254	50		○
R BIAS(COLOR3)	0~254	50		○
G BIAS(COLOR3)	0~254	50		○
B BIAS(COLOR3)	0~254	50		○
SUB-BRIGHT	0~254	220		○
ABL	0~254	254		○
B-LOW	0~187			
B-HI	0~187			
FACT 01				
YH-TT	0~254	127		○
YH-TB	0~254	127		○
YH-JT	0~254	127		○
YH-JB	0~254	127		○
4HTL	0~254	137		○
4HTR	0~254	127		○
4HBL	0~254	127		○
4HBR	0~254	127		○
YVTT	0~254	127		○
YVTB	0~254	127		○
YVJT	0~254	127		○
YVJB	0~254	127		○
4VTL	0~254	127		○
4VTR	0~254	127		○
4VBL	0~254	127		○
4VBR	0~254	127		○
PHASE	0~100	65		○
FACT 02				
HV-ADJUST	0~168			○
HV-ADJUST-TEMP	HV-ADJUST~254			
XRAY-PROTECT	0~254			○

2.8 Adjustment

2.8.1 How to select the factory adjustment (FACTORY) mode

2.8.1.1 Selecting with automatic adjustment device (Selecting with communication)

Using the communication command (DDC2Bi), issue the command from the automatic adjustment device to the monitor, and set the factory adjustment mode flag in the EEPROM to "01h" ("00h" for user mode).
(Refer to the A/B chassis automatic adjustment communication specifications (Protocol of DDC2Bi Enhanced) for details.)

2.8.1.2 Selecting with front panel switches

(1) Turn the power ON while holding down the CONNECTOR SELECT button.
(2) After step (1), release the button after one to two seconds.
(3) Confirm that 00 is displayed for the counter on the OSD display, and set to 225 with the (-) ADJUST button.
(4) Set to 05 with the (+) ADJUST button.
(5) When the adjustment item select button (RIGHT side) is pressed, the factory mode will be entered.
This factory adjustment mode is entered with the above steps.

*The factory adjustment mode remains valid even after the power is turned OFF.
Note that steps (3) to (4) must be carried out within ten seconds. If ten seconds are exceeded, the mode will return to the user mode.

<Returning to the user mode from the factory mode>

(1) OSD (for factory, user select) is displayed with the group selection.
(2) Set the counter value to 010 with the (-) (+) ADJUST buttons.
(3) When the adjustment item select button (RIGHT side) is pressed, the mode will return to the user mode.

2.8.2 Adjustments before aging

Status indicator	Adjustment item	Adjustment mode/set	Input signal/pattern
	Before aging		The only the sync. signal of No. 12 : 106.25K / 85Hz

2.8.2.1 Adjusting the high voltage and high voltage protector

Status indicator	Adjustment item	Adjustment mode/set	Input signal/pattern
	High voltage and high voltage protector		The only the sync. signal of No. 12 : 106.25K / 85Hz

(1) Turn the monitor power OFF, and connect a high voltage meter to the CRT anode. Then, turn the monitor power ON.
(2) Select the "GO TO FACTORY MODE" on the OSD and set to 250 with the ADJUST button (-) and then press the adjustment item select button (RIGHT side).
(3) Select HVAD (HV-ADJUST), and adjust high voltage to 27.0kV±0.5kV.
(4) Select HVTP (HV-TEMP), and adjust high voltage to 30.5kV±0.3kV.
(5) Select XPRO (XRAY-PROTECT), and turn the screen VR completely counterclockwise and set to the data the high voltage protector circuit operating with the ADJUST button (-).
(6) Set the power of the monitor OFF to ON. Turn the screen VR so that OSD is found and select the HV-ADJUST-TEMP on the OSD.
(7) Turn the screen VR completely counterclockwise and build up the high voltage with the

ADJUST button (+) to confirm that the high voltage protector circuit operates with30.5kV±0.3kV.
Note)You can also adjust while turning the screen VR completely counterclockwise.

<HVAD, HVTP and XPRO data>

(1) HVAD data
The data got by adjusting the high voltage are stored in IC106 so that the setting value does not change even if powering OFF or ON.

(2) HVTP data
Increase HVTP data and temporarily set the high voltage value to X ray protector operation voltage to set X ray protector operation point. When powering OFF/ON, the value same as HVAD is output.

(3) XPRO data
The data got when adjusting X ray protector operation point are stored in IC106 so that the setting value does not change even if powering OFF or ON.

<How to reset the high voltage adjustment data>
When adjusting the high voltage and X ray protector, it is possible to reset the items for the high voltge adjustment when executing the following setting operation.
When the XPRO setting value is more or less than the high voltage adjusted with HVAD, X ray protector operates as soon as powering ON. In this case, operate the following to reset the HVAD and XPRO data.

(1) Power ON the switch while pressing the ADJUST button (-) and (+).
Continue to press after powering ON.
(2) Approx. 30 seconds after, release only the (-) button.
Continue to press the (+) button 5 seconds moreover.
(3) Confirm that LED change over from GREEN to AMBER.
(4) Power OFF the switch.

OSD data after reset

HVAD	HVTP	PRO
0	0	254

2.8.2.2 SCREEN voltage adjustment

Status indicator	Adjustment item	Adjustment mode/set	Input signal/pattern
	SCREEN voltage		The only the sync. signal of No. 12 : 106.25K / 85Hz

(1) Connect a high voltage meter to the TP-SC terminal on the CRT PWB.
(2) Set to 700V±5V with the FBT picture potentiometer.

2.8.2.3

Adjust the focus pack "FOCUS 1, 2" so that both edges of the picture are clear.
that the high voltage protector operates.

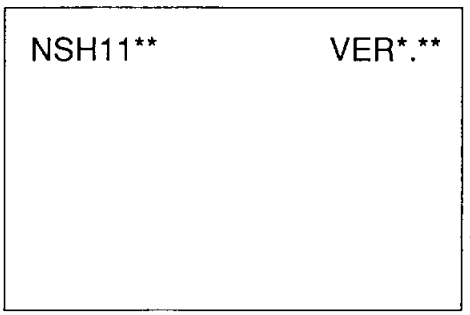
2.8.2.4 Shock test

Status indicator	Adjustment item	Adjustment mode/set	Input signal/pattern
	Shock test		The color bar pattern signal of No. 12 : 106.25K / 85Hz

(1) Display the "color bar" from the signal generator A.
(2) Confirm that there is no abnormality in the image when shock is applied on the monitor.

2.8.2.5 Preadjustment before aging

(1) Display a "full white" from the signal generator A.
(2) Confirm that the R, G and B channel images are output.
(3) Confirm that the H-CENT, picture position, picture size, PCC and balance can be controlled, and approximately adjust.
(4) Confirm that the OSD power management is turned OFF.
(5) Enter the factory mode (aging mode) beforehand.
(6) Disconnect the signal and confirm that the following display appears on the OSD. Then, adjust the picture to the specified luminance value before ITC adjustment using BRIGHT adjustment, and carry out heat run for 30 minutes or more.



2.8.2.6 Adjusting the landing (ITC/4 corner purity adjustment)

Status indicator	Adjustment item	Adjustment mode/set	Input signal/pattern
	landing		No. 12 : 106.25K / 85Hz
			Full green

(1) Display the timing No. 12 (1600 x 1200, 106.25K/85) and full green.
(2) Turn the monitor power OFF, and degauss with the hand demagnetizer.
(3) Select TL with the SELECT button.
(4) Using the ADJUST button and measuring instrument, adjust so that the landing value at the upper left corner is the "specified landing value".
At this time, confirm that the adjustment value is within the range of 86 to 170.
(Specify the working range limit for ITC here.)
The value indicated in the designs is to be used for the "specified landing value".
(5) Adjust the TF/BL/BR in the same manner.
(6) Display the timing No. 12 (1600 x 1200, 106.25K/85) and full white.

The luminance before ITC adjustment shall be the "specified luminance value before ITC adjustment."
The value indicated in the designs is to be used for the "specified luminance value before ITC adjustment".

2.8.3 Adjustments after aging

2.8.3.1 +B adjustment

Input the sync. signal of the following timings to adjust the picture width to 395±4mm.

Timing Nol	Timing	OSD adjustment item
A	30.0kHz	+B-L
12	106.25kHz	+B-H

2.8.4 Adjusting the picture size, position and distortion (using automatic adjustment device)

Status indicator	Adjustment item	Adjustment mode/set	Input signal/pattern
	Picture size, position, distortion	Factory	No. 12 : 106.25K / 85Hz
			Crosshatch with frame

The manual adjustment methods are explained below. The adjustments are executed in the factory adjustment (factory) mode.
Adjust the picture size to the value indicated in the list of adjustment values.
Adjust the distortion to the value indicated in the picture performance inspection item.

2.8.4.1 Adjusting the picture inclination

Status indicator	Adjustment item	Adjustment mode/set	Input signal/pattern
	Picture inclination	Factory	No. 12 : 106.25K / 85Hz
			Crosshatch with frame

Set the OSD to ROTATION, and using the (-) (+) ADJUST buttons, set the raster inclination to be horizontal to the CRT face surface.

2.8.4.2 Adjusting the back raster position

Status indicator	Adjustment item	Adjustment mode/set	Input signal/pattern
	Back raster position	Factory	No. 12 : 106.25K / 85Hz
			Only the sync. signal input

(1) Set BRT to 100% to show the back raster. (When using the automatic adjustment device, set RGB-BIAS to MAX also.)
(2) Input each adjustment timing, and set the OSD display to H-POSI. Using the (-) (+) ADJUST buttons, adjust the horizontal back raster position to the center of the bezel.
At this time, the raster width will be $|L1-L2| \leq 2.0$mm.

2.8.4.3 Adjusting the left/right distortion, picture width, picture position (H-PHASE) and vertical linearity (all modes)

Status indicator	Adjustment item	Adjustment mode/set	Input signal/pattern
	Left/right distortion, picture width, picture size, V-LIN		No. 12 : 106.25K / 85Hz
			Crosshatch with frame

(1) Set V-POSI of the user mode to 50%.

<Setting in the factory mode for the following steps>
(2) Adjust the vertical size to approx. 295mm, and the vertical position to the approximate center.
(3) Select V-LIN and V-LIN-BAL with the OSD, and adjust so that the vertical linearity is equal at the very top of the picture, at the very bottom of the picture, and at the center of the picture.
(4) Select V-SIZE and V-POSI with the OSD, and adjust the vertical width and vertical position to the specified values using the ADJUST buttons.
(5) Select PCC-AMP, PCC-PHASE, PCC-CENTER, TOP-PCC, and BOTTOM-PCC with the OSD, and adjust the vertical line at both side of the picture to the straight line using the ADJUST buttons.

(6) If the left and right distortions differ, select PIN-BALANCE, KEY-BALANCE, TOP-BALANCE and BOTTOM-BALANCE with the OSD, and adjust so that the distortions are visually balanced.

(7) Select H-PHASE with the OSD, and adjust the horizontal raster position to the center of the picture using the ADJUST buttons.

(8) Select H-SIZE with the OSD, and adjust the horizontal raster width to the value given in the adjustment list using the ADJUST buttons.
* Note that the picture position and distortion must be within the ranges given in the picture performance inspection items.

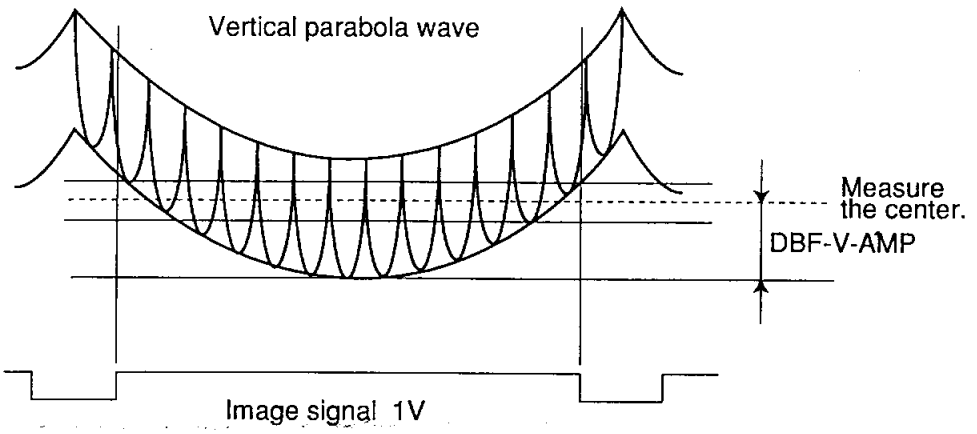
2.8.4.4 Adjusting the DBF amplitude and phase

(1) Connect the oscilloscope to the AG601 of PWB-MAIN and to one of the signal outputs for the signal sources full R, G, B (VIDEO).

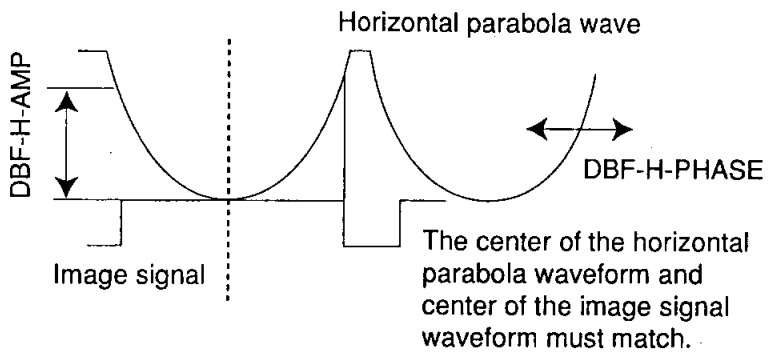
(2) Set the OSD to the select picture of DBF-H-AMP, and using the (-) (+) ADJUST buttons adjust the horizontal parabola wave amplitude (image area) to the value given in the list of adjustment values.

(3) Set the OSD to the select picture of DBF-H-PHASE, and using the (-) (+) ADJUST buttons adjust the horizontal parabola wave phase as shown below in respect to the image signal.

(4) Set the OSD to the DBF-V-AMP (X2-L) select picture, and using the (-) (+) ADJUST buttons adjust the vertical parabola wave amplitude (image area) to the value given in the list of adjustment values.



DBF-V-AMP adjustment



DBF-H-AMP adjustment

2.8.5 Adjusting the cut off (using the automatic adjustment device)

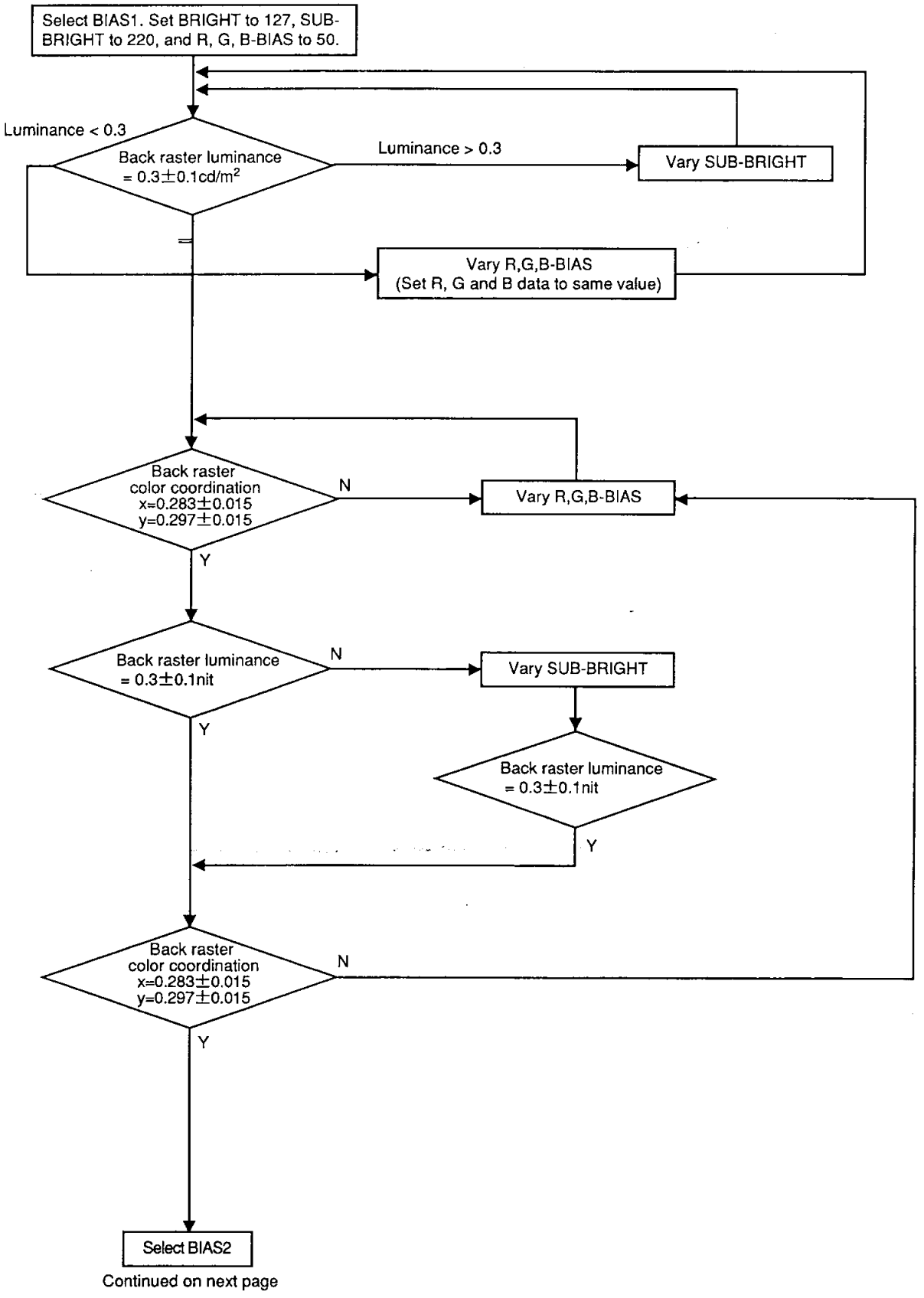
Status indicator	Adjustment item	Adjustment mode/set	Input signal/pattern
	Cut off	Factory	No. 12 : 106.25K / 85Hz

(1) Input the timing No. 12 from the signal source. (R, G, B OFF)
(2) Select BIAS1, and set BRIGHT to 127, SUB-BRIGHT to 220, and the R, G, B-BIAS to 50.
(3) Adjust the back raster luminance to 0.3±0.1cd/m².
(a) If 0.3cd/m² or more, change SUB-BRIGHT to adjust.
(b) If less than 0.3cd/m², change R, G, B-BIAS to adjust.
The R, G, B-BIAS data must be the same values at this time.
(4) Using two colors except for the basic colors, adjust the color coordination to the following values.
(5) Change SUB-BRIGHT, and adjust the back raster luminance to 0.3±0.1cd/m².
If adjustments with just SUB-BRIGHT are not possible, change BRIGHT and adjust.
(6) If the back raster color coordination is deviated from the following values, repeat steps (4) and (5).
(If the back raster cannot disappear, set BRIGHT to min., and set to the point where the back raster is eliminated with SUB-BRIGHT. Next, change BRIGHT, and adjust the back raster luminance to 0.3±0.05cd/m², and then adjust again from step (3).)
(7) Copy COLOR 1 G-BIAS, to the COLOR 2, 3 G-BIAS.
(8) Select BIAS 2, and change the BIAS data for the R and B colors (G-BIAS is fixed). Adjust the back raster color coordination to the following table.
(9) Select BIAS 3, and change the BIAS data for the R and B colors (G-BIAS is fixed). Adjust the back raster color coordination to the following table.

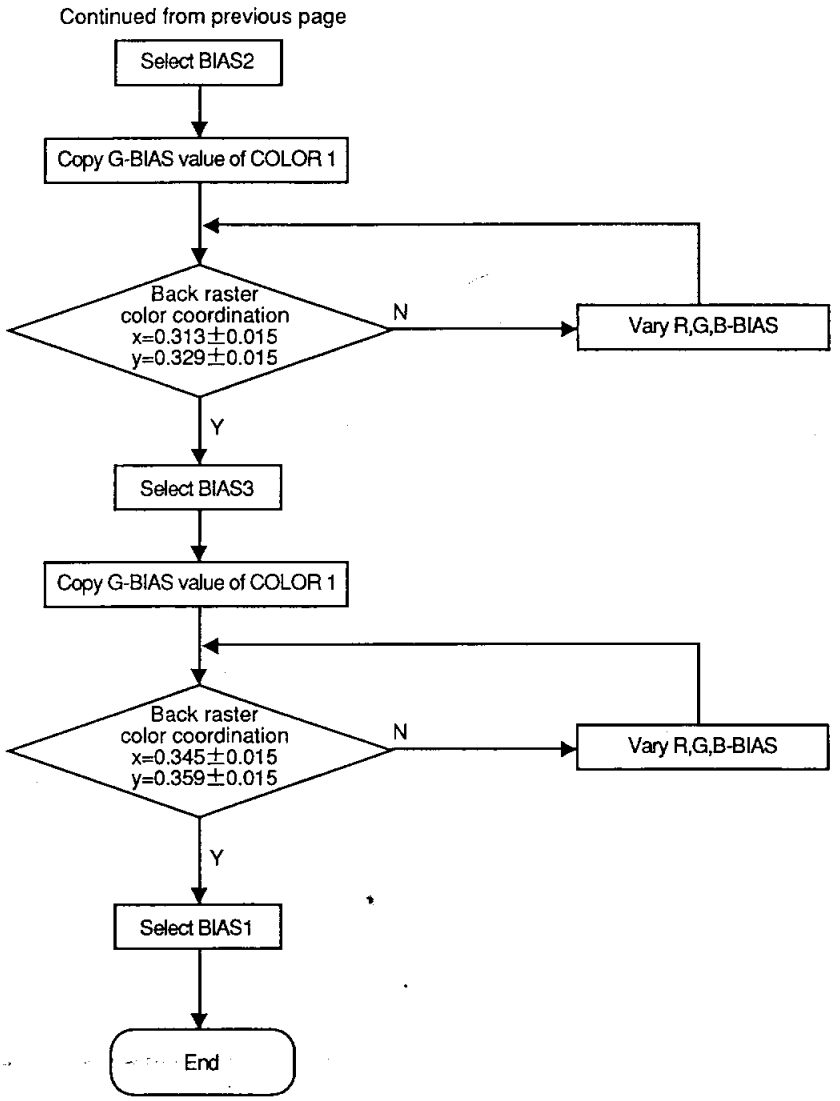
Model	Confirmation item		COLOR 1	COLOR 2	COLOR 3
All models	Color coordination	x	0.283±0.015	0.313±0.015	0.345±0.015
		y	0.297±0.015	0.329±0.015	0.359±0.015

*The flow chart is provided on the next page.

Cutoff adjustment procedures



Continued on next page


Continued from previous page
Select BIAS2
Copy G-BIAS value of COLOR 1
Back raster color coordination x=0.313±0.015 y=0.329±0.015
N
Vary R,G,B-BIAS
Y
Select BIAS3
Copy G-BIAS value of COLOR 1
Back raster color coordination x=0.345±0.015 y=0.359±0.015
N
Vary R,G,B-BIAS
Y
Select BIAS1
End

2.8.6 Adjusting the RGB drive signal

2.8.6.1 Adjusting the R, G, B drive signal (Adjustment of COLOR 1)

Status indicator	Adjustment item	Adjustment mode/set	Input signal/pattern
	R, G, B drive signal	Factory	No. 12 : 106.25K / 85Hz
			WINDOW picture

(1) Input the following adjustment timing at the signal source.
WINDOW picture (Input amplitude = 0.7Vp-p)

Model group	Adjustment timing
All model	Timing No. 12 (1600 x 1200 106.25K/85)

(2) Select CONTRAST with the OSD, and set to MAX with (+) ADJUST button.
(3) Select BRIGHT with the OSD, and set the data to 127 with the (-) (+) ADJUST buttons.
(4) Set the signal generator A output to the WINDOW pattern (approx. 80mm square at center of CRT picture), and input only "GREEN".
(5) Set the COLOR 1 G with the OSD, and adjust the luminance to the following value with the ADJUST button.
(6) Input BLUE, RED and GREEN, appropriately select the COLOR 1 B and R, and adjust the color coordination to the following value with the ADJUST button.
(7) Set CONTRAST to 25cd/m² with the OSD to confirm that the change in color coordination is within ±0.015 for both x and y.
*Adjust COLOR 2 and 3 to the following values with the same method.

(Note) After adjusting COLOR, always set to COLOR 1.
(The COLOR preset will be set to the default COLOR 1 with this step.)

Model group	COLOR		1	2	3	Remarks
All models	G-WINDOW luminance		(76.0)	(67.0)	(56.0)	(Reference value)
	W-WINDOW color coordination	x	0.283	0.313	0.345	±0.005
		y	0.297	0.329	0.359	±0.005
	Full white luminance(cd/m²)		105 or more	92 or more	77 or more	

2.8.6.2 Adjusting ABL

Status indicator	Adjustment item	Adjustment mode/set	Input signal/pattern
	ABL	Factory	No. 12 : 106.25K / 85Hz
			Full white

(1) Set the OSD ABL to 254.
(2) Input timing No. 12 at the signal source.
(Full white picture input amplitude = 0.7Vp-p)
(3) Set contrast to MAX, bright to MAX, and select ABL-ADJUST with OSD. Adjust to 115cd/m²±5 with COLOR 1.
The picture size must be approximately the H width given in the list of adjustment values at this time.

2.8.7 Adjusting the Purity

Status indicator	Adjustment item	Adjustment mode/set	Input signal/pattern
	Purity	Factory	Check 4 : 85Hz
			RED crosshatch reverse

(1) Input the check 4 timing: 1600 x 1200/85Hz at the signal source to confirm that the RED crosshatch is displayed in reverse.
(2) Set the chamber adjustment magnetic field to the northern hemisphere magnetic field (HORIZ. = 0mT, VERT. = +0.04mT).
(3) After carefully degaussing the monitor with 100V handy-demagnetizer, demagnetize with a demagnetizer.
(4) Set the monitor to the factory mode from the front, select H-Purity, and press the ENTER button once.
With this, the calibration of the horizontal (tube axis) and vertical (two way) geomagnetism sensor will be carried out by the MPU.
Confirm that the current that flows to HCANCEL-Coil at this time is within 0±5mA.
If not within 0±5mA, select H-Purity, and adjust to within 0±5mA.
(5) Fully scan the picture size with the normal mode to confirm the below effective magnetic field allowance. (Carry out the 45-degree rotation check only for the tube axis direction magnetic field.)

(a)Effective magnetic field (Magnetic field for adjustment magnetic field)
(1) BH: +0.04mT (2) BH: -0.04mT
(3) BV: +0.035mT (Northern hemisphere) (4) BV: -0.04mT (Northern hemisphere)
(5) BV: +0.04mT (Southern hemisphere) (6) BV: -0.04mT (Southern hemisphere)
(Equator) (Equator)
(b) Demagnetize with a demagnetizer.
(c)Judgment

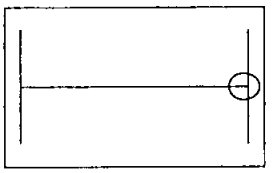
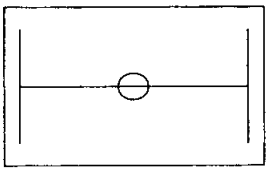
Repeat the effective magnetic field four times in the following order.
(1) (2) (3) (4) ... (Northern hemisphere)
(1) (2) (5) (6) ... (Southern hemisphere)
(Equator)

* Repeat (a) to (e) four times for each effective magnetic field.
** When another color is hit while checking the 45-degree rotation of the tube axis direction magnetic field, if the level is not a problem in use of the normal mode Corner Purity, the level will be OK.
*** Before checking the vertical magnetic field, set the effective magnetic field, and then carry out manual degaussing on OSD once.

(6) After confirming the effective magnetic field allowance in step (5), return to the adjustment (reference) magnetic field. After carefully degaussing the monitor with 100V handy-demagnetizer, confirm that the current flowing to the HCANCEL-Coil is within 0±5mA.
If not within 0±5mA, adjust again from step (4).
(7) Set the chamber adjustment magnetic field to the Southern hemisphere magnetic field (HORIZ. = 0mT, VERT. = -0.04mT).
(8) After carefully degaussing the monitor with 100V handy-demagnetizer, degauss with a demagnetizer.
(9) Repeat steps (5) and (6).
(10) Set the chamber adjustment magnetic field to the Equator magnetic field (HORIZ. = 0mT, VERT. = 0mT).
(11) After carefully degaussing the monitor with 100V handy-demagnetizer, degauss with a demagnetizer.
(12) Repeat steps (5) and (6).

2.8.8 Adjusting the focus

Status indicator	Adjustment item	Adjustment mode/set	Input signal/pattern
	Focus		No. 12 : 106.25K / 85Hz
			H character, crosshatch

	Normal or reverse display	Point to align with
Vertical line	Reverse display	 FOCUS JUST at center of right side vertical line (circle section).
Horizontal line	Normal display	 FOCUS JUST at center of screen (circle section).

<Adjusting the static focus>

Status indicator	Adjustment item	Adjustment mode/set	Input signal/pattern
	Static focus		No. 12 : 106.25K / 85Hz
			H character, crosshatch

For steps (1) and (2), use the timing No. 12 (1600 x 1200 106.25K/85) H character pattern and crosshatch pattern.
For step (3), use all preset timing H character patterns and crosshatch patterns.

(1) Display a white crosshatch pattern, and adjust the focus following section "2.8.8 Adjusting the focus".
(2) If the DBF voltage is insufficient or excessive, select DBF H AMP (X2-L)/DBF H AMP (X2-R) and DBF V AMP from the OSD, and readjust with the ADJUST button. Then repeat step (1), and adjust so that the following judgement conditions are satisfied.
(3) For all of the other preset timings, if the DBF voltage is insufficient or excessive, select DBF H AMP (X2-L)/DBF H AMP (X2-R) and DBF V AMP from the OSD, and readjust with the ADJUST button.

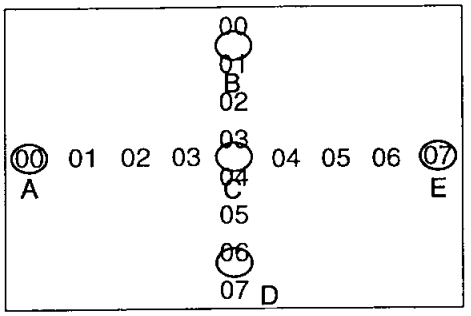
*Adjustment votlage max value:

DBF-H-AMP	H width: 393mm:	430V
	H width: 369mm:	400V
DBF-V-AMP	V width: 295mm:	190V

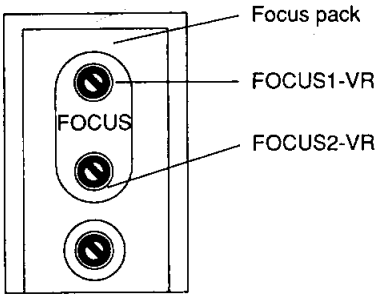
The focus is judged as follows.

Timing	Judgment pattern (Note 1) (Note 2)
Normal display (All preset)	Crosshatch pattern
Reverse display Resolution: ≤1600x1200 Resolution: ≥1600x1200	 Judge with pattern A Judge with pattern B

(Note 1) Pattern A: Font 7 ×9, Cell 10×11, e character
(Note 2) Pattern B: Font 7 ×9, Cell 10×11, H character
Core: Judge the ratio of the halo (total area 1:1).
To judge the reverse display, do not carry out a relative evaluation with the other point on the screen. Instead, judge whether the e (H) character can be read at that point.



Focus attention point



Focus pack

2.8.9 Adjusting the convergence

2.8.9.1 Adjusting with ITC

Before adjusting the center mis-convergence and axial mis-convergence, carry out sufficient full white aging (100cd/m² or more, for one hour or more). Then, adjust with the following timing.

Timing: No. 12 (1600 x 1200 106.25K/85) crosshatch pattern

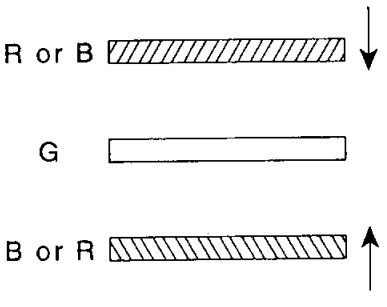
Confirm that the following DDCP default setting is as shown in the table.

Section 2.7.3.2 (1) Factory mode 1 in section 2.7.3 OSD display matrix
H-CONVERGENCE, V-CONVERGENCE,

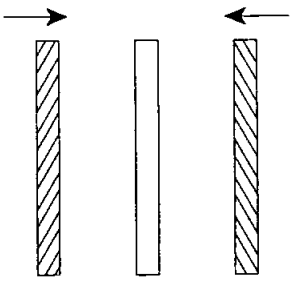
Section 2.7.3.2 (2) Factory mode 2 in section 2.7.3 OSD display matrix
All of FACT01

Adjust the horizontal and vertical convergence to the optimum setting with the CRT CP ring, etc.

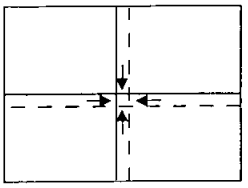
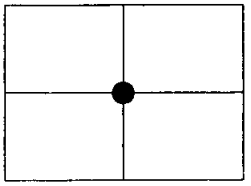
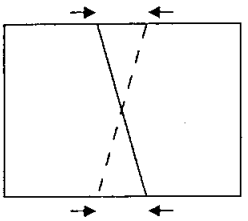
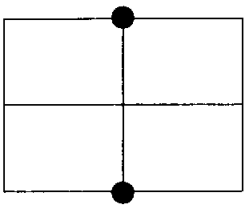
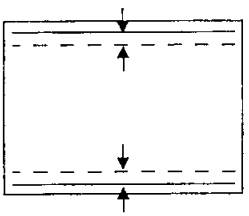
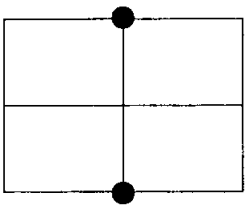
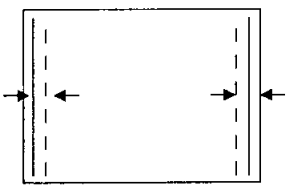
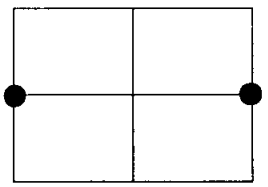
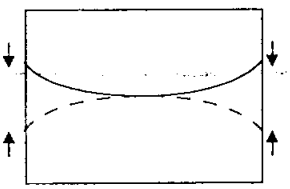
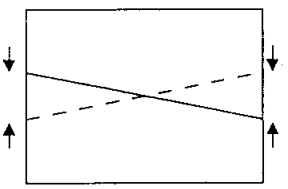
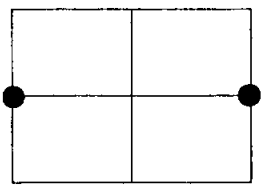
(Refer to following drawings.)



Vertical convergence


Horizontal convergence

Adjusting the center miss convergence and axial miss convergence

Adjustment item name	Problem	Adjustment point	Adjustment procedure
H-STATIC V-STATIC			Adjust to ±0.01mm or less with CP-ASSY 4P.
YH axial deviation			Adjust so that TOP+BOTTOM are ±0.01mm or less with YH volume.
YV axial deviation			Adjust so that TOP-BOTTOM is ±0.01mm or less with YV volume.
XH axial deviation			Adjust so that TOP+BOTTOM is ±0.01mm or less with XH slider.
XV characteristics XV axial deviation	 		Only when XV (B-Bow) is ± 0.01mm or more, adjust so that LEFT-RIGHT is ± 0.01mm or less with the interlock of B-Bow 4P and CP-ASSY 4P. Adjust so that LEFT+RIGHT is ±0.1mm or less with XV differential.

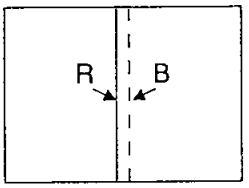
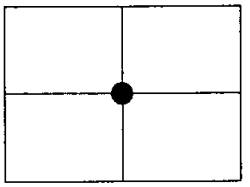
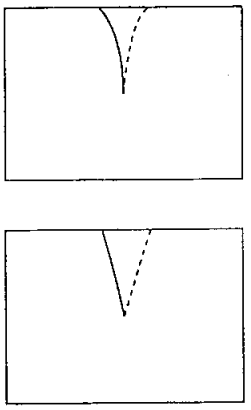
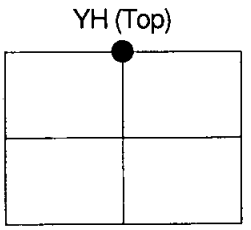
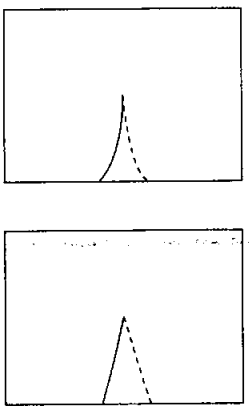
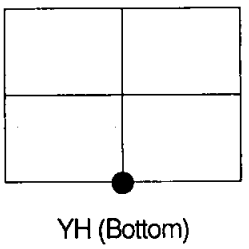
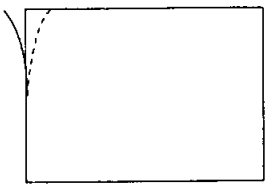
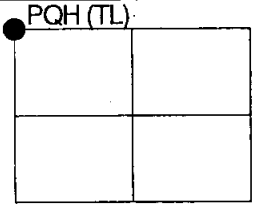
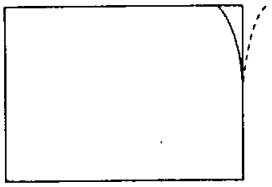
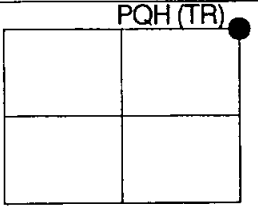
2.8.9.2 Adjusting DDCP (using automatic adjustment device)

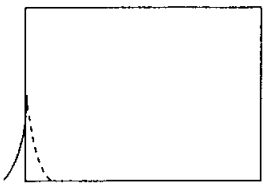
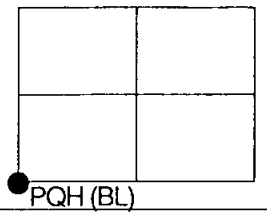
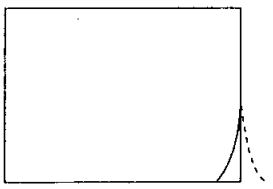
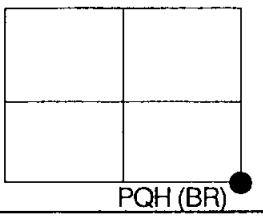
The method for carrying out the automatic adjustment manually is explained below.

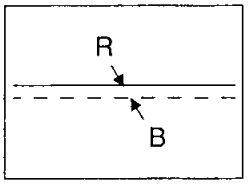
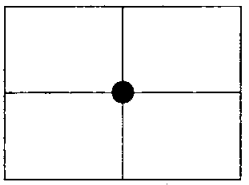
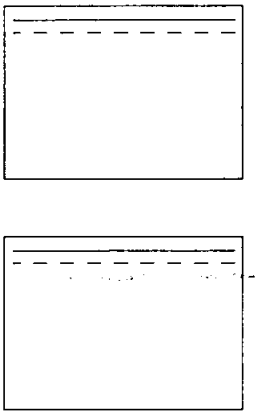
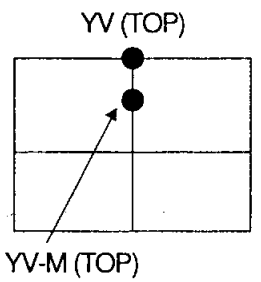
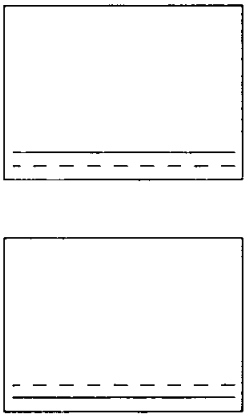
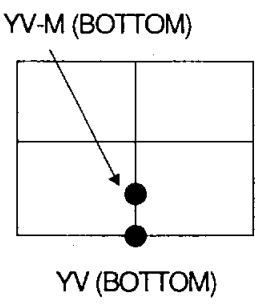
(1) Input the timing No. 12 (1600 x 1200 106.2K/85) crosshatch pattern.

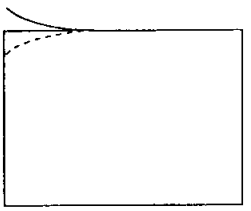
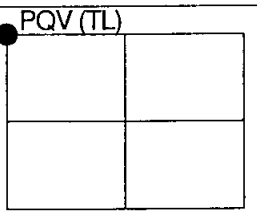
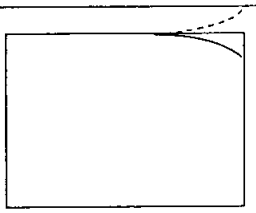
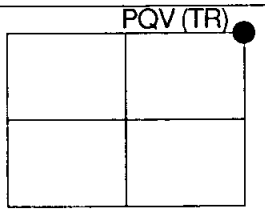
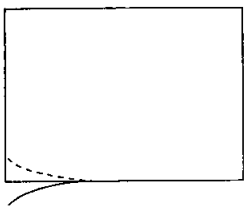
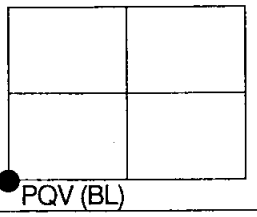
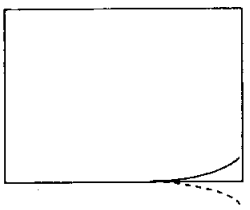
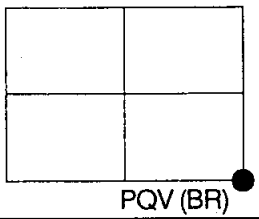
(2) Enter the factory mode.

(3) Adjust in the following order. (It is assumed that the center and axial mis-convergence on the previous page have already been adjusted.)

Adjustment order	Adjustment item name	Problem	Adjustment point	Adjustment procedure
4H-COIL				
1	HORIZ-CONVERGENCE			Adjust to 0.05mm or less. (Adjustment target is 0mm.)
2	YH-TT YH-JT			Adjust to 0.05mm or less. (Adjustment target is 0mm.)
3	YH-TB YY-JB			Adjust to 0.05mm or less. (Adjustment target is 0mm.)
4	4HTL			Adjust to 0.3mm or less.
5	4HTR			Adjust to 0.3mm or less.

Adjustment order	Adjustment item name	Problem	Adjustment point	Adjustment procedure
4H-COIL				
6	4HBL			Adjust to 0.3mm or less.
7	4HBR			Adjust to 0.3mm or less.

Adjustment order	Adjustment item name	Problem	Adjustment point	Adjustment procedure
4V-COIL				
1	VERT-CONVERGENCE			Adjust to 0.05mm or less. (Adjustment target is 0mm.)
2	YV-TT YV-JT			Adjust YV (TOP) to 0.05mm or less with balance adjustment of YV-TT and YV-JT. (Adjustment target is 0mm.) (Note) The operating amount at YV-M (TOP) when moving YV-TT and YV-JT. YV-TT<YV-JT
3	YV-TB YV-JB			Adjust YV (BOTTOM) to 0.05mm or less with balance adjustment of YV-TB and YV-JB. (Adjustment target is 0mm.) (Note) The operating amount at YV-M (BOTTOM) when moving YV-TB and YV-JB. YV-TB<YV-JB

Adjustment order	Adjustment item name	Problem	Adjustment point	Adjustment procedure
4V-COIL				
4	4VTL			Adjust to 0.3mm or less.
5	4VTR			Adjust to 0.3mm or less.
6	4VBL			Adjust to 0.3mm or less.
7	4VBR			Adjust to 0.3mm or less.

* Specify the adjustment value range of the following adjustment items in general DDCP adjustment.

Adjustment items	Adjustment value range (Factory mode))
H-CONVERGENCE	77~177 (OSD display value=DAC output value)
V-CONVERGENCE	77~177 (OSD display value=DAC output value)

2.8.10 Default settings (With factory mode)

Status indicator	Adjustment item	Adjustment mode/set	Input signal/pattern
	Default settings	Factory mode	Each adjustment timing
			Crosshatch

(1) Set the default values as shown in the table (user mode) given in the OSD display (Table of section 2.7.3-(1).)
If the setting class is an item for each timing, carry out for each adjustment timing except the item of default setting "CENTER".

(2) Return to the user mode with the front panel or automatic adjustment device.

(3) Execute ALL RESET to confirm that each OSD setting is as shown in the table (user mode) given in the OSD display (section 2.7.3(1)).
The default setting CENTER is the factory adjustment value called when the (-) (+) ADJUST buttons are pressed simultaneously in the normal mode.
Only CONTRAST will be set to 100% when the (-) (+) ADJUST buttons are pressed simultaneously in the normal mode.

(4) After setting the default values, turn the power switch OFF.

2.9 Inspections (In normal mode)

Status indicator	Adjustment item	Adjustment mode/set	Input signal/pattern
	Inspections	Normal mode	

2.9.1 Electrical performance

Inspect the electrical performance by setting contrast to MAX and bright to center (press the (-) (+) ADJUST buttons simultaneously).

2.9.1.1 Withstand voltage

There must be no abnormality when 1500VAC is applied for two seconds between both ends of the AC input terminal and chassis, and between the DG coil terminal and chassis.

2.9.1.2 Grounding conductivity check

Check that the resistance value is 100mΩ or less when 25A is passed between the AC input terminal grounding GND and chassis GND.

2.9.1.3 Degaussing coil operation

Confirm that when OSD DEGAUSS is executed, the picture vibrates and then stops.

2.9.1.4 POWER SAVE function operation (Set the AC power input to 230V)

Model	Confirmation timing
All model	Timing No. 12 (1600 x 1200 106.25K/85)

Use the full white pattern without R, G, B signals.
Select POWER-SAVE from the OSD, and set the POWER-SAVE function ON.
(Note) For the USB, do not connect a pseudo-USB load. Instead measure the following power consumption.

(1) POWER SAVE ON

(a) Confirm that when any SYNC (H, V, H&V) is removed, the system waits for approx. five seconds, displays POWER SAVE for approx. three seconds, and then the picture dark ens.
Also confirm that the power LED changes to orange and the power consumption is as follows.

Power consumption	5W or less

(b) Confirm that when SYNC is input again, the high voltage is recovered, and the picture appears in approx. three seconds.

2.9.1.5 Confirming the MOIRE-CLEAR function

Status indicator	Adjustment item	Adjustment mode/set	Input signal/pattern
	MOIRE-CLEAR		No. 10 : 91.1K / 85Hz

Input timing No. 10 (1280 x 1024 91.1K/85.0), and turn the MOIRE-CLEAR function ON. Confirm that the picture vibrates in the horizontal direction.

2.9.1.6 Confirming the CORNER-PURITY function

Model	Confirmation timing
All model	Timing No. 12 (1600 x 1200 106.25K/85)

Input a (full white display), and press the (-)(+) ADJUST buttons to change the CORNER PURITY (TR/TL/BR/BL). Confirm that the color coordination around the picture changes.

2.9.1.7 Focus, picture performance (Timing No. 12 (1600 x 1200 @ 85Hz))

Status indicator	Adjustment item	Adjustment mode/set	Input signal/pattern
	Focus, picture performance		No. 12 : 85Hz

The picture must be evenly bright with the "e" character normal and reverse displays.

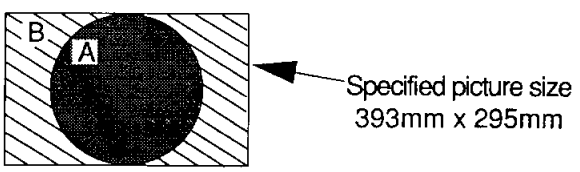
2.9.1.8 Mis-convergence

After heat running for 20 minutes or more, the mis-convergence amount in the horizontal and vertical directions when the set is faced to the East or West must be below the following values.

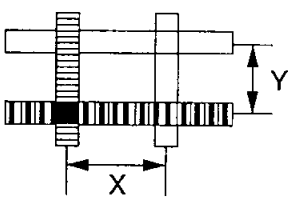
The mis-convergence amount is the value between the two colors of R, G and B separated the most in the horizontal (X) and vertical (Y) directions when a 17 vertical line x 13 horizontal line crosshatch is displayed.

Zone	Mis-convergence amount				
	All models				
Center	0.2mm or less				
A	0.3mm or less				
B	0.4mm or less				
Measurement timing (Timing No.)	12				

<Zone>



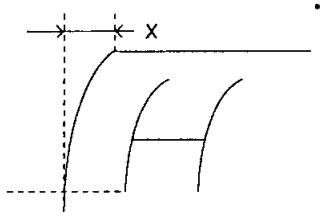
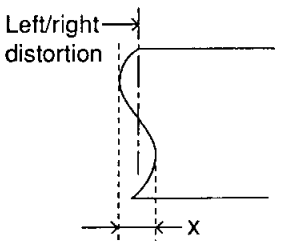
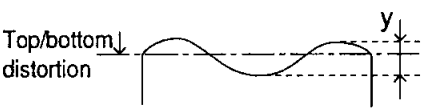
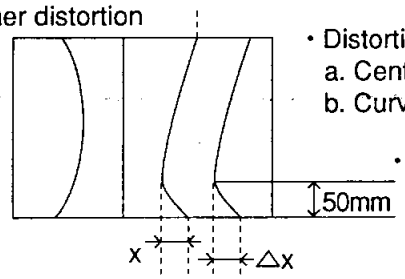
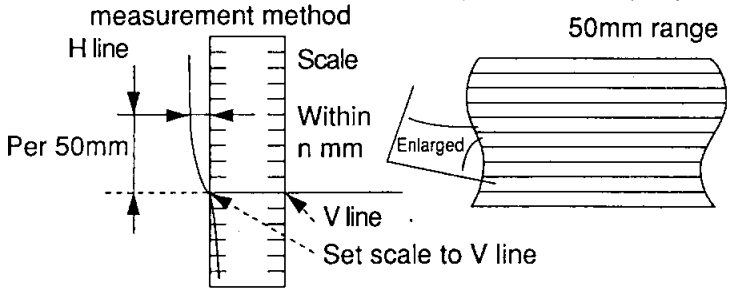
<Mis-convergence amount>

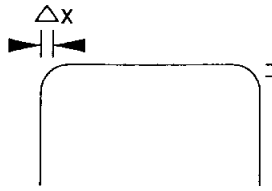
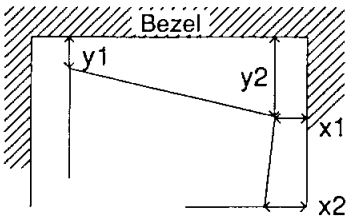
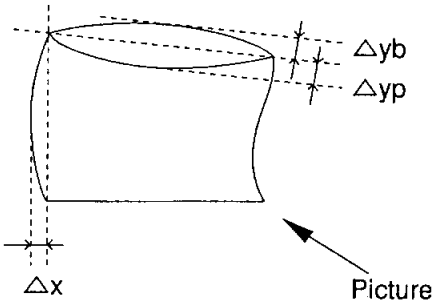
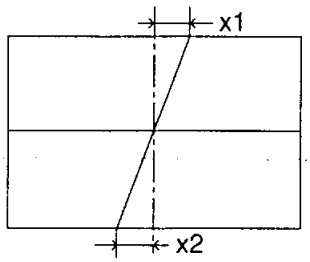
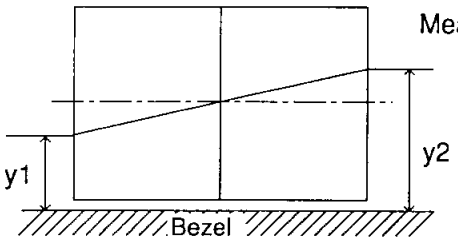


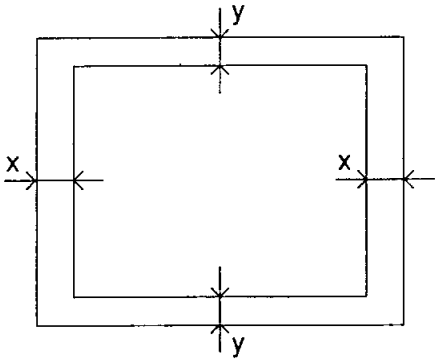
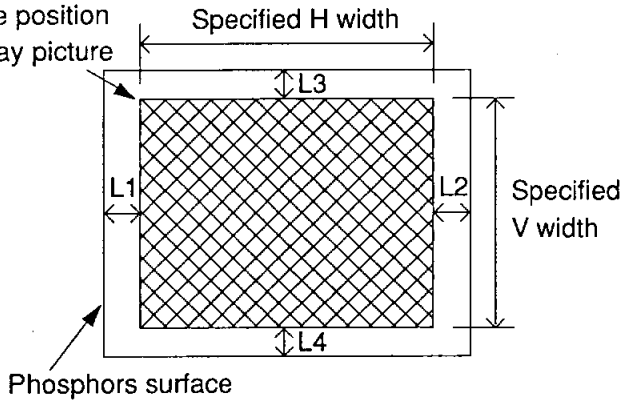
2.9.1.9 Picture distortion

When the picture distortion is measured, each distortion of the preset timing must be less than the following values.

<Picture performance inspection items> Inspect the following items for the picture distortion.

No.	Item	Judgement reference value	Input signal
1.	4-corner section distortion Inspect the distortion at the four corners. ・Signal, H character with frame (both normal/reverse)  ・Distortion x: Distortion in the range of one H character height. Judge with the white display G. (Judge the distortion amount with a fluorescent material stripe.)	x≦1pitch (=0.3mm)	H character with frame (both normal/ reverse)
2.	4-edge distortion When S-character or seagull type high frequency distortion is visible, check with the following method.  ・Distortion x of S-character distortion, etc.: Distortion excluding normal pin, barrel or trapezoid. Note: There must be no sea-gull distortion.  ・Distortion y: High frequency distortion excluding trapezoid.	x≦0.6mm * Note y≦1.0mm	Crosshatch pattern
3.	Inner distortion  ・Distortion x: a. Center line b. Curve of other vertical line ・Distortion x: a. Center line b. Curve of other vertical line Vertical line △X measurement method  ・Distortion △x: Curve within 50mm range	a. x≦1.0mm b. x≦1.5mm (*) (*) Present No. 0 (31.5kHz, 60Hz) is: a. x≦1.5mm b. x≦2.0mm △x≦0.6mm	

No.	Item	Judgement reference value	Input signal
4.	Line curve (crosshatch pattern outer contour)  △x: Curve within 50mm range (horizontal) △y: Curve within 50mm range (vertical)	△x≦1.0mm △y≦1.0mm	Crosshatch pattern
5.	Horizontal trapezoid (top/bottom), vertical trapezoid (left/right)  ・△y= | y1-y2 | △x= | x1-x2 | ・Control with the above right value for each the top, bottom, left and right.	△y≦2.0mm △x≦1.8mm	
6.	Top/bottom pin and barrel, left/right pin and barrel  	(Provisional standards) △yb≦1.0mm △yp≦1.5mm △x ≦1.0mm	
7.	Parallelogram distortion  Measure the larger of x1 and x2.	x ≦0.8mm	
8.	Inclination  Measure △y = |y1-y2|.	△y≦2.0mm	

No.	Item	Judgement reference value	Input signal
9.	Distortion Must be within the following frame. ※ (Note, excluding ROTATION) 	y≦2.0mm x≦2.0mm	Crosshatch pattern
10.	Picture position Display picture 	| L1-L2 | ≦ 5.0mm | L3-L4 | ≦ 3.0mm	Full white

2.9.1.10 Linearity

Measure the linearity with a 17 horizontal line x 13 vertical line crosshatch.

Horizontal linearity : fH=30-40kHz whole : 15% or less, adjacent : 7% or less
fH=40-60kHz whole : 12% or less, adjacent : 7% or less
fH=60-121kHz whole : 10% or less, adjacent : 7% or less

Vertical linearity : whole : 10% or less, adjacent : 7% or less

Calculation expression : (Xmax x Xmin) / Xmax x 100%

* If any doubts arise about the judgment, judge with the horizontal/vertical width tolerance of ±3mm, picture position: |L1-L2|≤3.0mm and |L3-L4|≤3.0mm.

2.9.1.11 Picture default

Refer to NF51 picture default detection standard.

2.9.1.12 Adjustment value list

The horizontal width, vertical width and DBF-H amplitude must be within the following ranges.

Timing	Horizontal width (mm)			Vertical width (mm)			DBF-H amplitude (V)			DBF-V amplitude (V)		
No.	Adj.value			Adj.value			Standard adj.value	Max. adj.value		Standard adj.value	Max. adj.value	
1												
2	393±5			295±4			370±10	430		145±10	190	
3												
4												
5												
6	393±5			295±4			370±10	430		145±10	190	
7	393±5			295±4			370±10	430		145±10	190	
8	393±5			295±4			370±10	430		145±10	190	
9	369±5			295±4			370±10	430		145±10	190	
10	369±5			295±4			370±10	430		145±10	190	
11	393±5			295±4			370±10	430		145±10	190	
12	393±5			295±4			370±10	430		145±10	190	
13												
14												
15	393±5			295±4			370±10	430		145±10	190	
16												
17												
18												
19	393±5			295±4			370±10	430		145±10	190	
20												
21												
22												
23												
24												
25	393±5			295±4			370±10	430		145±10	190	
26												
27												
28	393±5			295±4			370±10	430		145±10	190	

Standard adjustment value: in case of determining DBF voltage
Maximum adjustment value: the value impossible to set the maximum of DBF voltage

2.9.1.13 Confirming CLAMP PULSE POSITION

Confirm to satisfy the following standard when inputting the optional timing.

Timing : Check1 (35k/66), full white

Criterion: Back raster must be changed.

2.9.1.14 Checking the functions during Sync on Green and Composite Sync input

Status indicator	Adjustment item	Adjustment mode/set	Input signal/pattern
	Checking the functions during Sync on Green and Composite Sync input		Check 1 : 35K / 66Hz, Check 2 : 35K / 66Hz
			Full white

[Sync on Green]

Timing: Check 1 (35K/66), full white

[Composite Sync]

Timing: Check 2 (35K/66), full white

In the normal mode, input the above timing into any connector of D-SUBx2 input to confirm that the operation is normal.

2.9.1.15 Confirming the D-SUBx2 input (Timing No. 12 1600 x 1200 @85Hz)

Status indicator	Adjustment item	Adjustment mode/set	Input signal/pattern
	Confirming the D-SUBx2 input		No. 12 : 85Hz

Confirm the input select function for both D-SUBx2 with the following procedure.

Confirm one of the following with an independent stage.

(1) After connecting D-SUB, press the front button (D-SUBx2) and confirm that after the picture darkens it returns to the normal state.

(2) After connecting BNC, press the front button (D-SUBx2) and confirm that after the picture darkens it returns to the normal state.

2.9.1.16 Confirming the reset operation

Model	Confirmation timing
All model	Timing No. 12 (1600 x 1200 106.25K/85)

Carry out the following confirmation in the NORMAL MODE.

After varying the H-SIZE data somewhat, press the (-)(+) ADJUST buttons simultaneously to confirm that the data returns to the original value.

2.9.1.17 Confirming the full white luminance

Status indicator	Adjustment item	Adjustment mode/set	Input signal/pattern
	Confirming the full white luminance		No. 12 : 85Hz
			Full white

Timing No. 12 (1600 x 1200 106.25K/85), input amplitude = 0.7Vp-p

Confirm that the full white luminance is the following value.

Full white luminance (cd/m^2)

Model	COLOR 1	COLOR 2	COLOR 3	Remarks
All models	105 or more	92 or more	77 or more	

2.9.1.18 Confirming CONVERGENCE compensation function

Confirm that CONVERGENCE changes by varying H-CONVERGENCE and V-CONVERGENCE.

2.9.1.19 Confirming ROTATION compensation function

Confirm that the picture rorates by changing ROTATION.

2.9.1.20 Luminance/color coordination uniformity

Status indicator	Adjustment item	Adjustment mode/set	Input signal/pattern
	Luminance/color coordination uniformity		No. 12 : 106.25K / 85Hz

The luminance ratio between the center and periphery must be 80% or more with timing No. 12 (1600 x 1200 @85Hz) COLOR 1.
The color coordination difference between the center and periphery must be $\Delta x, y < \pm 0.012$ at COLOR 1/2/3.

2.9.1.21 Confirming the full white color coordination

Confirm that the color coordination at the center of the full white is within the following range at the drive signal adjustment timing.

Model	Confirmation item		COLOR 1	COLOR 2	COLOR 3
All models	Color coordination	x	0.283±0.007	0.313±0.007	0.345±0.007
		y	0.297±0.007	0.329±0.007	0.359±0.007

※ OSD color coordination confirmation X=0.283±0.04 Y=0.297±0.05
(Confirm at the white section of the OSD.)

2.9.1.22 Confirming the color tracking

Status indicator	Adjustment item	Adjustment mode/set	Input signal/pattern
	Confirming the color tracking		No. 12 : 106.25K / 85Hz
			Full white

Confirm with timing No. 12 (1600 x 1200 @85Hz).
Measure the color coordination at the center of the picture using a full white pattern (input amplitude = 0.7Vp-p).

(a) Confirm that the color coordination change is within the ±0.015 range when the CONTRAST is set to 25cd/m² with the OSD.
(b) Confirm that the color coordination change is within the ±0.015 range when the input amplitude is set to 0.22Vp-p at the signal source.

2.9.1.23 CRT installation position

CRT installation position tolerance Within ±3mm in vertical direction Within ±2.5mm in horizontal direction
Inclination: Within ±2.5mm at bezel reference

2.9.1.24 Confirming FPM operation

Confirm with Timing No. 12 and COLOR 1.
Confirm that the relation of the window luminance with the back raster luminance in each mode is as follows.

	Normal	Text	Graphic
Window luminance	Standard	Low	Standard
Back raster luminance	Standard	Low	Low

※ Confirm that the color is not saturated when Graphic mode.

2.9.1.25 Confirming the geomagnetism tolerance (Timing No. 12: 1600 x 1200 106.25K/85)

Status indicator	Adjustment item	Adjustment mode/set	Input signal/pattern
	Confirming the geomagnetism tolerance		No. 12 : 106.25K / 85Hz

There must be no apparent color unevenness with each single color when the magnetic field is changed with the following procedure. The display picture size is 393mm x 295mm.

1. Northern hemisphere magnetic field : Horizontal magnetic field (B_H) : 0±0.04mT
   Vertical magnetic field (B_V) : +0.04±0.035mT/-0.04mT
2. Southern hemisphere magnetic field : Horizontal magnetic field (B_H) : 0±0.04mT
   Vertical magnetic field (B_V) : -0.04±0.04mT
3. Equator magnetic field : Horizontal magnetic field (B_H) : 0±0.04mT
   Vertical magnetic field (B_V) : 0±0.04mT

<Confirmation procedure>
Completely demagnetize the entire unit including the monitor plates, CRT, funnel section, along the DG coil and face surface with handy-demagnetizer (100V) at the magnetic fields for BH = 0G and Bv = destination. Then, change BH and Bv to the above values, and demagnetize again. Then, visually confirm.
Note that when changing Bv, set to the effective magnetic field, and then carry out manual degaussing on the OSD once before confirming.

2.9.1.26 Confirming the cancel function operation

Status indicator	Adjustment item	Adjustment mode/set	Input signal/pattern
	Confirming the cancel function operation		No. 12 : 106.25K / 85Hz

(1) Confirm that the following cancel function operates correctly when the tube axial magnetic field (BH) is moved 0.04mT in the + direction or - direction.
(2) Confirm that the cancel function operates correctly when the vertical magnetic field (Bv) is moved by the following value in the + direction or - direction.
Note that when changing Bv, set to the effective magnetic field, and then carry out manual degaussing on the OSD once before confirming.
   1. Northern hemisphere magnetic field : +0.035mT/-0.04mT
   2. Southern hemisphere magnetic field : ±0.04mT
   3. Equator magnetic field : ±0.04mT

2.9.1.27 Confirming the grill vibration

Status indicator	Adjustment item	Adjustment mode/set	Input signal/pattern
	Confirming the grill vibration		No. 12 : 106.25K / 85Hz
			Full white

(1) Tap the top of the monitor with a rubber hammer.
(Strength equivalent to shock test.)
(2) Observe from a position 60cm away from the tube surface.
(3) If the vibration continues for 10 seconds or more, judge as line out.
(4) For the set judged as line out, after carry out normal aging (30 minutes or more), apply an impact on the center of the tube surface with an impact hammer. Impact strength: 0.35Nm
(5) Observe from a position 60cm away from the tube surface.
(6) If the vibration continues for 9.5 seconds or more, replace the CRT. If the vibration is within 9.5 seconds, return to the line.

2.9.1.28 Confirming the USB hub

<Confirming the funciton control>
User the PC installed the monitor control function.
(1) Open the application of control function.
(2) Connect the upstream connector and the PCwith USB cable.
(3) Confirm that the control fucntion recognizes the monitor.
(4) discconect the USB cable.

2.9.1.29 Others

(1) When the PUSH button is pressed, the changes must be smooth, and there must be no abnormalities such as noise.
(2) Synchronization must not flow when the power switch is turned ON and OFF.
(3) Confirm that the POWER LED is lit.

2.10 Checking the DDC function (using automatic adjustment device)

This writing operation is carried out in combination with the PC.
Confirm that the PC internal clock is correctly set when preparing for this work.

2.10.1 Writing/checking the DDC and EDID data (Confirm with both input of SIGNAL A and B.)

(1) Following the PC picture displays, select the target model. (This step is carried out only once when the device is started up or the model is changed.)
(2) Turn the monitor power ON.
(3) Following the PC picture displays, write the data into the EEPROM.
The data contents shall be those designated in the table of section 2.10.3 on the next page.
(4) Following the PC picture displays, check the DDC function.
(5) There may be an error of four weeks for the manufacturing week and year information.

Low-order 5 digits of S/N → Hexadecimal conversion → Store data in order from low-order byte
6th and higher digit of S/N → Set as 0 (Follow VESA Standards)

(Example) 512002978 → 00000BA2 → MPU side Address(H) / E2PROM side Address(H) Data(H)

MPU side Address(H)	E2PROM side Address(H)	Data(H)
B6C	C0	A2
B6D	0D	0B
B6E	0E	00
B6F	0F	00

[ASCII conversion] (All models)
Read the Mitsubishi serial No. with the barcode system, and set the serial No. with the following conversion.
Low-order 5 digits of S/N → ASCII code conversion → Store data in order from low-order byte (To MONITOR DESCRIPTOR #4)
(Example) 512A02978

↓
35 31 32 41 30 32 39 37 38
↓

MPU Control side Address (H)	E2PROM side Address (H)	Data (H)	
BD1	71	35	
BD2	72	31	
BD3	73	32	
BD4	74	41	
BD5	75	30	
BD6	76	32	
BD7	77	39	
BD8	78	37	
BD9	79	38	
BDA	7A	0A	← Indicates end of S/N data
BDB	7B	20	← Indicates blank
BDC	7C	20	← Indicates blank
BDD	7D	20	← Indicates blank

Fixed data (Set according to No. of S/N digits)

2.10.2 Setting the serial No.

Store the serial No. into the following address in the EEPROM with the following procedure.

[UNICODE conversion] (All models)
Read the Mitsubishi serial No. with the barcode system, and set the serial No. with the following conversion.

S/N → UNICODE conversion → Store data in order from low-order byte (To STRING DESCRIPTOR)

(Example) 512A02978

↓

0035 0031 0032 0041 0030 0032 0039 0037 0038

↓

Head address; 0F60h

Offset address from head address	Setting data	
00	35	
01	00	
02	31	
03	00	
04	32	
05	00	
06	41	
07	00	
08	30	
09	00	
0A	32	
0B	00	
0C	39	
0D	00	
0E	37	
0F	00	
10	38	
11	00	
12	20	; Insert the space "0020" when there is a blank
13	00	

2.10.3 DDC write data contents

The contents of DDC write data must be as follows.

-- EDID DATA DUMP TEXT --
Vendor Name: MEL
Product Code LSB (HEX): F3
Product Code MSB (HEX): 43
Product Code (DEC): 17395
(Microsoft INF ID: MEL43F3)
Serial Number: **
Week of Manuf: WW
Year of Manuf: YY

EDID Version: 1
EDID Revision: 1
Extension Flag: 0

Input Singal: ANALOG
Setup: NO
Sync on Green: YES
Composite Sync: YES
Separate Sync: YES
V Sync Serration: NO
V Signal Level: 0.700V/0.300V (1V p-p)

Max Image Size H (cm): 40
Max Image Size V (cm): 30
DPMS Stand By: YES
DPMS Suspend: YES
DPMS Active Off: YES
GTF Support: YES
Standard Default Color Space: NO
Preferred Timing Mode: NO
Display Type: RGB Color

Gamma: 2.20
Red x: 0.625
Red y: 0.340
Green x: 0.290
Green y: 0.605
Blue x: 0.150
Blue y: 0.070
White x: 0.283
White y: 0.297

Established Timings:
720x400@70
720x400@88
640x480@60
640x480@67
640x480@72
640x480@75
800x600@56
800x600@60
800x600@72
800x600@75
832x624@75
1024x768@87
1024x768@60
1024x768@70
1024x768@75
1152x870@75
1280x1024@75

Standard Timing #1:
Horizontal Active Pixels: 1920
Aspect Ratio: 4:3
(1440 active lines)
Refresh Rate: 75 Hz

Standard Timing #2:
Horizontal Active Pixels: 1800
Aspect Ratio: 4:3
(1350 active lines)
Refresh Rate: 85 Hz

Standard Timing #3:
Horizontal Active Pixels: 1600
Aspect Ratio: 4:3
(1200 active lines)
Refresh Rate: 85 Hz

Standard Timing #4:
Horizontal Active Pixels: 1600
Aspect Ratio: 4:3
(1200 active lines)
Refresh Rate: 75 Hz

Standard Timing #5:
Horizontal Active Pixels: 1280
Aspect Ratio: 5:4
(1024 active lines)
Refresh Rate: 85 Hz

Standard Timing #6:
Horizontal Active Pixels: 2048
Aspect Ratio: 4:3
(1536 active lines)
Refresh Rate: 75 Hz

Standard Timing #7:
Horizontal Active Pixels: 1024
Aspect Ratio: 4:3
(768 active lines)
Refresh Rate: 85 Hz

Standard Timing #8:
Horizontal Active Pixels: 800
Aspect Ratio: 4:3
(600 active lines)
Refresh Rate: 85 Hz

Detailed Timing (block #1):
Pixel Clock: 299.67 MHz
Horizontal Active: 1800 pixels
Horizontal Blanking: 688 pixels
Vertical Active: 1350 lines
Vertical Blanking: 67 lines
(Horizontal Frequency: 120.45 kHz)
(Vertical Frequency: 85.0Hz)
Horizontal Sync Offset: 144 pixels
Horizontal Sync Width: 200 pixels
Vertical Sync Offset: 1 lines
Vertical Sync Width: 3 lines
Horizontal Border: 0 pixels
Vertical Border: 0 lines
Horizontal Image Size: 393 mm
Vertical Image Size: 295 mm
Interlaced: NO
Image: Normal Display
Sync: Digital Separate
Bit 1: OFF
Bit 2: OFF

Monitor Range Limits (block #2):
Minimum Vertical Rate: 50 Hz
Maximum Vertical Rate: 160 Hz
Minimum Horizontal Rate: 30 kHz
Maximum Horizontal Rate: 121 kHz
Maximum Pixel Clock: 360 MHz
GTF Data: 00 0a 20 20 20 20 20 20

Monitor Name (block #3): NSH1157U

Monitor Serial Number (block #4): ##

EDID EDITOR V1. 36 (990907)
(C) Mitsubishi Electric 1995-1999

EDID DATA DUMP HEX

00	ff	ff	ff	ff	ff	ff	00
34	ac	f3	43	**	**	**	**
WW	YY	01	01	0e	28	1e	78
e9	04	88	a0	57	4a	9b	26
12	48	4c	ff	ff	80	d1	4f
c2	59	a9	59	a9	4f	81	99
e1	4f	61	59	45	59	0f	75
08	b0	72	46	43	50	90	c8
13	00	89	27	11	00	00	18
00	00	00	fd	00	32	a0	1e
79	24	00	0a	20	20	20	20
20	20	00	00	00	fc	00	4e
53	48	31	31	35	37	55	0a
20	20	20	20	00	00	00	ff
00	##	##	##	##	##	##	##
##	##	0a	20	20	20	00	SS

** : serial number 1
WW : manufacture week
YY : manufacture year
NN : serial number (ASCII)
SS : check sam

2.11 Default inspection

2.11.1 Default setting of switches

Confirm that the following switch is set as follows.

(1) Power switch: OFF

2.11.2 Default setting of OSD

Confirm that each OSD setting is as shown in the OSD display (section 3.7.3) table (user mode/factory mode).

If the setting class is an item for each timing, carry out for each adjustment timing.

* CENTER is the factory adjustment value called when the (-) (+) ADJUST buttons are pressed simultaneously in the normal mode.
Only CONTRAST will be set to MAX when the (-) (+) ADJUST buttons are pressed simultaneously in the normal mode.

2.11.3 Checking the labels

Confirm that the "SERVICEMAN WARNING", "rating label", "manufacturing date stamp", "SERIAL NO. label", and "set sub-No.", etc., are attached to the specified position, and have been checked.

2.11.4 Packaging

(1) There must be no remarkable contamination, tearing or scratches, etc.
(2) The model name must be accurately displayed.
(3) The SERIAL NO. must be attached. (Must be the same No. as the set.)
(4) The package must be accurately sealed.

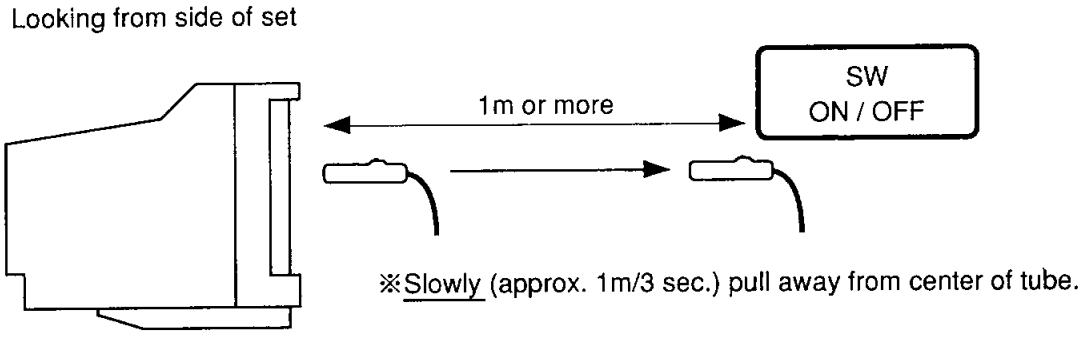
2.12 Degaussing with handy-demagnetizer

2.12.1 General precautions

(1) Carry this procedure out with the monitor power ON.
(2) When degaussing with handy-demagnetizer, the demagnetizer power must be turned ON and OFF at a position at least 1m away from CRT tube.
(3) Use a bar type demagnetizer instead of a ring type.
Carefully and slowly (1m/3 sec.) demagnetize the CRT tube and bezel side surface.
When separating the degaussing coil at the end, separate as slow as possible with the following procedure.
If separated quickly, stripes could remain at the picture corners.

2.12.2 How to hold and use the handy-demagnetizer

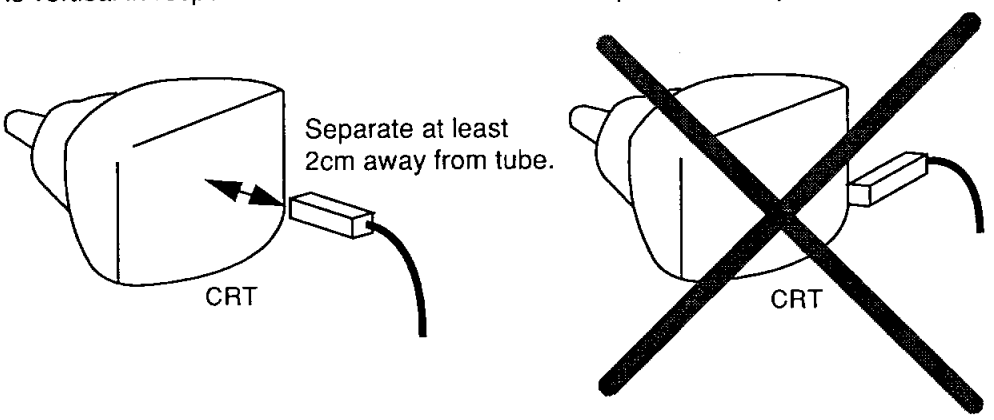
(1) Approach the demagnetizer as carefully and slowly (approx. 1m/3 sec.) as possible, and move around the bezel side periphery two to three times.
(2) Next, gradually (approx. 1m/3 sec.) move to the CRT tube side, and move around the CRT tube four to five times with the following procedure.
(3) Finally, leave the CRT tube as slowly (approx. 1m/3 sec.) as possible, and turn the handy-



<Holding the hand degaussing unit>

Face the hand degaussing unit so that the longitudinal direction is vertical in respect to the CRT.

Do not hold the hand degaussing unit so that the longitudinal direction is parallel in respect to the CRT.

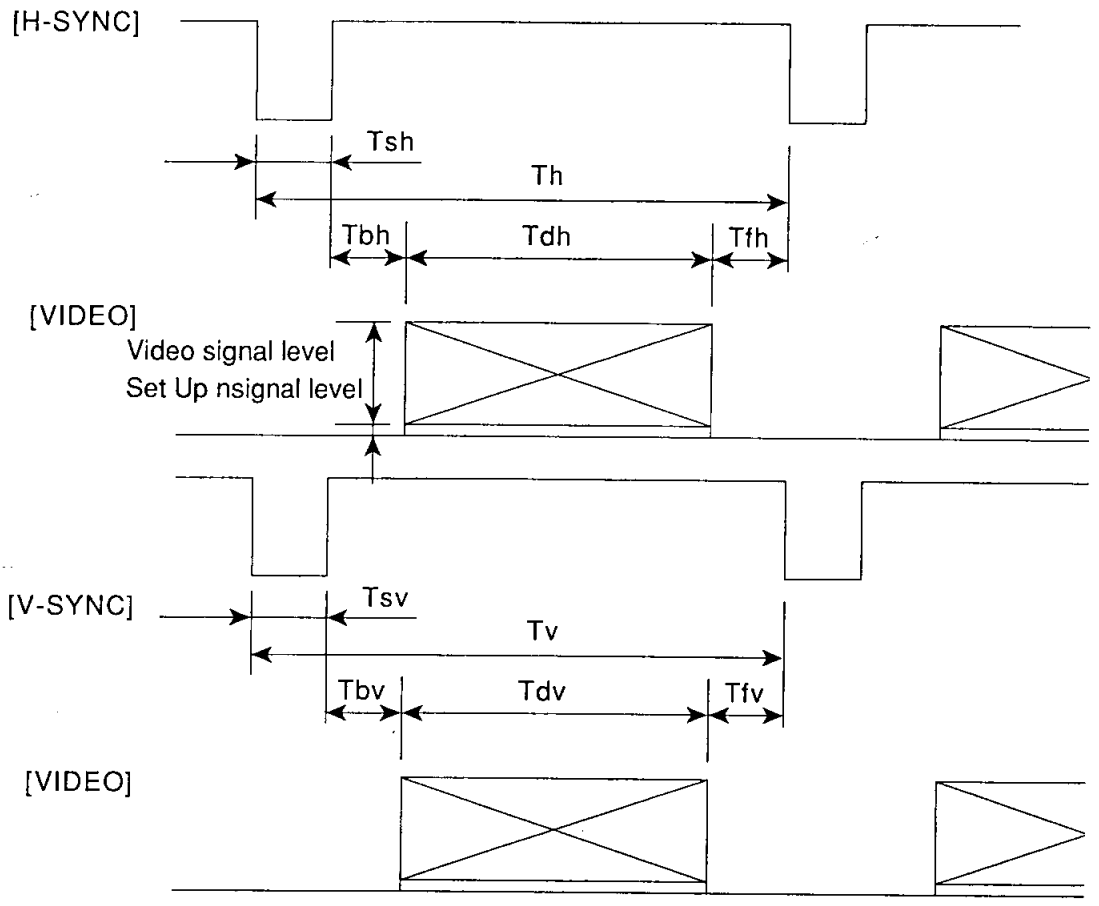


demagnetizer unit switch OFF at a position 1 to 1.5m away.

2.13 Caution

Do not input the user timing before factory adjustments.
(The automatic tracking of the FOCUS could be adversely affected.)

2.14 Timing chart



※Refer to after the next page for the preset timing details.

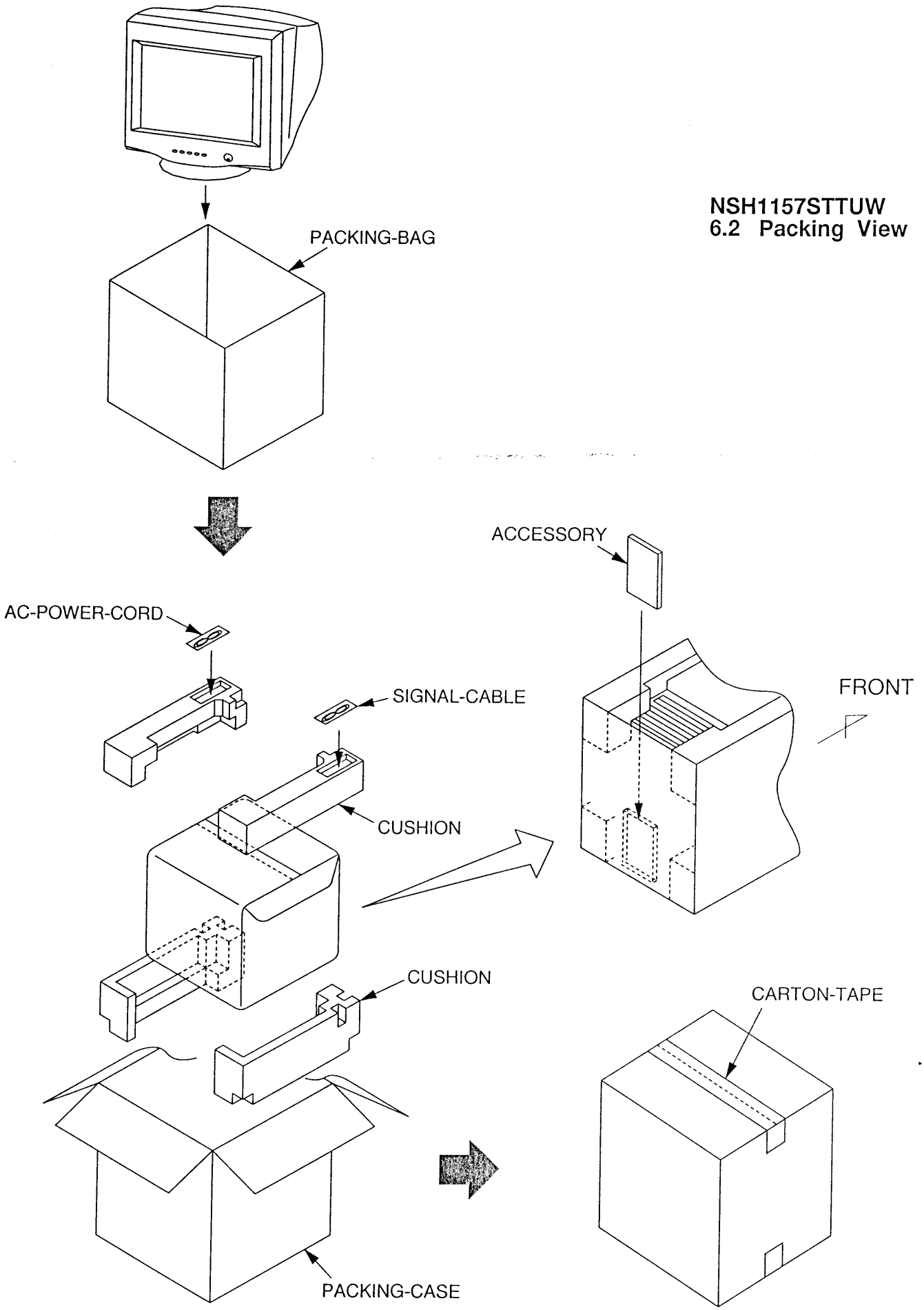
2.15 Adjustment timing

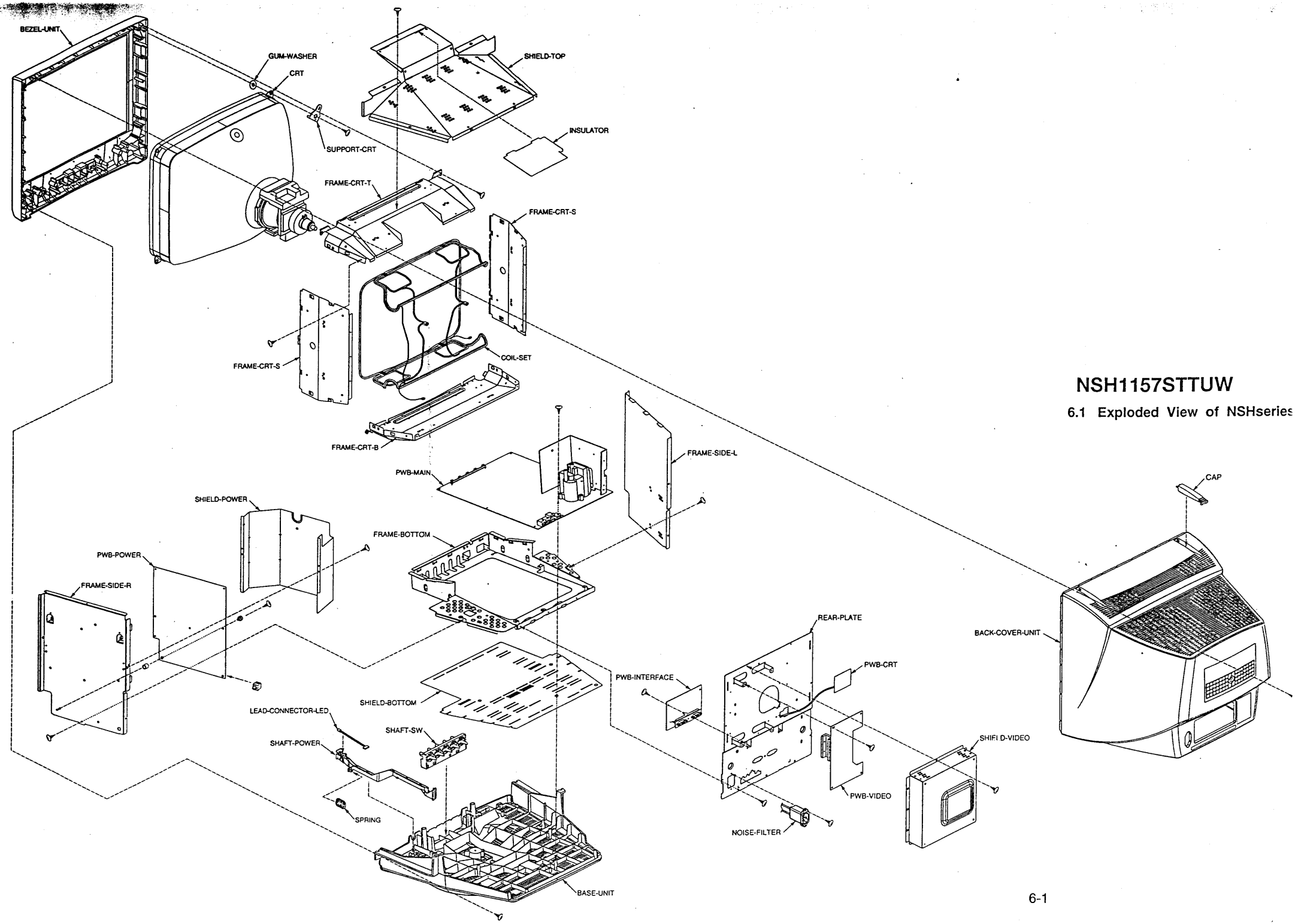
NO	Fh (kHz)	Clock (MHz)	Th (µSEC) (dot)	Tsh (µSEC) (dot)	Tfh (µSEC) (dot)	Tbh (µSEC) (dot)	Tdh (µSEC) (dot)	Fv (Hz)	Tv (mSEC) (line)	Tsv (mSEC) (line)	Tfv (mSEC) (line)	Tbv (mSEC) (line)	Tdv (mSEC) (line)	Hs	Vs	VIDEO level (V)	set up level (V)	Serra-tion		Remarks
Check 1	35		28.571	3.500	1.891	4.000	19.180	66.70	15.000	0.086	1.485	2.000	11.428	S/G		0.7	—	—		Check 1
Check 2	35		28.571	3.500	1.891	4.000	19.180	66.70	15.000	0.086	1.485	2.000	11.428	Com posite		0.7	—	1H		Check 2
Check 3	114.240	252.242	8.754	0.698	0.507	1.205	6.343	85.000	11.765	0.026	0.009	0.525	11.204	—	—	0.7	—	—		Check 3 GTF(1600*1280)85Hz
Check 4	106.250	229.500	9.412	0.837	0.279	1.325	6.972	85.000	11.765	0.028	0.009	0.433	11.294	+	—	0.7	—	—		Check 4 (1600*1200)85Hz
A	30		33.333	4.000	1.000	3.000	25.333	70.10	14.268	0.064	1.176	1.906	11.122	+	—	0.7	—	—		+B-L adjustment

NO	Fh (kHz)	Clock (MHz)	Th (SEC) (dot)	Tsh (SEC) (dot)	Tfh (SEC) (dot)	Tbh (SEC) (dot)	Tdh (SEC) (dot)	Utili-zation	H re-trace s+f+b	Fv (Hz)	Tv (mSEC) (line)	Tsv (mSEC) (line)	Tfv (mSEC) (line)	Tbv (mSEC) (line)	Tdv (mSEC) (line)	V re-trace	Hs	Vs	VIDEO level (V)	set up level (V)	Serra-tion	Group 1		Remarks
1	31.469	25.175	31.778 (800)	3.813 (96)	0.636 (16)	1.907 (48)	25.422 (640)	80.00	6.356	70.090	14.268 (449)	0.064 (2)	0.382 (12)	1.111 (35)	12.711 (400)	1.175	—	+	0.7	—	—			(640*400)70Hz
2	31.469	25.175	31.778 (800)	3.813 (96)	0.636 (16)	1.907 (48)	25.422 (640)	80.00	6.356	59.940	16.683 (525)	0.064 (2)	0.318 (10)	1.048 (33)	15.253 (480)	1.112	—	—	0.7	—	—	○0		VGA(640*480)60Hz
3	37.500	31.500	26.667 (840)	2.032 (64)	0.508 (16)	3.810 (120)	20.317 (640)	76.19	6.350	75.000	13.333 (500)	0.080 (3)	0.027 (1)	0.427 (16)	12.800 (480)	0.506	—	—	0.7	—	—			VESA(640*480)75Hz
4	43.269	36.000	23.111 (832)	1.556 (56)	1.556 (56)	2.222 (80)	17.778 (640)	76.92	5.334	85.008	11.764 (509)	0.069 (3)	0.023 (1)	0.578 (25)	11.093 (480)	0.647	—	—	0.7	—	—			VESA(640*480)85Hz
5	46.875	49.500	21.333 (1056)	1.616 (80)	0.323 (16)	3.232 (160)	16.162 (800)	75.76	5.171	75.000	13.333 (625)	0.064 (3)	0.021 (1)	0.448 (21)	12.800 (600)	0.512	+	+	0.7	—	—			VESA(800*600)75Hz
6	53.674	56.250	18.631 (1048)	1.138 (64)	0.569 (32)	2.702 (152)	14.222 (800)	76.34	4.409	85.061	11.756 (631)	0.056 (3)	0.019 (1)	0.503 (27)	11.179 (600)	0.559	+	+	0.7	—	—	○1		VESA(800*600)85Hz
7	60.023	78.750	16.660 (1312)	1.219 (96)	0.203 (16)	2.235 (176)	13.003 (1024)	78.05	3.657	75.029	13.328 (800)	0.050 (3)	0.017 (1)	0.466 (28)	12.795 (768)	0.516	+	+	0.7	—	—	▲9		VESA(1024*768)75Hz
8	68.677	94.500	14.561 (1376)	1.016 (96)	0.508 (48)	2.201 (208)	10.836 (1024)	74.42	3.725	84.997	11.765 (808)	0.044 (3)	0.015 (1)	0.524 (36)	11.183 (768)	0.568	+	+	0.7	—	—	○2		VESA(1024*768)85Hz
9	79.976	135.000	12.504 (1688)	1.067 (144)	0.119 (16)	1.837 (248)	9.481 (1280)	75.82	3.023	75.025	13.329 (1066)	0.038 (3)	0.013 (1)	0.475 (38)	12.804 (1024)	0.513	+	+	0.7	—	—	○3		VESA(1280*1024)75Hz
10	91.146	157.500	10.971 (1728)	1.016 (160)	0.406 (64)	1.422 (224)	8.127 (1280)	74.08	2.844	85.027	11.761 (1072)	0.033 (3)	0.011 (1)	0.483 (44)	11.235 (1024)	0.516	+	+	0.7	—	—	○4		VESA(1280*1024)85Hz
11	93.750	202.500	10.667 (2160)	0.948 (192)	0.316 (64)	1.501 (304)	7.901 (1600)	74.07	2.765	75.000	13.333 (1250)	0.032 (3)	0.011 (1)	0.491 (46)	12.800 (1200)	0.523	+	+	0.7	—	—	○5		VESA(1600*1200)75Hz
12	106.250	229.500	9.412 (2160)	0.837 (192)	0.279 (64)	1.325 (304)	6.972 (1600)	74.08	2.441	85.000	11.765 (1250)	0.028 (3)	0.009 (1)	0.433 (46)	11.294 (1200)	0.461	+	+	0.7	—	—	○6		VESA(1600*1200)85Hz
13	106.270	261.000	9.41 (2456)	0.828 (216)	0.368 (96)	1.349 (352)	6.866 (1792)	72.96	2.545	74.997	13.334 (1417)	0.028 (3)	0.009 (1)	0.649 (69)	12.647 (1344)	0.677	+	+	0.7	—	—			VESA(1792*1344)75Hz
14	112.500	288.000	8.889 (2560)	0.778 (224)	0.444 (128)	1.222 (352)	6.444 (1856)	72.49	2.444	75.000	13.333 (1500)	0.027 (3)	0.009 (1)	0.924 (104)	12.373 (1392)	0.951	+	+	0.7	—	—			VESA(1856*1392)75Hz
15	112.500	297.000	8.889 (2640)	0.754 (224)	0.485 (144)	1.185 (352)	6.465 (1920)	72.73	2.424	75.000	13.333 (1500)	0.027 (3)	0.009 (1)	0.498 (56)	12.800 (1440)	0.525	+	+	0.7	—	—	○7		VESA(1920*1440)75Hz
16	35.00	30.240	28.571 (864)	2.116 (64)	2.116 (64)	3.175 (96)	21.164 (640)	74.08	7.407	66.67	15.000 (525)	0.086 (3)	0.086 (3)	1.114 (39)	13.714 (480)	1.2	—	—	0.7	—	—			APPLE13(640*480)
17	49.710	57.270	20.115 (1152)	1.118 (64)	0.559 (32)	3.910 (224)	14.528 (832)	72.22	5.587	74.530	13.417 (667)	0.060 (3)	0.020 (1)	0.785 (39)	12.552 (624)	0.845	—	—	0.7	—	—			APPLE16(832*624)
18	60.240	80.000	16.600 (1328)	1.200 (96)	0.400 (32)	2.200 (176)	12.800 (1024)	77.11	3.800	74.930	13.346 (804)	0.050 (3)	0.049 (3)	0.498 (30)	12.749 (768)	0.548	—	—	0.7	—	—			APPLE19(1024*768)
19	68.680	100.000	14.560 (1456)	1.280 (128)	0.320 (32)	1.440 (144)	11.520 (1152)	79.12	3.040	75.060	13.322 (915)	0.044 (3)	0.043 (3)	0.568 (39)	12.667 (870)	0.612	—	—	0.7	—	—			APPLE21(1152*870)
20	100.200	219.638	9.980 (2192)	0.801 (176)	0.546 (120)	1.348 (296)	7.285 (1600)	73.00	2.695	75.000	13.333 (1336)	0.03 (3)	0.01 (1)	0.519 (52)	12.774 (1280)	0.549	—	—	0.7	—	—			GTF(1600*1280)75Hz
21	107.200	234.982	9.328 (2192)	0.749 (176)	0.511 (120)	1.260 (296)	6.809 (1600)	73.00	2.520	80.000	12.5 (1340)	0.028 (3)	0.009 (1)	0.522 (56)	11.94 (1280)	0.55	—	—	0.7	—	—			GTF(1600*1280)80Hz
22	114.240	252.242	8.754 (2208)	0.698 (176)	0.507 (128)	1.205 (304)	6.343 (1600)	72.46	2.410	85.000	11.765 (1344)	0.026 (3)	0.009 (1)	0.525 (60)	11.204 (1280)	0.551	—	—	0.7	—	—			GTF(1600*1280)85Hz
23	105.675	261.229	9.463 (2472)	0.766 (200)	0.521 (136)	1.286 (336)	6.891 (1800)	72.82	2.573	75.000	13.333 (1409)	0.028 (3)	0.009 (1)	0.52 (55)	12.775 (1350)	0.548	—	—	0.7	—	—			GTF(1800*1350)75Hz
24	113.040	279.435	8.846 (2472)	0.716 (200)	0.487 (136)	1.202 (336)	6.442 (1800)	72.82	2.405	80.000	12.5 (1413)	0.027 (3)	0.009 (1)	0.522 (59)	11.943 (1350)	0.549	—	—	0.7	—	—			GTF(1800*1350)80Hz
25	120.445	299.667	8.303 (2488)	0.667 (200)	0.481 (144)	1.148 (344)	6.007 (1800)	72.35	2.296	85.000	11.765 (1417)	0.025 (3)	0.008 (1)	0.523 (63)	11.208 (1350)	0.548	—	—	0.7	—	—	○8		GTF(1800*1350)85Hz
26	112.725	278.656	8.871 (2472)	0.718 (200)	0.488 (136)	1.206 (336)	6.460 (1800)	72.82	2.412	75.000	13.333 (1503)	0.027 (3)	0.009 (1)	0.523 (59)	12.774 (1440)	0.55	—	—	0.7	—	—			GTF(1800*1440)75Hz
27	120.560	299.953	8.295 (2488)	0.667 (200)	0.480 (144)	1.147 (344)	6.001 (1800)	72.34	2.294	80.000	12.5 (1507)	0.025 (3)	0.008 (1)	0.523 (63)	11.944 (1440)	0.548	—	—	0.7	—	—			GTF(1800*1440)80Hz
28	80.530	105.656	12.418 (1312)	1.060 (112)	0.303 (32)	1.636 (144)	9.692 (1024)	78.05	2.726	100.000	10.0 (805)	0.037 (3)	0.012 (1)	0.410 (33)	9.537 (768)	0.463	—	—	0.7	—	—			ELSA(1024*768)100Hz

Mark ○ : Factory adjustment
Mark □ : Factory adjustment [Though they are presets, it does not apply to the specification of the picture distortion. The sync. signals are reference to the above. (It is possible to reset with the above timings.))
Mark ▲ : Initial data [So long as initial data, the sync. signals are reference to Hs: + and Vs: -. However, it is necessary to adjust only the H-SIZE, H-PHASE, DBF-H-AMP, DBF-H-PHASE in factory mode.
The numbers after the marks are the number of preset.

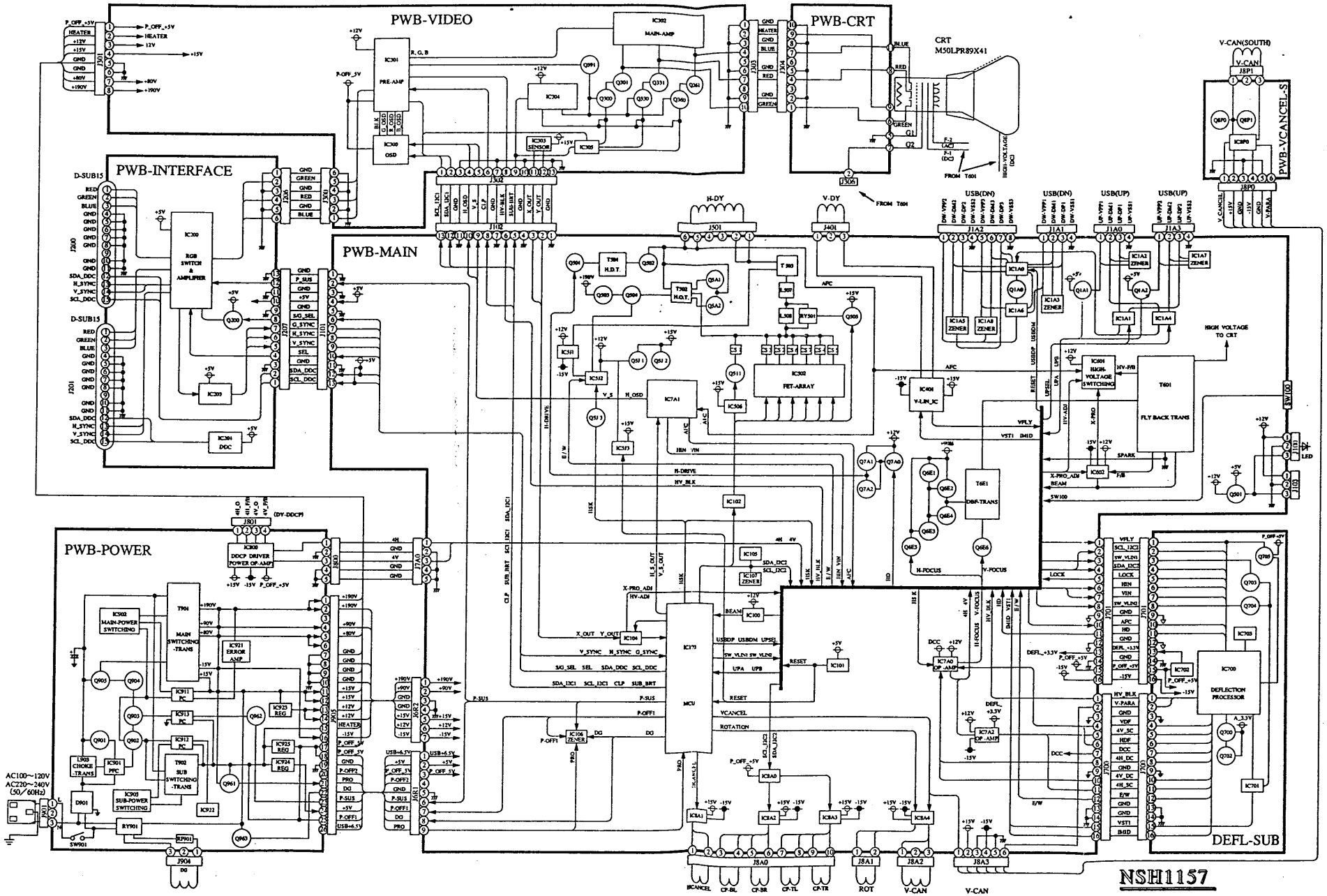
NSH1157STTUW
6.2 Packing View

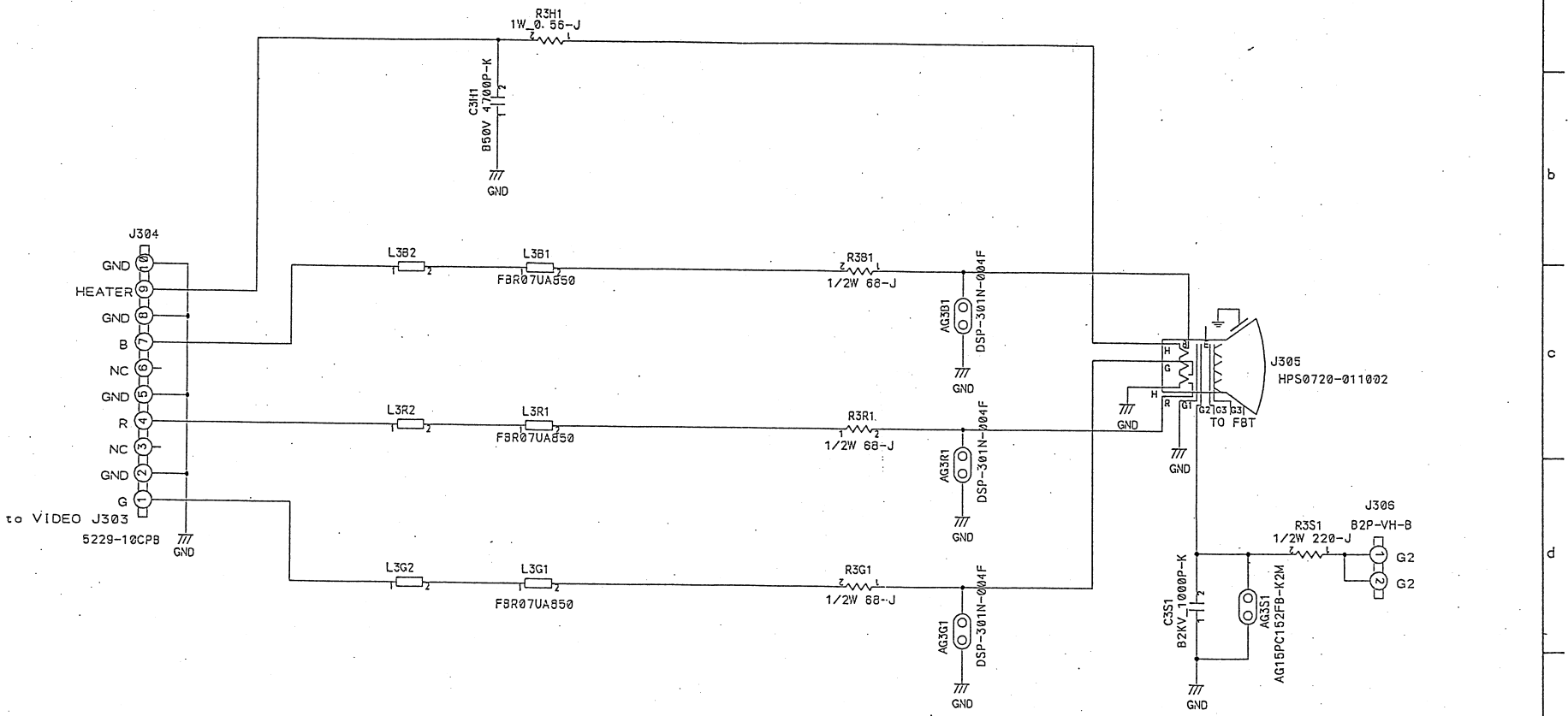




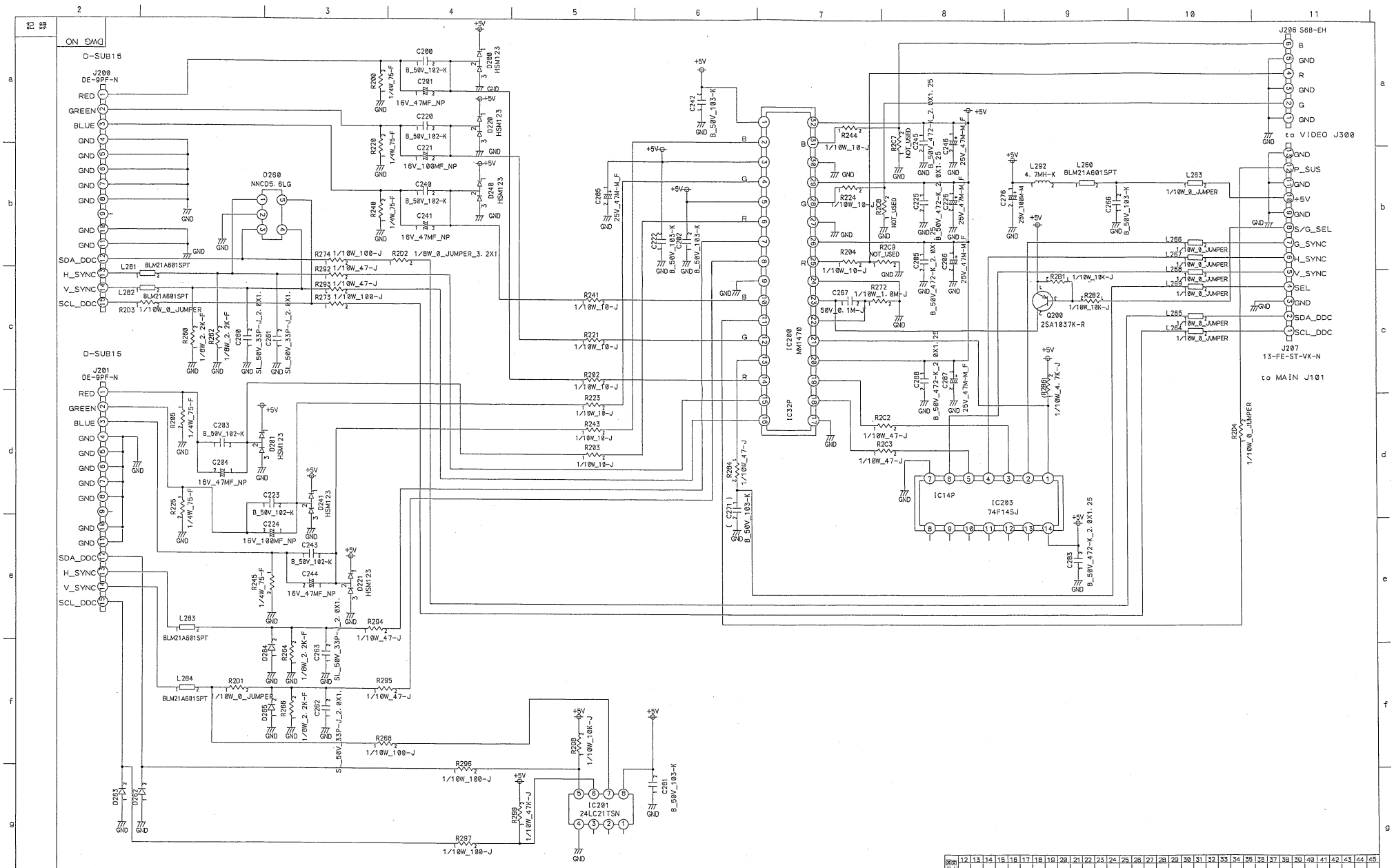
NSH1157STTUW

6.1 Exploded View of NSHseries


PWB-VIDEO
PWB-CRT
PWB-INTERFACE
PWB-MAIN
PWB-POWER
DEFL-SUB
PWB-VCANCEL-S
CRT
M50LPR89X41
V-CAN(SOUTH)
AC100~120V
AC220~240V
(50/60Hz)
NSH1157
12/3/99
BLOCK-DIAGRAM



改定 CHANGE		控		MITUBISHI ELECTRIC CORPORATION		TITLE SCHEMATIC DIAGRAM	
		出図用		NAGASAKI WORKS		CRT	
		外注用		DIM IN mm	作成日付 DATE	検認 APPROVED	CP 980C163
		計画	1	尺度 SCALE	作成 DRAWN		REV 1/1
				NTS	照査 CHECKED		
					設計 DESIGNED		



*200~

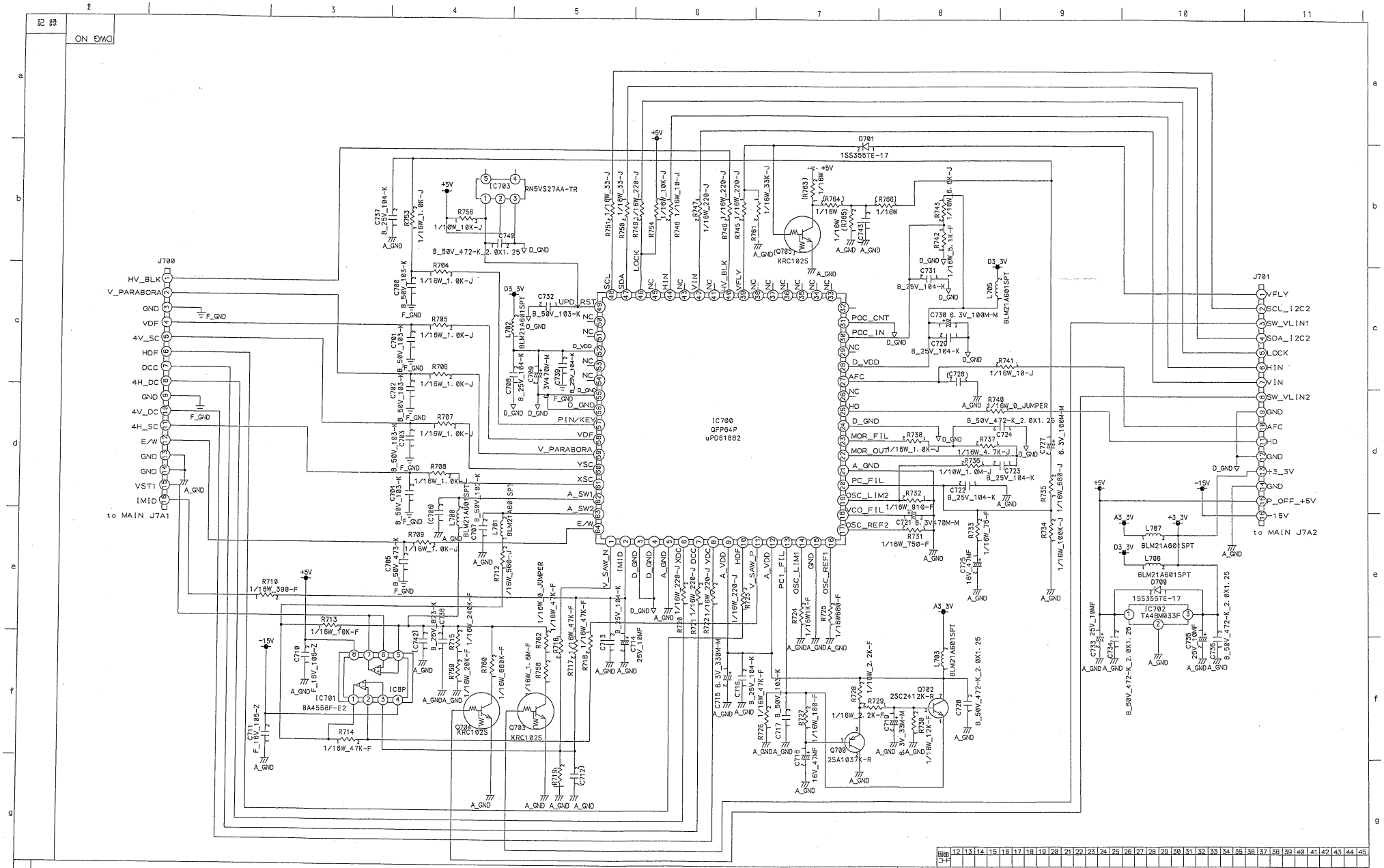
設		第3角法 3RD ANGLE PROJECTION	DIM IN mm	尺度 SCALE	作成日付 DATE
出図用					
外注用					
計画	1	MITUBISHI ELECTRIC CORPORATION NAGASAKI WORKS			
		作成 DRAWN		検認 APPROVED	
		照査 CHECKED			
		設計 DESIGNED			

TITLE SCHEMATIC DIAGRAM
INTERFACE

CP

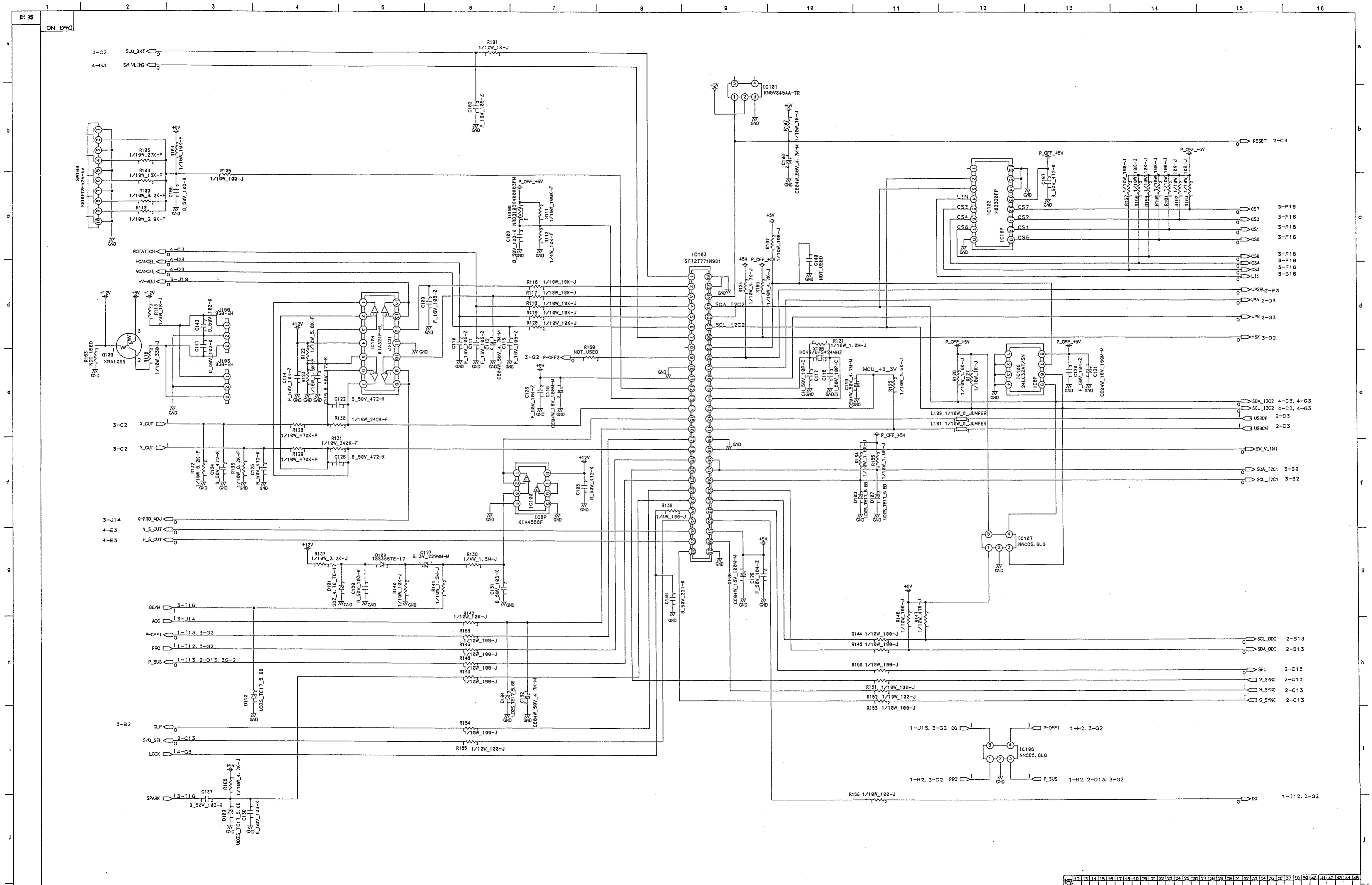
REV 1/1

CP980C164



控		第3角法 3RD ANGLE PROJECTION	DIM IN mm	尺度 SCALE 作成日付 DATE
出図用		MITUBISHI ELECTRIC CORPORATION NAGASAKI WORKS		TITLE SCHEMATIC DIAGRAM DEFL-SUB
外注用		作成 DRAWN	検認 APPROVED	
計画	1	照査 CHECKED		REV 1/1
		設計 DESIGNED		

CP980C165



*100~

CHANGE

MITSUBISHI ELECTRIC CORPORATION
NAGASAKI WORKS

3RD ANGLE PROJECTION

DIM IN mm

尺度 SCALE

作成日付 DATE

DRAWN

CHECKED

DESIGNED

APPROVED

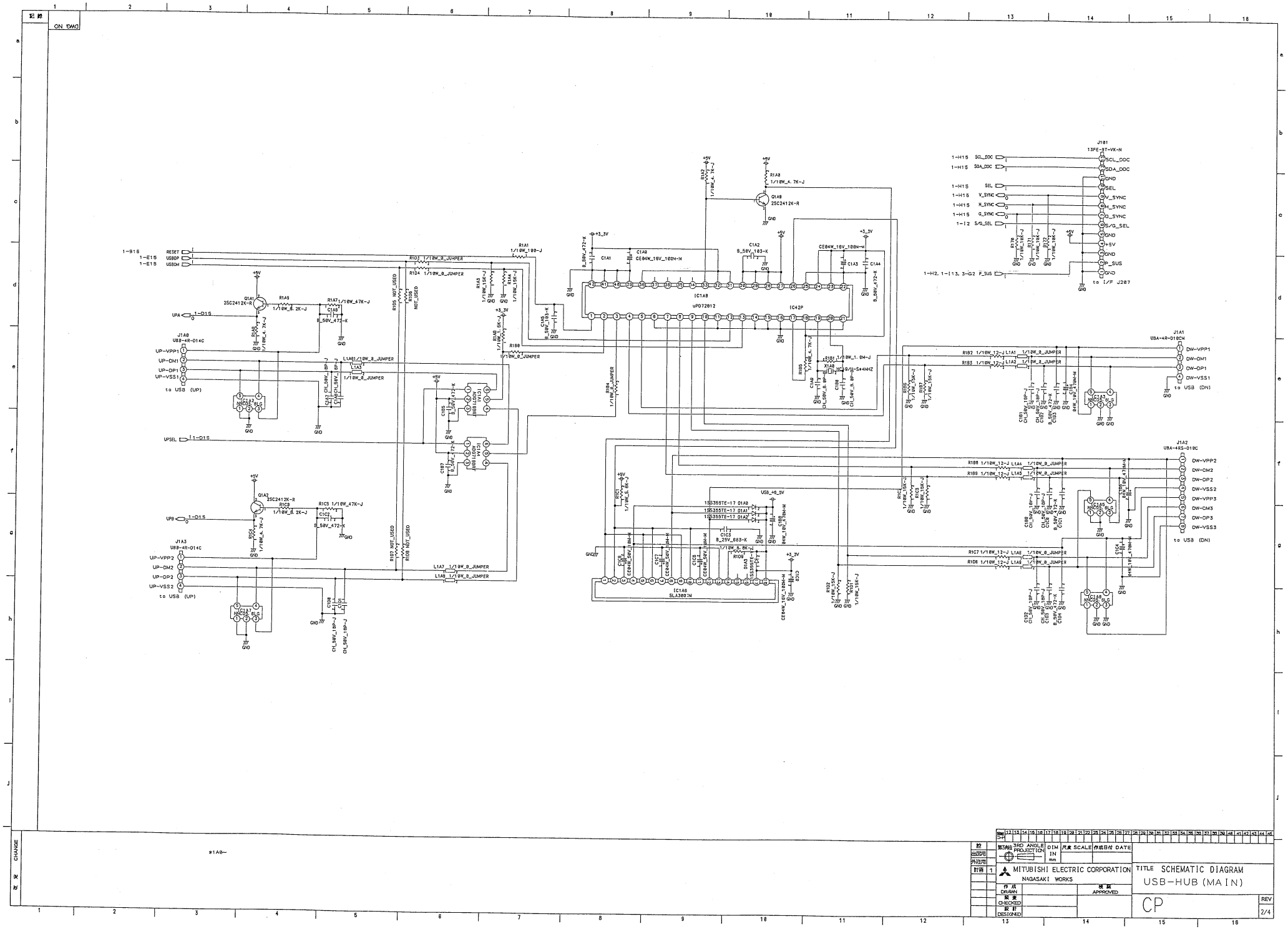
TITLE SCHEMATIC DIAGRAM
CONTROL (MAIN)

CP

REV

1/4

CP980B-297



CHANGE

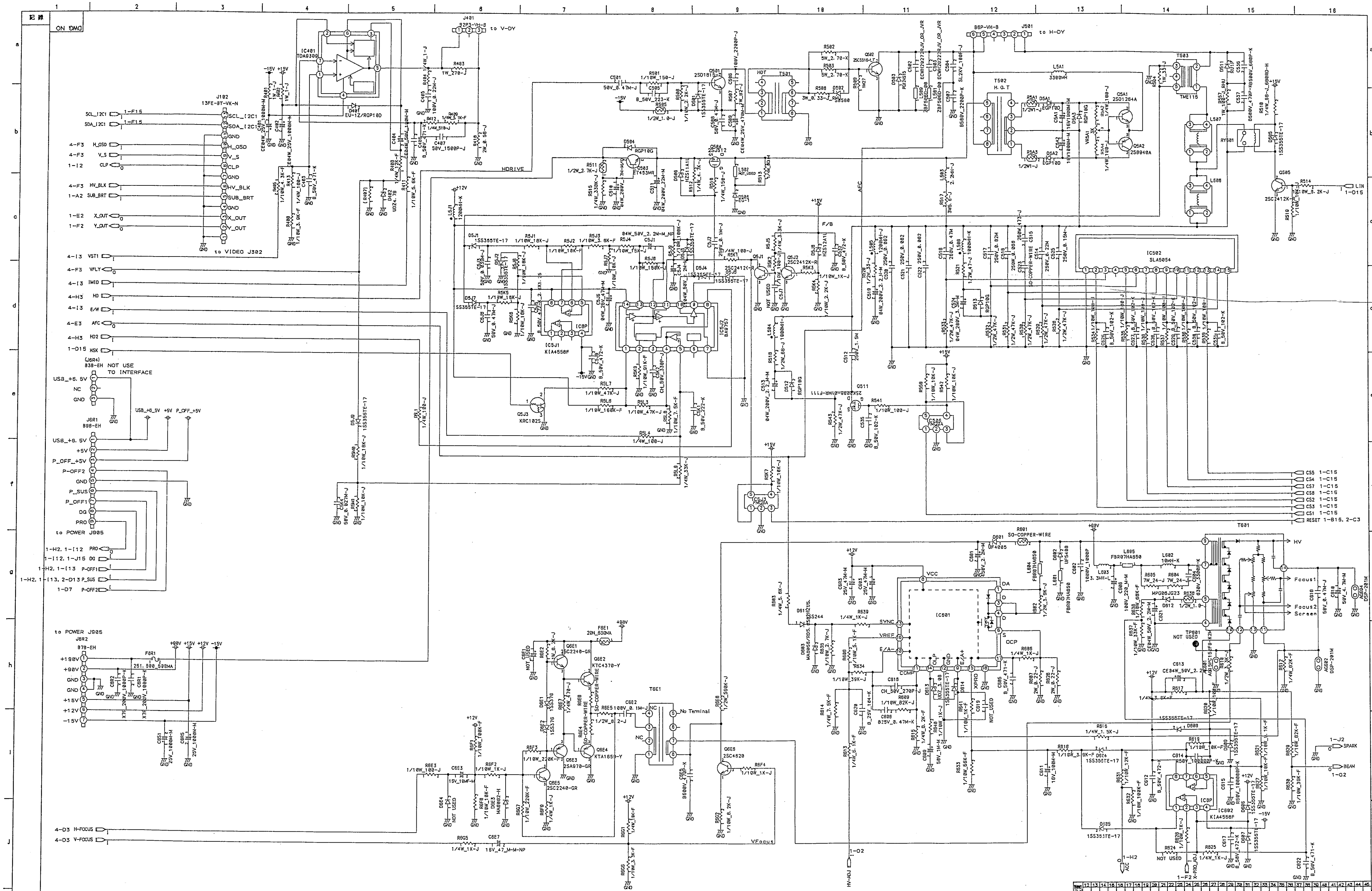
第3角法 3RD ANGLE PROJECTION	DIM IN mm
尺度 SCALE	作成日付 DATE
MITSUBISHI ELECTRIC CORPORATION NAGASAKI WORKS	
作成 DRAWN	承認 APPROVED
照査 CHECKED	
設計 DESIGNED	

TITLE SCHEMATIC DIAGRAM
USB-HUB (MAIN)

CP

REV 2/4

CP980B-297



REF. No.	CIRCUIT
*4**	V-DEFLECTION
*5**	H-DEFLECTION
5A, *5B*	H-POSITION
5F	TCO
5J, *5K*	+B CONTROL
5P, *5R*	CONTROL
5S, *5T*	CONTROL

REF. No.	CIRCUIT
*6**	HV
6E, *6F*	DBF
6R, *6S*	POWER (REG)

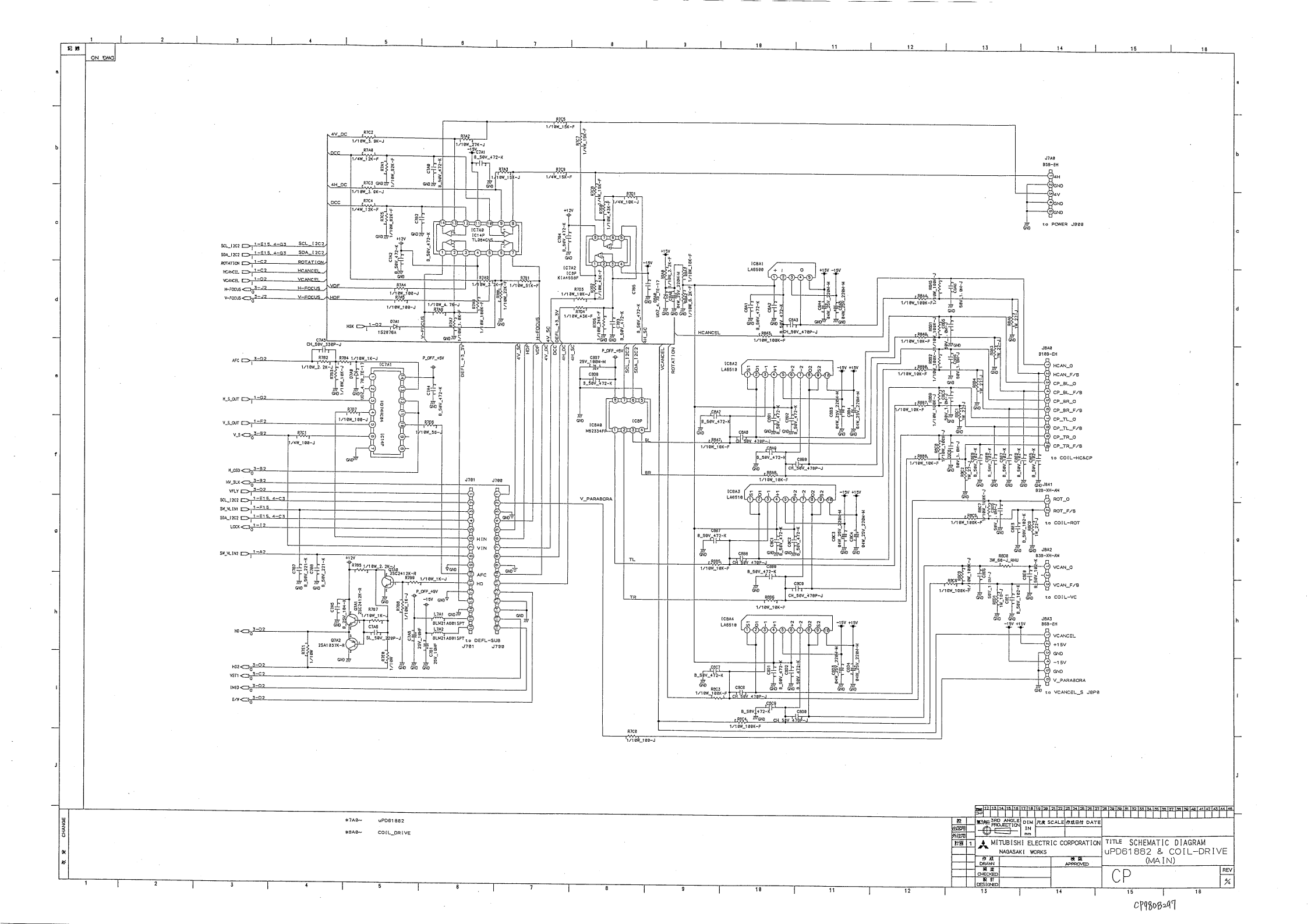
MITUBISHI ELECTRIC CORPORATION
NAGASAKI WORKS

TITLE SCHEMATIC DIAGRAM
DEFL (MAIN)

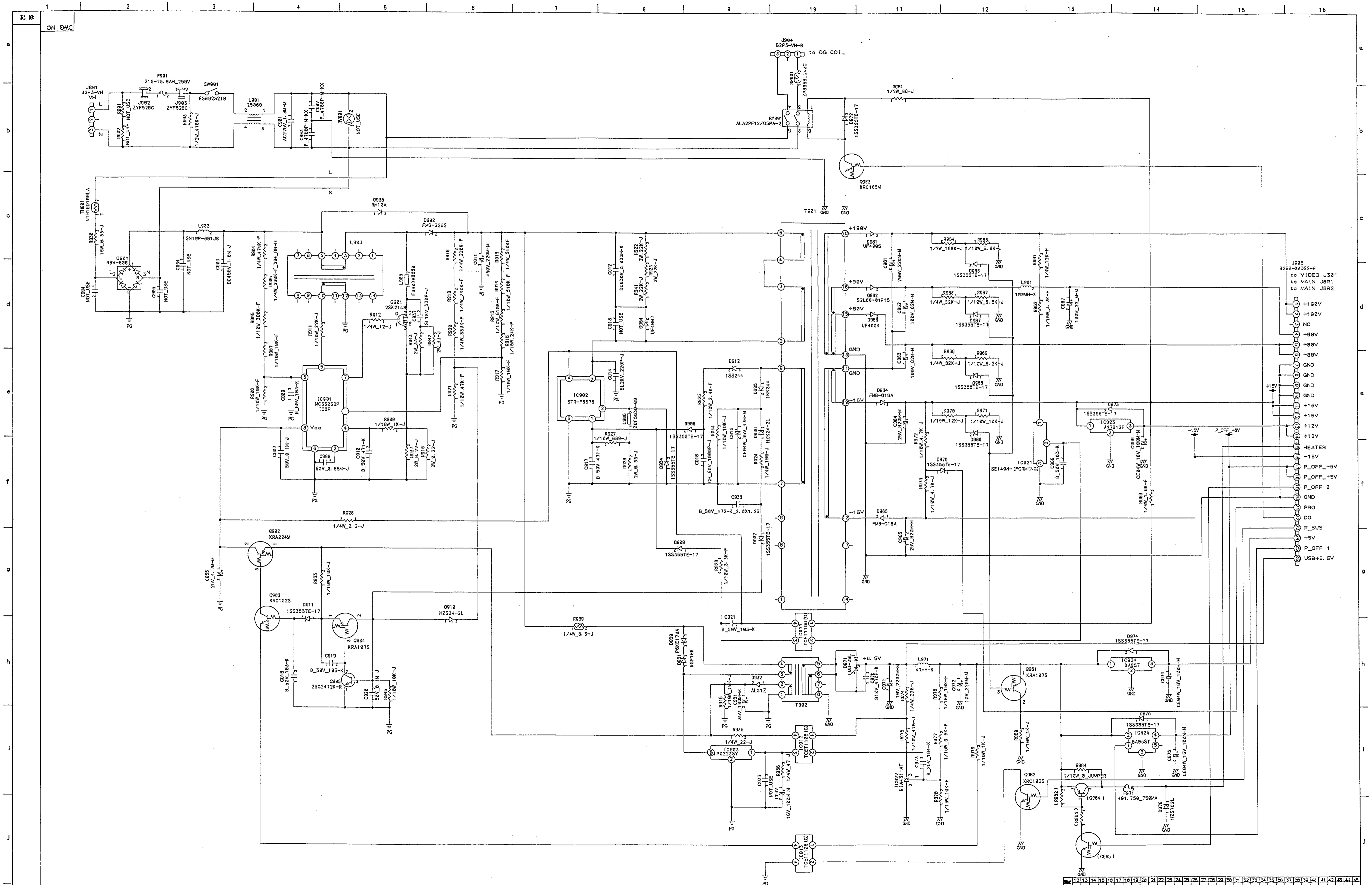
CP

REV 3/4

CP980B297


*7A8~ uPD61882
*8A8~ COIL_DRIVE
TITLE SCHEMATIC DIAGRAM
uPD61882 & COIL-DRIVE
(MAIN)
MITUBISHI ELECTRIC CORPORATION
NAGASAKI WORKS
CP
to PCWER J800
to COIL-HCACP
to COIL-ROT
to COIL-VC
to VCANCEL_S J8P8
to DEFL-SUB J701 J700

CP980B247



CHANGE

*900~ POWER

第3角法 3RD ANGLE PROJECTION | DIM IN mm | 尺度 SCALE | 作成日付 DATE 1999-6-17

MITUBISHI ELECTRIC CORPORATION
NAGASAKI WORKS

作成 DRAWN
調査 CHECKED
設計 DESIGNED
検認 APPROVED

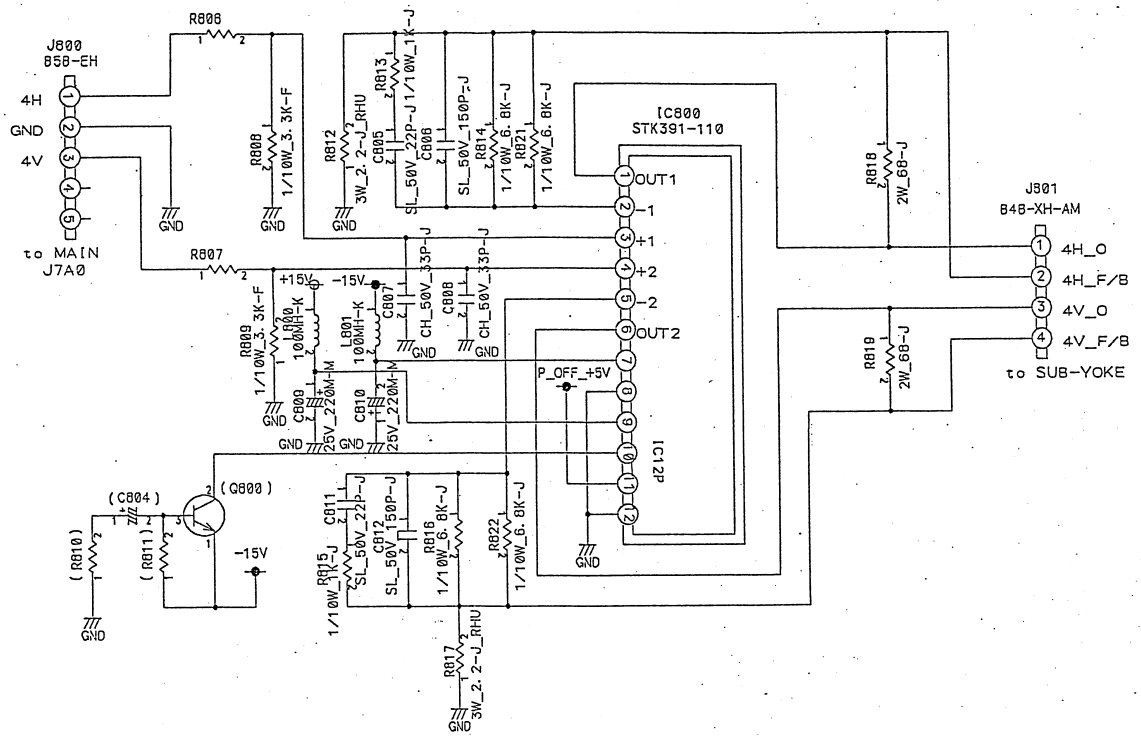
TITLE SCHEMATIC DIAGRAM
POWER

CP

REV 1/2

Ver. 0.1

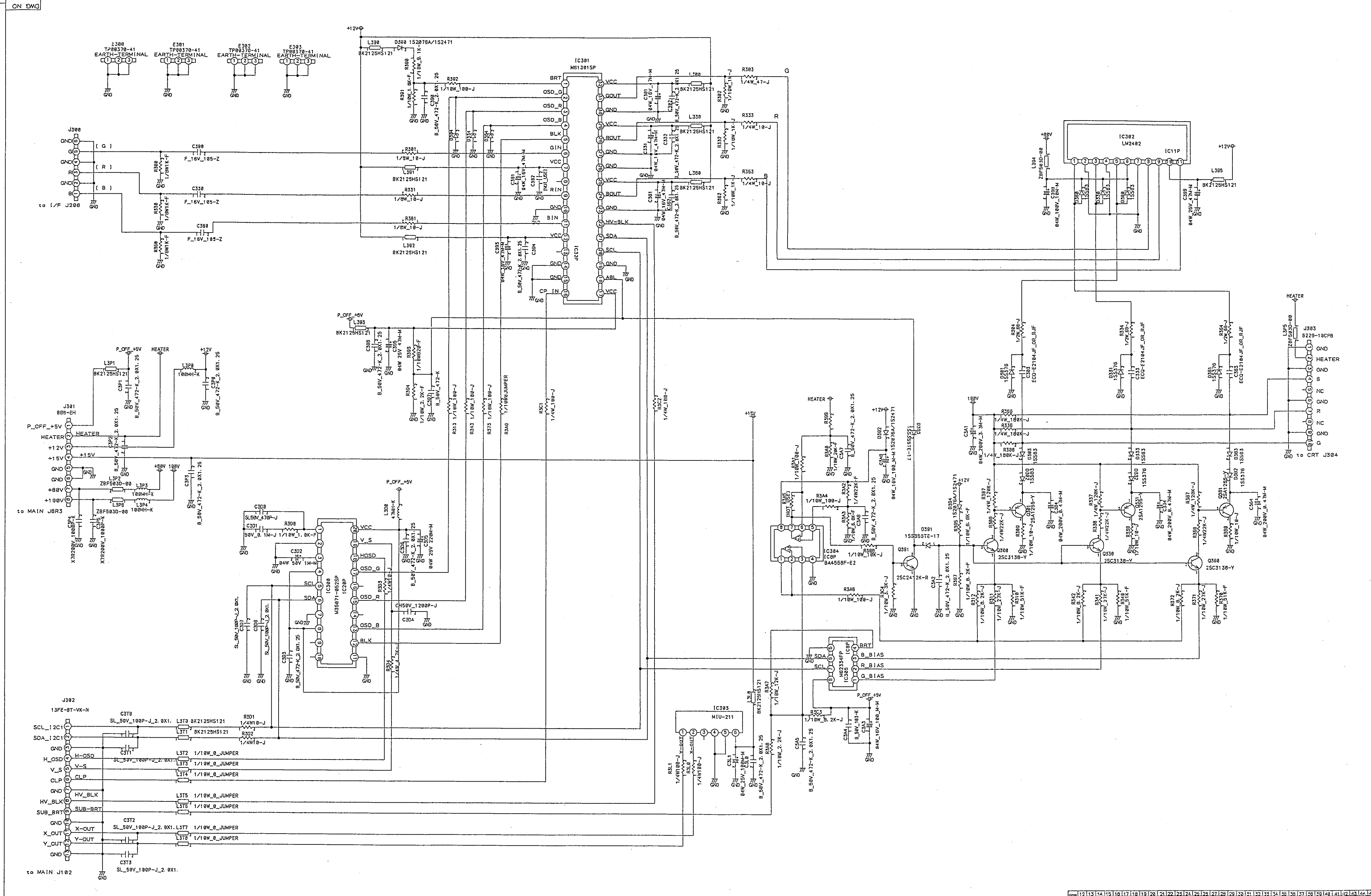
CP980B298



改定 CHANGE	*800~ DDCP	控 / 出図用 / 外注用 / 計画 1	DIM IN mm	作成日付 DATE	校認 APPROVED
			尺度 SCALE : NTS	作成 DRAWN M. Kobayashi	
				照査 CHECKED	
				設計 DESIGNED	

MITUBISHI ELECTRIC CORPORATION
NAGASAKI WORKS

TITLE SCHEMATIC DIAGRAM
DDCP (POWER)
CP 980B298
REV 2/2



Ref NO.	CIRCUIT	Ref NO.	CIRCUIT
*300～*329	GREEN	*3L*	EARTH
*330～*359	RED	*3P*	POWER
*360～*389	BLUE	*3T*	NOISE
30～*3F*	OSD		

3RD ANGLE PROJECTION

DIM IN mm

SCALE

DATE 99-6-16

MITSUBISHI ELECTRIC CORPORATION

NAGASAKI WORKS

DRAWN 山中

CHECKED

DESIGNED

APPROVED

TITLE SCHEMATIC DIAGRAM

VIDEO

CP

REV

/1

CP980B-99

RECOMMENDED SERVICE PARTS LIST

MODEL NO. : ELECTRON22BLUE (NSH1157U-LC) LaCie

ITEM	SYMBOL NO	DESCRIPTION/SPECIFICATION				PART NO.
1		AC-POWER-CORD		PM-1461C	(MT)	CP242C09901
2		AC-POWER-CORD			(MT)	CP242C22901
3		SIGNAL-CABEL	SC-B104			CP242C28603
4		CAP	ABS 500	NSH1157U-LC	(MI)	CP702C00805
5		CAP	ABS 500	NSH1157U-LC	(MI)	CP702C00806
6		BEZEL-UNIT	CP700A188-7	NSH1157U-LC	(ME)	CP720B08908
7		BACK-COVER-UNIT	CP700A189-7	NSH1157U-LC	(ME)	CP721B04808
8		BASE-UNIT	CP700A230-4	NSH1157U-LC	(ME)	CP722B02104
9		RATING-LABEL	YUPO 0.11	NSH1157U-LC		CP775C31302
10		PACKING-CASE		NUB1107U-LC		CP802C23102
11		LABEL-USE	POLYESTER TACK0.1	NSH1157U-LC		CP850C39905
12	CRT	M51LRY22X	CT251B022-2	ITC		0381F02Z
1	R 200	R-METAL-S	1/4W 75-F	750RN-H		CP103P06202
2	R 220	R-METAL-S	1/4W 75-F	750RN-H		CP103P06202
3	R 240	R-METAL-S	1/4W 75-F	750RN-H		CP103P06202
4	R 963	R-METAL-S	1/4W 1.8K-F	182 RN-H		CP103P06505
5	R 617	R-METAL-S	1/4W 3.6K-F	362 RN-H		CP103P06602
6	R 408	R-METAL-S	1/4W 3.9K-F	392 RN-H	(DH)	CP103P06603
7	R 409	R-METAL-S	1/4W 5.1K-F	512 RN-H		CP103P06606
8	R 613	R-METAL-S	1/4W 5.1K-F	512 RN-H		CP103P06606
9	R 614	R-METAL-S	1/4W 7.5K-F			CP103P06700
10	R 615	R-METAL-S	1/4W 8.2K-F	822 RN-H		CP103P06701
11	R 112	R-METAL-S	1/4W 10K-F	103 RN-H		CP103P06703
12	R 6G1	R-METAL-S	1/4W 10K-F	103 RN-H		CP103P06703
13	R 7A0	R-METAL-S	1/4W 12K-F 123 RN-H			CP103P06705
14	R 7C4	R-METAL-S	1/4W 12K-F 123 RN-H			CP103P06705
15	R 961	R-METAL-S	1/4W 12K-F 123 RN-H			CP103P06705
16	R 7C7	R-METAL-S	1/4W 15K-F	153 RN-H		CP103P06707
17	R 7C8	R-METAL-S	1/4W 15K-F	153 RN-H		CP103P06707
18	R 7C9	R-METAL-S	1/4W 15K-F	153 RN-H		CP103P06707
19	R 3A2	R-METAL-S	1/4W 22K-F 223RN-H			CP103P06801
20	R 612	R-METAL-S	1/4W 82K-F	823 RN-H		CP103P06905
21	R 918	R-METAL-S	1/4W 220K-F 224 RN-H			CP103P07009
22	R 919	R-METAL-S	1/4W 240K-F	244 RN-H		CP103P07100
23	R 920	R-METAL-S	1/4W 330K-F			CP103P07103
24	R 905	R-METAL-S	1/4W 390K-F 394 RN-H			CP103P07105
25	R 904	R-METAL-S	1/4W 470K-F	474 RN-H		CP103P07107
26	R 913	R-METAL-S	1/4W 510KF			CP103P07108
27	R 5K9	R-CARBON-CHIP	1/10W 91K-F			CP103P11008
28	R 3D0	R-CARBON-CHIP	1/10W 1.0K-F			CP103P11208
29	R 641	R-CARBON-CHIP	1/10W 1.0K-F			CP103P11208
30	R 7A7	R-CARBON-CHIP	1/10W 1.0K-F			CP103P11208
31	R 123	R-CARBON-CHIP	1/10W 1.5K-F			CP103P11300
32	R 393	R-CARBON-CHIP	1/10W 1.5K-F			CP103P11300
33	R 391	R-CARBON-CHIP	1/10W 1.8K-F			CP103P11301
34	R 394	R-CARBON-CHIP	1/10W 2.2K-F			CP103P11302
35	R 6G6	R-CARBON-CHIP	1/10W 2.2K-F			CP103P11302
36	R 7A9	R-CARBON-CHIP	1/10W 2.2K-F			CP103P11302
37	R 8A0	R-CARBON-CHIP	1/10W 2.2K-F			CP103P11302
38	R 6G2	R-CARBON-CHIP	1/10W 2.7K-F			CP103P11303

39	R 808	R-CARBON-CHIP	1/10W 3.3K-F	CP103P11304
40	R 809	R-CARBON-CHIP	1/10W 3.3K-F	CP103P11304
41	R 929	R-CARBON-CHIP	1/10W 3.3K-F	CP103P11304
42	R 110	R-CARBON-CHIP	1/10W 3.9K-F	CP103P11305
43	R 406	R-CARBON-CHIP	1/10W 3.9K-F	CP103P11305
44	R 618	R-CARBON-CHIP	1/10W 3.9K-F	CP103P11305
45	R 962	R-CARBON-CHIP	1/10W 4.7K-F	CP103P11306
46	R 122	R-CARBON-CHIP	1/10W 5.6K-F	CP103P11307
47	R 411	R-CARBON-CHIP	1/10W 5.6K-F	CP103P11307
48	R 3A3	R-CARBON-CHIP	1/10W 6.8K-F	CP103P11308
49	R 395	R-CARBON-CHIP	1/10W 6.8K-F	CP103P11308
50	R 977	R-CARBON-CHIP	1/10W 6.8K-F	CP103P11308
51	R 132	R-CARBON-CHIP	1/10W 8.2K-F	CP103P11309
52	R 133	R-CARBON-CHIP	1/10W 8.2K-F	CP103P11309
53	R 397	R-CARBON-CHIP	1/10W 8.2K-F	CP103P11309
54	R 6F8	R-CARBON-CHIP	1/10W 8.2K-F	CP103P11309
55	R 104	R-CARBON-CHIP	1/10W 10K-F	CP103P11400
56	R 5J2	R-CARBON-CHIP	1/10W 10K-F	CP103P11400
57	R 5M1	R-CARBON-CHIP	1/10W 10K-F	CP103P11400
58	R 619	R-CARBON-CHIP	1/10W 10K-F	CP103P11400
59	R 620	R-CARBON-CHIP	1/10W 10K-F	CP103P11400
60	R 627	R-CARBON-CHIP	1/10W 10K-F	CP103P11400
61	R 8A7	R-CARBON-CHIP	1/10W 10K-F	CP103P11400
62	R 8A8	R-CARBON-CHIP	1/10W 10K-F	CP103P11400
63	R 8A9	R-CARBON-CHIP	1/10W 10K-F	CP103P11400
64	R 8B0	R-CARBON-CHIP	1/10W 10K-F	CP103P11400
65	R 8B5	R-CARBON-CHIP	1/10W 10K-F	CP103P11400
66	R 8B6	R-CARBON-CHIP	1/10W 10K-F	CP103P11400
67	R 8B7	R-CARBON-CHIP	1/10W 10K-F	CP103P11400
68	R 8B8	R-CARBON-CHIP	1/10W 10K-F	CP103P11400
69	R 907	R-CARBON-CHIP	1/10W 10K-F	CP103P11400
70	R 908	R-CARBON-CHIP	1/10W 10K-F	CP103P11400
71	R 917	R-CARBON-CHIP	1/10W 10K-F	CP103P11400
72	R 976	R-CARBON-CHIP	1/10W 10K-F	CP103P11400
73	R 978	R-CARBON-CHIP	1/10W 10K-F	CP103P11400
74	R 631	R-CARBON-CHIP	1/10W 12K-F	CP103P11401
75	R 108	R-CARBON-CHIP	1/10W 15K-F	CP103P11402
76	R 7C6	R-CARBON-CHIP	1/10W 15K-F	CP103P11402
77	R 8A1	R-CARBON-CHIP	1/10W 18K-F	CP103P11403
78	R 399	R-CARBON-CHIP	1/10W 22K-F	CP103P11404
79	R 7B0	R-CARBON-CHIP	1/10W 22K-F	CP103P11404
80	R 103	R-CARBON-CHIP	1/10W 27K-F	CP103P11405
81	R 637	R-CARBON-CHIP	1/10W 33K-F	CP103P11406
82	R 630	R-CARBON-CHIP	1/10W 39K-F	CP103P11407
83	R 5M0	R-CARBON-CHIP	1/10W 47K-F	CP103P11408
84	R 921	R-CARBON-CHIP	1/10W 47K-F	CP103P11408
85	R 633	R-CARBON-CHIP	1/10W 56K-F	CP103P11409
86	R 636	R-CARBON-CHIP	1/10W 68K-F	CP103P11500
87	R 629	R-CARBON-CHIP	1/10W 82K-F	CP103P11501
88	R 7A1	R-CARBON-CHIP	1/10W 82K-F	CP103P11501
89	R 7C5	R-CARBON-CHIP	1/10W 82K-F	CP103P11501
90	R 111	R-CARBON-CHIP	1/10W 100K-F	CP103P11502
91	R 6F1	R-CARBON-CHIP	1/10W 100K-F	CP103P11502
92	R 632	R-CARBON-CHIP	1/10W 100K-F	CP103P11502
93	R 7A8	R-CARBON-CHIP	1/10W 100K-F	CP103P11502
94	R 8A3	R-CARBON-CHIP	1/10W 100K-F	CP103P11502
95	R 8A4	R-CARBON-CHIP	1/10W 100K-F	CP103P11502

96	R 8C3	R-CARBON-CHIP	1/10W 100K-F		CP103P11502
97	R 8C4	R-CARBON-CHIP	1/10W 100K-F		CP103P11502
98	R 8C5	R-CARBON-CHIP	1/10W 100K-F		CP103P11502
99	R 8C6	R-CARBON-CHIP	1/10W 100K-F		CP103P11502
100	R 906	R-CARBON-CHIP	1/10W 390K-F		CP103P11509
101	R 128	R-CARBON-CHIP	1/10W 470K-F		CP103P11600
102	R 129	R-CARBON-CHIP	1/10W 470K-F		CP103P11600
103	R 109	R-CARBON-CHIP	1/10W 6.2K-F		CP103P11605
104	R 8A2	R-CARBON-CHIP	1/10W 6.2K-F		CP103P11605
105	R 7B1	R-CARBON-CHIP	1/10W 51K-F		CP103P11606
106	R 608	R-CARBON-CHIP	1/10W 5.1K-F		CP103P11700
107	R 390	R-CARBON-CHIP	1/10W 9.1K-F		CP103P11701
108	R 621	R-CARBON-CHIP	1/10W 9.1K-F		CP103P11701
109	R 3A0	R-CARBON-CHIP	1/10W 20K-F		CP103P11702
110	R 7D5	R-CARBON-CHIP	1/10W 24K-F		CP103P11703
111	R 916	R-CARBON-CHIP	1/10W 24K-F		CP103P11703
112	R 5L6	R-CARBON-CHIP	1/10W 160K-F		CP103P11704
113	R 5L8	R-CARBON-CHIP	1/10W 7.5K-F		CP103P11706
114	R 7D0	R-CARBON-CHIP	1/10W 43K-F		CP103P11800
115	R 7D2	R-CARBON-CHIP	1/10W 43K-F		CP103P11800
116	R 7D4	R-CARBON-CHIP	1/10W 43K-F		CP103P11800
117	R 925	R-CARBON-CHIP	1/10W 2.4K-F		CP103P11801
118	R 405	R-CARBON-CHIP	1/10W 4.3K-F		CP103P11804
119	R 130	R-CARBON-CHIP	1/10W 240K-F		CP103P11808
120	R 131	R-CARBON-CHIP	1/10W 240K-F		CP103P11808
121	R 5J3	R-CARBON-CHIP	1/10W 3.6K-F		CP103P11908
122	R 300	R-METAL-CHIP	1/8W 1.0K-F	3.2X1.6	CP103P14409
123	R 330	R-METAL-CHIP	1/8W 1.0K-F	3.2X1.6	CP103P14409
124	R 360	R-METAL-CHIP	1/8W 1.0K-F	3.2X1.6	CP103P14409
125	R 260	R-METAL-CHIP	1/8W 2.2K-F	3.2X1.6	CP103P14507
126	R 262	R-METAL-CHIP	1/8W 2.2K-F	3.2X1.6	CP103P14507
127	R 264	R-METAL-CHIP	1/8W 2.2K-F	3.2X1.6	CP103P14507
128	R 266	R-METAL-CHIP	1/8W 2.2K-F	3.2X1.6	CP103P14507
129	R 205	R-METAL-CHIP	1/4W 75-F		CP103P48204
130	R 225	R-METAL-CHIP	1/4W 75-F		CP103P48204
131	R 245	R-METAL-CHIP	1/4W 75-F		CP103P48204
132	R 733	R-CHIP	1/16W 75-F	1.6X0.8	CP104P00202
133	R 727	R-CHIP	1/16W 180-F	1.6X0.8	CP104P00301
134	R 710	R-CHIP	1/16W 470-F	1.6X0.8	CP104P00401
135	R 725	R-CHIP	1/16W 680-F	1.6X0.8	CP104P00405
136	R 731	R-CHIP	1/16W 750-F	1.6X0.8	CP104P00406
137	R 732	R-CHIP	1/16W 910-F	1.6X0.8	CP104P00408
138	R 724	R-CHIP	1/16W 1K-F	1.6X0.8	CP104P00409
139	R 728	R-CHIP	1/16W 2.2K-F	1.6X0.8	CP104P00507
140	R 729	R-CHIP	1/16W 2.2K-F	1.6X0.8	CP104P00507
141	R 742	R-CHIP	1/16W 5.1K-F	1.6X0.8	CP104P00606
142	R 713	R-CHIP	1/16W 10K-F	1.6X0.8	CP104P00703
143	R 730	R-CHIP	1/16W 12K-F	1.6X0.8	CP104P00705
144	R 759	R-CHIP	1/16W 20K-F	1.6X0.8	CP104P00800
145	R 714	R-CHIP	1/16W 47K-F	1.6X0.8	CP104P00809
146	R 716	R-CHIP	1/16W 47K-F	1.6X0.8	CP104P00809
147	R 717	R-CHIP	1/16W 47K-F	1.6X0.8	CP104P00809
148	R 718	R-CHIP	1/16W 47K-F	1.6X0.8	CP104P00809
149	R 726	R-CHIP	1/16W 47K-F	1.6X0.8	CP104P00809
150	R 762	R-CHIP	1/16W 100K-F	1.6X0.8	CP104P01001
151	R 715	R-CHIP	1/16W 240K-F	1.6X0.8	CP104P01100
152	R 760	R-CHIP	1/16W 680K-F	1.6X0.8	CP104P01201

153	R 758	R-CHIP	1/16W 1.6M-F	1.6X0.8	CP104P01300
154	R 914	R-CARBON-CHIP	1/10W 510K-F		CP104P22001
155	R 915	R-CARBON-CHIP	1/10W 510K-F		CP104P22001
156	R 410	R-METAL	2W 0.56-F		CP104P30301
157	VR5A1	VR-SEMIFIXED	1/5W B-3K		CP127C03107
158	C 935	C-ELECTROLYTIC	04W 25V 4.7M-M		CP181P03001
159	C 5J6	C-ELECTROLYTIC	04W 25V 47M-M		CP181P03005
160	C 8D7	C-ELECTROLYTIC	04W 25V 100M-M		CP181P03006
161	C 6E1	C-ELECTROLYTIC	04W 100V 47M-M		CP181P03409
162	C 399	C-ELE	04W 25V 47M-M		CP181P04005
163	C 8A0	C-ELECTROLYTIC	04W 25V 220M-M		CP181P04007
164	C 8A4	C-ELECTROLYTIC	04W 25V 220M-M		CP181P04007
165	C 8A5	C-ELECTROLYTIC	04W 25V 220M-M		CP181P04007
166	C 8B3	C-ELECTROLYTIC	04W 25V 220M-M		CP181P04007
167	C 8B4	C-ELECTROLYTIC	04W 25V 220M-M		CP181P04007
168	C 8C3	C-ELECTROLYTIC	04W 25V 220M-M		CP181P04007
169	C 8C4	C-ELECTROLYTIC	04W 25V 220M-M		CP181P04007
170	C 8D3	C-ELECTROLYTIC	04W 25V 220M-M		CP181P04007
171	C 8D4	C-ELECTROLYTIC	04W 25V 220M-M		CP181P04007
172	C 304	C-ELECTROLYTIC	04W 200V 0.47M-M		CP181P04604
173	C 334	C-ELECTROLYTIC	04W 200V 0.47M-M		CP181P04604
174	C 364	C-ELECTROLYTIC	04W 200V 0.47M-M		CP181P04604
175	C 3A1	C-ELECTROLYTIC	04W 200V 3.3M-M		CP181P04607
176	C 601	C-ELECTROLYTIC	04W 450V 2.2M-M		CP181P04900
177	C 809	C-ELECTROLYTIC	25V 220M-M		CP181P06100
178	C 810	C-ELECTROLYTIC	25V 220M-M		CP181P06100
179	C 606	C-ELECTROLYTIC	04W 100V 220 M-M		CP181P09707
180	C 513	C-ELECTROLYTIC	04W 200V 2.2 M-M		CP181P14202
181	C 519	C-ELECTROLYTIC	04W 200V 2.2 M-M		CP181P14202
182	C 524	C-ELECTROLYTIC	04W 200V 3.3M-M		CP181P14203
183	C 6E7	C-ELECTROLYTIC-NP	04 16V 47 M-M-NP		CP181P17206
184	C 301	C-ELECTROLYTIC	04W 16V 47M-M		CP181P18204
185	C 331	C-ELECTROLYTIC	04W 16V 47M-M		CP181P18204
186	C 361	C-ELECTROLYTIC	04W 16V 47M-M		CP181P18204
187	C 391	C-ELECTROLYTIC	04W 16V 47M-M		CP181P18204
188	C 393	C-ELECTROLYTIC	04W 16V 47M-M		CP181P18204
189	C 3A3	C-ELECTROLYTIC	04W 16V 100 M-M		CP181P18205
190	C 3A6	C-ELECTROLYTIC	04W 16V 100 M-M		CP181P18205
191	C 395	C-ELECTROLYTIC	04W 25V 47M-M		CP181P18306
192	C 3D5	C-ELECTROLYTIC	04W 25V 220M-M		CP181P18308
193	C 3D2	C-ELECTROLYTIC	04W 50V 1M-M		CP181P18602
194	C 6E3	C-ELE-NP	16V 10MF-M		CP181P24009
195	C 718	C-ELE	16V 47MF		CP181P50304
196	C 725	C-ELE	16V 47MF		CP181P50304
197	C 7A8	C-ELE	25V 10MF		CP181P50401
198	C 7B1	C-ELE	25V 10MF		CP181P50401
199	C 714	C-ELE	25V 10MF		CP181P50401
200	C 733	C-ELE	25V 10MF		CP181P50401
201	C 201	C-ELE	16V 47MF NP		CP181P50504
202	C 204	C-ELE	16V 47MF NP		CP181P50504
203	C 241	C-ELE	16V 47MF NP		CP181P50504
204	C 244	C-ELE	16V 47MF NP		CP181P50504
205	C 221	C-ELE-NP	16V 100MF NP		CP181P50505
206	C 224	C-ELE-NP	16V 100MF NP		CP181P50505
207	C 932	C-ELECTROLYTIC	16V 100M-M	5X11	CP182P10207
208	C 931	C-ELECTROLYTIC	35V 100M-M	6.3X11	CP182P10504
209	C 398	C-ELECTROLYTIC	100V 33M-M	8X11.5	CP182P11008

210 C 610	C-ELE	50V 4.7M-M	5X11	CP182P13304
211 C 276	C-ELE	25V 100M-M	8X7 1TE/1BA	CP182P14406
212 C 206	C-ELE	25V 47M-M F=5MM	6.3X7	CP182P14407
213 C 226	C-ELE	25V 47M-M F=5MM	6.3X7	CP182P14407
214 C 246	C-ELE	25V 47M-M F=5MM	6.3X7	CP182P14407
215 C 285	C-ELE	25V 47M-M F=5MM	6.3X7	CP182P14407
216 C 287	C-ELE	25V 47M-M F=5MM	6.3X7	CP182P14407
217 C 709	C-ELECTROLYTIC	CE04W 6.3V 470M-M		CP182P16005
218 C 721	C-ELECTROLYTIC	CE04W 6.3V 470M-M		CP182P16005
219 C 116	C-ELECTROLYTIC	CE04W 16V 100M-M		CP182P16204
220 C 121	C-ELECTROLYTIC	CE04W 16V 100M-M		CP182P16204
221 C 128	C-ELECTROLYTIC	CE04W 16V 100M-M		CP182P16204
222 C 611	C-ELECTROLYTIC	CE04W 16V 100M-M		CP182P16204
223 C 968	C-ELECTROLYTIC	CE04W 16V 100M-M		CP182P16204
224 C 974	C-ELECTROLYTIC	CE04W 16V 100M-M		CP182P16204
225 C 975	C-ELECTROLYTIC	CE04W 16V 100M-M		CP182P16204
226 C 5A1	C-ELECTROLYTIC	CE04W 16V 1000M-M		CP182P16208
227 C 5A2	C-ELECTROLYTIC	CE04W 16V 1000M-M		CP182P16208
228 C 509	C-ELECTROLYTIC	CE04W 25V 470M-M		CP182P16307
229 C 401	C-ELECTROLYTIC	CE04W 25V 1000M-M		CP182P16308
230 C 402	C-ELECTROLYTIC	CE04W 25V 1000M-M		CP182P16308
231 C 6R5	C-ELECTROLYTIC	CE04W 25V 1000M-M		CP182P16308
232 C 6S1	C-ELECTROLYTIC	CE04W 25V 1000M-M		CP182P16308
233 C 915	C-ELECTROLYTIC	CE04W 35V 47M-M		CP182P16405
234 C 609	C-ELECTROLYTIC	CE04W 50V 1M-M		CP182P16501
235 C 5J4	C-ELECTROLYTIC	CE04W 50V 2.2M-M		CP182P16502
236 C 613	C-ELECTROLYTIC	CE04W 50V 2.2M-M		CP182P16502
237 C 621	C-ELECTROLYTIC	CE04W 50V 2.2M-M		CP182P16502
238 C 1A0	C-ELECTROLYTIC	CE04W 50V 4.7M-M		CP182P16504
239 C 1A3	C-ELECTROLYTIC	CE04W 50V 4.7M-M		CP182P16504
240 C 106	C-ELECTROLYTIC	CE04W 50V 4.7M-M		CP182P16504
241 C 112	C-ELECTROLYTIC	CE04W 50V 4.7M-M		CP182P16504
242 C 119	C-ELECTROLYTIC	CE04W 50V 4.7M-M		CP182P16504
243 C 132	C-ELECTROLYTIC	CE04W 50V 4.7M-M		CP182P16504
244 C 1C6	C-ELECTROLYTIC	CE04W 50V 10M-M		CP182P16505
245 C 1C7	C-ELECTROLYTIC	CE04W 50V 10M-M		CP182P16505
246 C 1C8	C-ELECTROLYTIC	CE04W 50V 10M-M		CP182P16505
247 C 1C9	C-ELECTROLYTIC	CE04W 50V 10M-M		CP182P16505
248 C 404	C-ELECTROLYTIC	CE04W 50V 100M-M		CP182P16509
249 C 511	C-ELECTROLYTIC	04W 200V 22M-M/Q	10X20	CP182P17206
250 C 961	C-ELECTROLYTIC	04W 200V 220M-M/Q	18X35.5	CP182P17300
251 C 510	C-ELECTROLYTIC	04W 200V 47M-M/Q	12.5X20	CP182P17908
252 C 5J1	C-ELECTROLYTIC-NP	04W 50V 2.2M-M NP	5X11	CP182P18400
253 C 972	C-ELECTROLYTIC	04W 10V 220M-M	6.3X11	CP182P19009
254 C 967	C-ELECTROLYTIC	04W 100V 22M-M	6.3X11	CP182P19705
255 C 127	C-ELE	6.3V 2200M-M	12.5X20	CP182P27006
256 C 719	C-ELECTROLYTIC	6.3V 33M-M	5X7	CP182P29002
257 C 727	C-ELECTROLYTIC	6.3V 100M-M	6.3X7	CP182P29004
258 C 730	C-ELECTROLYTIC	6.3V 100M-M	6.3X7	CP182P29004
259 C 715	C-ELECTROLYTIC	6.3V 330M-M	8X7	CP182P29006
260 C 971	C-ELECTROLYTIC	10V 2200M-M		CP182P31203
261 C 1B4	C-ELECTROLYTIC	16V 470M-M		CP182P31302
262 C 1B6	C-ELECTROLYTIC	16V 470M-M		CP182P31302
263 C 1B8	C-ELECTROLYTIC	16V 470M-M		CP182P31302
264 C 1C4	C-ELECTROLYTIC	16V 470M-M		CP182P31302
265 C 6R3	C-ELECTROLYTIC	25V 47M-M		CP182P31402
266 C 603	C-ELECTROLYTIC	25V 47M-M		CP182P31402

267	C 735	C-ELECTROLYTIC	25V 47M-M			CP182P31402
268	C 964	C-ELECTROLYTIC	25V 820M-M			CP182P31408
269	C 965	C-ELECTROLYTIC	25V 820M-M			CP182P31408
270	C 962	C-ELECTRORYTIC	100V 82M	10X20		CP182P34008
271	C 963	C-ELECTRORYTIC	100V 82M	10X20		CP182P34008
272	C 911	C-ELECTROLYTIC	450V 220M-M	(25X45)		CP185P02601
273	C 604	C-PLASTIC-PP	630V 0.0033MF-K	ECQ-F6332KZ		CP189P12007
274	C 901	C-M-P	AC275V 1.0M-M	ECQU2A105ML		CP189P20104
275		LEAD-CONNECTOR-LED		NFJ9905U	(MT)	CP246C37802
276		FFC-CABLE		TFA1105U	(MT)	CP246C39201
277		FFC-CABLE	6P	NUH1107U	(MT)	CP246C41601
278		FFC-CABLE	13P	NUH1107U	(MT)	CP246C41602
279		FFC-CABLE	13P	NUH1107U	(MT)	CP246C41603
280	AG602	SURGE-ABSORBER	DSP-201M			CP252P00102
281	AG604	SURGE-ABSORBER	DSP-201M			CP252P00102
282	AG3B1	SURGE-ABSORBER	DSP-301N-C04F			CP252P00106
283	AG3G1	SURGE-ABSORBER	DSP-301N-C04F			CP252P00106
284	AG3R1	SURGE-ABSORBER	DSP-301N-C04F			CP252P00106
285	AG3S1	SURGE-ABSORBER	AG15PC152FB-K2M			CP252P00502
286	AG601	SURGE-ABSORBER	AG15PC152FB-K2M			CP252P00502
287	Q 301	TRANSISTOR-CHIP	2SA1255-Y			CP260P09801
288	Q 331	TRANSISTOR-CHIP	2SA1255-Y			CP260P09801
289	Q 361	TRANSISTOR-CHIP	2SA1255-Y			CP260P09801
290	Q 300	TRANSISTOR	2SC3138-Y			CP260P09901
291	Q 330	TRANSISTOR	2SC3138-Y			CP260P09901
292	Q 360	TRANSISTOR	2SC3138-Y			CP260P09901
293	Q 1A0	TRANSISTOR-CHIP	2SC2412K-R			CP260P11001
294	Q 1A1	TRANSISTOR-CHIP	2SC2412K-R			CP260P11001
295	Q 1A2	TRANSISTOR-CHIP	2SC2412K-R			CP260P11001
296	Q 391	TRANSISTOR-CHIP	2SC2412K-R			CP260P11001
297	Q 5J1	TRANSISTOR-CHIP	2SC2412K-R			CP260P11001
298	Q 5J2	TRANSISTOR-CHIP	2SC2412K-R			CP260P11001
299	Q 505	TRANSISTOR-CHIP	2SC2412K-R			CP260P11001
300	Q 7A0	TRANSISTOR-CHIP	2SC2412K-R			CP260P11001
301	Q 7A1	TRANSISTOR-CHIP	2SC2412K-R			CP260P11001
302	Q 702	TRANSISTOR-CHIP	2SC2412K-R			CP260P11001
303	Q 905	TRANSISTOR-CHIP	2SC2412K-R			CP260P11001
304	Q 200	TRANSISTOR-CHIP	2SA1037AK-R			CP260P11401
305	Q 7A2	TRANSISTOR-CHIP	2SA1037AK-R			CP260P11401
306	Q 700	TRANSISTOR-CHIP	2SA1037AK-R			CP260P11401
307	Q 6E1	TRANSISTOR	2SC2240-GR			CP260P13801
308	Q 6E5	TRANSISTOR	2SC2240-GR			CP260P13801
309	Q 5A1	TRANSISTOR	2SD1264A			CP260P20901
310	Q 5A2	TRANSISTOR	2SB940A			CP260P21001
311	Q 503	TRANSISTOR	ET453MR			CP260P33401
312	Q 6E2	TRANSISTOR	KTC4370-Y			CP260P41701
313	Q 6E4	TRANSISTOR	KTA1659-Y			CP260P41801
314	Q 6E6	TRANSISTOR	2SC4620			CP260P41901
315	Q 5J3	TRANSISTOR-CHIP	KRC102S			CP260P42201
316	Q 703	TRANSISTOR-CHIP	KRC102S			CP260P42201
317	Q 704	TRANSISTOR-CHIP	KRC102S			CP260P42201
318	Q 705	TRANSISTOR-CHIP	KRC102S			CP260P42201
319	Q 903	TRANSISTOR-CHIP	KRC102S			CP260P42201
320	Q 962	TRANSISTOR-CHIP	KRC102S			CP260P42201
321	Q 504	MOS-FET	2SJ512-LB107			CP260P42302
322	Q 6E3	TRANSISTOR	2SA970-GR			CP260P42401
323	Q 502	TRANSISTOR	2SC5516-M1			CP260P43102

324	Q 501	TRANSISTOR	2SD1815-T		CP260P43501
325	Q 511	MOS-FET	2SK3157-F15		CP260P44502
326	Q 100	TRANSISTOR-CHIP	KRA109S		CP260P44701
327	Q 902	TRANSISTOR	KRA224M		CP260P46101
328	Q 904	TRANSISTOR-CHIP	KRA107S		CP260P46201
329	Q 961	TRANSISTOR-CHIP	KRA107S		CP260P46201
330	Q 963	TRANSISTOR	KRC105M		CP260P46301
331	Q 901	MOS-FET	2SK2148	FORMING	CP260P46401
332	IC921	IC	SE140N-(FORMING)		CP263P04502
333	IC7A0	IC-SOP	TL084CNS		CP263P07301
334	IC923	IC-REGULATOR	AN7812F		CP263P07701
335	IC304	IC-LINEAR	BA4558F-E2		CP263P12901
336	IC602	IC-LINEAR	BA4558F-E2		CP263P12901
337	IC701	IC-LINEAR	BA4558F-E2		CP263P12901
338	IC7A1	IC-CMOS-SOP	HD74HC04FP		CP263P14201
339	IC104	IC	KIA324F		CP263P21201
340	IC922	IC	KIA431-AT		CP263P21501
341	IC924	IC-REGULATOR	BA05T		CP263P24001
342	IC925	IC-REGULATOR	BA05ST		CP263P25301
343	IC401	IC	TDA9309		CP263P25501
344	IC8A1	IC	LA6500		CP263P26401
345	IC5J2	IC	BA9757		CP263P26501
346	IC5J3	IC	FMG9A		CP263P26801
347	IC506	IC	FMG9A		CP263P26801
348	IC901	IC	MC33262P		CP263P26901
349	IC100	IC	KIA4558F		CP263P27401
350	IC5J1	IC	KIA4558F		CP263P27401
351	IC7A2	IC	KIA4558F		CP263P27401
352	IC702	IC-REGULATOR	TA48M033F(TE16L)	3.3V	CP263P28202
353	IC502	IC	SLA5054		CP263P29701
354	IC8A2	IC	LA6510		CP263P30001
355	IC8A3	IC	LA6510		CP263P30001
356	IC8A4	IC	LA6510		CP263P30001
357	IC902	HIC	STR-F6676		CP263P30401
358	IC200	IC	MM1470XD		CP263P30601
359	IC1A6	IC	SLA3007M		CP263P30701
360	IC301	IC	M52746SP		CP263P30801
361	IC903	IC-MOS	MIP0223SY3M1		CP263P56606
362	IC300	IC	M35071-052SP		CP263P90701
363	D 401	DIODE	EU-1Z/RGP10D		CP264D00501
364	D 511	DIODE	RU1P		CP264P01301
365	D 508	DIODE	EG-1		CP264P01901
366	D 901	DIODE	RBV-606 STRAIGHT		CP264P12304
367	D 504	DIODE	RGP10G		CP264P15501
368	D 512	DIODE	RGP10G		CP264P15501
369	D 513	DIODE	RGP10G		CP264P15501
370	D 976	DIODE-ZENER	HZS7C2L		CP264P18107
371	D 506	DIODE-ZENER	HZS11A1L		CP264P18208
372	D 5J6	DIODE-ZENER	HZS12A1L		CP264P18307
373	D 906	DIODE-ZENER	HZS20-1L		CP264P18506
374	D 906	DIODE-ZENER	HZS24-2L		CP264P18603
375	D 910	DIODE-ZENER	HZS24-2L		CP264P18603
376	D 931	DIODE	RGP10K-5008 G23		CP264P21801
377	D 602	DIODE	UF5408		CP264P22201
378	D 612	DIODE	MPG06JG23		CP264P22801
379	D 962	DIODE	S2L60-01P15	15MM	CP264P23103
380	D 603	DIODE-ZENER-CHIP	MA8056/RD5.6SB/HZU5.		CP264P24301

381	D 5A1	DIODE	EGP10D STRAIGHT		CP264P25002
382	D 5A2	DIODE	EGP10D STRAIGHT		CP264P25002
383	D 613	DIODE-ZENER-CHIP	UDZ3.0B TE-17		CP264P31005
384	D 101	DIODE-ZENER-CHIP	UDZ 4.7B TE-17		CP264P31100
385	D 402	DIODE-ZENER-CHIP	UDZ 4.7B TE-17		CP264P31100
386	D 7A0	DIODE-ZENER-CHIP	UDZ 4.7B TE-17		CP264P31100
387	D 8A0	DIODE-ZENER-CHIP	UDZ 4.7B TE-17		CP264P31100
388	D 611	DIODE	1SS244		CP264P32001
389	D 905	DIODE	1SS244		CP264P32001
390	D 912	DIODE	1SS244		CP264P32001
391	D 963	DIODE	UF4004		CP264P34104
392	D 601	DIODE	UF4005		CP264P34105
393	D 961	DIODE	UF4005		CP264P34105
394	D 904	DIODE	UF4007		CP264P34107
395	D 1A0	DIODE	1SS355TE-17		CP264P38001
396	D 1A1	DIODE	1SS355TE-17		CP264P38001
397	D 1A2	DIODE	1SS355TE-17		CP264P38001
398	D 1A3	DIODE	1SS355TE-17		CP264P38001
399	D 100	DIODE	1SS355TE-17		CP264P38001
400	D 391	DIODE	1SS355TE-17		CP264P38001
401	D 393	DIODE	1SS355TE-17		CP264P38001
402	D 5J1	DIODE	1SS355TE-17		CP264P38001
403	D 5J2	DIODE	1SS355TE-17		CP264P38001
404	D 5J3	DIODE	1SS355TE-17		CP264P38001
405	D 5J4	DIODE	1SS355TE-17		CP264P38001
406	D 5J5	DIODE	1SS355TE-17		CP264P38001
407	D 5J7	DIODE	1SS355TE-17		CP264P38001
408	D 5J9	DIODE	1SS355TE-17		CP264P38001
409	D 501	DIODE	1SS355TE-17		CP264P38001
410	D 505	DIODE	1SS355TE-17		CP264P38001
411	D 604	DIODE	1SS355TE-17		CP264P38001
412	D 605	DIODE	1SS355TE-17		CP264P38001
413	D 614	DIODE	1SS355TE-17		CP264P38001
414	D 615	DIODE	1SS355TE-17		CP264P38001
415	D 616	DIODE	1SS355TE-17		CP264P38001
416	D 617	DIODE	1SS355TE-17		CP264P38001
417	D 618	DIODE	1SS355TE-17		CP264P38001
418	D 700	DIODE	1SS355TE-17		CP264P38001
419	D 701	DIODE	1SS355TE-17		CP264P38001
420	D 907	DIODE	1SS355TE-17		CP264P38001
421	D 908	DIODE	1SS355TE-17		CP264P38001
422	D 909	DIODE	1SS355TE-17		CP264P38001
423	D 911	DIODE	1SS355TE-17		CP264P38001
424	D 934	DIODE	1SS355TE-17		CP264P38001
425	D 966	DIODE	1SS355TE-17		CP264P38001
426	D 967	DIODE	1SS355TE-17		CP264P38001
427	D 968	DIODE	1SS355TE-17		CP264P38001
428	D 969	DIODE	1SS355TE-17		CP264P38001
429	D 970	DIODE	1SS355TE-17		CP264P38001
430	D 972	DIODE	1SS355TE-17		CP264P38001
431	D 973	DIODE	1SS355TE-17		CP264P38001
432	D 974	DIODE	1SS355TE-17		CP264P38001
433	D 975	DIODE	1SS355TE-17		CP264P38001
434	D 301	DIODE-CHIP	1SS376	TE-17	CP264P39701
435	D 331	DIODE-CHIP	1SS376	TE-17	CP264P39701
436	D 332	DIODE-CHIP	1SS376	TE-17	CP264P39701
437	D 361	DIODE-CHIP	1SS376	TE-17	CP264P39701

438	D 362	DIODE-CHIP	1SS376	TE-17	CP264P39701
439	D 6E1	DIODE-CHIP	1SS376	TE-17	CP264P39701
440	D 6E2	DIODE-CHIP	1SS376	TE-17	CP264P39701
441	D 104	DIODE-ZENER-CHIP	UDZS TE17 5.6B	(DH)	CP264P42603
442	D 107	DIODE-ZENER-CHIP	UDZS TE17 5.6B	(DH)	CP264P42603
443	D 108	DIODE-ZENER-CHIP	UDZS TE17 5.6B	(DH)	CP264P42603
444	D 109	DIODE-ZENER-CHIP	UDZS TE17 5.6B	(DH)	CP264P42603
445	D 110	DIODE-ZENER-CHIP	UDZS TE17 5.6B	(DH)	CP264P42603
446	D 304	DIODE-ZENER-CHIP	MA8039-H		CP264P43102
447	D 334	DIODE-ZENER-CHIP	MA8039-H		CP264P43102
448	D 364	DIODE-ZENER-CHIP	MA8039-H		CP264P43102
449	D 6E3	DIODE-ZENER-CHIP	MA8082-H		CP264P43308
450	D 262	DIODE-ZENER-CHIP	MA8056		CP264P43901
451	D 263	DIODE-ZENER-CHIP	MA8056		CP264P43901
452	D 264	DIODE-ZENER-CHIP	MA8056		CP264P43901
453	D 265	DIODE-ZENER-CHIP	MA8056		CP264P43901
454	D 502	DIODE	SB560L-6511		CP264P46402
455	D 930	DIODE	P6KE170A		CP264P46604
456	D 971	DIODE	FMB-29L		CP264P46701
457	D 503	DIODE	PG124S15		CP264P46901
458	D 902	DIODE	FMG-G26S		CP264P47701
459	D 964	DIODE	FMB-G16L		CP264P49101
460	D 965	DIODE	FMB-G16L		CP264P49101
461	D 932	DIODE	AL01Z		CP264P49701
462	D 933	DIODE	RM10A		CP264P49801
463	D 200	DIODE	HSM123		CP264P51301
464	D 201	DIODE	HSM123		CP264P51301
465	D 220	DIODE	HSM123		CP264P51301
466	D 221	DIODE	HSM123		CP264P51301
467	D 240	DIODE	HSM123		CP264P51301
468	D 241	DIODE	HSM123		CP264P51301
469	RP901	POSISTOR	ZPB35BL9R0C	(MI)	CP265P10901
470	TH901	THERMISTOR	NTH18D100LA		CP265P11001
471	TH100	THERMISTOR	NRD3103K400K03FMT		CP265P11401
472	IC201	IC-MOS-EEPROM	24LC21TSN		CP266P18201
473	D 260	IC	NNCD5.6LG		CP266P28001
474	IC1A2	IC	NNCD5.6LG		CP266P28001
475	IC1A3	IC	NNCD5.6LG		CP266P28001
476	IC1A5	IC	NNCD5.6LG		CP266P28001
477	IC1A7	IC	NNCD5.6LG		CP266P28001
478	IC1A8	IC	NNCD5.6LG		CP266P28001
479	IC106	IC	NNCD5.6LG		CP266P28001
480	IC107	IC	NNCD5.6LG		CP266P28001
481	IC305	IC-MOS	M62334FP		CP266P28301
482	IC8A0	IC-MOS	M62334FP		CP266P28301
483	IC102	IC-MOS	M62320FP		CP266P28401
484	IC103	IC-MOS	ST72771N9B1/LJJ		CP266P29603
485	IC101	IC	RN5VS45AA-TR		CP266P30901
486	IC703	IC	RN5VS27AA-TR		CP266P30902
487	IC1A0	IC	UPD72012CU-500		CP266P31602
488	IC700	IC-CMOS	UPD61882		CP266P32301
489	IC105	IC-MOS	M24C32-W/24LC32A	282-1/288-1	CP266P91601
490	IC1A1	IC	ADG719BRT-REEL7		CP266P91801
491	IC1A4	IC	ADG719BRT-REEL7		CP266P91801
492	IC800	HIC	STK391-110		CP267P12801
493	IC303	HIC	MIU-211		CP267P13201
494	IC601	HIC	STR-J6703		CP267P14701

495	IC302	IC	LM2402T			CP267P14801
496	IC911	PHOTO-COUPLER	TCET1106(G)			CP268P01207
497	IC912	PHOTO-COUPLER	TCET1106(G)			CP268P01207
498	IC913	PHOTO-COUPLER	TCET1106(G)			CP268P01207
499	IC203	IC-CMOS	TC74VHCT14AF			CP272P13001
500	F 901	FUSE	215-T5.0AH 250V			CP283P01708
501	F 6E1	PROTECTOR	491.630 0.6A			CP283P05006
502	F 971	PROTECTOR	491.750 0.7A			CP283P05007
503	X 100	CRYSTAL	HC49/U-S*24MHZ			CP285P00804
504	X 1A0	CRYSTAL	HC49/U-S*4MHZ			CP285P00806
505	RY901	RELAY	P040-1/P039-1			CP287P04401
506	RY501	RELAY	AC250V			CP287P90201
507	L 971	COIL-RF	47MH-K	470	SO	CP321P03105
508	L 1B0	COIL-RF	100MH-K	101	SO	CP321P03109
509	L 3P0	COIL-RF	100MH-K	101	SO	CP321P03109
510	L 3P3	COIL-RF	100MH-K	101	SO	CP321P03109
511	L 3P4	COIL-RF	100MH-K	101	SO	CP321P03109
512	L 800	COIL-RF	100MH-K	101	SO	CP321P03109
513	L 801	COIL-RF	100MH-K	101	SO	CP321P03109
514	L 961	COIL-RF	100MH-K	101	SO	CP321P03109
515	L 504	COIL-RF	1000MH-J	102	SO	CP321P03301
516	L 506	COIL-RF	1000MH-J	102	SO	CP321P03301
517	L 505	COIL-RF	1200MH-J	122	SO	CP321P03302
518	L 602	COIL-RF	COIL-RF 10MH-K	100K		CP321P14103
519	L 603	COIL-RF	3.3MH-L	3R3		CP321P17005
520	L 5J1	COIL-RF	1200MH-K	122		CP321P17309
521	L 1B1	COIL-RF	68MH-K	680		CP321P19006
522	L 503	COIL-RF	2200MH-J	222		CP321P19106
523	L 903	TRANS-CHOKE	0155009300		(MI)	CP321P41001
524	L 5A1	COIL-CHOKE			(MI)	CP321P41101
525	L 3D0	COIL-PEAKING	47MH-K	470		CP325P02301
526	L 292	COIL-PEAKING	4.7MH-K	4R7		CP325P03109
527	T 502	TRANS-HORIZ-OUT	0133010800		(MI)	CP332P03501
528	L 507	COIL-HORIZ-LIN	LH 13PA 34FR-T4		(MI)	CP333P04301
529	L 508	COIL-HORIZ-LIN	LH 13PA 35FR-T4		(MI)	CP333P04401
530	T 601	TRANS-FLYBACK	ETF30L6002AZ		(MD)	CP334P06401
531	T 501	TRANS-HORIZ-DRIVE			(MI)	CP336P03301
532	T 503	TRANS-CURRENT	16LAZA		(MI)	CP349P01901
533	T 901	TRANS-POWER	0111017300		(MI)	CP350P09101
534	T 902	TRANS-POWER	P-ST22E		(MI)	CP350P09201
535	L 901	LINE-FILTER	25060		(MI)	CP351P07201
536	L 902	LINE-FILTER	SN10P-601JB		(MI)	CP351P07402
537		COIL-SET		NSH1107U	(MT)	CP409B02901
538	T 6E1	TRANS-DBF	0133013000		(MI)	CP409P08701
539		CORE-FERRITE	ZCAT2035-0940A	TFX1105K	(MI)	CP410C01701
540	L 501	CORE-FERRITE	ZBF506D-00			CP410D00201
541	L 509	CORE-FERRITE	ZBF506D-00			CP410D00201
542	L 3P2	CORE-FERRITE	ZBF503D-00			CP410D00202
543	L 3P5	CORE-FERRITE	ZBF503D-00			CP410D00202
544	L 3P6	CORE-FERRITE	ZBF503D-00			CP410D00202
545	L 394	CORE-FERRITE	ZBF503D-00			CP410D00202
546	L 906	CORE-FERRITE	ZBF503D-00			CP410D00202
547		CORE-FERRITE	3A4 TR-23-11-14			CP410D01304
548	L 601	BEAD-FERRITE	FBR07HA850			CP410P01201
549	L 604	BEAD-FERRITE	FBR07HA850			CP410P01201
550	L 605	BEAD-FERRITE	FBR07HA850			CP410P01201
551	L 905	BEAD-FERRITE	FBR07VB850			CP410P01203

552	L 3B1	BEAD-FERRITE	FBR07UA850			CP410P01204
553	L 3B2	BEAD-FERRITE	FBR07UA850			CP410P01204
554	L 3G1	BEAD-FERRITE	FBR07UA850			CP410P01204
555	L 3G2	BEAD-FERRITE	FBR07UA850			CP410P01204
556	L 3R1	BEAD-FERRITE	FBR07UA850			CP410P01204
557	L 3R2	BEAD-FERRITE	FBR07UA850			CP410P01204
558	L 3L0	FERRITE-CHIP	BK2125HS121			CP410P04101
559	L 3P1	FERRITE-CHIP	BK2125HS121			CP410P04101
560	L 3T0	FERRITE-CHIP	BK2125HS121			CP410P04101
561	L 3T1	FERRITE-CHIP	BK2125HS121			CP410P04101
562	L 300	FERRITE-CHIP	BK2125HS121			CP410P04101
563	L 330	FERRITE-CHIP	BK2125HS121			CP410P04101
564	L 360	FERRITE-CHIP	BK2125HS121			CP410P04101
565	L 390	FERRITE-CHIP	BK2125HS121			CP410P04101
566	L 391	FERRITE-CHIP	BK2125HS121			CP410P04101
567	L 392	FERRITE-CHIP	BK2125HS121			CP410P04101
568	L 393	FERRITE-CHIP	BK2125HS121			CP410P04101
569	L 395	FERRITE-CHIP	BK2125HS121			CP410P04101
570	L 260	FERRITE-CHIP	BLM21A601SPT			CP410P07205
571	L 281	FERRITE-CHIP	BLM21A601SPT			CP410P07205
572	L 282	FERRITE-CHIP	BLM21A601SPT			CP410P07205
573	L 283	FERRITE-CHIP	BLM21A601SPT			CP410P07205
574	L 284	FERRITE-CHIP	BLM21A601SPT			CP410P07205
575	L 7A1	FERRITE-CHIP	BLM21A601SPT			CP410P07205
576	L 7A2	FERRITE-CHIP	BLM21A601SPT			CP410P07205
577	L 700	FERRITE-CHIP	BLM21A601SPT			CP410P07205
578	L 701	FERRITE-CHIP	BLM21A601SPT			CP410P07205
579	L 702	FERRITE-CHIP	BLM21A601SPT			CP410P07205
580	L 703	FERRITE-CHIP	BLM21A601SPT			CP410P07205
581	L 705	FERRITE-CHIP	BLM21A601SPT			CP410P07205
582	L 706	FERRITE-CHIP	BLM21A601SPT			CP410P07205
583	L 707	FERRITE-CHIP	BLM21A601SPT			CP410P07205
584		CORE-FERRITE	HF57RH16X17X9		(MI)	CP410P12105
585		CORE-FERRITE	HF57SH35X0.8X12		(MI)	CP410P12108
586	SW901	SW-PUSH	ESB92S21B			CP432P02001
587	SW100	SW-TACT	SKHH92F525-AA			CP432P02102
588		NOISE-FILTER	SUP-L3G-E-3B	TFA1105U	(MT)	CP452P25301
589		SHAFT-POWER	PC+PS X7203L		(MI)	CP770A01901
590		SHAFT-SW	PC+PS X7203L		(MI)	CP770B00401
591		CUSHION	FOAMED-P.S P=0.017	NSH1117K		CP803A09001
592		PACKING-BAG	POLYETHYLENE-SHEET-T	TFA1105U		CP831C02201
593		ASSY PCB MAIN	+DEFL-SUB	NSH1157		CT920A31703
594		ASSY PCB POWER	NSH1157			CT920B46703
595		ASSY PCB VIDEO	NSH1157			CT920B46803
596		ASSY PCB INTERFACE	NSH1157			CT920B46903
597		ASSY PCB CRT	NSH1157			CT920C23103
598	R 939	R-FUSE	1/4W 3.3-J	3R3 RNF-H		QX103P37806
599	R 511	R-FUSE	1/2W 2.7K-J			QX103P39300
600	R 5A1	R-FUSE	1/2W 1.0-J	010RNF-H		QX103P39800
601	R 5A3	R-FUSE	1/2W 1.0-J	010RNF-H		QX103P39800
602	R 505	R-FUSE	1/2W 1.0-J	010RNF-H		QX103P39800
603	R 638	R-FUSE	1/2W 1.0-J	010RNF-H		QX103P39800
604	D 390	DIODE	1S2076A/1S2471			QX264P04508
605	D 392	DIODE	1S2076A/1S2471			QX264P04508
606	D 394	DIODE	1S2076A/1S2471			QX264P04508
607	D 7A1	DIODE	1S2076A/1S2471			QX264P04508
608	D 7A2	DIODE	1S2076A/1S2471			QX264P04508

609	D 300	DIODE	1SS83	QX264P36701
610	D 302	DIODE	1SS83	QX264P36701
611	D 303	DIODE	1SS83	QX264P36701
612	D 330	DIODE	1SS83	QX264P36701
613	D 333	DIODE	1SS83	QX264P36701
614	D 360	DIODE	1SS83	QX264P36701
615	D 363	DIODE	1SS83	QX264P36701