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ENGINEERING SPECIFICATIONS

for

**SD7704C
SD7704CM**

REVISION CHANGE RECORD:

REVISION	CHANGE CONTENTS	DATE

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1. SCOPE

This specification defines the performance of SD7704C/CM 17 inch multisync color monitor.

2. INPUT REQUIREMENTS

2.1 AC Power Supply

- 2.1.1 Power Source : 90~264VAC , 45~66Hz
- 2.1.2 Power Consumption : Less than 90W (SD7704C)
Less than 100W (SD7704CM)
- 2.1.3 Inrush Current : less than 30Ao-p at 100V~240V on cold starting.
- 2.1.4 Input Current : 1.5A (SD7704C)
1.8A (SD7704CM)
- 2.1.5 Leakage Current : 0.75mA at AC 100V/240V.
- 2.1.6 Ripple / Noise : should not cause any visible interference.
- 2.1.7 Power Cord : Please refer to SD7704C / SD7704CM Technical Specification.

2.2 Input Signals

- 2.2.1 RGB Video : Analog , 0.7Vp-p, positive , Input impedance 75 Ω .
- 2.2.2 Sync Signal : Separate or composite horizontal and vertical sync (TTL level).
- 2.2.3 Input Connector :

a. 15 pin MINI "D" SUB :

<u>Pin No.</u>	<u>Signal</u>	<u>Pin No.</u>	<u>Signal</u>
1	Red	9	NC
2	Green	10	Ground
3	Blue	11	Ground
4	Ground	12	SDA
5	Ground	13	H. Sync
6	R Return	14	V. Sync
7	G Return	15	SCL
8	B Return		

- 2.2.4 Signal memory modes : 10 preset modes, 10 user modes , see APPENDIX A .
- 2.2.5 Plug & play : VESA DDC1 / 2B. DDC data APPENDIX B.

2.3 Scanning Frequency

- 2.3.1 Horizontal : 30KHz to 70KHz
- 2.3.2 Vertical : 50Hz to 100Hz

3. ADJUSTMENT CONTROL

3.1 User Control

- 3.1.1 Power switch
- 3.1.2 OSD key : See APPENDIX C.
 - MENU : Main menu select only
 - ▼ : Select sub item
 - + : Contrast and brightness OSD / Scale increase
 - : Contrast and brightness OSD / Scale decrease
 - MENU & ▼ : Exit

3.2 OSD Adjustment function

- 3.2.1 CONTRAST
- BRIGHTNESS
- 3.2.2 VOLUME (Option for SD7704CM)
- BASIC
 - V-POSITION
 - H-POSITION
 - V-SIZE
 - H-SIZE
 - V-MOIRE
 - DEGAUSS
- GEOMETRY
 - PINCUSHION
 - TRAPEZOID
 - PARALLEL
 - ROTATION
- COLOR
 - 9300K / 6500K SELECT
 - COLOR ADJUST (R.G.B)
- STATUS (FREQ. / POLARITY)
- RESET (FACTORY PRESET MODE)
- OSD OFF (EXIT OSD)

3.3 LED Indication

Status		LED
Power On	Normal	Green
	Power Saving	Stand-by Suspend Active Off
	Over Range Freq.	Amber
Power Off		Amber
		Off

4.0. ELECTRICAL SPECIFICATION

A. ELECTRICAL SPECIFICATION

4.1 Standard Condition of measurement

- 4.1.1 Brightness – 50% Factory shipment condition
- 4.1.2 Contrast– 100% Factory shipment condition (MAX)
- 4.1.3 Other SW – Factory shipment condition
- 4.1.4 Back Ground Color -- Black
- 4.1.5 Brightness – 100~130cd/m² (Full white)
- 4.1.6 Temperature, Humidity -- 25°C , 10~80% , Non-condensing
- 4.1.7 Power Input – (AC 100V / 240V · 50Hz / 60Hz)
- 4.1.8 Magnetic field – Northern Hemisphere magnetic field
(Ver. 0.4 GAUSS · Hor. 0.0 GAUSS)
- 4.1.9 Warm up time –30 Minutes minimum
- 4.1.10 Timing chart – Refer to APPENDIX A
- 4.1.11 Ambient lighting environment – 400 to 600lux

4.2 CRT Specification

ITEM	SPEC.	NOTE
Size	17 inch	
Deflection	90°	
Persistence	P22 Medium Short persistence phosphor	
Phosphor pitch	0.28mm	
Neck-diameter	29.1mm	
Screen finish	Flat-square ARCAS 570 Coating	
Face plate	Filter Glass	
Maker/Type	TOSHIBA [M41LLJ107XX530]	

4.3 Power Saving

4.3.1

Status	Hor. Sync.	Vert. Sync.	Power Consumption	Power LED
Normal	Yes	Yes	Normal	Green
Stand-by	No	Yes	< 15W	Amber
Suspend	Yes	No	< 15W	Amber
Auto-Off	No	No	< 8W	Amber

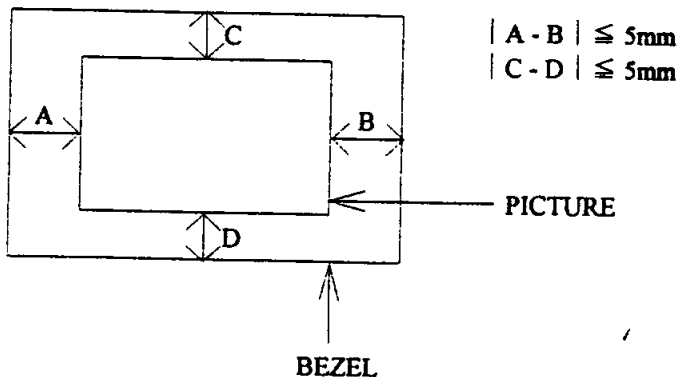
B. SCREEN CHARACTERISTICS

4.4 Picture display size

Horizontal size : $300 \pm 5\text{mm}$

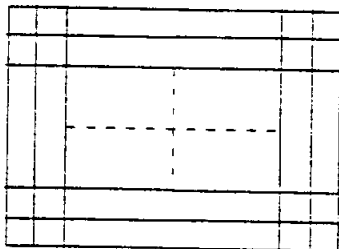
Vertical size : $225 \pm 5\text{mm}$

4.5 Picture Center :



4.6 Linearity

16x12



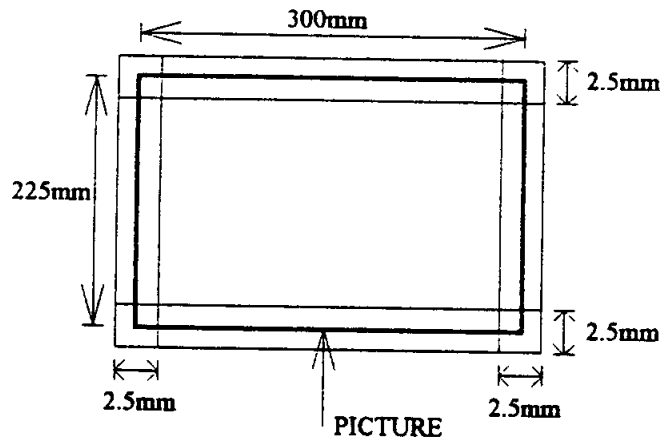
$$\text{H-Linearity} : \frac{X_{\text{max}} - X_{\text{min}}}{X_{\text{max}}} \times 100\% \leq 10\%$$

$$\text{V-Linearity} : \frac{Y_{\text{max}} - Y_{\text{min}}}{Y_{\text{max}}} \times 100\% \leq 10\%$$

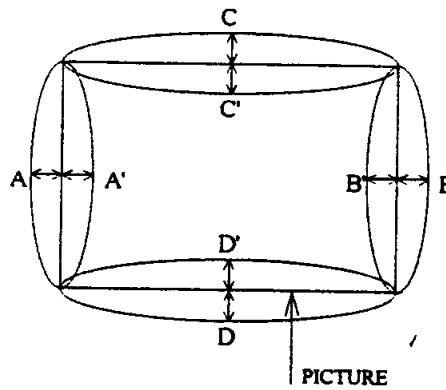
Input signal : Cross-hatch pattern

4.7 Picture Distortion :

4.7.1 Trapezoid / Parallelogram : Within 2.5mm frame

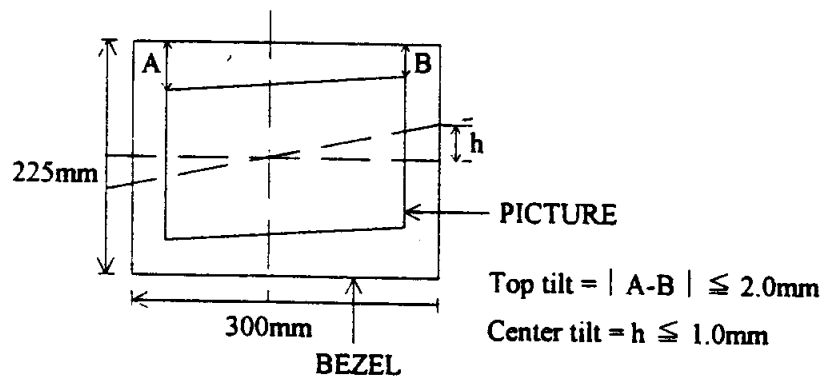


4.7.2 Pincushion / Barrel :

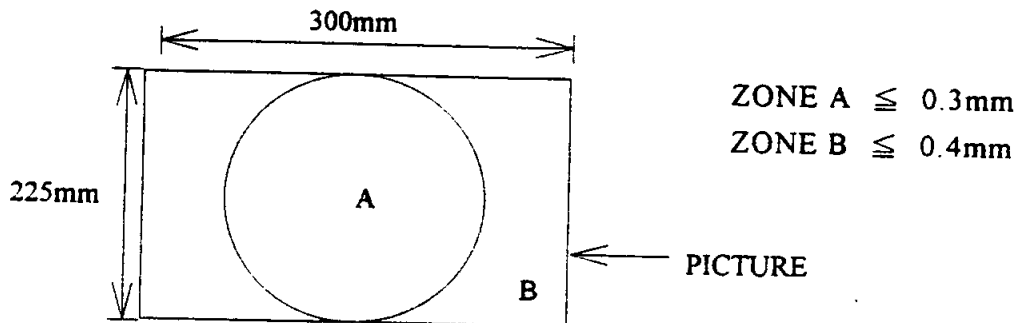


PINCUSHION $\leq 2\text{mm}$
 BARREL $\leq 1.0\text{mm}$

4.7.3 Tilt



4.8 Misconvergence



4.9 Focus

4.9.1 Under the condition of Brightness : Center and Contrast : maximum, each "H" character (approx. 2x2.5mm) within the full screen of "H" pattern can be seen clearly by using the preset timing No.8 (60.023KHz) If necessary, limit sample agreed by both parties will be made for final focus judgement.

4.10 Jitters

4.10.1 No more than one dot movement 50cm away

4.11 White Balance

4.11.1 Color Temperature : Using the CIE color temperature coordinate system ,
Color 9300K: $x = 0.283 \pm 0.02$
 $y = 0.297 \pm 0.02$
Color 6500K: $x = 0.313 \pm 0.02$
 $y = 0.329 \pm 0.02$

4.11.2 Color Tracking : When the white window pattern (approx. 70mm x 70mm) (only for 9300K) is displayed at preset condition. The difference of white balance between contrast max. and low contrast (25cd/m²) must be less than following value.

$$\begin{aligned} | x (\text{at con. Max}) - x (\text{at } 25\text{cd/m}^2) | &\leq 0.02 \\ | y (\text{at con. Max.}) - y (\text{at } 25\text{cd/m}^2) | &\leq 0.02 \end{aligned}$$

4.11.3 Purity : Impurity should not appear in the pattern of all green, all red, all blue or all white.

4.12 Light Output

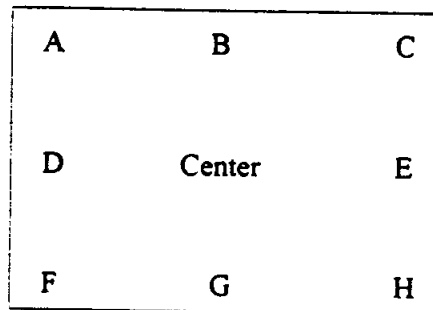
- 4.12.1 At 70mm x 70mm white block pattern : $150 \pm 20 \text{cd/m}^2$
- 4.12.2 At full-white pattern : $100\text{-}130 \text{cd/m}^2$

4.13 Video Amplifier Performance

- 4.13.1 Video Bandwidth : $50\text{Hz} \sim 100\text{MHz} \pm 3\text{dB}$
- 4.13.2 Resolution : 1280dots x 1024 lines

4.14 Brightness Uniformity

- 4.14.1 25% deviation maximum between center any eight points within the display picture .



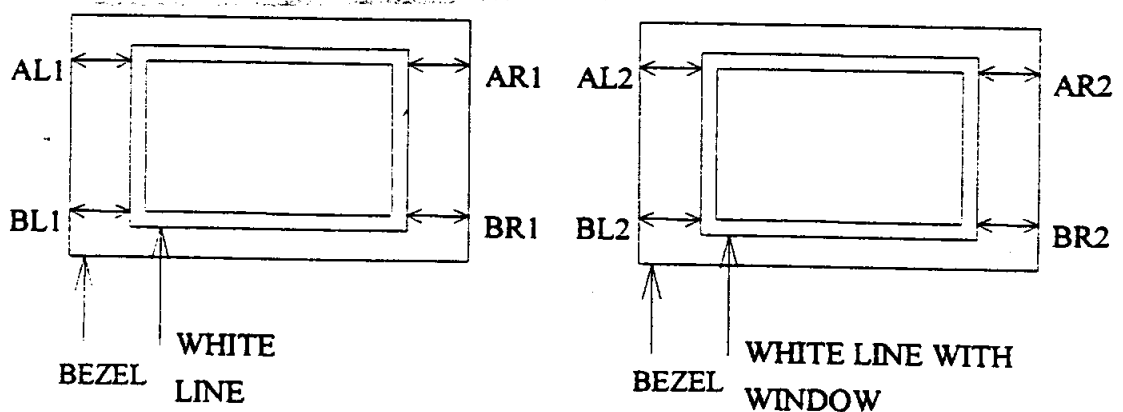
4.15 Size Regulation

4.15.1 Static Regulation

Picture growth from minimum light output to maximum light output shall be less than 4mm for horizontal size, 3mm for vertical size at white pattern.

4.15.2 Dynamic Regulation

Picture growth shall be less than 1.5mm when picture is exchanged from :



Spec. : $| (AL2 - BL2) - (AL1 - BL1) | < 1.5\text{mm}$
 $| (AR2 - BR2) - (AR1 - BR1) | < 1.5\text{mm}$

Condition :

White line size : 300mm x 225mm
White window size : 295mm x 56mm
Brightness : Center
Contrast : Maximum
Timing : All Preset Timings

4.16 Audio (ML)

- (A) Input signal for testing:
 - Amplitude : 2.2Vp-p
 - Frequency : 1KHz
 - Waveform : Sine Wave
- (B) Output signal spec under volume maximum condition (Volume=100%)
 - Audio Output : 3Wrms + 15% -10%
 - Distortion : Less than 10%
- (C) Output signal spec under volume minimum condition (Volume=0%)
 - Audio output must be inaudible.
- (D) Audio output must be mute under following condition.
 - 1) While power ON and OFF.
 - 2) While display timing mode change.
- (E) Previous volume setting must be kept whenever power is OFF and then ON.
- (F) Volume setting must be set to 0% manually before monitor is packed for shipment.

5. REGULATIONS

5.1 The basic requirements shall comply with the latest revisions of the following :

- 1) **Electromagnetic Interference:**
 - FCC Class B, DOC-B, EN55022-B, EN50082-1, VCCI-2.
- 2) **Safety and Regulatory approvals:**
 - UL1950(UL), CSA C22.2 No.950(cUL), DHHS, HWC, ROV vom8.1.1987
- 3) **Low radiation:**
 - CE-Marking, NUTEK Spec.903299/94, ZH1/618(TUV-GS), MPR- II , TCO95
- 4) **Ergonomics:**
 - ISO9241-3 (TUV-ERGO)
- 5) **Power save:**
 - International energy star office equipment program.
- 6) **Display data channel (DDC):**
 - VESA DDC 1/2B

6. ENVIRONMENTAL CONDITIONS

- 6.1 Temperature and Humidity at operation : 0 ~ 35°C
10% ~ 80% RH (without condensation)
- 6.2 Temperature and Humidity at storage : -40°C ~ 60°C
0 ~ 90% RH Less than 6 month
- 6.3 Vibration Test (packaged) : Sine Wave 10~300Hz 1.5G
Sweep rate : 1 octave / min
Sweep time : 5 min
Test time : 1 HR / axis
- 6.4 Shock Test (packaged) : 30G for 11ms half sine wave
1 time on each surface.
- 6.5 Drop Test (packaged) : 61cm height
1 corner, 3 edges, 6 faces
1 time on each tested unit.
Less than 30G for each face.
- 6.6 Power line interference noise : Amplitude : 1.4KV
Pulse width : 50ns, 100ns, 400ns, 800ns
Phase : 0 ~ 360°
Polarity : + / -
Test time : 1 min
No unrecoverable damage is allowed.
(Recoverable misfunction by changing timing or power on/off is allowed.)
- 6.7 Electrostatic discharge + Contact discharge : 8KV
Air discharge : 20KV
No unrecoverable damage is allowed.
(Recoverable misfunction by changing timing or power on/off is allowed.)
- 6.8 Arcing Test
500 times to each pin of CRT (except heater). After arcing happen, no unrecoverable damage is allowed. (Recoverable misfunction by changing timing or power on/off is allowed.)
- 6.9 Altitude
Operating : 0 ~ 10000 feet
Non-operating : 0 ~ 40000 feet

7. RELIABILITY

7.1 Mean Time Between Failures (MTBF)

The MTBF of the display unit shall be longer than 30,000 hours under MIL-HDBK-217E.

Manufacture shall tender DEMO-MTBF data which is based on the MIL-STD-718C with longer than 50,00 hours.

7.2 CRT Lifetime

The lifetime of cathode ray tube shall be longer than 10,000 hours.

The lifetime of cathode ray tube shall be defined as a period between the beginning of use and the time when its brightness decreases to 70% of its beginning.

8. PHYSICAL SPECIFICATION

8.1 Dimension

Height 430mm

Width 423mm

Depth 425mm

8.2 Weight

17.0Kg (NET) 20.0Kg (GROSS)

8.3 Mechanical adjustment

Tilt - 5 / + 15 degrees

Swivel ± 90 degrees

8.4 Packaging

(1) Carton Dimension

Height 518mm

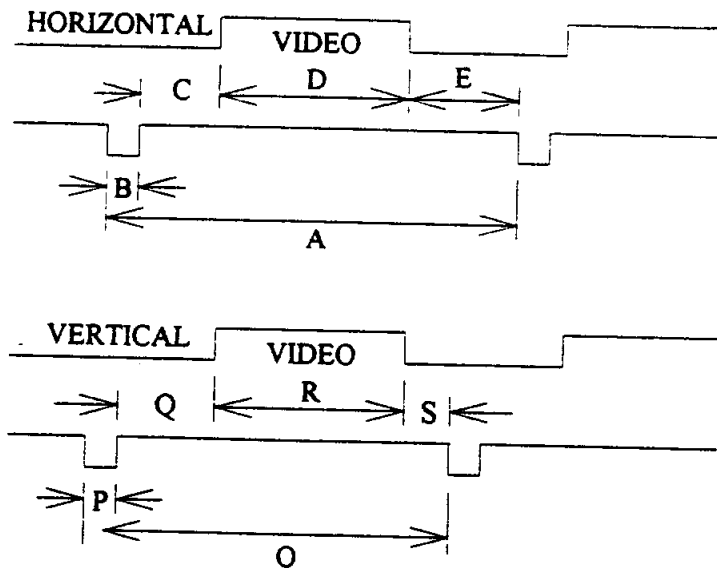
Width 565mm

Depth 565mm

(2) Shipping Weight

TBD

APPENDIX A : Timing of input signals



- | | |
|------------------------|------------------------|
| A : H-TOTAL TIME | O : V-TOTAL TIME |
| B : H-SYNC PULSE WIDTH | P : V-SYNC PULSE WIDTH |
| C : H-BACK PORCH | Q : V-BACK PORCH |
| D : H-DISPLAY TIME | R : V-DISPLAY TIME |
| E : H-FRONT PORCH | S : V-FRONT PORCH |

Magnetic Field

The northern hemisphere :	VERT.	0.4 (GAUSS)
	HOR.	0.0
The southern hemisphere :	VERT.	-0.4 (GAUSS)
	HOR.	0.0
EQUATOR :	VERT.	-0.0 (GAUSS)
	HOR.	0.0 (GAUSS)

SD7704C / SD7704CM ENGINEERING SPECIFICATION

Mode No.	1	2	3	4	5	6	7	8	9	10
Mode Name	VGA 640X 400	VGA 640X 480	VESA 640X 480	VESA 800X 600	VESA 800X 600	VESA 1024X 768	VESA 1024X 768	VESA 1024X 768	VESA 1280X 1024	VESA 1024X 768
Horizontal Dots	640	640	640	800	800	1024	1024	1024	1280	1024
Vertical Lines	400	480	480	600	600	768	768	768	1024	768
Pixel Clock (MHz)	25.175	25.175	31.5	49.5	50.0	64.999	75.003	78.75	108	94.5
Horizontal Freq (KHz)	31.47	31.47	37.5	46.875	48.077	48.363	56.476	60.023	63.981	68.677
Sync. Polarity	-	-	-	+	+	-	-	+	+	+
A H. total (us) (Pixels)	31.778 (800)	31.778 (800)	26.667 (840)	21.333 (1056)	20.800	20.677	17.707	16.66 (1312)	15.63 (1688)	14.51 (1376)
B H. sync. (us) (Pixels)	3.813 (96)	3.813 (96)	2.032 (64)	1.616 (80)	2.400	2.092	1.813	1.219 (96)	1.037 (112)	1.016 (96)
C H. back porch (us) (Pixels)	1.907 (48)	1.907 (48)	3.81 (120)	3.232 (160)	1.280	2.462	1.921	2.235 (176)	2.296 (248)	2.201 (208)
D H. active (us) (Pixels)	25.422 (640)	25.422 (640)	20.317 (640)	16.162 (800)	16.00	15.754	13.653	13.003 (1024)	11.852 (1280)	10.836 (1024)
E H. front porch (us) (Pixels)	0.636 (16)	0.636 (16)	0.508 (16)	0.323 (16)	1.120	0.369	0.320	0.203 (16)	0.444 (64)	0.508 (48)
Vertical Freq. (Hz)	70.08	59.94	75	75	72.188	60.004	70.069	75.029	60.02	85
Sync. Polarity	+	-	-	+	+	-	-	+	+	+
O V. total (ms) (Lines)	14.268 (449)	16.684 (525)	13.333 (500)	13.333 (625)	13.853	16.667	14.272	13.328 (800)	16.661 (1066)	11.765 (808)
P V. sync. (ms) (Lines)	0.064 (2)	0.064 (2)	0.08 (3)	0.064 (3)	0.125	0.124	0.106	0.05 (3)	0.047 (3)	0.044 (3)
Q V. back porch (ms) (Lines)	1.112 (35)	1.048 (33)	0.427 (16)	0.448 (21)	0.478	0.601	0.514	0.466 (28)	0.594 (38)	0.524 (36)
R V. active (ms) (Lines)	12.711 (400)	15.254 (480)	12.8 (480)	12.8 (600)	12.48	15.880	13.599	12.795 (768)	16.005 (1024)	11.183 (768)
S V. front porch (ms) (Lines)	0.381 (12)	0.318 (10)	0.027 (1)	0.021 (1)	0.770	0.062	0.106	0.017 (1)	0.016 (1)	0.015 (1)
Scantype Interlaced	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO

APPENDIX B:

DDC Contents for SD7704C / SD7704CM
(TOSHIBA TUBE)

Address	Data	Description	Define by
00	00	Header	Manufacture
01	FF		
02	FF		
03	FF		
04	FF		
05	FF		
06	FF		
07	00		
08	34	ID Manufacture Name	Purchaser
09	AC	(EISA 3 character ID)	
0A	10	ID Product Code	Purchaser
0B	42	(Vender Assigned)	
0C	**	ID Serial Name 32 bits serial no.	Manufacture
0D	**		
0E	**		
0F	**		
10	**	Week of manufacture (0-53)	Manufacture
11	**	Year of Manufacture (year-1990)	
12	01	EDID version	Manufacture
13	01	Revision	
14	0C	Video Input Define (see Note 1)	Manufacture
15	1E	Max. H. Image Size (cm)	Manufacture
16	17	Max. V. Image Size (cm)	Manufacture
17	C8	(gamma*100)-100	Manufacture
18	E8	DPMS (see Note 2)	Manufacture
19	E1	Red Green bits Rx1Rx0Rxy1Ry0Gx1GxGy1Gy0	Manufacture
1A	68	Blue White bits Bx1Bx0By1By0Wx1Wx0Wy1Wy0	
1B	9E	Red x bits9-2	
1C	55	Red y bits9-2	
1D	4A	Green x bits9-2	
1E	98	Green y bits9-2 (See Note 3)	
1F	27	Blue x bits9-2	
20	12	Blue y bits9-2	
21	48	White x bits9-2	
22	4C	White y bits9-2	
23	A4	Established Timing I	Manufacture
24	CE	Established Timing II	
25	00	Established Timing III (See Not 4)	
26	61	Standard Timing Identification	Manufacture
27	59	#1	
28	81	#2	Manufacture
29	80		

SD7704C / SD7704CM ENGINEERING SPECIFICATION

Address	Data	Description	Define by	
2A	01	#3	Manufacture	
2B	01			
2C	01	#4	Manufacture	
2D	01			
2E	01	#5	Manufacture	
2F	01			
30	01	#6	Manufacture	
31	01			
32	01	#7	Manufacture	
33	01			
34	01	#8	Manufacture	
35	01			
36	EA	Detailed Timing Description #1	Purchaser	
37	24			
38	00			
39	60			
3A	41			
3B	00			
3C	28			
3D	30			
3E	D0			
3F	60			
40	43			
41	08			
42	2C			
43	E1			
44	10			
45	00			
46	00			
47	1E			
48	00	Monitor Range Limit	Purchaser	
49	00			
4A	00			
4B	FD			
4C	00			
4D	32			Vertical Range
4E	64			50Hz - 100Hz
4F	1E			Horizontal Range
50	46			30KHz - 70KHz
51	0A			Bandwidth (max.)
52	00			100MHz
53	0A			
54	20			
55	20			
56	20			
57	20			
58	20			
59	20			

SD7704C / SD7704CM ENGINEERING SPECIFICATION

Address	Data	Description		Define by
5A	00			Purchaser
5B	00			
5C	00			
5D	FC			
5E	00			
5F	53	S		
60	44	D		
61	37	7		
62	37	7		
63	30	0		
64	34	4		
65	43	C		
66	0A			
67	20			
68	20			
69	20			
6A	20			
6B	20			
6C	00	Monitor Serial Number Serial Number in ASC II code		Purchaser
6D	00			
6E	00			
6F	FF			
70	00			
71	**			
72	**			
73	**			
74	**			
75	**			
76	**			
77	**			
78	**			
79	**			
7A	0A			
7B	20			
7C	20			
7D	20			
7E	00	Extension Flag		Manufacture
7F	—	Check sum		

Note 1

Bit	Bits Description
7	Analog / Digital Signal Level
6	Signal Level Standard (6)
5	Signal Level Standard (5)
4	Setup
3	Signal Level Standard (3)
2	Signal Level Standard (2)
1	Signal Level Standard (1)
0	Signal Level Standard (0)

Bit	Description															
7	Analog / Digital Input : Defines usage of the rest of the bytes as "analog" or "digital" input. Analog=0, Digital=1. If input is described as analog, the following definitions to bits 6-0. Digital is as yet undefined in the following but provisions have been made in anticipation of a common video output standard for Flat Panel Display (FPD) use.															
6:5	Signal Level Standard (6:5) : Refer to the following bit definitions. Identified by the level of reference white volts above blank, following by the level of the sync tips in volts below blank. <table border="1" style="margin-left: 40px;"> <thead> <tr> <th>Bit 6</th> <th>Bit 5</th> <th>Operation</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0.700V / 0.300V (1.000Vp-p)</td> </tr> <tr> <td>0</td> <td>1</td> <td>0.714V / 0.286V (1.000Vp-p)</td> </tr> <tr> <td>1</td> <td>0</td> <td>1.000V / 0.400V (1.400Vp-p)</td> </tr> <tr> <td>1</td> <td>1</td> <td>Reserved : TBD</td> </tr> </tbody> </table>	Bit 6	Bit 5	Operation	0	0	0.700V / 0.300V (1.000Vp-p)	0	1	0.714V / 0.286V (1.000Vp-p)	1	0	1.000V / 0.400V (1.400Vp-p)	1	1	Reserved : TBD
Bit 6	Bit 5	Operation														
0	0	0.700V / 0.300V (1.000Vp-p)														
0	1	0.714V / 0.286V (1.000Vp-p)														
1	0	1.000V / 0.400V (1.400Vp-p)														
1	1	Reserved : TBD														
4	Setup : IF set, the display is set to expect a blank-to black setup or pedestal per the appropriate signal level standard.															
3:0	Sync Input (See Bit Operation below)															
	3 Separate Sync															
	2 Composite Sync (on H. Sync line)															
	1 Sync on Green Video															
	0 Serration of the V. Sync Pulse is required when composite sync or sync-on-green video is used.															

Note 2

Bit 7	Stand-by
Bit 6	Suspend
Bit 5	Active off
Bit 4 : 3	Display Type
	0, 0 – Monochrome / gray scale display
	0, 1 – RGB color display
	1, 0 – Non-RGB multicolor display (example: RGY)
	1, 1 – Undefined.
Bit 2 : 0	Reserved Set at 00H until defined.

SD7704C / SD7704CM ENGINEERING SPECIFICATION

Note 3

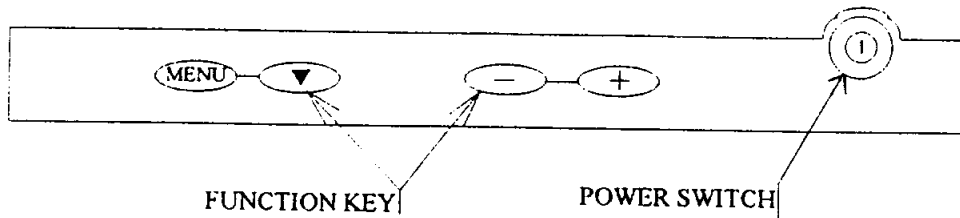
CRT Vendor	Red (x / y)	Green (x / y)	Blue (x / y)	Gamma
Toshiba	0.620 / 0.334	0.289 / 0.595	0.153 / 0.072	3.0

Note 4

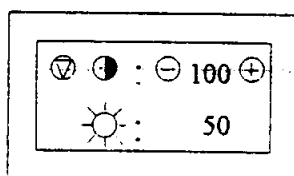
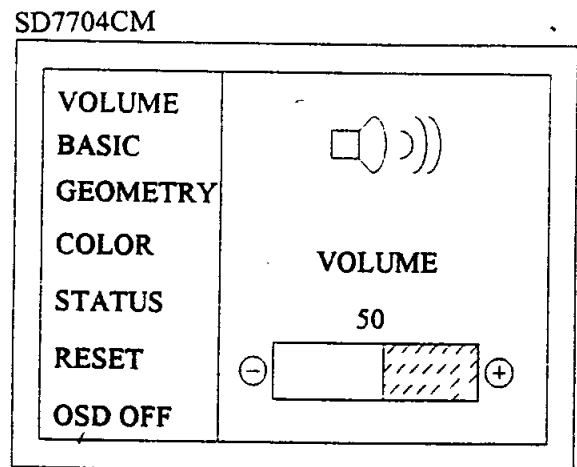
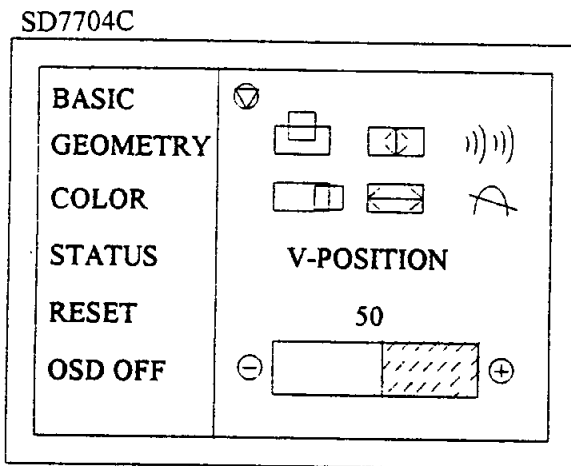
Byte 1	bit	Established Timings I	Source
	7	720x400 @ 70Hz (640x400)	(VGA , IBM)
	6	720x400 @ 88Hz	(XG2 , IBM)
	5	640x480 @ 60Hz	(VGA , IBM)
	4	640x480 @ 67Hz	(MAC II , APPLE)
	3	640x480 @ 72Hz	(VESA)
	2	640x480 @ 75Hz	(VESA)
	1	800x600 @ 56Hz	(VESA)
	0	800x600 @ 60Hz	(VESA)
Byte 2	bit	Established Timings II	
	7	800x600 @ 72Hz	(VESA)
	6	800x600 @ 75Hz	(VESA)
	5	832x624 @ 75Hz	(MAC II , APPLE)
	4	1024x768 @ 87Hz (interlaced)	(IBM)
	3	1024x768 @ 60Hz	(VESA)
	2	1024x768 @ 70Hz	(VESA)
	1	1024x768 @ 75Hz	(VESA)
	0	1280x1024 @ 75Hz	(VESA)
Byte 3	bit	Manufacturer's Timings	Manufacturer's Specified Timings
	7	1152x870 @ 75Hz	(MAC II , APPLE)
	6	Reserved	Manufacturer's Specified Timings
	5	Reserved	
	4	Reserved	
	3	Reserved	
	2	Reserved	
	1	Reserved	
	0	Reserved	

APPENDIX C : Adjustment Control

1. Key Control:



2. On Screen Display:



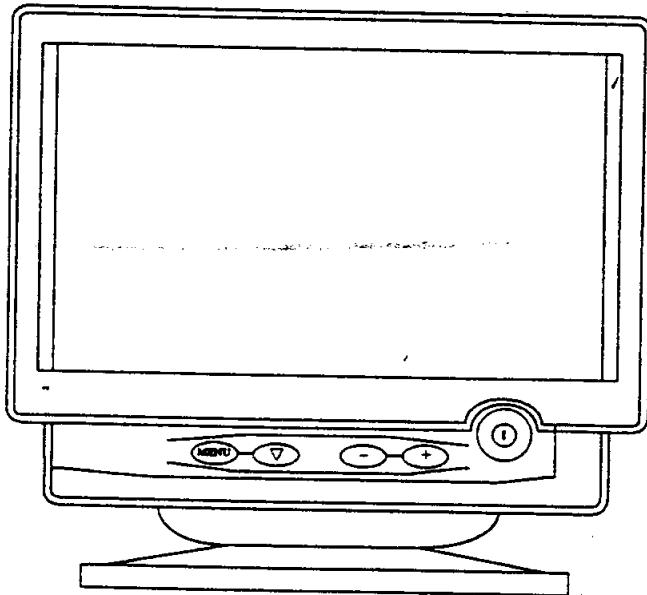
Front Panel Function Control Description

Control Function

- A. User Control
- B. OSD Function Control

A. User Control

- Power Switch
- Function Select Button (MENU)
- Degauss Button and Select SUB Manual Button (▽)
- Contrast Adjust Button and Picture Adjust Button (-)
- Brightness Adjust Button and Picture Adjust Button (+)



FRONT PANEL FUNCTION CONTROL DESCRIPTION

Control Name

a. Power Switch : Push-on / Push-off Switch for AC Power.

b. LED Indication

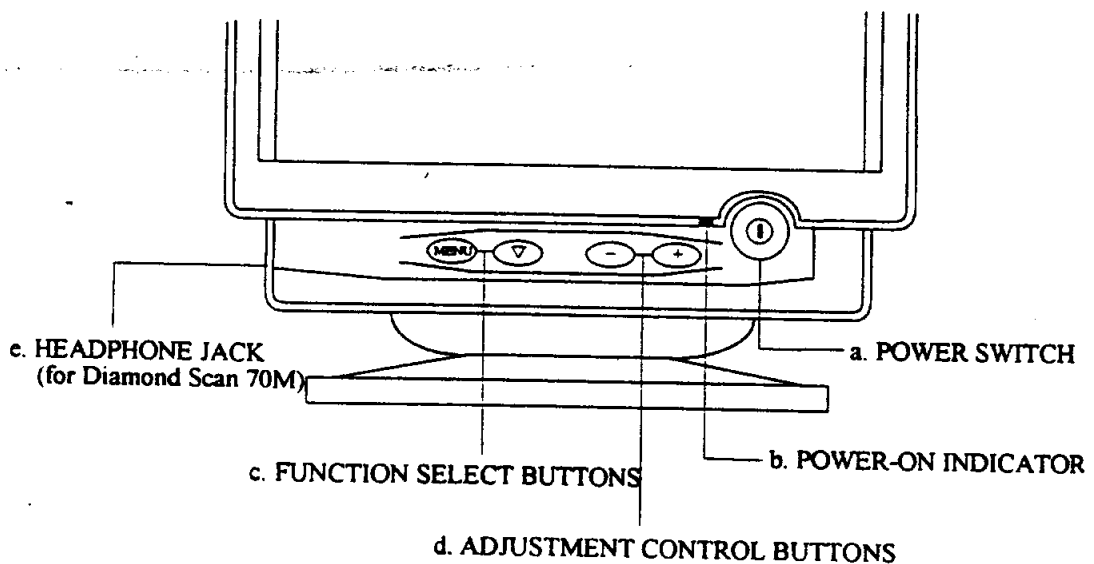
Status	LED
Power on	Green
Power saving	Amber
Over range freq.	Amber
Power off	Off

c. Function Select Button :

- Press the "MENU" Button to Select the Function Item.
(Basic , Geometry , Color , Status , Reset , OSD Off) Function item will turn RED when selected.
- Press the "▽" Button to Select control Icon Function.

d. Adjustment Control Button :

- Push the Increased "+" or Decrease "-" Button for the Desired Adjustment, All Adjustment are Memorized Automatically immediately.
- Press "+" or "-" Button to Display Brightness / Contrast MENU when OSD is off. Press "+" to select Brightness item or Press "-" to select Contrast item when OSD is off. Press "+" or "-" to Adjust Brightness / Contrast when Brightness / Contrast item Display. Press "▽" to select Contrast or Brightness item.



B. OSD (on screen display) Function Control Method

- a. Basic
 - V-Position
 - H-Position
 - V-size
 - H-size
 - V-moire
 - Degauss

- b. Geometry
 - Pincushion
 - Trapezoid
 - Parallelogram
 - Rotation

- c. Color
 - 9300 / 6500
 - Color Adjust

- d. Status

- e. Reset
 - Geometry
 - Color

- f. OSD Off

- g. Brightness / Contrast

- h. Volume (option)


FRONT PANEL FUNCTION CONTROL DESCRIPTION


OSD Function Control :


Push the "MENU" Button to select the Basic / Geometry / Color / Status / Reset / OSD Off/ Volume (option) Item.


a. Basic Function Control


Push the "▽" Button to select the "V-Position / H-Position / V-size / H-size / V-moire / Degauss /" Item.


- V-Position Control 
Press the +/- Button
+ to move up
- to move down

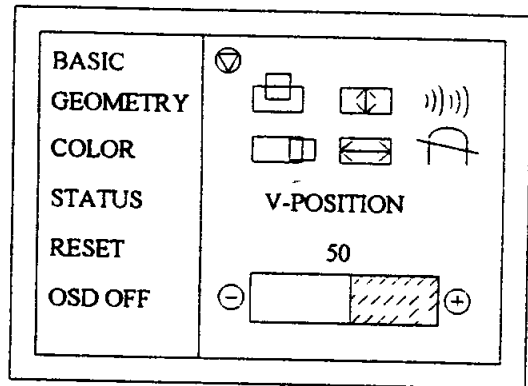
- H-Position Control 
Press the +/- Button
+.... to move right
-..... .to move left

- V-Size Control 
Press the +/- Button
+.... to enlarge
-..... to diminish

- H-Size Control 
Press the +/- Button
+.... to enlarge
-..... to diminish

- V-moire control 
Press the +/- Button to Decrease the Level of the Vertical Moire wave.


- Degauss Control 
Press the + or - Button to Produce Screen Degaussing





FRONT PANEL FUNCTION CONTROL DESCRIPTION


b. Geometry

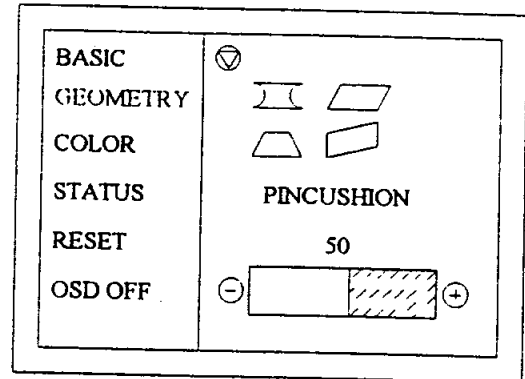
Push the "▽" to select the "Pincushion / keystone / Parallel / Rotation" item.

- Pincushion Control 
 - Press +/- Button
 - + to expand the picture side.
 - to diminish the picture side.

- Trapezoid Control 
 - Press +/- Button
 - + to expand the top side and the bottom side be diminish.
 - to diminish the top side and the bottom side be expand.

- Parallelogram 
 - Press +/- Button
 - + the top side shift right and the bottom side shift left.
 - the top side shift left and the bottom side shift right.

- Rotation 
 - Press +/- Button
 - + to rotate clock wise
 - to rotate counterclockwise

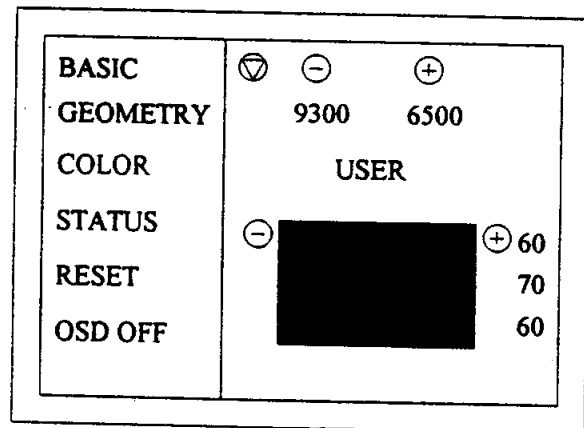


c. Color Control

Press the "▽" Button to select "9300 / 6500 , R/G/B color " item.

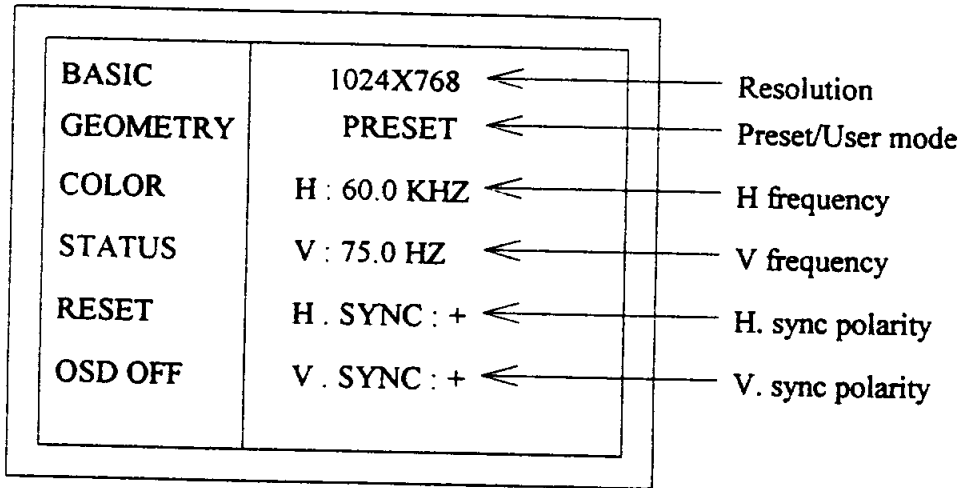
- 9300 / 6500 Item
 - Press +/- Button
 - + select 6500
 - select 9300

- R/G/B Color
 - Press +/- Button
 - + color gain increase
 - color gain decrease



FRONT PANEL FUNCTION CONTROL DESCRIPTION

d. STATUS



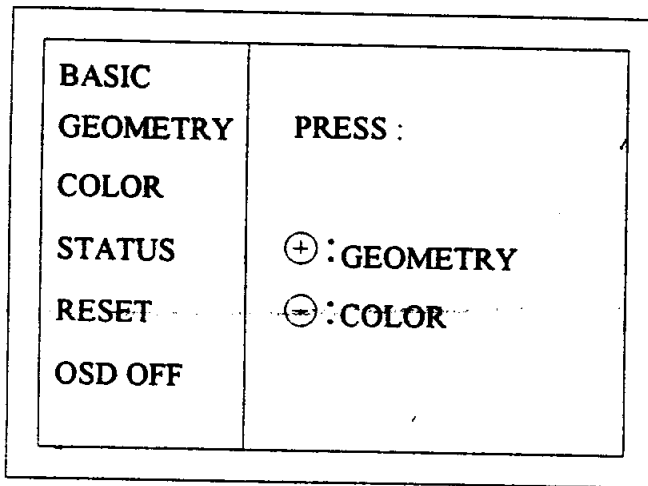
Note : It show preset mode when resolution is displayed,if not it shows users mode.

e. RESET

Press +/- Button

+ Reset Geometry

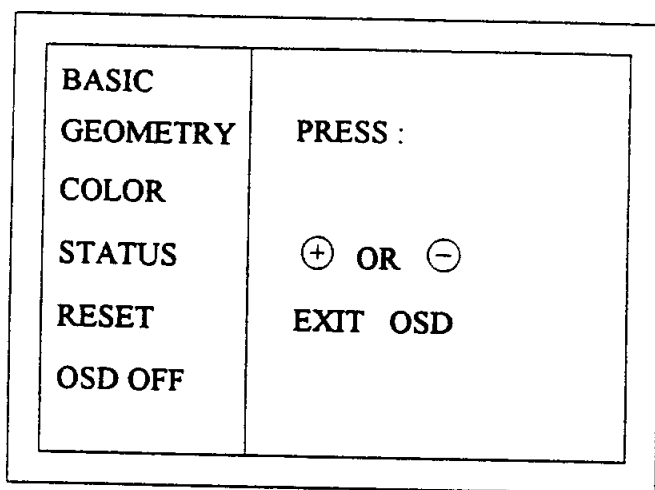
- Reset Color



FRONT PANEL FUNCTION CONTROL DESCRIPTION

f. OSD Off

- Press + or - Button EXIT OSD
- The screen will clear automatically about 30 seconds after stop operating OSD menu.
- Press "MENU" and "▽" Button to EXIT OSD.

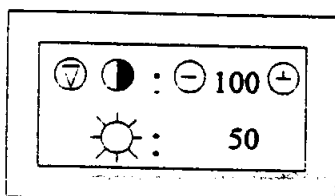


g. Contrast / Brightness Control

Push "▽" Button to select Contrast / Brightness item.

Press +/- Button

- + for increase Contrast (Brightness)
- for decrease Contrast (Brightness)



Note : OSD will shut down when Contrast / Brightness after stop operating for 5 seconds.

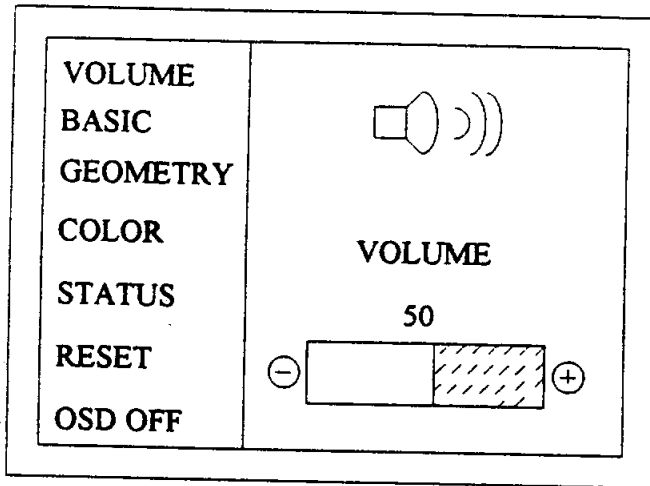
FRONT PANEL FUNCTION CONTROL DESCRIPTION

h. Volume control (for SD7704CM)

Press the + / - Button

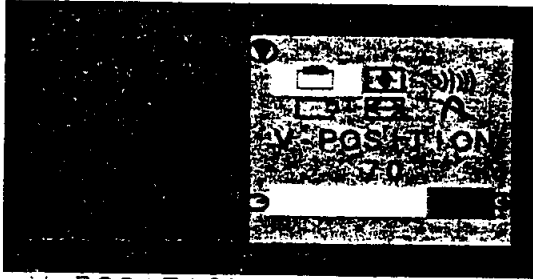
+ for increase volume

- for decrease volume



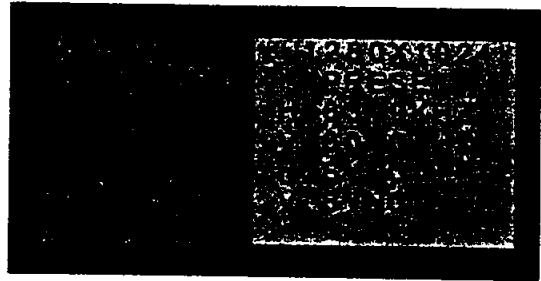
FRONT PANEL FUNCTION CONTROL DESCRIPTION

BASIC

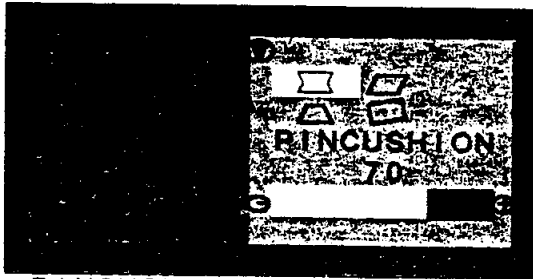


V-POSITION V-MCIRE
 H-POSITION DEGUASS
 V-SIZE
 H-SIZE

STATUS

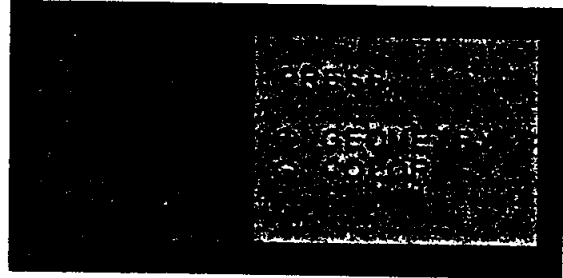


GEOMETRY

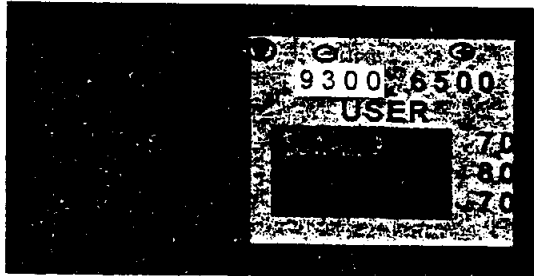


PINCUSHION
 TRAPEZOID
 PARALLEL
 ROTATION

RESET

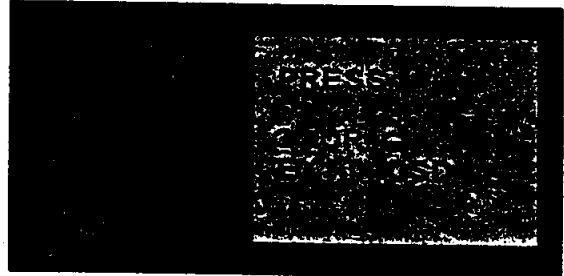


COLOR

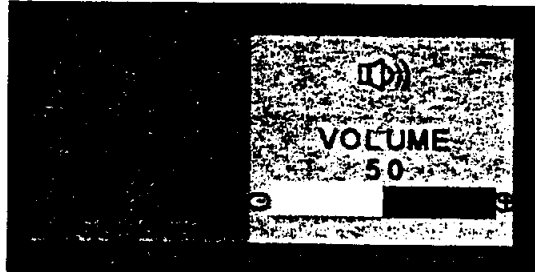


9300 K
 6500 K
 R,G,B ADJUST

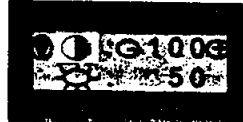
OSD OFF



VOLUME (OPTION)

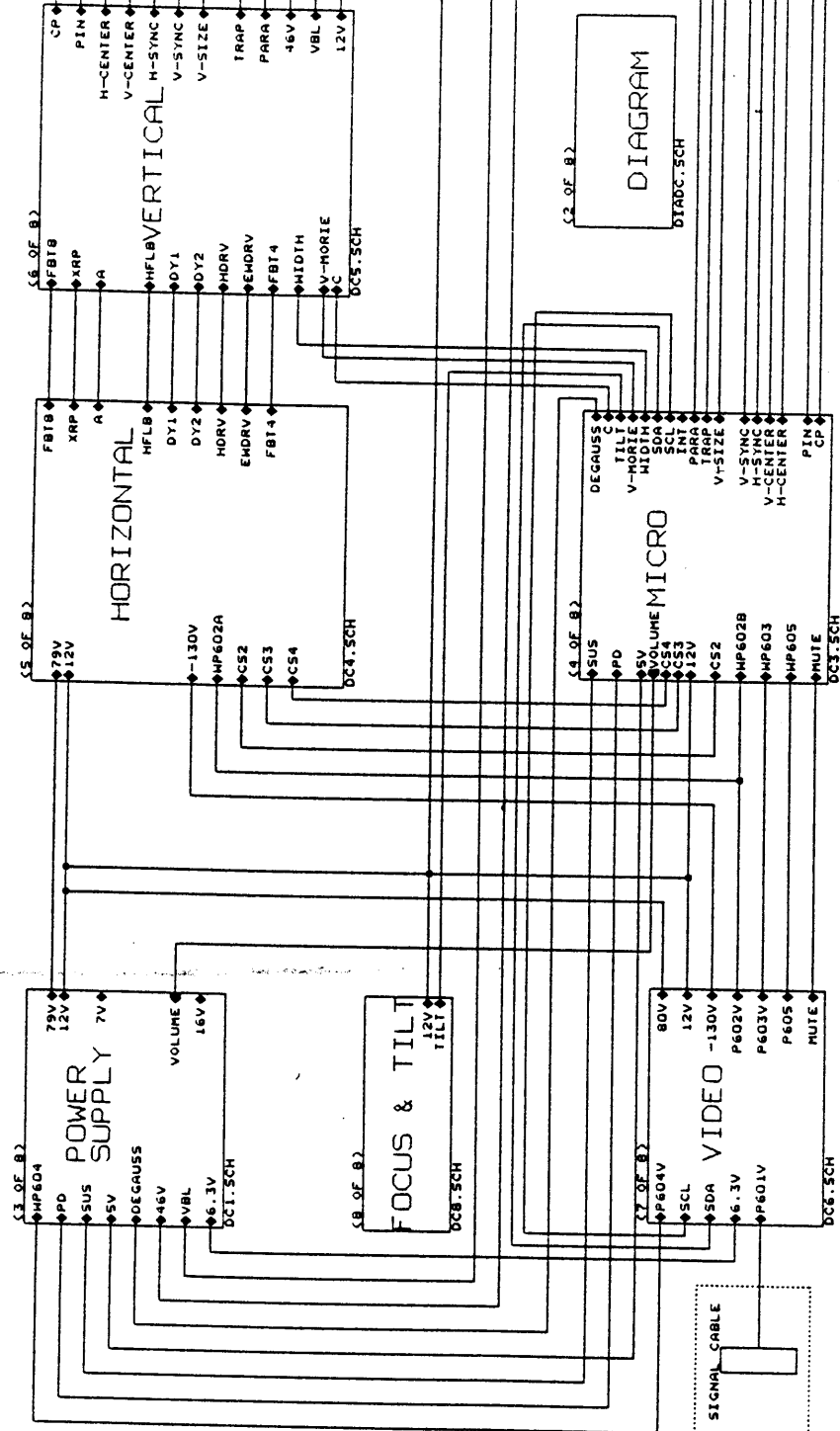


CONTRAST & BRIGHTNESS

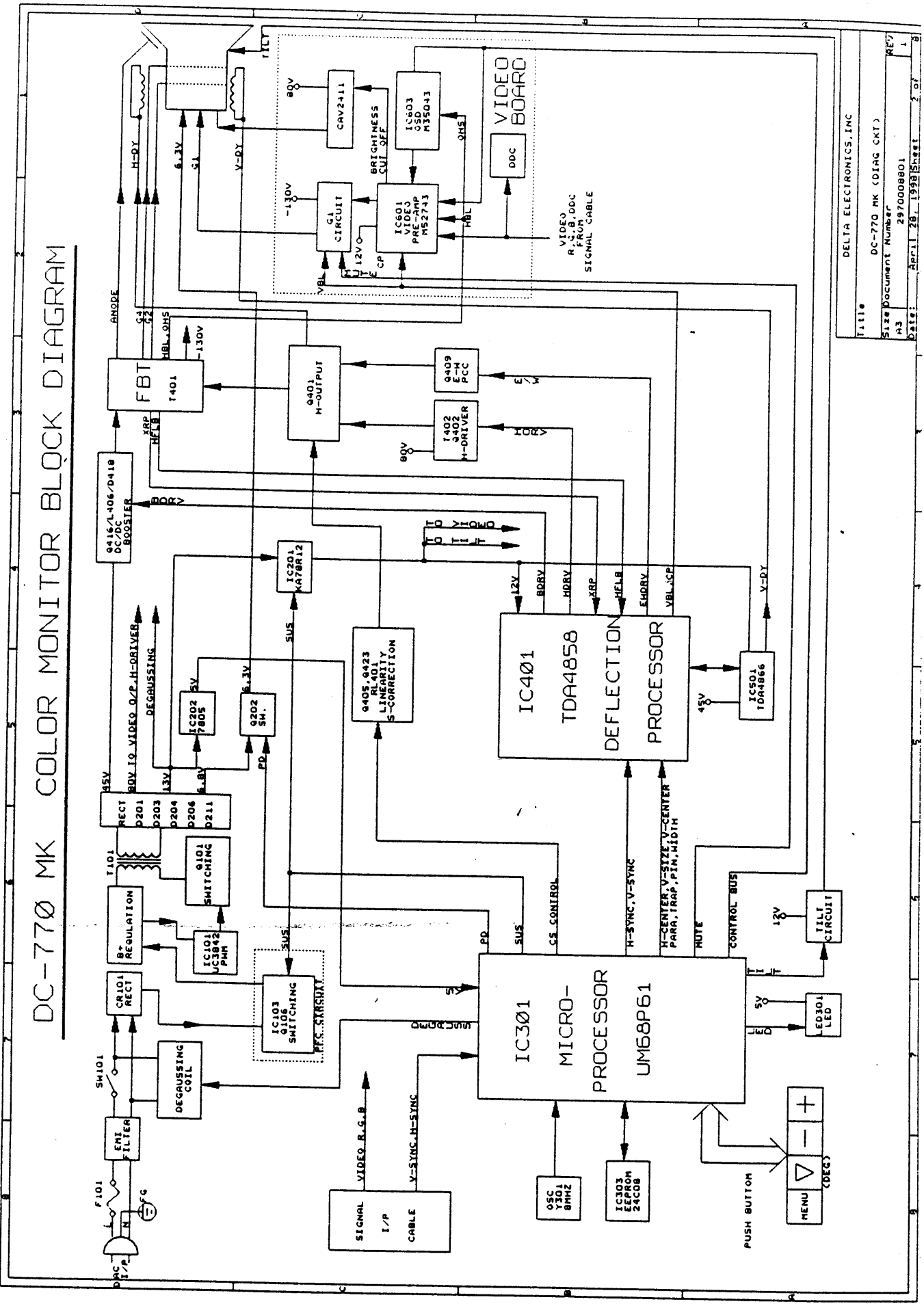


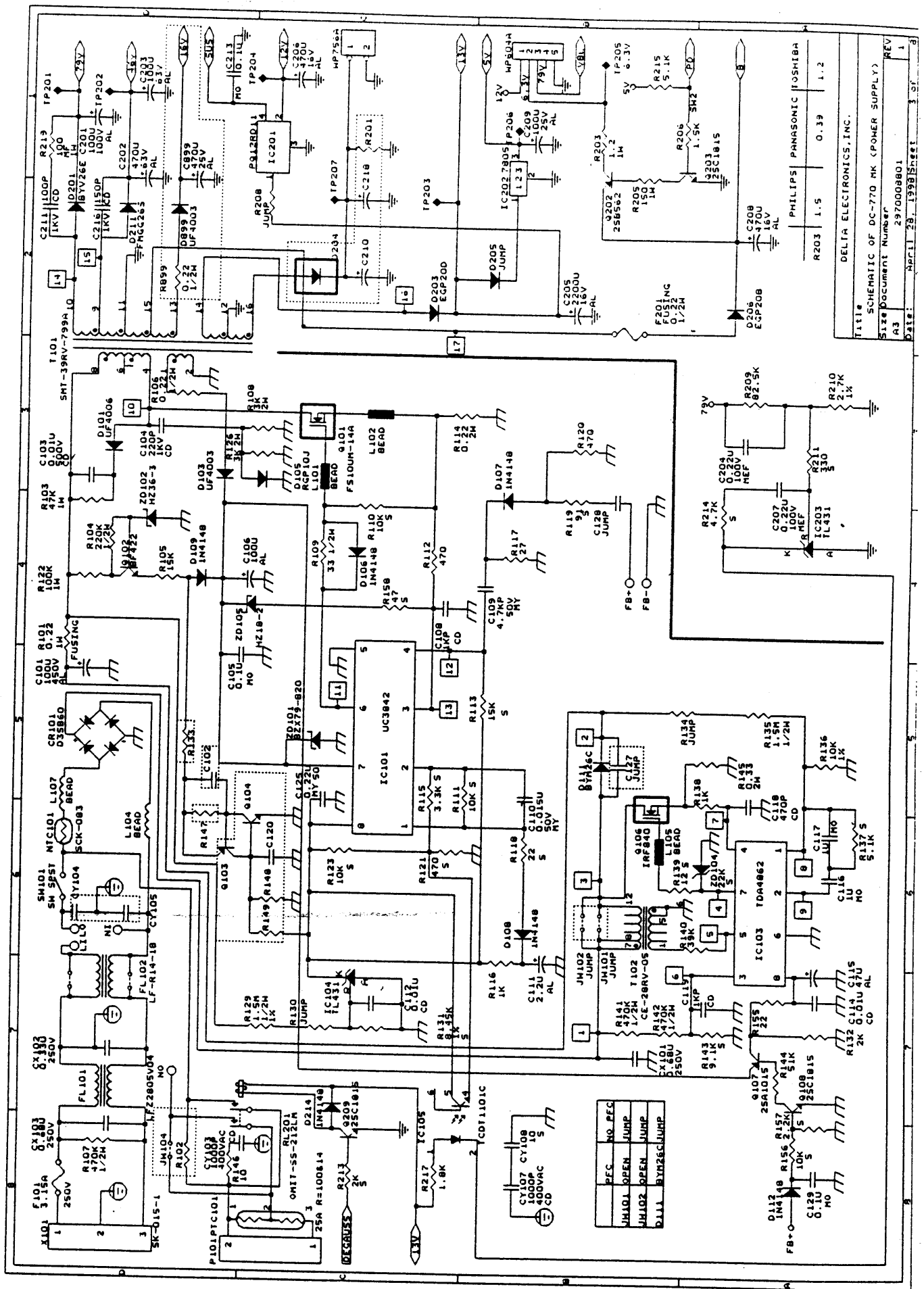
SELECT     ADJUST

DC-770MK



DC-770 MK COLOR MONITOR BLOCK DIAGRAM

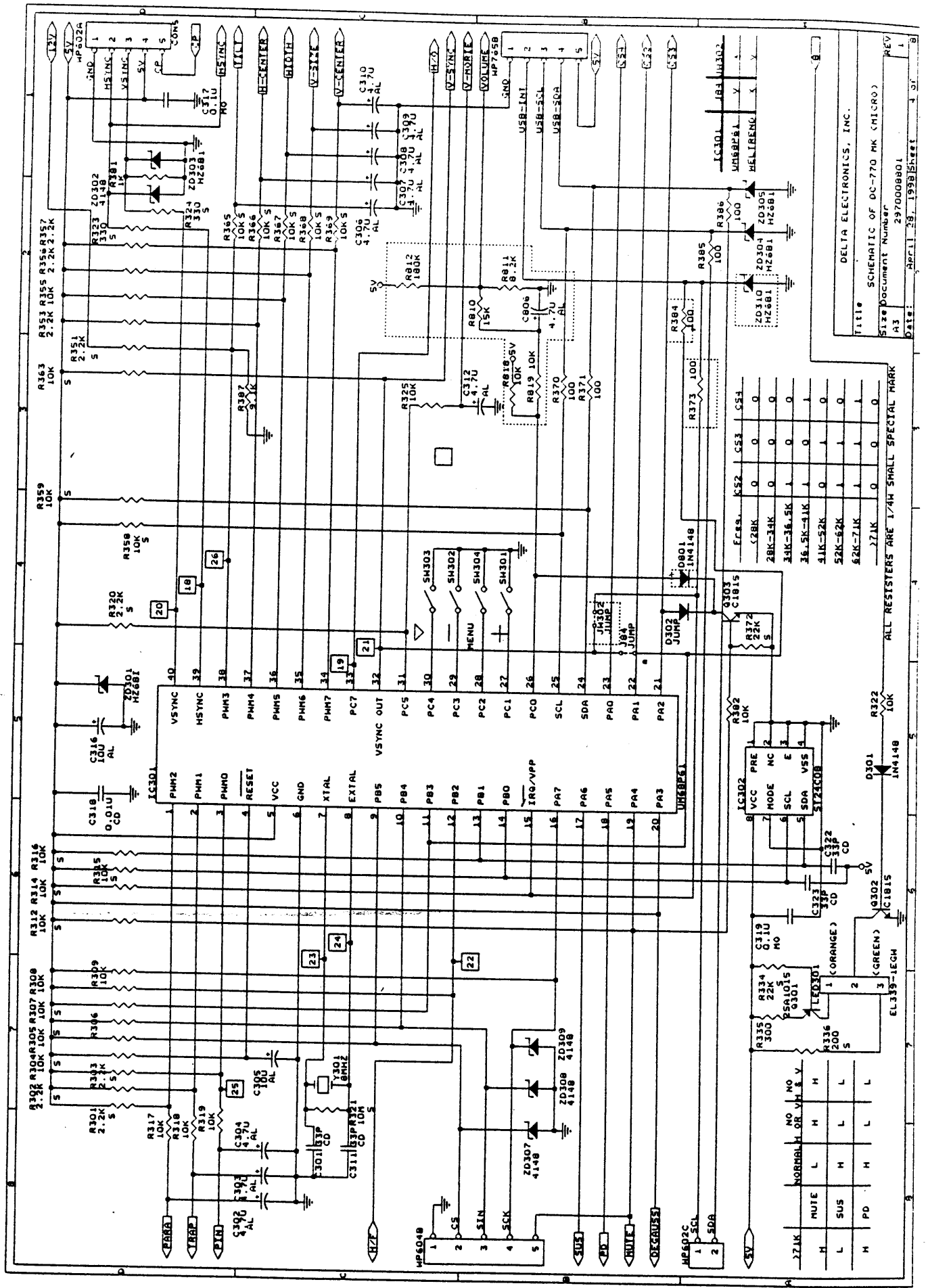




DEC	NO	REC
JH101	OPEN	JUMP
JH102	OPEN	JUMP
D111	BY282	JUMP

TITLE
 SCHEMATIC OF DC-770 MK (POWER SUPPLY)
 SIZE Document Number
 03
 DATE: April 28, 1999
 Sheet 3 of 3
 REV 1

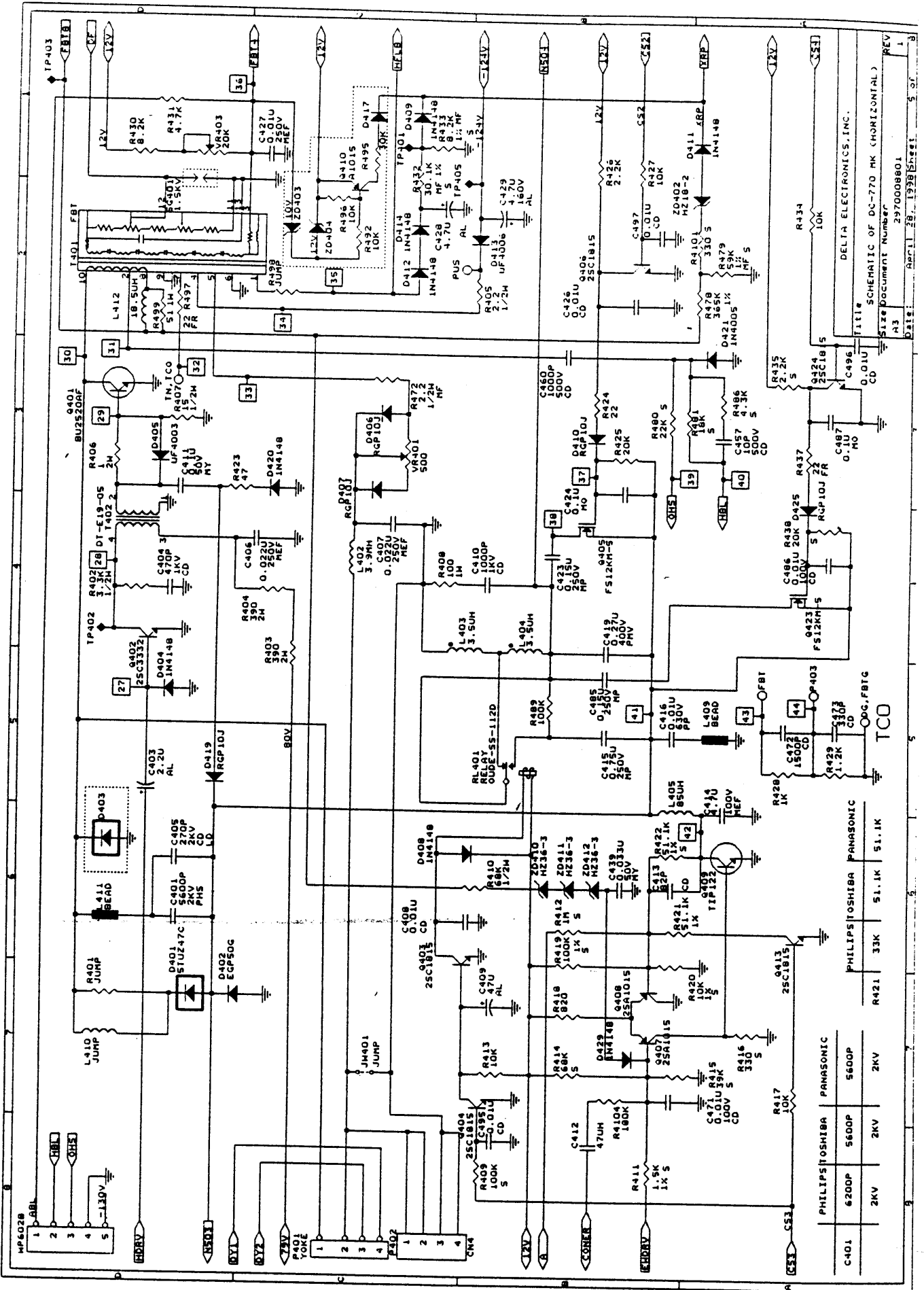
PHILIPS PANASONIC TOSHIBA
 R203 1.5 0.39 1.2
 DELTA ELECTRONICS, INC.



RESISTOR VALUE	R321	R322	R323	R324	R325	R326
2.2K	0	0	0	0	0	0
10K	0	0	0	0	0	0
15K	0	0	0	0	0	0
20K	0	0	0	0	0	0
25K	0	0	0	0	0	0
30K	0	0	0	0	0	0
35K	0	0	0	0	0	0
40K	0	0	0	0	0	0
45K	0	0	0	0	0	0
50K	0	0	0	0	0	0
55K	0	0	0	0	0	0
60K	0	0	0	0	0	0
65K	0	0	0	0	0	0
70K	0	0	0	0	0	0
75K	0	0	0	0	0	0
80K	0	0	0	0	0	0
85K	0	0	0	0	0	0
90K	0	0	0	0	0	0
95K	0	0	0	0	0	0
100K	0	0	0	0	0	0

Title: SCHEMATIC OF DC-770 MK (MICRO)
 Size: Document Number 2970008801
 Date: APR 11 2019 10:58:57
 Delta Electronics, Inc.

ALL RESISTORS ARE 1/4W 5% TOLERANCE



PHILIPS	TOSHIBA	PANASONIC
C401	6200P	5600P
	2K	2K
R421	33K	51.1K
	51.1K	51.1K
PHILIPS	TOSHIBA	PANASONIC
R421	33K	51.1K
	51.1K	51.1K

PHILIPS	TOSHIBA	PANASONIC
R429	1.2K	33K
	1.2K	33K
C429	0.01uF	5600P
	0.01uF	5600P
C429	0.01uF	5600P
	0.01uF	5600P

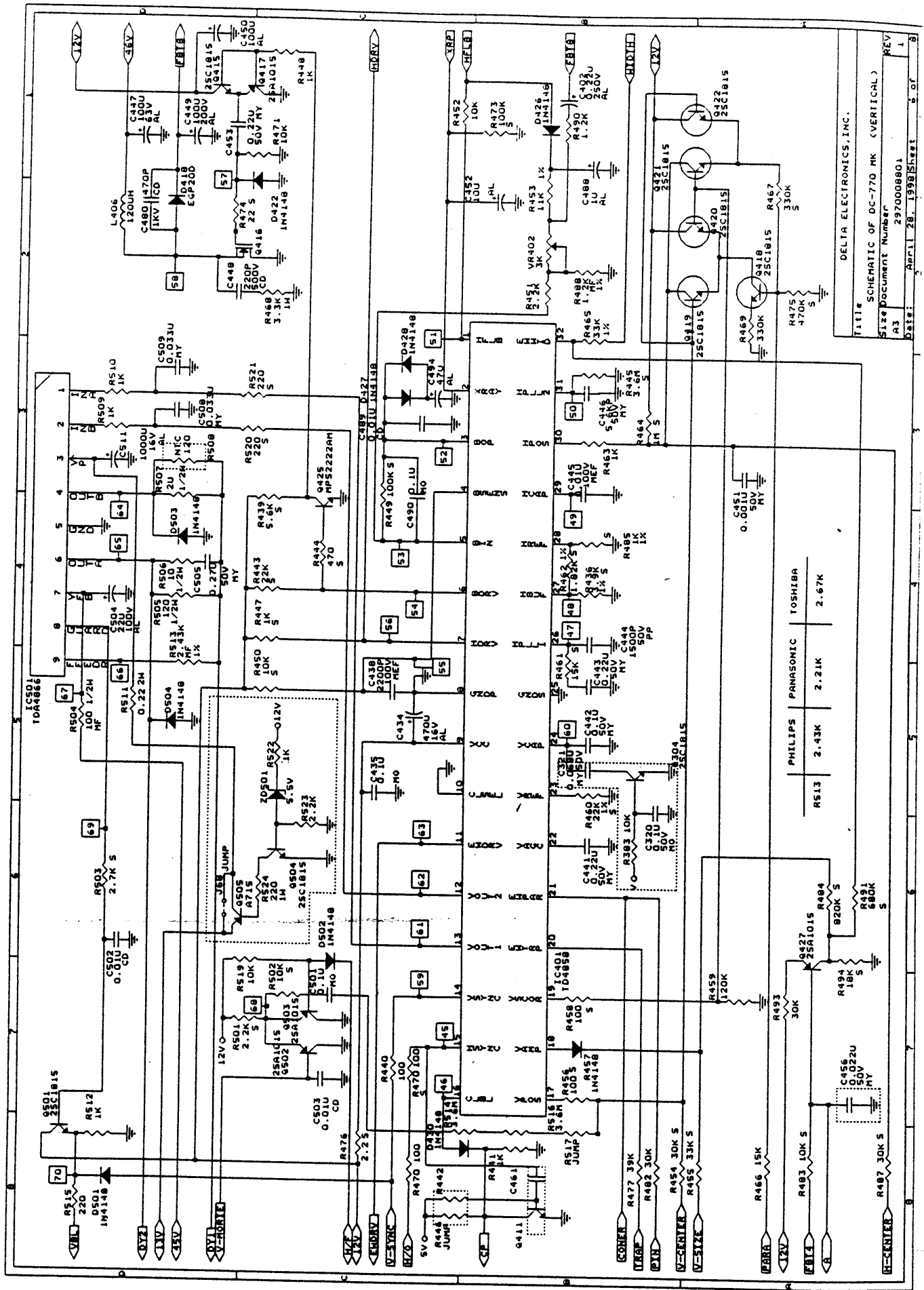
C426	0.01uF	5600P
	0.01uF	5600P
C426	0.01uF	5600P
	0.01uF	5600P
C426	0.01uF	5600P
	0.01uF	5600P

R426	2.2K	5600P
	2.2K	5600P
R426	2.2K	5600P
	2.2K	5600P
R426	2.2K	5600P
	2.2K	5600P

R426	2.2K	5600P
	2.2K	5600P
R426	2.2K	5600P
	2.2K	5600P
R426	2.2K	5600P
	2.2K	5600P

R426	2.2K	5600P
	2.2K	5600P
R426	2.2K	5600P
	2.2K	5600P
R426	2.2K	5600P
	2.2K	5600P

SIZE DOCUMENT NUMBER 297000801
 DATE April 28, 1978 Sheet 5 of 9
 REV 1
 SCHEMATIC OF DC-770 MK (HORIZONTAL)
 DELTA ELECTRONICS, INC.



DELTA ELECTRONICS, INC.

SCHEMATIC OF DC-770 MK (VERTICAL)

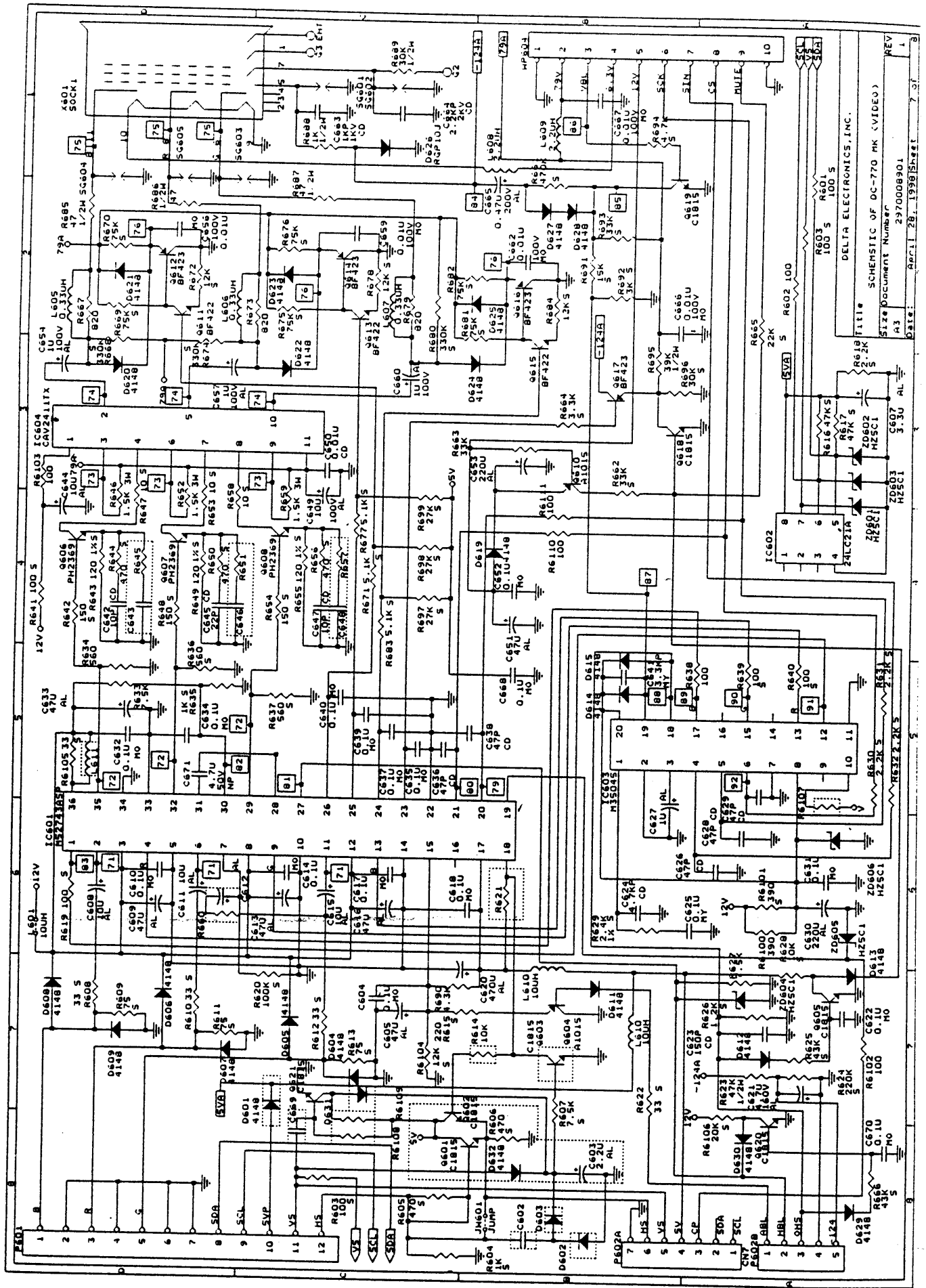
Size Document Number 297000801

REV 1

Date: April 28, 1958 Sheet 6 of 7

PHILIPS	PANASONIC	TOSHIBA
RS13	2.43K	2.21K
		2.67K

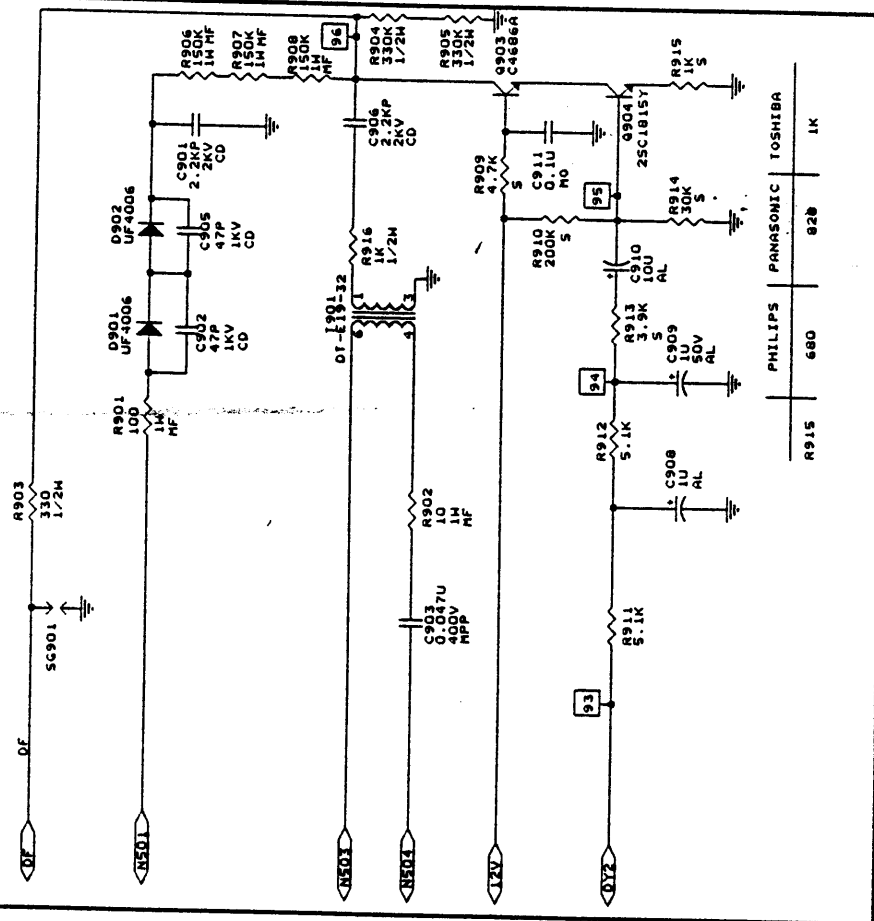
PHILIPS	PANASONIC	TOSHIBA
RS13	2.43K	2.21K
		2.67K



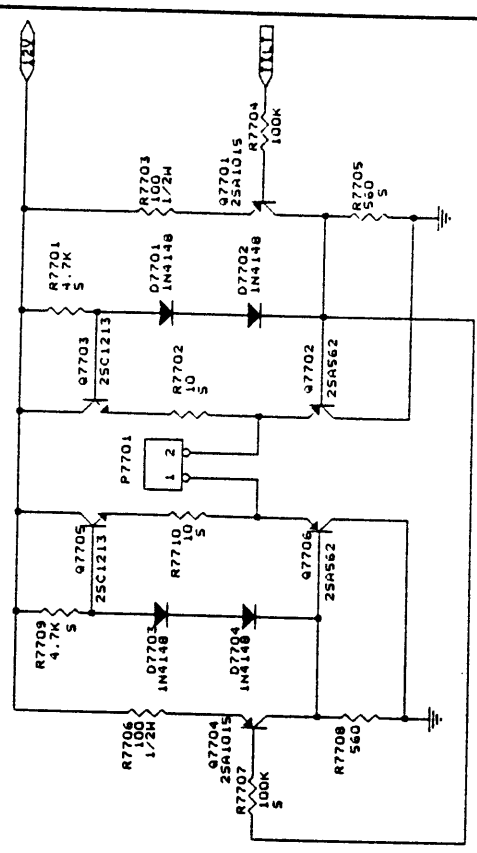
DELTA ELECTRONICS, INC.
SCHEMATIC OF DC-770 MK (VIDEO)
SIZE Document Number 2970008901
Date: April 28, 1998 Sheet 7 of 8

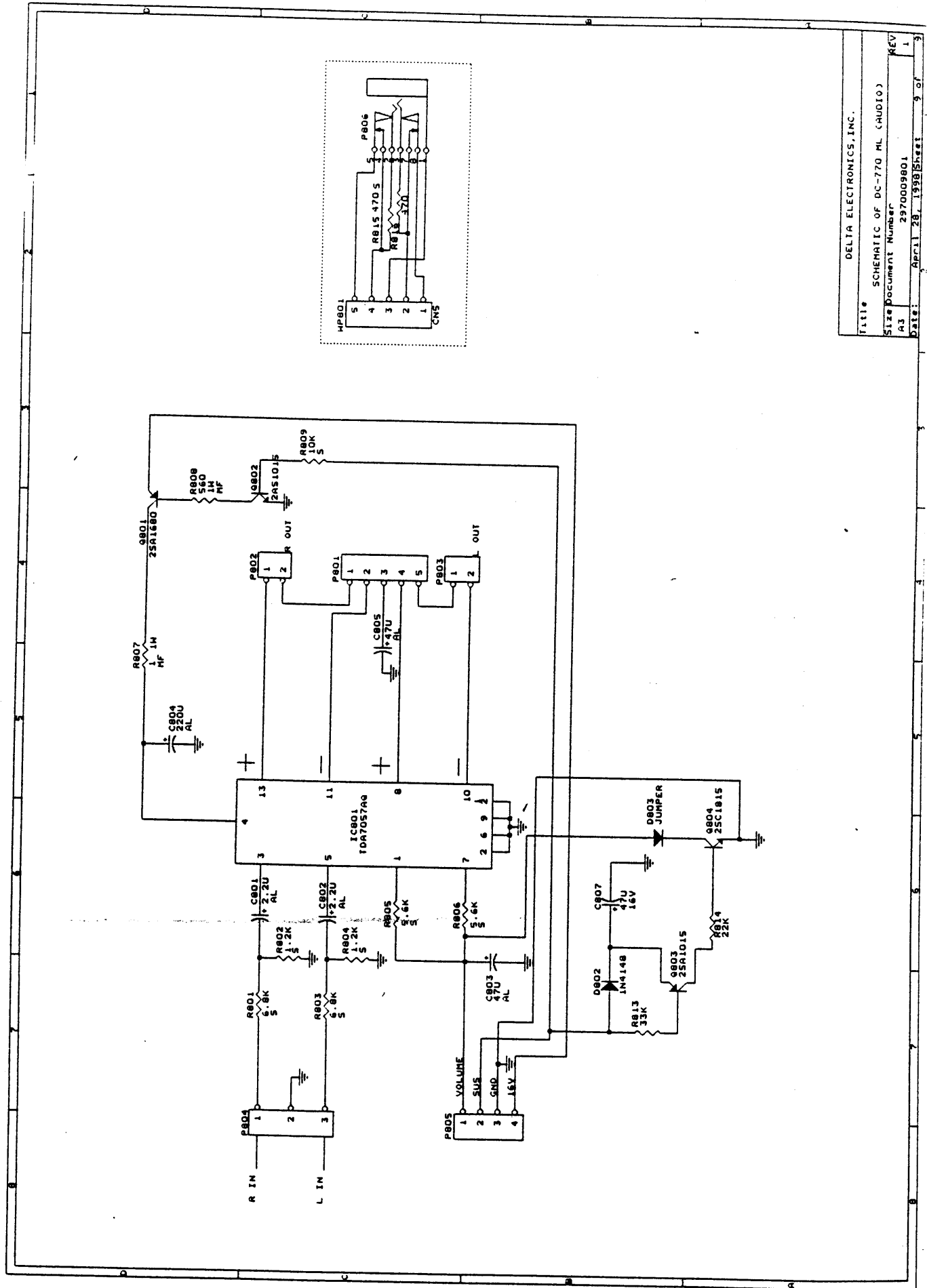
REV 1
1

FOCUS



TILT

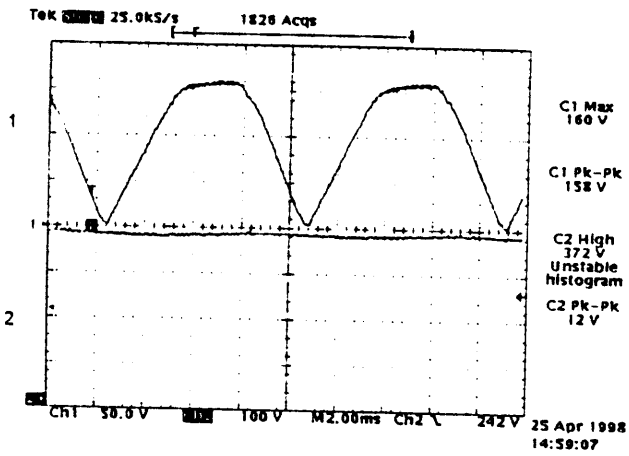




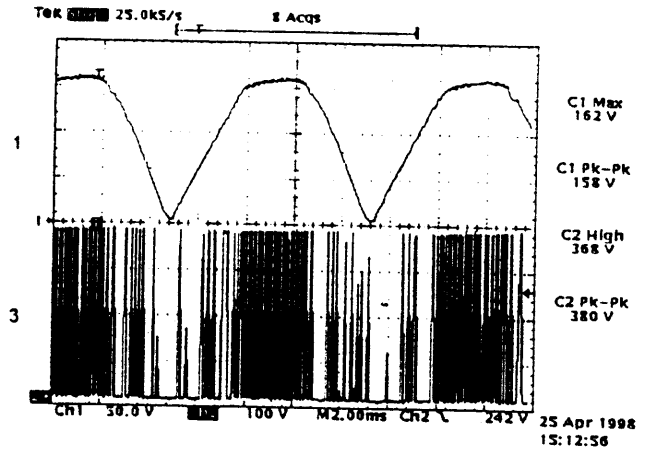
POWER SUPPLY CKT WAREFORM

INPUT : 110VAC VESA 1024x768 69KHz/85Hz

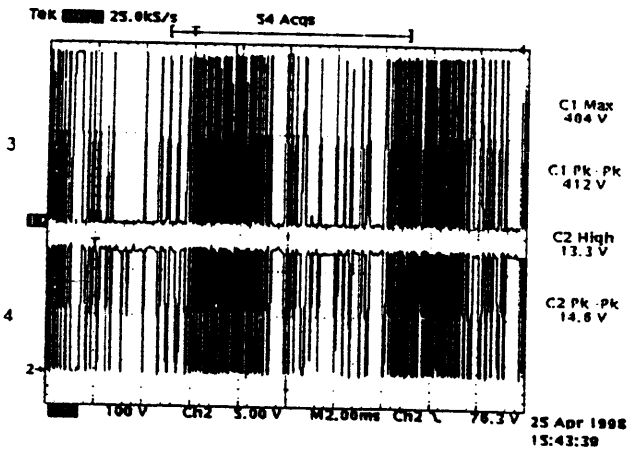
CH1 : CX101
CH2 : C101



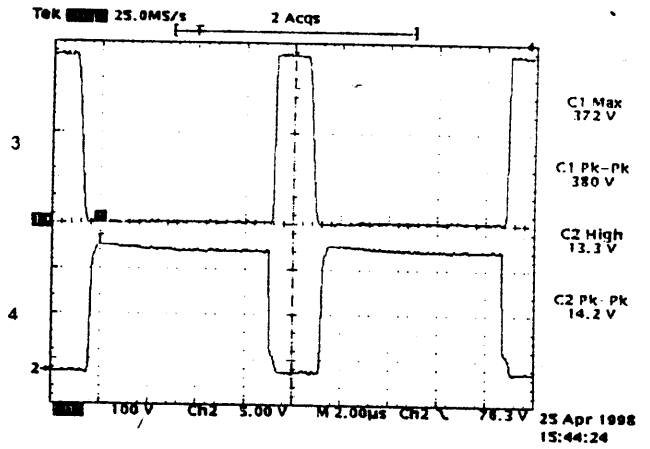
CH1 : CX101
CH2 : Q106 "D"



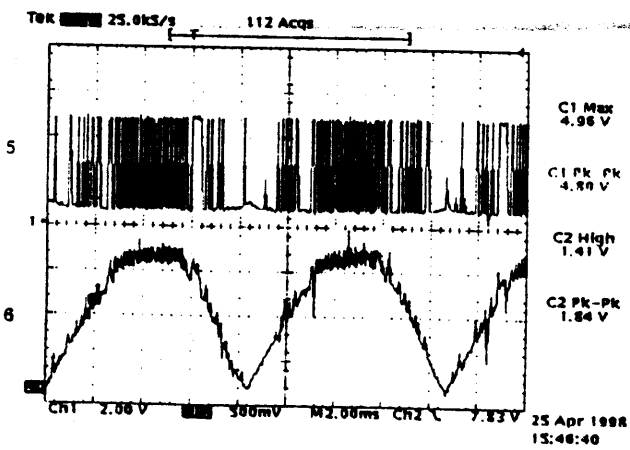
CH1 : Q106 "D"
CH2 : IC103 PIN7



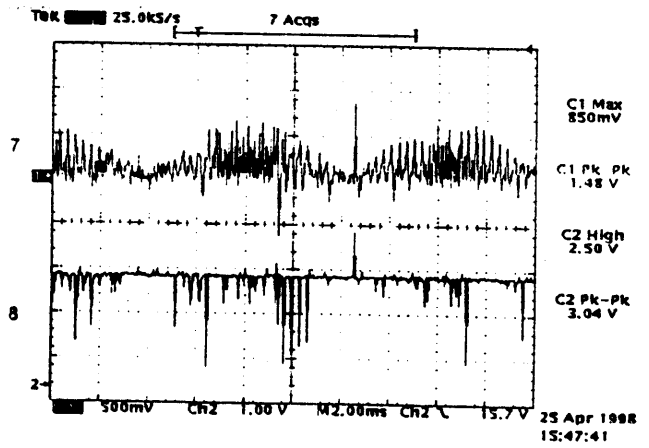
CH1 : Q106 "D"
CH2 : IC103 PIN7



CH1 : IC103 PIN5
CH2 : IC103 PIN3



CH1 : IC103 PIN4
CH2 : IC103 PIN1

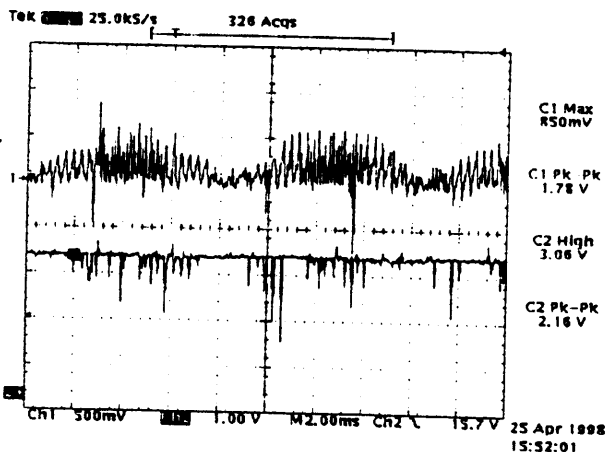


POWER SUPPLY CKT WAREFORM

VFSA 1024x768 69KHz/85Hz

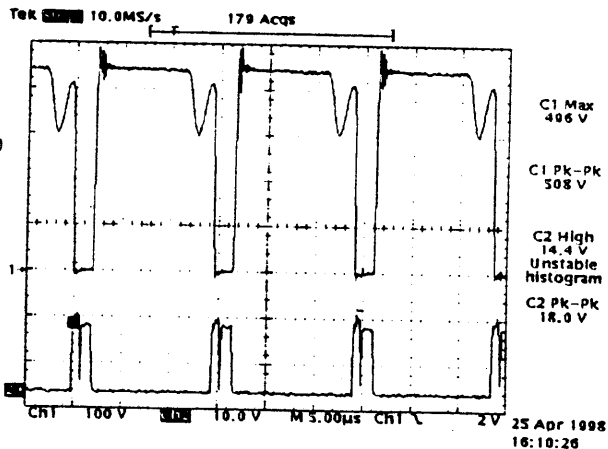
CH1: IC103 PIN4

CH2: IC103 PIN2



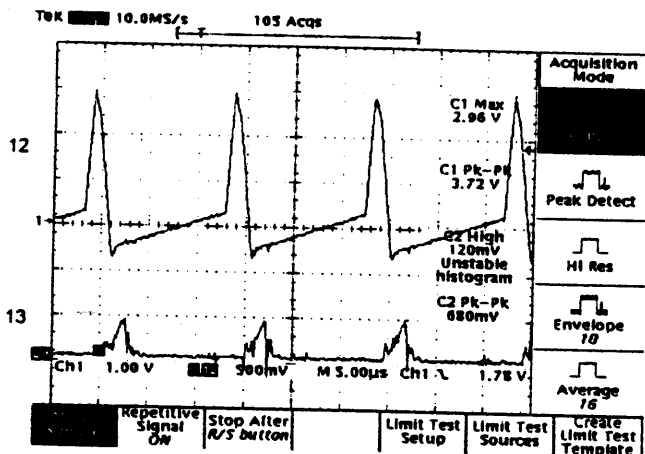
CH1: Q101 "D"

CH2: IC101 PIN6



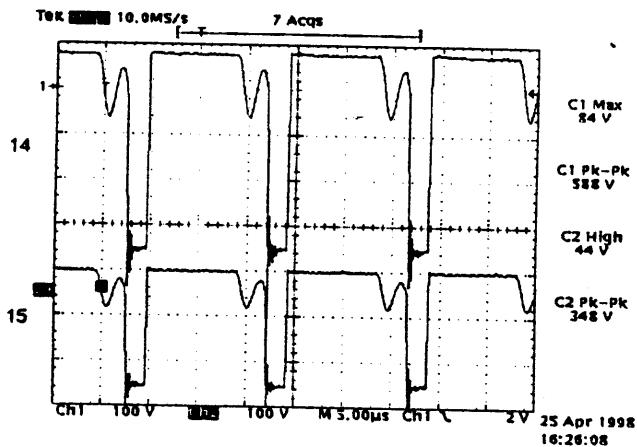
CH1: IC101 PIN4

CH2: IC101 PIN3



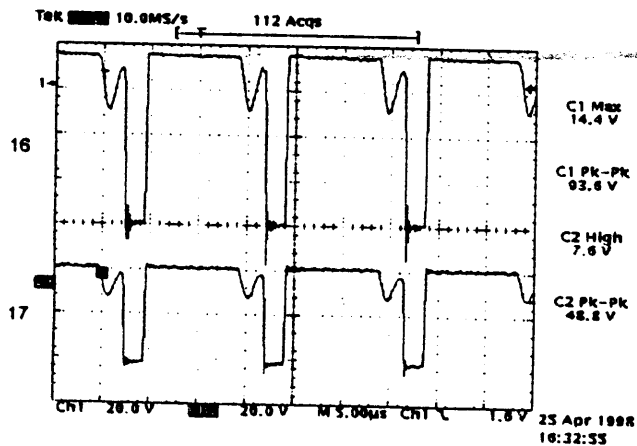
CH1: T101 PIN10

CH2: T101 PIN9



CH1: T101 PIN14

CH2: T101 PIN15

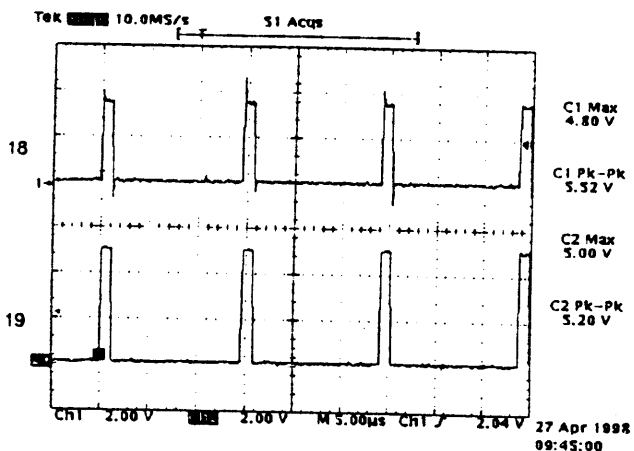


MICRO CKT WAREFORM

VESA 1024x768 69KHz/85Hz

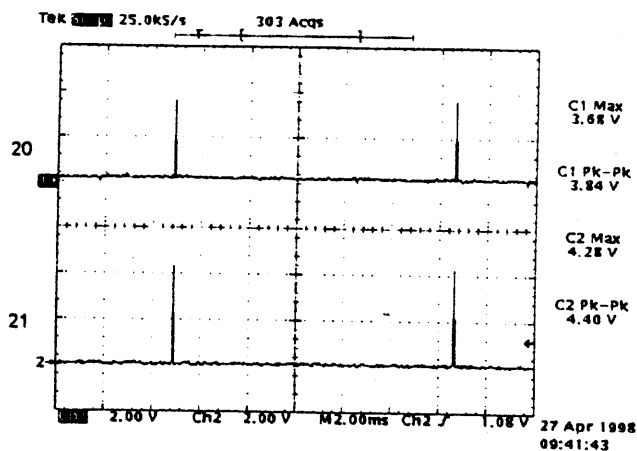
CH1 : IC301 PIN39 H-SYNC

CH2 : IC301 PIN33 H/O



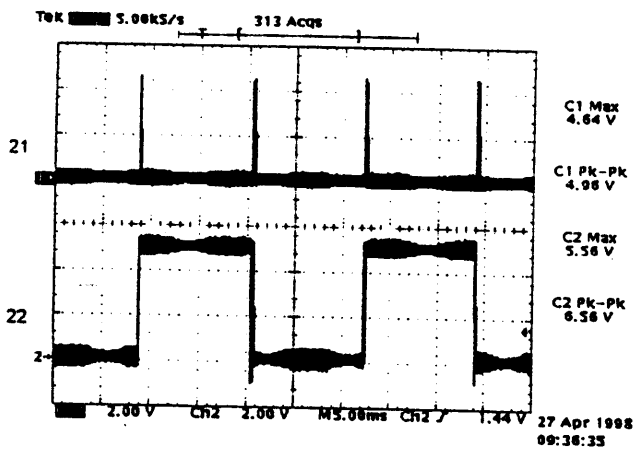
CH1 : IC301 PIN40 V-SYNC

CH2 : IC301 PIN32 V-SYNC



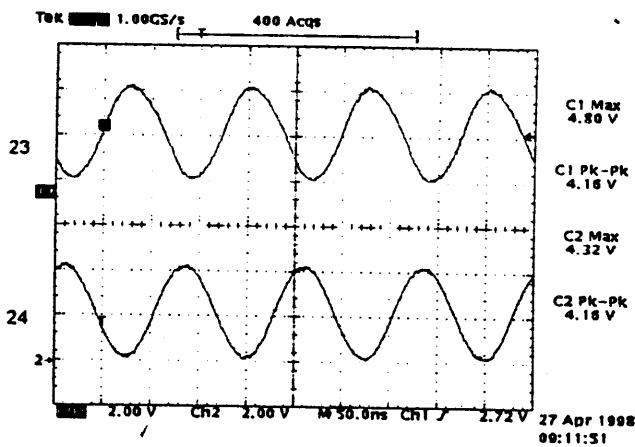
CH1 : IC301 PIN32 V-SYNC

CH2 : IC301 PIN12 H/F



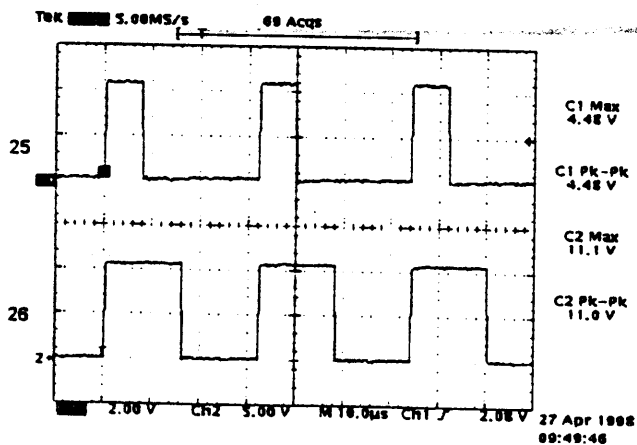
CH1 : IC301 PIN7 XTAL

CH2 : IC301 PIN8 EXTAL



CH1 : IC301 PIN3 PWM0 (+5V)

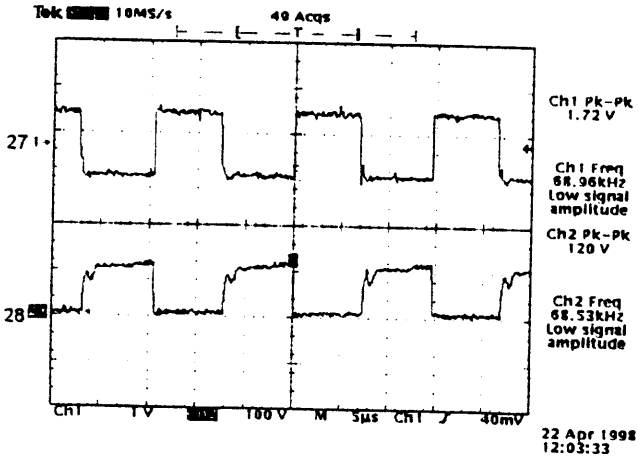
CH2 : IC301 PIN38 PWM3 (+12V)



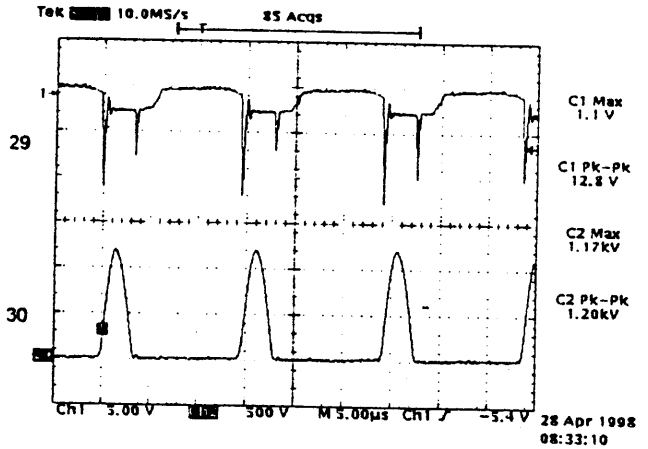
HORIZONTAL CKT WAREFORM

VESA 1024x768 69KHz/85Hz

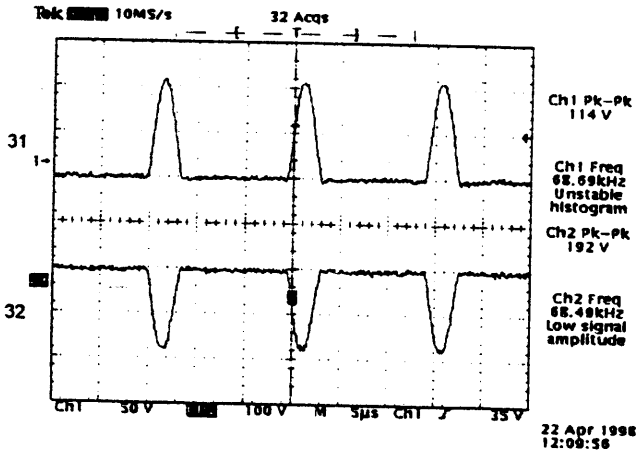
CH1 : Q402 "B"
CH2 : Q402 "C" (T402 PIN4)



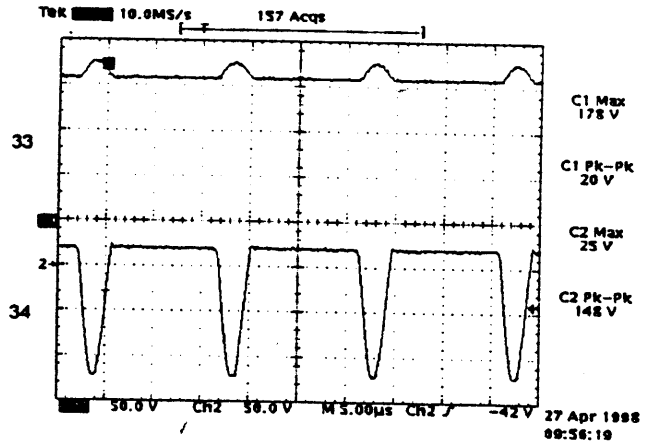
CH1 : Q401 "B"
CH2 : Q401 "C"



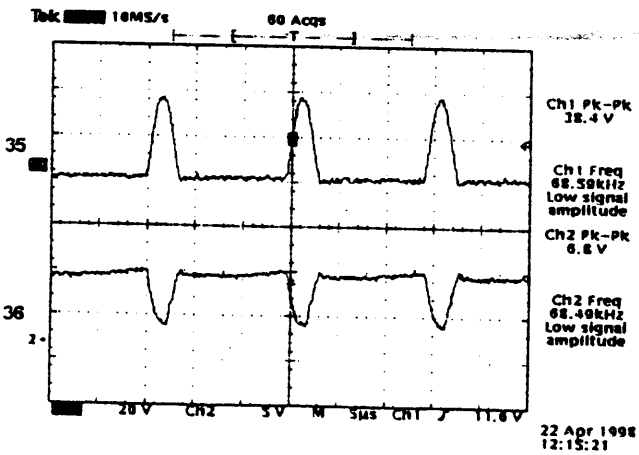
CH1 : T401 PIN2
CH2 : T401 PIN7 (TCO)



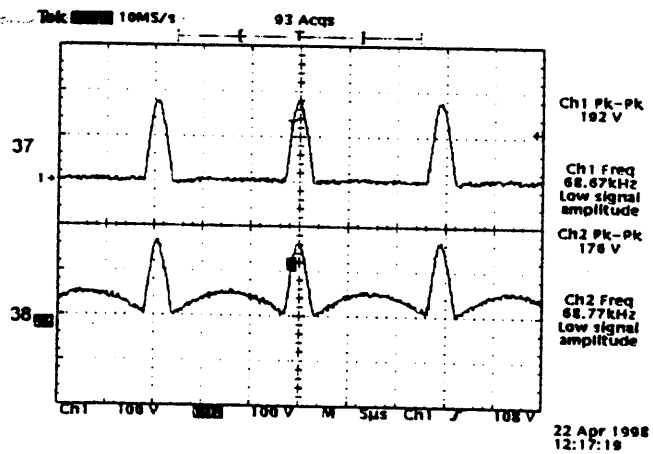
CH1 : T401 PIN5
CH2 : T401 PIN4



CH1 : T401 PIN1
CH2 : T401 PIN3



CH1 : Q405 "G"
CH2 : Q405 "D"

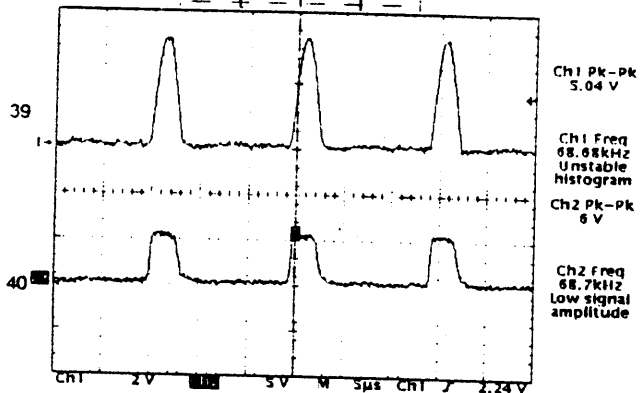


HORIZONTAL CKT WAREFORM

VESA 1024x768 69KHz/85Hz

CH1 : OHS
CH2 : HBL

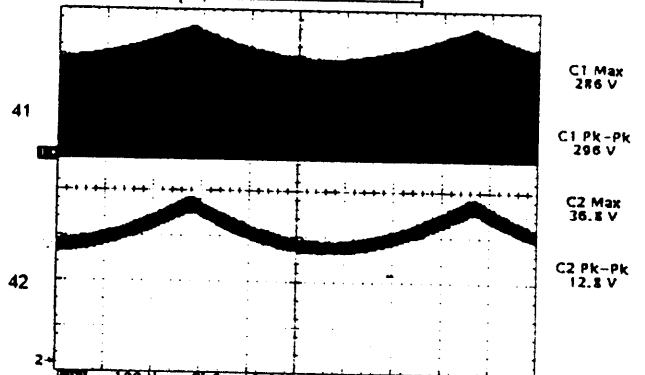
Tek 10MS/s 12 Acqs



22 Apr 1998 12:20:39

CH1 : C416
CH2 : C414

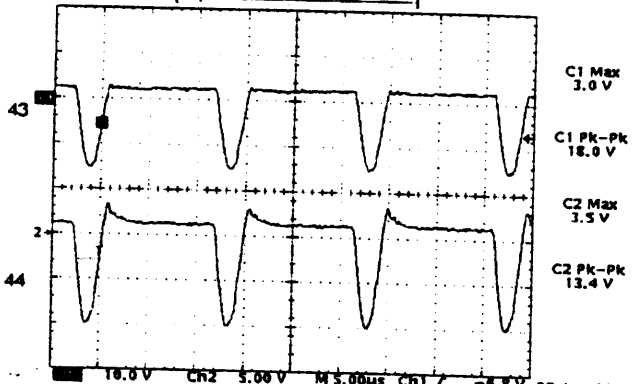
Tek 12.5KS/s 31 Acqs



27 Apr 1998 10:22:39

CH1 : FBT (TCO)
CH2 : P403

Tek 10.0MS/s 521 Acqs



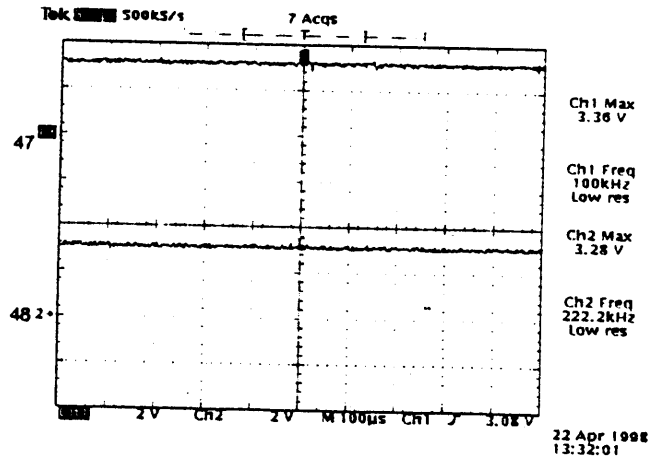
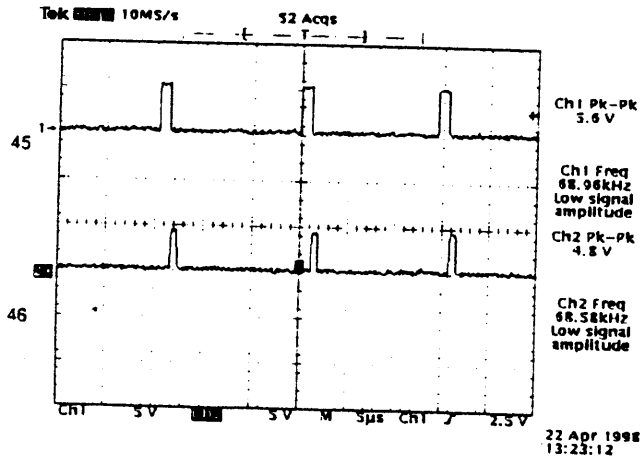
28 Apr 1998 09:11:14

VERTICAL CKT WAREFORM

VESA 1024x768 69KHz/85Hz

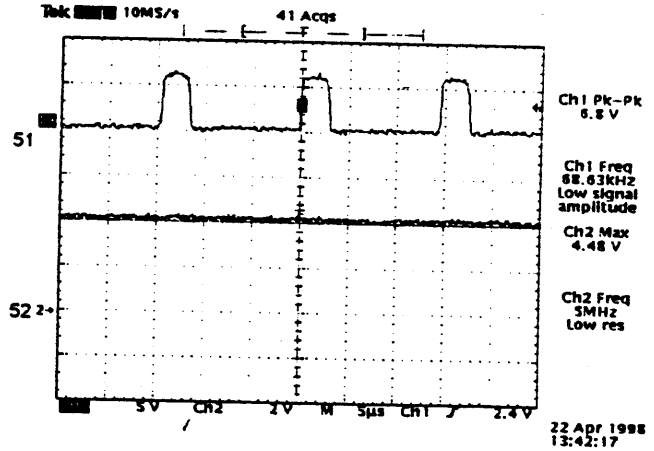
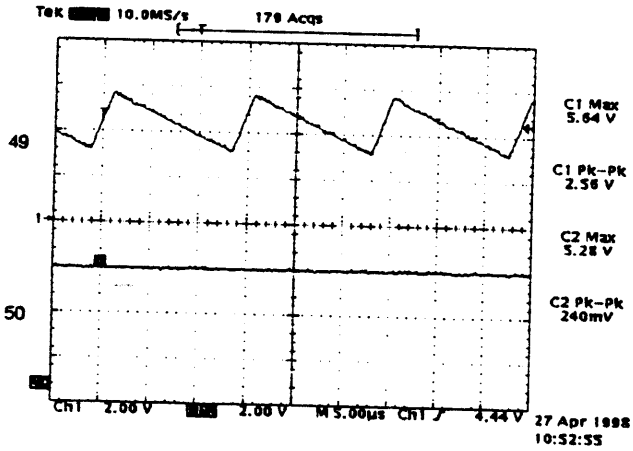
CH1 : IC401 PIN15
CH2 : IC401 PIN16 (CLBL)

CH1 : IC401 PIN26 (HPPL1)
CH2 : IC401 PIN27



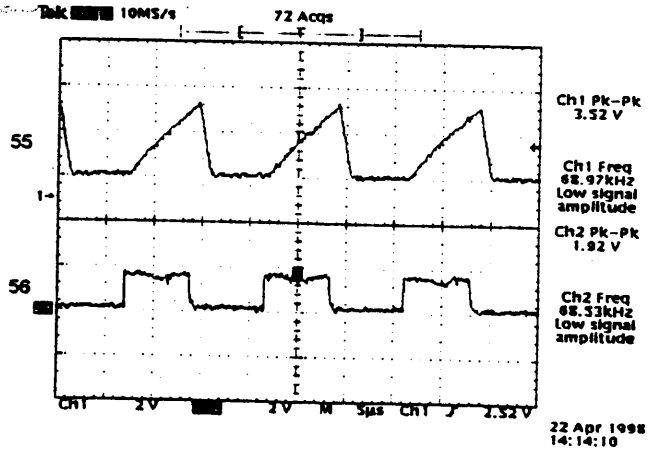
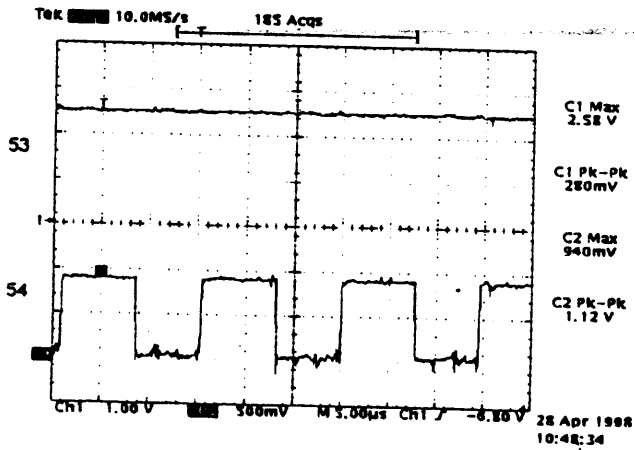
CH1 : IC401 PIN29 (HCAP)
CH2 : IC401 PIN31 (HPLL2)

CH1 : IC401 PIN1 (HFLB)
CH2 : IC401 PIN3 (BOP)



CH1 : IC401 PIN5
CH2 : IC401 PIN6

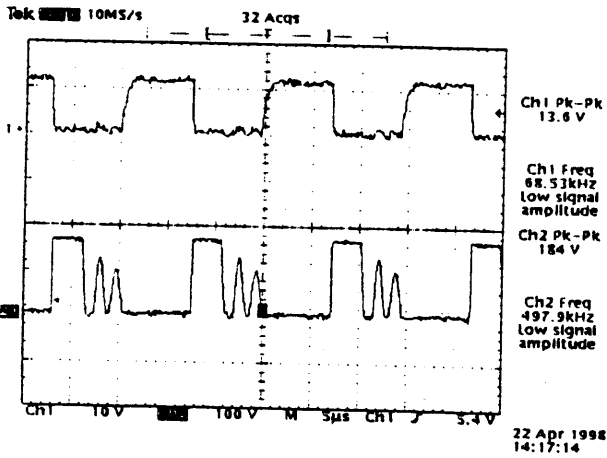
CH1 : IC401 PIN4
CH2 : IC401 PIN7



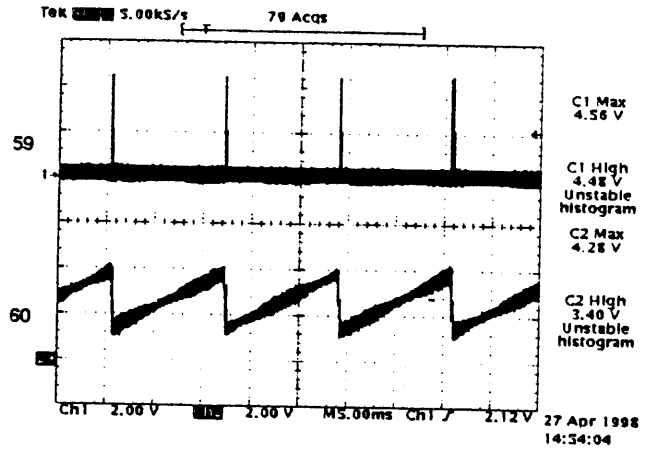
VERTICAL CKT WAREFORM

VESA 1024x768 69KHz/85Hz

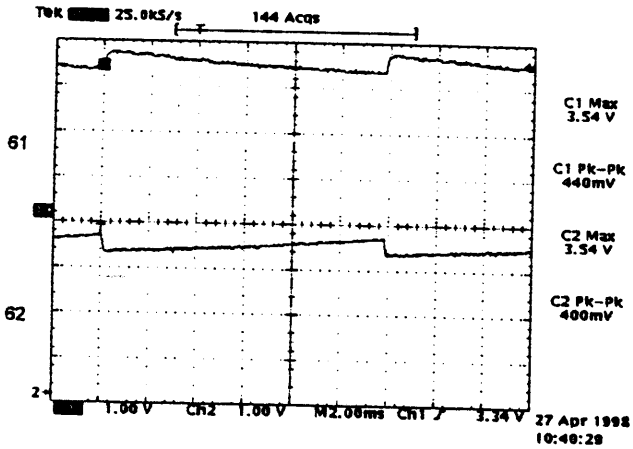
CH1 : D422
CH2 : Q416 "D"



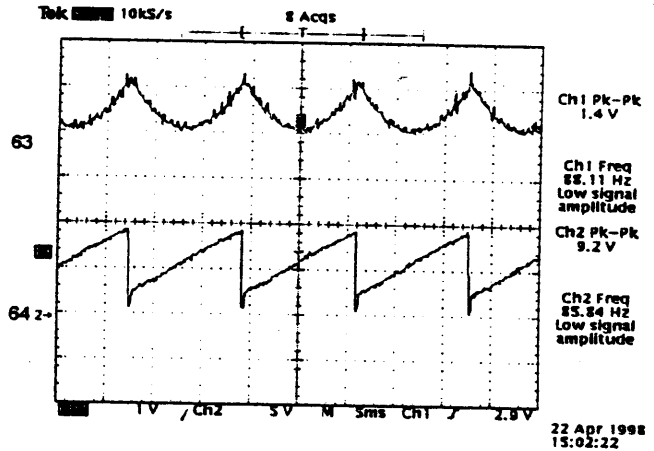
CH1 : IC401 PIN14 (V-SYNC)
CH2 : IC401 PIN24 (VCAP)



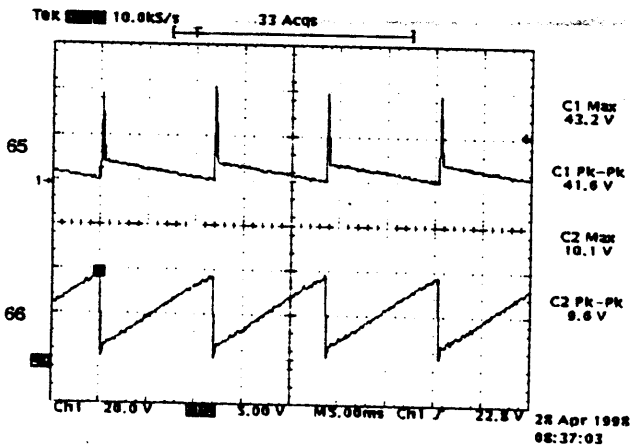
CH1 : IC401 PIN13 (VOUT1)
CH2 : IC401 PIN12 (VOUT2)



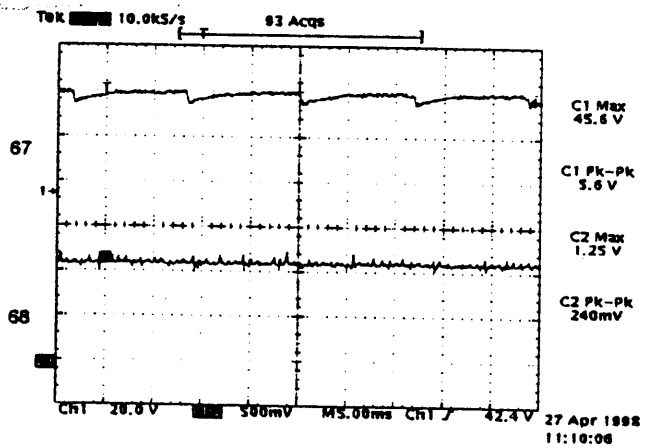
CH1 : IC401 PIN11 (EWDRV)
CH2 : IC501 PIN4 (OUTB)



CH1 : IC501 PIN6 (OUTA)
CH2 : IC501 PIN9



CH1 : IC501 PIN7
CH2 : Q503 "E"



VERTICAL CKT WAREFORM

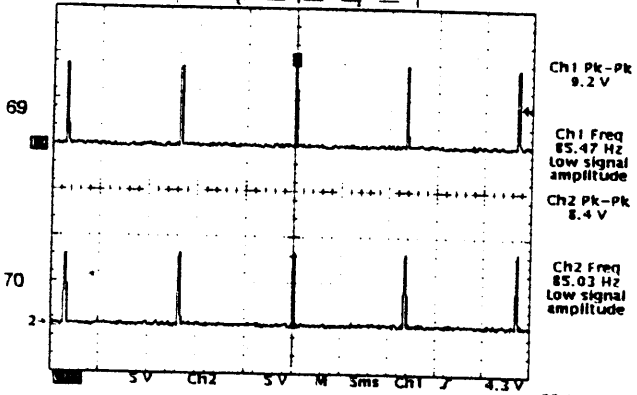
VESA 1024x768 69KHz/85Hz

CH1 : IC501 PIN8

CH2 : Q501 "E"

Tab 10kS/s

17 Acqs

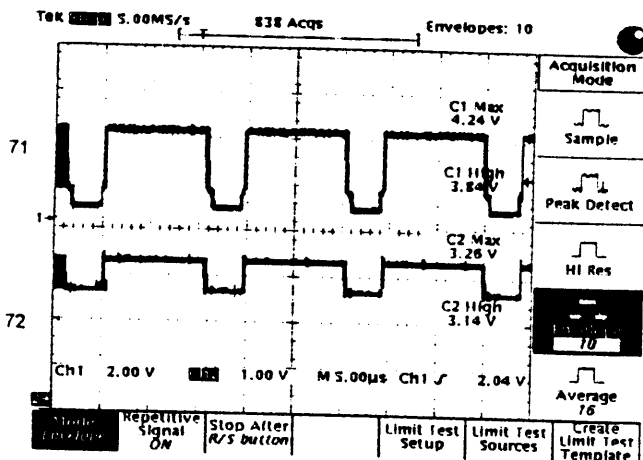


22 Apr 1998
17:15:39

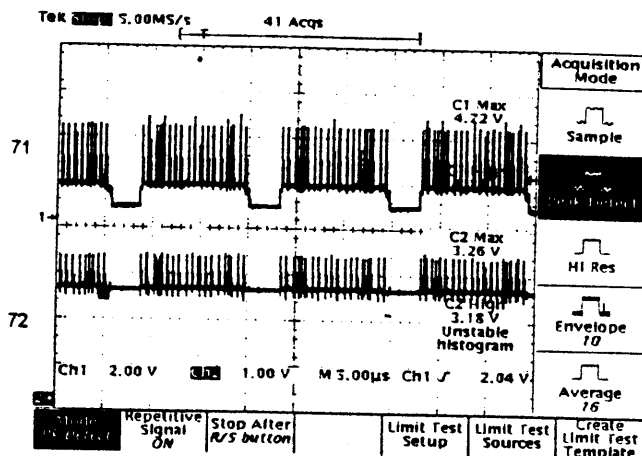
VIDEO CKT WAREFORM

VESA 1024x768 69KHz/85Hz

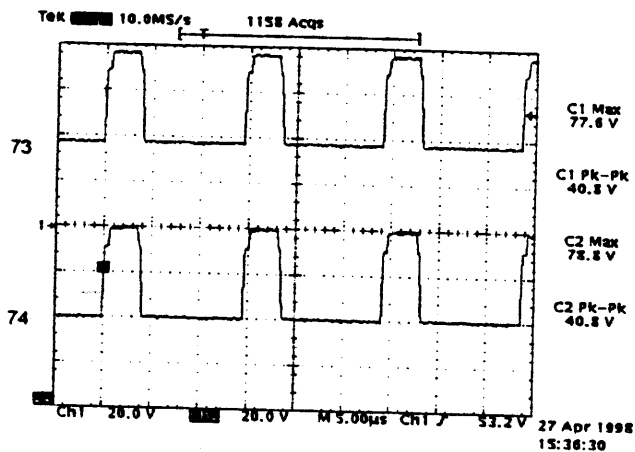
CH1: IC601 PIN2/6/11 (FULL WHITE)
CH2: IC601 PIN35/32/29 (FULL WHITE)



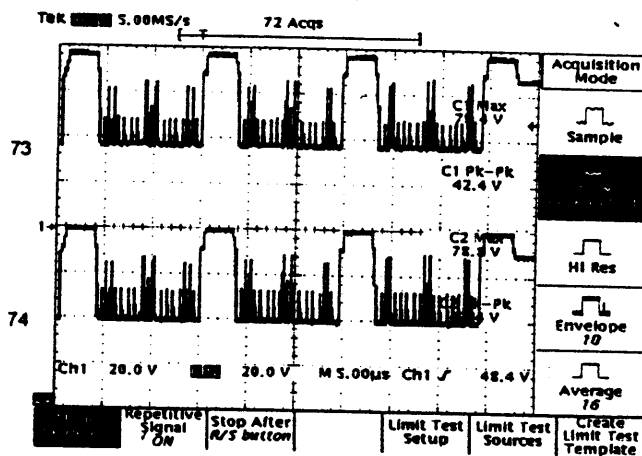
CH1: IC601 PIN2/6/11 (CROSSHATCH)
CH2: IC601 PIN35/32/29 (CROSSHATCH)



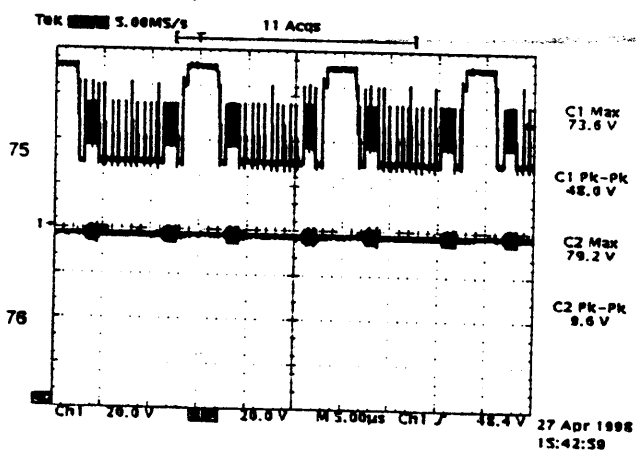
CH1: IC604 PIN3/6/9 (FULL WHITE)
CH2: IC604 PIN2/5/10 (FULL WHITE)



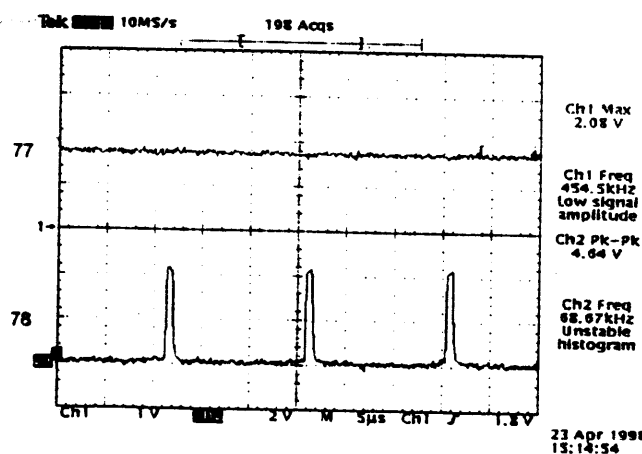
CH1: IC604 PIN3/6/9 (CROSSHATCH)
CH2: IC604 PIN2/5/10 (CROSSHATCH)



CH1: X601 PIN11/8/6
CH2: Q612/Q614/Q616 "E"



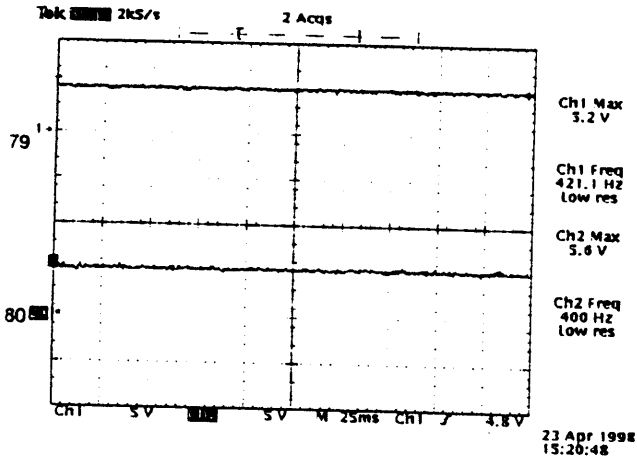
CH1: IC601 PIN15
CH2: IC601 PIN19



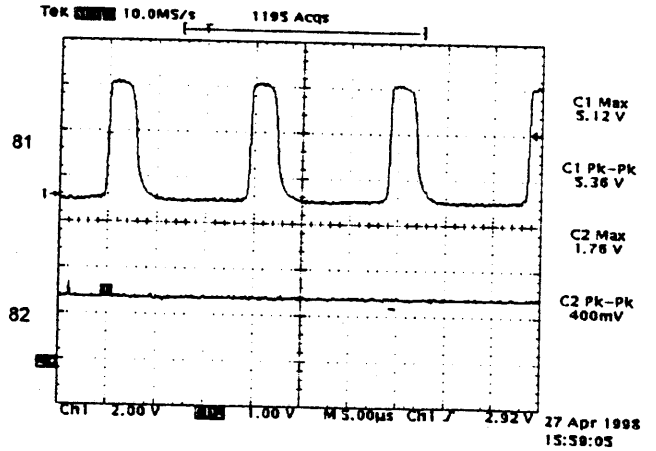
VIDEO CKT WAREFORM

VESA 1024x768 69KHz/85Hz

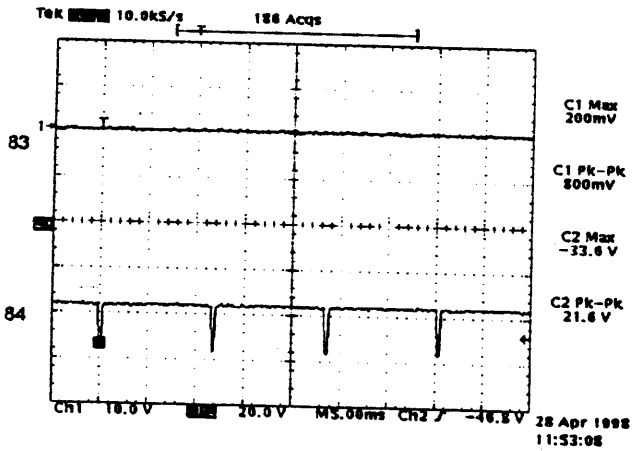
CH1: IC601 PIN20
CH2: IC601 PIN21



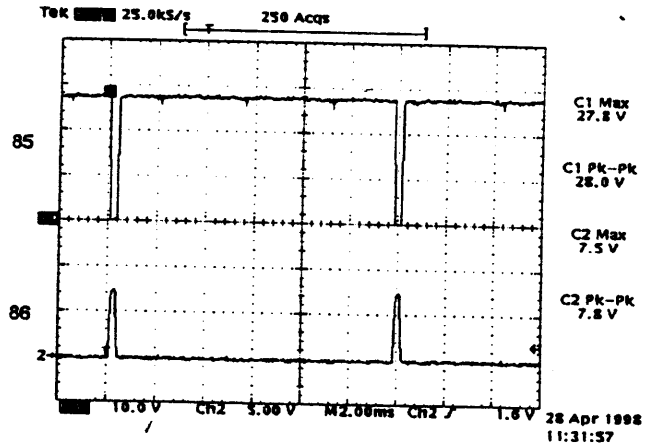
CH1: IC601 PIN27
CH2: IC601 PIN30



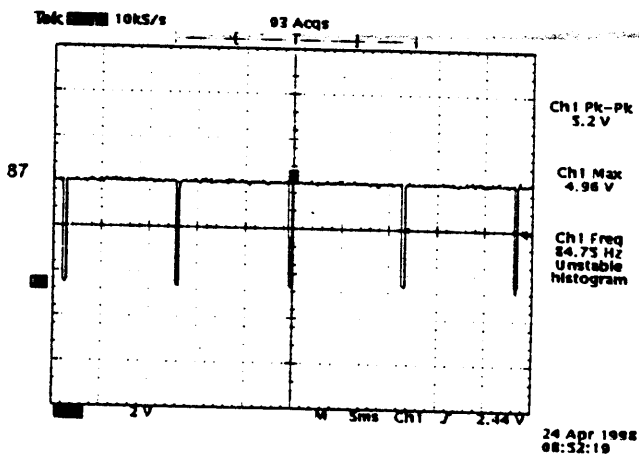
CH1: IC601 PIN1
CH2: D626



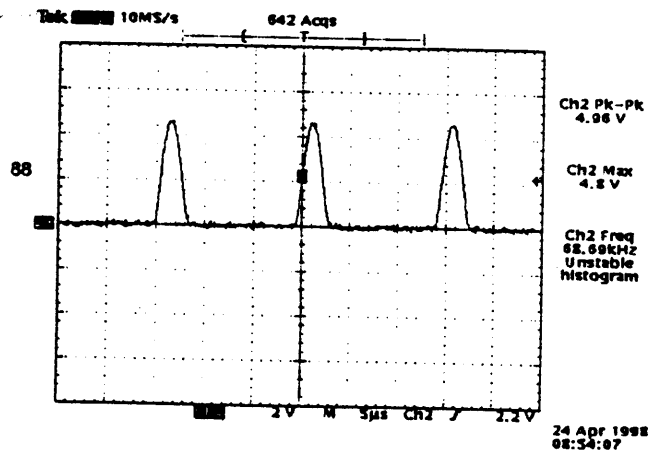
CH1: Q619 "C"
CH2: WP604 PIN3 (VBL)



IC603 PIN19



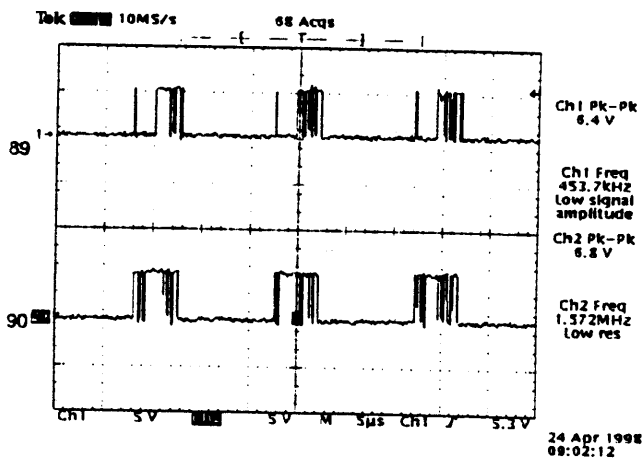
IC603 PIN18



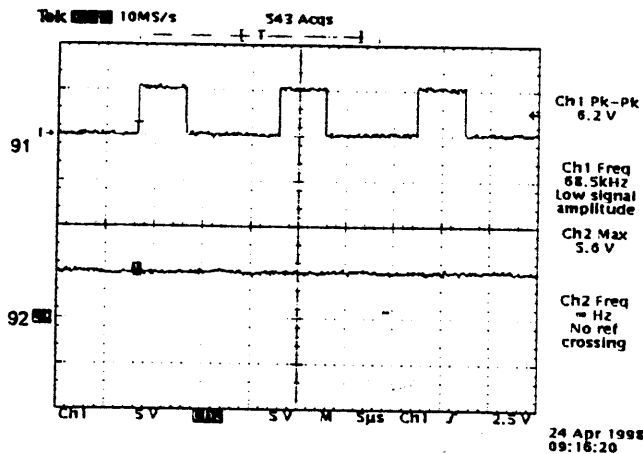
VIDEO CKT WAREFORM

VESA 1024x768 69KHz/85Hz

CH1 : IC603 PIN17
CH2 : IC603 PIN15



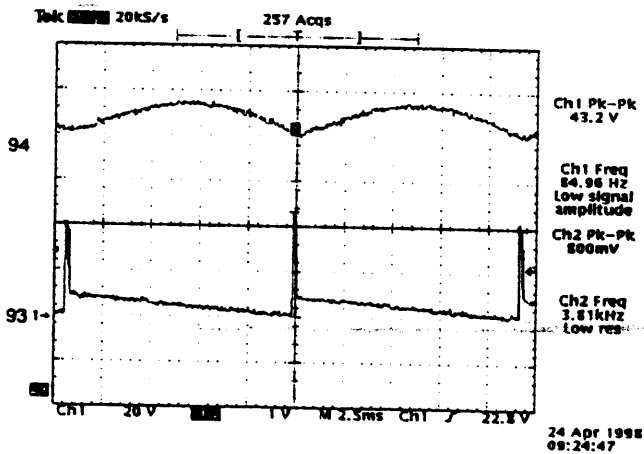
CH1 : IC603 PIN12
CH2 : IC603 PIN6



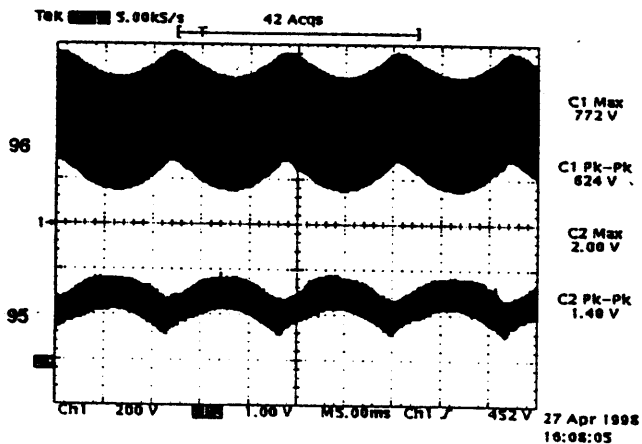
FOCUS CKT WARE FORM

VESA 1024x768 69KHz/85Hz

CH1 : C909
CH2 : DY2



CH1 : Q903 "C"
CH2 : R914



4. Circuit description

- 4.1 Power supply (switching power supply)
- 4.2 Power saving
- 4.3 Micro-controller unit
- 4.4 Sync Processor

- 4.5 Deflection
 - 4.5.1 Horizontal phase shifter
 - 4.5.2 Horizontal synchronization processing
 - 4.5.3 Horizontal Driver stage
 - 4.5.4 Horizontal scanning and high voltage power supply circuit
 - 4.5.5 Boost converter
 - 4.5.6 The E-W Pincushion correction and width control circuit
 - 4.5.7 Trapezoid control / Parallel Control
 - 4.5.8 X-Ray-radiation protection
 - 4.5.9 Vertical Deflection
 - 4.5.10 Focus

- 4.6 Video
 - 4.6.1 Video amplifier
 - 4.6.2 On screen Display (OSD)
 - 4.6.3 Auto Beam Limit CKT (A,B,L,CKT)
 - 4.6.4 Brightness control
 - 4.6.5 Blanking CKT
 - 4.6.6 Contrast, gain & Bias control
 - 4.6.7 DDC 1/2B

- 4.7 Tilt
- 4.8 Audio (for SD7704CM)

4. CIRCUIT DESCRIPTION

4.1 POWER SUPPLY (switching mode power supply fly-back type)(IC101)

The raw DC B+ voltage is got from AC input voltage after EMI filter rectifier and PFC CKT. It supplies lower voltage VCC to PWM controller, IC101 (UC3842), through start-up circuit (R122, R104, R105, Q102, ZD102). R113 & C109 generate triangle wave-form to decide switching frequency. In order to power supply synchronism that must feedback Horizontal-Synch to "FB+" from FBT(T401) and forced power supply synchronization with Horizontal deflection circuit. The pin6 is output of IC101 to drives power MOSFET Q101. A High-frequency & High-Voltage square wave-form is across the primary winding and transfers energy to the secondary. The output DC voltage gets after rectifying and filtering.

In order to have a stable and regulated output voltage while AC input voltage and output load change. IC203 will produce a current change through IC105 couple a volt change on R121 and through R115 feed to IC101 pin2. PWM controller circuit will adjust duty cycle and maintain stable voltage.

The PWM controller IC101 is started up from the raw B⁺. The lower voltage VCC is provided by T101's AUX-Winding(pin1) through D103, C106, C105 to IC101 pin7.

The PFC CKT (IC103 TDA4862, Q106, T102 and D111, C101) control a boost converter in a way that sinusoidal current is take from the single-phase line supply (CX101) and produce a about 380VDC at C101, The power factor is almost 1 (110VAC).

At power saving mode, Q108, Q107 will be off, than IC103 will be turn off. The power factor is about 0.45.

Degauss CKT : When the power is on and press manual degauss the IC301 pin20 will high to turn on Q209 and RL201, degauss will active about 4 second.

4.2 POWER SAVING

According to TCO agreement with monitor manufacturer is as the following table:

SYNC. INPUT	H. & V. PRESENTED	NO H. OR V.	NO H. AND V.
MODE	NORMAL	SUSPEND	POWER OFF
TTL SIGNAL	ON		
SW1	Hi	Lo	Lo
SW2	Hi	Hi	Lo
LED	Green	Amber	Amber
Power (Watt)	Normal	< 15W	< 8W

SW1 : IC301 pin17, suspend (SUS)

SW2 : IC301 pin18, power down (PD)

- SW1 and SW2 are Hi level at normal-on mode.
- The suspend mode occurs when sw1 is at low level. (by IC301 pin17)
The B⁺ (12V) are switch off via IC201.
- The power-off mode occurs when sw1 and sw2 are at low level.
Both B⁺ (12V) and 6.3V are switch off via IC201, Q202, Q203 respectively.
- The micro-processor IC301 are driven to power off mode when signal cable is not connected to PC.

4.3 MICRO-CONTROLLER UNIT (MCU)(IC301)

IC301 is a 8-bit micro-controller (UM68P61) with 16K byte ROM memory, which play a main role of the digital control monitor. It performs as mode timing detector, key control scanner and controller, DPMS power saving handling, on screen display programmer and auto-alignment geometry controller Pin26, 27, 28, 29, 30 are for key control. Pin21, 22, 23 are for s-correction switch control, pin39, 40 are for Horizontal and Vertical sync. input respectively, pin32, 33 is the V-sync. and horizontal-sync output to IC401 pin14, 15. Pin10(SIN) and pin16 (SCK) are as series data input and clock (CLK) input for IC603(OSD) IC601(DAC). Pin9 is chip selection to IC603. Pin14/13 are serial clock and serial data (SCL, SDA) bus communicate with IC302 (EEPROM) pin6/5. Pin24(SPA)/25(SCL) are as a port to communicate with alignment fixture / DDC 1/2B access by signal cable.

CS CONTROL FUNCTION

	VGA 640X400	VGA 640X480	VESA640 X480/75	VESA800 X600/75	VESA800 X600/72	VESA1024 X768/60	VESA1024 X768/70	VESA1024 X768/75	VESA1024 X768/85	VESA1080 X1024/60
CS2 (PIN22)	LO	LO	HI	LO	LO	LO	HI	HI	HI	HI
CS3 (PIN21)	LO	LO	LO	HI	HI	HI	HI	HI	HI	HI
CS4 (PIN23)	LO	LO	HI	LO	LO	LO	LO	LO	HI	HI

4.4 SYNC. PROCESSOR

The horizontal sync. is connected from signal cable to IC301(MCU) pin39 input and from IC301 pin33 output positive polarity sync to IC401 pin15.

Vertical sync. is connector from signal cable to IC301(MCU) pin40 input comes out at pin32 a positive polarity sync to IC401 pin14 and Q615 (vertical blanking CKT).

- The IC301(UM68P61) and the IC401(TDA4858) sync input can handle either composite or separate sync input.

4.5 DEFLECTION CIRCUIT

4.5.1 Horizontal Phase Shifter:

This function is operated by a part of circuit inside IC401 (TDA4858). The picture phase adjustment is control by a current range at pin30. The current of this point change from PWM DAC voltage pin37 of IC301 (DAC).

4.5.2 Horizontal Synchronization Processing

The horizontal synchronization processor is integrated inside the chip of TDA4858(IC401). It uses a dual phase-lock-loop (PLL1/PLL2) design. This operation ensures a smooth tuning and avoids fast changes of H-frequency during catching.

The processor can synchronize with the input sync. up to triple of free-run frequency which is determined by R462 , R485 and C445..

The PLL1 phase detector circuit is used to control the oscillator frequency and maintains it in proper frequency and phase with the incoming sync signal. One input is coupled from output of VCO which is built inside the IC.

A loop filter with a properly selected time constant (C444, C443, R461) is connected at pin26.

The PLL2 circuit is used to compare the line flyback pulse at pin HFLB with the oscillator sawtooth voltage, to compensates the delay in H-deflection by adjusting the PHASE of HDRV. One input is from the output of VCO (which is inside the IC) and a second input (pin1 of IC 401) is coupled from pin2 of T402 (FBT) via R452.

The control voltage formed through loop filter is to control horizontal output pulse output at proper duty cycle and maintain the phase between raster and picture.

The horizontal drive pulses are sent from pin7 of IC401.

CIRCUIT DESCRIPTION

4.5.3 Horizontal Driver Stage

The horizontal drive pulse is applied to the base of driver transistor Q402. B⁺ is provided by the regulated 80V voltage source via R403, R404, R405 and C406. The output of driver transformer T402 is coupled to the base of Horizontal output Transistor Q401. C404 and R402 compose of damping network which is to eliminate the leakage flux of T402 during Q402 turns off.

4.5.4 Horizontal Scanning And High Voltage Power Supply Circuit

The horizontal scanning is accomplished in a diode modulator method. Except the basic horizontal scan output, the diode modulator add one second resonant circuit during retrace time, which also performs the parabola modulation in yoke current to compensate the pincushion effect. Linearity coil L404/L403 corrects the asymmetrical distortion. C415/C485/C419/C423 are S-Correction capacitors, C415/C485/C423 are switched on/off according to different H-frequency.

The conducting period of horizontal output transistor Q401 and D402 completes the second half of scan. The conducting period of damper diode D401 completes the first half part of horizontal scan.

The retrace capacitor is C401, the charge and discharge actions of retrace capacitor via yoke after Q401 turned off, which is designed for the same resonant frequency with the main scan circuit.

In the high voltage drive circuit, the output of Q401 is applied to the primary winding of flyback transformer, (FBT) T401 and drives the flyback transformer to supply CRT anode voltage of about 25.8KV by stepping up FBT during retrace period.

Several driven power sources are developed in the FBT secondary, including 110Vp-p source (pin1) for Horizontal blanking pulse (HBL) and OSD horizontal synch(OHS). AFC pulse (pin1), XRP pulse (pin1).

TCO negative pulse (pin4) and -120VDC for G1 B⁺.

CIRCUIT DESCRIPTION

4.5.5 Boost Converter

In order to maintain same scan width and anode voltage within 31K-69KHz, the scan supply B+ tracked with continuous H-frequency is necessary, and the design is implemented by a conventional method of boost converter.

The boost converter mainly consists of a n-channel MOSFET (Q416), choke L406, capacitor C449 and rectifier diode (D418).

The PWM control circuit is integrated in IC401, pin5 is inverting, pin3 is output of error amplifier, both for frequency compensation and gain setting and pin5 is DC controlled (VR402) of B+ adjustment. PWM pulse width output at pin6 is modulated according to internal error amplifier output and pin4 current sense.

4.5.6 The E-W Pincushion Correction And Width Control Circuit

The voltage across C414 can be varied in accordance with a vertical parabolic wave-form which is generated by two stage drive Q407, Q408, Q409. The peak yoke current is decreased in proportion to the voltage across C419, as the voltage across C414 is increased for compensating the pincushion effect. The parabolic wave-form is generated from IC401 pin11 which is controlled by pin21 of IC401.

The DC voltage across C414 also can be varied to control the picture width, which can be done through IC301(PWM DAC) pin36.

4.5.7 TRAPEZOID CONTROL / PARALLEL CONTROL

Trapezoid is controlled by pin20 of IC401 that DC control from pin2 of IC301 (PWM DAC) pin2.

Parallel CKT (Q418~Q422) is superimposed the vertical saw tooth current on IC401 pin30 (H-POS), the wave form amplitude is adjusted by IC301 pin1.

4.5.8 X-RAY-RADIATION PROTECTION

Therefore, should a fault occur which would activate the X-ray protect circuit, Should a fault occur which would cause the high voltage to increase above a predetermined level, the positive pulse at pin1 of the FBT (T402) would go more positive. This action in turn would increase the voltage applied to pin2 of IC401 to exceed its breakdown voltage for a certain time. an internal latch switches the IC into protection mode. Shutting down the horizontal HPLL2 and drive pulse. (INCLUDE HDRV BDRV VOUT 1 AND VOUT 2)

NOTE: The X-RAY-Radiation protection circuit used in this monitor is a latching type the monitor will shutdown and continue until turn-off the monitor with power switch.

4.5.9 Vertical Deflection (IC501)

Vertical deflection function is operated in the chip IC401(TDA4858), IC501 (TDA4866) which mainly contains the oscillator, ramp generator, power output amplifier and flyback generator. Vertical oscillator is obtained amplifier by means of and integrator driven by oscillation circuit that is determined by C442, R460. The vertical sync signal is applied to the pin14 of IC401 through R440. Once the sync signal synchronized a clock pulse is generated inside this chip. The clock pulse is just as a sync input of ramp generator. A liner voltage ramp is produced at pin12,13 of IC401, and is couple to IC501 pin1,2 for vertical output amplitude Vertical output amplitude is controlled by pin18 of IC401.

The CKT of the TDA4866 provides a high CMRR current driven differential input (pin1,2), two output stages (pin4,6) in a full bridge configuration, a flyback generator, a protection CKT for the output stage and a guard CKT.

Pin4, pin6 are the outputs of the power amplifier and it drives the yoke by a current driven in opposite phase current ramp. R505 and the series network R506, C505(damping function) are used to stabilize the power amplifier. Pin3 is the supply voltage 13VDC, pin7 is the flyback supply voltage pin8 is the guard output, provide a blanking signal for the CRT pin9 is the feedback input (fed back to the input stage).

Vertical centering is controlled by changing the DC voltage at vertical output that is caused from the DC shift of IC401 pin17, and that can be adjusted by DC control (pin34 of IC301).

CIRCUIT DESCRIPTION

V-moire canceling CKT (Q502, Q503) is operated by changing the vertical position at next frame. The 50% duty FV/2 sync is from IC301 pin12, the shift amplitude is adjusted by IC301 pin31 and through C501, R514, R516 to IC401 pin17.

4.5.10 FOCUS

Horizontal parabolic wave form is take from C419, through T901 amplifier, C906 coupling to Q903 collector. Vertical parabolic waveform is take from R911, C908, R912, C909 integral CKT through Q903, Q903 cascade simplifier.

4.6 VIDEO

4.6.1 VIDEO AMPLIFIER(IC601)

The video amplifier module is composed of three amplifiers for red, green, blue channel.

The video input signal is fed to the video preamplifier IC601(M52743ASP) (pin2 blue, pin6 red, pin11 green) through AC coupling capacitor. C608, C610, C615.

The clamping pulse comes from IC401 pin16 via D430, P602A pin3 to IC601 pin19.

(Q602, Q619) (Q603, Q620) & (Q604, Q621) are cascade amplifier for B.R.G. channel respectively.

4.6.2 On Screen Display (OSD)(IC603)

IC603 (M35045) is a on screen display generator. Pin18 for H-sync input, pin19 for V-sync input. The IC603 is controlled by IC301 (UM68P61) via SCK, SIN bus IC603 (pin4, pin5, PIN6).

The on screen display signal is output from pin13(R). Pin15(G), pin17(B) and connected to mixer circuit of IC601 pin4, pin9, pin13.

4.6.3 Auto Beam Limit CKT (A. B. L. CKT)

When beam current over 400uA by VR403, the voltage build at base of Q604 will be low enough to turn on Q604, then the voltage of pin15 of IC601 will be pulled down accordingly to reduce the video preamplifier gain output.

4.6.4 Brightness Control

Brightness is controlled by varying the DC voltage of G1 with the IC601 pin23 (DAC).

4.6.5 Blanking CKT

IC501 (TDA4866) pin8 vertical blanking pulse are fed to the base of Q501 and via Q619. The blanking pulse O/P is coupled to G1 by C665. Horizontal blanking pulse are fed to IC601 pin27 and let video O/P Amp cut off during the period of horizontal retrace. While mode change. IC301 pin19 will pull high to turn on Q618 (mute function) and Q617 will be off. The G1 volt will down to -120V then CRT will cut off the video output.

4.6.6 CONTRAST, GAIN & BIAS CONTROL

The IC601 (M52743ASP) contains three gated single ended input black level clamp compurgators for brightness control, three matched DC controlled attenuators for contrast control, and three DC controlled sub-contrast attenuators providing gain trim capability for white balance.

All the DC control voltage are comes from IC601 M52743ASP internal (DAC) is controlled by IC301(UM68P61) Micro controller via a serial bus. (IC301 pin9, pin10). The IC601 DAC output pin24, 25, 26 for G.R.B (BIAS) controller.

4.6.7 DDC1/2B(IC51)

IC601(24LC21A) can transmit continuously it's extended identification, "EDID" using DDC1 communication channel. In addition, the monitor can respond to a regrets for EDID, or complete VDIF, to be transmitted using DDC2, level B commands. Pin6 SCL is clock input for DDC 2B, pin5 SDA for data input. Pin7 V sync is clock input for DDC1 through V-sync.

CIRCUIT DESCRIPTION

In DDC1 data transfer (UNI-directional mode) the V sync input pin is used as input clock for data transmission and SDA output pin as serial data line the SCL pin will hold high.

The DDC2 B mode (BI - directional mode), BUS consists of two wires SCL is for the data transmission clock and SDA is for the data lin.

4.7 TILT

Tilt CKT is operated a volt different on ratation coil. The IC301 pin38 output 0~12V to Q7701, to control the volt amplitude and polarity on P7701, when IC301 pin38 output is 0V, the current is flow from +12V via Q7703, R7702, P7701 to Q7706. When IC301 pin38 output is +12V, the current is flow from +12V via Q7705, R7710, P7701 to Q7702.

4.8 AUDIO (for SD7704CM)

The audio IC801 (TDA7057AQ) is a stereo BTL output amplifier with DC volume control (pin1 and pin7), the R, L input a audio signal, via R801, C801, R803, C802 to IC801 pin3 and pin5.

“POP” Fix CKT is composed Q803, Q804 when power on/off mode change mute function is operated by D801 and Q303 volume is controlled by IC301 pin26.



UC1842/3/4/5
UC2842/3/4/5
UC3842/3/4/5

Current Mode PWM Controller

FEATURES

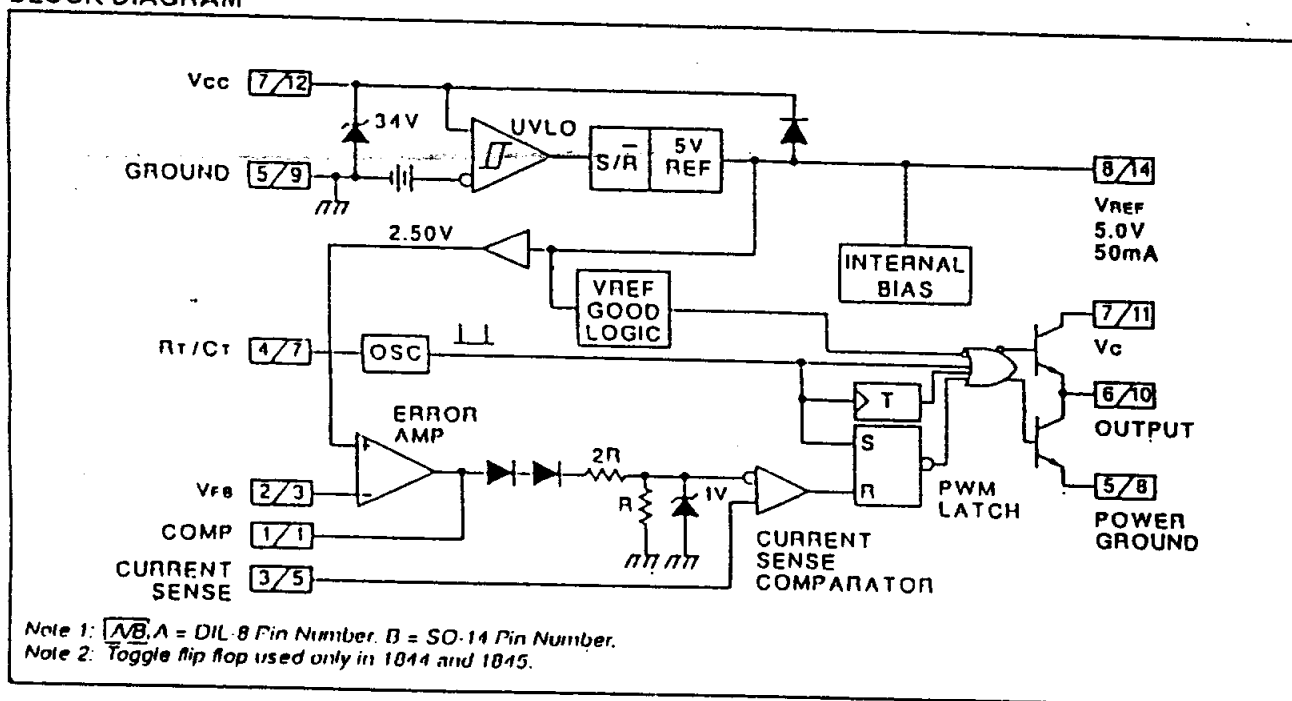
- Optimized For Off-line And DC To DC Converters
- Low Start Up Current (< 1mA)
- Automatic Feed Forward Compensation
- Pulse-by-pulse Current Limiting
- Enhanced Load Response Characteristics
- Under-voltage Lockout With Hysteresis
- Double Pulse Suppression
- High Current Totem Pole Output
- Internally Trimmed Bandgap Reference
- 500kHz Operation
- Low Ro Error Amp

DESCRIPTION

The UC1842/3/4/5 family of control ICs provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include under-voltage lockout featuring start up current less than 1mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N Channel MOSFETs, is low in the off state.

Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The UC1842 and UC1844 have UVLO thresholds of 16V (on) and 10V (off), ideally suited to off-line applications. The corresponding thresholds for the UC1843 and UC1845 are 8.4V and 7.6V. The UC1842 and UC1843 can operate to duty cycles approaching 100%. A range of zero to 50% is obtained by the UC1844 and UC1845 by the addition of an internal toggle flip flop which blanks the output off every other clock cycle.

BLOCK DIAGRAM



CIRCUIT DESCRIPTION

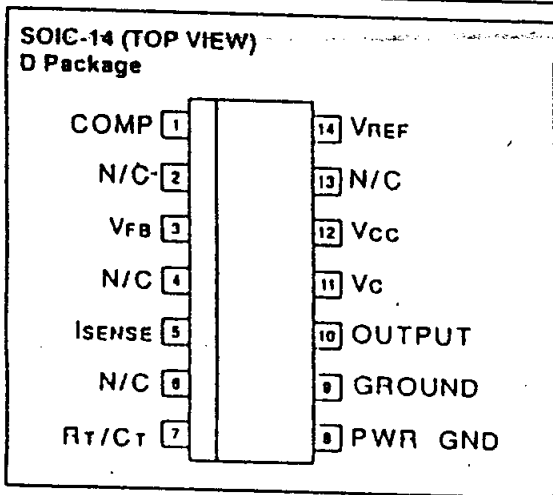
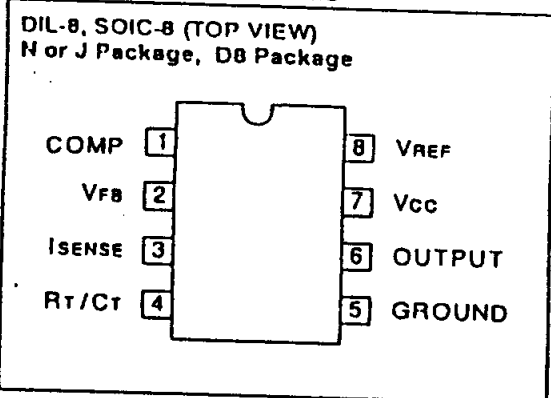
UC1842/3/4/5
UC2842/3/4/5
UC3842/3/4/5

ABSOLUTE MAXIMUM RATINGS (Note 1)

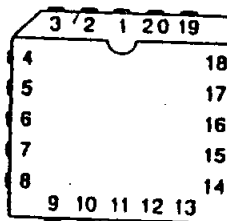
Supply Voltage (Low Impedance Source)	30V
Supply Voltage ($I_{CC} < 30mA$)	Self Limiting
Output Current	$\pm 1A$
Output Energy (Capacitive Load)	5 μ J
Analog Inputs (Pins 2, 3)	-0.3V to +6.3V
Error Amp Output SINK Current	10mA
Power Dissipation at $T_A \leq 25^\circ C$ (DIL-8)	1W
Power Dissipation at $T_A \leq 25^\circ C$ (SOIC-14)	725mW
Storage Temperature Range	-65 $^\circ C$ to +150 $^\circ C$
Lead Temperature (Soldering, 10 Seconds)	300 $^\circ C$

Note 1: All voltages are with respect to Pin 5.
All currents are positive into the specified terminal.
Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS



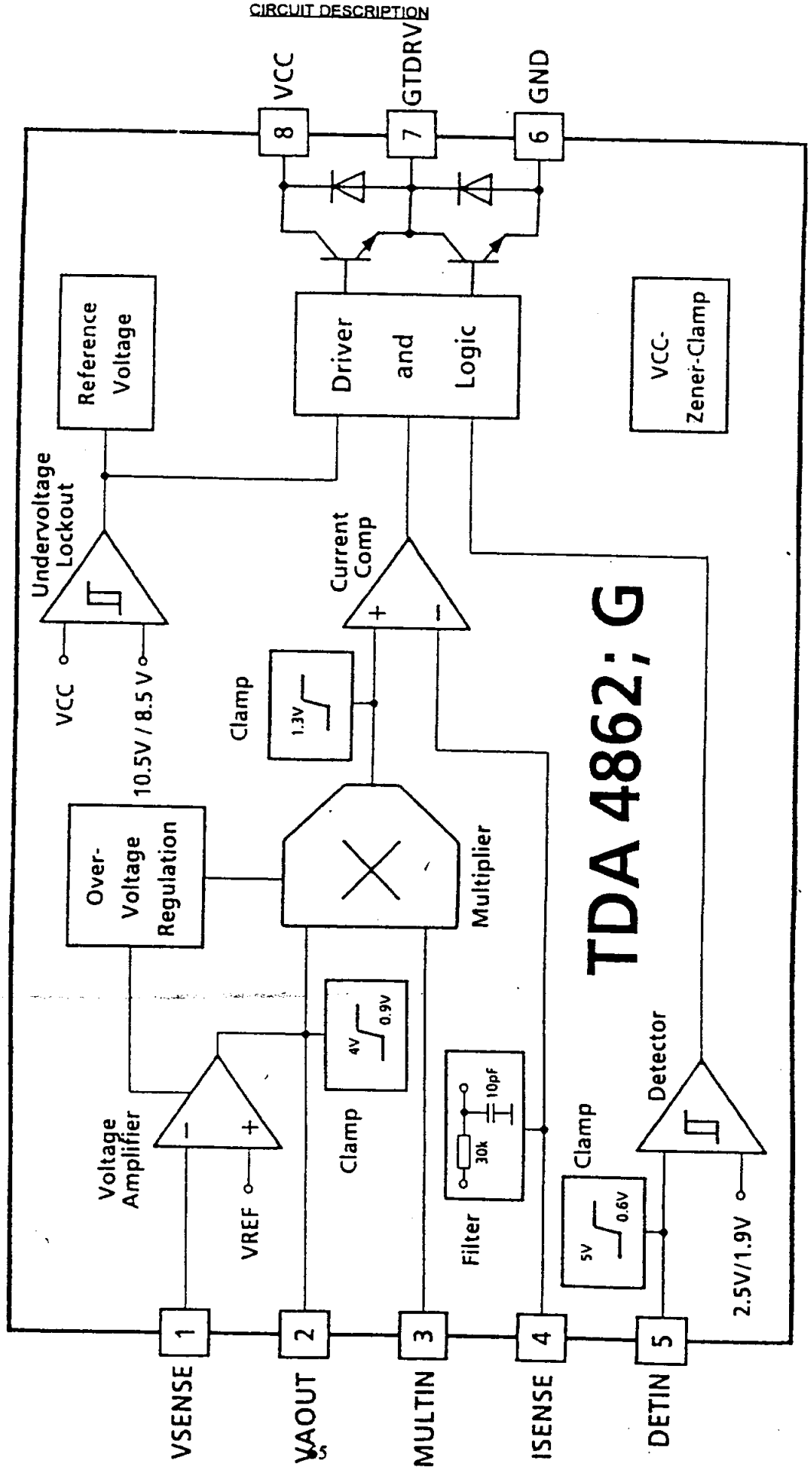
PLCC-20 (TOP VIEW)
Q Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
COMP	2
N/C	3
N/C	4
VFB	5
N/C	6
ISENSE	7
N/C	8
N/C	9
Rt/Ct	10
N/C	11
PWR GND	12
GROUND	13
N/C	14
OUTPUT	15
N/C	16
Vc	17
Vcc	18
N/C	19
VREF	20

CIRCUIT DESCRIPTION

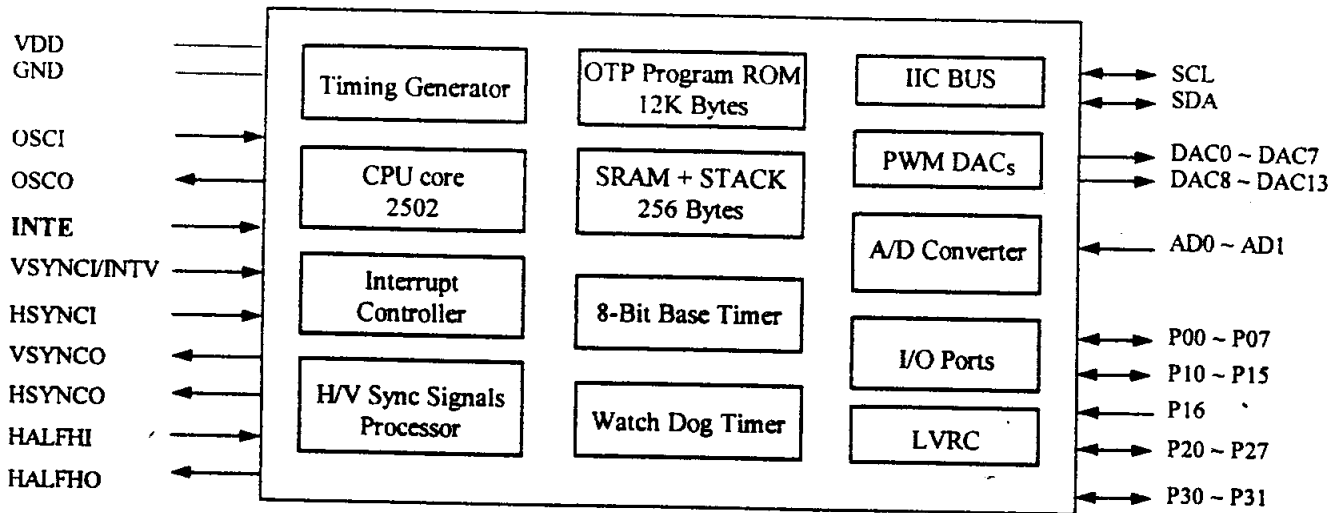
Block Diagram



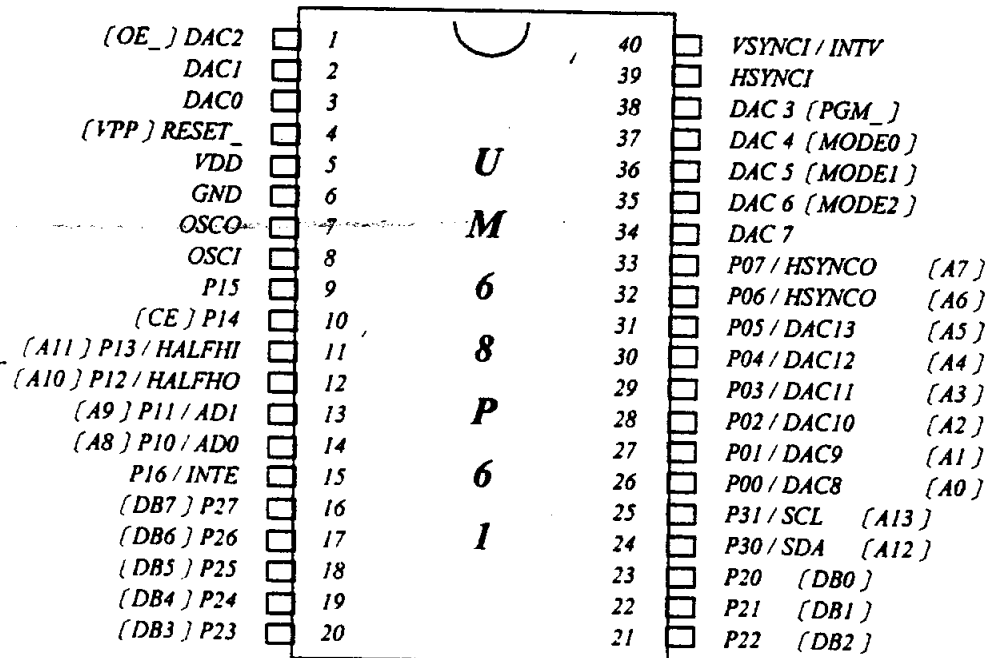
CIRCUIT DESCRIPTION

UM68P61 preliminary data sheet V2.1

3. Block diagram



4. Pin Assignment



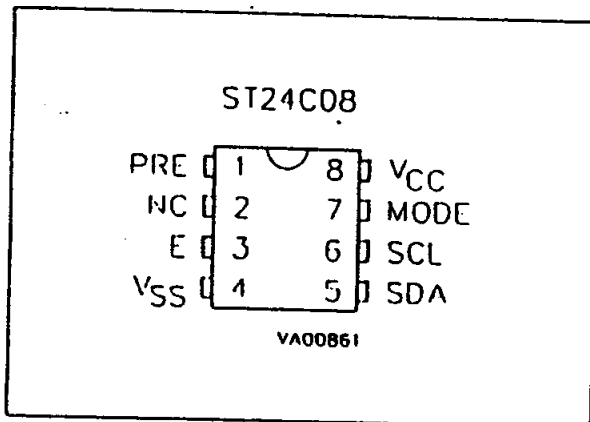
ST24C08

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T _A	Ambient Operating Temperature	grade 1	0 to 70
		grade 3	-40 to 125
		grade 6	-40 to 85
T _{STG}	Storage Temperature	-65 to 150	°C
T _{LEAD}	Lead Temperature, Soldering (PSDIP8 package) 10 sec	260	°C
V _{IO}	Input or Output Voltages	-0.3 to 6.5	V
V _{CC}	Supply Voltage	-0.3 to 6.5	V
V _{ESD}	Electrostatic Discharge Voltage (Human Body model)	4000	V
	Electrostatic Discharge Voltage (Machine model)	1000	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

Figure 2. DIP Pin Connections



DESCRIPTION (cont'd)

ST24C08's may be attached to the I²C bus and selected individually.

The ST24C08 behaves as a slave device in the I²C protocol with all memory operations synchronised by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 5 device select bits, 2 block select bits, plus one read/write bit and terminated by an acknowledge bit. When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Data in the upper block of the memory may be write protected. The protected area is programmable to

start on any 16 byte boundary. Protection is enabled by setting a memory bit flag and the PRE signal input.

OPERATING MODES

There are both Read and Write modes. Each is entered by the correct sequence of serial bits sent to the device on the SDA bus line. For some Write modes the status of the MODE input is also used to set the operating mode. For the Protect mode the status of the PRE input determines whether protection is enabled or disabled.

The 8 bits sent after a START condition are made up of a device select of 4 bits that identify the device type, a chip enable bit, 2 block select bits and one bit for a READ (RW = 1) or WRITE (RW = 0) operation.

There are three modes both for read and write. These are summarised in Table 4 and described below.

Byte Write. In this mode a device select is sent with the RW bit at '0', followed by the address of the byte. This is followed by the 8 bit data to be written during the programming cycle.

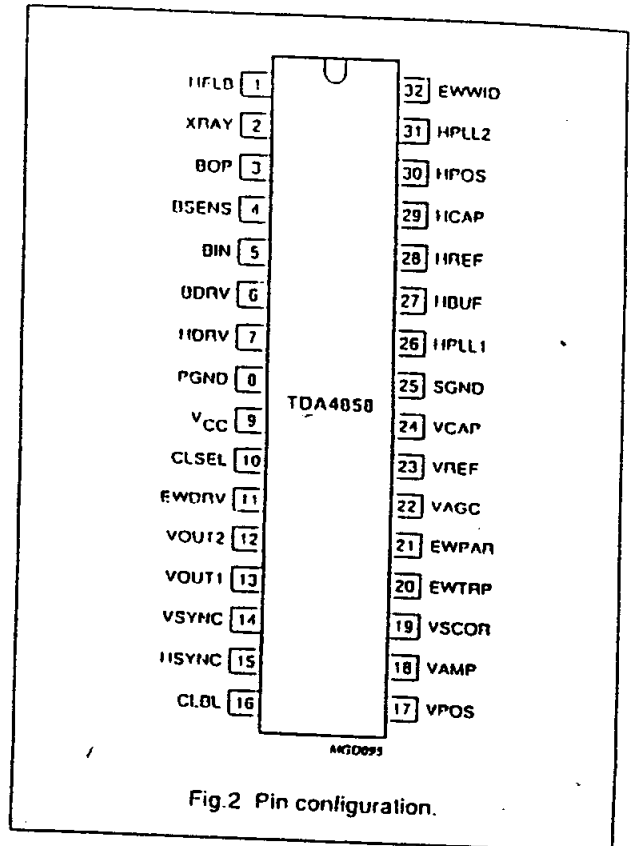
Multibyte Write and Page Write. In these modes up to 8 or up to 16 bytes respectively may be written in one programming cycle. Multibyte Write mode is activated when the MODE pin is at V_{HH} level and Page Write when MODE is at V_{IL}. A device select is sent with the RW bit at '0', followed by the address of the first byte. This is followed by the data bytes to write. The bytes are written in the programming cycle. All 8 bytes in the Page Write mode must have the same five upper address bits.

Economy Autosync Deflection Controller
(EASDC)

TDA4858

PINNING

SYMBOL	PIN	DESCRIPTION
HFLB	1	horizontal flyback input
XRAY	2	X-ray protection input
BOP	3	B+ control OTA output; comparator input
BSSENS	4	B+ control comparator input/output
BIN	5	B+ control OTA input
BDRV	6	B+ control driver output
HDRV	7	horizontal driver output
PGND	8	power ground
V _{CC}	9	supply voltage
CLSEL	10	selection input for horizontal clamping trigger
EWDRV	11	EW parabola output
VOUT2	12	vertical output 2 (ascending sawtooth)
VOUT1	13	vertical output 1 (descending sawtooth)
VSYNC	14	vertical synchronization input/output (TTL level)
HSYNC	15	horizontal/composite synchronization input (TTL level or sync-on-video)
CLBL	16	video clamping pulse/vertical blanking and protection output
VPOS	17	vertical shift input
VAMP	18	vertical size input
VSCOR	19	vertical S-correction input
EWTRP	20	EW trapezium correction input
EWPAR	21	EW parabola amplitude input
VAGC	22	external capacitor for vertical amplitude control
VREF	23	external resistor for vertical oscillator
VCAP	24	external capacitor for vertical oscillator
SGND	25	signal ground
HPLL1	26	external filter for PLL1
HBUF	27	buffered f/v voltage output
HREF	28	reference current for horizontal oscillator
HCAP	29	external capacitor for horizontal oscillator
HIPOS	30	horizontal shift input
HPLL2	31	external filter for PLL2/soft start
EWVID	32	horizontal size input



CIRCUIT DESCRIPTION

Philips Semiconductors

Preliminary specification

Economy Autosync Deflection Controller
(EASDC)

TDA4858

BLOCK DIAGRAM

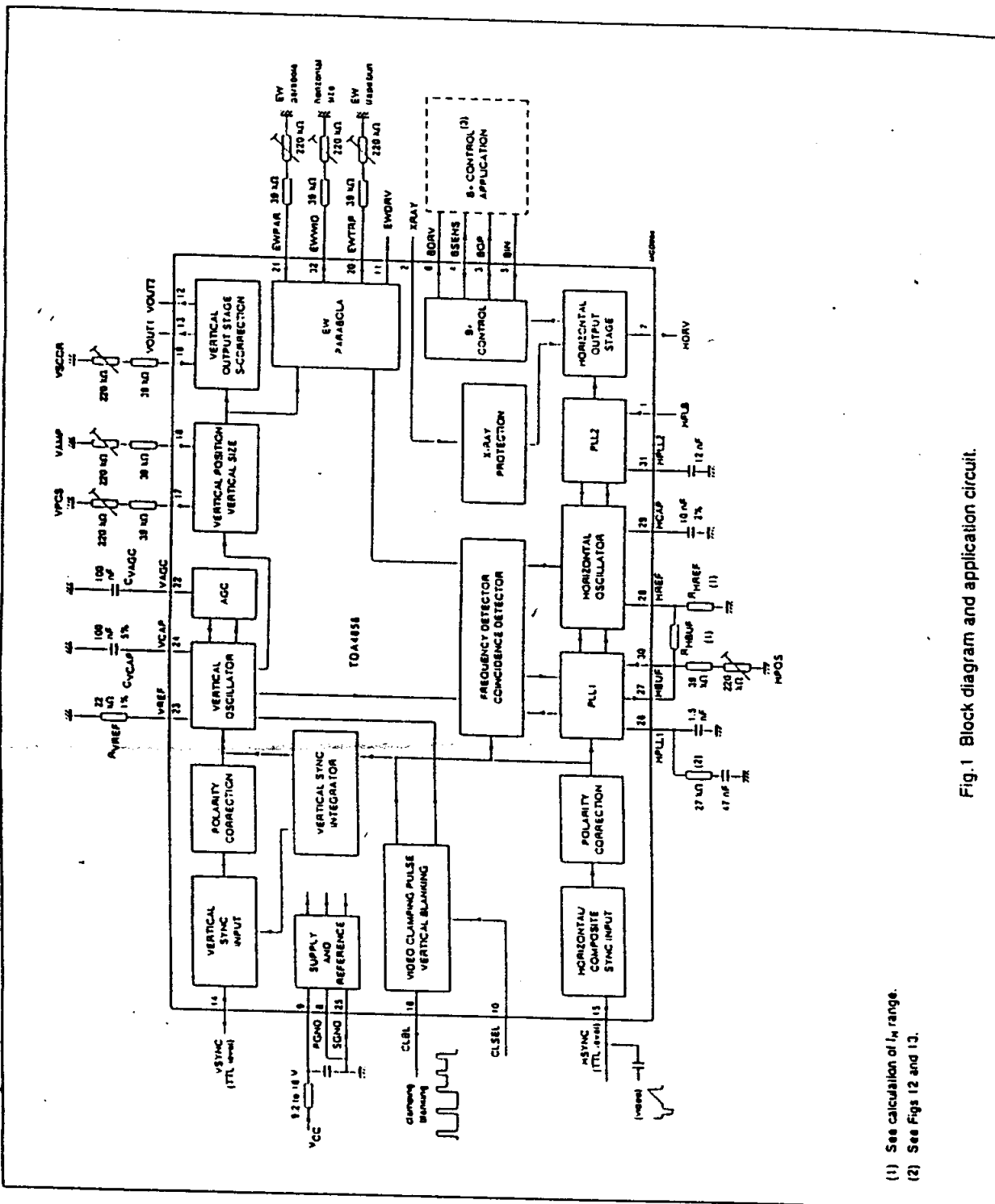


Fig. 1 Block diagram and application circuit.

(1) See calculation of I_m range.
(2) See Figs 12 and 13.

CIRCUIT DESCRIPTION

Philips Semiconductors

Preliminary specification

Full bridge current driven vertical deflection booster

TDA4866

BLOCK DIAGRAM

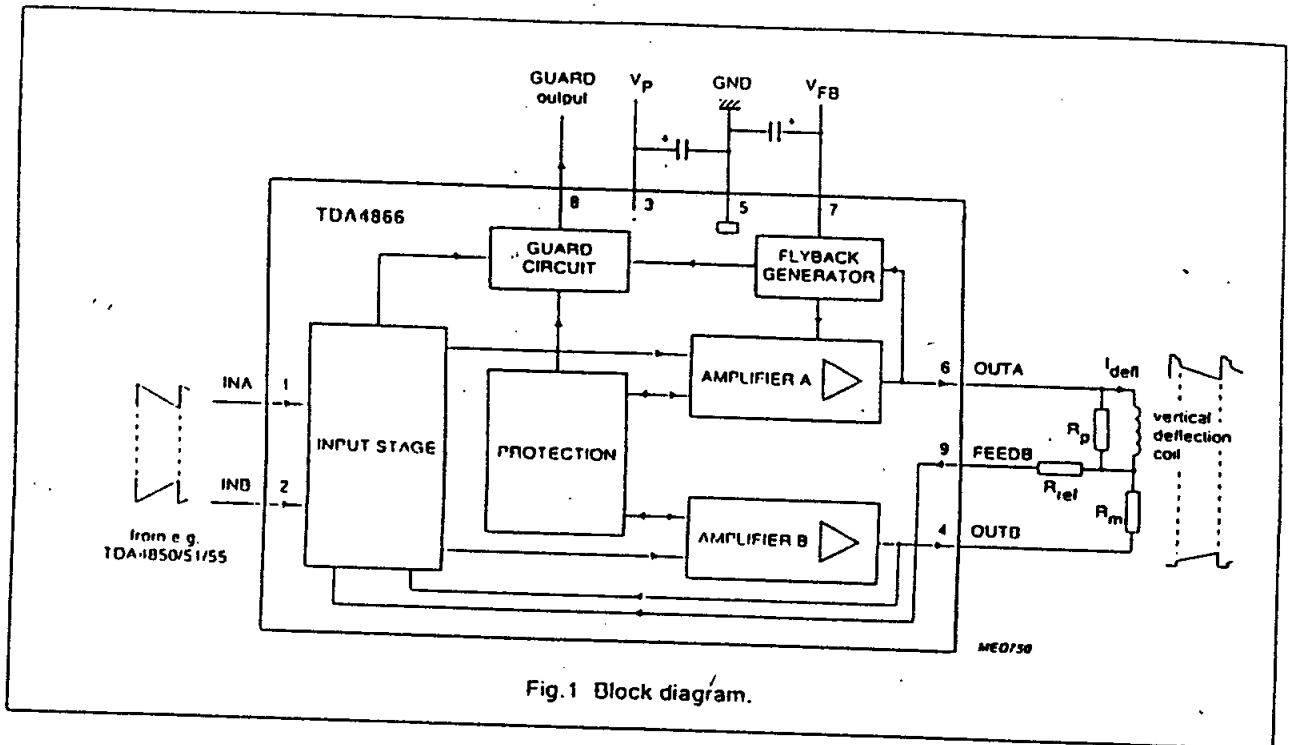


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
INA	1	input A
INB	2	input B
V _P	3	supply voltage
OUTB	4	output B
GND	5	ground; note 1
OUTA	6	output A
V _{FB}	7	flyback supply voltage
GUARD	8	guard output
FEEDB	9	feedback input

Note

- The mounting base is connected to pin 5 (GND).

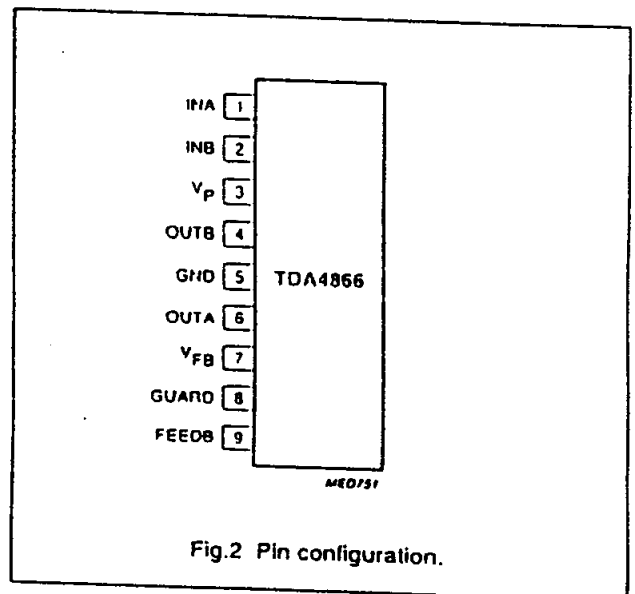


Fig.2 Pin configuration.

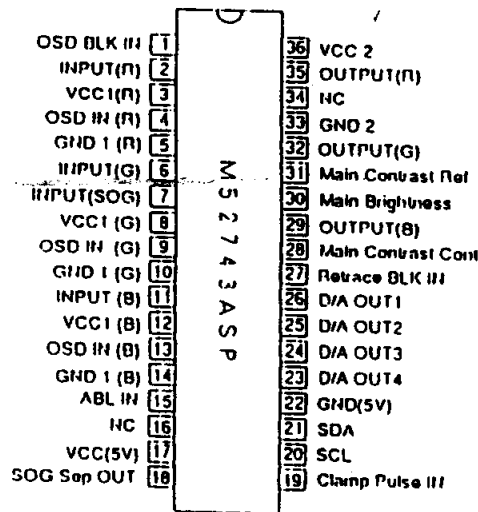
CIRCUIT DESCRIPTION

MITSUBISHI ELECTRIC CORPORATION

SPECIFICATION	PREPARED	<i>Yamauchi</i>	N	E	Y
	APPROVED	<i>A. Toyama</i>			

Title : Integrated Circuit

1. Type Name: M52743ASP
2. Function
 - 2.1 Function name: I²c bus controled 3channel video pre-amplifier.
 - 2.2 Block diagram: Fig. 1
3. Application: Display monitor
4. Outline
 - 4.1 Name: 36 pin plastic mold SDIP
 - 4.2 Outline drawing number: G 4 6 5 0 3 8
5. Circuit drawing
Drawing number : _____
6. Pin Configuration



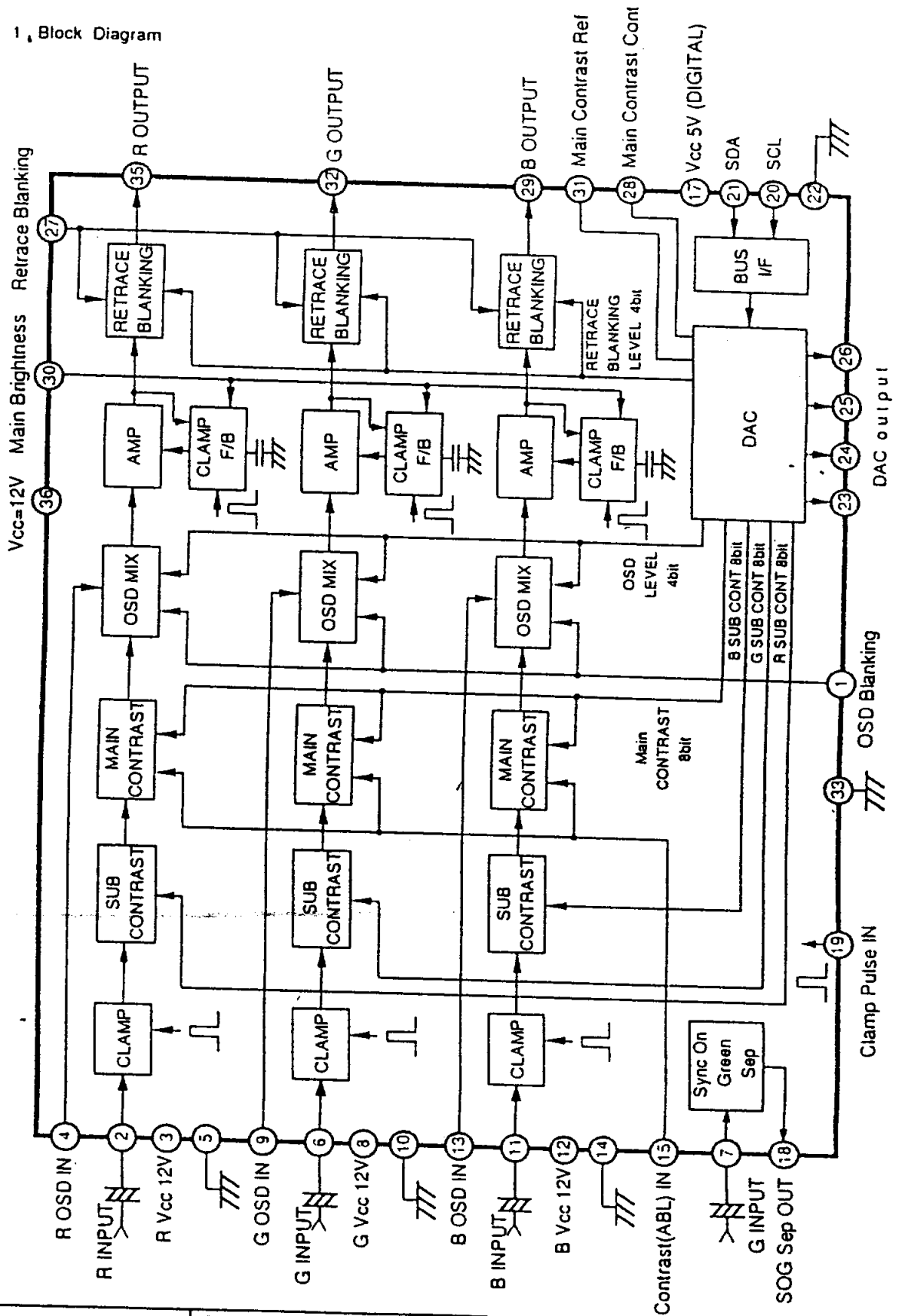
Outside Package: 36P4E

7. Related Standards

SPECIFICATION	TYPE	M52743ASP	SPECIFICATION NO. 1
			GNOK-M52743ASP-600

CIRCUIT DESCRIPTION

Fig. 1, Block Diagram



SPECIFICATION

TYPE

M52743ASP

SPECIFICATION NO.

GNOK-M52743ASP-600



Improved Low Cost Triple CRT Driver

CVA2411TX

FEATURES

- Ease of Use
- Small Heat Sink
- OSD Option
- EMI Control Option
- Excellent Gray Scale Linearity

APPLICATIONS

- CRT Displays for 1280 x 1024 Resolution with Pixel Clock Frequency up to 160MHz

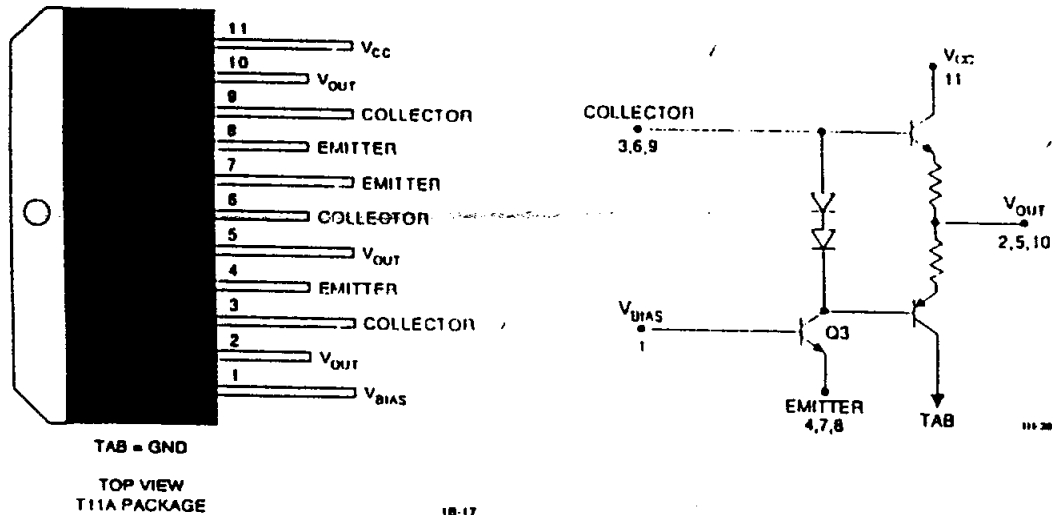
DESCRIPTION

The CVA2411TX is an improved low cost version that features excellent gray scale linearity with no crossover distortion and less EMI for 64KHz (horizontal scanning frequency) monitors. The CVA2411TX can be used with pre-amplifiers where the common emitter transistor is part of the pre-amp. With this device, OSD, peaking coil, and peaking capacitor can be available. A very small heat sink is required to pick-up ground from the standard TO220 package Tab. With 65MHz bandwidth, the device is an ideal low cost solution for 14", 15" and 17" monitors.

ORDERING INFORMATION

Part	Package	Temperature
CVA2411TX	T11A	-20°C to +100°C

CONNECTION DIAGRAM AND SIMPLIFIED SCHEMATIC



CIRCUIT DESCRIPTION

M35045-XXXSP

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

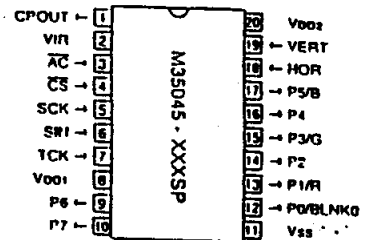
DESCRIPTION

The M35045-XXXSP is a character pattern display controller designed to display characters. It uses a silicon gate CMOS process and is housed in a 20-pin shrink DIP package.

FEATURES

- Screen composition 24 columns x 12 lines
- Number of characters displayed 208 (Max.)
- Character composition 12 x 18 dot matrix
- Characters available 256 characters
- Character sizes available 4 (horizontal) x 4 (vertical)
- Display locations available
 - Horizontal direction 1000 locations
 - Vertical direction 1023 locations
- Blinking Character units
 - Cycle : division of vertical synchronization signal into 64 or 32
 - Duty : 25%, 50%, or 75%
- Data input By the 16-bit serial input function
- Coloring
 - Character color Character unit
 - Background coloring Character unit
 - Matrix-outline (shadow) coloring 8 colors (RGB output)
Specified by register
 - Border coloring 8 colors (RGB output)
Specified by register
 - Raster coloring 8 colors (RGB output)
Specified by register
- Blanking
 - Blanking off
 - Character size blanking
 - Border size blanking
 - Matrix-outline blanking
 - All blanking (all raster area)
- Output ports
 - 4 shared output ports (logged between RGB output)
 - 4 dedicated output ports
- Display RAM erase function
- Display input frequency range Fosc = 30MHz-80MHz

PIN CONFIGURATION (TOP VIEW)



Outline 20P4B

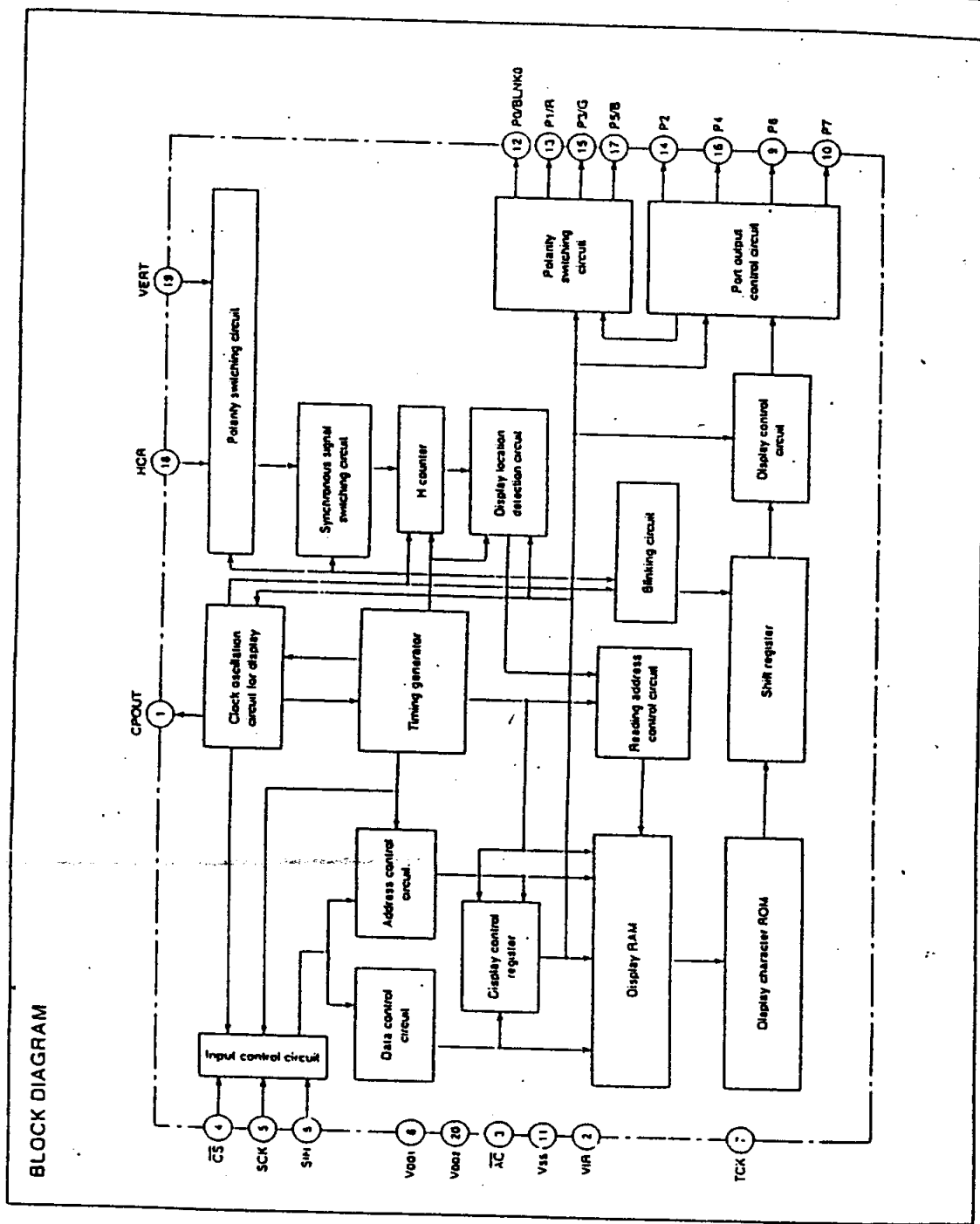
APPLICATION

Monitor

CIRCUIT DESCRIPTION

M35045-XXXSP

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS



CIRCUIT DESCRIPTION

Philips Semiconductors

Objective specification

2 x 5 W stereo BTL audio output amplifier with DC volume control

TDA7057AQ

PINNING

SYMBOL	PIN	DESCRIPTION
VC1	1	DC volume control 1
n.c.	2	not connected
$V_{i(1)}$	3	voltage input 1
V_P	4	positive supply voltage
$V_{i(2)}$	5	voltage input 2
SGND	6	signal ground
VC2	7	DC volume control 2
OUT2+	8	positive output 2
PGND2	9	power ground 2
OUT2-	10	negative output 2
OUT1-	11	negative output 1
PGND1	12	power ground 1
OUT1+	13	positive output 1

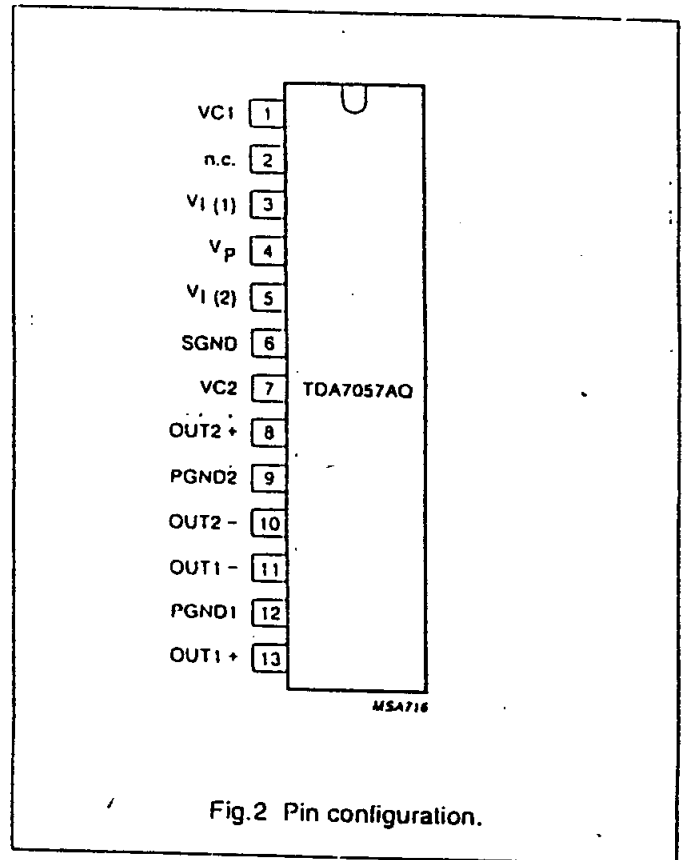


Fig.2 Pin configuration.

CIRCUIT DESCRIPTION

Philips Semiconductors

Objective specification

2 x 5 W stereo BTL audio output amplifier with DC volume control

TDA7057AQ

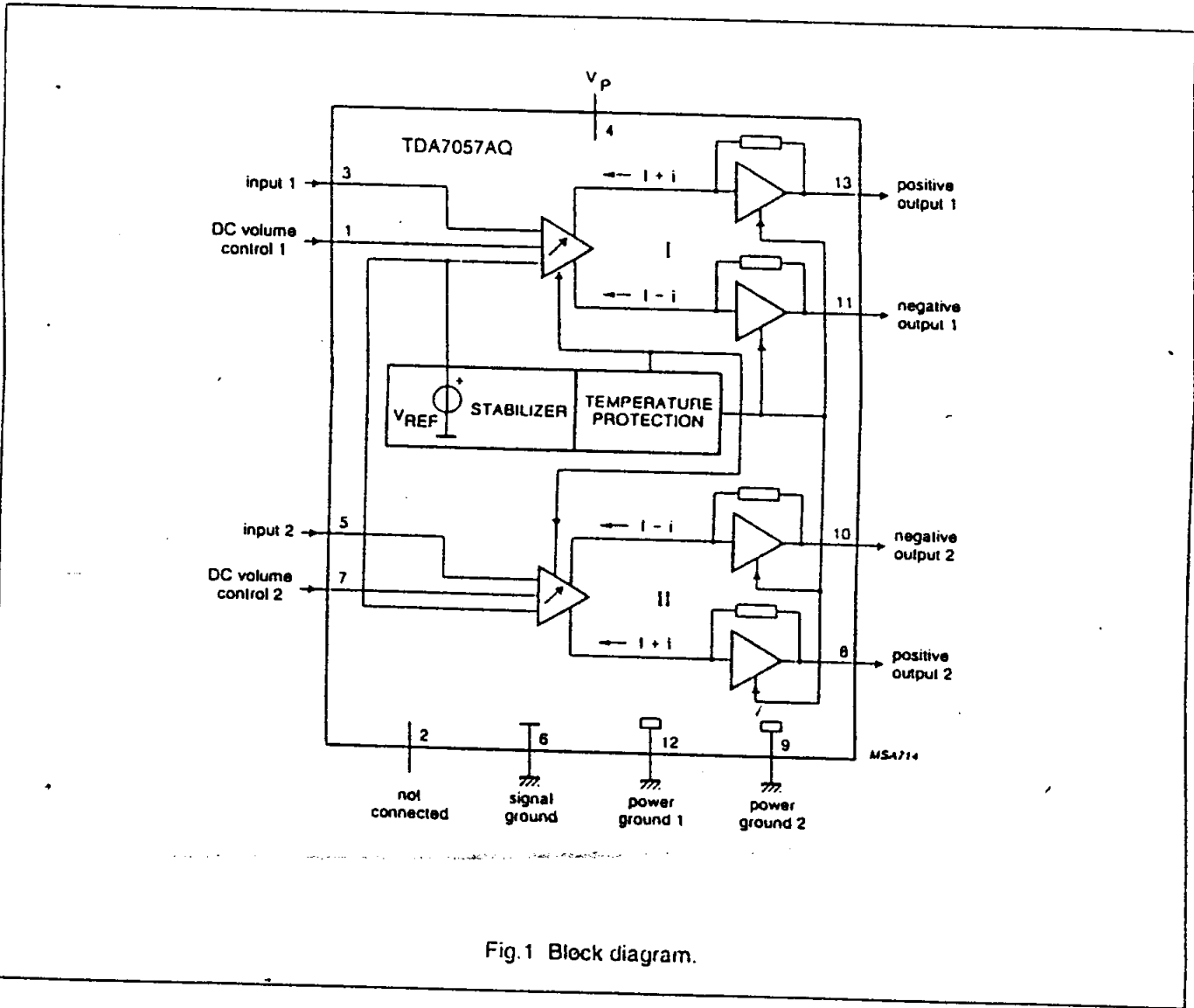


Fig.1 Block diagram.

Adjusting Procedure

A. GENERAL

B. INSTRUMENT ALIGNMENT

1. Deflection Presets
2. Power Supply Alignment
3. Size & Geometry Adjustment
4. Video Alignment
5. Focus adjustment / function "RESET"

C. PCB DEFINED

D. FIXTURE FUNCTION DESCRIPTION

ADJUSTING PROCEDURE

A. GENERAL

1. All specification must be met over line voltage range of 90vac to 264vac 50Hz / 60Hz, unless otherwise specified.
2. Operating temperature range is 0°C to 35°C with a relative humidity of 10% or less to 80%.
3. The monitor must be operational in a usable state within 30 minutes after turn-on.
4. All signal levels are measured assuming termination at the monitor's input jacks or in its characteristic impedance.
5. An ambient lighting level of 400 to 600 Lux is assumed when setting brightness for raster extinction threshold.
6. All purity related specifications must be met without external degaussing.
7. All controls must have excess range (no control may be left at an end stop when proper alignment is completed).
8. The monitor is not required to meet specs during the following but must tolerate, without damage to the CRT or circuits, any sequence or combination of power on and off, signal on and off, unplugging of power or signal, erratic, wrong frequency or noisy inputs while at any possible settings of user accessible controls likewise, the monitor should survive extended periods of operation with line voltage reduced below the specified minimum.
9. An isolation transformer should be used when performing alignment and tests. Portions of the power supply board are hot ground. The remaining boards are cold ground.
10. Discharge of CRT anode should be done only to CRT ground strap.
11. Geometric measurements are assumed to be made along a straight surface with a flat rule or template.

B. INSTRUMENT ALIGNMENT

1. Defection Presets

Control pots VR401, VR402, VR403 are set at middle point. Screen, Focus VR set to min.

2. Power Supply Alignment

2.1 Input VGA (480) signal & beam current set at $0\mu\text{A}$.

2.2 Adjust VR402 until voltage at TP403 = $67.5\text{V} \pm 0.3\text{V}$ (300x225mm).

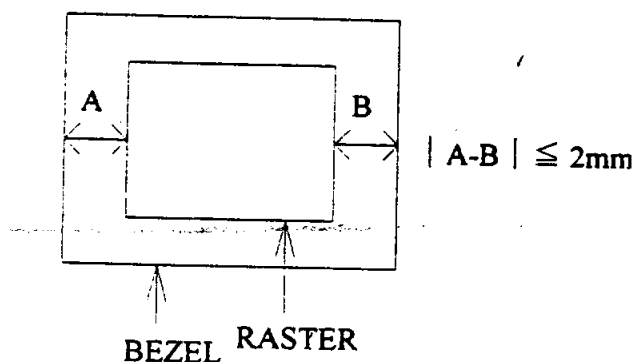
3. Size & Geometry Adjustment

3.1 Raster Centering

3.1.1 Input cross hatch pattern at 60K 1024*768 Hz mode.

3.1.2 Adjust contrast to 10FL, adjust screen just raster visible.

3.1.3 Adjust VR401 to center raster on screen such that the horizontal distance from the midpoint of the left display edge to the left bezel edge is within 2mm of the distance from the midpoint of the right display edge to the right bezel edge.



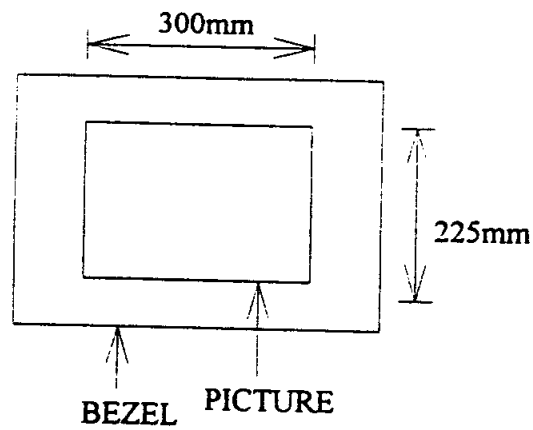
ADJUSTING PROCEDURE

3.2 Picture Size

Input Preset mode signal adjust "V-SIZE, H-SIZE" to achieve

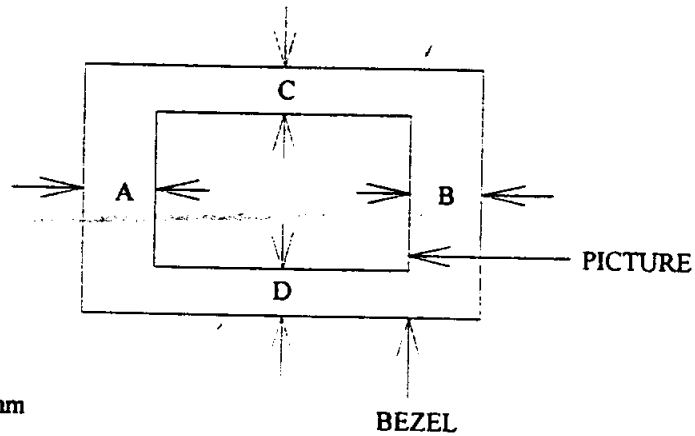
H-SIZE : 300mm \pm 2mm

V-SIZE : 225mm \pm 2mm



3.3 Picture Centering

Input preset mode adjust V-position, H-position such that the picture is centered with the screen.



$$|A - B| \leq 2\text{mm}$$

$$|C - D| \leq 2\text{mm}$$

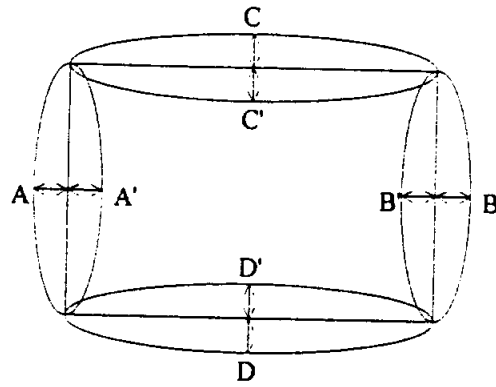
screen.

3.4 Geometry Adjustment

3.4.1 Input preset mode

ADJUSTING PROCEDURE

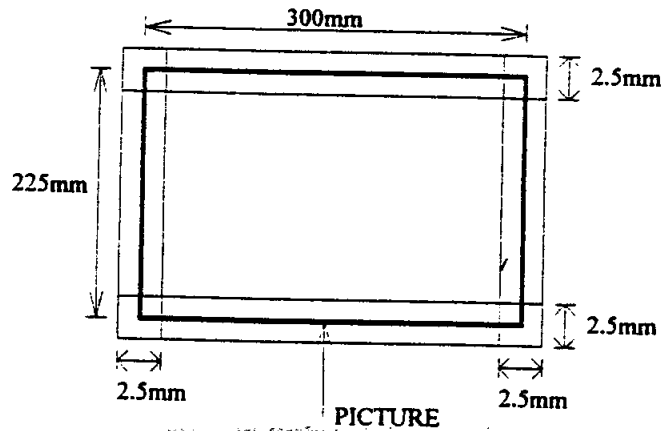
3.4.2 Pincushion and barrel distortion



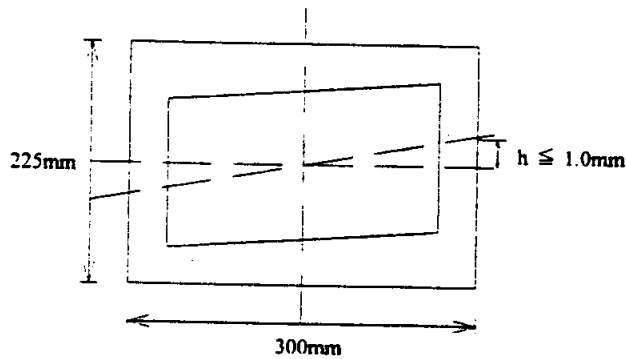
PINCUSHION $\leq 2\text{mm}$ (A',B',C',D')

BARREL $\leq 1\text{mm}$ (A,B,C,D)

3.4.3 Trapezoid and parallelogram distortion trapezoid / parallelogram $\leq 1.5\text{mm}$.



3.4.4 Rotate adjustment



ADJUSTING PROCEDURE

4. Video Alignment

4.1 Input 1024x768 60KHz full black pattern.

4.2 Set Brightness 100%, Contrast 0%, turn the G2 knob to obtain raster light O/P about 0.4 FL

4.3 Adjust R.G.B bias Control to meet following chromaticity spec.

9300 K → $x = 0.283 \pm 0.03$, $y = 0.297 \pm 0.03$, $Y = 0.7 \pm 0.3$ FL

6500 K → $x = 0.313 \pm 0.03$, $y = 0.329 \pm 0.03$, $Y = 0.7 \pm 0.3$ FL

4.4 Adjust Brightness to 50%, Contrast 100%.

4.5 Apply 70mmx70mm green window pattern, adjust G-Driver to obtain green window pattern light o/p about 32 FL (9300 K)

4.6 Apply white window pattern, adjust r-driver, B-Driver to meet following chromaticity spec.

9300 K → $x = 0.283 \pm 0.003$, $y = 0.297 \pm 0.003$, $Y = 46 \pm 1$ FL

4.7 Apply 70mmx70mm green window pattern, adjust G-Driver to obtain green window pattern light O/P about 32 FL (6500 k)

4.8 Apply white window pattern, adjust r-driver, B-Driver to meet following chromaticity spec.

6500 K → $x = 0.313 \pm 0.003$, $y = 0.329 \pm 0.003$, $Y = 46 \pm 1$ FL

4.9 Apply full white pattern.

4.10 Adjust VR403 to obtain light O/P = 32 ± 0.5 FL

4.11 Apply white window pattern (70x70mm) adjust contrast from max to 7FL and check the chromaticity meet following spec.

$| x (\text{AT CONT, MAX}) - x (\text{AT 7FL}) | \leq 0.02$

$| y (\text{AT CONT, MAX}) - y (\text{AT 7FL}) | \leq 0.02$

4.12 Check the percentage of R.G.B driver both 9300 K and 6500 K must between 20% to 90%.

ADJUSTING PROCEDURE

4.13 Functions "RESET"

Push "MENU" button to "RESET" function, then push "+" to reset geometry, push "-" to reset color.

5. Focus Adjustment

5.1 Apply signal ALL "H" pattern at 60K (1024*768) mode.

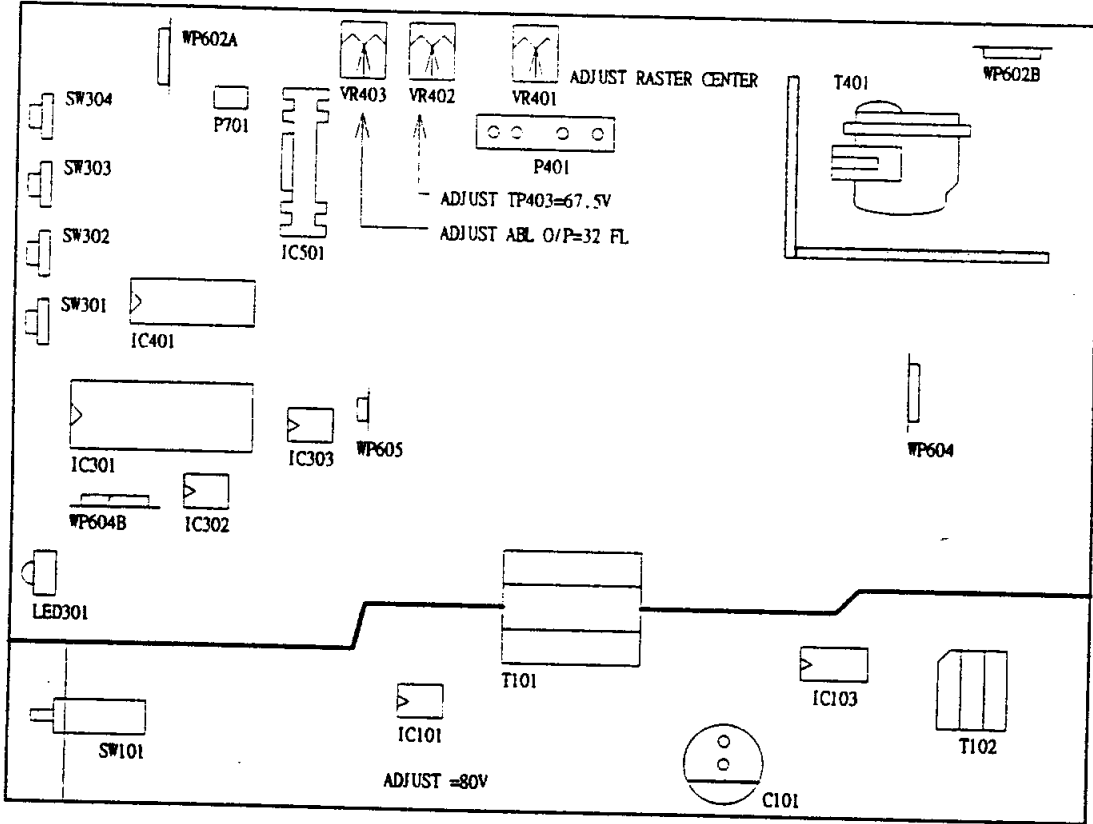
5.2 Set Brightness 50%, Contrast 100%.

5.3 Set focus control for best focus.

ADJUSTING PROCEDURE

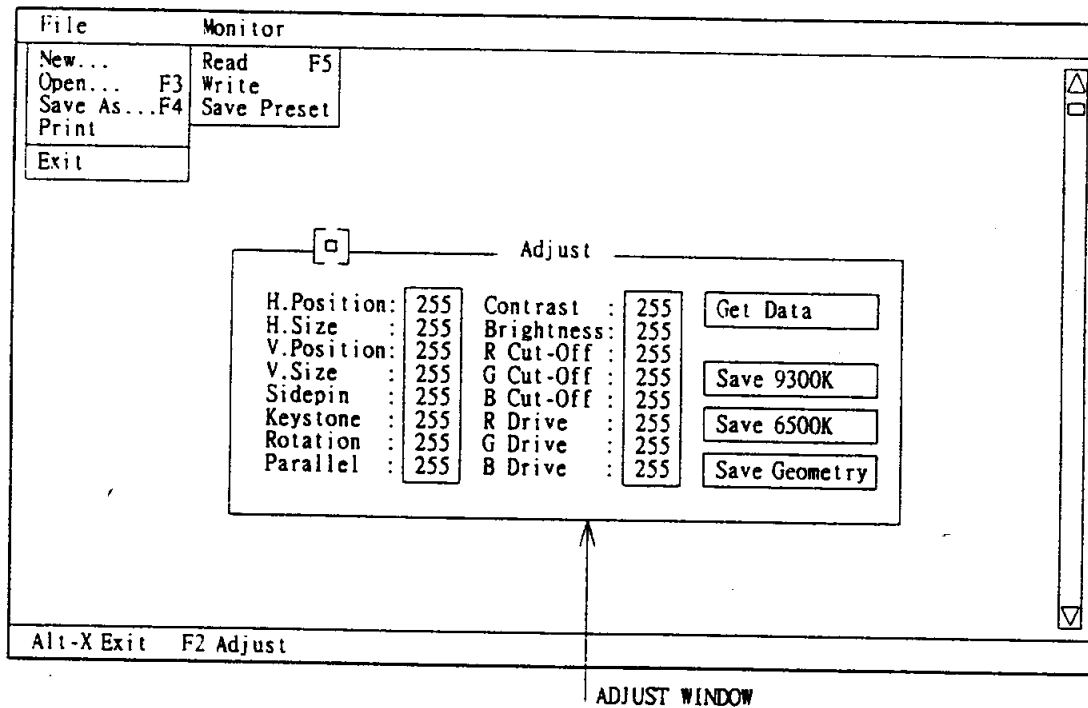
C. PCB DEFINED

Main Board



D. Fixture Function Description

1. Fixture Adjust



2. Adjuster Define

2.1 Adjuster Define

2.1.1 F2 : Into adjuster window

2.1.2 ALT F : NEW : Open new file (Initial Data)

OPEN : Open old file (*.DAT)

SAVE AS : Save file (*.DAT)

PRINT : Print data

EXIT : Exit adjust

2.1.3 ALT M : READ : Read E²PROM data (all data)

WRITE : Write data to E²PROM

SAVE PRESET : Save adjust data to E²PROM

2.1.4 ALT X : Exit adjust

ADJUSTING PROCEDURE

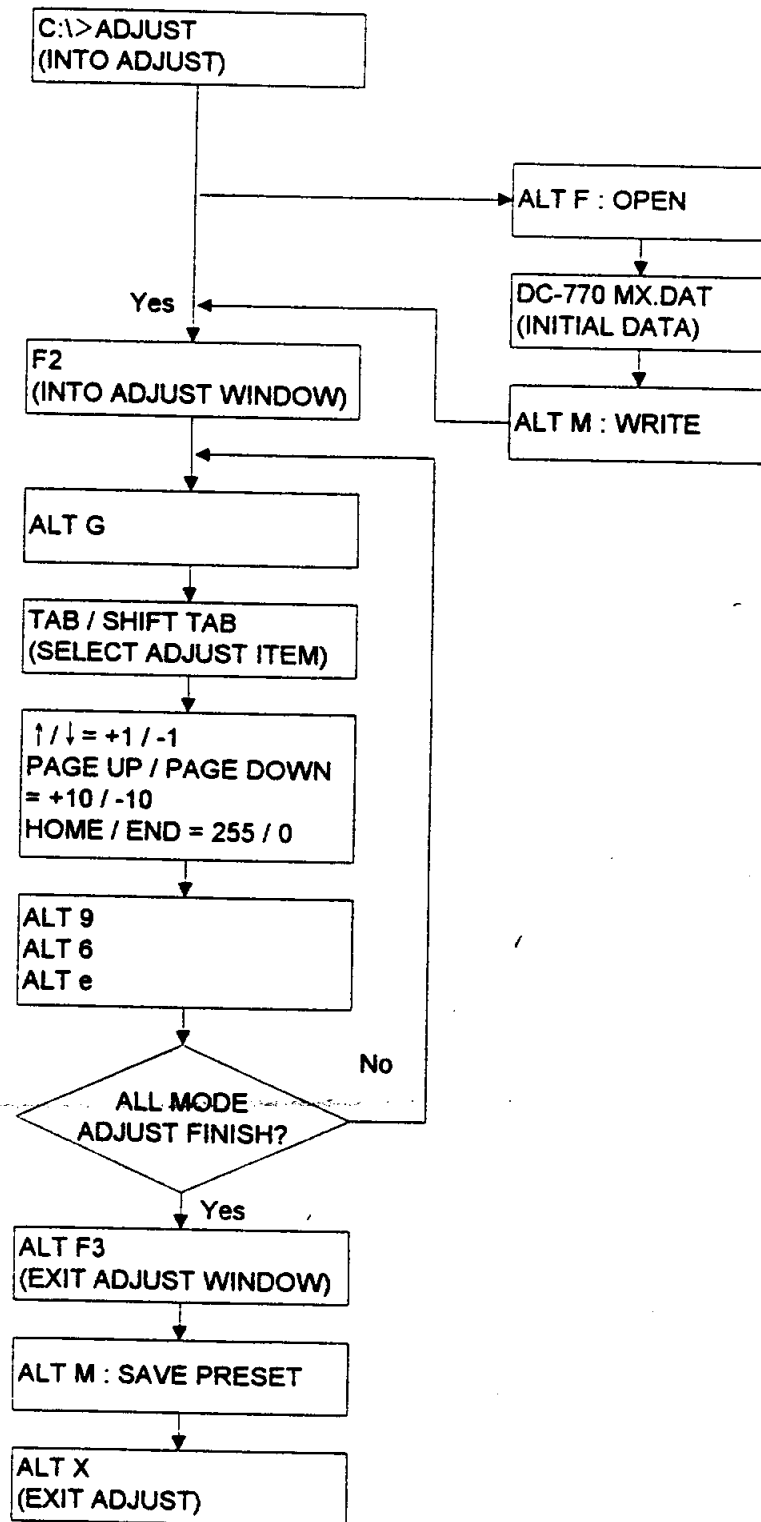
(ADJUST WINDOW)

- 2.1.5 ALT G : GET DATA : Read E²PROM data (one mode)
- 2.1.6 ALT 9 : SAVE 9300K : Save color 9300K adjust data
- 2.1.7 ALT 6 : SAVE 6500K : Save color 6500K adjust data
- 2.1.8 ALE e : SAVE GEOMETRY : Save geometry adjust data
- 2.1.9 ALT F3 : Exit adjust window

2.2 Adjust Item

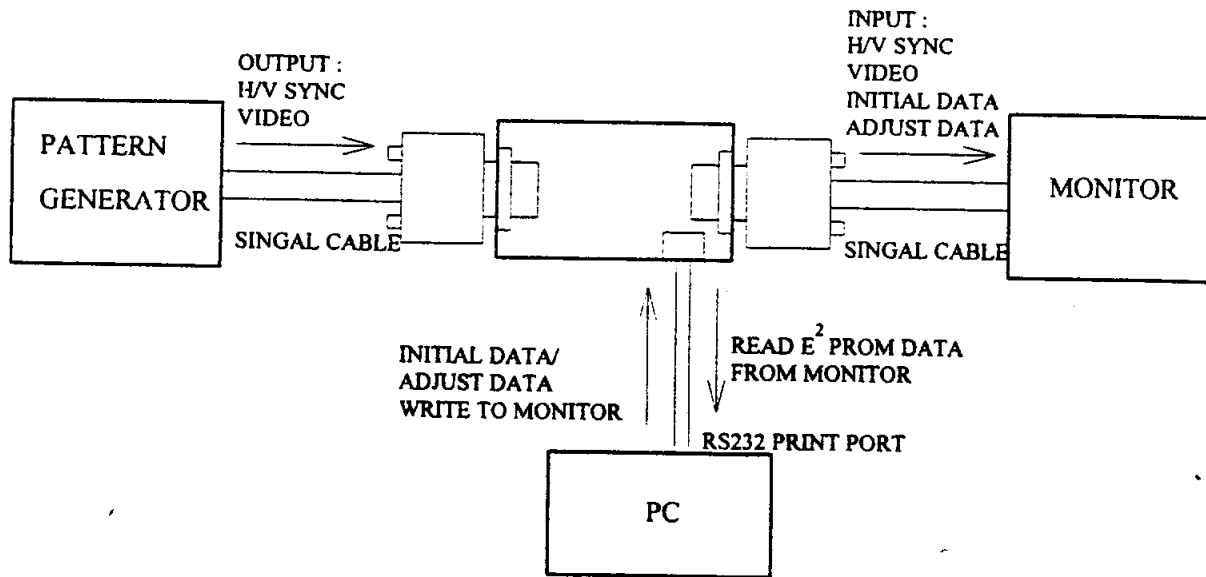
H-POSITION	CONTRAST
H-SIZE	BRIGHTNESS
V-POSITION	R CUT-OFF (BIAS)
V-SIZE	G CUT-OFF (BIAS)
SIDEPIN (PINCUSHION)	B CUT-OFF (BIAS)
KEYSTONE (TRAPEZOID)	R DRIVE (GAIN)
ROTATION	G DRIVE (GAIN)
PARALLEL (PARALLELOGRAM)	B DRIVE (GAIN)

3. Fixture Alignment Procedure



ADJUSTING PROCEDURE

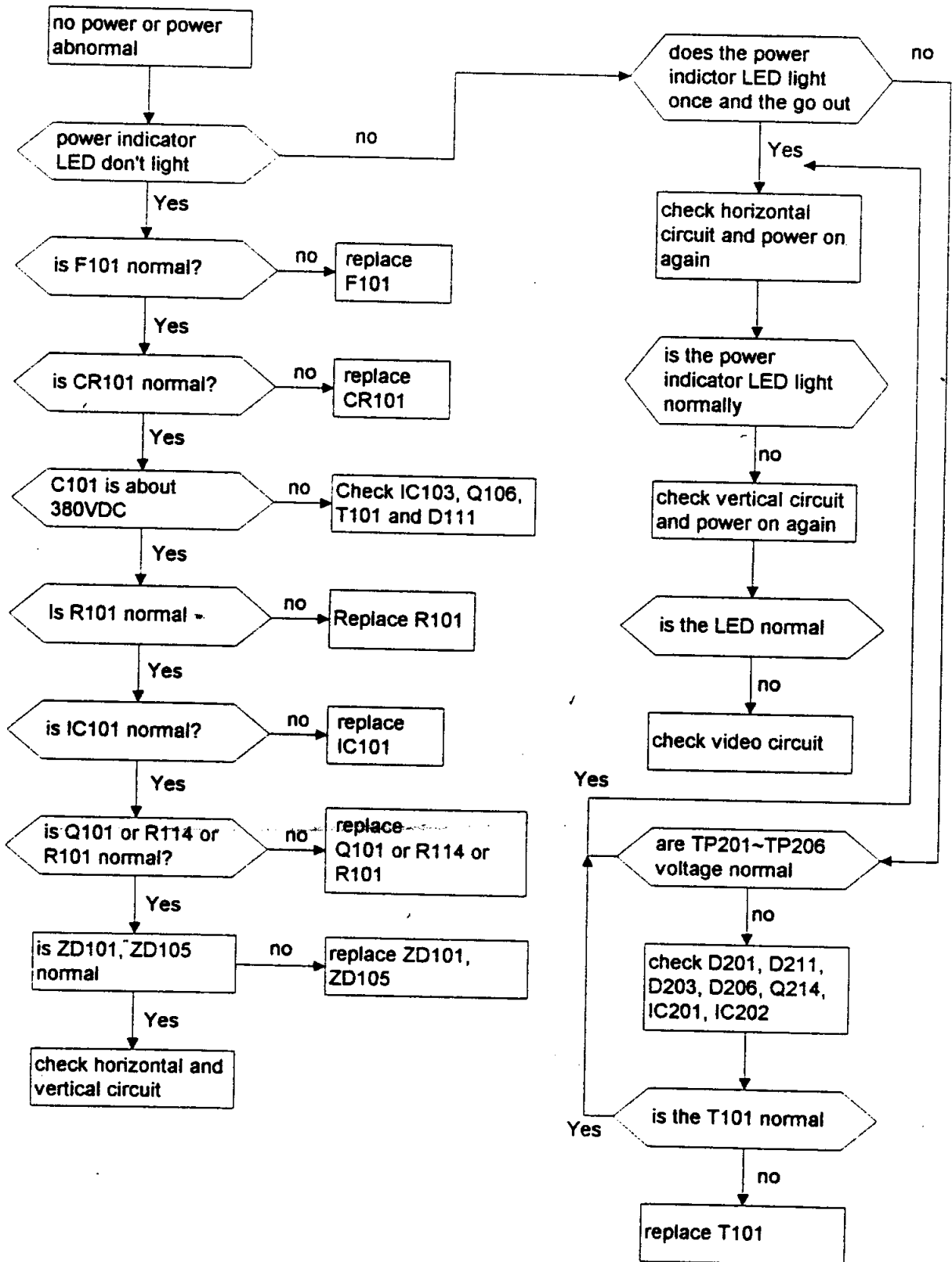
4. Fixture Connect



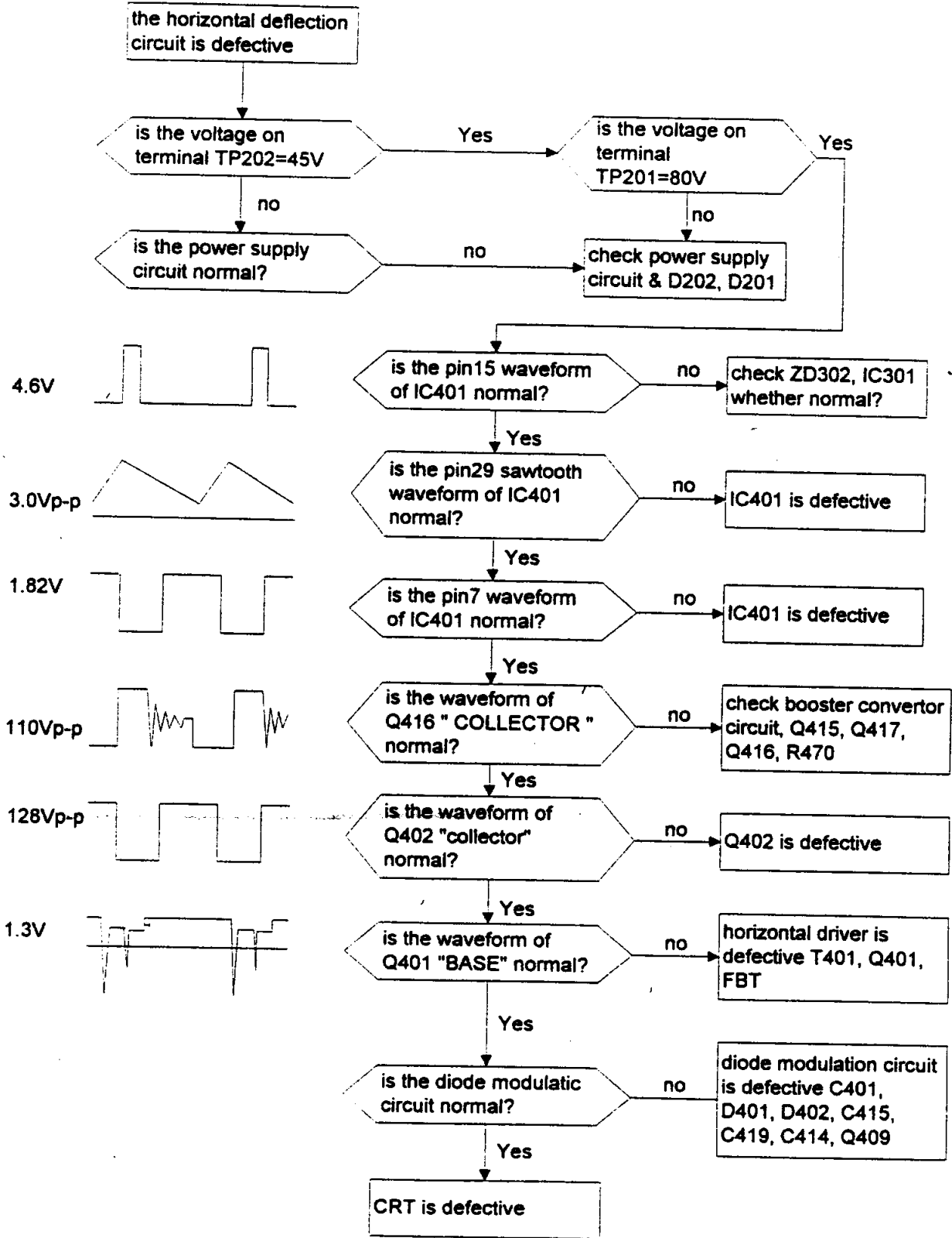
6. Trouble shooting flow chart

- a. Power Supply is Defective
- b. Horizontal Deflection Circuit is Defective
- c. Vertical Deflection Circuit is Defective
- d. The raster don't appear & spot in CRT
- e. One color missing
- f. Video is Defective
- g. OSD is Defective

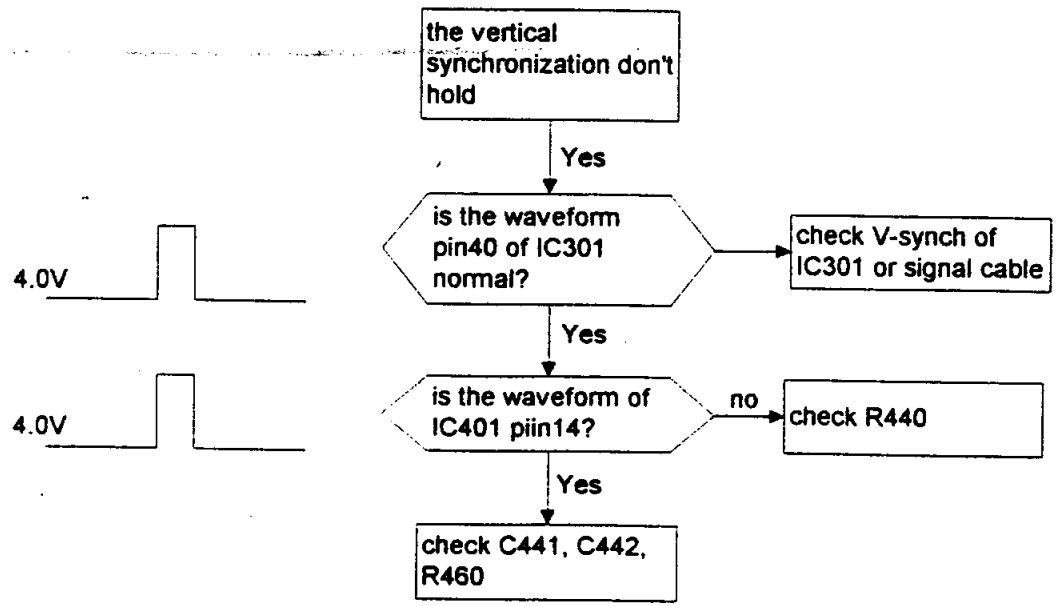
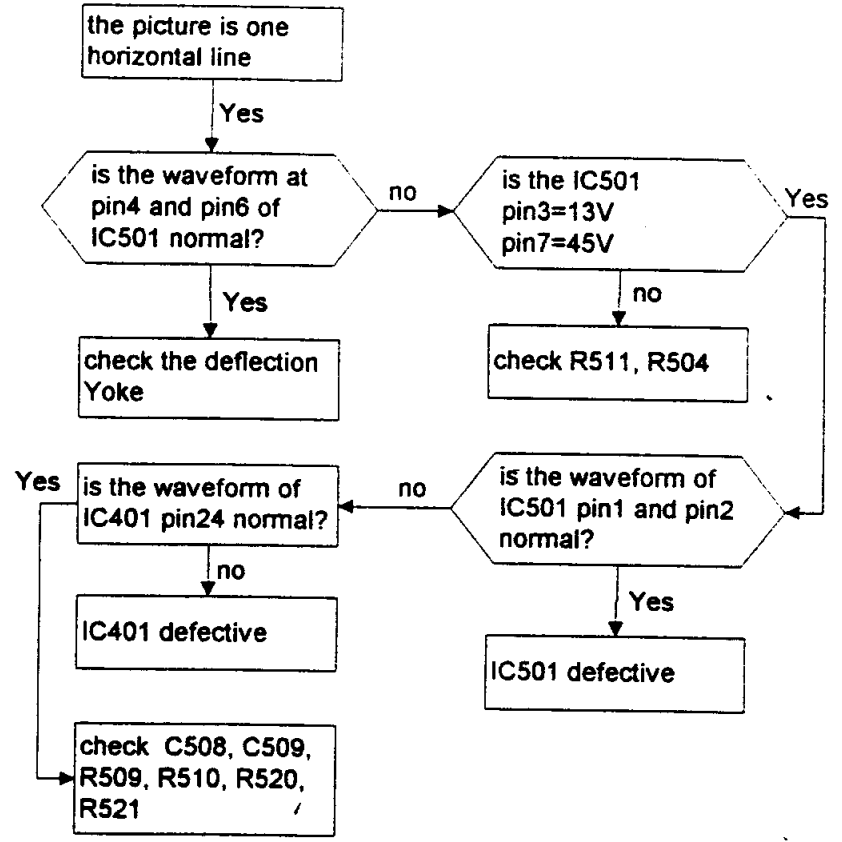
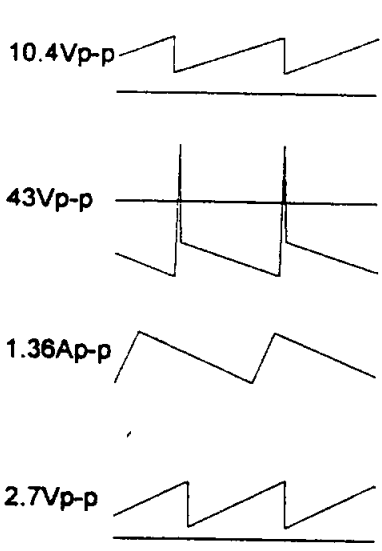
a. Power Supply is Defective



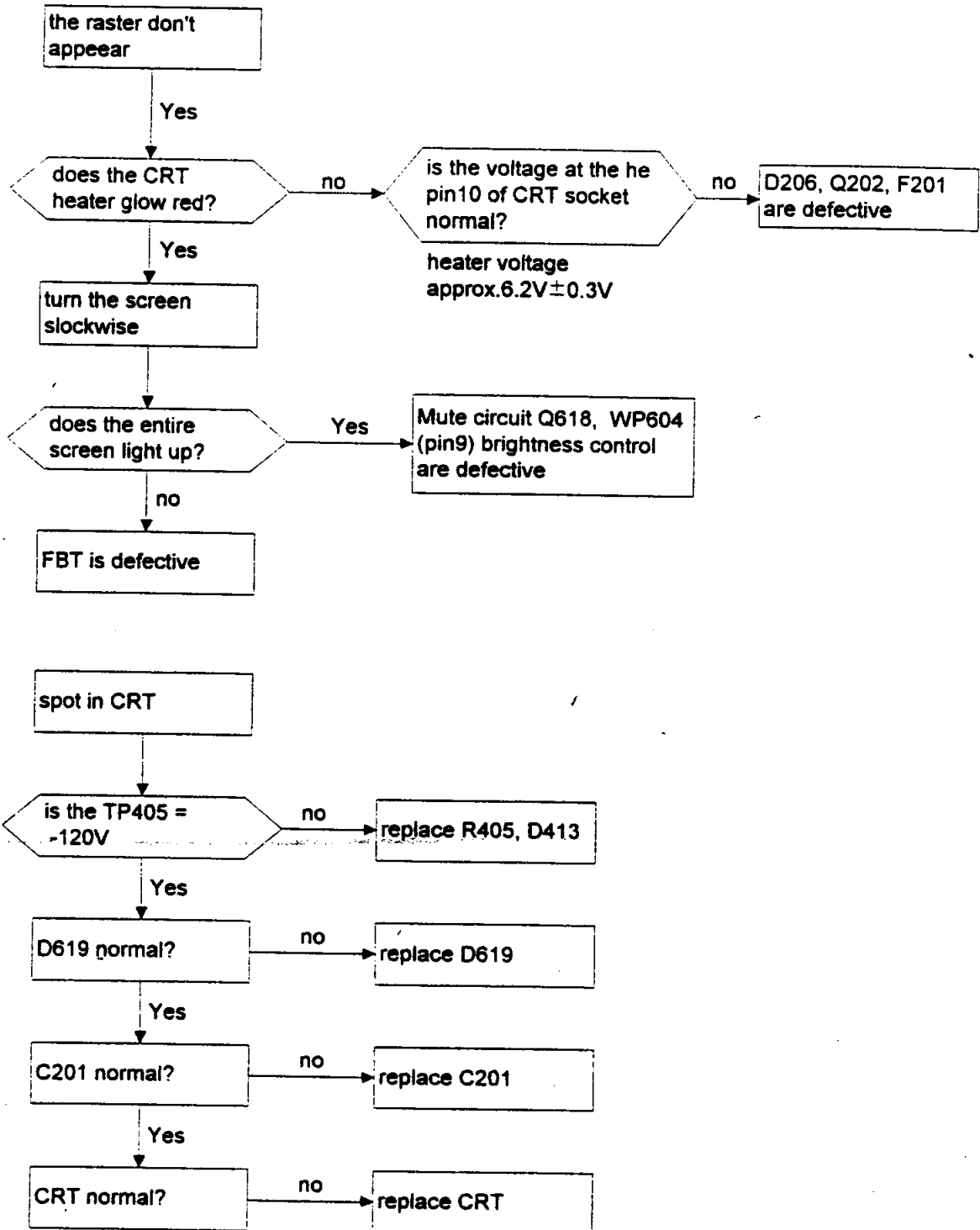
b. Horizontal Deflection Circuit is Defective



C. Vertical Deflection Circuit is Defective

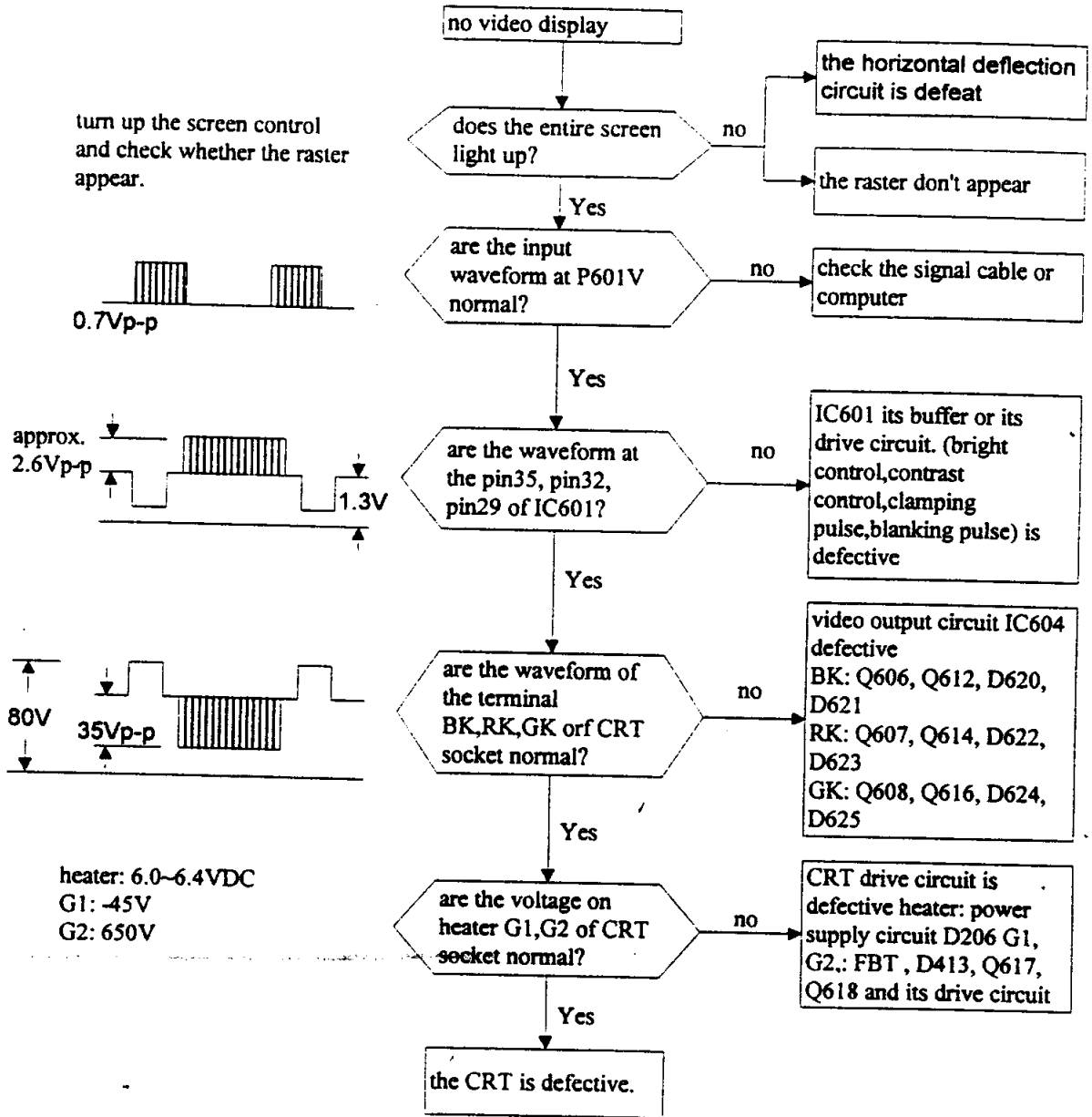


d. The raster don't appear & spot in CRT



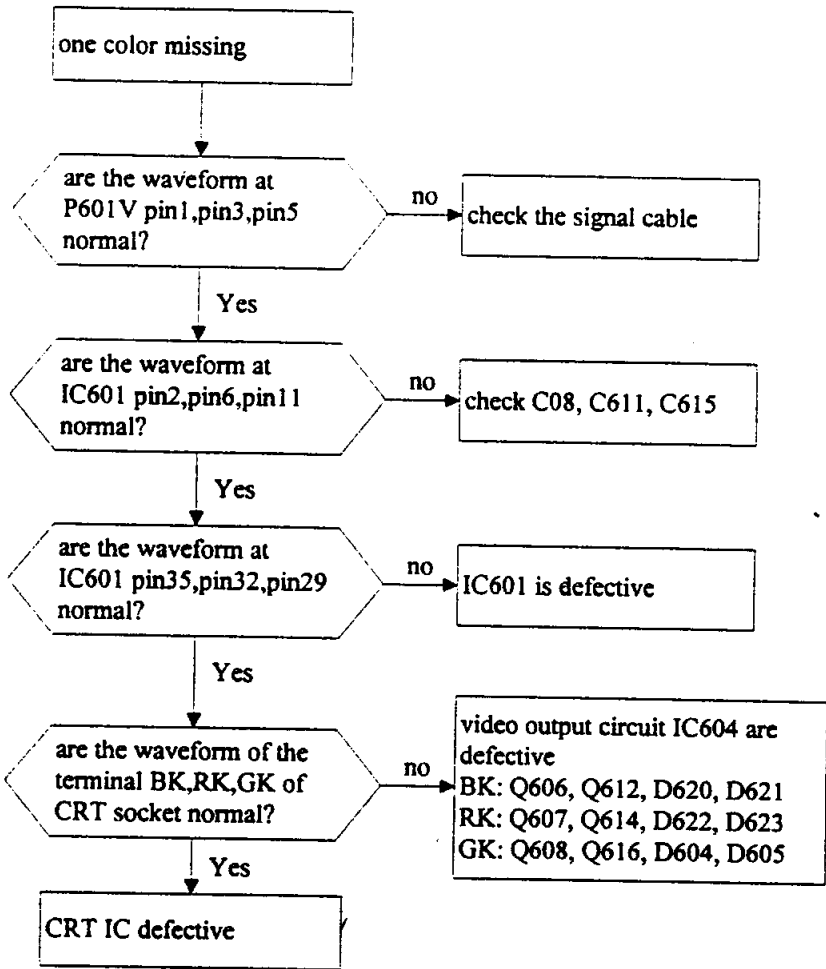
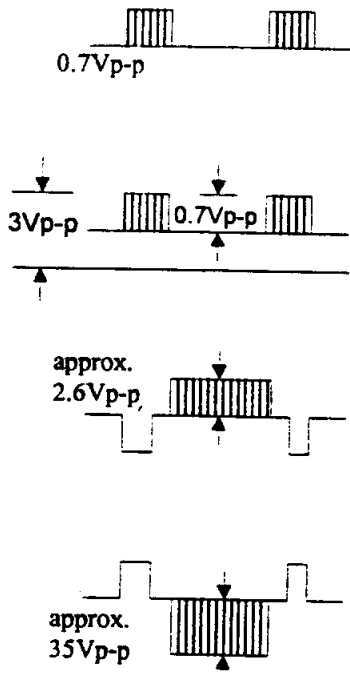
TROUBLE SHOOTING FLOW CHART

e. One Color missing



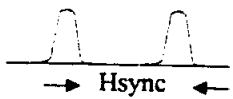
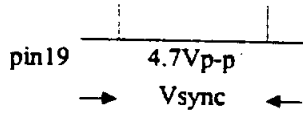
TROUBLE SHOOTING FLOW CHART

f. Video is Defective



TROUBLE SHOOTING FLOW CHART

g. OSD is Defective



press control bottom, IC301 transfer CS, SCL, SDA clock pulse to IC603

press control bottom



no OSD or OSD abnormal

M35045



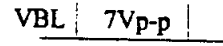
are the pin19 (Vsync) pin18(Hsync) of IC603 normal?

no

check pin3(OHS) of WP602B pin3(VBL) of WP604 whether normal ?

Yes

are the pin4(CS) pin5(SCK) pin6(SIN) of IC603 normal?



no

Yes

is the pin12 BLNK pulse of IC603 normal?

no

IC603 is defective

Yes

are the pin13, pin15, pin17 OSD video output of IC603 normal?

no

IC603 is defective

Yes

IC601 is defeat

are the pin9(CS) pin16(SCK) pin10(SIN) of IC301 normal?

Yes

IC603 is defective

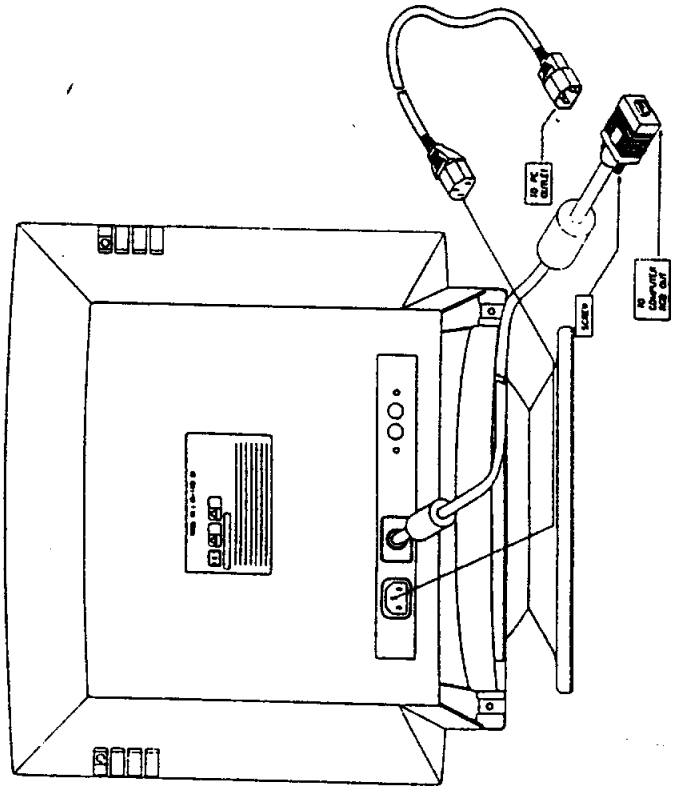
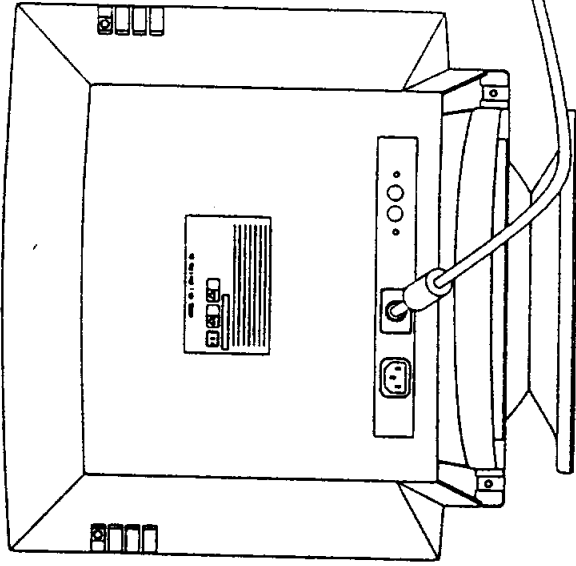
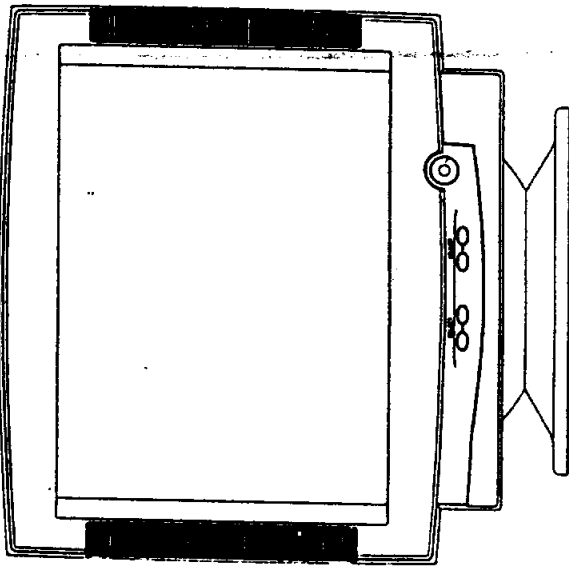
no

IC301 is defective

Mechanical assembly

- Outline drawing
- Explode drawing
- FBT assembly drawing
- Packing assembly
- CRT Grounding wire assembly

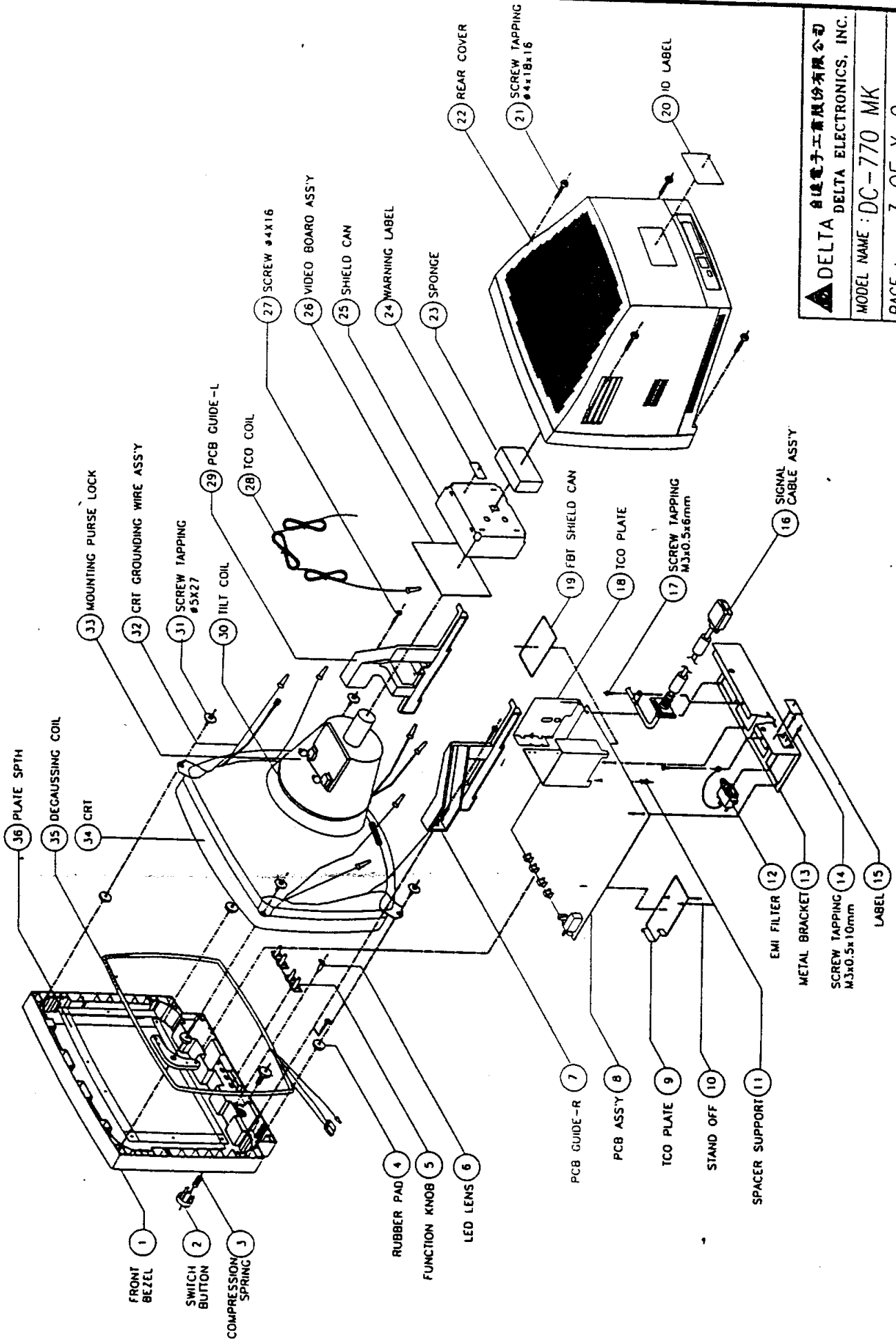
SD7704CM



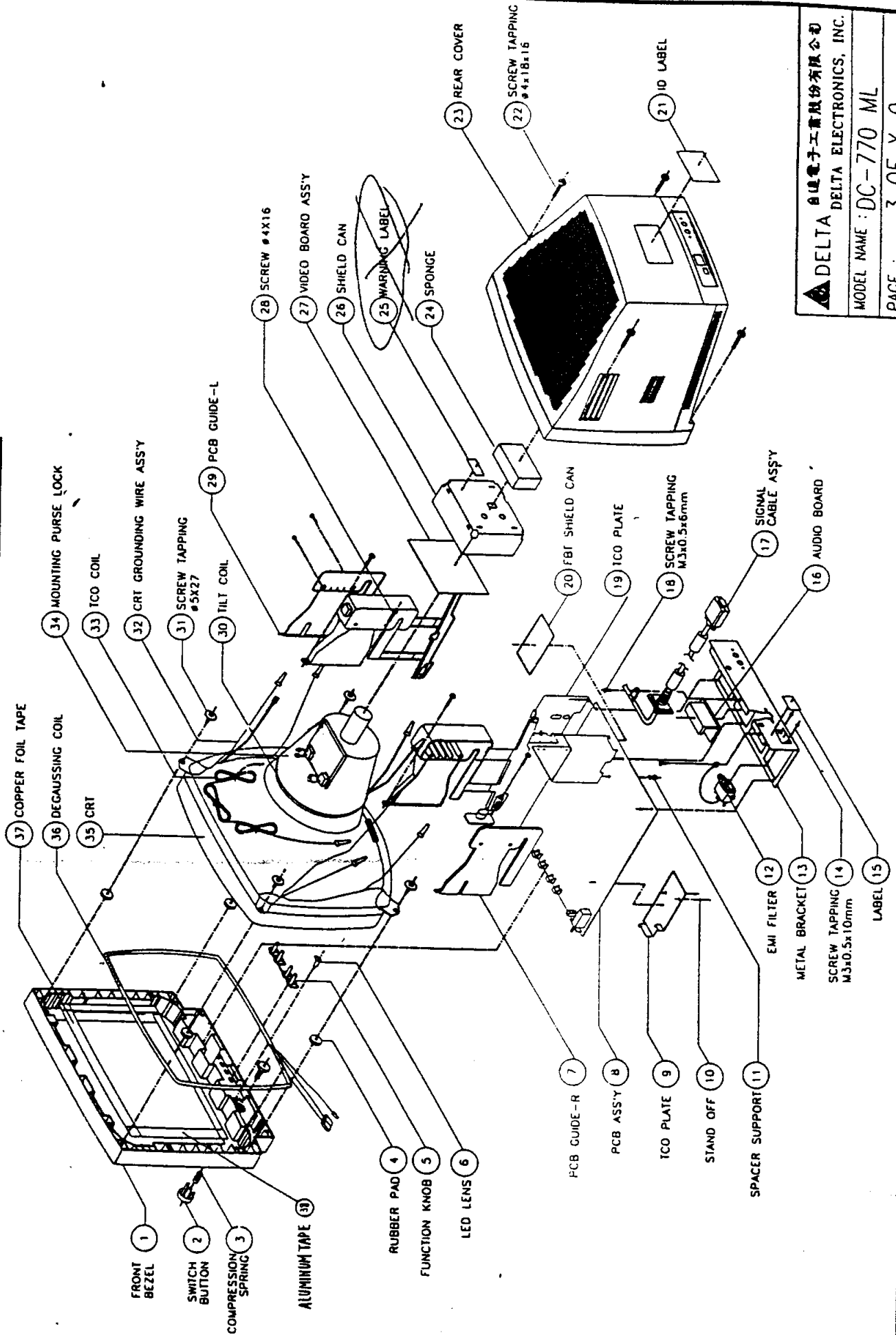
NOTE : UNLESS OTHERWISE SPECIFIED

1. 後殼確實蓋妥後方可上鎖 4 顆螺絲 (P/N : 31090210XX)
2. REMEMBER TO ADHERE ID LABEL (P/N : 3200125700) ON THE BACK SIDE OF REAR COVER.
3. MAKE SURE THE MOTION BETWEEN TILT AND SWIVEL IS SMOOTH, WITHOUT SOUJAKS AND GAPS, APPLY LUBRICANT ONTO FRICTION SURFACE OF SWIVEL DEVICES IS ACCEPTABLE.
4. PACKING MATERIAL HAVE TO MEET ENG., DEPT., SPEC.
5. 外觀檢驗請參考：外觀檢驗規範 10000-0151.

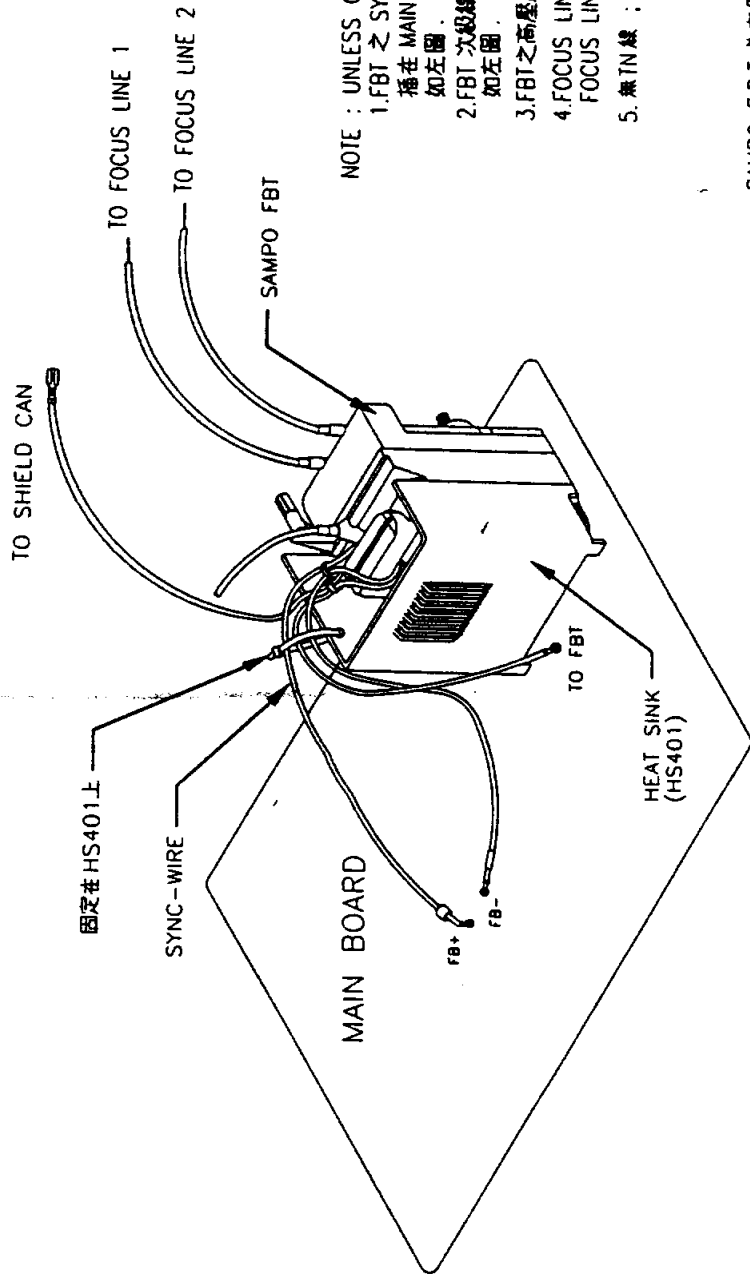
SD7704C



SD7704CM



SD7704CM



NOTE : UNLESS OTHERWISE SPECIFIED

1. FBT 之 SYNC-WIRE 插在 MAIN BOARD 之 FB+ , FB- 兩孔上 , 並注意其方向性 , 如左圖 .
2. FBT 次級線插在 M/B 之 FBT 孔 , 並注意其方向性 , 如左圖 .
3. FBT 之高壓線 請勿碰到其它零件 請整線時特別注意
4. FOCUS LINE (RED) CONNECTOR TO 2(V/B) ; FOCUS LINE (WHITE) CONNECTOR TO 1(V/B).
5. 無 TN 線 ; HS401 為 L 型 .

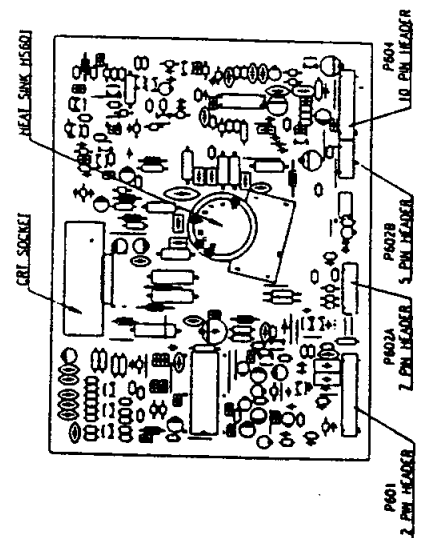
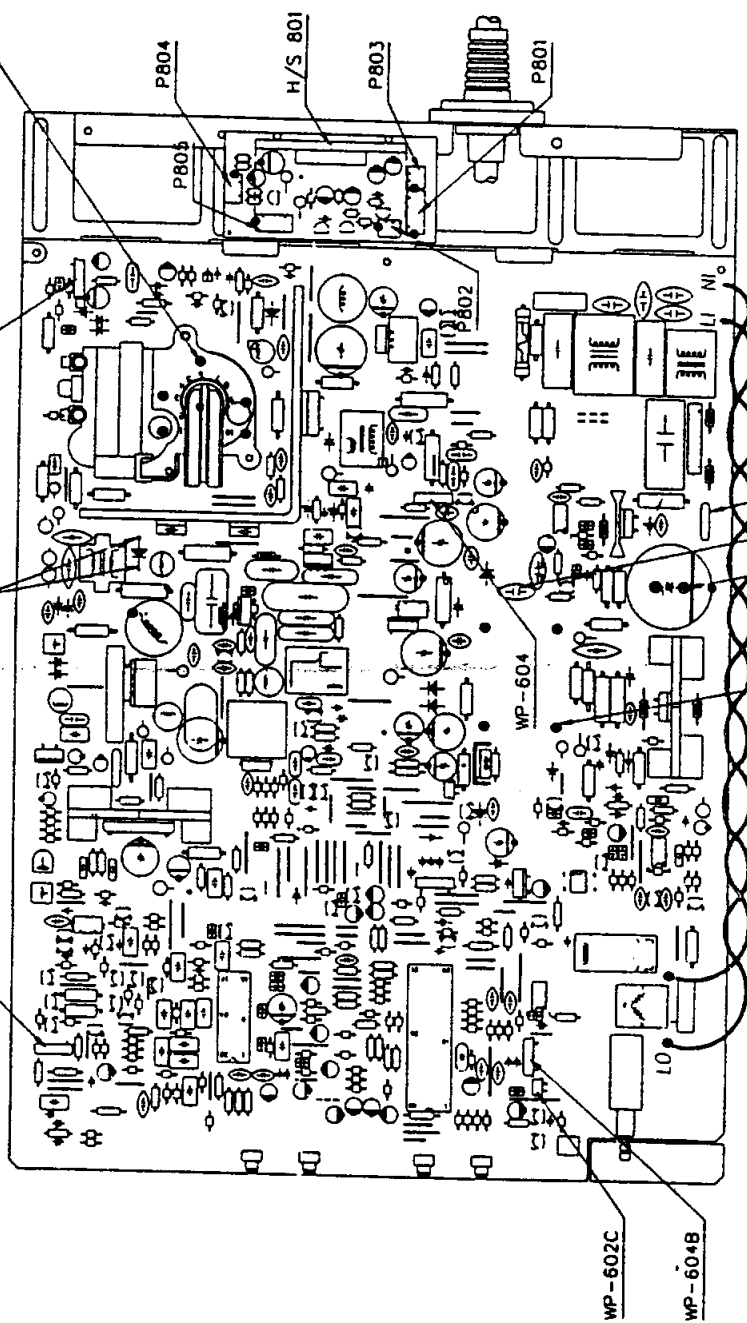
SAMPO F.B.T 為左圖 :

1. FB+ 加套管以利辨別

FOR SAMPO FBT

SD7704CM

(b) MOUNTING 5 RIVETS ON CAPACITOR T401: PIN 1, 3, 6, 9, 10



NOTE : UNLESS OTHERWISE SPECIFIED

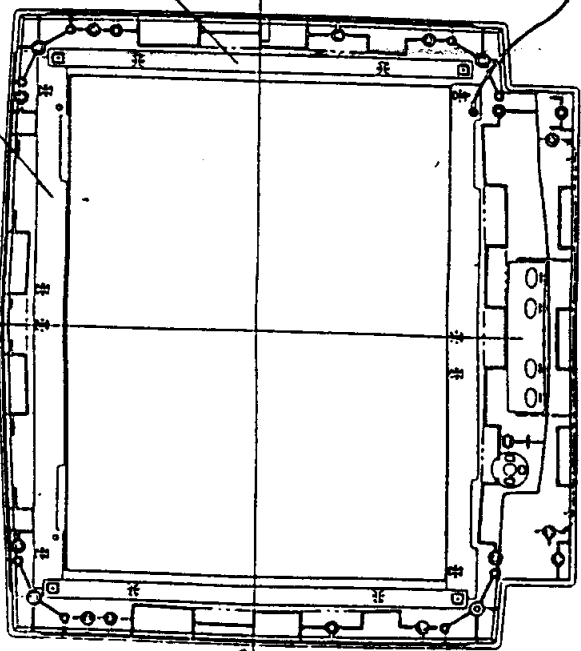
1. WIRE WITH HOUSING (P/N:36700568XX) 5PIN (MAIN BD TO VIDEO BD) 之安裝位置如下:
 - (a): 直接 ON BOARD 過錫罐之 5PINS 插 Housing 插 MAIN BD 之 WP602B
 - (b): 另一端 5 PINS HOUSING 插 VIDEO BOARD P602B 之 HEADER
2. WIRE WITH HOUSING 5 PINS & 5PINS 對應 10 PINS (MAIN BD TO VIDEO BD P/N:36701010XX) 之安裝位置如下:
 - (a): 直接 ON BOARD 過錫罐之兩組 HOUSING 5PIN MAIN BD 之 WP604 5PIN MAIN BD 之 WP604B
 - (b): 另一端 10 PINS 之 HOUSING 插 VIDEO BD 之 P604 HEADER
3. WIRE WITH HOUSING 5PINS & 2PINS WIRE WITH HOUSING (P/N:36700739XX) HOMOLOGIZE 7 PIN (MAIN BD TO VIDEO BD) 之安裝位置如下:
 - (a): 直接 ON BOARD 過錫罐之 5PINS HOUSING 插 MAIN BD 之 WP602A and 2 PIN HOUSING 插 WP602C
 - (b): 另一端 7 PIN HOUSING 插 VIDEO BOARD P602A
4. LED 須先安裝於 LED HOUSING (P/N:33600534XX) 後, (注意其方向性) 再安裝至 MAIN BOARD 之 LED201 上. 注意卡鉤應確實, 勾住前方 螺絲孔中
5. MAIN BOARD P101 安裝 2 PINS CONNECTOR (P/N:30712731XX) FOR DECAUSING WIRE 2 PINS HOUSING.
6. MAIN BOARD P402 安裝 4 PINS CONNECTOR (P/N:30711643XX)
7. POWER SWITCH (P/N:33600627XX) SHOULD BE MOUNTED PROPERLY ON MAIN BOARD SW101.
8. HEAT SINK (P/N:33400345xx) 安裝在 MAIN BD HS401 上
9. LI NILO NO 紅黑線 TWIST (5 圈半) 僅量沿著線繞走 不可超過 HS101.

(c) MOUNTING 2 RIVETS ON CAPACITOR

(e) MOUNTING 2 RIVETS ON CAPACITOR T101: PIN 1, 9, 10, 18

SD7704C

1.75-IN PLATE (P/N:34212295XX,P/N:34212294XX)
5.6-IN PLATE (P/N:34212293XX)X2

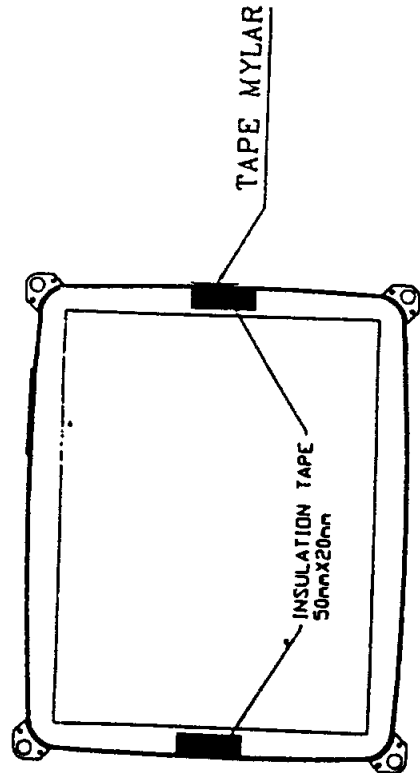


CRT SOURCE: TOSHIBA M41LLJ107XX530(F5G1)

NOTE:

UNLESS OTHERWISE SPECIFIED

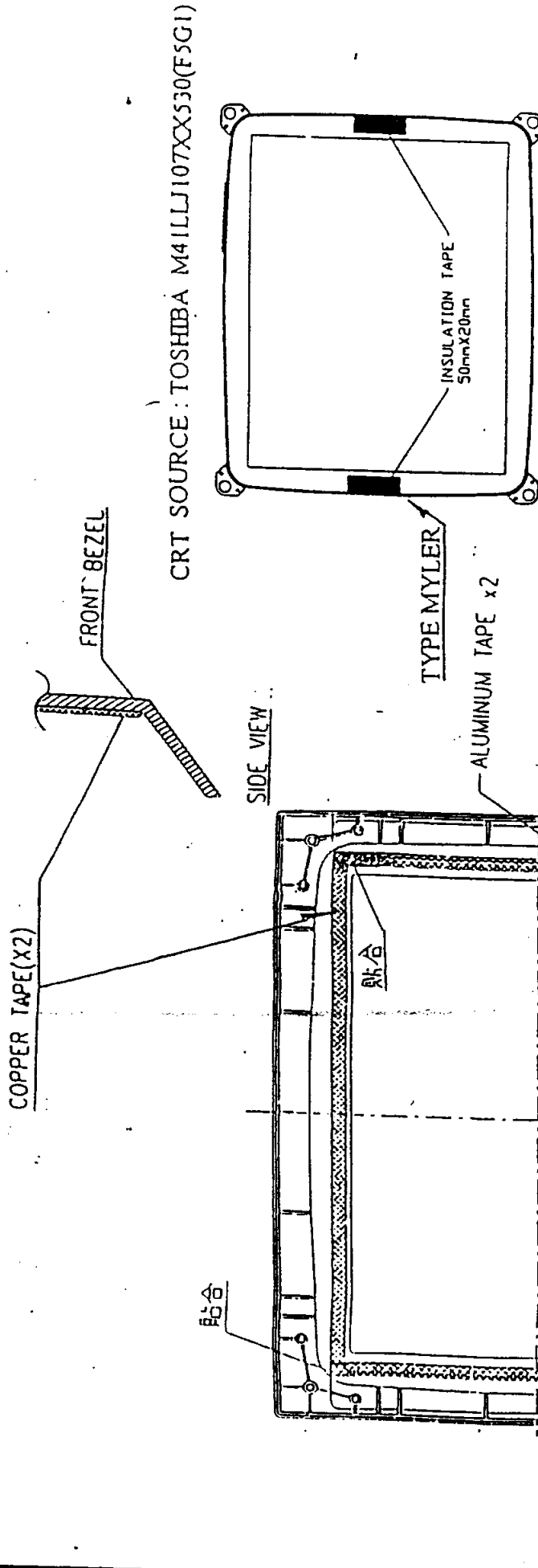
1. 4 PIECES OF TIN PLATE PUT INSIDE OF FRONT BEZEL FIX BY RIB BUT DO NOT EMERGENCE FRONT BEZEL.
2. ATTACHED TYPE MYLAR (P/N:32201316XX) TO THE CRT R/L ALUMINUM TYPE, BUT TAPE MYLAR DO NOT EMERGENCE FRONT BEZEL.



TAPE MYLAR

INSULATION TAPE
50mmX20mm

SD7704CM



CRT SOURCE : TOSHIBA M41LLJ107XX530(F5G1)

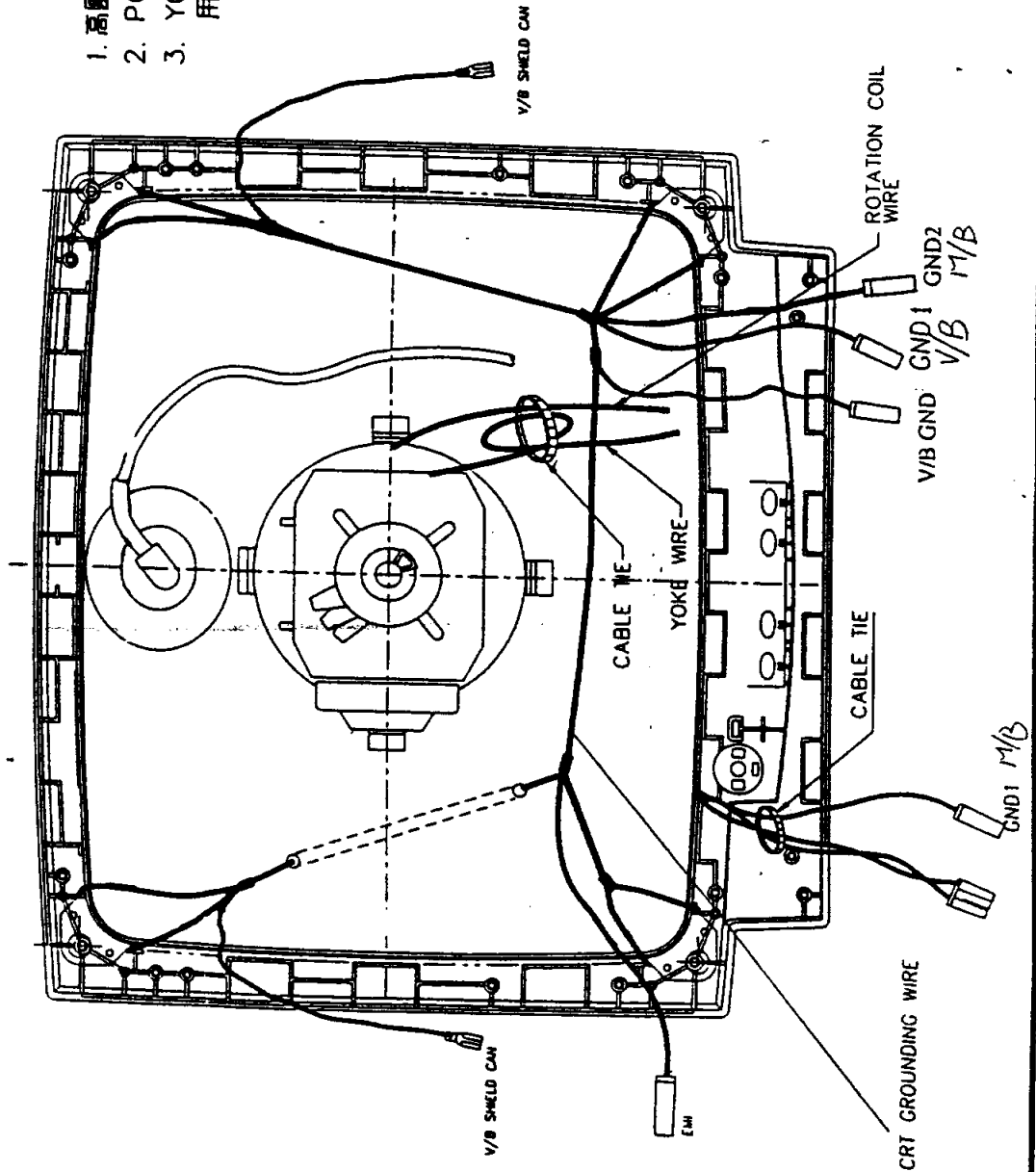
NOTE : UNLESS OTHERWISE SPECIFIED

1. COPPER TAPE 平貼於 FRONT BEZEL 上下
2. ALUMINUM TAPE 平貼於 FRONT BEZEL 左右
3. WIRE WITH HOUSING 焊於左側如圖示
4. 鋁箔膠帶須貼在銅箔膠帶之上
5. ATTACHED TYPE MYLAR (P/N : 32201316XX) TO THE CRT R/L ALUMINUM TYPE, BUT TAPE MYLAR DO NOT EMERGE FROM BEZEL.

SD7704CM

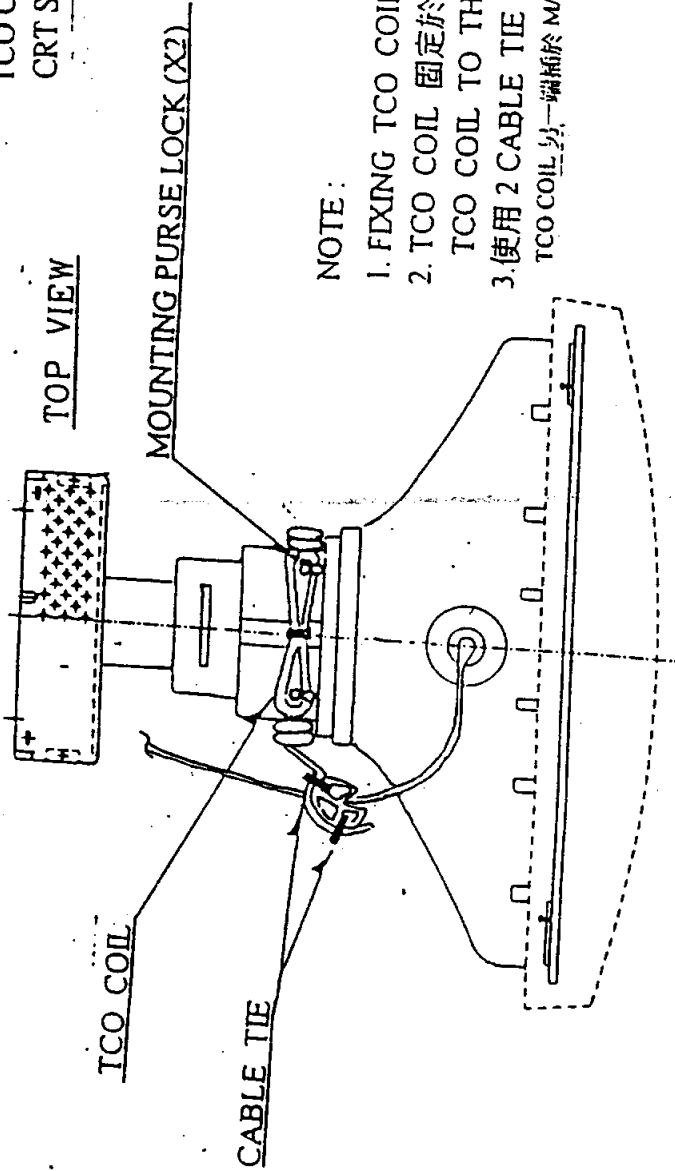
CRT SOURCE :
TOSHIBA M41LLJ107XX530(F5G1)

1. 高壓輸出線端，約 2 呎距離方向（即大約 60'）。
2. POWER CORD 須 SHIELDED.
3. YOKE WIRE 打一圈後與 ROTATION COIL WIRE 用-CABLE TIE 固定



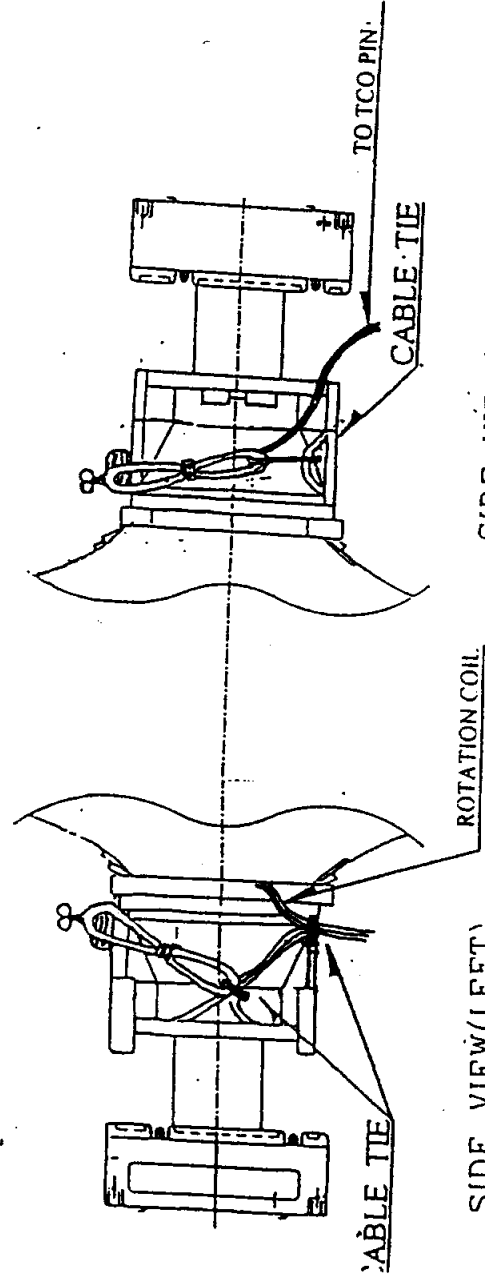
SD7704CM

TCO COIL SHIELDING WIRE ASS'Y VS
 CRT SOURCE : TOSHIBA M4ILLJ107XX530 (F5G1)



NOTE :

1. FIXING TCO COIL WITH 2 MOUNTING PURSE LOCK & 4 CABLE TIE.
2. TCO COIL 固定於 DY 控制盒上, USING 2 CABLE TIE TO BIND THE TCO COIL TO THE DEFLECTION YOKE.
3. 使用 2 CABLE TIE TO BIND THE TCO COIL 尾線與高壓套環, 約半圈以上. TCO COIL 另一端插於 M/B 之 TCO PIN 上.



SIDE VIEW (LEFT)

SIDE VIEW (RIGHT)

SD7704CM

MOUNTING PURSE LOCK

TCO COIL SHIELDING WIRE ASSY VS CRT SOURCE : TOSHIBA

TCO COIL

TO H.V.

DY 控制盒

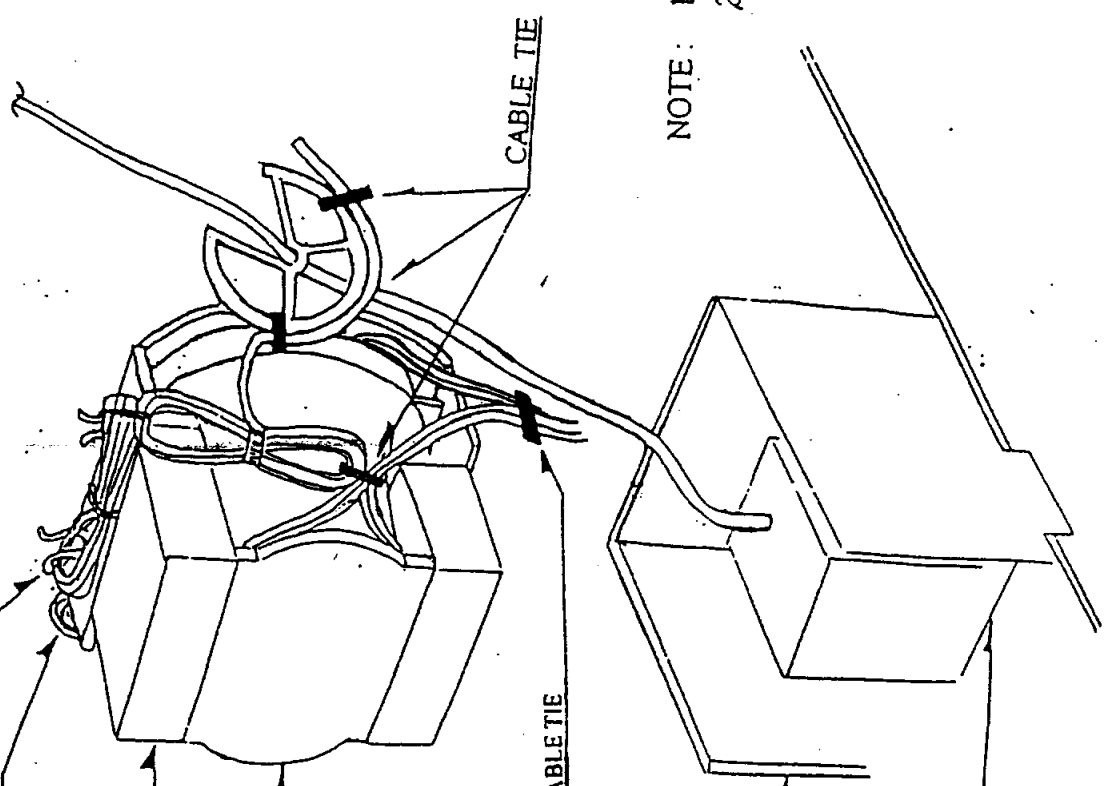
DY

CABLE TIE

CABLE TIE

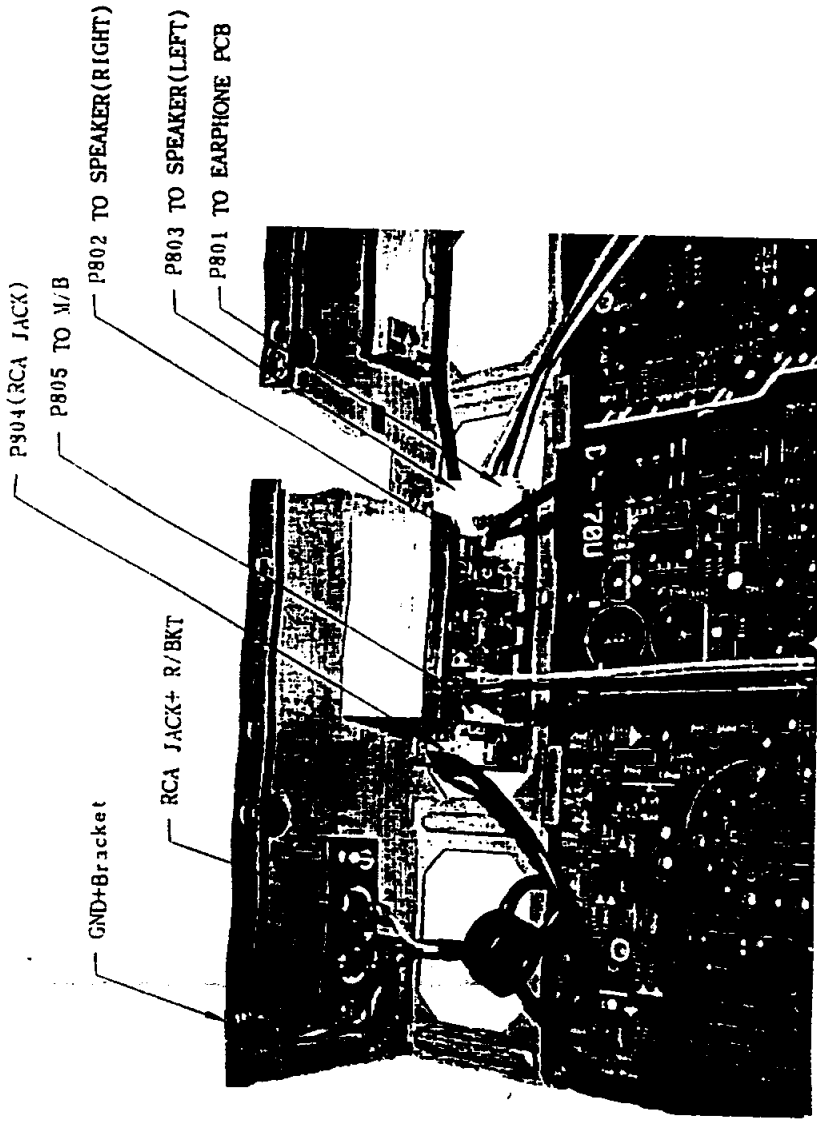
SINK

FBI




NOTE: 1. MOUNTING PURSE LOCK 位置應在DY控制盒前面角落
2. 高壓線接於與DY控制盒上方, TCO COIL 小行

SD7704CM



Note: Unless Otherwise Specified:

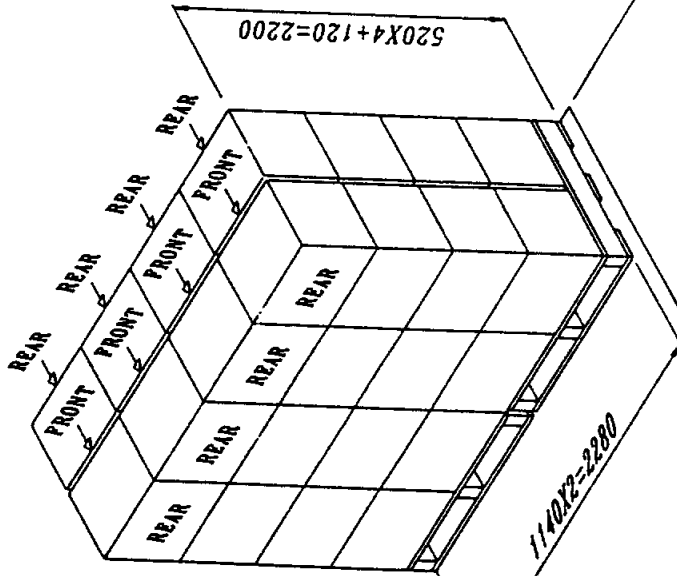
- (1) 將AUDIO Board用2PCS Screw P/N:3109010100固定Rear Bracket上。
- (2) 將RCA Jack 用2PCS Screw P/N:3109010100固定在Rear Bracket上，將GND Wire 用相同 Screw 固定在Bracket上端。
- (3) P801~P805按圖示插入。

 DELTA 台灣電子工業股份有限公司 DELTA ELECTRONICS, INC.	
MODEL:	DC-770 ML
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REV.	00

SD7704CM

20' CONTAINER'S PACKING
FOR 17" MONITOR
PALLET (P/N:3520015700) 20 呎
裝載數量共 160 台

40' CONTAINER'S PACKING
FOR 17" MONITOR
PALLET (P/N:3520015700) 40 呎
裝載數量共 320 台



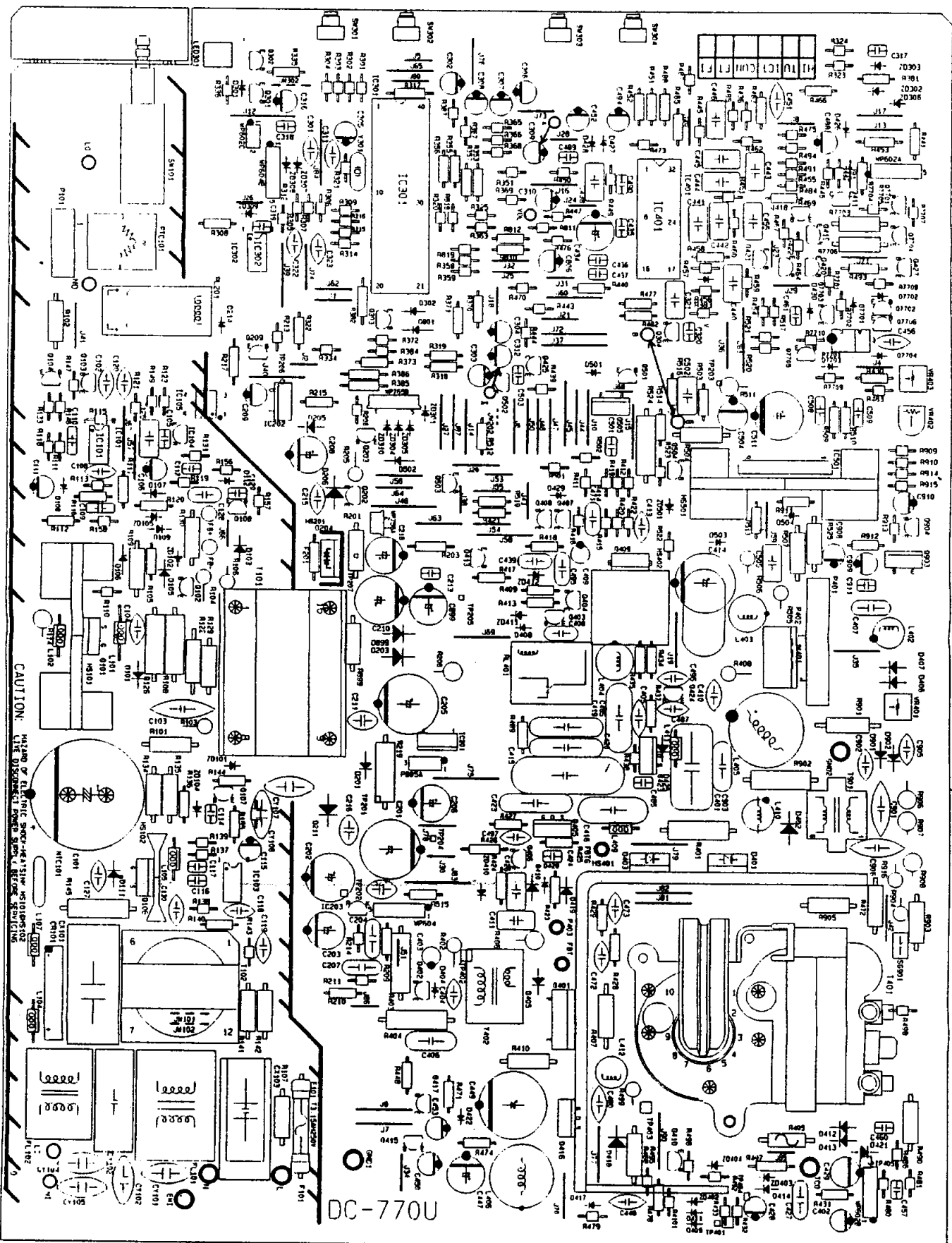
1140X5=5700 (20' CONTAINERS)
1140X10=11400 (40' CONTAINERS)
5898 (40' CONTAINERS)
11980 (40' CONTAINERS)

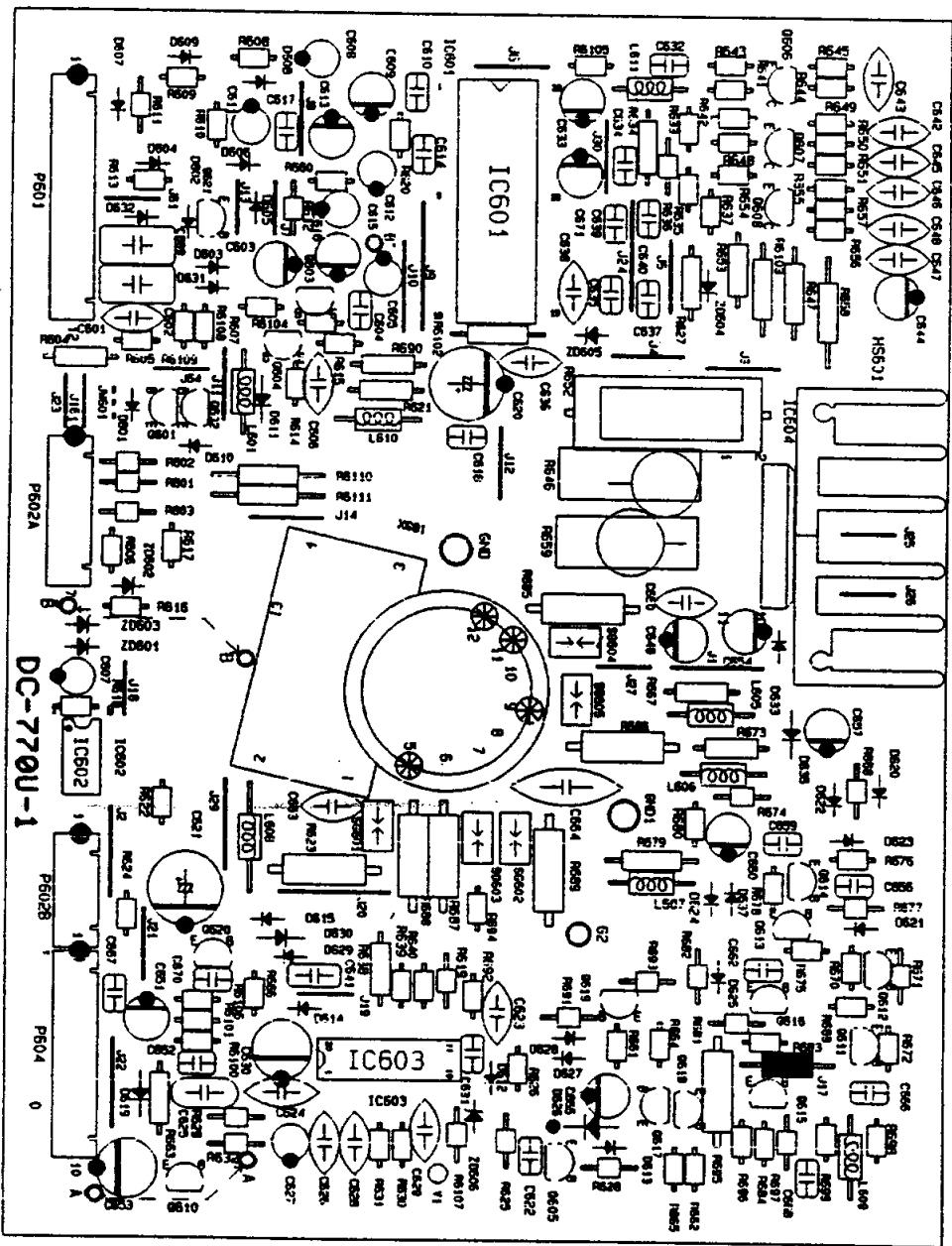
2280

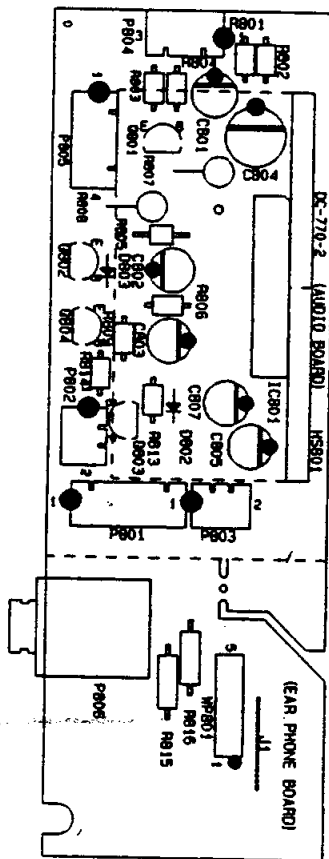
DELTA 台達電子工業股份有限公司
DELTA ELECTRONICS, INC.

PART NO. DC-770 ML

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RECOMMENDED SERVICE PARTS AND PRICE LIST

MODEL NO.: SD7704C / SD7704CM

THIS LIST IS VALID FOR MASS-PRODUCTION

SYMBOL NO.	DESCRIPTION	SPECIFICATION	PART NO.
R406	RES MF 2W 1 J		0143108203,05
R114	RES MF 2W 0.22 J		0143229203,05
R511	RES MF 2W .22 J		0143229203,05
R126	RES MF 2W 3K J		0143302002,03,05,10
R145	RES MF 2W 0.33 J		0143339002,03,05,10
R646	RES MF 3W 1.5K J		0153152617
R652	RES MF 3W 1.5K J		0153152617
R659	RES MF 3W 1.5K J		0153152617
R106	RES FUSING MF 1/2W .22 J		0190200403,06
R101	RES FUSING MF 1W .22 J		0190300403,06
R129	RES HI-VOL 1/2W 1.5M F	PHILIPS	0651464014
R135	RES HI-VOL 1/2W 1.5M F	PHILIPS	0651464014
RL201	RELAY 240VAC/12VDC 5A DPST	OMIT-SS-212LM	0720060501
RL201	RELAY 240VAC/12VDC 5A DPST	VB-12MBU-5	0720060607
RL401	RELAY 240VAC/12VDC 5A SPDT	OUDE-SS-112D	0720140001,07
Y301	CRYSTAL 8MHZ 30PPM 30PF	HC-49/U 8MHZ	0730240212
F101	FUSE TSC 3.15A UL SEM PIG	5HTP3.15	0805340601,02,04
PTC101	PTC R=100&14 OHM 25A	DGC3R14M	0900090018,16,124
NTC101	NTC R=8 OHM L 3A	SCK-083	0910800211,16
CY107	CAP Y CD 400VAC 1KP K B I		1100045003,07,32
C405	CAP CD LD 2KV 270P K B		1155084012
C101	CAP AL 450V 100U M 105C		1430036914,1410036908
C449	CAP AL LD 200V 100U M 105C		1433027007
C419	CAP PMV 400V .27U J		1763156206,15
C419	CAP MP 400V .27U J		1764156821
C416	CAP PP 630V .01U J		1803106006
CR101	DIO BRD 600V 4A	D3SB60	2000111604
CR101	DIO BRD 600V 4A	KBJ406G	2000141612,03
D105	DIO FRD 1A 600V D41	RGP10J	2010101601,19
D425	DIO FRD 1A 600V D41	RGP10J	2010101601,19
D103	DIO FRD 1A 200V D41	UF4003	2010271201
D405	DIO FRD 1A 200V D41	UF4003	2010271201
D101	DIO FRD 1A 800V D41	UF4006	2010271801
D901	DIO FRD 1A 800V D41	UF4006	2010271801
D201	DIO FRD 1A 1000V	BYV26E	2010282001

RECOMMENDED SERVICE PARTS AND PRICE LIST

MODEL NO.: SD7704C / SD7704CM

THIS LIST IS VALID FOR MASS-PRODUCTION

SYMBOL NO.	DESCRIPTION	SPECIFICATION	PART NO.
D206	DIO FRD 2A 100V D15	EGP20B	2010351001
D203	DIO FRD 2A 200V D15	EGP20D	2010351207
D418	DIO FRD 2A 200V D15	EGP20D	2010351207
D211	DIO FRD 4A 600V T220C	FMGG26S	2010381601
D111	DIO FRD 2.3A 600V	BYM26C	2010391601
D402	DIO FRD 5A 400V D201AD	EGP50G	2010481401
D401	DIO FRD 5A 1500V T220	5TUZ47C	201112115
ZD105	DIO ZEN .5W 17.5~18.3V 2A	HZ18-2	2030120309,16
ZD402	DIO ZEN .5W 17.5~18.3V 2A	HZ18-2	2030120309,16
ZD102	DIO ZEN .5W 36.4~38V D35	HZ36-3	2030120616
ZD410	DIO ZEN .5W 36.4~38V D35	HZ36-3	2030120616
ZD601	DIO ZEN 0.5W 5.0~5.1V D35	HZ5C1	2030120816,2030121609
ZD606	DIO ZEN 0.5W 5.0~5.1V D35	HZ5C1	2030120816,2030121609
ZD301	DIO ZEN .5W 5.5~5.8V D35	HZ6B1	2030122516
ZD302	DIO ZEN .5W 6.15V 2.44% D35	HZ6C2	2030129016
ZD305	DIO ZEN .5W 6.15V 2.44% D35	HZ6C2	2030129016
ZD101	DIO ZEN .5W 19.6~20.4V D35	BZX79-B20,133	2031920409
D106	DIO SW 0.5A 75V D0-35	1N4148	2040010001,02,03,04
D430	DIO SW 0.5A 75V D0-35	1N4148	2040010001,02,03,04
D504	DIO SW 0.5A 75V D0-35	1N4148	2040010001,02,03,04
D604	DIO SW 0.5A 75V D0-35	1N4148	2040010001,02,03,04
D630	DIO SW 0.5A 75V D0-35	1N4148	2040010001,02,03,04
D7704	DIO SW 0.5A 75V D0-35	1N4148	2040010001,02,03,04
D801	DIO SW 0.5A 75V D0-35	1N4148 [SD7704CM]	2040010001,02,03,04
R457	DIO SW 0.5A 75V D0-35	1N4148	2040010001,02,03,04
ZD309	DIO SW 0.5A 75V D0-35	1N4148	2040010001,02,03,04
D421	DIO SI 1A 600V D41	1N4005	2050011601
Q425	TR 40V 0.8A T92	MPS2222AM	2100001001
Q7703	TR 50V 0.5A T92	2SC1213ACTZ	2100006001
Q7705	TR 50V 0.5A T92	2SC1213ACTZ	2100006001
Q802	TR 30V 0.1A T92 160~320	2SC458CTZ [SD7704CM]	2100026001
Q108	TR 60V 0.15A T92	2SC1815Y	2100039001
Q203	TR 60V 0.15A T92	2SC1815Y	2100039001
Q424	TR 60V 0.15A T92	2SC1815Y	2100039001
Q501	TR 60V 0.15A T92	2SC1815Y	2100039001

RECOMMENDED SERVICE PARTS AND PRICE LIST

MODEL NO.: SD7704C / SD7704CM

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SYMBOL NO.	DESCRIPTION	SPECIFICATION	PART NO.
Q605	TR 60V 0.15A T92	2SC1815Y	2100039001
Q620	TR 60V 0.15A T92	2SC1815Y	2100039001
Q804	TR 60V 0.15A T92	2SC1815Y [SD7704CM]	2100039001
Q904	TR 60V 0.15A T92	2SC1815Y	2100039001
Q402	TR 180V 0.7A T92 140~280	2SC3332S,T	2100044010,110
Q606	TR 40V 0.5A T92	PH2369	2100063013
Q608	TR 40V 0.5A T92	PH2369	2100063013
Q102	TR 250V 50mA T0-92 hfe=50min	BF422	2100067006
Q615	TR 250V 50mA T0-92 hfe=50min	BF422	2100067006
Q202	TR 20V 1A T92 120~240	2SB562CTZ	2110003001
Q801	TR 50V 2A T92	2SA1680 [SD7704CM]	2110019001
Q7702	TR 35V 0.5A T92	2SA562TM	2110022001
Q7706	TR 35V 0.5A T92	2SA562TM	2110022001
Q612	TR 250V 50mA T0-92 hfe=50min	BF423	2110037006
Q617	TR 250V 50mA T0-92 hfe=50min	BF423	2110037006
Q107	TR 50V .15A T92 TP	2SA1015Y	2110041106
Q301	TR 50V .15A T92 TP	2SA1015Y	2110041106
Q407	TR 50V .15A T92 TP	2SA1015Y	2110041106
Q427	TR 50V .15A T92 TP	2SA1015Y	2110041106
Q502	TR 50V .15A T92 TP	2SA1015Y	2110041106
Q503	TR 50V .15A T92 TP	2SA1015Y	2110041106
Q604	TR 50V .15A T92 TP	2SA1015Y	2110041106
Q610	TR 50V .15A T92 TP	2SA1015Y	2110041106
Q7701	TR 50V .15A T92 TP	2SA1015Y	2110041106
Q7704	TR 50V .15A T92 TP	2SA1015Y	2110041106
Q803	TR 50V .15A T92 TP	2SA1015Y [SD7704CM]	2110041106
Q409	TR 100V 5A T220	TIP122	2120067020
Q401	TR 1500V 10A T220	BU2520AF	2120068013
Q903	TR 1200V 50mA T0-220A	2SC4686A	2120086006
LED301	LED 5mm ORG/GRN 3PIN	EL339-1EGW	2300062706
IC105	PHOTO 32V 6PIN 100~200% VDE	TCDT1101C	2310017107,07107
Q106	FET 500V 8A T220	IRF840	2430007001
Q405	FET 200V 8.5A T220	YTA630,IRF630	2430044006,10
Q423	FET 200V 8.5A T220	YTA630,IRF630	2430044006,10
Q405	FET 250V 12A T220-FN	FS12KM-5	2430121033
Q416	FET 250V 12A T220-FN	FS12KM-5	2430121033
Q423	FET 250V 12A T220-FN	FS12KM-5	2430121033

RECOMMENDED SERVICE PARTS AND PRICE LIST

MODEL NO.: SD7704C / SD7704CM

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SYMBOL NO.	DESCRIPTION	SPECIFICATION	PART NO.
Q101	FET 700V 10A T220	FS10UM-14A	2430135033
IC104	IC VOL ADJ T92 3PIN	TL431CLP	2500004001,02,03
IC203	IC VOL ADJ T92 3PIN	TL431CLP	2500004001,02,03
IC202	IC REGU 5V 1.5A T220 3PIN	MC7805CT	2500005001,04,10,11,14
IC202	IC REGU 5V .5A T220 3PIN	L78M05CV	2500005710
IC201	IC REGU 12V 1.3A T0-220F 4P	PQ12RD11	2500041220
IC201	IC REGU 12V .8A T220F 4P	PQ12RD08	2500087020
IC101	IC PWM 8PIN	UC3842N	2510004001,03,106
IC103	IC POWER-FACTOR CNTRER 8PIN	TDA4862	2510067009
IC401	IC AUTOSYNC DEFL CTRL 32P	TDA4858	2510077047
IC604	IC TRIPLE CRT DRIVER T11A	CVA2411TX	2520069044
IC501	IC VERT DEFLECTION 9PIN	TDA4866	2530015016
IC801	IC 2*3W AUDIO AMP SOT-13PIN	TDA7057AQ [SD7704CM]	2530032016
IC603	IC OSD DIP-20	M35045-090SP	2530033507
IC601	IC 3CH VIDEO PRE-AMP 36PIN	M52743ASP	2530063107
IC602	IC 1K EEPROM 8PIN	24LC21A	2610099237
IC302	IC EEPROM 8K 8PIN	ST24C08B1	2610185042
IC301	IC MASK UP 40P	NT6861-6021	2610240618
T101	X'FMR SMT 300uH J	SMT-39RV-798A [SD7704CM]	2801502900
T101	X'FMR SMT 300uH J	SMT-39RV-799A [SD7704C]	2801503000
T402	X'FMR DT 50mH K	DT-E19-05	2802901100
T901	X'FMR DT 2.4mH MIN	DT-E19-32	2802908100
T102	CHOKE CE L=470uH	CE-28RV-05	2806530200
L402	CHOKE 3.9mH K	E-4840A	2816800210
L406	CHOKE CD 120uH K		2816903700
FL101	LF 25mH MIN	LFZ2805V04	2817202700
L405	CHOKE WIDTH COIL 85uH		2820200600
L403	CHOKE LINEAR COIL3.5uH	D12058	2820401101
L404	CHOKE LINEAR COIL3.5uH	D12058	2820401101
T401	FLYBACK TRANSFORMER 17"	FEA 726	2850003805
X101	EMI FILTER 115/250V 3A	03GEEW3J	2900301701
	CRT 17" SS .28 90D AREC575	M41LLJ107XX630	0741700804
	POWER CORD 3PIN	[USA]	3072000900
	POWER CORD	[GERMANY]	3072037900
	POWER CORD	[US]	3072038000
	POWER CORD	[S'PORE]	3072038100
	POWER CORD	[AUSTRALIA]	3072038200

RECOMMENDED SERVICE PARTS AND PRICE LIST

MODEL NO.: SD7704C / SD7704CM

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SYMBOL NO.	DESCRIPTION	SPECIFICATION	PART NO.
	AUDIO CABLE	[SD7704CM]	3072020701
	FRONT BEZEL ASSY (PC+ABS)	[SD7704C]	3360017500
	FRONT BEZEL ASSY (PC+ABS)	[SD7704CM]	3360101000
	REAR COVER PC+ABS GY-7454		3360021500
	SWIVEL BASE ASSY ABS 94HB		3368034300
	CARTON 560*560*503	[SD7704C]	3510287000
	CARTON 560*560*503	[SD7704CM]	3510287100
	END BLOCK-L [CUSHION]		3500039300
	END BLOCK-R [CUSHION]		3500039400
	MANUAL	[USA]	3520312502
	MANUAL	[EUROPE]	3520312601
	MANUAL	[S'PORE]	3520312701
	CHASSIS	[SD7704C]	5610008800
	CHASSIS	[SD7704CM]	5610008900
	SIGNAL CABLE		3072007800