SERVICE MANUAL

PV430T

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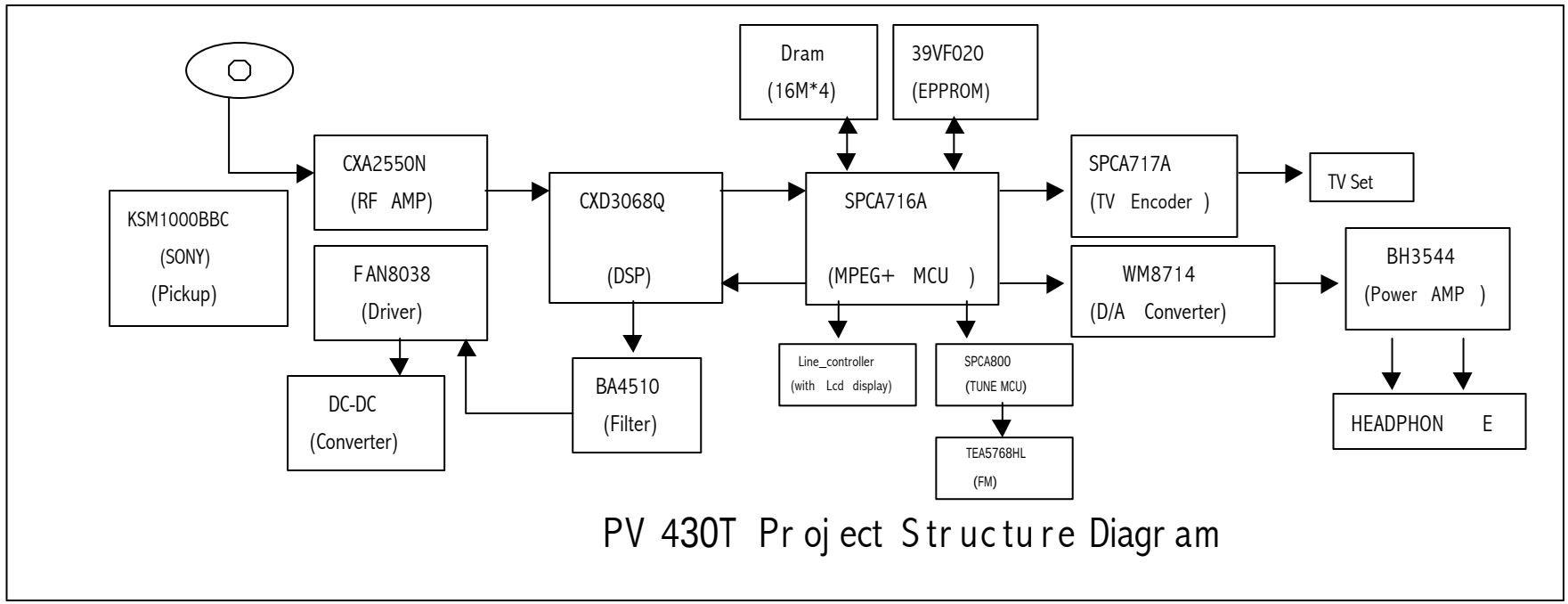
CON TEN TS



PV 430T Project Structure Diagram

Briefness introduce main part of system :

Pickup : KSM-1000BBC CD-deck compatible with CD, CD-R, CD-RW,Can be playing 12 cm & 8cm Discs.

RF AMP : The CXA2550N is 3-Beam Head Amp IC of SONY, Compatible with CD, CD-R.

Driver : The FAN8038 is 4CH H bridge driver and S8520 is step down DC-DC contvertor.

DSP : The CXD3068Q is a digital signal processor LSI for CD player, this LSI incorporates a digital servo.

MPEG : The SPCA716A A /V decoder is a single-chip VCD decoder, this LSI incorporates a MCU.

TV ENCODER : The SPCA717A is a single-chip VCD encoder.

D/A : The WM8714 is a digital to analog converter.

Power AMP : The BH3544 is audio power AMP, so that to driver headphone.

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技　術　資　料

TECHNICAL DATA

MODEL : KSM1000BBC

＊ 当該モデルの参考資料であり、この資料の内容は将来変更する可能性があります
Sony reserves the right to change specification of products and discontinue products without notice.

担 当 者 印

ソニー株式会社　光デバイス事業部
SONY CORPORATION
OPTICAL DEVICE DIVISION

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1）適　用
Scope of Document

◆ **本仕様書は、コンパクトディスク用光学ドライブユニットＫＳＭ１０００ＢＢＣについて規定します。なお、業務用には使用できません。**
This document describes the specification of drive unit KSM1000BBC, for use in compact disc player. This model is not for professional use.

◆ **本仕様書の内容において改善の為、双方事前に協議して変更することがあります。**
The provisions of this document may be altered upon agreement between both parties.

◆ **不都合事項発生時は、本仕様書記載事項にもとづき双方協議の上、解決実施するものとします。**
If any disagreement should arise, these two parties shall meet in good faith to resolve the problem.

◆ **本仕様書を満足する範囲内において、改良・性能の向上の為、部品等の一部を変更する場合がありますので御了承下さい。**
Within the range of these specifications, parts are subject to change without notice for technical improvement.

◆ **次の事項をお守りの上で、当デバイスを組み込んだセット商品あるいは半完成品を市場に出荷して下さい。お守り頂けない場合、当社では責任を負うことが出来ません。**
Please be sure to observe the following each time you deliver your finished and /or semi-finished products containing the device(s). Otherwise, SONY may not be able to assume the responsibility for things to happen.

- **本仕様書に定めた条件以内で使用して下さい。**
  Always use the device(s) within conditions given in the specifications.
- **当デバイスに追加工を行わないで下さい。**
  Never given additional process to the device(s).
- **セットと一体で不要輻射を測定して、規制値を満足していることを確認して下さい。**
  Make sure that a finished product containing SONY device(s) is in compliance with the rules and regulations for spurious radiation.
- **デバイスをセットに実装した状態にてレーザー出力を測定して、セットからの漏れ光が規制値を満足していることを確認して下さい。**
  Measure leak laser output from a finished product containing the device(s) and make sure that the finished product is in compliance with applicable requirements.

2）仕　様
General Specifications

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2-1. 光学的仕様 Optical Specifications

◆ **対物レンズ** Objective lens

焦点距離	Effective focal length (f)	3.85 mm
開口数	Numerical aperture (NA)	0.45
作動距離	Working distance (WD)	1.8 mm

◆ **半導体レーザー** Semiconductor laser

レーザー波長 Laser wavelength(λ) 775 ～ 815 nm

◆ **サーボエラー信号の検出法** Servo error detection methods

フォーカスエラー Focus error **：ＳＳＤ法** SSD method
トラッキングエラー Tracking error **：３スポット法** 3-SPOT method

2-2. 機械的仕様 Mechanical Specifications

◆ **外形寸法** Dimensions Figure 2

◆ **質　量** Mass 35g **（標準値）** Standard value

◆ **対物レンズ動作方向** Direction of objective lens movement

Figure 1.**参照** see Figure 1

フォーカス方向 Focus Direction
フレキ端子 ⑬ (ﾌｫｰｶｽ＋)にプラス電圧が印加された場合、対物レンズはディスクに近づく方向に動く。
A positive voltage applied to pin ⑬ (FCS＋) of the flex moves the objective lens toward the disc.

トラッキング方向 Tracking Direction
フレキ端子 ⑮ (ﾄﾗｯｷﾝｸ＋)にプラス電圧が印加された場合、対物レンズはディスクの内周方向に動く。
A positive voltage applied to pin ⑮ (TRK＋) of the flex moves the objective lens toward the center of the disc.

◆ **対物レンズ可動範囲** Range of objective lens movement

フォーカス方向 Focus Direction
面振れ± 0.5 mm **相当のディスクが再生可能なこと。**
The disc equal to surfacewave ± 0.5 mm should be able to play back.

トラッキング方向 Tracking Direction
± 0.5 mm **以上** or more
（中立位置基準、ディスク上ビームスポット移動量にて規定）
Specified at the datum of center position and the amount of beam movement on the disc.

◆ **送り動作** Slide direction

送りモータ端子 ① にプラス電圧が印加された場合、ピックアップはディスクの外周方向へ動く。
A positive voltage applied to pin ① of sled motor moves the objective lens toward the outer of the disc.

◆ **ピックアップ可動範囲** Pick-up movable distance

機械的内周位置 Mechanical center position ≦ 24 mm
機械的最外周位置 Mechanical the most periphery position ＞ 58 mm

（ターンテーブルセンターから対物レンズセンターまでの距離）
Length between the center of turntable and objective lens

◆ **ターンテーブル動作** Direction of turntable movement

スピンドルモータ端子⑤にプラス電圧が印加された場合、ターンテーブルは時計方向に回転する。
A positive voltage applied to pin ⑤ of spindle motor rotates the turntable clockwise.

2-3. **ピックアップ部電気的仕様** Electrical Specifications of Pick-up

項　　目 Item	**仕　　様** Specifications
レーザー部電源 Power supply for LD	**片　電　源** Single power supply
フォトディテクタ部信号出力 PD signal out put method	**電圧出力** Voltage out put

3）評価条件
Evaluation Conditions

3-1. 姿　勢　Position

重力方向が、図１のＺ軸（－）方向にて規定します。
The negative Z axis is defined as the direction of gravity as shown in Figure 1.

3-2. 環　境　Environment

◆ **温　度** Temperature　22 ± 2 ℃
◆ **湿　度** Relative Humidity　50 ± 5 % RH

但し、判定に疑義が生じない場合には、下記条件で評価してよい。
If no errors occur in evaluation, the following range of conditions is acceptable.

温　度 Temperature　15 ～ 35 ℃
湿　度 Relative Humidity　45 ～ 85 % RH

3-3. 機　器　Equipment

◆ **測定用標準基台** Standard cabinet for measurement
◆ **ＡＰＣ回路** (Figure 4) APC circuit
◆ **標準評価回路** (Figure 5) Standard measurement circuit
◆ **ジッターメーター** Jitter meter
(菊水電子工業製, KJM-6235SA) (KJM-6235SA, KIKUSUI ELE.CO.)
◆ **デジタルマルチメータ** Digital multimeter
◆ **サーボアナライザー** Servo analyzer
◆ **オシロスコープ** Oscilloscope

3-4. ディスク　Disc

ソニー製ガラスディスク：GLD-CR11
Glass disc manufactured by SONY : GLD-CR11

3-5. 電　圧　Voltage

ピックアップ PDIC**部**　V_{CC} = 3±0.1 V
Pick-up PDIC　V_C = 1/2 V_{CC}±0.1 V

4）特性規格
Characteristics Specifications

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4-1. 絶対最大定格 Absolute Maximum Rating

◆ **２軸部** Actuator

項　　目 Item		規　　格 Standard value	備　　考 Remarks
コイル許容電流 Coil current	フォーカス Focus	150 mA RMS	但しﾌｫｰｶｽ＋ﾄﾗｯｷﾝｸﾞの総電流が150mAを越えないこと Focus ＋Tracking total current must be less than 150mA RMS
	トラッキング Tracking		

◆ **レーザーダイオード部** Laser diode

項　　目 Item	規　　格 Standard value	備　　考 Remarks
レーザーダイオード逆電圧 Laser diode inverse voltage	2 V	
ﾓﾆﾀｰ用ﾋﾟﾝﾌｫﾄﾀﾞｲｵｰﾄﾞ逆電圧 Monitor pin photo diode inverse voltage	15 V	

◆ **ＰＤＩＣ部**

項　　目 Item	規　　格 Standard value	備　　考 Remarks
電　源　電　圧 Supply Voltage	6 V	

◆ スピンドル / 送りモータ Spindle/Sled motor

項　　目 Item		規　　格 Standard value	備　　考 Remarks
許容電圧 Allowable voltage	スピンドル Spindle	3 V	
	送　り Sled	3 V	

4-2. 使用電圧範囲 Operating Voltage Range

◆ **ＰＤＩＣ部**

項　　目 Item	規　　格 Standard value	備　　考 Remarks
動作電源電圧(Vcc) Operating supply voltage(Vcc)	2.7 ～ 5.5 V	
中点電位電圧(Vc) Neutral point voltage(Vc)	1.3 ～ (Vcc－1.3) V	

4-3. **性能規格** Performance Specifications

4-3-1. **光学ピックアップ部** Optical Pick-up

2軸部 Actuator

低温，高温動作規格は、常温常湿における実測値からの変化量（但し、*は変化率）を示す。
Temperature deviation from room temperature and humidity measurement.
(* : Deviation percentage)

項目 Item		規格 Standard value	温度変化 Temperature Deviation		備考 Remarks
		常温常湿 Room temperature and humidity	- 5°C	+ 55°C	
フォーカス Focus	**直流抵抗** DC resistance	6 ± 1Ω	————		
	低域感度 Sensitivity	$1.5\ ^{+0.65}_{-0.45}$ mm/V	* within ±35%**以内**	* within ±35%**以内**	**5Hzにて規定** Specified at 5Hz
	共振周波数 (fo) Resonant frequency	46 ± 7 Hz	within $^{+7}_{-2}$ Hz**以内**	within $^{2}_{-6}$ Hz**以内**	**Q値MAXにて規定** Specified at maximum Q-value
	Q 値 Q-value	12.5 ± 6 dB	within ±8dB**以内**	within ±7dB**以内**	**Q 値** Q-value=Gain(fo)-Gain(5Hz)
トラッキング Tracking	**直流抵抗** DC resistance	6.3 ± 1Ω	————		
	低域感度 1) Sensitivity	$0.48\ ^{+0.22}_{-0.15}$mm/V	* within ±35%**以内**	* within ±35%**以内**	**5Hzにて規定** Specified at 5Hz
	共振周波数 (fo) Resonant frequency	46 ± 8 Hz	within $^{+8}_{-2}$ Hz**以内**	within $^{+2}_{-6}$ Hz**以内**	**Q値MAXにて規定** Specified at maximum Q-value
	Q 値 Q-value	14.5 ± 6 dB	within ±8dB**以内**	within ±7dB**以内**	**Q 値** Q-value=Gain(fo)-Gain(5Hz)

1) **ディスク上ビームスポットにて規定**
Specified at beam spot on the disc.

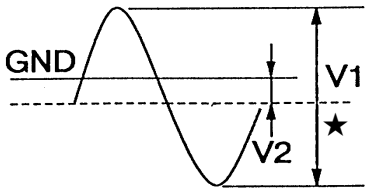
光学部 Optics

低温，高温動作規格は、常温常湿における実測値からの変化量
（但し、*印は変化量、印は実測値）を示す。**
Temperature deviation from room temperature and humidity measurement.
(* : Deviation percentage ** : Actually measured value)

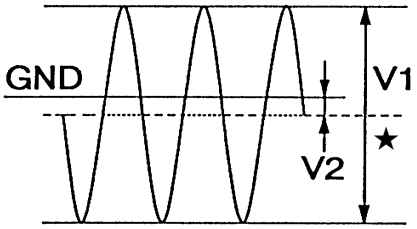
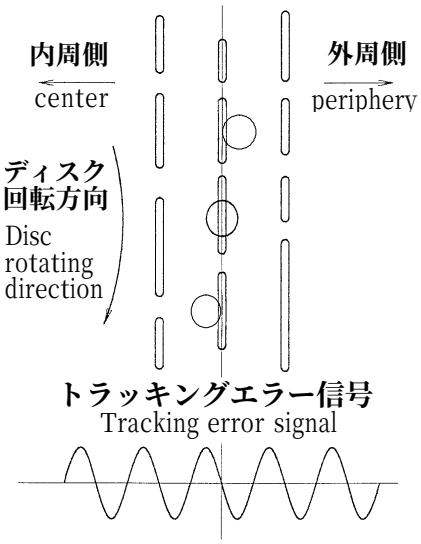
◆ **ＲＦ信号** RF signal

項　目 Item	**規　格** Standard value	**温 度 変 化** Temperature Deviation		**備　考** Remarks
	常 温 常 湿 Room temperature and humidity	- 5℃	+ 55℃	
RF **信号振幅** RF signal amplitude	1.0 ± 0.2 Vp-p	* within ±20%**以内**	* within ±20%**以内**	**ＡＰＣの温特は含まず** APC temperature characteristics excluded
ジッター Jitter	26ns RMS**以下** or less	** 34ns RMS**以下** or less	** 32.5ns RMS**以下** or less	
RF**信号ｵﾌｾｯﾄ電圧** RF signal offset voltage	within 0± 0.25V **以内**	———	———	**ＬＤ ＯＮ時** At LD on.

◆ **フォーカスエラー信号** Focus error signal

項　目 Item	**規　格** Standard value	**温 度 変 化** Temperature Deviation		**備　考** Remarks
	常 温 常 湿 Room temperature and humidity	- 5℃	+ 55℃	
ﾌｫｰｶｽｴﾗｰ信号振幅 Focus error signal amplitude	12± 5 Vp-p	* within ±20%**以内**	* within ±20%**以内**	**ﾌｫｰｶｽｴﾗｰ** P－P 7μm Focus error
デフォーカス Defocus	within 0± 1.2μm**以内**	within ± 1μm**以内**	within ± 1μm**以内**	**ﾃﾞﾌｫｰｶｽ**＝ $\frac{V_2 - F.E._{\text{off set}}^{\text{ｵﾌｾｯﾄ}}}{V_1} \times 7\mu m$ Defocus V_1 : **ﾌｫｰｶｽｴﾗｰ信号振幅** Focus error signal amplitude V_2 : **ｼﾞｯﾀｰ最良点のﾌｫｰｶｽﾊﾞｲｱｽ** Focus bias at minimum jitter F.E.**ｵﾌｾｯﾄ** off set : **ﾚｰｻﾞｰ**ON**,ﾃﾞｨｽｸからの戻り光が無い状態でのﾌｫｰｶｽｴﾗｰのDCｵﾌｾｯﾄ** Focus error DC off set at laser on and no reflection from the disc.  ★ **ﾌｫｰｶｽｴﾗｰ信号振幅の中心** Center of Focus error signal amplitude **ﾃﾞﾌｫｰｶｽの極性** Defocus polarity **対物ﾚﾝｽﾞをﾃﾞｨｽｸに近づける方向にﾌｫｰｶｽﾊﾞｲｱｽをかけた場合にｼﾞｯﾀｰ最良点がある時、ﾃﾞﾌｫｰｶｽの極性はﾌﾟﾗｽといい、逆の場合をﾏｲﾅｽと規定する。** When objective lens moves toward the disc and able to get minimum jitter,it is defined as plus, otherwise, it is defined as minus.
ﾌｫｰｶｽｴﾗｰ信号ｵﾌｾｯﾄ電圧 Focus error signal offset voltage	within 0± 2.3V **以内**	———	———	**ＬＤ ＯＮ時** At LD on.
極　性 Polarity	**対物レンズがディスク側に近づいた時のF.E.信号がマイナスからプラスに変化する。** The focus error signal changes from minus to plus the objective lens approaches the disc.			

◆ トラッキングエラー信号 Tracking error signal

項　　目 Item	規　　格 Standard value 常 温 常 湿 Room temperature and humidity	温 度 変 化 Temperature Deviation - 5℃	 + 55℃	備　　考 Remarks
トラッキング エラー信号振幅 Tracking error signal amplitude	14.5±7.5Vp-p	*within ± 30% 以内	*within ± 30% 以内	
EFバランス EF balance	within 0±30% 以内	** within 0±35% 以内	** within 0±35% 以内	TPPバランス＝$\frac{V_2}{V_1}\times 100\%$ TPP balance  ★トラッキングエラー信号の中心 The center of tracking error signal
E-F位相差 E-F phase difference	within ± 60 ° 以内	** within ± 90 ° 以内	** within ± 90 ° 以内	
極　性 Polarity	読み取りスポットがデトラックした時、 内周側にずれるとプラス、外周側にずれると マイナスと規定する。 When the spot is off track, the direction toward the center of the disc is defined as plus and the periphery of the disc is defined as minus.			 トラッキングエラー信号 Tracking error signal

4-3-2. **ターンテーブル部** Turntable unit

項　　目 Item	**規　　格** Standard value	**備　　考** Remarks
ターンテーブル高さ Height of turntable	6.1±0.2 mm	**インシュレーター取り付け面より** From insulator fixing surface
ターンテーブル面振れ Surface vibrations of turntable	0.07 mm 以下 or less	
ターンテーブル最大耐圧荷重 Maximum load of turntable	98 N 以上 or more	

4-3-3. **送り機構部** Sled mechanism

項　　目 Item	**規　　格** Standard value	**温 度 変 化** Temperature Deviation		**備　　考** Remarks
	常 温 常 湿 Room temperature and humidity	- 5°C	+ 55°C	
最低起動電圧 Minimum starting voltage	1.0 V 以下 or less	1.2 V 以下 or less	1.2 V 以下 or less	
フルストローク移動時間 Full stroke time	2.3 s 以下 or less	3.0 s 以下 or less	3.0 s 以下 or less	**印加電圧** 1.5V**(片道)** Applied voltage 1.5V (one way)
消費電流 Current consumption	160mA 以下 or less	210mA 以下 or less	210mA 以下 or less	**印加電圧** 1.5V Applied voltage 1.5V
リミットスイッチメイク位置 Make position of limit switch	**ピックアップが機械的最内周位置に達する前にメイクしていること。** Make should be completed before pick-up operation reaches mechanically innermost position.			

５）信頼性保証基準
Reliability Standard

5-1. 信頼性保証基準 Reliability Standard

◆ **動作温度** Operating Temperature

温　度　Temperature　：　-5 ～ 55 ℃

高温又は低温時に於ける動作特性は、性能規格に示す。
非動作にて４ｈ放置後、測定する。　但し、結露させないこと。
The operating characteristics at -5℃ and 55℃ are expressed as deviations from standard values as shown in the performance specifications.
Leave the pick-up in the idle state within the above temperature range for four hours. Do not let condensation to form on the mechanism.

◆ **保存温度** Storage Temperature

温　度　Temperature　：　-30 ～ 60 ℃

上記環境に２４ｈ放置し、常温に戻して１６ｈ以上放置後の初期値に対する特性変化は、信頼性保証規格の範囲内とする。　但し、結露させないこと。
Leave the pick-up at temperatures in the above range for 24 hours and then at room temperature for over 16 hours. After the test, the deviation of characteristics from the standard values must be within the tolerance specified in the reliability specifications. Do not let condensation to form on the mechanism.

◆ **高温高湿保存** Storage in hot and humid conditions

温　度　Temperature　：　60 ℃
湿　度　Humidity　：　90%

上記環境に４８ｈ放置し、常温に戻して１６ｈ以上放置後の初期値に対する特性変化は、信頼性保証規格の範囲内とする。　但し、結露させないこと。
Leave the pick-up at temperatures in the above range for 48 hours and then at room temperature for over 16 hours. After the test, the deviation of characteristics from the standard values must be within the tolerance specified in the reliability specifications. Do not let condensation to form on the mechanism.

◆ **単体振動** Vibration

振　動　：　23.6m/s² {2.4G}, 7～30Hz **直線スイープ，３方向**
Conditions　linear sweep, three directions

上記振動を各方向１５分（スイープ時間は往復で５分）印加後の初期値に対する特性変化は、信頼性保証規格の範囲内とする。
Subject the drive unit to above vibrations under the above conditions for 15 minutes in each direction(time for return sweep:5 minutes). After the test, the deviation of characteristics from the standard values must be within the tolerance specified in the reliability specifications.

◆ **単体衝撃**　Impact

衝　撃　：　2,940m/s² {300G} 1.6mSec, ±X, ±Y, ±Z**方向**
Conditions　directions

上記振動を各方向１回印加後の初期値に対する特性変化は、信頼性保証規格の範囲内とする。
Subject the drive unit to above impact in each direction.　After the test, the deviation of characteristics from the standard values must be within the tolerance specified in the reliability specifications.

◆ **レーザーダイオードの寿命**　Service life of laser diode

２５℃，３,０００ｈ動作にて、不良率０.１%以下。
（但し、静電破壊等による事故を除く）
Percent defective : 0.1% max after 3,000 hours operation at 25°C
(excluding damage due to electrostatic discharge)

◆ **スピンドルモータ寿命**　Service life of spindle motor

再生時間１,０００ｈ経過後、スピンドルモータの消費電流は、
初期値＋３０%以下。
The current consumption of spindle motor must be less than initial value plus 30% after 1,000 hours of playback.

◆ **送りモータ寿命**　Service life of Sled motor

１０,０００サイクル動作後、送りモータの消費電流は、
初期値＋３０%以下。（１サイクル：最内周→最外周→最内周）
The current consumption of sled motor must be less than initial value plus 30% after 10,000 cycles.
(1cycle : innermost track → outermost track → innermost track)

◆ **リミットスイッチ寿命**　Service life of limit switch

１０,０００サイクル動作後、接触抵抗は５００mΩ以下。
The contact resistance must be less than 500mΩ after 10,000 cycles.
(1cycle : innermost track → outermost track → innermost track)

◆ **ピックアップスライド動作**　Pick-up slide operation

１０,０００サイクル動作後、実用上支障無きこと。
（１サイクル：最内周→最外周→最内周）
The pick-up should operate perfectly after 10,000 cycles.
(1cycle : innermost track → outermost track → innermost track)

5-2. **信頼性保証規格** Reliability Specifications

信頼性保証条件で評価後の変化量；動作試験は除く。
但し、＊印は実測値を表わす。
Deviations after evaluation tests under the conditions specified on reliability test except operating temperature test.(＊: Actually measured value)

２軸可動部 Actuator

項　　目 Item		**規　　格** Standard value
フォーカス Focus	**低域感度** Sensitivity	± 25 % **以内** within ± 25 %
	共振周波数 (fo) Resonant frequency	± 6 Hz **以内** within ± 6 Hz
	Q　　値 Q-value	± 6 dB **以内** within ± 6 dB
トラッキング Tracking	**低域感度** Sensitivity	± 25 % **以内** within ± 25 %
	共振周波数 (fo) Resonant frequency	± 7 Hz **以内** within ± 7 Hz
	Q　　値 Q-value	± 6 dB **以内** within ± 6 dB

光学部 Optics

項　　目 Item		**規　　格** Standard value
ＲＦ信号 RF signal	**ＲＦ信号振幅** RF signal Amplitude	± 20 % **以内** within ± 20 %
	ジッター Jitter ＊	34 ns RMS **以下** 34 ns RMS or less
ﾌｫｰｶｽ信号 Focus signal	**ﾌｫｰｶｽｴﾗｰ信号振幅** Focus error signal amplitude	± 20 % **以内** within ± 20 %
	デフォーカス Defocus	± 1 μm **以内** within ± 1 μm
ﾄﾗﾊﾞｰｽ信号 Traverse signal	**ﾄﾗｯｷﾝｸﾞｴﾗｰ信号振幅** Tracing error signal amplitude	±30 % **以内** within ± 30 %
	EFバランス EF balance ＊	0±35 % **以内** within 0±35 %
	EF位相差 EF phase difference ＊	0±90° **以内** within 0±90°

送り機構部 Sled mechanism

項　　目 Item	規　　格 Standard value	備　　考 Remarks
最低起動電圧 Minimum starting voltage	＊　1.2 V **以下** or less	
送り時間 Sled time	＊　3 sec **以下** or less	**印加電圧** 1.5 V Applied voltage 1.5V
消費電流 Current consumption	＊　210 mA **以下** or less	

6）表　示
Markings

TENTATIVE
2002 August 23

6-1. 捺　印　Stamp

	日	月	西暦年号の末尾	品質管理No.	英字又は数字
BBC ○○○○○○○○	Day	Month	Last digit of year	Quality control No.	Alphabet or Number
Lot No.	○○	○	○	○	○○○

但し、月表示の10, 11, 12**は**X, Y, Z**で表わす。**
X,Y and Z signify October, November and December respectively.

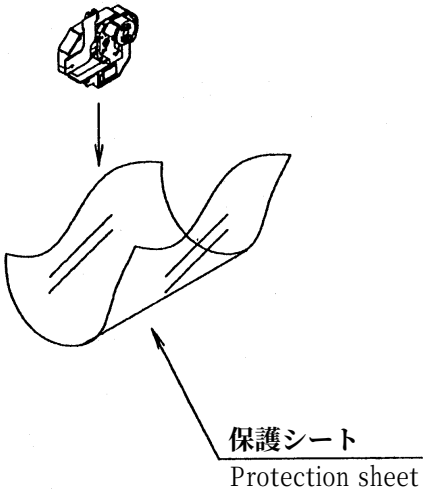
末尾の英字は、製造所の管理に用いる場合がある。
但し、桁数は０～３桁迄とする。
The last alphabet is for management purposes in the factory. Use up to three characters.

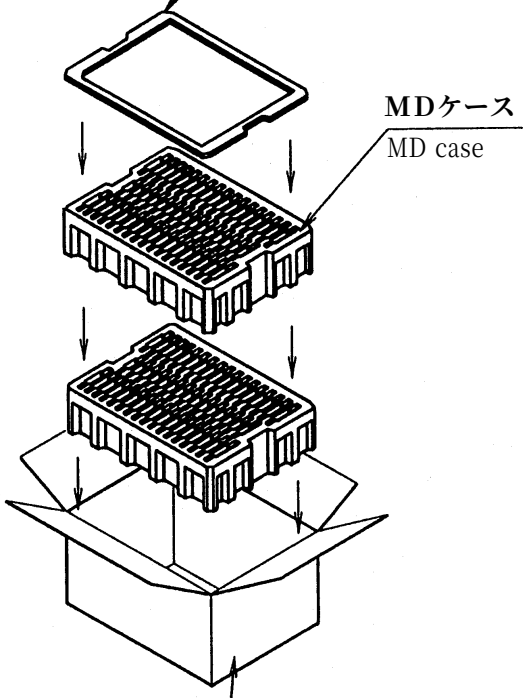
6-2. 表示場所　Position of label

Fig.1**の各部名称参照。**
Refer to Fig 1. Description of components.

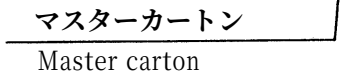
7）梱包仕様
Package Specifications

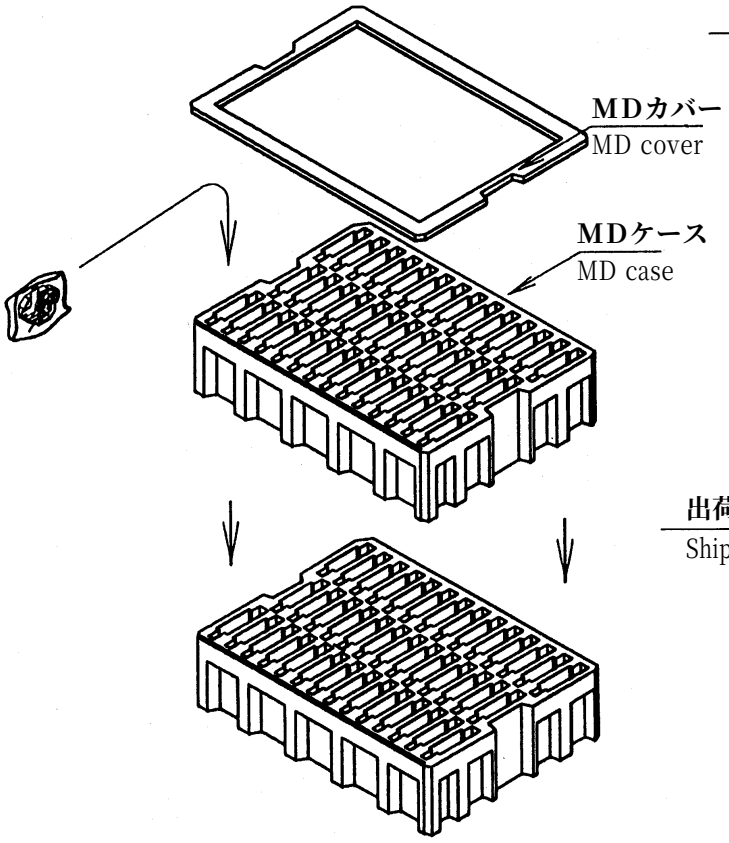
① **本機種を保護シートに入れる。**
Set into protection sheet.

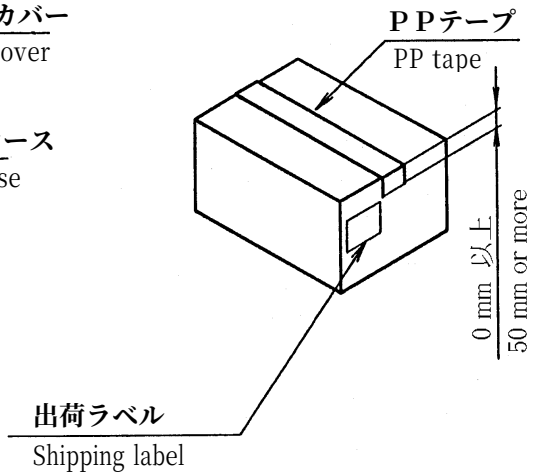




② **MDケースに１００個(50×2列)収納する。**
Set into MD case. 50 pcs×2 lines (Total 100 pcs)

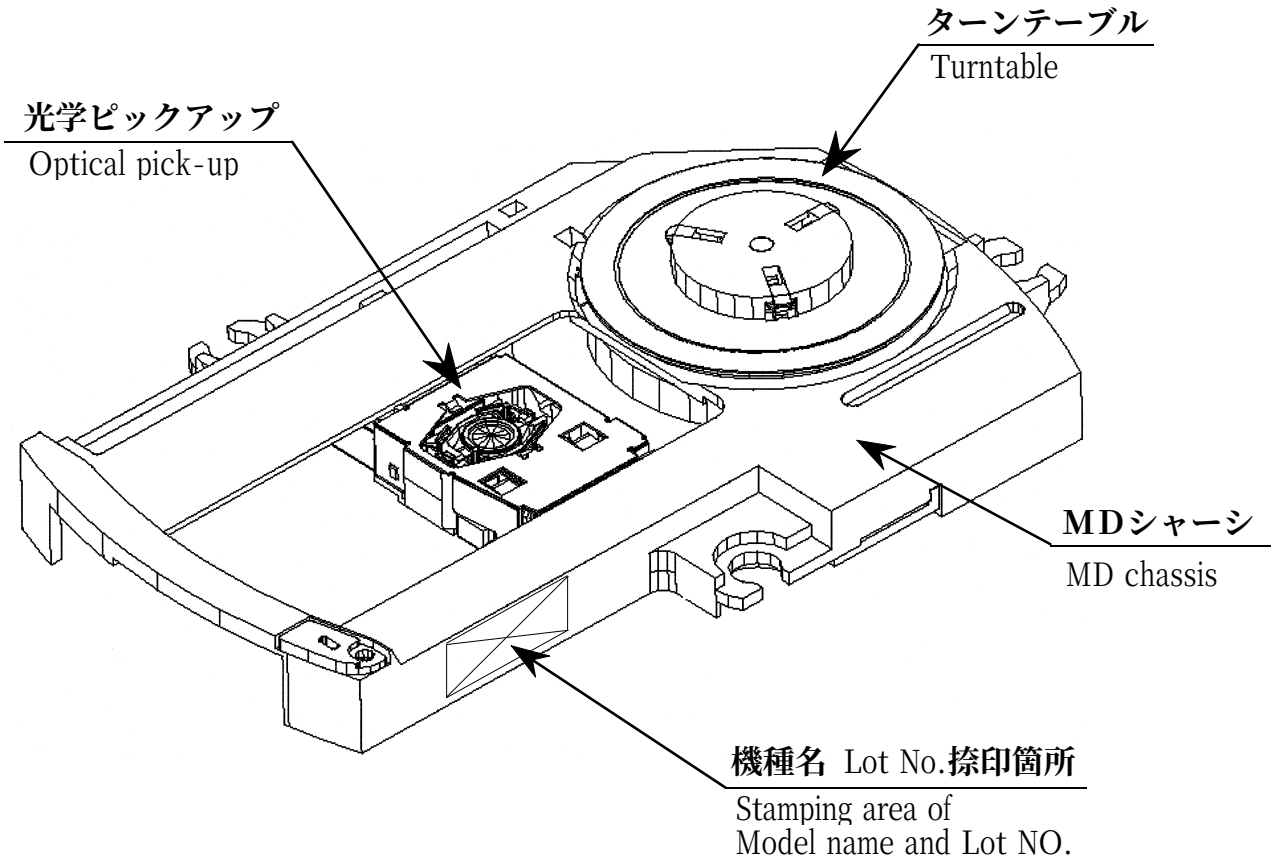






8）付　図
Attachment

Figure 1. **各部の名称** Description of components



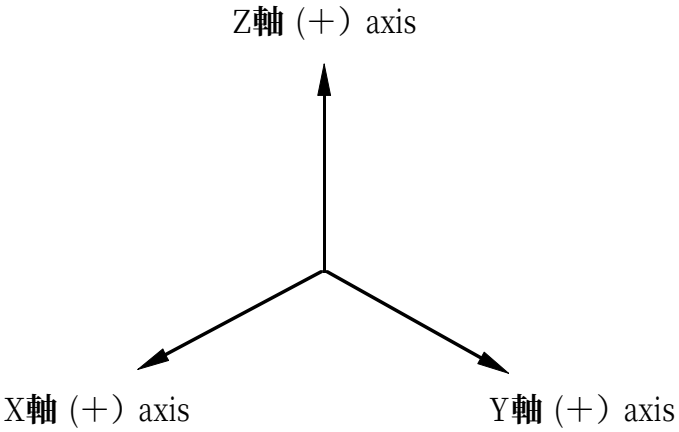


Figure 2. **外形図** Appearance Drawing

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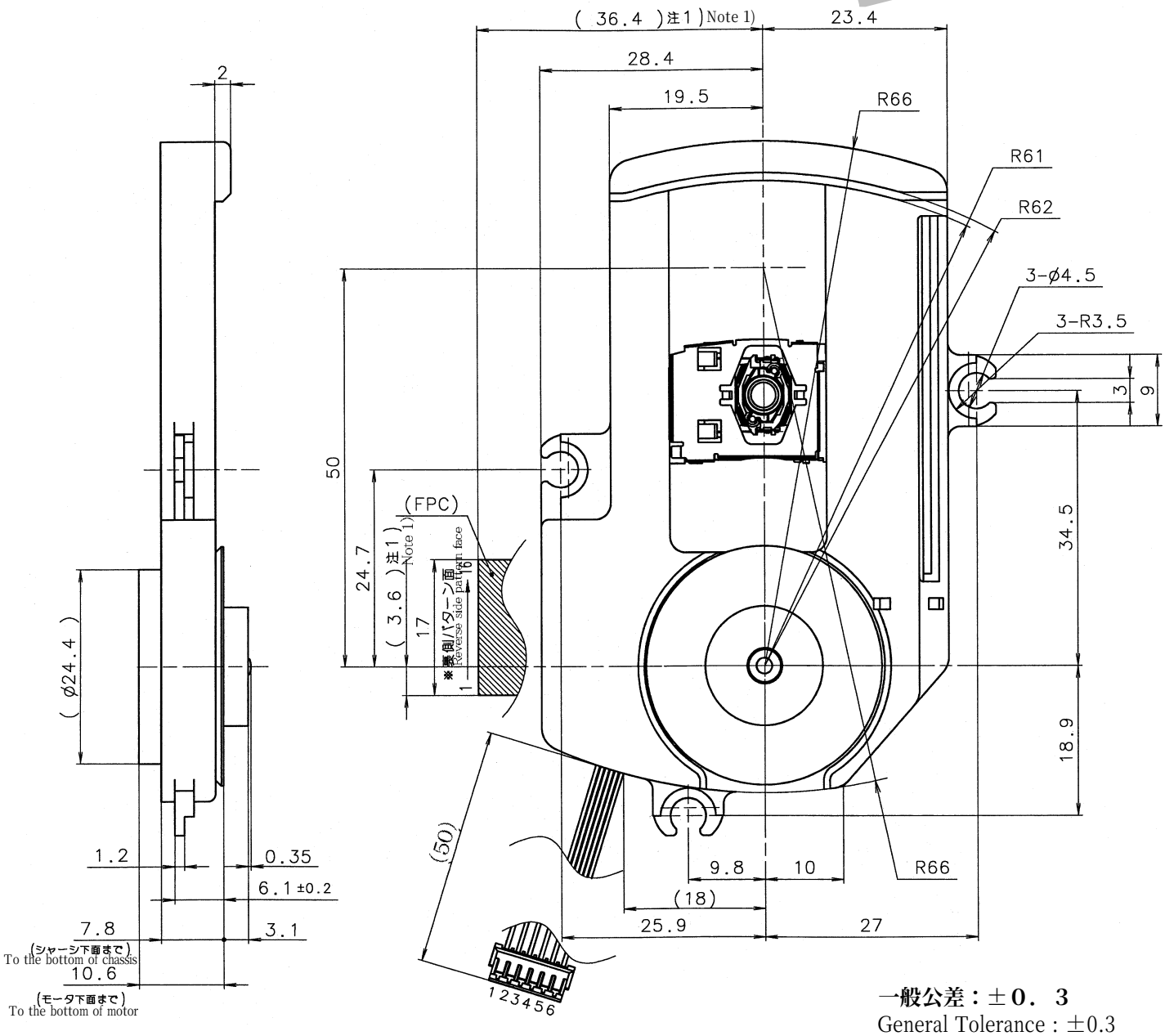
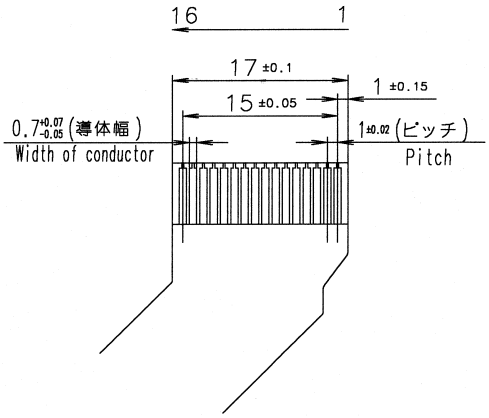


一般公差：±0．3
General Tolerance : ±0.3

注1)推奨フレキ位置
Note 1) Recommended FPC position

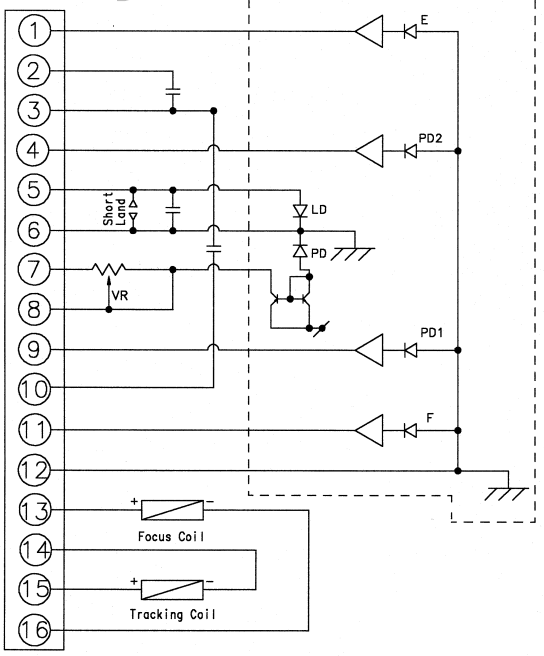
Figure 3. **コネクター結線図** Pin connection diagram

1.**フレキ端子** FPC Terminal



ピンNo. Pin No.	端子名称 Terminal
1	E
2	Vcc
3	GND (Vcc)
4	PD2
5	LD+
6	GND (LD)
7	VR
8	Mon out
9	PD1
10	VC
11	F
12	GND (PDIC)
13	FCS+
14	TRK-
15	TRK+
16	FCS-

ホログラムユニット
Hologram Unit

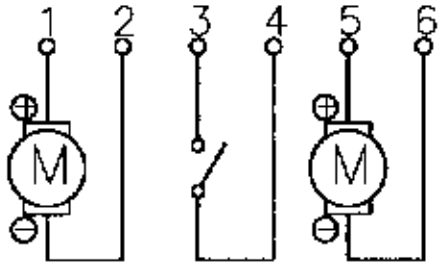


推奨コネクター：エルコインターナショナル 6224**シリーズ**
Recommended connector : Product of ELCO INTERNATIONAL CO., LTD.
Series 6224

フォーカスエラー 信号：PD1 - PD2
トラッキングエラー信号：E - F
RF **信号：**PD1 + PD2

2.**ハウジング端子** Housing Terminal

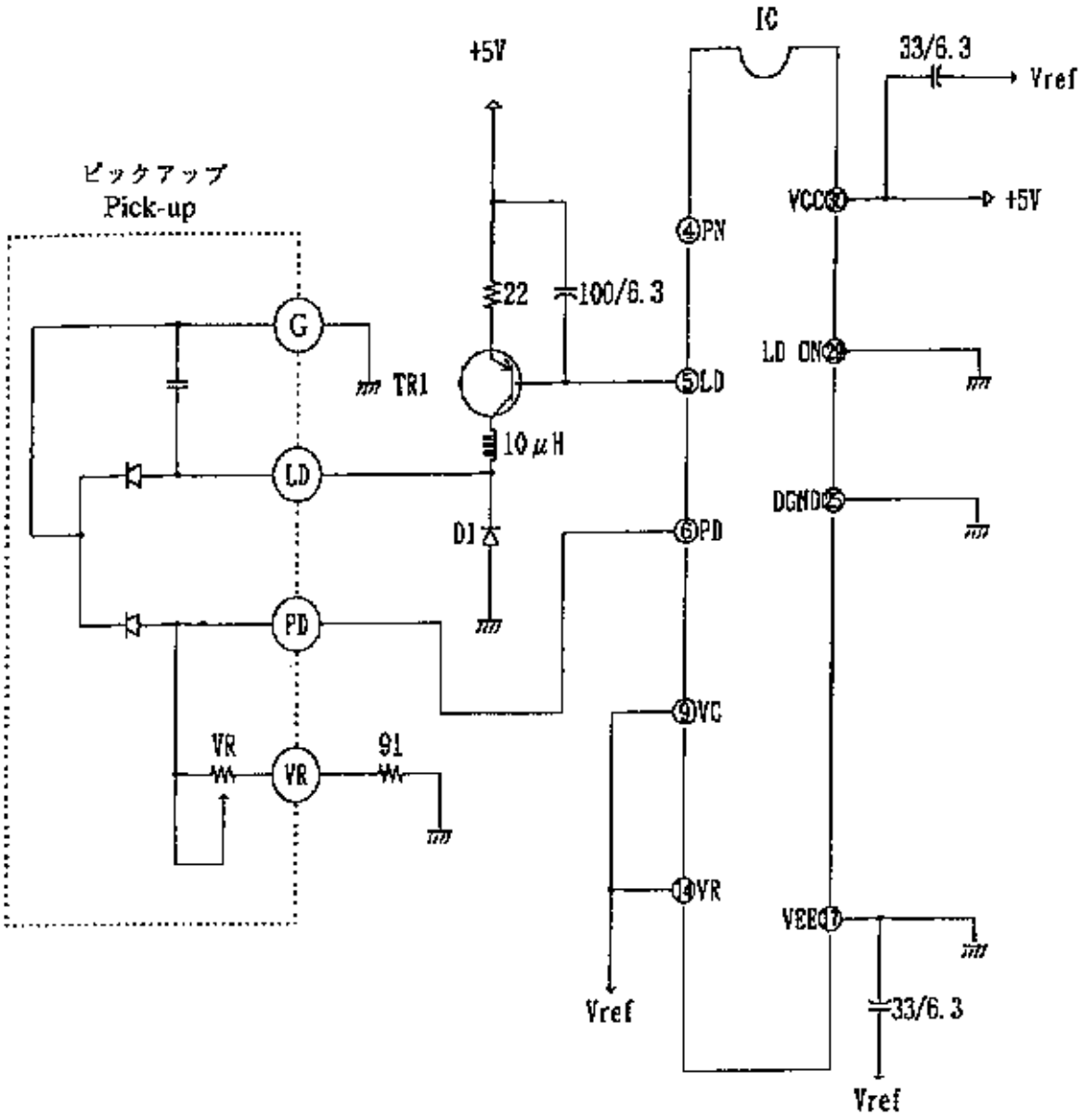
ピンNo. Pin No.	**端子名称** Terminal
1	SLED +
2	SLED -
3	LIMIT SW
4	LIMIT SW
5	SPINDLE (+)
6	SPINDLE (-)



SLD Mo. LIMIT SW SP Mo.

推奨コネクター：日本圧着端子 ZR**シリーズ**
Recommended connector : Product of JAPAN SOLDERLESS TERMINAL CO., LTD.
Series ZR.

Figure 4. **ＡＰＣ回路参考図** APC Circuit diagram (Reference)



ＩＣ　：ＣＸＡ－１０８１Ｍ

ＴＲ１：２ＳＢ７３１

Ｄ１　：１Ｓ１５５５

Figure 5. **標準評価回路図** Standard test circuit diagram

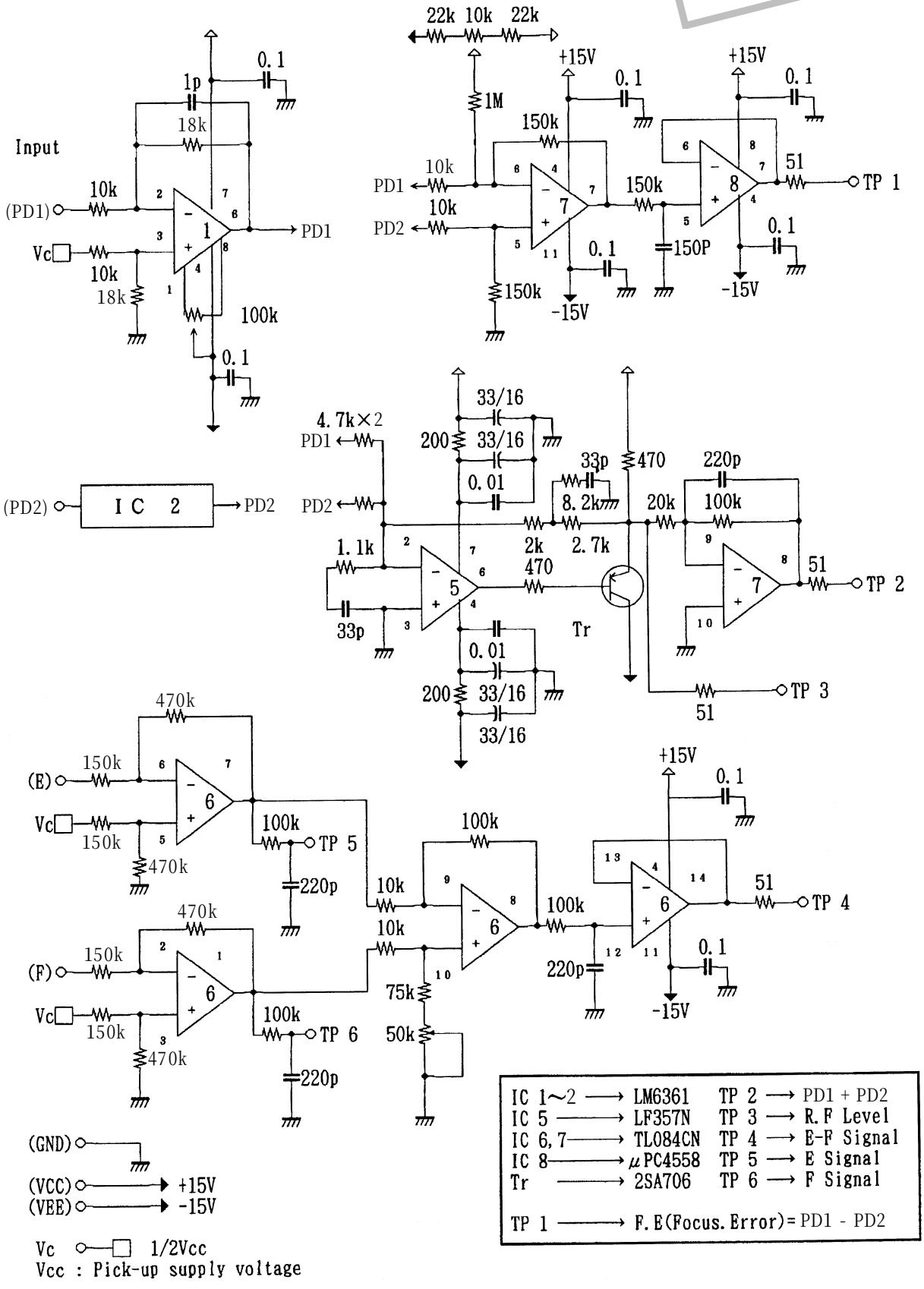


Figure 6. スピンドルモータ代表特性（三洋精密製モータ）
Major characteristics of Spindle motor (Made by SANYO SEIMITSU)

◆ **標準使用状態及び電気的特性（参考値）**
Standard operating conditions and electrical characteristics (for reference)

標準使用状態 Standard operating conditions	**定格電圧（ＤＣ）** Rated voltage (DC)		2.0 V
	使用電圧範囲（モータ端子間：ＤＣ） Used voltage range (between motor terminals : DC)		1.0 ～ 3.0 V
	定格負荷 Rated load		0.49 mN・m
電気的特性 Electrical characteristics	**定格負荷回転数** Speed	**定格電圧，定格負荷にて** At rated voltage and load	2300 ± 345 r/min
	定格負荷電流 Current	**定格電圧，定格負荷にて** At rated voltage and load	145 mA **以下** or less
	始動トルク Initial torque	**定格電圧，巻き上げ法にて** At rated voltage and by winding-up method	1.37 mN・m **以上** or more
	始動電流 Initial current	**定格電圧にて** At rated voltage	400 mA **以下** or less

◆ **モータ特性図** Motor characteristics diagram

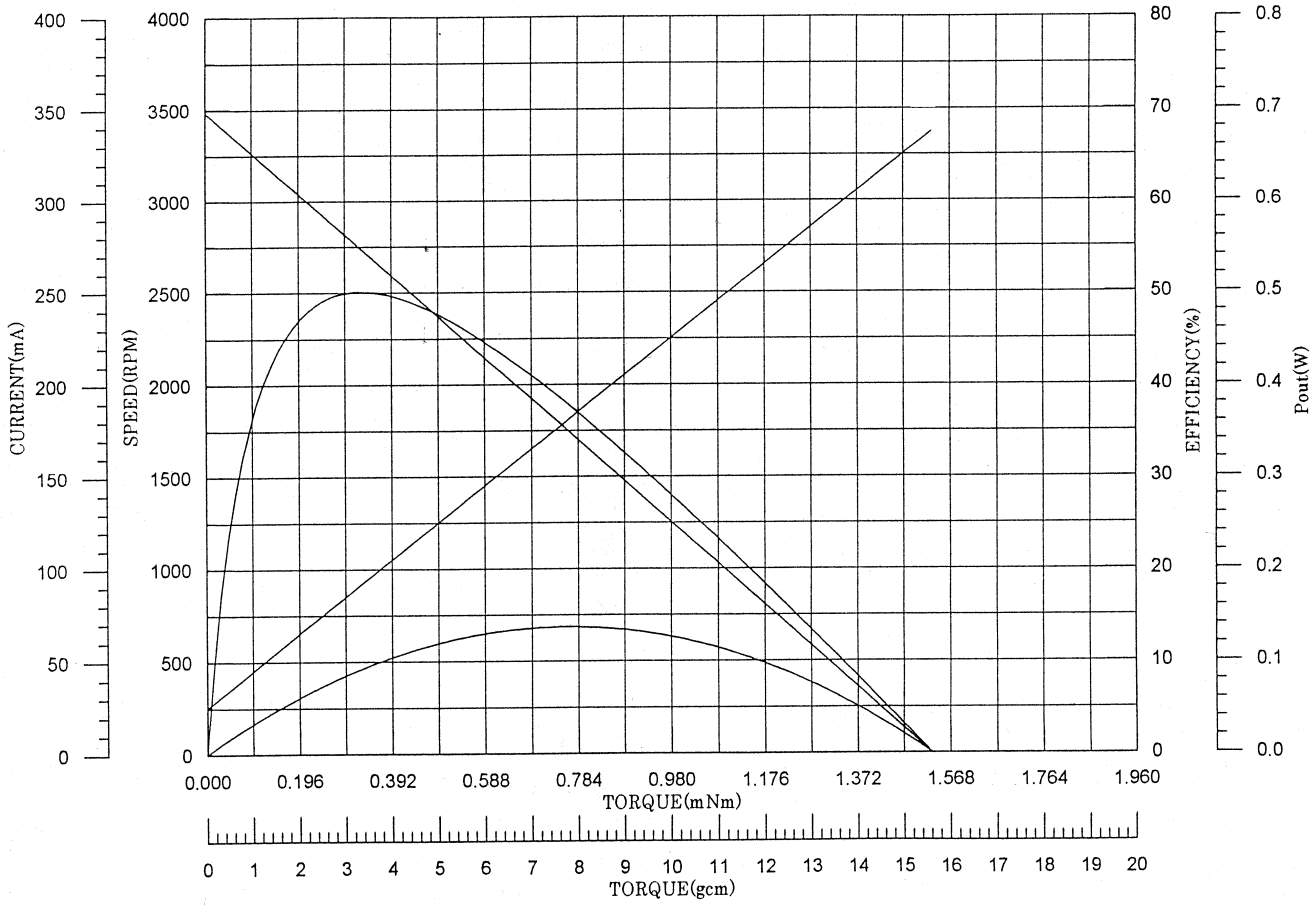
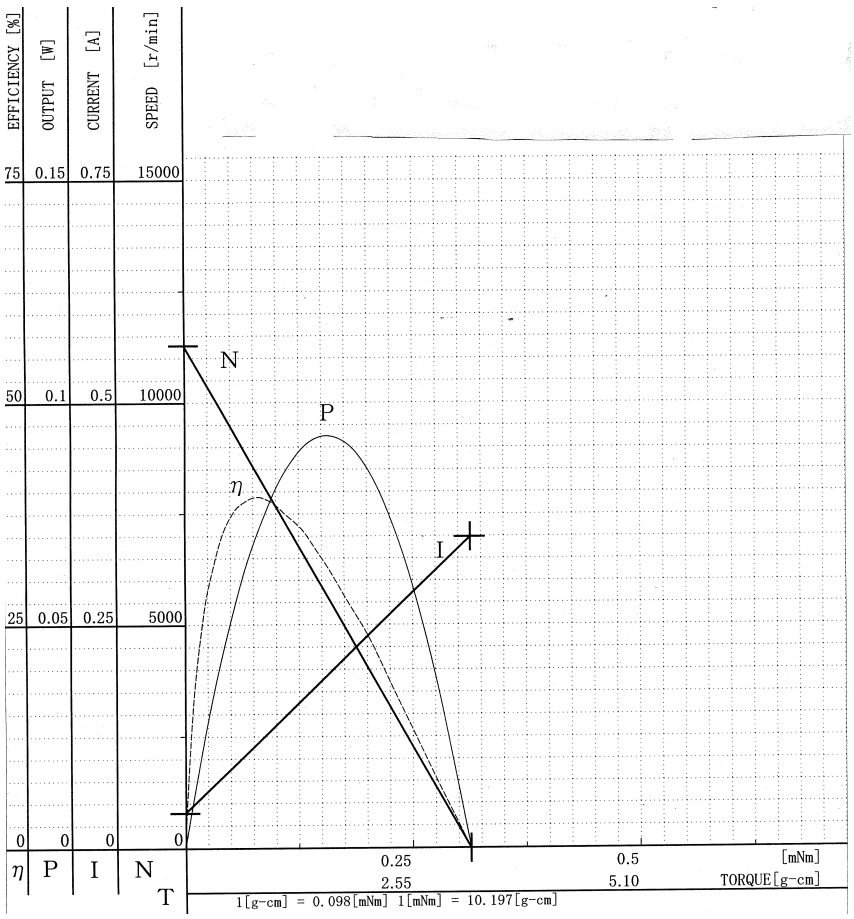


Figure 7. 送りモータ代表特性（マブチ製モータ）
Major characteristics of Sled motor (Made by MABUCHI)

◆ **標準使用状態及び電気的特性（参考値）**
Standard operating conditions and electrical characteristics (for reference)

標準使用状態 Standard operating conditions	**定格電圧（ＤＣ）** Rated voltage (DC)		1.5 VDC
	使用電圧範囲（モータ端子間：ＤＣ） Used voltage range (between motor terminals :DC)		1.5 ～ 3.0 V
	定格負荷 Rated load		0.0981 mN・m
電気的特性 Electrical characteristics	**定格負荷回転数** Speed	**定格電圧，定格負荷にて** At rated voltage and load	7550 ± 2300 min^{-1}
	定格負荷電流 Current	**定格電圧，定格負荷にて** At rated voltage and load	180 mA **以下** or less
	始動トルク Initial torque	**定格電圧，２点法** At rated voltage and by 2points	0.196 mN・m **以上** or more
	始動電流 Initial current	**定格電圧にて** At rated voltage	390 mA **以下** or less

◆ **モータ特性図** Motor characteristics diagram



9）その他
Others

9-1. 使用上の注意 Precautions in use

◆ ＡＰＣ回路 APC Circuit

**レーザーダイオード（ＬＤ）は、温度により光出力が大きく変化しますので、
ＬＤに内蔵のモニターフォトダイオードを使用し、光出力の補正を行って下さい。
モニターフォトダイオードのバラツキを無くすため、ピックアップに付属する
ＶＲは、光出力とモニターフォトダイオードの関係をＲＦ出力一定になるように
調節して有ります。
付属の標準評価回路を用いた時、ＲＦレベルは** 1Vp-p**になります。**
The output laser power must be controlled with the built-in monitor photodiode, since laser power changes with temperature. To prevent the characteristics dispersion of the monitor photodiode, the relation between the potentiometer (VR) attached to the pick-up and the monitor photodiode is factory adjusted so that the RFoutput will be constant.
RF level will be 1 Vp-p when the attached standard test circuit is used.

◆ 結　線 Connections

**結線は、必らず指定形状のフレキシブル基板を使用してください。
フォトダイオードからのハーネス近くにマイコン等のデジタルノイズ源が
有りますと、アイパターンが劣化することが有りますので注意して下さい。
２軸，レーザーダイオードコネクターに関する結線に接触不良が有りますと、
レーザー劣化の原因となりますので、コネクター等のゆるみがないように
して下さい。**
Use the specified connectors for electrical connections.
The eye pattern may deteriorate if a digital noise source such as a microcomputer is positioned near the harness from the photodiode. The laser may deteriorate if the actuator or laser diode connection is poor; securely connect these connecters.

◆ ＧＮＤ の短絡 Short - circuit of GND

ピンNo.3 **(**GND(Vcc))**、ピン**No.6 **(**GND(LD))**、ピン**No.12 **(**GND(PDIC))**は
ピックアップ内でオープン（開放）となっているため、必ずセット回路内で
共通接続して下さい。**
Pin No.3, 6 and 12 are not common nodes in the circuit of optical pick-up circuit itself. These lines shall be connected on customer's PWB.

9-2. 取り扱い注意事項 Handling instructions

本機種は、当社の専門工場にて組立調整されております。
安易に分解、調整等を行わないで下さい。
取り扱いに関して次の点に注意して下さい。　又、サービス，ユーザー等にも注意する措置をお願い致します。
This model is assembled and precisely adjusted in our special plant.
Never attempt to disassemble or readjust it.
Pay attention to the following instructions when handling this model.
Please inform service personnel and users about it.

◆ 一　般 General

保　管 Storage

高温高湿下，ホコリの多い所での保存は避けて下さい。
Avoid storing this model in hot, humid or dusty conditions.

取り扱い Handling

精密に調整されていますので、落下や不用意な取り扱いによる衝撃が加わらないようにして下さい。
This model is a precise unit. Be careful not to subject it to shocks by dropping or rough handling.

◆ レーザーダイオード Laser diode

レーザー光に対する目の保護 Shield your eyes from the laser beam

ＬＤの出力は、対物レンズ出射出力でMAX 1mW**ですが、集光された所では約**0.7×10^4 W/cm^2 **に達します。　動作中のＬＤを直視したり、あるいは他のレンズやミラーを介して光束を観察すると危険ですから、絶対に行わないで下さい。**
もし観察するときは、赤外線ビューアーかＩＴＶカメラを使用して下さい。
The output from the LD is only 1mW maximum after going through the objective lens . However, the intensity of the focused beam reaches about 0.7×10^4 W/cm^2 . Never look directly into the LD or observe the laser beam through another lens or mirror. If you need to view the beam, use an infrared viewer or an ITV camera.

ヒ素の毒性 Toxicity of As

ＬＤのチップは、GaAs+GaAlAs**で毒物として良く知られているヒ素を含んでいます。　毒性は、他の化合物、例えば**As_2O_3 , $AsCl_3$ **等に比較し、はるかに弱い毒性で素子１ケ当たりは少量ですが、チップを取り出し酸やアルカリへ入れたり、200℃以上に加熱したり、口に入れたりすることは絶対に行わないで下さい。　ライン不良，サービスパーツの不良品は、廃棄物入れにまとめて入れ、御社指定の方法で廃棄処理をして下さい。**
The LD chip is manufactured from GaAs and GaAlAs, which contains toxic As (Arsenic). The toxicity of As in this form is far lower than other As compounds such as As_2O_3 and $AsCl_3$, and the As content of one chip is very small. However, avoid putting the chip in an acid or alkali solution, heating it over 200°C, or putting it your mouth. Defective LDs from the production line and parts removed in servicing should be disposed of with due care.

サージ電流，静電気による破壊 Avoid current surges and electrostatic discharges

ＬＤに大電流を流すと、きわめて短時間であっても自身が発する強い光によって劣化が促進され、或いは破壊します。　ＬＤ駆動回路には、スイッチ，その他によるサージ電流が流れないようにして下さい。　又、不注意に扱うと人体からの静電気が加わって瞬時に破壊されてしまいます。　ＬＤの端子は、出荷時に輸送による静電気破壊防止のため、ショートされています。　更に安全を期するため取り付け時、人体アース，計測器及び治工具のアースを必ず行って下さい。
又、作業台や床等にアースマットを用いて接地することが望ましい。
ショート部の解放は、コネクター差し込み後、半田ゴテで行って下さい。
使用する半田ゴテは、金属部分が接地されたもの、或いは通電５分後の絶縁抵抗が10MΩ**以上**(DC 500V)**のもので、半田ゴテ先温度が320℃以下**(30W)**のものを使用し、すみやかに行って下さい。**
The LD may deteriorated if its output is too high and damage may occur if it is exposed to large currents for even a short time. Protect the LD drive circuit from current surges caused by switches or other sources. An electrostatic discharge from the human body may destroy the LD instantaneously if it is handled carelessly. LD terminals are factory -strapped before shipment to protect LD from electrostatic discharges during transportation. For safe handling of the LD, ground your body, measuring equipment, jigs, and tools during installation. Use of a grounding mat on the workbench and floor is recommended. After connector insertion, unstrap the LD terminal with a soldering iron with its metallic tip grounded or worse insulation resistance is 10 megohms or more (at 500V DC) five minutes after it is tuned on. The temperature of the soldering iron tip must be 320℃ or below (30W) and the unstrapping should be performed quickly.

Vcc無通電状態でのLD通電による破損
Avoid the application of current to LD in the case when voltage is not applied to Vcc

Vccに規定の電圧が通電されていない状態でLD**に通電しますと、素子の回路が動作せず、**LD**に過電流が流れてLD劣化を引き起こします。**
Vccに無通電の状態でLD**に通電することが無きよう、ご注意願います。**
LD may deteriorate if the current is applied to LD in the case when the regulated voltage is not applied to Vcc, because the circuit of element does not operate and LD is applied over current. Do not apply the current to LD with voltage is not applied to Vcc.

◆ **２軸部** Actuator

アクチュエータ Actuator

アクチュエータ部は強力な磁気回路を有していますので、磁性体が近づきすぎますと特性が変化します。　又、すきまから異物が入ることの無いようにして下さい。
The performance of the actuator may be affected if a magnetic material is located nearby, since the actuator has a strong magnetic field.
Do not allow foreign materials to enter through gap.

◆ **取り扱い** Handling

光学ドライブユニットの取り扱いは、シャーシを持って行って下さい。
プリント基板の回路部に人体或いは他の物体が直接触れますと、劣化の原因になることが有りますので、充分注意下さい。
Hold the chassis when handling the drive unit. Note that the LD and PD may be damaged if you come in contact with any of the circuit boards.

9-3. **安全規格対象部品** Conformity of main parts to safety standards(UL standard)

本機種は、各国安全規格に準じて設計されておりますが、使われ方により承認が決まるめ、単体での承認はされておりません。 安全規格については、セットでの承認申請及び確認をお願い致します。

This model is designed to conform with the safety standards of various countries. Since approval depends on the mode of use, however, it is not approved as a unit. Therefore, apply for approval after mounting the optical drive unit in a player and check it for safety after mounting, too.

◆ **光学ピックアップ部** Optical Pick-up

Parts Name	Material Manufacturer	Grade	Generic Name	Type No.	ID Mark
HOEﾌﾚｷｼﾌﾞﾙ基板 HOE FPC	SI FLEX CO LTD	94V-0	——	——	ᖇ Si F5a▲
スライドベース Slide base	DAINIPPON INK & CHEMICALS INC	94V-0	PPS	FZ-3000-X0	——
	SUMITOMO BAKELITE CO LTD	94V-0	PPS	FM-MK113	——

◆ **ドライブユニット部** Drive unit

Parts Name	Material Manufacturer	Grade	Generic Name	Type No.	ID Mark
MDシャーシ MD Chassis	ASAHI KASEI CORP	94V-1	PPE	L543V	——

4-ch Motor Driver for Portable CD Players
Monolithic IC MM1538

Outline

This driver IC contains a 4ch H bridge driver and DC-DC converter control circuit on one chip, and was developed for use in portable CD players. QFP-44 is used for the package, making it ideal for smaller sets.

Features

(1) Built-in 4ch H bridge driver, and PWM control of load drive voltage is made possible by external components.
(2) DC-DC converter control circuit on chip.
(3) With reset output inversion output pin.
(4) Empty detection level can be switched between rechargeable battery and dry battery.
(5) Constant current charging; current value can be varied using external resistor.
(6) Built-in power transistor for charging.
(7) Built-in independent thermal shutdown circuit.

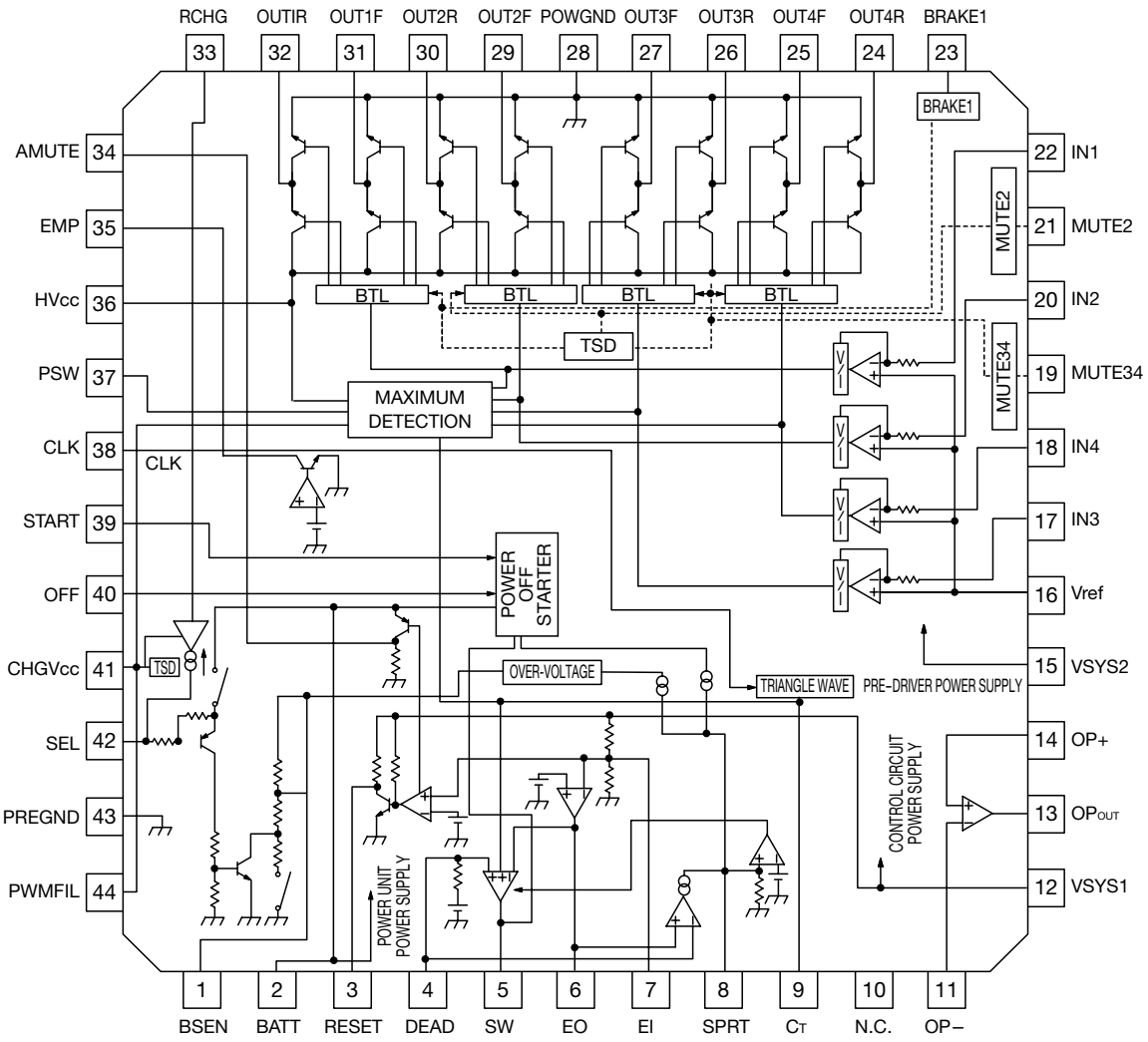
Package

QFP-44

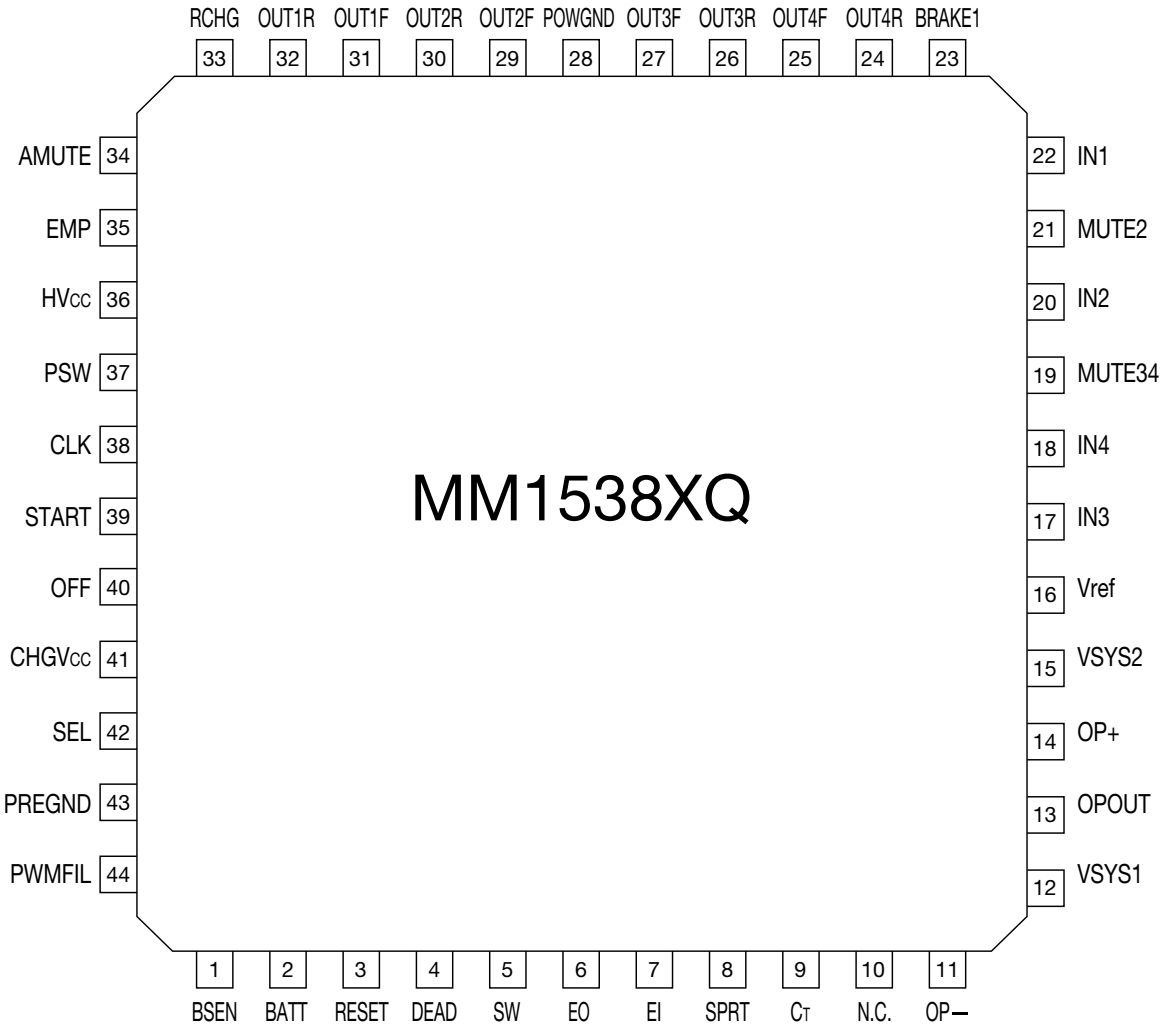
Applications

Portable CD radio cassette recorders

Block Diagram

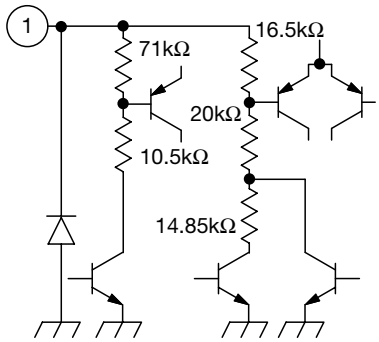
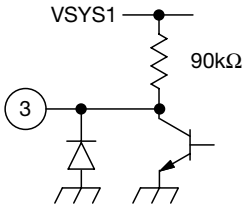
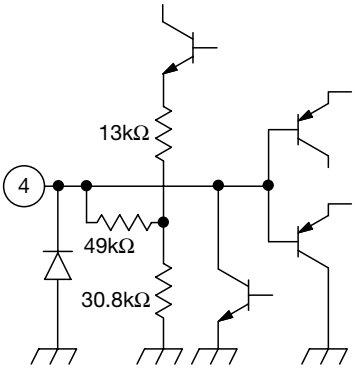
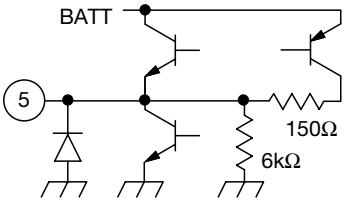
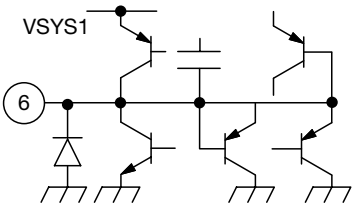


Pin Assignment

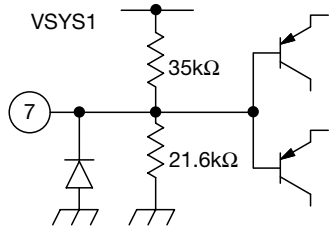
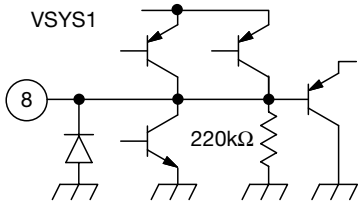
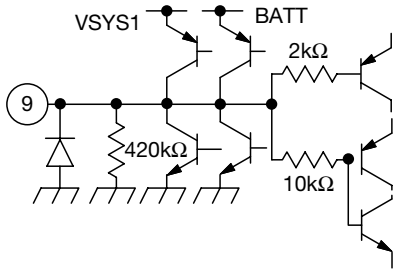
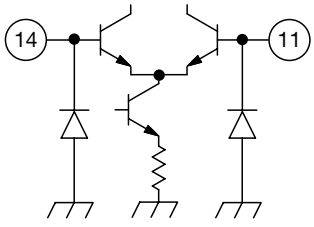
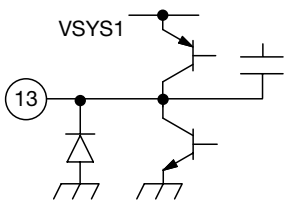


1	BSEN	23	BRAKE1
2	BATT	24	OUT4R
3	RESET	25	OUT4F
4	DEAD	26	OUT3R
5	SW	27	OUT3F
6	EO	28	POWGND
7	EI	29	OUT2F
8	SPRT	30	OUT2R
9	C_T	31	OUT1F
10	N.C.	32	OUT4R
11	OP–	33	RCHG
12	VSYS1	34	AMUTE
13	OPOUT	35	EMP
14	OP+	36	HV_{CC}
15	VSYS2	37	PSW
16	Vref	38	CLK
17	IN3	39	START
18	IN4	40	OFF
19	MUTE34	41	$CHGV_{CC}$
20	IN2	42	SEL
21	MUTE2	43	PREGND
22	IN1	44	PWMFIL

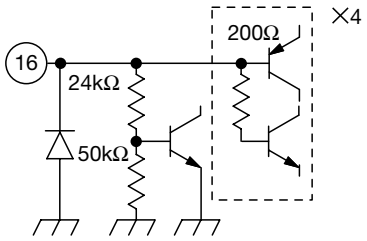
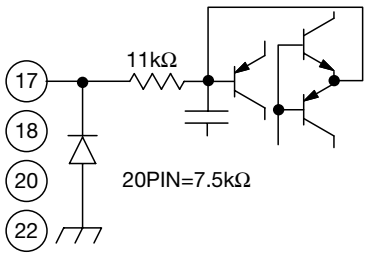
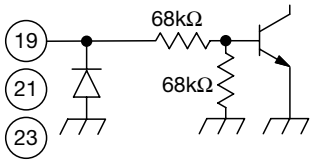
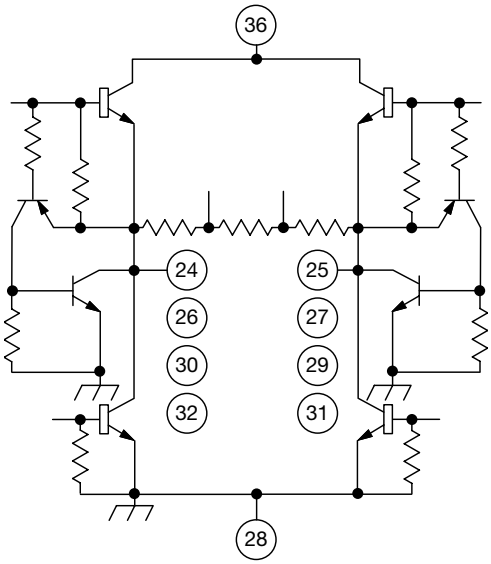
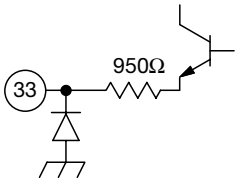
Pin Description

Pin No.	Pin Name	Input/Output	Function	Internal Equivalent Circuit
1	BSEN	Input	Battery Voltage Monitor	
2	BATT	Input	Battery Power Supply Input	Power Supply
3	RESET	Output	Reset Detect Output	
4	DEAD	Input	DEAD Time Setting	
5	SW	Output	Transistor Drive For Voltage Multiplier	
6	EO	Output	Error Amplifier Output	

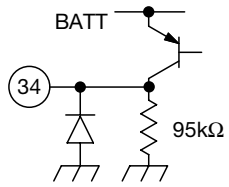
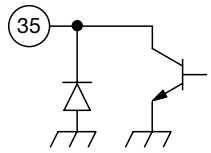
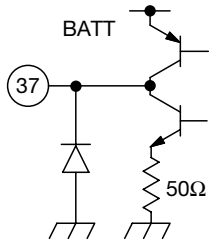
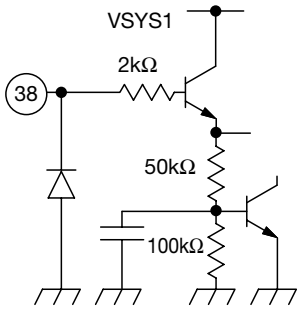
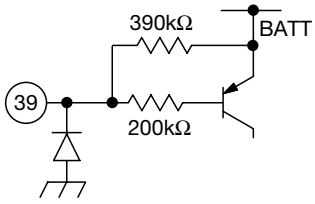
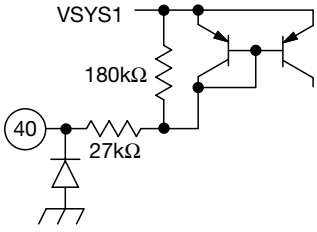
Pin Description

Pin No.	Pin Name	Input/Output	Function	Internal Equivalent Circuit
7	EI	Input	Error Amplifier Input	
8	SPRT	Output	Short Circuit Protection Setting	
9	CT	Output	Triangular–Wave Output	
10	N.C.			
11 14	OP– OP+	Input	Op Amp Negative Input Op Amp Positive Input	
12	VSYS1	Input	Control Circuit Power Supply Input	Control Circuit Power Supply
13	OPOUT	Output	Op Amp Output	

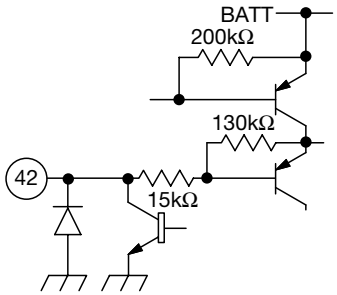
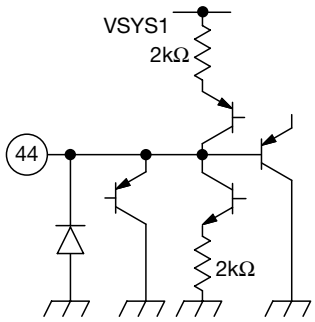
Pin Description

Pin No.	Pin Name	Input/Output	Function	Internal Equivalent Circuit
15	VSYS2	Input	Driver Pre–step Power Supply	Pre–Drive Power Supply
16	Vref	Input	Reference Voltage Input	
17 18 20 22	IN3 IN4 IN2 IN1	Input	ch3 Control Signal Input ch4 Control Signal Input ch2 Control Signal Input ch1 Control Signal Input	
19 21 23	MUTE34 MUTE2 BRAKE1	Input	ch3 and 4 Mute ch2 Mute ch1 Brake	
24 25 26 27 29 30 31 32	OUT4R OUT4F OUT3R OUT3F OUT2F OUT2R OUT1F OUT1R	Output	ch4 Negative Output ch4 Positive Output ch3 Negative Output ch3 Positive Output ch2 Positive Output ch2 Negative Output ch1 Positive Output ch1 Negative Output	
28	POWGND		Power Block Power Supply Ground	
36	HVcc	Input	H–Bridge Power Supply Input	
33	RCHG	Input	Charge Current Setting	

Pin Description

Pin No.	Pin Name	Input/Output	Function	Internal Equivalent Circuit
34	AMUTE	Output	Reset Invert Output	
35	EMP	Output	Empty Detect Output	
37	PSW	Output	PWM Transistor Drive	
38	CLK	Input	External Clock Synchronizing Input	
39	START	Input	Voltage Multiplier DC–DC Converter Start	
40	OFF	Input	Voltage Multiplier DC–DC Converter OFF	

Pin Description

Pin No.	Pin Name	Input/Output	Function	Internal Equivalent Circuit
41	CHGVcc	Input	Charging Circuit Power Supply Input	Charging Circuit Power Supply
42	SEL	Input Output	Empty Detect Level Switch	
43	PREGND		Pre Section Power Supply Ground	Pre Section Power Supply Ground
44	PWMFIL	Input	PWM Phase Compensation	

* The positive and negative outputs are the polarity with respect to the input

Absolute Maximam Ratings (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	Vcc *1	13.5	V
Driver Output Current	Io	500	mA
Power Dissipation	Pd	625 *2	mW
Operating Temperature	Topr	–30 ~ +85	°C
Storage Temperature	Tstg	–55 ~ +150	°C

*1 Vcc shows input voltage of VSYS1,VSYS2,HVcc,BATT,and CHGVcc.

*2 Reduced by 5mW for each increase in Ta of 1°C over 25°C.

Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Control Circuit Power Supply Voltage	VSYS1	2.7	3.2	5.5	V
Pre-Driver Circuit Power Supply Voltage	VSYS2	2.7	3.2	5.5	V
H-Bridge Power Supply Voltage	HVcc		PWM	BATT	V
Power Supply Voltage	BATT	1.5	2.4	8.0	V
Charging circuit Power Supply Voltage	CHGVcc	3.0	4.5	8.0	V
Operating Temperature	Ta	–10	25	70	°C

Electrical Characteristics (unless otherwise specified, Ta=25°C , BATT=2.4V, VSYS1=VSYS2=3.2V,Vref=1.6V, CHGVcc=0V,fCLK=88.2kHz)

Item	Symbol	Measurement Conditions	Min.	Typ.	Max.	Unit
<Common Section>						
BATT Stand-by Current	Ist	BATT=9.0V, VSYS1=VSYS2=Vref=0V		0	3	µA
BATT Supply Current (No load)	Ibat	HVcc=0.45V, MUTE34=3.2V		2.5	4.0	mA
VSYS1 Supply Current (No load)	Isys1	HVcc=0.45V, MUTE34=3.2V, EI=0V		4.7	6.4	mA
VSYS2 Supply Current (No load)	Isys2	HVcc=0.45V, MUTE34=3.2V		4.1	5.5	mA
CHGVcc Supply Current (No load)	Icgvcc	CHGVcc=4.5V, Rout=OPEN		0.65	2.00	mA
<H–Bridge Driver Part>						
Voltage Gain ch1,ch3.ch4	Gvc134		12	14	16	dB
Voltage Gain ch2	Gvc2		21.5	23.5	24.5	dB
Gain Error By Polarity	⊿Gvc		–2	0	2	dB
Input pin resistance ch1,ch3,ch4	Rin134	IN=1.7V and 1.8V	9	11	13	kΩ
Input pin resistance ch2	Rin2	IN=1.7V and 1.8V	6	7.5	9	kΩ
Maximum Output Voltage	Vout	RL=8Ω, HVcc=BATT=4.0V, IN=0-3.2V	1.9	2.1		V
Saturation Voltage (Lower)	VsatL	Io=–300mA, IN=0 and 3.2V		240	400	mV
Saturation Voltage (Upper)	VsatU	Io=–300mA, IN=0 and 3.2V		240	400	mV
Input Offset Voltage	Voi		–8	0	8	mV
Output Offset Voltage ch1,ch3,ch4	Voo134	Vref=IN=1.6V	–50	0	50	mV
Output Offset Voltage ch2	Voo2	Vref=IN=1.6V	–130	0	130	mV
Dead Zone	Vdb		–10	0	10	mV
BRAKE1ON Threshold Voltage	Vbron	IN1=1.8V	2.0			V
BRAKE1OFF Threshold Voltage	Vbroff	IN1=1.8V			0.8	V
MUTE2 ON Threshold Voltage	Vm2on	IN2=1.8V	2.0			V

Electrical Characteristics

(unless otherwise specified, Ta=25°C , BATT=2.4V, VSYS1=VSYS2=3.2V,Vref=1.6V, CHGVcc=0V,fCLK=88.2kHz)

Item	Symbol	Measurement Conditions	Min.	Typ.	Max.	Unit
<H−Bridge Driver Part>						
MUTE2 OFF Threshold Voltage	V_{M2OFF}	IN2=1.8V			0.8	V
MUTE34 ON Threshold Voltage	V_{M34ON}	IN3=IN4=1.8V			0.8	V
MUTE34 OFF Threshold Voltage	V_{M34OFF}	IN3=IN4=1.8V	2.0			V
Vref ON Threshold Voltage	V_{refON}	IN1=IN2=IN3=IN4=1.8V	1.2			V
Vref OFF Threshold Voltage	V_{refOFF}	IN1=IN2=IN3=IN4=1.8V			0.8	V
BRAKE1 Brake Current	I_{BRAKE1}	Current difference between BRAKE pin "H" time and "L" time.	4	7	10	mA
<PWM Power Supply Driving>						
PSW Sink Current	I_{PSW}	IN1=2.1V	10	13	17	mA
HVcc Level Shift Voltage	V_{SHIF}	IN1=1.8V, HV_{CC}−OUT1F	0.35	0.45	0.55	V
HVcc Leak Current	I_{HLK}	HV_{CC}=9.0V, VSYS1=VSYS2=BATT=0V		0	5	µA
PWM Amp Transfer Gain	G_{PWM}	IN1=1.8V, HV_{CC}=1.2 ~ 1.4V	1/60	1/50	1/40	1/kΩ
<DC−DC Converter>						
<Error Amp>						
VSYS1 Threshold Voltage	V_{S1TH}		3.05	3.20	3.35	V
EO Pin Output Voltage "H"	V_{EOH}	EI=0.7V, Io=−100µA	1.4	1.6		V
EO Pin Output Voltage "L"	V_{EOL}	EI=1.3V, Io=100µA			0.3	V
<Short Circuit Protection>						
SPRT Pin Voltage	V_{SPR}	EI=1.3V		0	0.1	V
EO=H SPRT Pin Current1	I_{SPR1}	EI=0.7V	6	10	16	µA
OFF=L SPRT Pin Current2	I_{SPR2}	EI=1.3V, OFF=0V	12	20	32	µA
SPRT Pin Current3 Over-Voltage	I_{SPR3}	EI=1.3V, BATT=9.5V	12	20	32	µA
SPRT Pin Impedance	R_{SPR}		175	220	265	kΩ
SPRT Pin Threshold Voltage	V_{SPTH}	EI=0.7V, C_T=0V	1.10	1.20	1.30	V
Over-Voltage Protection Detect	V_{HVPR}	BSEN Pin Voltage	8.0	8.4	9.0	V
<Transistor Driving>						
SW Pin Output Voltage1 "H"	V_{SW1H}	BATT=C_T=1.5V, VSYS1=VSYS2=0V, Io=−2mA Starting Time	0.78	0.98	1.13	V
SW Pin Output Voltage2 "H"	V_{SW2H}	C_T=0V, Io=−10mA, EI=0.7V, SPRT=0V	1.00	1.50		V
SW Pin Output Voltage2 "L"	V_{SW2L}	C_T=2.0V, Io=10mA		0.30	0.45	V
SW Pin Oscillating Frequency1	f_{SW1}	C_T=470pF, VSYS1=VSYS2=0V Starting Time	65	80	95	kHz
SW Pin Oscillating Frequency2	f_{SW2}	C_T=470pF, CLK=0V	60	70	82	kHz
SW Pin Oscillating Frequency3	f_{SW3}	C_T=470pF		88.2		kHz
SW Pin Minimum Pulse Width	T_{SWmin}	C_T=470pF, EO=0.5V→ 0.7V Sweep	0.01		0.60	µs
Pulse Duty Start	D_{SW1}	C_T=470pF, VSYS1=VSYS2=0V	40	50	60	%
Max.Pulse Duty At Self-Running	D_{SW2}	C_T=470pF, EI=0.7V, CLK=0V	70	80	90	%
Max. Pulse Duty At CLK Synchronization	D_{SW3}	C_T=470pF, EI=0.7V	65	75	85	%
<Interface>						
OFF Pin Threshold Voltage	V_{OFTH}	EI=1.3V			VSYS1-2.0	V
OFF Pin Bias Current	I_{OFF}	OFF=0V	75	95	115	µA
START Pin ON Threshold Voltage	V_{STATH1}	VSYS1=VSYS2=0V, C_T=2.0V			BATT-1.0	V
START Pin OFF Threshold Voltage	V_{STATH2}	VSYS1=VSYS2=0V, C_T=2.0V	BATT-0.3			V

Electrical Characteristics

(unless otherwise specified, Ta=25°C , BATT=2.4V, VSYS1=VSYS2=3.2V,Vref=1.6V, CHGVcc=0V,fCLK=88.2kHz)

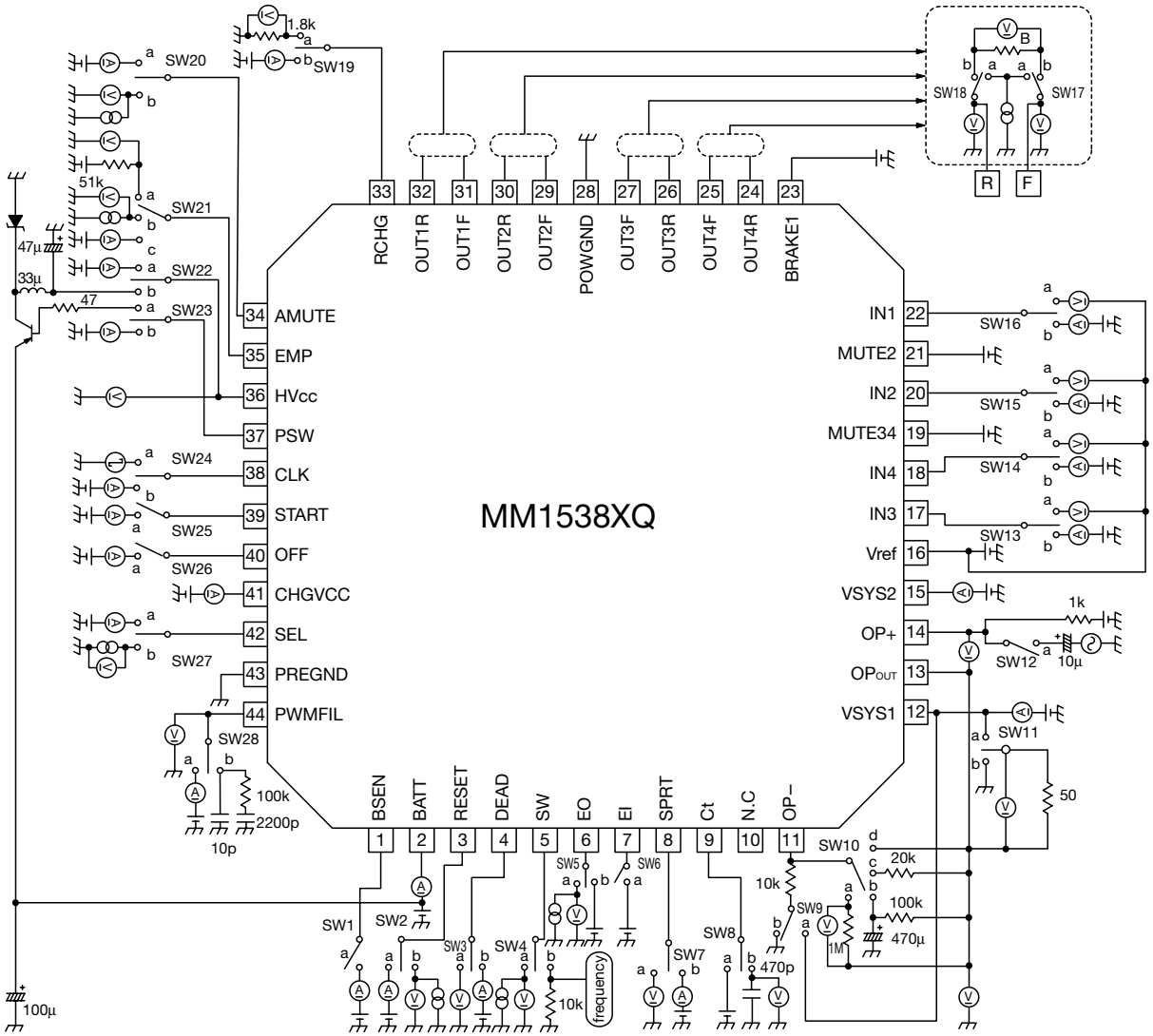
Item	Symbol	Measurement Conditions	Min.	Typ.	Max.	Unit
<Interface>						
START Pin Bias Current	I_{START}	START=0V	10 13	20 16	30 19	µA
CLK Pin Threshold Voltage"H"	V_{CLKTHH}		2.0			V
CLK Pin Threshold Voltage"L"	V_{CLKTHL}				0.8	V
CLK Pin Bias Current	I_{CLK}	CLK=3.2V			10	µA
<Dead Time>						
DEAD Pin Impedance	R_{DEAD}		52	65	78	kΩ
DEAD Pin Output Voltage	V_{DEAD}		0.78	0.88	0.98	V
<Starter Circuit>						
Starter Switching Voltage	V_{STNM}	VSYS1=VSYS2=0V→3.2V, START=0V	2.3	2.5	2.7	V
Starter Switching Hysteresis Width	V_{SNHS}	START=0V	130	200	300	mV
Discharge Release	V_{DIS}		1.63	1.83	2.03	V
<Empty Detection>						
EMP Detection Voltage 1	V_{EMPT1}	VSEL=0V	2.1	2.2	2.3	V
EMP Detection Voltage 2	V_{EMPT2}	ISEL=– 2µA	1.7	1.8	1.9	V
EMP Detection Hysteresis Voltage 1	V_{EMHS1}	VSEL=0V	25	50	100	mV
EMP Detection Hysteresis Voltage 2	V_{EMHS2}	ISEL=– 2µA	25	50	100	mV
EMP Pin Output Voltage	V_{EMP}	Io=1mA, BSEN=1V			0.5	V
EMP Pin Output Leak Current	I_{EMPL}	BSEN=2.4V			1.0	µA
BSEN Pin Input Resistance	R_{BSEN}	VSEL=0V	17	23	27	kΩ
BSEN Pin Leak Current	I_{BSENL}	VSYS1=VSYS2=0V, BSEN=4.5V			1.0	µA
SEL Pin Detection Voltage	V_{SELTH}	V_{SELTH}=BATT–SEL, BSEN=2.0V	1.5			V
SEL Pin Detection Current	I_{SELT}		–2			µA
<Reset Circuit>						
VSYS1 RESET Threshold Voltage Ratio	H_{SRT}	Comparison with error amplifier threshold voltage	85	90	95	%
RESET Detection Hysteresis Width	V_{RSTHS}		25	50	100	mV
RESET Pin Output Voltage	V_{RST}	Io=1mA, VSYS1=VSYS2=2.8V			0.5	V
RESET Pin PULL UP Resistance	R_{RST}		72	90	108	kΩ
AMUTE Pin Output Voltage 1	V_{AMT1}	Io=–1mA, VSYS1=VSYS2=2.8V	BATT–0.4		BATT	V
AMUTE Pin Output Voltage 2	V_{AMT2}	Io=–1mA, START=0V, VSYS1=VSYS2=0V	BATT–0.4		BATT	V
AMUTE Pin PULL DOWN Resistance	R_{AMT}		77	95	113	kΩ
<Op Amp>						
Input Bias Current	I_{BIAS}	OP+=1.6V			300	nA
Input Offset Voltage	V_{OIOP}		–5.5	0	5.5	mV
High Level Output Voltage	V_{OHOP}	R_L=OPEN	2.8			V
Low level Output Voltage	V_{OLOP}	R_L=OPEN			0.2	V
Output Drive Current (Source)	I_{SOU}	50Ω GND		–6.5	–3.0	mA
Output Drive Current (Sink)	I_{SIN}	50Ω VSYS1	0.4	0.7		mA
Open Loop Voltage Gain	GVO	V_{IN}=–75dBV, f=1kHz		70		dB
Slew Rate	SR			0.5		V/µs
<Battery Charging Circuit>						
RCHG Pin Bias Voltage	V_{RCHG}	$CHGV_{CC}$=4.5V, RCHG=1.8kΩ	0.71	0.81	0.91	V

Electrical Characteristics

(unless otherwise specified, Ta=25°C , BATT=2.4V, VSYS1=VSYS2=3.2V,Vref=1.6V, CHGVcc=0V,fCLK=88.2kHz)

Item	Symbol	Measurement Conditions	Min.	Typ.	Max.	Unit
<Battery Charging Circuit>						
RCHG Pin Output Resistance	R_{RCHG}	CHGVcc=4.5V, RCHG=0.5 and 0.6V	0.75	0.95	1.20	kΩ
SEL Pin Leak Current 1	I_{SELLK1}	CHGVcc=4.5V, RCHG=OPEN, BATT=4.5V			1.0	µA
SEL Pin Leak Current 2	I_{SELLK2}	CHGVcc=0.6V, RCHG=1.8kΩ, BATT=4.5V			1.0	µA
SEL Pin Saturation Voltage	V_{SELCG}	CHGVcc=4.5V, Io=300mA, RCHG=0Ω		0.45	1.00	V

Measuring Circuit



Switching Position Table

Item	SW No.									
	1	4	5	6	7	8	22	24	25	26
BATT Stand-by Current	–	–	–	–	–	–	–	–	–	–
BATT Supply Current (No load)	–	–	–	–	–	–	a	–	a	–
VSYS1 Supply Current (No load)	–	–	–	a	–	–	a	–	a	–
VSYS2 Supply Current (No load)	–	–	–	–	–	–	a	–	a	–
CHGVcc Supply Current (Noload)	–	–	–	–	–	–	–	–	–	–
VSYS1 Threshold Voltage	–	–	a	–	–	–	–	–	–	–
EO Pin Output Voltage "H"	–	–	a	a	–	–	–	–	–	–
EO Pin Output Voltage "L"	–	–	a	a	–	–	–	–	–	–
SPRT Pin Voltage	–	–	–	a	a	–	–	–	–	–
SPRT Pin Current1 EO="H"	–	–	–	a	b	–	–	–	–	–
SPRT Pin Current2 OFF="L"	–	–	–	a	b	–	–	–	–	a
SPRT Pin Current3 Over-Voltage	a	–	–	a	b	–	–	–	–	–
SPRT Pin Impedance	–	–	–	–	b	–	–	–	–	–
SPRT Pin Threshold Voltage	–	–	–	a	a	a	–	–	–	–
Over-Voltage Protection Detect	a	–	–	–	a	–	–	–	–	–
SW Pin Output Voltage1 "H"	–	a	–	–	–	a	–	–	a	–
SW Pin Output Voltage2 "H"	–	a	–	a	b	a	–	–	–	–
SW Pin Output Voltage2 "L"	–	a	–	–	–	a	–	–	–	–
SW Pin Oscillating Frequency 1	–	b	–	–	–	b	–	–	a	–
SW Pin Oscillating Frequency 2	–	b	–	–	–	b	–	b	–	–
SW Pin Oscillating Frequency 3	–	b	–	–	–	b	–	a	–	–
SW Pin Minimum Pulse Width	–	b	b	–	–	b	–	–	–	–
Pulse Duty Start	–	b	–	–	–	b	–	b	a	–
Max. Pulse Duty At Self-Running	–	b	–	–	–	b	–	b	–	–
Max. Pulse Duty At CLK Synchronization	–	b	–	a	–	b	–	a	–	–

– : Turn off switch

Switching Position Table

Item	SW No.									
	2	3	4	6	7	8	20	24	25	26
DEAD Pin Impedance	–	b	–	–	–	–	–	–	–	–
DEAD Pin Output Voltage	–	a	–	–	–	–	–	–	–	–
OFF Pin Threshold Voltage	–	–	–	a	a	–	–	–	–	a
OFF Pin Bias Current	–	–	–	–	–	–	–	–	–	a
START Pin ON Threshold Voltage	–	–	a	–	–	a	–	–	a	–
START Pin OFF Threshold Voltage	–	–	a	–	–	a	–	–	a	–
START Pin Bias Current	–	–	–	–	–	–	–	–	a	–
CLK Pin Threshold Voltage"H"	–	–	a	–	–	b	–	b	–	–
CLK Pin Threshold Voltage"L"	–	–	a	–	–	b	–	b	–	–
CLK Pin Bias Current	–	–	–	–	–	–	–	a	–	–
Starter Switching Voltage	–	–	a	–	–	–	–	–	a	–
Starter Switching Hysteresis Width	–	–	a	–	–	–	–	–	a	–
Discharge Release Voltage	–	–	–	–	a	–	–	–	–	–
VSYS1 Pin RESET Threshold Voltage Ratio	b	–	–	–	–	–	–	–	–	–
RESET Detection Hysteresis Width	b	–	–	–	–	–	–	–	–	–
RESET Pin Output voltage	b	–	–	–	–	–	–	–	–	–
RESET Pin PULL UP Resistance	a	–	–	–	–	–	–	–	–	–
AMUTE Pin Output Voltage 1	–	–	–	–	–	–	b	–	–	–
AMUTE Pin Output Voltage 2	–	–	–	–	–	–	b	–	a	–
AMUTE Pin PULL DOWN Resistance	–	–	–	–	–	–	a	–	–	–

– : Turn off switch

Switching Position Table

Item	SW No.						
	1	9	10	11	12	21	27
EMP Detection Voltage 1	a	–	–	–	–	a	a
EMP Detection Voltage 2	a	–	–	–	–	a	b
EMP Detection Hysteresis Voltage 1	a	a	–	–	–	a	a
EMP Detection Hysteresis Voltage 2	a	–	–	–	–	a	b
EMP Pin Output Voltage	a	–	–	–	–	b	–
EMP Pin Output Leak Current	a	–	–	–	–	c	–
BSEN Pin Input Resistance	a	–	–	–	–	–	a
BSEN Pin Leak Current	a	–	–	–	–	–	–
SEL Pin Detection Voltage	a	–	–	–	–	a	a
SEL Pin Detection Current	a	–	–	–	–	a	b
Input Bias Current	–	–	a	–	–	–	–
Input Offset Voltage	–	–	d	–	–	–	–
"H" Level Output Voltage	–	b	c	–	–	–	–
"L" Level Output Voltage	–	a	c	–	–	–	–
Output Drive Current (Source)	–		d	b	–	–	–
Output Drive Current (Sink)	–	–	d	a	–	–	–
Open Loop Voltage Gain	–	–	b	–	a	–	–
Slew Rate	–	–	d	–	a	–	–

– : Turn off switch

Switching Position Table

Item		SW No.						
		13	14	15	16	17	18	22
Voltage Gain	ch1R	–	–	–	b	b	b	a
	ch2R	–	–	b	–	b	b	a
	ch3R	b	–	–	–	b	b	a
	ch4R	–	b	–	–	b	b	a
Gain Error By Polarity	ch1	–	–	–	b	b	b	a
	ch2	–	–	b	–	b	b	a
	ch3	b	–	–	–	b	b	a
	ch4	–	b	–	–	b	b	a
Input pin resistance	ch1	–	–	–	b	b	b	a
	ch2	–	–	b	–	b	b	a
	ch3	b	–	–	–	b	b	a
	ch4	–	b	–	–	b	b	a
Maximum Output Voltage	ch1R	–	–	–	b	b	b	a
	ch2R	–	–	b	–	b	b	a
	ch3R	b	–	–	–	b	b	a
	ch4R	–	b	–	–	b	b	a
Saturation Voltage (Lower)	ch1F	–		–	b	a	–	a
	ch1R	–		–	b	–	a	a
	ch2F	–		b	–	a	–	a
	ch2R	–		b	–	–	a	a
	ch3F	b		–	–	a	–	a
	ch3R	b		–	–	–	a	a
	ch4F	–	b	–	–	a	–	a
	ch4R	–	b	–	–	–	a	a
Saturation Voltage (Upper)	ch1F	–	–	–	b	a	–	a
	ch1R	–	–	–	b	–	a	a
	ch2F	–	–	b	–	a	–	a
	ch2R	–	–	b	–	–	a	a
	ch3F	b	–	–	–	a	–	a
	ch3R	b	–	–	–	–	a	a
	ch4F	–	b	–	–	a	–	a
	ch4R	–	b	–	–	–	a	a
Input Offset Voltage	ch1	–	–	–	a	–	–	a
	ch2	–	–	a	–	–	–	a
	ch3	a	–	–	–	–	–	a
	ch4	–	a	–	–	–	–	a
Output Offset Voltage	ch1	–	–	–	b	b	b	a
	ch2	–	–	b	–	b	b	a
	ch3	b	–	–	–	b	b	a
	ch4	–	b	–	–	b	b	a
Dead Zone	ch1	–	–	–	b	b	b	a
	ch2	–	–	b	–	b	b	a
	ch3	b	–	–	–	b	b	a
	ch4	–	b	–	–	b	b	a

– : Turn off switch

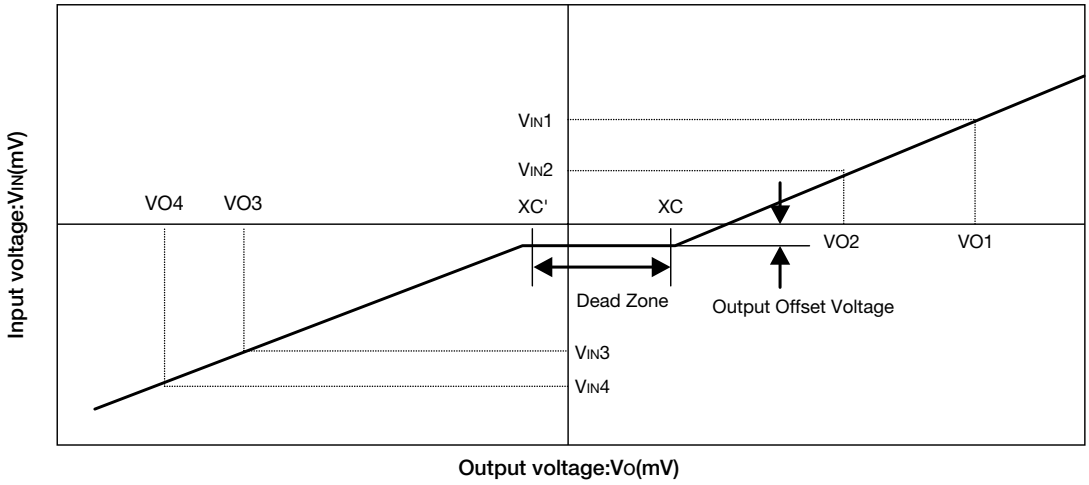
Switching Position Table

Item		SW No.								
		13	14	15	16	17	18	22	23	28
BRAKE1 ON Voltage	ch1	–	–	–	b	b	b	a	–	–
BRAKE1 OFF Voltage	ch1	–	–	–	b	b	b	a	–	–
MUTE2 ON Voltage	ch2	–	–	b	–	b	b	a	–	–
MUTE2 OFF Voltage	ch2	–	–	b	–	b	b	a	–	–
MUTE34 ON Voltage	ch3	b	–	–	–	b	b	a	–	–
	ch4	–	b	–	–	b	b	a	–	–
MUTE34 OFF Voltage	ch3	b	–	–	–	b	b	a	–	–
	ch4	–	b	–	–	b	b	a	–	–
Vref ON Voltage	ch1	–	–	–	b	b	b	a	–	–
	ch2	–	–	b	–	b	b	a	–	–
	ch3	b	–	–	–	b	b	a	–	–
	ch4	–	b	–	–	b	b	a	–	–
Vref OFF Voltage	ch1	–	–	–	b	b	b	a	–	–
	ch2	–	–	b	–	b	b	a	–	–
	ch3	b	–	–	–	b	b	a	–	–
	ch4	–	b	–	–	b	b	a	–	–
BREAK1 Brake Current	ch1	–	–	–	b	b	b	a	–	–
PWM Sink Current		–	–	–	b	–	–	a	b	a
HVcc Level Shift Voltage		–	–	–	b	b	b	b	a	b
HVcc Leak Current		–	–	–	–	b	b	a	–	–
PWM Amp Transfer Gain		–	–	–	b	b	b	a	–	–

Item	SW No.	
	19	27
CHGSET Pin Bias Voltage	a	–
CHGSET Pin Output Resistance	b	–
SEL Pin Leak Current 1	–	a
SEL Pin Leak Current 2	a	a
SEL Pin Saturation Voltage	b	b

– : Turn off switch

Switching Position Table



◎Voltage Gain

$$G_{VC}(+)=20\log\frac{VO1-VO2}{V_{IN}1-V_{IN}2}$$

$$G_{VC}(-)=20\log\frac{VO3-VO4}{V_{IN}3-V_{IN}4}$$

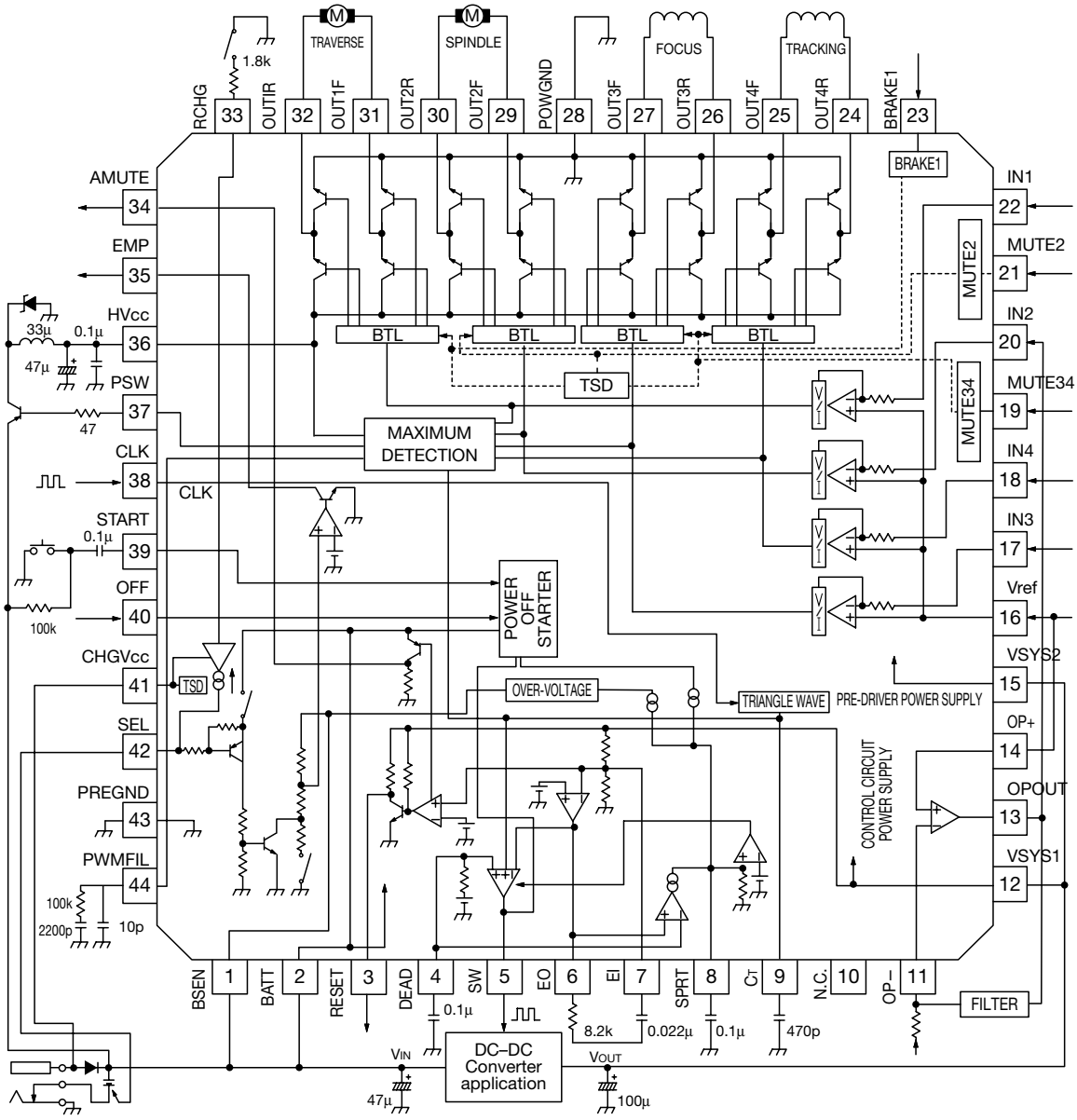
◎Gain Error By Polarity

$$G_{VC}=G_{VC}(+)-G_{VC}(-)$$

◎Dead Zone

$$XC-XC'=\frac{V_{IN}2\cdot VO1-V_{IN}1\cdot VO2}{VO1-VO2}-\frac{V_{IN}3\cdot VO4-V_{IN}4\cdot VO3}{VO3-VO4}$$

Application Circuit



· We shall not be liable for any trouble or damege caused by using this circuit.
· In the event a problem which may affect industrial property or any other rights of us or a third party is encountered during the use of information described in these circuit, Mitsumi Electric Co., Ltd. shall not be liable for any such problem, nor grant a license therefor.

Circuit operation

1 H-bridge driver block

(1) Gain setting

· The driver input resistance (ch 1,3 and 4) are 11kΩ typ. ,ch2 is 7.5kΩ typ. . Set the gain according to the following formula.

ch1 ch2 ch3	GV=20log	$\frac{55k}{11k+R}$	(db)
ch2	GV=20log	$\frac{110k}{7.5k+R}$	(db)

R:Externally-connected input

· The driver output stage power supply is HVcc(36PIN), and the bridge circuit power supply is VSYS2 (15PIN). Connect a bypass capacitor between these two power supplies(approximately 0.1μF).

(2) Mute function

· Of the four drivers,ch1 has a brake function,and the other channels have a mute function.
· When BRAKE1(23PIN)is set to high level, both ch1 outputs go low level, and the circuit enters brake mode.
· When MUTE2(21PIN)is set to high level, the ch2 output is muted.
· When MUTE34(19PIN)is set to high level, the ch3 and 4 outputs are muted.

(3) Vref drop mute

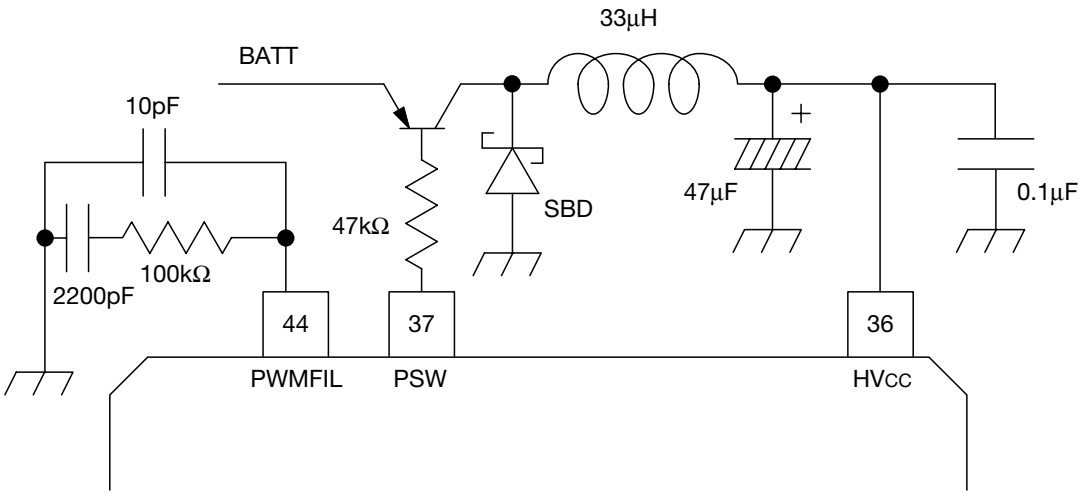
· When the voltage applied to Vref(16PIN)is 1.0V or less typ. , the driver outputs are set to high impedance.

(4) Thermal shutdown

· When the chip temperature reaches 150°C typ. the output current is cut. The chip starts operating again at about 120°C typ. .

2 PWM power supply drive block

· This detects the maximun output level from among the four channels, and supplies the load drive power supply(36PIN)for the PWM. The external components are a PNP transistor, coil, Schottky diode,and capacitor.

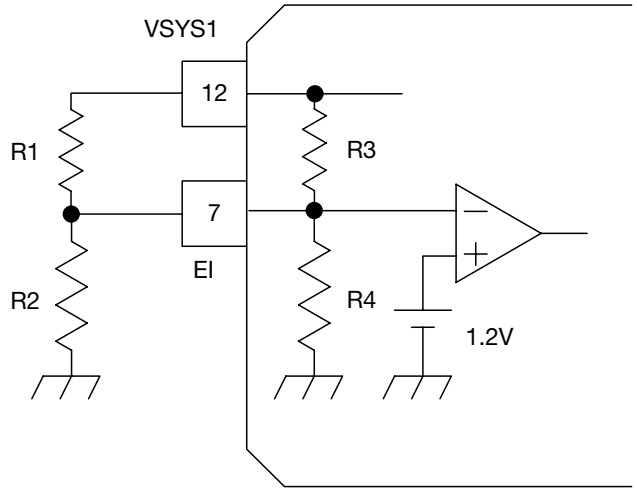


3 DC-DC converter block

(1) Output voltage

· 3.2V typ. voltage multiplier circuit can be constructed using external components. This voltage can be varied with the addition of an external resistor. The setting method is as follows.

$$VSYS1=1.2\times\frac{\frac{R1\cdot R3}{R1+R3}+\frac{R2\cdot R4}{R2+R4}}{\frac{R2\cdot R4}{R2+R4}}\ (V)$$



R1=external resistor
R2=external resistor
R3=35kΩ
R4=21kΩ

(2) Short protect function

· When the error amplifier output(6PIN)has switched to the high-level state,SPRT(8PIN)is charged, and when the voltage reaches 1.2V typ. , the SW(5PIN)switching stops.The time until switching stops is set by the capacitor connected to SPRT(8PIN)according to the following formula.

$$t=CSPRT\times\frac{V_{TH}}{ISPRT}\ (sec)\ \ (V_{TH}=1.2V,\ ISPRT=10\mu A)$$

(3) Soft start function

· The soft start function operates when a capacitor is connected between DEAD(4PIN)and GND.
Also, the maximum duty can be varied by connecting a resistor to 4PIN.

$$t=CDEAD\times R\ (sec)\ \ (R=65k\Omega)$$

(4) Power off function

· When low-level is applied to OFF(40PIN), SPRT(8PIN)is charged, and when the voltage reaches 1.2V typ. , the SW(5PIN)switching stops. The time until switching stops is set by the capacitor connected to SPRT(8PIN)according to the following formula.

$$t=CSPRT\ \ \frac{V_{TH}}{I_{OFF}}\ (sec)\ \ (V_{TH}=1.2V,\ I_{OFF}=20\mu A)$$

(5) Over voltage protection circuit

· When the voltage applied to BSEN(1PIN)reaches 8.4V typ. , SPRT(8PIN)is charged, and when the voltage reaches 1.2V typ. , theSW(5PIN)switching stops. The time until switching stops is set by the capacitor connected to SPRT(8PIN)according to the following formula.

$$t=CSPRT \times \frac{V_{TH}}{IHV} \text{ (sec)} \quad (V_{TH}=1.2V,\ I_{HV}=20\mu A)$$

4 Empty detector block

(1) Output voltage

· When the voltage applied to the BSEN(1PIN)falls below the detector voltage, EMP(35PIN)goes from high level to low level(open-collector output). The detector voltage has 50mV typ. of hysteresis to prevent output chattering. Use SEL(42PIN)to switch the detection voltage as shown below.

SEL	Detect Voltage	Return Voltage
L	2.20V typ.	2.25V typ.
High-Z	1.80V typ.	1.85V typ.

5 Reset circuit block

· At about 90% typ. of the DC-DC converter output voltage, RESET(3PIN)goes from low level to high level, and AMUTE(34PIN)goes from high level to low level. The reset voltage has 50mV typ. of hysteresis to prevent output chattering.

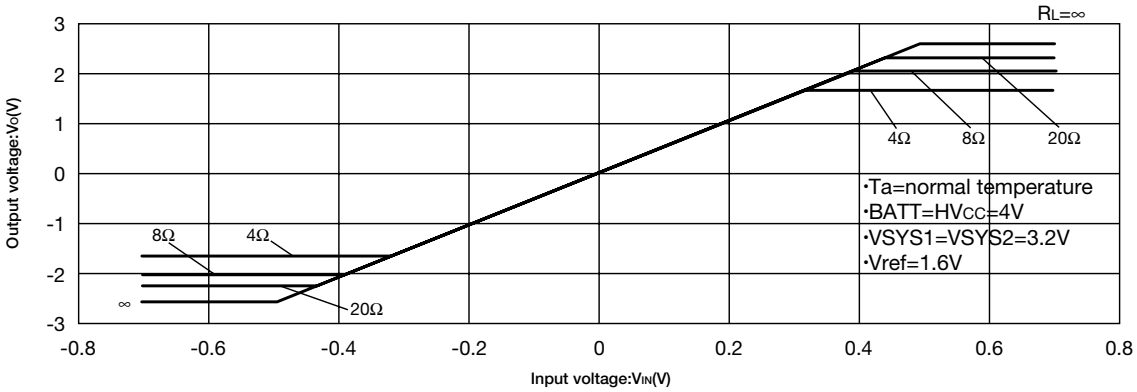
6 Charging circuit block

· The power supply for the charging circuit block is $CHGV_{CC}$(41PIN), and is independent from the other circuits.The resistance between RCHG(33PIN)and GND sets the charging current. This current is drawn from SEL(42PIN).

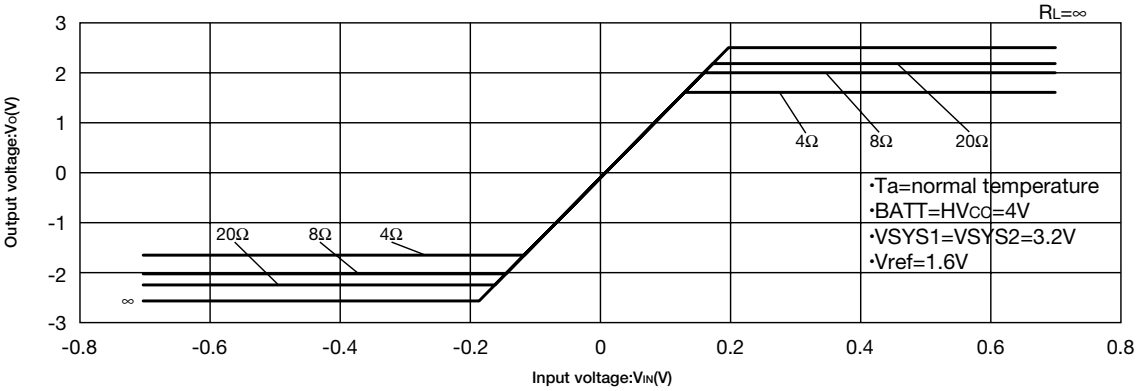
· A thermal shutdown circuit is provided,and when the chip temperature reaches 150°C typ. the charging current is cut. The chip starts operating again at about 120°C typ. .

Characteristics

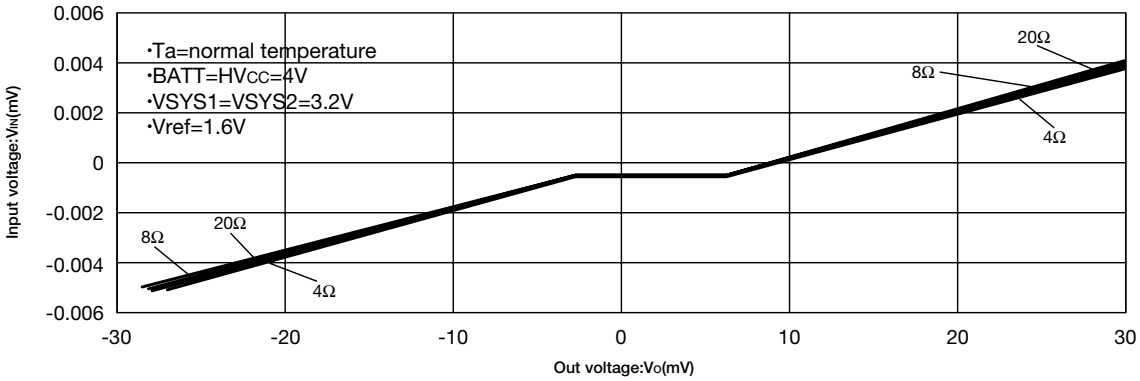
Input Load Fluctuation



Input Load Fluctuation (ch2)

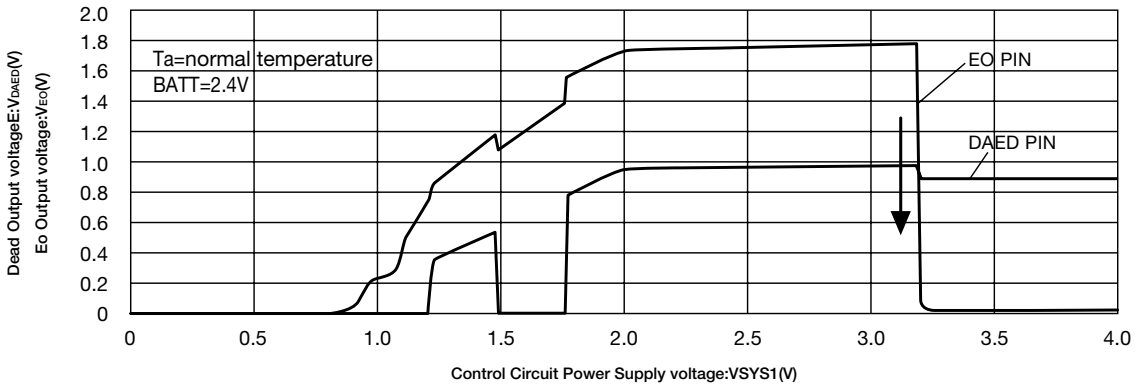


Daed Zone

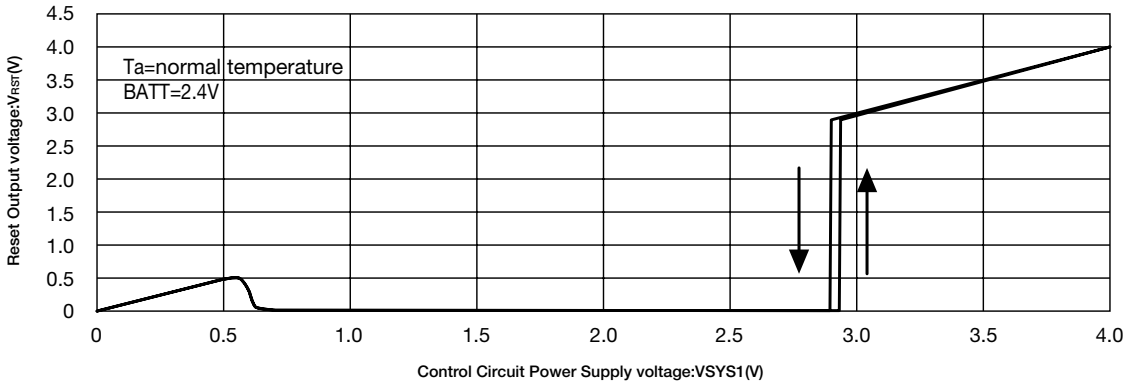


Characteristics

Error Amp Output Voltage



Resete Pin Voltage



SONY

CXA2550M/N

RF Amplifier for CD Players

Description

The CXA2550M/N is an IC developed for compact disc players. This IC incorporates an RF amplifier, focus error amplifier, tracking error amplifier, APC circuit and RF level control circuit. (The voltage-converted optical pickup output is supported.)

Features

- Low power consumption (35mW at 3.5V)
- APC circuit
- RF level control circuit
- Both single power supply and dual power supply operations possible.

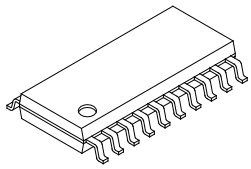
Structure

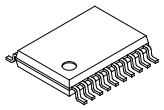
Bipolar silicon monolithic IC

Applications

Compact disc players

CXA2550M	CXA2550N
20 pin SOP (Plastic)	20 pin SSOP (Plastic)





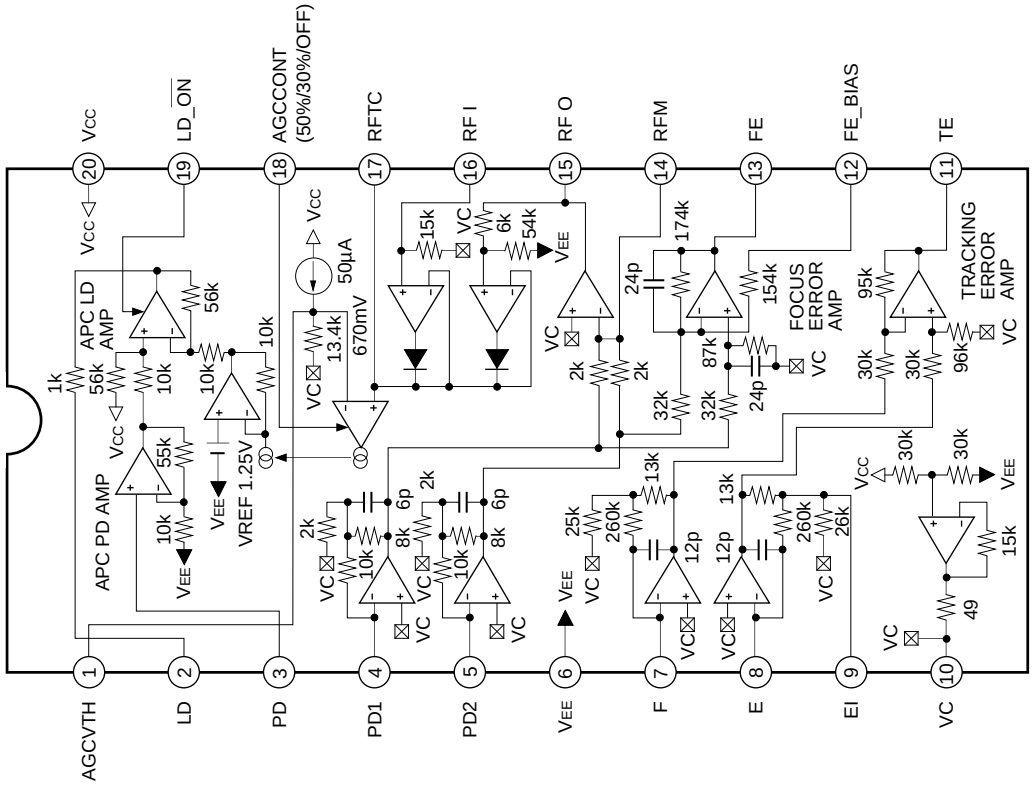
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{CC}	12	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation			
	P_D (SOP)	620	mW
	(SSOP)	370	mW

Operating Conditions

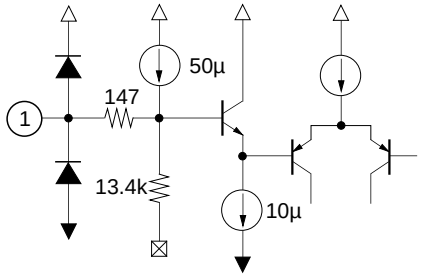
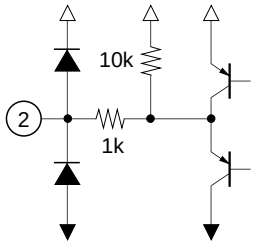
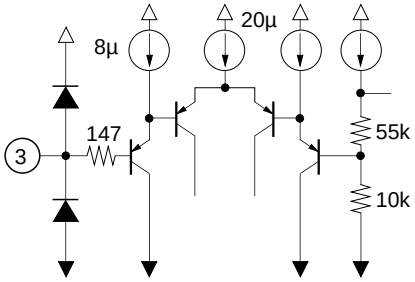
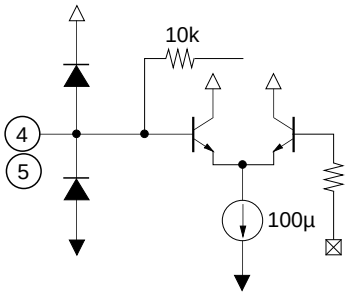
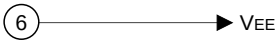
Supply voltage	$V_{CC} – V_{EE}$	3.0 to 4.0	V

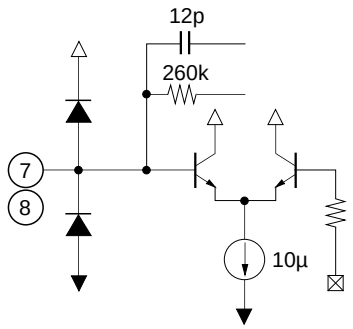
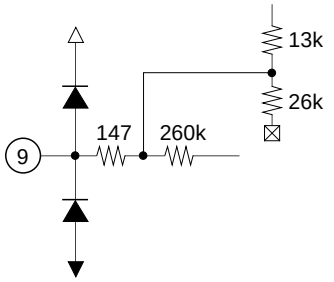
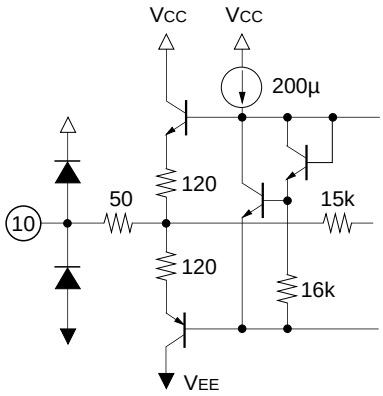
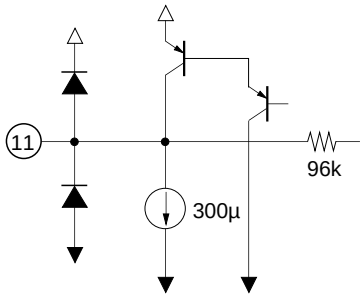
Block Diagram and Pin Configuration (Top View)

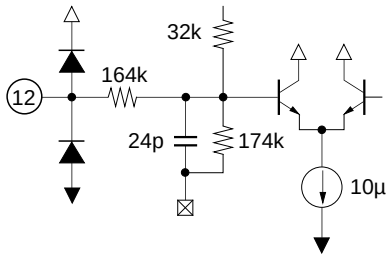
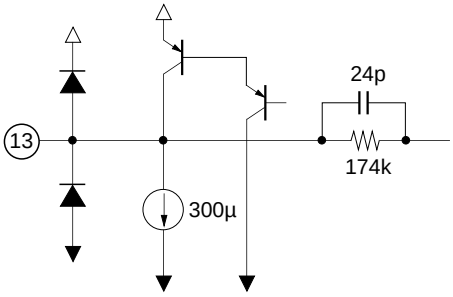
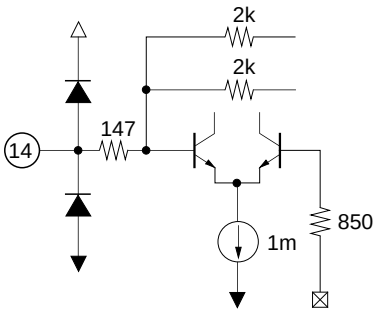
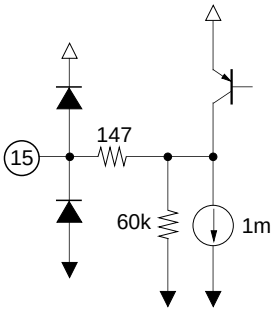


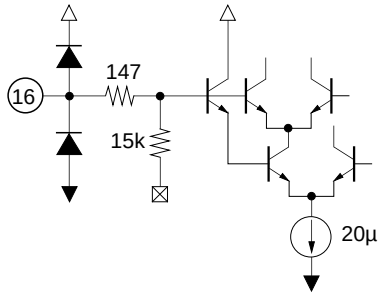
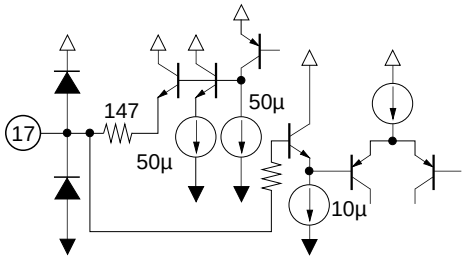
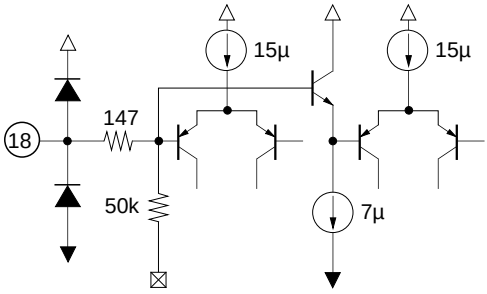
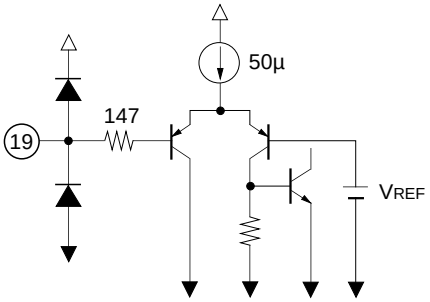
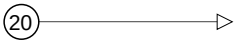
E97514-PS

Pin Description

Pin No.	Symbol	I/O	Equivalent circuit	Description
1	AGCVTH	—		Reference level variable pin for RF level control. The reference level can be varied by the external resistor.
2	LD	O		APC amplifier output pin.
3	PD	I		APC amplifier input pin.
4 5	PD1 PD2	I I		Inversion input pin for RF I-V amplifiers. Connect these pins to the photodiodes A + C and B + D respectively. The current is supplied.
6	V_{EE}	—		V_{EE} pin.

Pin No.	Symbol	I/O	Equivalent circuit	Description
7 8	F E	I I		Inversion input pin for F and E I-V amplifiers. Connect these pins to the photodiodes F and E respectively. The current is supplied.
9	EI	—		Gain adjustment pin for I-V amplifier.
10	VC	O		DC voltage output pin of (Vcc + V_{EE})/2. Connect to GND for ±1.75 power supply; connect a smoothing capacitor for single +3.5V power supply.
11	TE	O		Tracking error amplifier output pin. E-F signal is output.

Pin No.	Symbol	I/O	Equivalent circuit	Description
12	FE_BIAS	I		Bias adjustment pin for inverted side of focus error amplifier.
13	FE	O		Focus error amplifier output pin.
14	RFM	I		RF amplifier inverted side input pin. RF amplifier gain is determined by the resistor connected between this pin and RFO pin.
15	RF O	O		RF amplifier output pin.

Pin No.	Symbol	I/O	Equivalent circuit	Description
16	RF I	I		The RF amplifier output RFO is input with its capacitance coupled.
17	RFTC	—		External time-constant pin for RF level control.
18	AGCCONT	I		RF level control ON (limit level of 50%/30%)/OFF switching pin. OFF for Vcc, 30% for open or Vc and 50% for V_{EE}.
19	LD_$\overline{ON}$	I		APC amplifier ON/OFF switching pin. OFF for Vcc and ON for V_{EE}.
20	V_{CC}			Vcc pin.

Electrical Characteristics

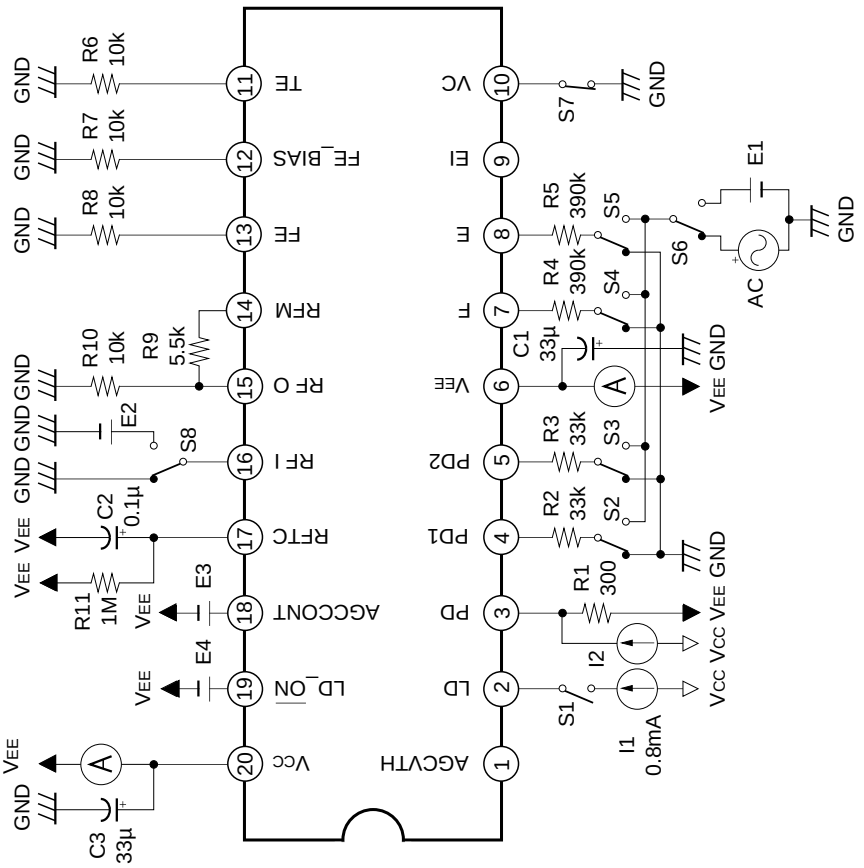
(Ta = 25°C, V_{CC} = 1.75V, V_{EE} = –1.75V, VC = GND)

No.	Measurement item		Symbol	SW conditions								Bias conditions						Measurement pin	Description of I/O waveform and measurement method		Min.	Typ.	Max.	Unit
				1	2	3	4	5	6	7	8	I1	I2	E1	E2	E3	E4							
1	Current consumption		I_{CC}							O								20	Input GND		6.37	9.8	13.23	mA
2			I_{EE}							O								6	Input GND		–13.23	–9.8	–6.37	mA
3	RF amplifier	Offset voltage 1	V15-1															15	Input resistance 33kΩ	Output DC measurement	–50.0	–10	60.0	mV
4		Voltage gain	V15-2		O	O												15	Input 1kHz 120mVp-p	Output AC measurement	16.7	19.7	22.7	dB
5		Frequency response	V15-3															15	Input 3MHz 120mVpp	Output AC measurement	–3	—	—	dB
6		Maximum output amplitude H	V15-4		O	O			O					300mV				15		Output DC measurement	1.45	—	—	V
7		Maximum output amplitude L	V15-5		O	O			O					–300mV				15		Output DC measurement	—	—	–1.25	V
8	FE amplifier	Offset voltage	V13-1															13	Input resistance 33kΩ	Output DC measurement	–120.0	0	120.0	mV
9		Voltage gain 1	V13-2		O													13	Input 1kHz 120mVp-p	Output AC measurement	16.4	19.4	22.4	dB
10		Voltage gain 2	V13-3			O												13	Input 1kHz 120mVp-p	Output AC measurement	16.4	19.4	22.4	dB
11		Voltage gain difference	V13-4															13	V13-4 = V13-2 – V13-3		–3.0	0	3.0	dB
12		Maximum output amplitude L	V13-5			O			O					300mV				13		Output DC measurement	—	—	–1.25	V
13		Maximum output amplitude H	V13-6		O				O					300mV				13		Output DC measurement	1.25	—	—	V
14	TE amplifier	Offset voltage 1	V11-1															11	Input resistance 390kΩ	Output DC measurement	–50	0	50	mV
15		Voltage gain 1	V11-2				O											11	Input 1kHz 240mVp-p	Output AC measurement	7.3	10.3	13.3	dB
16		Voltage gain 2	V11-3					O										11	Input 1kHz 240mVp-p	Output AC measurement	7.3	10.3	13.3	dB
17		Voltage gain difference	V11-4															11	V11-4 = V11-2 – V11-3		–3.0	0	3.0	dB
18		Maximum output amplitude H	V11-5				O		O					1V				11		Output DC measurement	1.25	—	—	V
19		Maximum output amplitude L	V11-6					O	O					1V				11		Output DC measurement	—	—	–1.25	V
20	APC	Output voltage 1	V2-1										450µA			2.7V	2.0V	2		Output DC measurement	–830	–330	170	mV
21		Output voltage 2	V2-2										570µA			2.7V	2.0V	2		Output DC measurement	470	970	1470	mV
22		Output voltage 3	V2-3										0µA			2.7V	0.5V	2	LD OFF	Output DC measurement	1400	1590	—	mV
23		Maximum output amplitude	V2-5	O								0.8mA	0µA			2.7V	2.0V	2		Output DC measurement	–600	—	100	mV

No.	Measurement item		Symbol	SW conditions								Bias conditions						Measurement pin	Description of I/O waveform and measurement method		Min.	Typ.	Max.	Unit
				1	2	3	4	5	6	7	8	I1	I2	E1	E2	E3	E4							
24	RF level control	50% limit	V2-7		O	O							800µA	50mV		0.5V/ 2.7V	2.0V	2	Level control: 50% – Level control OFF		–1900	–1322	–100	mV
25		30% limit	V2-8		O	O							700µA	50mV		1.3V/ 2.7V	2.0V	2	Level control: 30% – Level control OFF		–1700	–1163	–200	mV
26		–50% limit	V2-9						O		O		230µA		800mV	0.5V/ 2.7V	2.0V	2	Level control: –50% – Level control OFF		700	1471	1900	mV
27		–30% limit	V2-10						O		O		320µA		800mV	2.2V/ 2.7V	2.0V	2	Level control: –30% – Level control OFF		700	1204	1700	mV
28	AGCCONT	High Level	V18-1															18			2.7	—	—	V
29		Middle Level	V18-2															18			1.3	—	2.2	V
30		Low Level	V18-3															18			—	—	0.5	V
31	Center output voltage		V10-1							O								10		Output DC measurement	–100	—	100	mV

Note) O in the SW conditions 7 represents the OFF state.

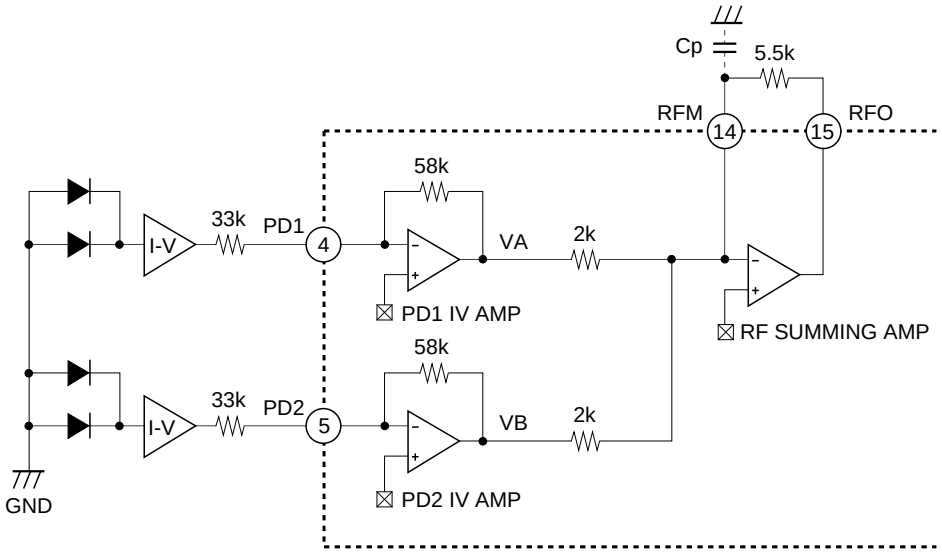
Electrical Characteristics Measurement Circuit



Description of Functions

RF Amplifier

The photodiode current input to the input pins (PD1, PD2) are current-to-voltage (I-V) converted by the equivalent resistance of 58kΩ at PD I-V amplifiers, respectively. The signal is added by the RF summing amplifier and then the I-V converted output voltage of the photodiode (A + B + C + D) is output to RFO pin. This pin is used check the eye pattern.

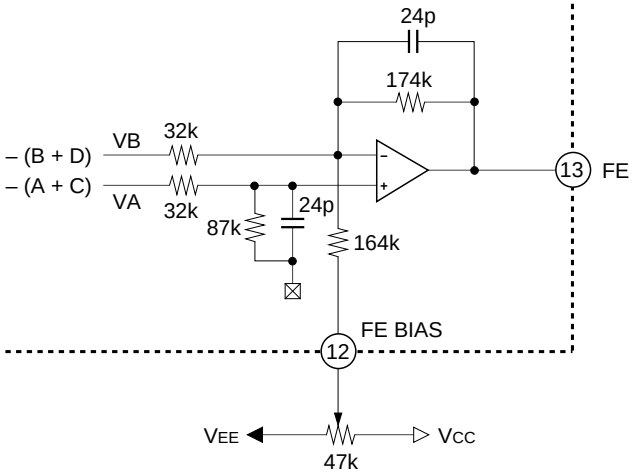


The frequency response of the RF output signal can be equalized by adding the capacitance (Cp) to RFI pin. The low frequency component of the RFO output voltage is as follows;

$$V_{RFO} = -2.75 \times (V_A + V_B)$$
$$= 159.5k\Omega \times (iPD1 + iPD2)$$

Focus Error Amplifier

The difference between the RF I-V amplifier output VA and VB is obtained and the I-V converted voltage of the photodiode (A + C – B – D) is output.

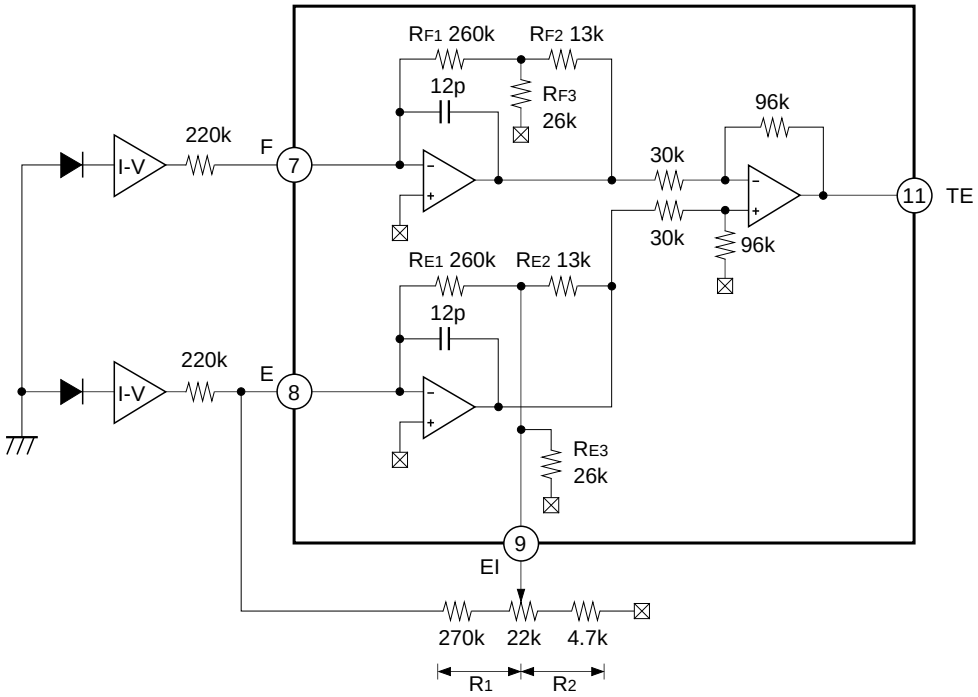


The FE output voltage (low frequency) is as follows;

$$V_{FE} = 5.4 \times (V_A - V_B)$$
$$= (iPD2 - iPD1) \times 315k\Omega$$

Tracking Error Amplifier

Each signal current from the photodiodes E and F is I-V converted and input to Pins 7 and 8 via a resistor which determines the gain. The signal is amplified by the gain amplifier, operated by the tracking error amplifier and then the (F-E) signal is output to Pin 11.



The balance adjustment is performed by varying the combined resistance value of the feedback resistors, which are T type-configured at the E I-V amplifier, by using the external resistance value of EI pin.

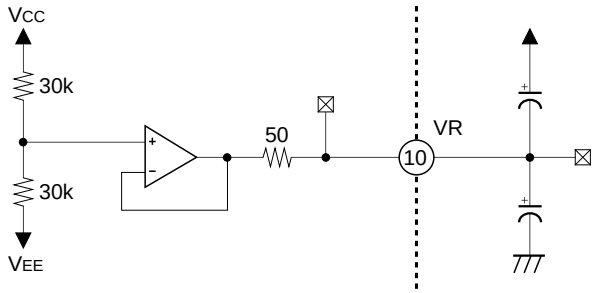
$$\text{F I-V amplifier feedback resistance value} = R_{F1} + R_{F2} + \frac{R_{F1} \times R_{F2}}{R_{F3}} = 403k\Omega$$

$$\text{E I-V amplifier feedback resistance value} = (R_{E1} \,//\, R_1) + R_{E2} + \frac{(R_{E1} \,//\, R_1) \times R_{E2}}{(R_{E3} \,//\, R_2)}$$

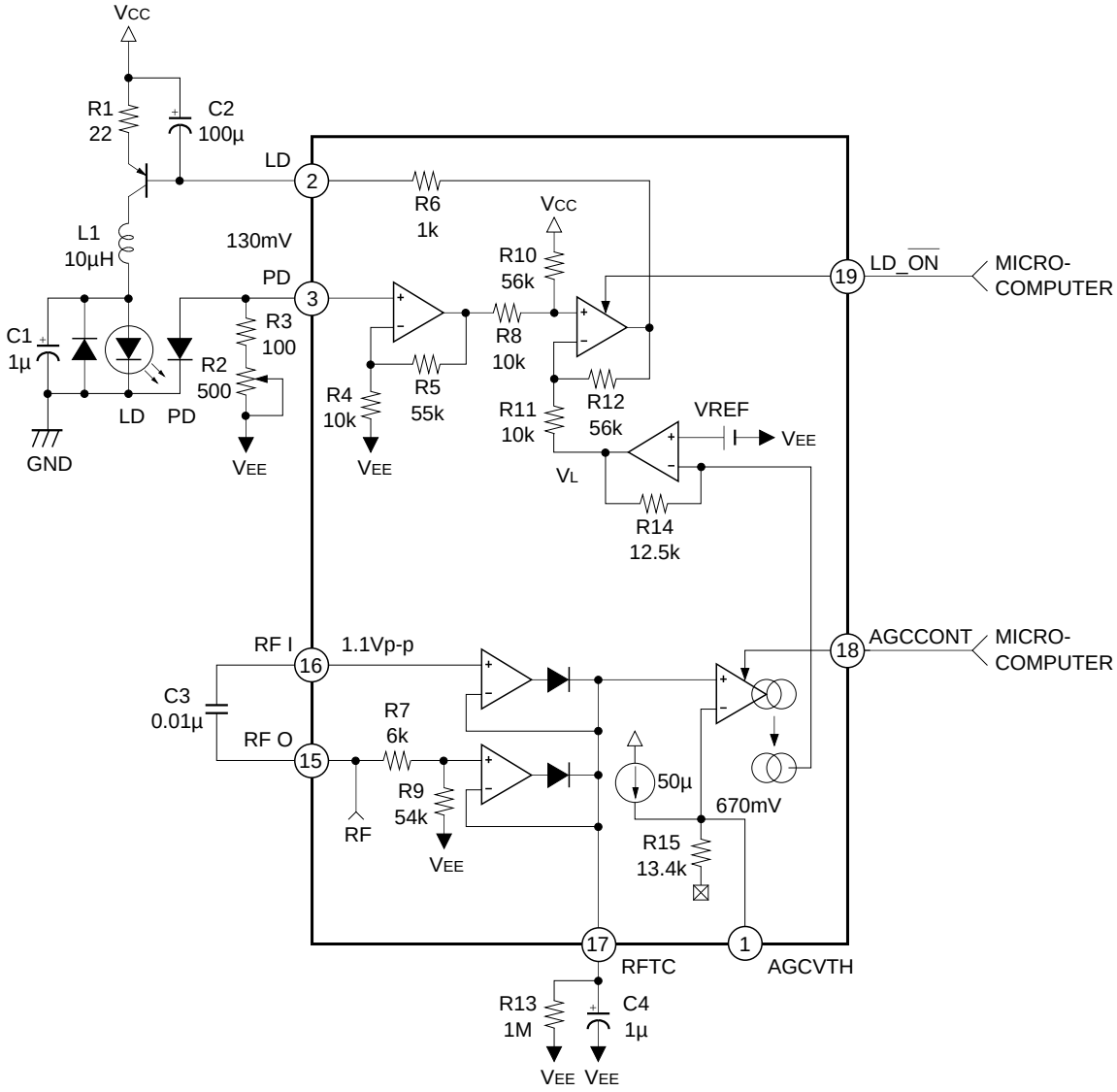
Leave EI pin open when the balance adjustment is not executed in this IC.
The gain for F I-V and E I-V amplifiers becomes the same when EI pin is left open.

Center Voltage Generation Circuit

This circuit provides the center potential when this IC is used at single power supply. The maximum current is approximately ±3mA. The output impedance is approximately 50Ω.



APC & Laser Power Control



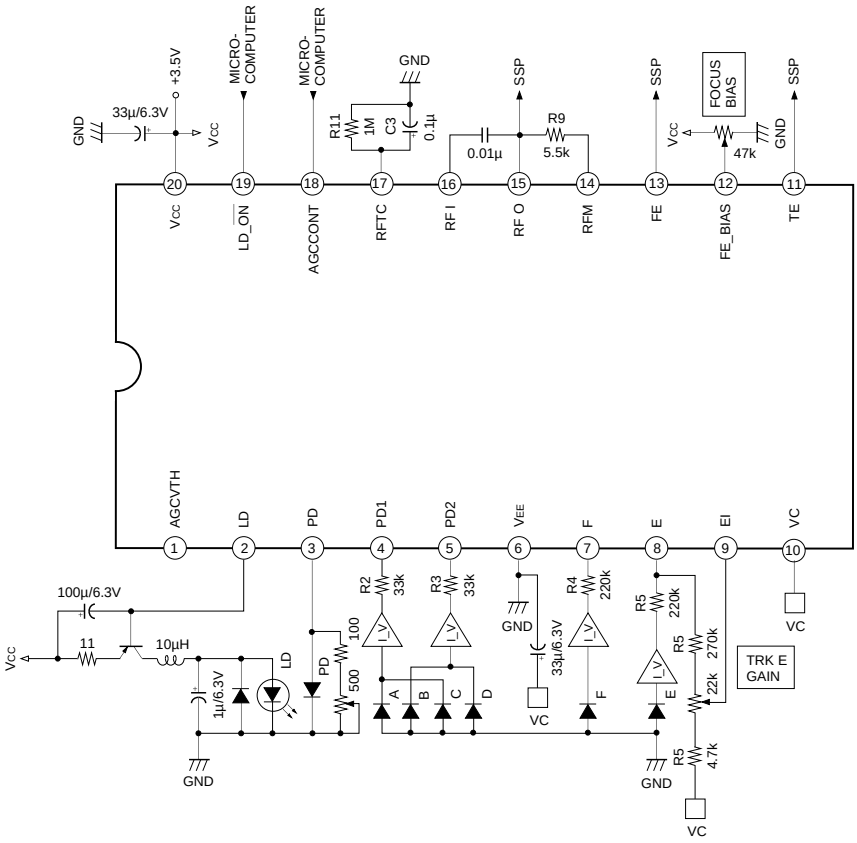
• APC

When the laser diode is driven by a constant current, the optical power output has extremely large negative temperature characteristics. The APC circuit is used to maintain the optical power output at a constant level. The laser diode current is controlled according to the monitor photo diode output.

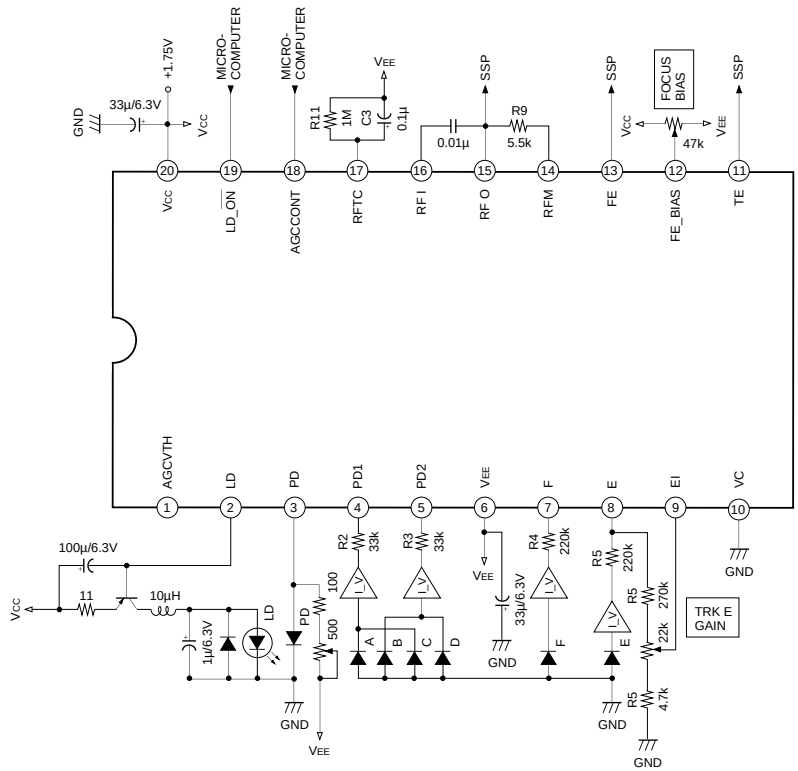
APC is set to ON by connecting the LD_$\overline{ON}$ pin to V_{CC}; OFF by connecting it to V_{CC}.

Application Circuit

• For single power supply +3.5V



• For dual power supply ±1.75V



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

• LASER POWER CONTROL (LPC)

The RF level is stabilized by attaching an offset to the APC V_L and controlling the laser power in sync with the RF level fluctuations.

The RF O and RF I levels are compared and the larger of the two is smoothed by the RFTC's external CR.

This signal is then compared with the reference level.

The laser power is controlled by attaching an offset to V_L according to the results of comparison with the reference level.

Set the reference level to 670mV. (center voltage reference)

When the reference level is changed, connect the external resistor to the AGCVTH pin (Pin 1). The reference level can be lowered by connecting the resistor between Pin 1 and the center output voltage or between Pin 20 and V_{CC}.

The AGCCONT pin (pin 18) is used to switch the level of the laser power control circuit; OFF, ON (laser power limit of 30%) and ON (laser power limit of 50%)

Note) For the laser power limit, 50% is recommended for PD IC; 30% for LC.

AGCCONT	LPC	LPC limit	V_L variable range
H (V_{CC})	OFF	—	Approximately 1.27V
M (VC or OPEN)	ON	30%	Approximately 1.27V ± 350mV
L (V_{EE})	ON	50%	Approximately 1.27V ± 570mV

Notes on Operation

1. Power supply

The CXA2550M/N can be used either at dual power supply or single power supply. The table below shows the connection of power supply for each case.

	V_{CC}	V_{EE}	VC
Dual power supply	+power supply	–power supply	GND
Single power supply	Power supply	GND	OPEN

2. RF amplifier

In this circuit, the IC internal phase compensation value is set so as to support the voltage output-type pickup. Therefore, when the current output-type pickup is used, the capacitance of optical pickup and leads etc. are attached to PD1 and PD2 pins and oscillation may occur.

3. laser power control

The RF level is stabilized by attaching an offset to the APC V_L and controlling the laser power in sync with the RF level fluctuations. Therefore, use this circuit in the state where the focus servo is applied.

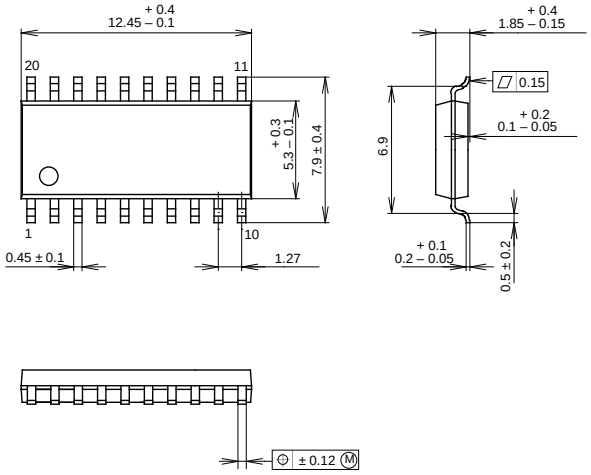
The laser life is shortened by increasing the laser power when the less light is reflected from the disc. It is recommended that the typical laser power value is set lower to maintain the laser life.

Take care of the laser maximum ratings when using the laser power control circuit.

Package Outline Unit: mm

CXA2550M

20PIN SOP (PLASTIC) 300mil



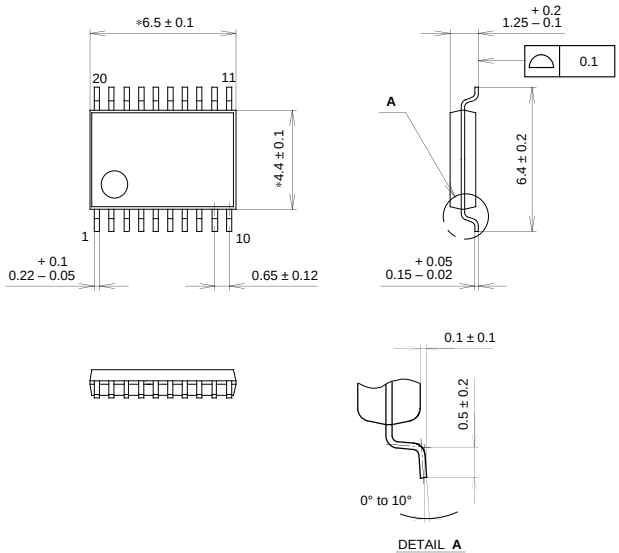
PACKAGE STRUCTURE

SONY CODE	SOP-20P-L01
EIAJ CODE	∗SOP020-P-0300-A
JEDEC CODE	————————

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE WEIGHT	0.3g

CXA2550N

20PIN SSOP (PLASTIC)



NOTE: Dimension "∗" does not include mold protrusion.

PACKAGE STRUCTURE

SONY CODE	SSOP-20P-L01
EIAJ CODE	SSOP020-P-0044
JEDEC CODE	————————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.1g

SONY

CXD3068Q

CD Digital Signal Processor with Built-in Digital Servo

Preliminary

Description

The CXD3068Q is a digital signal processor LSI for CD players. This LSI incorporates a digital servo.

Features

- All digital signal processings during playback are performed with a single chip
- Highly integrated mounting possible due to a built-in RAM

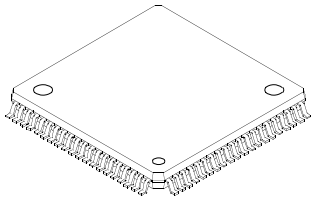
Digital Signal Processor (DSP) Block

- Playback mode supporting CAV (Constant Angular Velocity)
  - Frame jitter free
  - 0.5× to 4× continuous playback possible
  - Allows relative rotational velocity readout
- Wide capture range playback mode
  - Spindle rotational velocity following method
  - Supports 1× to 4× playback variable pitch playback
- Bit clock, which strobes the EFM signal, is generated by the digital PLL.
- EFM data demodulation
- Enhanced EFM frame sync signal protection
- Refined super strategy-based powerful error correction
  C1: double correction, C2: quadruple correction
  Supported during 4× playback
- Noise reduction during track jumps
- Auto zero-cross mute
- Subcode demodulation and Sub-Q data error detection
- Digital spindle servo
- 16-bit traverse counter
- Asymmetry correction circuit
- CPU interface on serial bus
- Error correction monitor signal, etc. output from a new CPU interface
- Servo auto sequencer
- Fine search performs track jumps with high accuracy
- Digital audio interface output
- Digital level meter, peak meter
- Bilingual supported
- VCO control mode
- CD TEXT data demodulation
- EFM playability reinforcement function

Digital Servo (DSSP) Block

- Microcomputer software-based flexible servo control
- Offset cancel function for servo error signal
- Auto gain control function for servo loop
- E:F balance, focus bias adjustment function
- Surf jump function supporting micro two-axis
- Tracking filter: 6 stages
  Focus filter: 5 stages

80 pin QFP (Plastic)



Structure

Silicon gate CMOS IC

Absolute Maximum Ratings

• Supply voltage	V_{DD}	–0.5 to +4.6	V
• Input voltage	V_I	–0.5 to +4.6	V
		(V_{SS} – 0.5V to V_{DD} + 0.5V)	
• Output voltage	V_O	–0.5 to +4.6	V
		(V_{SS} – 0.5V to V_{DD} + 0.5V)	
• Storage temperature	Tstg	–55 to +150	°C
• Supply voltage difference			
	V_{SS} – AV_{SS}	–0.3 to +0.3	V
	V_{DD} – AV_{DD}	–0.3 to +0.3	V

Note) AV_{DD} includes XV_{DD} and AV_{SS} includes XV_{SS}.

Recommended Operating Conditions

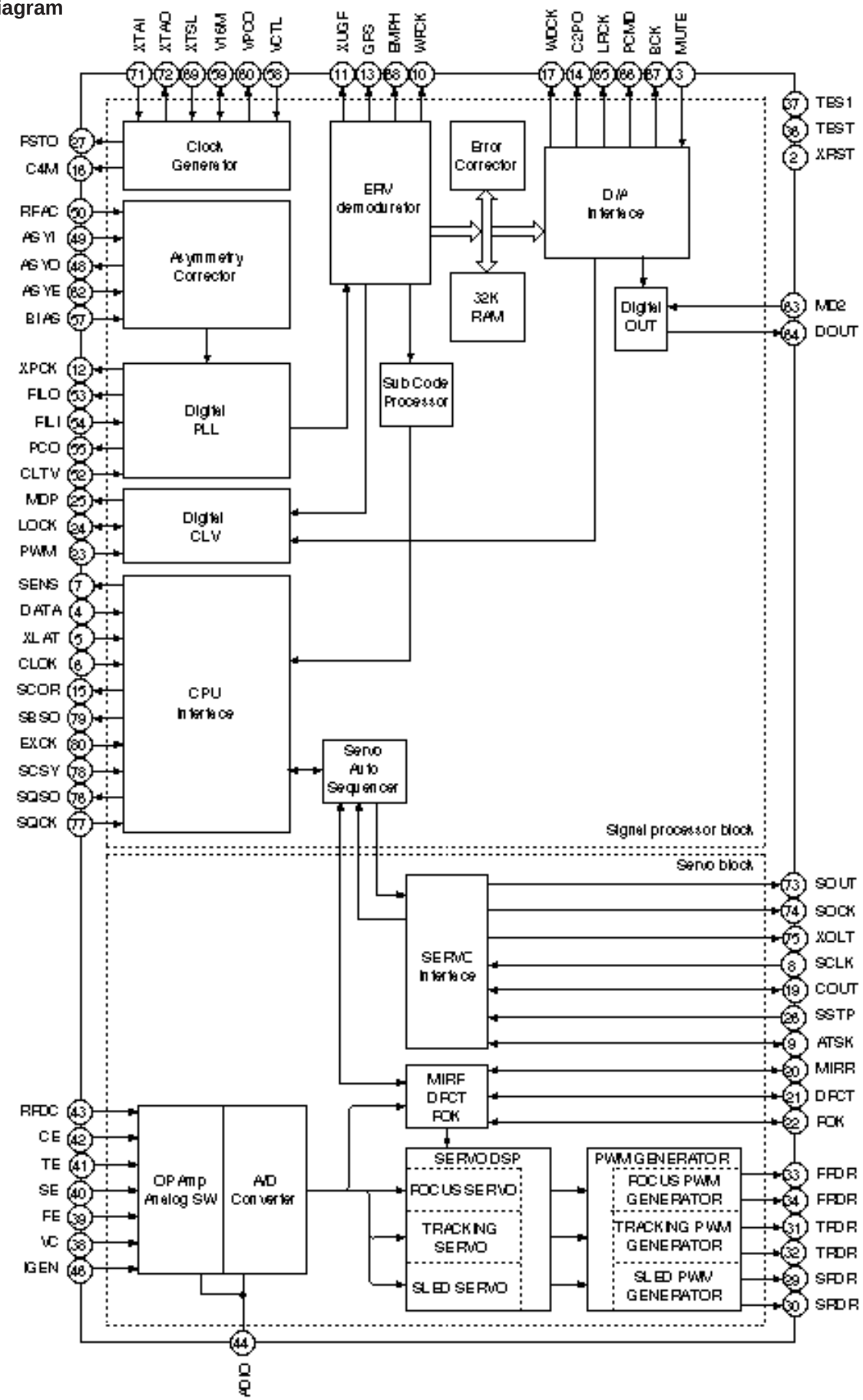
• Supply voltage	V_{DD}	2.7 to 3.6	V
• Operating temperature			
	Topr	–20 to +75	°C

I/O Capacitance

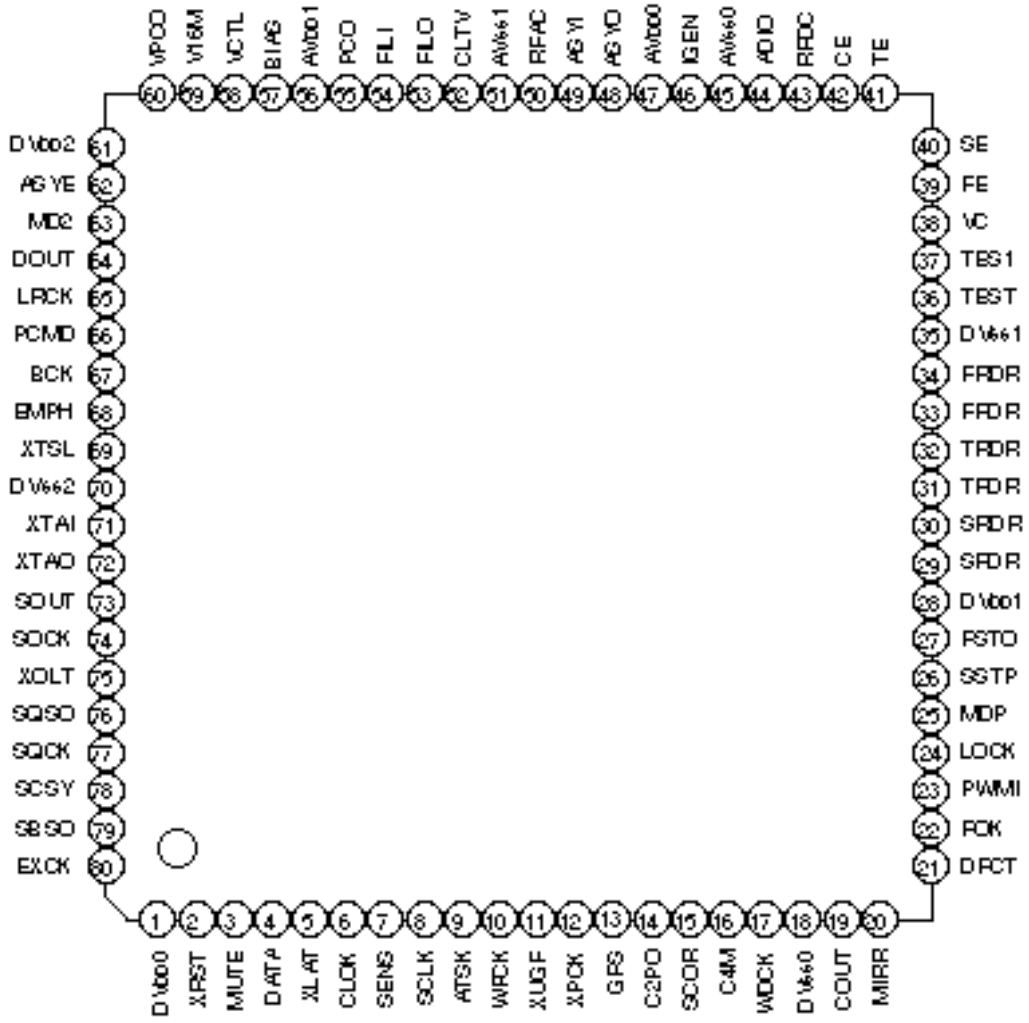
• Input pin	C_I	9 (Max.)	pF
• Output pin	C_O	11 (Max.)	pF
• I/O pin	$C_{I/O}$	11 (Max.)	pF

Note) Measurement conditions $V_{DD} = V_I = 0V$, f_M = 1MHz

Block Diagram



Pin Configuration



Pin Description

Pin No.	Symbol	I/O		Description
1	$DV_{DD}0$	—		Digital power supply.
2	XRST	I		System reset. Reset when low.
3	MUTE	I		Mute input (low: off, high: on)
4	DATA	I		Serial data input from CPU.
5	XLAT	I		Latch input from CPU. Serial data is latched at the falling edge.
6	CLOK	I		Serial data transfer clock input from CPU.
7	SENS	O	1, 0	SENS output to CPU.
8	SCLK	I		SENS serial data readout clock input.
9	ATSK	I/O	1, 0	Anti-shock input/output.
10	WFCK	O	1, 0	WFCK output.
11	XUGF	O	1, 0	XUGF output. MNT0 or RFCK is output by switching with the command.
12	XPCK	O	1, 0	XPCK output. MNT1 is output by switching with the command.
13	GFS	O	1, 0	GFS output. MNT2 or XROF is output by switching with the command.
14	C2PO	O	1, 0	G2PO output. MNT3 or GTOP is output by switching with the command.
15	SCOR	O	1, 0	Outputs a high signal when either subcode sync S0 or S1 is detected.
16	C4M	O	1, 0	4.2336MHz output. 1/4 frequency division output for V16M in CAV-W mode or variable pitch mode.
17	WDCK	O	1, 0	Word clock output. f = 2Fs. GRSCOR is output by the command switching.
18	$DV_{SS}0$	—	—	Digital GND.
19	COUT	I/O	1, 0	Track count signal I/O.
20	MIRR	I/O	1, 0	Mirror signal I/O.
21	DFCT	I/O	1, 0	Detect signal I/O.
22	FOK	I/O	1, 0	Focus OK signal I/O.
23	PWMI	I		Spindle motor external control input.
24	LOCK	I/O	1, 0	GFS is sampled at 460Hz; when GFS is high, this pin outputs a high signal. If GFS is low eight consecutive samples, this pin outputs low. Input when LKIN = 1.
25	MDP	O	1, Z, 0	Spindle motor servo control output.
26	SSTP	I		Disc innermost track detection signal input.
27	FSTO	O	1, 0	2/3 frequency division output for XTAI pin.
28	$DV_{DD}1$	—	—	Digital power supply.
29	SFDR	O	1, 0	Sled drive output.
30	SRDR	O	1, 0	Sled drive output.
31	TFDR	O	1, 0	Tracking drive output.
32	TRDR	O	1, 0	Tracking drive output.
33	FFDR	O	1, 0	Focus drive output.

Pin No.	Symbol	I/O		Description
34	FRDR	O	1, 0	Focus drive output.
35	$DV_{SS}1$	—	—	Digital GND.
36	TEST	I		Test. Normally, GND.
37	TES1	I		Test. Normally, GND.
38	VC	I		Center voltage input.
39	FE	I		Focus error signal input.
40	SE	I		Sled error signal input.
41	TE	I		Tracking error signal input.
42	CE	I		Center servo analog input.
43	RFDC	I		RF signal input.
44	ADIO	O	Analog	Test. No connected.
45	$AV_{SS}0$	—	—	Analog GND.
46	IGEN	I		Constant current input for operational amplifier.
47	$AV_{DD}0$	—	—	Analog power supply.
48	ASYO	O	1, 0	EFM full-swing output. (low = Vss, high = V_{DD})
49	ASYI	I		Asymmetry comparator voltage input.
50	RFAC	I		EFM signal input.
51	$AV_{SS}1$	—	—	Analog GND.
52	CLTV	I		Multiplier VCO1 control voltage input.
53	FILO	O	Analog	Master PLL filter output (slave = digital PLL).
54	FILI	I		Master PLL filter input.
55	PCO	O	1, Z, 0	Master PLL charge pump output.
56	$AV_{DD}1$	—	—	Analog power supply.
57	BIAS	I		Asymmetry circuit constant current input.
58	VCTL	I		Wide-band EFM PLL VCO2 control voltage input.
59	V16M	I/O	1, 0	Wide-band EFM PLL VCO2 oscillation output. Serves as wide-band EFM PLL clock input by switching with the command.
60	VPCO	O	1, Z, 0	Wide-band EFM PLL charge pump output.
61	$DV_{DD}2$	—	—	Digital power supply.
62	ASYE	I		Asymmetry circuit on/off (low = off, high = on).
63	MD2	I		Digital Out on/off control (low = off, high = on).
64	DOUT	O	1, 0	Digital Out output.
65	LRCK	O	1, 0	D/A interface. LR clock output. f = Fs
66	PCMD	O	1, 0	D/A interface. Serial data output (two's complement, MSB first).
67	BCK	O	1, 0	D/A interface. Bit clock output.

Pin No.	Symbol	I/O		Description
68	EMPH	O	1, 0	Outputs a high signal when the playback disc has emphasis, and a low signal when there is no emphasis.
69	XTSL	I		Crystal selection input. Low when the crystal is 16.9344MHz; high when it is 33.8688MHz.
70	$DV_{SS}2$	—	—	Digital GND.
71	XTAI	I		Crystal oscillation circuit input. When the master clock is input externally, input it from this pin.
72	XTAO	O		Crystal oscillation circuit output.
73	SOUT	O	1, 0	Serial data output in servo block.
74	SOCK	O	1, 0	Serial data readout clock output in servo block.
75	XOLT	O	1, 0	Serial data latch output in servo block.
76	SQSO	O	1, 0	Sub-Q 80-bit, PCM peak or level data outputs. CD TEXT data output.
77	SQCK	I		SQSO readout clock input.
78	SCSY	I		GRSCOR resynchronization input.
79	SBSO	O	1, 0	Sub-Q P to W serial output.
80	EXCK	I		SBSO readout clock input.

Notes)

- PCMD is a MSB first, two's complement output.
- GTOP is used to monitor the frame sync protection status. (High: sync protection window released.)
- XUGF is the frame sync obtained from the EFM signal, and is negative pulse. It is the signal before sync protection.
- XPCK is the inverse of the EFM PLL clock. The PLL is designed so that the falling edge and the EFM signal transition point coincide.
- The GFS signal goes high when the frame sync and the insertion protection timing match.
- RFCK is derived from the crystal accuracy, and has a cycle of 136µs. (during normal speed)
- C2PO represents the data error status.
- XROF is generated when the 32K RAM exceeds the ±28F jitter margin.

Combination of Monitor Pin Outputs

Command bit		Output data			
MTSL1	MTSL0				
0	0	XUGF	XPCK	GFS	C2PO
0	1	MNT0	MNT1	MNT2	MNT3
1	0	RFCK	XPCK	XROF	GTOP

Electrical Characteristics

1. DC Characteristics

(V_{DD} = AV_{DD} = 3.3 ± 0.3V, Vss = AVss = 0V, Topr = –20 to +75°C)

Item			Conditions	Min.	Typ.	Max.	Unit	Applicable pins
Input voltage (1)	High level	V_{IH1}		0.7V_{DD}			V	*1, *9
	Low level	V_{IL1}				0.2V_{DD}	V	
Input voltage (2)	High level	V_{IH2}	$V_I \leq 5.5V$	0.8V_{DD}			V	*2
	Low level	V_{IL2}				0.2V_{DD}	V	
Input voltage (3)	High level	V_{IH3}	$V_I \leq 5.5V$ Schmitt input	0.8V_{DD}			V	*3
	Low level	V_{IL3}				0.2V_{DD}	V	
Input voltage (4)		V_{IN4}	Analog input	V_{SS}		V_{DD}	V	*4, *5
Output voltage (1)	High level	V_{OH1}	I_{OH} = –4mA I_{OL} = 4mA	V_{DD} – 0.4		V_{DD}	V	*6, *8, *9
	Low level	V_{OL1}		0		0.4	V	
Output voltage (2)	High level	V_{OH2}	I_{OH} = –0.28mA I_{OH} = 0.36mA	V_{DD} – 0.5		V_{DD}	V	*7
	Low level	V_{OL2}		0		0.4	V	
Input leak current (1)		I_{LI1}	V_I = Vss or V_{DD}	–10		10	µA	*1, *4
Input leak current (2)		I_{LI2}	V_I = 0 to 5.5V	–10		10	µA	*2, *3
Input leak current (3)		I_{LI3}	V_I = Vss or V_{DD}	–40		40	µA	*9
Input leak current (4)		I_{LI4}	V_I = 0.25V_{DD} to 0.75V_{DD}	–40		40	µA	*5
Tri-state pin output leak current		I_{LO}	V_I = Vss or V_{DD}	–40		40	µA	*8

1-1. Applicable pins and classification

*1 CMOS level input pins:
TEST, TES1
*2 CMOS level input pins:
MUTE, SCSY, PWMI, DATA, XLAT, SSTP, XTSL
*3 CMOS Schmitt input pins:
ASYE, EXCK, V16M, SQCK, XRST, CLOK, SCLK
*4 Analog input pins (1):
VCTL, ASYI, CLTV, FILI
*5 Analog input pins (2):
VC, FE, SE, TE, CE, RFDC
*6 Normal output pins (1):
V16M, SQSO, C4M, WDCK, FSTO, SOUT, SOCK, XOLT, FSTO, SQSO, WFCK, XUGF, XPCK, GFS, C2PO, SCOR, SFDR, SRDR, TFDR, TRDR, FRDR, ASYO, DOUT, LRCK, PCMD, BCK, EMPH
*7 Normal output pin (2):
FILO
*8 Tri-state output pins:
VPCO, SENS, MDP, FFDR, PCO
*9 Normal input/output pins:
ATSK, COUT, MIRR, DFCT, FOK, LOCK

Note) When the external pull-down resistors are connected to the pins *2 and *3, the resistance applied to these pins should be 5kΩ or less in total.

2. AC Characteristics

(1) XTAI pin

(a) When using self-excited oscillation

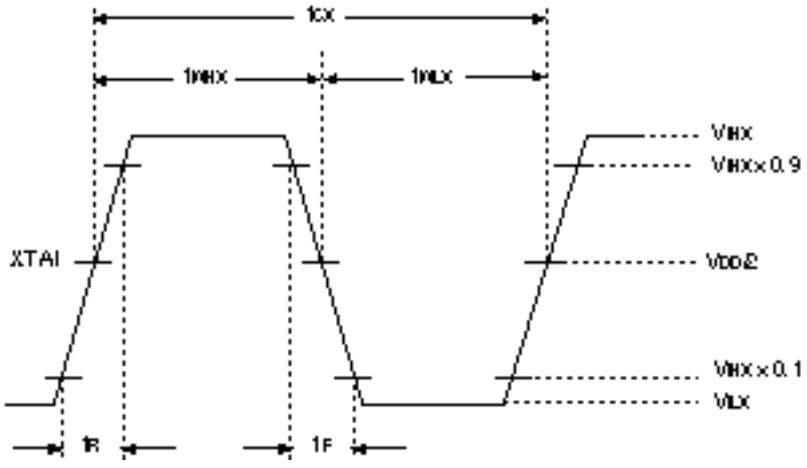
(Topr = –20 to +75°C, V_{DD} = AV_{DD} = 3.3 ± 0.3V)

Item	Symbol	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{MAX}	7		34	MHz

(b) When inputting pulses to XTAI pin

(Topr = –20 to +75°C, V_{DD} = AV_{DD} = 3.3 ± 0.3V)

Item	Symbol	Min.	Typ.	Max.	Unit
High level pulse width	t_{WHX}	13		500	ns
Low level pulse width	t_{WLX}	13		500	ns
Pulse cycle	t_{CX}	26		1000	ns
Input high level	V_{IHX}	V_{DD} – 1.0			V
Input low level	V_{ILX}			0.8	V
Rise time, fall time	t_R, t_F			10	ns



(c) When inputting sine waves to XTAI pin via a capacitor

(Topr = –20 to +75°C, V_{DD} = AV_{DD} = 3.3 ± 0.3V)

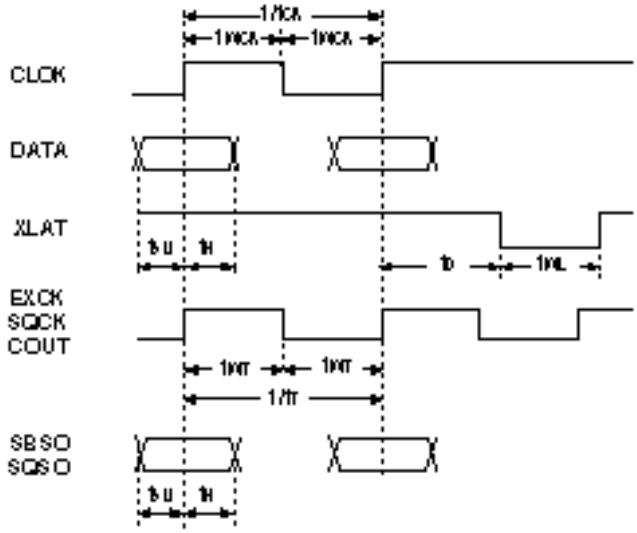
Item	Symbol	Min.	Typ.	Max.	Unit
Input amplitude	V_I	2.0		V_{DD} + 0.3	Vp-p

(2) CLOK, DATA, XLAT, SQCK and EXCK pins

(V_{DD} = AV_{DD} = 3.3 ± 0.3V, V_{SS} = AV_{SS} = 0V, Topr = –20 to +75°C)

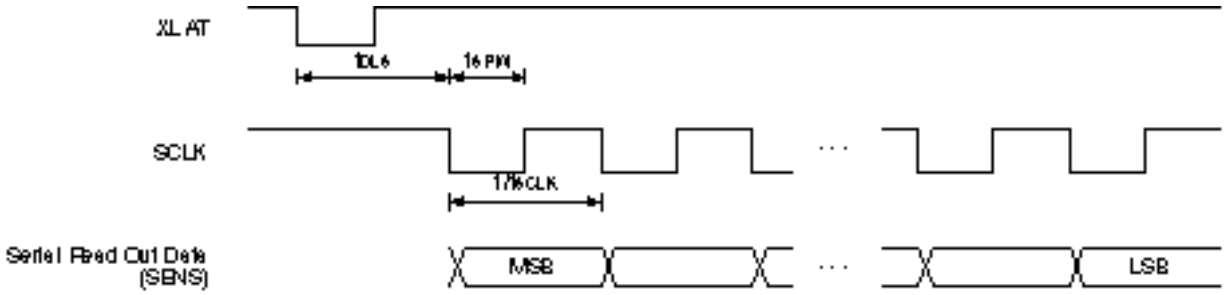
Item	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	f_{CK}			0.65	MHz
Clock pulse width	t_{WCK}	750			ns
Setup time	t_{SU}	300			ns
Hold time	t_H	300			ns
Delay time	t_D	300			ns
Latch pulse width	t_{WL}	750			ns
EXCK SQCK frequency	f_T			0.65 **Note)**	MHz
EXCK SQCK pulse width	t_{WT}	750 **Note)**			ns
COUT frequency (for input) *	f_T			65	kHz
COUT pulse width (for input) *	t_{WT}	7.5			µs

* Only when $44 and $45 are executed.



Note) In quasi double-speed playback mode, except when SQSO is Sub Q Read, the SQCK maximum operating frequency is 300kHz and its minimum pulse width is 1.5µs.

(3) SCLK pin



Item	Symbol	Min.	Typ.	Max.	Unit
SCLK frequency	f_{SCLK}			16	MHz
SCLK pulse width	t_{SPW}	31.3			ns
Delay time	t_{DLS}	15			µs

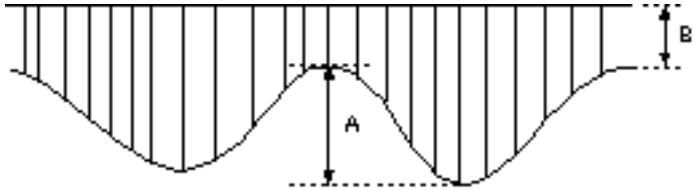
(4) COUT, MIRR and DFCT pins

Operating frequency (V_{DD} = AV_{DD} = 3.3 ± 0.3V, V_{SS} = AV_{SS} = 0V, Topr = –20 to +75°C)

Signal	Symbol	Min.	Typ.	Max.	Unit	Conditions
COUT maximum operating frequency	f_{COUT}	40			kHz	*1
MIRR maximum operating frequency	f_{MIRR}	40			kHz	*2
DFCT maximum operating frequency	f_{DFCTH}	5			kHz	*3

*1 When using a high-speed traverse TZC.

*2



When the RF signal continuously satisfies the following conditions during the above traverse.

- A = 0.11V_{DD} to 0.23V_{DD}
- $\frac{B}{A + B} \leq 25\%$

*3 During complete RF signal omission.
When settings related to DFCT signal generation are Typ.

Contents

Explanation of abbreviations

AVRG:	Average
AGCNTL:	Auto gain control
FCS:	Focus
TRK:	Tracking
SLD:	Sled
DFCT:	Defect

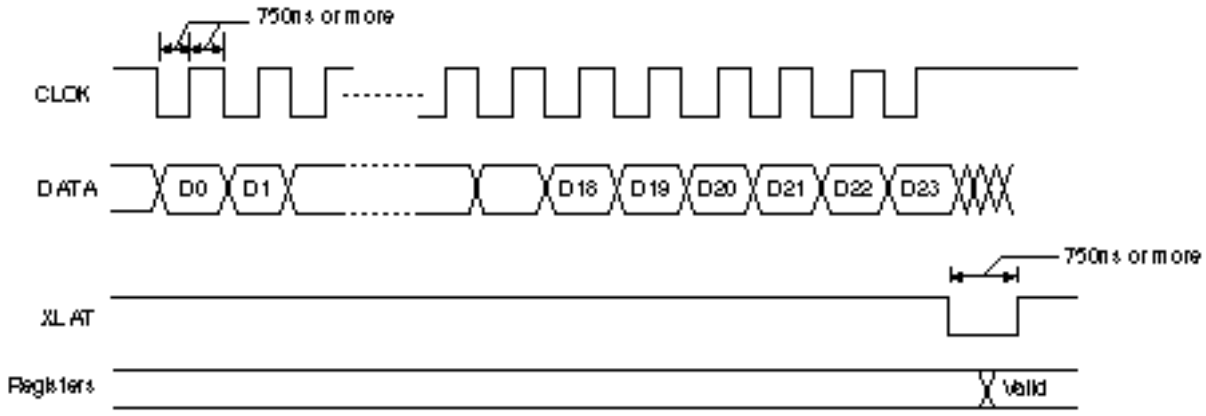
[1] CPU Interface

§ 1-1. CPU Interface Timing

• CPU interface

This interface uses DATA, CLOK and XLAT to set the modes.

The interface timing chart is shown below.



• The internal registers are initialized by a reset when XRST = 0.

Note) Be sure to set SQCK to high when XLAT is low.

§ 1-2. CPU Interface Command Table

Total bit length for each register

Register	Total bit length
0 to 2	8 bits
3	8 to 24 bits
4 to 6	16 bits
7	20 bits
8	28 bits
9	28 bits
A	28 bits
B	24 bits
C	28 bits
D	20 bits
E	20 bits

Command Table ($0X to 1X)

Register	Command	Address	Data 1				Data 2				Data 3				Data 4				Data 5				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
0	FOCUS CONTROL	0 0 0 0	1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FOCUS SERVO ON (FOCUS GAIN NORMAL)
			1	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FOCUS SERVO ON (FOCUS GAIN DOWN)
			0	—	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FOCUS SERVO OFF, 0V OUT
			0	—	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FOCUS SERVO OFF, FOCUS SEARCH VOLTAGE OUT
			0	—	1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FOCUS SEARCH VOLTAGE DOWN
			0	—	1	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FOCUS SEACH VOLTAGE UP
1	TRACKING CONTROL	0 0 0 1	1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ANTI SHOCK ON
			0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ANTI SHOCK OFF
			—	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BRAKE ON
			—	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BRAKE OFF
			—	—	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING GAIN NORMAL
			—	—	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING GAIN UP
			—	—	—	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING GAIN UP FILTER SELECT 1
			—	—	—	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING GAIN UP FILTER SELECT 2

—: Don't care

Command Table ($2X to 3X)

Register	Command	Address	Data 1				Data 2				Data 3				Data 4				Data 5				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
2	TRACKING MODE	0 0 1 0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING SERVO OFF
			0	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING SERVO ON
			1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FORWARD TRACK JUMP
			1	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	REVERSE TRACK JUMP
			—	—	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SLED SERVO OFF
			—	—	0	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SLED SERVO ON
			—	—	1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FORWARD SLED MOVE
			—	—	1	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	REVERSE SLED MOVE

Register	Command	Address		Data 1		Data 2				Data 3				Data 4				Data 5				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0 0 1 1	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SLED KICK LEVEL (±1 × basic value) (Default)
			0	0	0	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SLED KICK LEVEL (±2 × basic value)
			0	0	1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SLED KICK LEVEL (±3 × basic value)
			0	0	1	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SLED KICK LEVEL (±4 × basic value)

—: Don't care

Command Table ($340X)

Register	Command	Address 1	Address 2	Address 3	Address 4				Data 1				Data 2				
		D23 to D20	D19 to D16	D15 to D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0011	0100	0000	0	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K00) SLED INPUT GAIN
					0	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K01) SLED LOW BOOST FILTER A-H
					0	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K02) SLED LOW BOOST FILTER A-L
					0	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K03) SLED LOW BOOST FILTER B-H
					0	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K04) SLED LOW BOOST FILTER B-L
					0	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K05) SLED OUTPUT GAIN
					0	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K06) FOCUS INPUT GAIN
					0	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K07) SLED AUTO GAIN
					1	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K08) FOCUS HIGH CUT FILTER A
					1	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K09) FOCUS HIGH CUT FILTER B
					1	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K0A) FOCUS LOW BOOST FILTER A-H
					1	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K0B) FOCUS LOW BOOST FILTER A-L
					1	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K0C) FOCUS LOW BOOST FILTER B-H
					1	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K0D) FOCUS LOW BOOST FILTER B-L
					1	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K0E) FOCUS PHASE COMPENSATE FILTER A
					1	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K0F) FOCUS DEFECT HOLD GAIN

Command Table ($341X)

Register	Command	Address 1	Address 2	Address 3	Address 4				Data 1				Data 2				
		D23 to D20	D19 to D16	D15 to D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0011	0100	0001	0	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K10) FOCUS PHASE COMPENSATE FILTER B
					0	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K11) FOCUS OUTPUT GAIN
					0	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K12) ANTI SHOCK INPUT GAIN
					0	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K13) FOCUS AUTO GAIN
					0	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K14) HPTZC / AUTO GAIN HIGH PASS FILTER A
					0	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K15) HPTZC / AUTO GAIN HIGH PASS FILTER B
					0	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K16) ANTI SHOCK HIGH PASS FILTER A
					0	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K17) HPTZC / AUTO GAIN LOW PASS FILTER B
					1	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K18) FIX
					1	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K19) TRACKING INPUT GAIN
					1	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K1A) TRACKING HIGH CUT FILTER A
					1	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K1B) TRACKING HIGH CUT FILTER B
					1	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K1C) TRACKING LOW BOOST FILTER A-H
					1	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K1D) TRACKING LOW BOOST FILTER A-L
					1	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K1E) TRACKING LOW BOOST FILTER B-H
					1	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K1F) TRACKING LOW BOOST FILTER B-L

Command Table ($342X)

Register	Command	Address 1	Address 2	Address 3	Address 4				Data 1				Data 2				
		D23 to D20	D19 to D16	D15 to D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0011	0100	0010	0	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K20) TRACKING PHASE COMPENSATE FILTER A
					0	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K21) TRACKING PHASE COMPENSATE FILTER B
					0	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K22) TRACKING OUTPUT GAIN
					0	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K23) TRACKING AUTO GAIN
					0	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K24) FOCUS GAIN DOWN HIGH CUT FILTER A
					0	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K25) FOCUS GAIN DOWN HIGH CUT FILTER B
					0	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K26) FOCUS GAIN DOWN LOW BOOST FILTER A-H
					0	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K27) FOCUS GAIN DOWN LOW BOOST FILTER A-L
					1	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K28) FOCUS GAIN DOWN LOW BOOST FILTER B-H
					1	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K29) FOCUS GAIN DOWN LOW BOOST FILTER B-L
					1	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K2A) FOCUS GAIN DOWN PHASE COMPENSATE FILTER A
					1	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K2B) FOCUS GAIN DOWN DEFECT HOLD GAIN
					1	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K2C) FOCUS GAIN DOWN PHASE COMPENSATE FILTER B
					1	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K2D) FOCUS GAIN DOWN OUTPUT GAIN
					1	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K2E) NOT USED
					1	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K2F) NOT USED

Command Table ($343X)

Register	Command	Address 1	Address 2	Address 3	Address 4				Data 1				Data 2				
		D23 to D20	D19 to D16	D15 to D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0011	0100	0011	0	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K30) SLED INPUT GAIN (when TGup2 is accessed with SFSK = 1)
					0	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K31) ANTI SHOCK LOW PASS FILTER B
					0	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K32) NOT USED
					0	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K33) ANTI SHOCK HIGH PASS FILTER B-H
					0	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K34) ANTI SHOCK HIGH PASS FILTER B-L
					0	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K35) ANTI SHOCK FILTER COMPARATE GAIN
					0	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K36) TRACKING GAIN UP2 HIGH CUT FILTER A
					0	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K37) TRACKING GAIN UP2 HIGH CUT FILTER B
					1	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K38) TRACKING GAIN UP2 LOW BOOST FILTER A-H
					1	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K39) TRACKING GAIN UP2 LOW BOOST FILTER A-L
					1	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K3A) TRACKING GAIN UP2 LOW BOOST FILTER B-H
					1	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K3B) TRACKING GAIN UP2 LOW BOOST FILTER B-L
					1	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K3C) TRACKING GAIN UP PHASE COMPENSATE FILTER A
					1	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K3D) TRACKING GAIN UP PHASE COMPENSATE FILTER B
					1	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K3E) TRACKING GAIN UP OUTPUT GAIN
					1	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K3F) NOT USED

Command Table ($344X)

Register	Command	Address 1	Address 2	Address 3	Address 4				Data 1				Data 2				
		D23 to D20	D19 to D16	D15 to D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0011	0100	0100	0	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K40) TRACKING HOLD FILTER INPUT GAIN
					0	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K41) TRACKING HOLD FILTER A-H
					0	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K42) TRACKING HOLD FILTER A-L
					0	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K43) TRACKING HOLD FILTER B-H
					0	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K44) TRACKING HOLD FILTER B-L
					0	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K45) TRACKING HOLD FILTER OUTPUT GAIN
					0	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K46) TRACKING HOLD INPUT GAIN (when TGup2 is accessed with THSK = 1)
					0	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K47) NOT USED
					1	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K48) FOCUS HOLD FILTER INPUT GAIN
					1	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K49) FOCUS HOLD FILTER A-H
					1	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K4A) FOCUS HOLD FILTER A-L
					1	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K4B) FOCUS HOLD FILTER B-H
					1	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K4C) FOCUS HOLD FILTER B-L
					1	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K4D) FOCUS HOLD FILTER OUTPUT GAIN
					1	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K4E) NOT USED
					1	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K4F) NOT USED

Command Table ($348X to 34FX)

Register	Command	Address 1					Address 2				Data 1				Data 2				Data 3				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0 0 1 1	0	1	0	0	1	0	0	0	PGFS1	PGFS0	PFOK1	PFOK0	0	0	0	MRS	MRT1	MRT0	0	0	PGFS, PFOK, RFAC
							1	0	1	1	SFBK1	SFBK2	0	0	0	0	0	0	0	0	0	0	Booster Surf Brake
							1	1	0	0	THBON	FHBON	TLB1ON	FLB1ON	TLB2ON	0	HBST1	HBST0	LB1S1	LB1S0	LB2S1	LB2S0	Booster
							1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	
							1	1	1	0	IDFSL3	IDFSL2	IDFSL1	IDFSL0	0	0	IDFT1	IDFT0	0	0	0	0	

							Address 2						Data 1		Data 2				Data 3				
							D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0 0 1 1	0	1	0	0	1	1	1	1	1	0	FBL9	FBL8	FBL7	FBL6	FBL5	FBL4	FBL3	FBL2	FBL1	—	FCS Bias Limit
											0	1	FB9	FB8	FB7	FB6	FB5	FB4	FB3	FB2	FB1	—	FCS Bias Data
											0	0	TV9	TV8	TV7	TV6	TV5	TV4	TV3	TV2	TV1	TV0	Traverse Center Data

—: Don't care

Command Table ($35X to 3FX)

Register	Command	Address 1					Address 2				Data 1				Data 2				Data 3				
		D23～D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0011	1	1	1	1	1	0	0	0	SYG3	SYG2	SYG1	SYG0	FI FZB3	FI FZB2	FI FZB1	FI FZB0	FI FZA3	FI FZA2	FI FZA1	FI FZA0	System GAIN
		Address					Data 1				Data 2				Data 3				Data 4				
		D23～D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
		0011	0	1	0	1	FT1	FT0	FS5	FS4	FS3	FS2	FS1	FS0	FTZ	FG6	FG5	FG4	FG3	FG2	FG1	FG0	FCS search, AGF
			0	1	1	0	TDZC	DTZC	TJ5	TJ4	TJ3	TJ2	TJ1	TJ0	SFJP	TG6	TG5	TG4	TG3	TG2	TG1	TG0	TRK jump, AGT
			0	1	1	1	FZSH	FZSL	SM5	SM4	SM3	SM2	SM1	SM0	AGS	AGJ	AGGF	AGGT	AGV1	AGV2	AGHS	AGHT	FZC, AGC, SLD move
			1	0	0	0	VCLM	VCLC	FLM	FLC0	RFLM	RFLC	AGF	AGT	DFSW	LKSW	TBLM	TCLM	FLC1	TLC2	TLC1	TLC0	DC measure, cancel
			1	0	0	1	DAC	SD6	SD5	SD4	SD3	SD2	SD1	SD0	0	0	0	0	0	0	0	0	Serial data read out
		0011	1	0	1	0	0	FBON	FBSS	FBUP	FBV1	FBV0	FIFZC	TJD0	FPS1	FPS0	TPS1	TPS0	0	SJHD	INBK	MTI0	FCS Bias, Gain, Surf jump/brake
			1	0	1	1	SFO2	SFO1	SDF2	SDF1	MAX2	MAX1	SFOX	BTF	D2V2	D2V1	D1V2	D1V1	RINT	0	0	0	Mirr, DFCT, FOK
			1	1	0	0	COSS	COTS	CETZ	CETF	COT2	COT1	MOT2	0	BTS1	BTS0	MRC1	MRC0	0	0	0	0	TZC, Cout, Bottom, Mirr
			1	1	0	1	SFID	SFSK	THID	THSK	0	TLD2	TLD1	TLD0	0	0	0	0	0	0	0	0	SLD filter
			1	1	1	0	F1NM	F1DM	F3NM	F3DM	TINM	TIUM	T3NM	T3UM	DF1S	TLCD	0	LKIN	COIN	MDFI	MIRI	XT1D	Filter
			1	1	1	1	0	AGC4	XT4D	XT2D	0	DRR2	DRR1	DRR0	0	ASFG	FTQ	1	0	0	AGHF	ASOT	Clock, others

Note) Be sure to set D4 (Data2) of $3F to 1 for CXD3068Q.

Command Table ($4X to EX)

Register	Command	Address				Data1				Data2				Data3				Data4			
		D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
4	Auto sequence	0	1	0	0	AS3	AS2	AS1	AS0	MT3	MT2	MT1	MT0	LSSL	0	0	0	—	—	—	—
5	Blind (A, E), Brake (B), Overflow (C, G)	0	1	0	1	TR3	TR2	TR1	TR0	0	0	0	0	0	0	0	0	—	—	—	—
6	Sled KICK, BRAKE (D), KICK (F)	0	1	1	0	SD3	SD2	SD1	SD0	KF3	KF2	KF1	KF0	0	0	0	0	—	—	—	—
7	Auto sequence (N) track jump count setting	0	1	1	1	32768	16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1
8	MODE specification	1	0	0	0	CD-ROM	DOUT Mute	DOUT Mute-F	WSEL	VCO SEL1	ASHS	SOCT0	VCO SEL2	KSL3	KSL2	KSL1	KSL0	0	VCO1 CS0	XVCO2 THRU	0
9	Function specification	1	0	0	1	1	DSPB ON/OFF	ASEQ ON/OFF	1	BiliGL MAIN	BiliGL SUB	FLFC	1	0	0	0	0	1	0	0	1
A	Audio CTRL	1	0	1	0	0	0	Mute	ATT	PCT1	PCT2	0	SOC2	0	0	0	0	0	1	0	0
	EFM playability reinforcement setting					1	0	1	1	ARDTEN	1	1	1	1	0	1	0	0	0	1	0
	Sync expanding specification					1	1	0	0	AVW	0	SFP5	SFP4	SFP3	SFP2	SFP1	SFP0	—	—	—	—
	Sleep setting					1	1	0	1	ADCPS	DSP SLEEP	DSSP SLEEP	ASYM SLEEP	—	—	—	—	—	—	—	—
	Variable pitch					1	1	1	0	VARI ON	VARI USE	0	0	—	—	—	—	—	—	—	—
B	Traverse monitor counter setting	1	0	1	1	32768	16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1
C	Spindle servo coefficient setting	1	1	0	0	Gain MDP1	Gain MDP0	Gain MDS1	Gain MDS0	Gain DCLV1	Gain DCLV0	PCC1	PCC0	SFP3	SFP2	SFP1	SFP0	SRP3	SRP2	SRP1	SRP0
D	CLV CTRL	1	1	0	1	0	TB	TP	CLVS Gain	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0	VP CTL1	VP CTL0	0	0
E	SPD mode	1	1	1	0	CM3	CM2	CM1	CM0	EPWM	SPDC	ICAP	SFSL	VC2C	HIFC	LPWR	VPON	Gain CAV1	Gain CAV0	0	INV VPCO

— : Don't care

Command Table ($4X to EX) cont.

Register	Command	Address	Data 1	Data 2	Data 3	Data 4	Data 5				Data 6				Data 7			
							D7	D6	D5	D4	D3	D2	D1	D0	D3	D2	D1	D0
8	MODE specification	1 0 0 0					ERC4	SCOR SEL	SCSY	SOCT1	TXON	TXOUT	OUTL1	OUTL0	—	—	—	—
9	Function specification	1 0 0 1					0	0	0	0	0	0	0	0	—	—	—	—
A	Audio CTRL	1 0 1 0	0 0 * *				0	0	0	0	0	0	0	0	—	—	—	—
	EFM playability reinforcement setting		1 0 1 1				1	0	0	0	0	0	0	0	1	0	0	0
B	Traverse monitor counter setting	1 0 1 1					0	0	MTSL1	MTSL0	—	—	—	—	—	—	—	—
C	Spindle servo coefficient setting	1 1 0 0					EDC7	EDC6	EDC5	EDC4	EDC3	EDC2	EDC1	EDC0	—	—	—	—

—: Don't care

§ 1-3. CPU Command Presets

Command Preset Table ($0X to 34X)

Register	Command	Address	Data 1				Data 2				Data 3				Data 4				Data 5				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
0	FOCUS CONTROL	0 0 0 0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FOCUS SERVO OFF, 0V OUT
1	TRACKING CONTROL	0 0 0 1	0	0	0	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING GAIN UP FILTER SELECT 1
2	TRACKING MODE	0 0 1 0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING SERVO OFF SLED SERVO OFF
Register	Command	Address			Data 1		Data 2				Data 3				Data 4				Data 5				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D0	D0	
3	SELECT	0 0 1 1	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SLED KICK LEVEL (±1 × basic value) (Default)
		Address 1					Address 2				Address 3				Data 1				Data 2				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D0	D0	
		0 0 1 1	0	1	0	0	0	See "Coefficient ROM Preset Values Table".															KRAM DATA ($3400XX to $344fXX)

—: Don't care

Command Preset Table ($348X to 34FX)

Register	Command	Address 1					Address 2				Data 1				Data 2				Data 3				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0 0 1 1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PGFS, PFOK, RFAC
							1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	Booster Surf Brake
							1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Booster
							1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	
							1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	
							Address 2						Data 1		Data 2				Data 3				
							D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
							1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	FCS Bias Limit
											0	1	0	0	0	0	0	0	0	0	0	0	FCS Bias Data
											0	0	0	0	0	0	0	0	0	0	0	0	Traverse Center Data

Command Preset Table ($35X to 3FX)

Reg-ister	Command	Address1					Address2				Data1				Data2				Data3				
		D23～D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
		0011	1	1	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	System GAIN
		Address					Data1				Data2				Data3				Data4				
		D23～D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0011	0	1	0	1	0	1	0	1	1	0	0	0	0	0	1	0	1	1	0	1	FCS search, AGF
			0	1	1	0	0	0	0	0	1	1	1	0	0	0	1	0	1	1	1	0	TRK jump, AGT
			0	1	1	1	0	1	0	1	0	0	0	0	1	0	1	1	1	0	1	0	FZC, AGC, SLD move
			1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DC measure, cancel
			1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Serial data read out
			1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FCS Bias, Gain, Surf jump/brake
			1	0	1	1	1	1	1	0	0	0	0	0	0	1	0	1	0	0	0	0	Mirr, DFCT, FOK
			1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	TZC, Cout, Bottom, Mirr
			1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SLD filter
			1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Filter
			1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Clock, others

Command Preset Table ($4X to EX)

Register	Command	Address				Data1				Data2				Data3				Data4			
		D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
4	Auto sequence	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	—	—	—	—
5	Blind (A, E), Brake (B), Overflow (C, G)	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	—	—	—	—
6	Sled KICK, BRAKE (D), KICK (F)	0	1	1	0	0	1	1	1	0	0	0	0	0	0	0	0	—	—	—	—
7	Auto sequence(N) track jump count setting	0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
8	MODE specification	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9	Function specification	1	0	0	1	1	0	0	1	0	0	0	1	0	0	0	0	1	0	0	1
A	Audio CTRL	1	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0
	EFM playability reinforcement setting					1	0	1	1	0	1	1	1	1	0	1	0	0	0	1	0
	Sync expanding specification					1	1	0	0	0	0	0	0	1	1	0	0	—	—	—	—
	Sleep setting					1	1	0	1	0	0	0	0	—	—	—	—	—	—	—	—
	Variable pitch					1	1	1	0	0	0	0	0	—	—	—	—	—	—	—	—
B	Traverse monitor counter setting	1	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
C	Spindle servo coefficient setting	1	1	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1
D	CLV CTRL	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
E	SPD mode	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

— : Don't care

Command Preset Table ($4X to EX)

Register	Command	Address	Data 1	Data 2	Data 3	Data 4	Data 5				Data 6				Data 7			
							D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
8	MODE specification	1 0 0 0					0	0	0	0	0	0	0	0	—	—	—	—
9	Function specification	1 0 0 1					0	0	0	0	0	0	0	0	—	—	—	—
A	Audio CTRL	1 0 1 0	0 0 * *				0	0	0	0	0	0	0	0	—	—	—	—
	EFM playability reinforcement setting		1 0 1 1				0	0	0	0	0	0	0	0	0	0	0	0
B	Traverse monitor counter setting	1 0 1 1					0	0	0	0	—	—	—	—	—	—	—	—
C	Spindle servo coefficient setting	1 1 0 0					0	0	0	0	0	0	0	0	—	—	—	—

—: Don't care

<Coefficient ROM Preset Values Table (1)>

ADDRESS	DATA	CONTENTS
K00	E0	SLED INPUT GAIN
K01	81	SLED LOW BOOST FILTER A-H
K02	23	SLED LOW BOOST FILTER A-L
K03	7F	SLED LOW BOOST FILTER B-H
K04	6A	SLED LOW BOOST FILTER B-L
K05	10	SLED OUTPUT GAIN
K06	14	FOCUS INPUT GAIN
K07	30	SLED AUTO GAIN
K08	7F	FOCUS HIGH CUT FILTER A
K09	46	FOCUS HIGH CUT FILTER B
K0A	81	FOCUS LOW BOOST FILTER A-H
K0B	1C	FOCUS LOW BOOST FILTER A-L
K0C	7F	FOCUS LOW BOOST FILTER B-H
K0D	58	FOCUS LOW BOOST FILTER B-L
K0E	82	FOCUS PHASE COMPENSATE FILTER A
K0F	7F	FOCUS DEFECT HOLD GAIN
K10	4E	FOCUS PHASE COMPENSATE FILTER B
K11	32	FOCUS OUTPUT GAIN
K12	20	ANTI SHOCK INPUT GAIN
K13	30	FOCUS AUTO GAIN
K14	80	HPTZC / Auto Gain HIGH PASS FILTER A
K15	77	HPTZC / Auto Gain HIGH PASS FILTER B
K16	80	ANTI SHOCK HIGH PASS FILTER A
K17	77	HPTZC / Auto Gain LOW PASS FILTER B
K18	00	Fix*
K19	F1	TRACKING INPUT GAIN
K1A	7F	TRACKING HIGH CUT FILTER A
K1B	3B	TRACKING HIGH CUT FILTER B
K1C	81	TRACKING LOW BOOST FILTER A-H
K1D	44	TRACKING LOW BOOST FILTER A-L
K1E	7F	TRACKING LOW BOOST FILTER B-H
K1F	5E	TRACKING LOW BOOST FILTER B-L
K20	82	TRACKING PHASE COMPENSATE FILTER A
K21	44	TRACKING PHASE COMPENSATE FILTER B
K22	18	TRACKING OUTPUT GAIN
K23	30	TRACKING AUTO GAIN
K24	7F	FOCUS GAIN DOWN HIGH CUT FILTER A
K25	46	FOCUS GAIN DOWN HIGH CUT FILTER B
K26	81	FOCUS GAIN DOWN LOW BOOST FILTER A-H
K27	3A	FOCUS GAIN DOWN LOW BOOST FILTER A-L
K28	7F	FOCUS GAIN DOWN LOW BOOST FILTER B-H
K29	66	FOCUS GAIN DOWN LOW BOOST FILTER B-L
K2A	82	FOCUS GAIN DOWN PHASE COMPENSATE FILTER A
K2B	44	FOCUS GAIN DOWN DEFECT HOLD GAIN
K2C	4E	FOCUS GAIN DOWN PHASE COMPENSATE FILTER B
K2D	1B	FOCUS GAIN DOWN OUTPUT GAIN
K2E	00	NOT USED
K2F	00	NOT USED

* Fix indicates that normal preset values should be used.

<Coefficient ROM Preset Values Table (2)>

ADDRESS	DATA	CONTENTS
K30	80	SLED INPUT GAIN (Only when TRK Gain Up2 is accessed with SFSK = 1.)
K31	66	ANTI SHOCK LOW PASS FILTER B
K32	00	NOT USED
K33	7F	ANTI SHOCK HIGH PASS FILTER B-H
K34	6E	ANTI SHOCK HIGH PASS FILTER B-L
K35	20	ANTI SHOCK FILTER COMPARATE GAIN
K36	7F	TRACKING GAIN UP2 HIGH CUT FILTER A
K37	3B	TRACKING GAIN UP2 HIGH CUT FILTER B
K38	80	TRACKING GAIN UP2 LOW BOOST FILTER A-H
K39	44	TRACKING GAIN UP2 LOW BOOST FILTER A-L
K3A	7F	TRACKING GAIN UP2 LOW BOOST FILTER B-H
K3B	77	TRACKING GAIN UP2 LOW BOOST FILTER B-L
K3C	86	TRACKING GAIN UP PHASE COMPENSATE FILTER A
K3D	0D	TRACKING GAIN UP PHASE COMPENSATE FILTER B
K3E	57	TRACKING GAIN UP OUTPUT GAIN
K3F	00	NOT USED
K40	04	TRACKING HOLD FILTER INPUT GAIN
K41	7F	TRACKING HOLD FILTER A-H
K42	7F	TRACKING HOLD FILTER A-L
K43	79	TRACKING HOLD FILTER B-H
K44	17	TRACKING HOLD FILTER B-L
K45	6D	TRACKING HOLD FILTER OUTPUT GAIN
K46	00	TRACKING HOLD FILTER INPUT GAIN (Only when TRK Gain Up2 is accessed with THSK = 1.)
K47	00	NOT USED
K48	02	FOCUS HOLD FILTER INPUT GAIN
K49	7F	FOCUS HOLD FILTER A-H
K4A	7F	FOCUS HOLD FILTER A-L
K4B	79	FOCUS HOLD FILTER B-H
K4C	17	FOCUS HOLD FILTER B-L
K4D	54	FOCUS HOLD FILTER OUTPUT GAIN
K4E	00	NOT USED
K4F	00	NOT USED

§ 1-4. Description of SENS Signals

SENS output

Microcomputer serial register (latching not required)	ASEQ = 0	ASEQ = 1	Output data length
$0X	Z	FZC	—
$1X	Z	AS (Anti Shock)	—
$2X	Z	TZC	—
$30 to 37	Z	SSTP	—
$38	Z	AGOK*	—
$38	Z	XAVEBSY*	—
$3904	Z	TE Avrg Reg.	9 bits
$3908	Z	FE Avrg Reg.	9 bits
$390C	Z	VC Avrg Reg.	9 bits
$391C	Z	TRVSC Reg.	9 bits
$391D	Z	FB Reg.	9 bits
$391F	Z	RFDC Avrg Reg.	8 bits
$3A	Z	FBIAS Count STOP	—
$3B to 3F	Z	SSTP	—
$4X	Z	XBUSY	—
$5X	Z	FOK	—
$6X	Z	0	—
$AX	GFS	GFS	—
$BX	COMP	COMP	—
$CX	COUT	COUT	—
$EX	$\overline{\text{OV64}}$	$\overline{\text{OV64}}$	—
$7X, 8X, 9X, DX, FX	Z	0	—

* $38 outputs AGOK during AGT and AGF command settings, and XAVEBSY during AVRG measurement. SSTP is output in all other cases.

Description of SENS Signals

SENS output	
Z	The SENS pin is high impedance.
XBUSY	Low while the auto sequencer is in operation, high when operation terminates.
FOK	Outputs the same signal as the FOK pin. High for "focus OK".
GFS	High when the regenerated frame sync is obtained with the correct timing.
COMP	Counts the number of tracks set with Reg.B. High when Reg.B is latched, low when the initial Reg.B number is counted through COUT.
COUT	Counts the number of tracks set with Reg.B. High when Reg.B is latched, toggles each time the Reg.B number is counted through COUT. While $44 and $45 are being executed, toggles with each COUT 8-count instead of the Reg.B number.
$\overline{\text{OV64}}$	Low when the EFM signal is lengthened by 64 channel clock pulses or more after passing through the sync detection filter.

The meaning of the data for each address is explained below.

$4X commands

Register name	Data 1				Data 2				Data 3			
4	Command				MAX timer value				Timer range			
	AS3	AS2	AS1	AS0	MT3	MT2	MT1	MT0	LSSL	0	0	0

Command	AS3	AS2	AS1	AS0
Cancel	0	0	0	0
Fine Search	0	1	0	RXF
Focus-On	0	1	1	1
1 Track Jump	1	0	0	RXF
10 Track Jump	1	0	1	RXF
2N Track Jump	1	1	0	RXF
M Track Move	1	1	1	RXF

RXF = 0 Forward

RXF = 1 Reverse

- When the Focus-on command ($47) is canceled, $02 is sent and the auto sequence is interrupted.
- When the Track jump commands ($44 to $45, $48 to $4D) are canceled, $25 is sent and the auto sequence is interrupted.

MAX timer value				Timer range			
MT3	MT2	MT1	MT0	LSSL	0	0	0
23.2ms	11.6ms	5.8ms	2.9ms	0	0	0	0
1.49s	0.74s	0.37s	0.18s	1	0	0	0

- To disable the MAX timer, set the MAX timer value to 0.

$5X commands

Timer	TR3	TR2	TR1	TR0
Blind (A, E), Overflow (C, G)	0.18ms	0.09ms	0.045ms	0.022ms
Brake (B)	0.36ms	0.18ms	0.09ms	0.045ms

$6X commands

Register name	Data 1				Data 2			
6	KICK (D)				KICK (F)			
	SD3	SD2	SD1	SD0	KF3	KF2	KF1	KF0

Timer	SD3	SD2	SD1	SD0
When executing KICK (D) $44 or $45	23.2ms	11.6ms	5.8ms	2.9ms
When executing KICK (D) $4C or $4D	11.6ms	5.8ms	2.9ms	1.45ms

Timer	KF3	KF2	KF1	KF0
KICK (F)	0.72ms	0.36ms	0.18ms	0.09ms

$7X commands

Auto sequencer track jump count setting

Command	Data 1				Data 2				Data 3				Data 4			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
Auto sequence track jump count setting	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

This command is used to set N when a 2N-track jump is executed, to set M when an M-track move is executed and to set the jump count when fine search is executed for auto sequencer.

- The maximum track count is 65,535, but note that with a 2N-track jump the maximum track jump count depends on the mechanical limitations of the optical system.
- When the track jump count is from 0 to 15, the COUT signal is counted for 2N-track jumps and M-track moves; when the count is 16 or over, the MIRR signal is counted. For fine search, the COUT signal is counted.

$8X commands

Command	Data 1				Data 2			
	D23	D22	D21	D20	D19	D18	D17	D16
MODE specification	CD-ROM	DOUT Mute	DOUT Mute-F	WSEL	VCO SEL1	ASHS	SOCT0	VCO SEL2

Command bit	C2PO timing	Processing
CDROM = 1	1-3	CDROM mode; average value interpolation and pre-value hold are not performed.
CDROM = 0	1-3	Audio mode; average value interpolation and pre-value hold are performed.

Command bit	Processing
DOUT Mute = 1	When Digital Out is on (MD2 pin = 1), DOUT output is muted.
DOUT Mute = 0	When Digital Out is on, DOUT output is not muted.

Command bit	Processing
D. out Mute F = 1	When Digital Out is on (MD2 pin = 1), DA output is muted.
D. out Mute F = 0	DA output mute is not affected when Digital Out is either on or off.

MD2	Other mute conditions*	DOUT Mute	D.out Mute F	DOUT output	DA output for 48-bit slot
0	0	0	0	OFF	0dB
0	0	0	1		
0	0	1	0		
0	0	1	1		
0	1	0	0		−∞dB
0	1	0	1		
0	1	1	0		
0	1	1	1		
1	0	0	0	0dB	0dB
1	0	0	1		−∞dB
1	0	1	0	−∞dB	0dB
1	0	1	1		−∞dB
1	1	0	0		
1	1	0	1		
1	1	1	0		
1	1	1	1		

* See mute conditions (1), (2), and (4) to (6) under $AX commands for other mute conditions.

Command bit	Sync protection window width	Application
WSEL = 1	±26 channel clock	Anti-rolling is enhanced.
WSEL = 0	±6 channel clock	Sync window protection is enhanced.

* In normal-speed playback, channel clock = 4.3218MHz.

Command bit	Function
ASHS = 0	The command transfer rate to DSSP block from auto sequencer is set to normal speed.
ASHS = 1	The command transfer rate to DSSP block from auto sequencer is set to half speed.

* See "§ 4-8. Playback Speed" for settings.

Command bit		Processing
SOCT0	SOCT1	
0	—	Sub-Q is output from the SQSO pin.
1	0	Each signal is output from the SQSO pin. Input the readout clock to SQCK. (See Timing Chart 2-4.)
1	1	The error rate is output from the SQSO pin. Input the readout clock to SQCK. (See Timing Chart 2-6.)

—: Don't care

Command	Data 2				Data 3			
	D3	D2	D1	D0	D3	D2	D1	D0
MODE specification	VCO SEL1	ASHS	SOCT0	VCO SEL2	KSL3	KSL2	KSL1	KSL0

See the previous page.

Command bit	Processing
VCOSEL1 = 0	Multiplier PLL VCO1 is set to normal speed.
VCOSEL1 = 1	Multiplier PLL VCO1 is set to approximately twice the normal speed.

Command bit		Processing
KSL3	KSL2	
0	0	Output of multiplier PLL VCO1 is 1/1 frequency-divided.
0	1	Output of multiplier PLL VCO1 is 1/2 frequency-divided.
1	0	Output of multiplier PLL VCO1 is 1/4 frequency-divided.
1	1	Output of multiplier PLL VCO1 is 1/8 frequency-divided.

Command bit	Processing
VCOSEL2 = 0	Wide-band PLL VCO2 is set to normal speed.
VCOSEL2 = 1	Wide-band PLL VCO2 is set to approximately twice the normal speed.

Command bit		Processing
KSL1	KSL0	
0	0	Output of wide-band PLL VCO2 is 1/1 frequency-divided.
0	1	Output of wide-band PLL VCO2 is 1/2 frequency-divided.
1	0	Output of wide-band PLL VCO2 is 1/4 frequency-divided.
1	1	Output of wide-band PLL VCO2 is 1/8 frequency-divided.

Command	Data 4				Data 5				Data 6			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
Mode specification	0	VCO1 CS0	VCO2 THRU	0	ERC4	SCOR SEL	SCSY	SOCT1	TXON	TXOUT	OUTL1	OUTL0

Command bit	Processing
VCO2 THRU = 0	V16M is output.
VCO2 THRU = 1	The wide-band EFM PLL clock can be input from the V16M pin.

* These bits select the internal or external connection for the VCO2 used in CAV-W or variable pitch mode.

Command bit	Processing
ERC4 = 0	C2 error double correction is performed when DSPB = 1.
ERC4 = 1	C2 error quadruple correction is performed even when DSPB = 1.

Command bit	Processing
SCOR SEL = 0	WDCK signal is output.
SCOR SEL = 1	GRSCOR (protected SCOR) is output.

* Used when outputting GRSCOR from the WDCK pin.

Command bit	Processing
SCSY = 0	No processing.
SCSY = 1	GRSCOR (protected SCOR) synchronization is applied again.

* Used to resynchronize GRSCOR.

The rising edge signal of this commnd bit is used internally. Therefore, when resynchronizing GRSCOR, first return the setting to 0 and then set to 1.
GRSCOR achieves the crystal accuracy by removing the jitter components included in the SCOR signal. This signal is synchronized with PCMDATA.
The resynchronization conditions are when GTOP = high or when the SCSY pin = high.
(same as when SCSY = 1 is sent by the $8X command.)

Command bit	Processing
TXON = 0	When CD TEXT data is not demodulated, set TXON to 0.
TXON = 1	When CD TEXT data is demodulated, set TXON to 1.

* See "$4-10. CD TEXT Data Demodulation"

Command bit	Processing
TXOUT = 0	Various signals except for CD TEXT is output from the SQSO pin.
TXOUT = 1	CD TEXT data is output from the SQSO pin.

* See "$4-10. CD TEXT Data Demodulation"

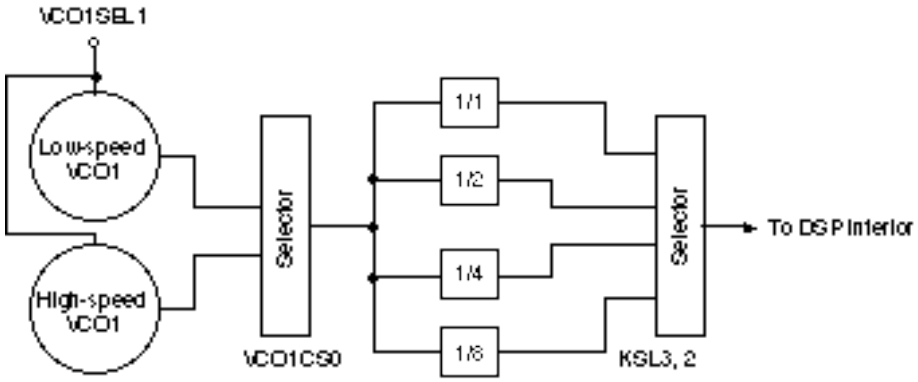
Command bit	Processing
OUTL1 = 0	WFCK, XPCK C4M, WDCK and FSTO are output. V16M is output when VCO2 THRU = 0.
OUTL1 = 1	WFCK, XPCK C4M, WDCK and FSTO outputs are set to low. The V16M output is low when VCO2 THRU = 0.

Command bit	Processing
OUTL0 = 0	PCMD, BCK, LRCK and EMPH are output.
OUTL0 = 1	PCMD, BCK, LRCK and EMPH outputs are low.

Command bit	Processing
VCO1CS0 = 0	Multiplier PLL VCO1 low speed is selected.
VCO1CS0 = 1	Multiplier PLL VCO1 high speed is selected.

* The CXD3068Q has two VCO1s, and this command selects one of these VCO1s.

* **Block Diagram of VCO Internal Path**



VCO1 Internal Path

$9X commands

Command	Data 1				Data 2			
	D23	D22	D21	D20	D19	D18	D17	D16
Function specification	1	DSPB ON-OFF	A.SEQ ON-OFF	1	BiliGL MAIN	BiliGL SUB	FLFC	1

Command bit	Processing
DSPB = 0	Normal-speed playback, C2 error quadruple correction.
DSPB = 1	Double-speed playback, C2 error double correction. (quadruple correction when ERC4 = 1)

FLFC is normally 0.

FLFC is 1 in CAV-W mode, for any playback speed.

Command bit	BiliGL MAIN = 0	BiliGL MAIN = 1
BiliGL SUB = 0	STEREO	MAIN
BiliGL SUB = 1	SUB	Mute

Definition of bilingual capable MAIN, SUB and STEREO

The left channel input is output to the left and right channels for MAIN.

The right channel input is output to the left and right channels for SUB.

The left and right channel inputs are output to the left and right channels for STEREO.

$AX commands

Command	Data 1				Data 2			
	D23	D22	D21	D20	D19	D18	D17	D16
Audio CTRL	VARI ON	VARI USE	Mute	ATT	PCT1	PCT2	0	SOC2

Command bit	Processing
VARION = 0	Variable pitch mode is turned off. (The crystal is the reference to the internal clock.)
VARION = 1	Variable pitch mode is turned on. (The VCO2 is the reference to the internal clock.)

Command bit	Processing
VARIUSE = 0	When the variable pitch mode is not used, set VARIUSE to 0 .
VARIUSE = 1	When the variable pitch mode is used, set VARIUSE to 1.

* See "$DX commands" for the variable range and the usage example of the variable pitch.

Command bit	Meaning
Mute = 0	Mute off if other mute conditions are not set.
Mute = 1	Mute on. Peak register reset.

Command bit	Meaning
ATT = 0	Attenuation off.
ATT = 1	–12dB

Mute conditions

(1) When register A mute = 1.
(2) When Mute pin = 1.
(3) When register 8 D.out Mute F = 1 and the Digital Out is on (MD2 pin = 1).
(4) When GFS stays low for over 35 ms (during normal-speed).
(5) When register 9 BiliGL MAIN = Sub = 1.
(6) When register A PCT1 = 1 and PCT2 = 0.

(1) to (4) perform zero-cross muting with a 1ms time limit.

Command bit		Meaning	PCM Gain	ECC error correction ability
PCT1	PCT2			
0	0	Normal mode	× 0dB	C1: double; C2: quadruple
0	1	Level meter mode	× 0dB	C1: double; C2: quadruple
1	0	Peak meter mode	Mute	C1: double; C2: double
1	1	Normal mode	× 0dB	C1: double; C2: double

Description of level meter mode (see Timing Chart 1-4.)

- When the LSI is set to this mode, it performs digital level meter functions.
- When the 96-bit clock is input to SQCK, 96 bits of data are output to SQSO.
  The initial 80 bits are Sub-Q data (see "§ 2. Subcode Interface"). The last 16 bits are LSB first, which are 15-bit PCM data (absolute values) and an L/R flag.
  The L/R flag is high when the 15-bit PCM data is from the left channel and low when the data is from the right channel.
- The PCM data is reset and the L/R flag is reversed after one readout.
  Then maximum value measuring continues until the next readout.

Description of peak meter mode (see Timing Chart 1-5.)

- When the LSI is set to this mode, the maximum PCM data value is detected regardless of if it comes from the left or right channel.
  The 96-bit clock must be input to SQCK to read out this data.
- When the 96-bit clock is input, 96 bits of data are output to SQSO and the value is set in the LSI internal register again.
  In other words, the PCM maximum value detection register is not reset by the readout.
- To reset the PCM maximum value register to zero, set PCT1 = PCT2 = 0 or set the $AX mute.
- The Sub-Q absolute time is automatically controlled in this mode.
  In other words, after the maximum value is generated, the absolute time for CRC to become OK is retained in the memory. Normal operation is conducted for the relative time.
- The final bit (L/R flag) of the 96-bit data is normally 0.
- The pre-value hold and average value interpolation data are fixed to level (–∞) for this mode.

Command bit	Processing
SOC2 = 0	The SENS signal is output from the SENS pin as usual.
SOC2 = 1	The SQSO pin signal is output from the SENS pin.

SENS output switching

- This command enables the SQSO pin signal to be output from the SENS pin.
  When SOC2 = 0, SENS output is performed as usual.
  When SOC2 = 1, the SQSO pin signal is output from the SENS pin.
  At this time, the readout clock is input to the SCLK pin.

Note) SOC2 should be switched when SQCK = SCLK = high.

$AB commands (preset: $AB7A28)

Command	Data 1				Data 2				Data 3				Data 4				Data 5			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
EFM playability reinforcement function	1	0	1	1	ARDTEN	1	1	1	1	0	1	0	0	0	1	0	1	0	0	0

Command	Data 6				Data 7			
	D3	D2	D1	D0	D3	D2	D1	D0
EFM playability reinforcement function	0	0	0	0	1	0	0	0

Command bit	Processing
ARDTEN = 0	Normal playback is performed.
ARDTEN = 1	EFM playability reinforcement function is turned on.

Note) Set these command bits when the disc is not played back.

$AC commands (preset: $AC0C)

Command	Data 1				Data 2				Data 3			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
Sync expanding bit	1	1	0	0	AVW	0	SFP5	SFP4	SFP3	SFP2	SFP1	SFP0

Command bit	Processing
AVW = 0	Automatic expanding function of sync protection window width is turned off.
AVW = 1	Automatic expanding function of sync protection window width is turned on.

* During the period from 16th forward protection to the GFS rise, the sync protection window width (±6 channel clocks when WSEL = 0 and ±26 channel clocks when WSEL = 1) expands by 32 channel clocks whenever the inserted sync is generated. GTOP rises when the window width becomes maximum (in excess of 588 channel clocks).

Note) The sync forward protection times are not affected by SFP5 to SFP0.

Command bit	Processing
SFP5 to 0	Sets the frame sync forward protection times. The setting range is 1F to 3F (Hex).

* See "§4-2. Frame Sync Protection" for the protection of the frame sync.

Note) This command bit register is shared with the $CX commands and the command bit set last is valid. When the command bit is used in the existing state, set to the $CX commands. When the command bit is used with the $AC address, make the settings same as for SFP3 to SFP0 set with the $CX commands.

$AD commands (preset: $AD0)

Command	Data 1				Data 2			
	D3	D2	D1	D0	D3	D2	D1	D0
AD (Sleep setting)	1	1	0	1	ADCPS	DSP SLEEP	DSSP SLEEP	ASYM SLEEP

ADCPS: This bit sets the operating mode of the DSSP block A/D converter.
When 0, the operating mode of the DSSP block A/D converter is set to normal. (default)
When 1, the operating mode of the DSSP block A/D converter is set to power saving.

DSP SLEEP: This bit sets the operating mode of the DSP block.
When 0, the DSP block operates normally. (default)
When 1, the DSP block clock is stopped. This makes it possible to reduce power consumption.

DSSP SLEEP: This bit sets the operating mode of the DSSP block.
When 0, the DSSP block operates normally. (default)
When 1, the DSSP block clock is stopped. In addition, the A/D converter and operational amplifier in the DSSP block are set to standby mode. This makes it possible to reduce power consumption.

ASYM SLEEP: This bit sets the operating mode of the asymmetry correction circuit and VCO1.
When 0, the asymmetry correction circuit and VCO1 operate normally. (default)
When 1, the operational amplifier in the asymmetry correction circuit is set to standby mode. In addition, the multiplier PLL VCO1 oscillation is stopped. This makes it possible to reduce power consumption.

$AE commands (preset: $AE0)

Command	Data 1				Data 2			
	D3	D2	D1	D0	D3	D2	D1	D0
Audio CTRL	1	1	1	0	VARI ON	VARI USE	0	0

Command bit	Processing
VARION = 0	Variable pitch mode is turned off. (The crystal is the reference to the internal clock.)
VARION = 1	Variable pitch mode is turned on. (The VCO2 is the reference to the internal clock.)

Command bit	Processing
VARIUSE = 0	When the variable pitch mode is not used, set VARIUSE to 0.
VARIUSE = 1	When the variable pitch mode is used, set VAIRUSE to 1.

* See "$DX commands" for the variable range and the usage example of the variable pitch.

$BX commands

This command sets the traverse monitor count.

Command	Data 1				Data 2				Data 3				Data 4			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
Traverse monitor count setting	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

- When the set number of tracks are counted during fine search, the sled control for the traverse cycle control goes off.
- The traverse monitor count is set to monitor the traverse status from the SENS output as COMP and COUT.

This command sets the monitor output switching.

Command	Data 5			
	D3	D2	D1	D0
Traverse monitor count setting	0	0	MTSL1	MTSL0

Command bit		Output data			
MTSL1	MTSL0				
0	0	XUGF	XPCK	GFS	C2PO
0	1	MNT0	MNT1	MNT2	MNT3
1	0	RFCK	XPCK	XROF	GTOP

$CX commands

Command	Data 1				Data 2			
	D3	D2	D1	D0	D3	D2	D1	D0
Spindle servo coefficient setting	Gain MDP1	Gain MDP0	Gain MDS1	Gain MDS0	Gain DCLV1	Gain DCLV0	PCC1	PCC0
CLV CTRL ($DX)				Gain CLVS				

• CLVS mode gain setting: GCLVS

Gain MDS1	Gain MDS0	Gain CLVS	GCLVS
0	0	0	–12dB
0	0	1	–6dB
0	1	0	–6dB
0	1	1	0dB
1	0	0	0dB
1	0	1	+6dB

• CLVP mode gain setting: GMDP : GMDS

Gain MDP1	Gain MDP0	GMDP
0	0	–6dB
0	1	0dB
1	0	+6dB

Gain MDS1	Gain MDS0	GMDS
0	0	–6dB
0	1	0dB
1	0	+6dB

• DCLV overall gain setting: GDCLV

Gain DCLV1	Gain DCLV0	GDCLV
0	0	0dB
0	1	+6dB
1	0	+12dB

Command bit		Processing
PCC1	PCC0	
0	0	The VPCO signal is output.
0	1	The VPCO pin output is high impedance.
1	0	The VPCO pin output is low.
1	1	The VPCO pin output is high.

• This command controls the VPCO pin signal.

The VPCO output can be controlled with this setting.

Command	Data 3				Data 4			
	D3	D2	D1	D0	D3	D2	D1	D0
Spindle servo coefficient setting	SFP3	SFP2	SFP1	SFP0	SRP3	SRP2	SRP1	SRP0

Command bit	Processing
SFP3 to 0	Sets the frame sync forward protection times. The setting range is 1 to F (Hex).

Command bit	Processing
SRP3 to 0	Sets the frame sync backward protection times. The setting range is 1 to F (Hex).

* See "§ 4-2. Frame Sync Protection" regarding frame sync protection.

• The CXD3068Q can serially output the 40 bits (10 BCD codes) of error monitor data selected by EDC0 to 7 from the SQSO pin and monitor this data using a microcomputer.
The C1 and C2 error rate settings are sent one at a time by the $C commands by setting $8 commands SOCT0 and SOCT1 = 1. Then, the data can be read out from the SQSO pin by sending 40 SQCK pulses.

$CX commands

Command	Data 5				Data 6			
	D3	D2	D1	D0	D3	D2	D1	D0
Spindle servo coefficient setting	EDC7	EDC6	EDC5	EDC4	EDC3	EDC2	EDC1	EDC0

Error monitor commands

Command bit		Processing
EDC7 = 0	EDC6	The [No C1 errors, pointer reset] count is output when 0.
	EDC5	The [One C1 error corrected, pointer reset] count is output when 0.
	EDC4	The [No C1 errors, pointer set] count is output when 0.
	EDC3	The [One C1 error corrected, pointer set] count is output when 0.
	EDC2	The [Two C1 errors corrected, pointer set] count is output when 0.
	EDC1	The [C1 correction impossible, pointer set] count is output when 0.
	EDC0	7350 frame count cycle mode*1 when 1. 73500 frame count cycle mode*2 when 0.
EDC7 = 1	EDC6	The [No C2 errors, pointer reset] count is output when 0.
	EDC5	The [One C2 error corrected, pointer reset] count is output when 0.
	EDC4	The [Two C2 errors corrected, pointer reset] count is output when 0.
	EDC3	The [Three C2 errors corrected, pointer reset] count is output when 0.
	EDC2	The [Four C2 errors corrected, pointer reset] count is output when 0.
	EDC1	The [C2 correction impossible, pointer copy] count is output when 0.
	EDC0	The [C2 correction impossible, pointer set] count is output when 0.

*1 The number selected by C1 (EDC1 to 6) and C2 (EDC0 to 6) is added to C1 and C2 and output every 7350 frames.

*2 The number selected by C1 (EDC1 to 6) and C2 (EDC0 to 6) is added to C1 and C2 and output every 73500 frames.

$DX commands

Command	Data 1			
	D3	D2	D1	D0
CLV CTRL	0	TB	TP	Gain CLVS

See "$CX commands".

Command bit	Description
TB = 0	Bottom hold at a cycle of RFCK/32 in CLVS mode.
TB = 1	Bottom hold at a cycle of RFCK/16 in CLVS mode.
TP = 0	Peak hold at a cycle of RFCK/4 in CLVS mode.
TP = 1	Peak hold at a cycle of RFCK/2 in CLVS mode.

Command	Data 2				Data 3				Data 4			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
CLV CTRL	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0	VP CTL1	VP CTL0	0	0

The settings are as follows in CAV-W mode.

Command bit	Processing
VP0 to 7	The spindle rotational velocity is set.

Command bit		Processing
VPCTL1	VPCTL0	
0	0	The setting of VP0 to 7 is multiplied by 1.
0	1	The setting of VP0 to 7 is multiplied by 2.
1	0	The setting of VP0 to 7 is multiplied by 3.
1	1	The setting of VP0 to 7 is multiplied by 4.

* The above setting should be 0, 0 except for the CAV-W operating mode.

The rotational velocity R of the spindle can be expressed with the following equation.

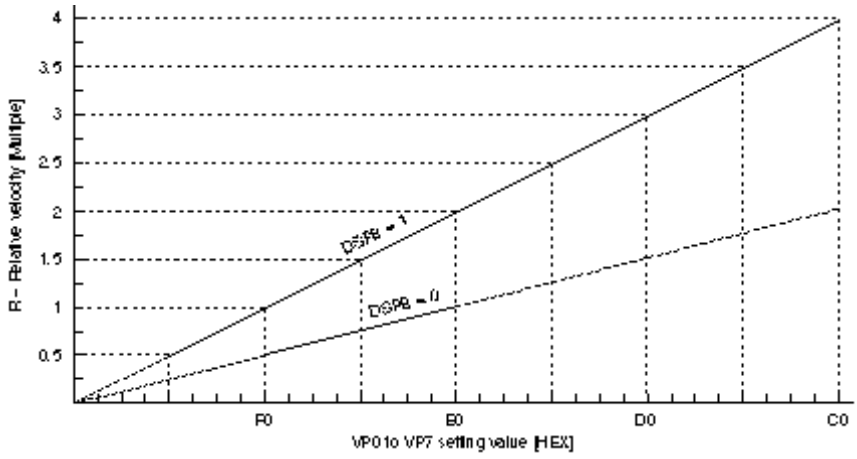
$$R = \frac{256 - n}{32} \times I$$

R: Relative velocity at normal speed = 1
n: VP0 to 7 setting value
I: Multiple set by VPCTL0, 1

Command bit	Description
VP0 to 7 = F0 (H)	Playback at 1/2 (1) × speed
⋮	⋮
VP0 to 7 = E0 (H)	Playback at 1 (2) × speed
⋮	⋮
VP0 to 7 = C0 (H)	Playback at (4) × speed

Notes)

1. Values when crystal is 16.9344MHz and XTSL is low or when crystal is 33.8688MHz and XTSL is high.
2. The values in parentheses are for when DSPB is 1.



The setting in variable pitch mode is as shown below.

Command bit	Processing
VPCTL1 to 0, VP7 to 0	The pitch of variable pitch mode is set.

The setting of the pitch can be expressed with the equation below.

$$P = \frac{-n}{10} \ [\%]$$

P: Setting value of pitch
n: Setting value for VPCTL1, VPCTL0 and VP7 to VP0 (two's complementary, VPCTL1 is sign bit)

Command bit			Setting value of pitch [%]	Example of command setting
VPCTL1	VPCTL0	VP7 to 0		
1	0	00 (H)	+51.2	$D60080
		:	:	:
		FF (H)	+25.7	$D6FF80
1	1	00 (H)	+25.6	$D600C0
		:	:	:
		FF (H)	+0.1	$D6FFC0
0	0	00 (H)	0.0	$D60000
		:	:	:
		FF (H)	–25.5	$D6FF00
0	1	00 (H)	–25.6	$D60040
		:	:	:
		FF (H)	–48.7	$D6E740

The setting range of the pitch is –48.7 to +51.2%.
The pitch setting for + side should be within the playback speed of the recommended operating conditions.

The following is the example of the command in variable pitch mode.

$EX001 (Sets to CLV-N mode. The INV VPCO is set to 1.)
$AE4XX (Sets to use variable pitch mode)
WAIT (Wait time for VCO2 pull-in: until VCTL stabilizes.)
$AECXX (Variable pitch mode is turned on. The VCO2 is the reference to the internal clock.)
$D60A00 (The pitch is set to -1.0%)
$D60000 (The pitch is set to 0.0%)
$AE4XX (Variable pitch mode is turned off. The crystal is the reference to the internal clock.)

$EX commands

Command	Data 1				Data 2				Data 3			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
SPD mode	CM3	CM2	CM1	CM0	EPWM	SPDC	ICAP	SFSL	VC2C	HIFC	LPWR	VPON

Command bit				Mode	Description
CM3	CM2	CM1	CM0		
0	0	0	0	STOP	Spindle stop mode.*1
1	0	0	0	KICK	Spindle forward rotation mode.*1
1	0	1	0	BRAKE	Spindle reverse rotation mode. Valid only when LPWR = 0 in any mode.*1
1	1	1	0	CLVS	Rough servo mode. When the RF-PLL circuit isn't locked, this mode is used to pull the disc rotations within the RF-PLL capture range.
1	1	1	1	CLVP	PLL servo mode.
0	1	1	0	CLVA	Automatic CLVS/CLVP switching mode. Used for normal playback.

*1 See Timing Charts 1-6 to 1-12.

Command bit									Mode	Description
EPWM	SPDC	ICAP	SFSL	VC2C	HIFC	LPWR	VPON	INV VPCO		
0	0	0	0	0	0	0	0	0	CLV-N	Crystal reference CLV servo.
0	0	0	0	1	1	0	0	0	CLV-W	Used for playback in CLV-W mode.*2
0	1	1	0	0	1	0	1	0	CAV-W	Spindle control with VP0 to 7.
1	0	1	0	0	1	0	1	0	CAV-W	Spindle control with the external PWM.
0	0	0	0	0	1	0	1	1	VCO-C	VCO control*3

*2 Figs. 3-1 and 3-2 show the control flow with the microcomputer software in CLV-W mode.

*3 Fig. 3-3 shows the control flow with the microcomputer software in VCO-C mode.

Mode	LPWR	Command	Timing chart
CLV-N	0	KICK	1-6 (a)
		BRAKE	1-6 (b)
		STOP	1-6 (c)
CLV-W	0	KICK	1-7 (a)
		BRAKE	1-7 (b)
		STOP	1-7 (c)
	1	KICK	1-8 (a)
		BRAKE	1-8 (b)
		STOP	1-8 (c)
CAV-W	0	KICK	1-9 (a)
		BRAKE	1-9 (b)
		STOP	1-9 (c)
	1	KICK	1-10 (a)
		BRAKE	1-10 (b)
		STOP	1-10 (c)

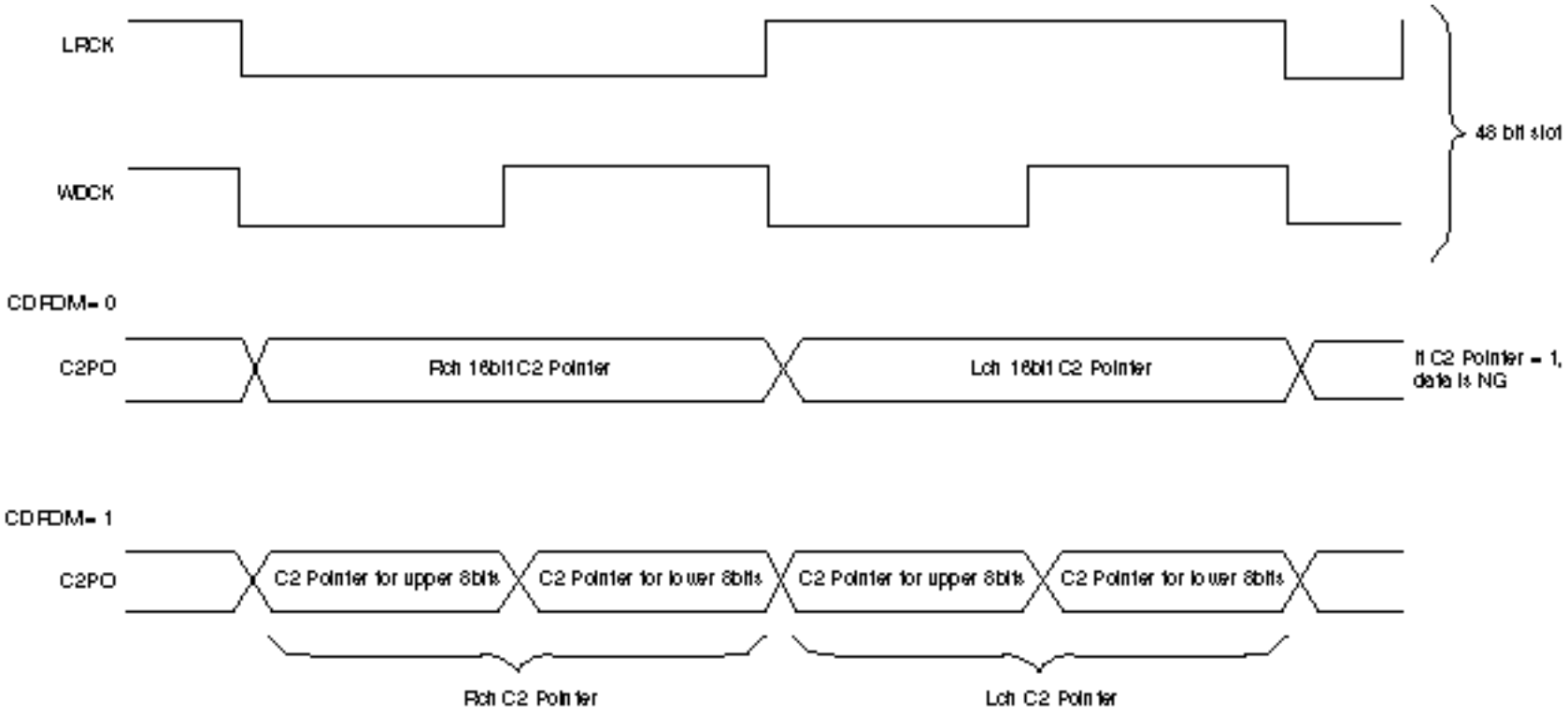
Mode	LPWR	Timing chart
CLV-N	0	1-11
CLV-W	0	1-12
	1	1-13
CAV-W	0	1-14 (EPWM = 0)
	1	1-15 (EPWM = 0)
	0	1-16 (EPWM = 1)
	1	1-17 (EPWM = 1)

Command	Data 4			
	D3	D2	D1	D0
SPD mode	Gain CAV1	Gain CAV0	0	INV VPCO

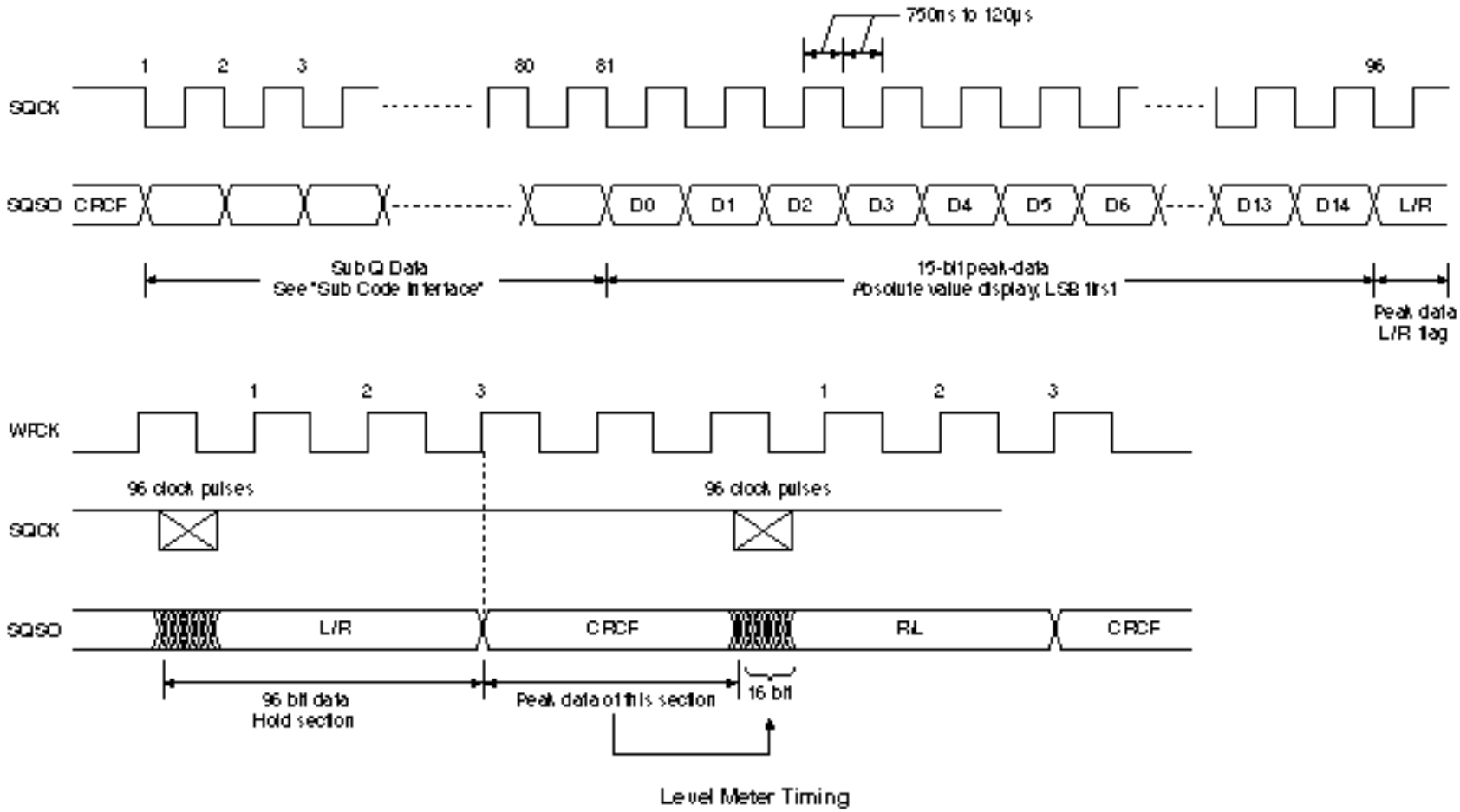
Gain CAV1	Gain CAV0	Gain
0	0	0dB
0	1	–6dB
1	0	–12dB
1	1	–18dB

• This sets the gain when controlling the spindle with the phase comparator in CAV-W mode.

Timing Chart 1-3

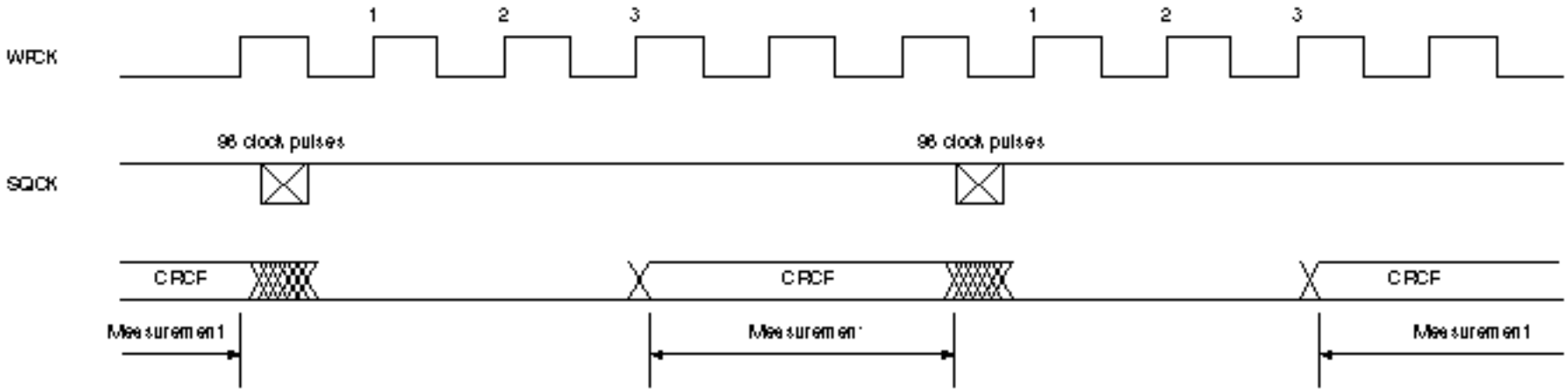


Timing Chart 1-4



Level Meter Timing

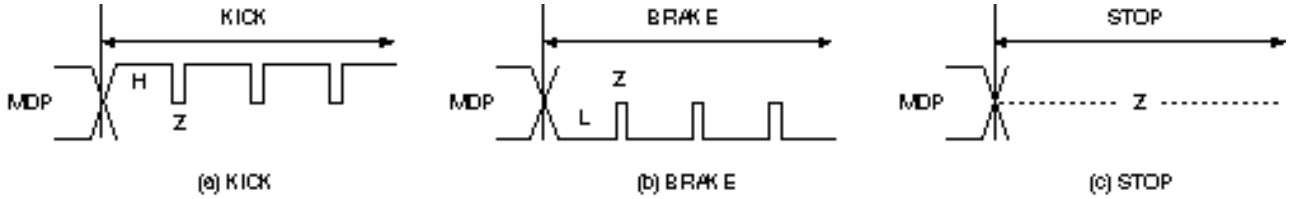
Timing Chart 1-5



Peak Meter Timing

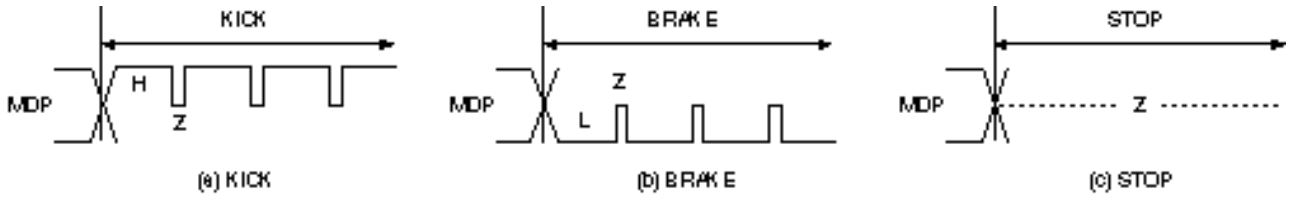
Timing Chart 1-6

CLV-N mode LPWR = 0



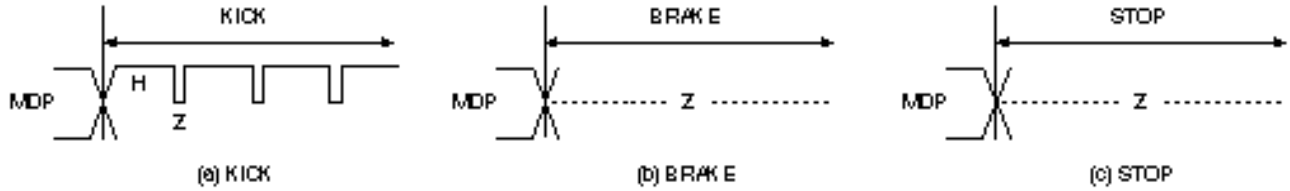
Timing Chart 1-7

CLV-W mode (when following the spindle rotational velocity) LPWR = 0



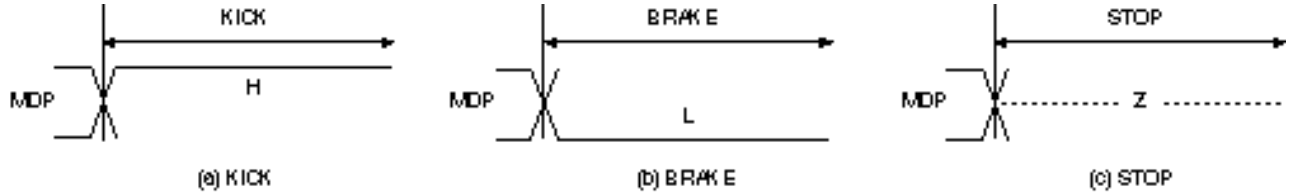
Timing Chart 1-8

CLV-W mode (when following the spindle rotational velocity) LPWR = 1



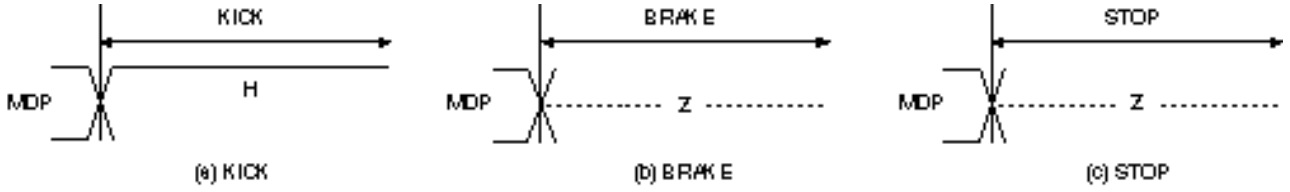
Timing Chart 1-9

CAV-W mode LPWR = 0



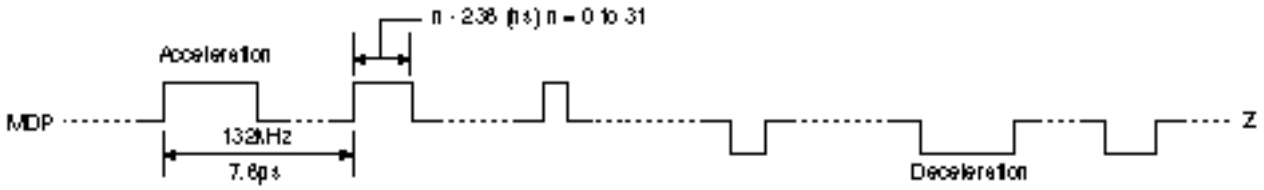
Timing Chart 1-10

CAV-W mode LPWR = 1



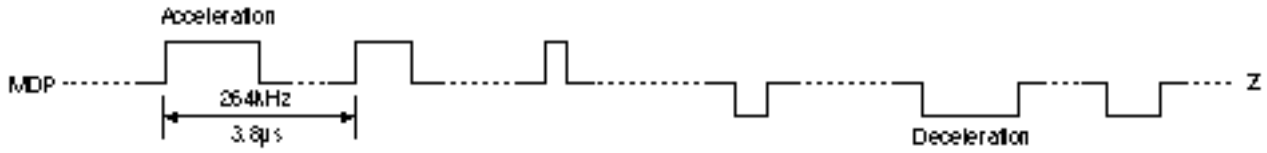
Timing Chart 1-11

CLV-N mode LPWR = 0



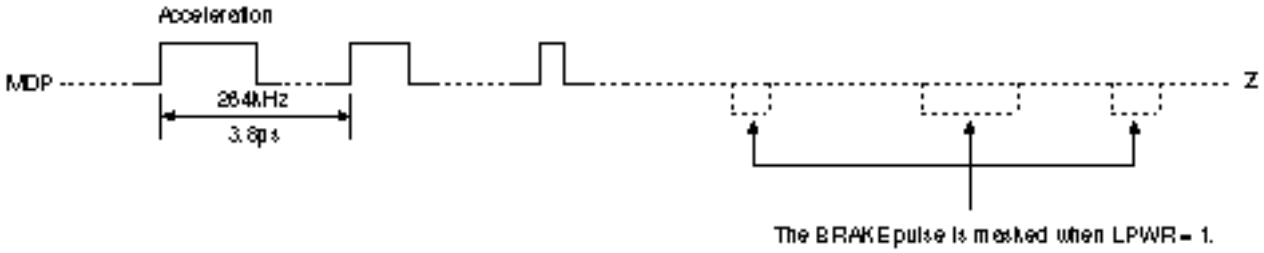
Timing Chart 1-12

CLV-W mode LPWR = 0



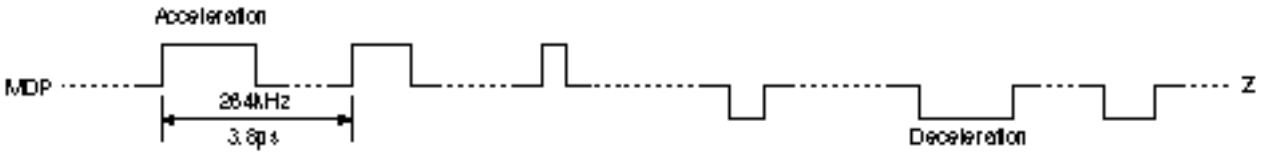
Timing Chart 1-13

CLV-W mode LPWR = 1



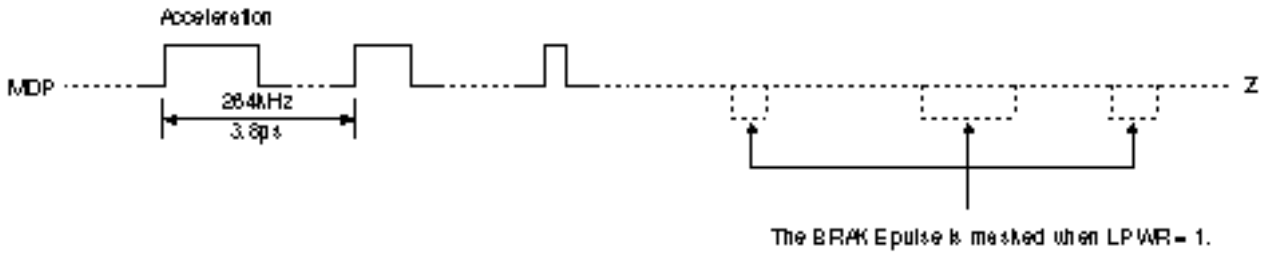
Timing Chart 1-14

CAV-W mode EPWM = LPWR = 0



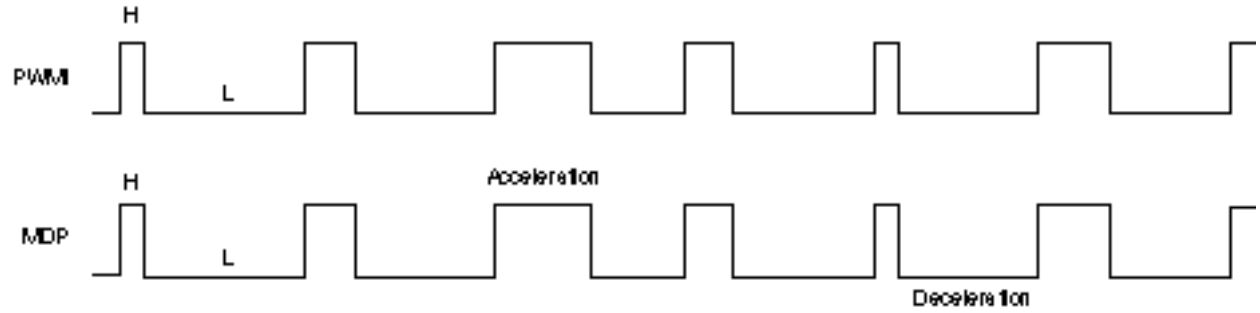
Timing Chart 1-15

CAV-W mode EPWM = LPWR = 1



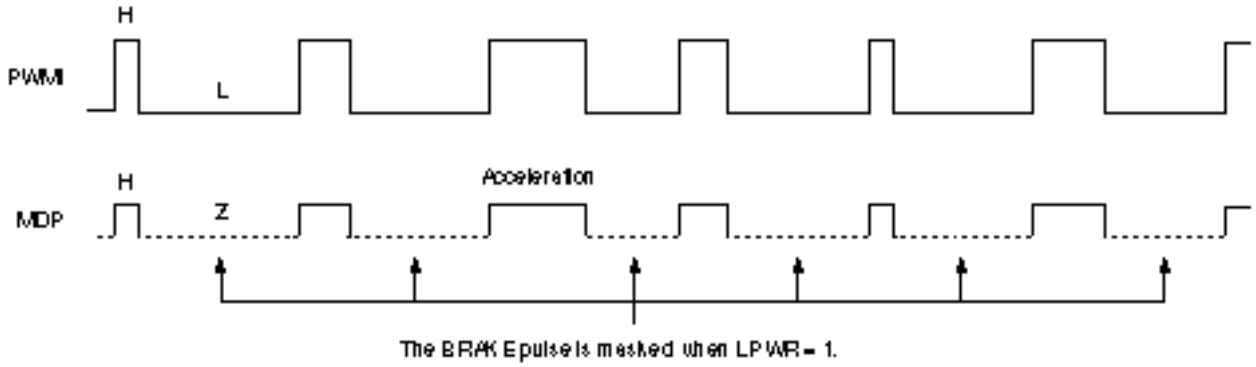
Timing Chart 1-16

CAV-W mode EPWM = 1, LPWR = 0



Timing Chart 1-17

CAV-W mode EPWM = LPWR = 1



[2] Subcode Interface

There are two methods for reading out a subcode externally.
The 8-bit subcodes P to W can be read out from SBSO by inputting EXCK.
Sub-Q can be read out after checking CRC of the 80 bits in the subcode frame.
Sub-Q can be read out from the SQSO pin by inputting 80 clock pulses to the SQCK pin when SCOR comes correctly and CRCF is high.

§ 2-1. P to W Subcode Readout

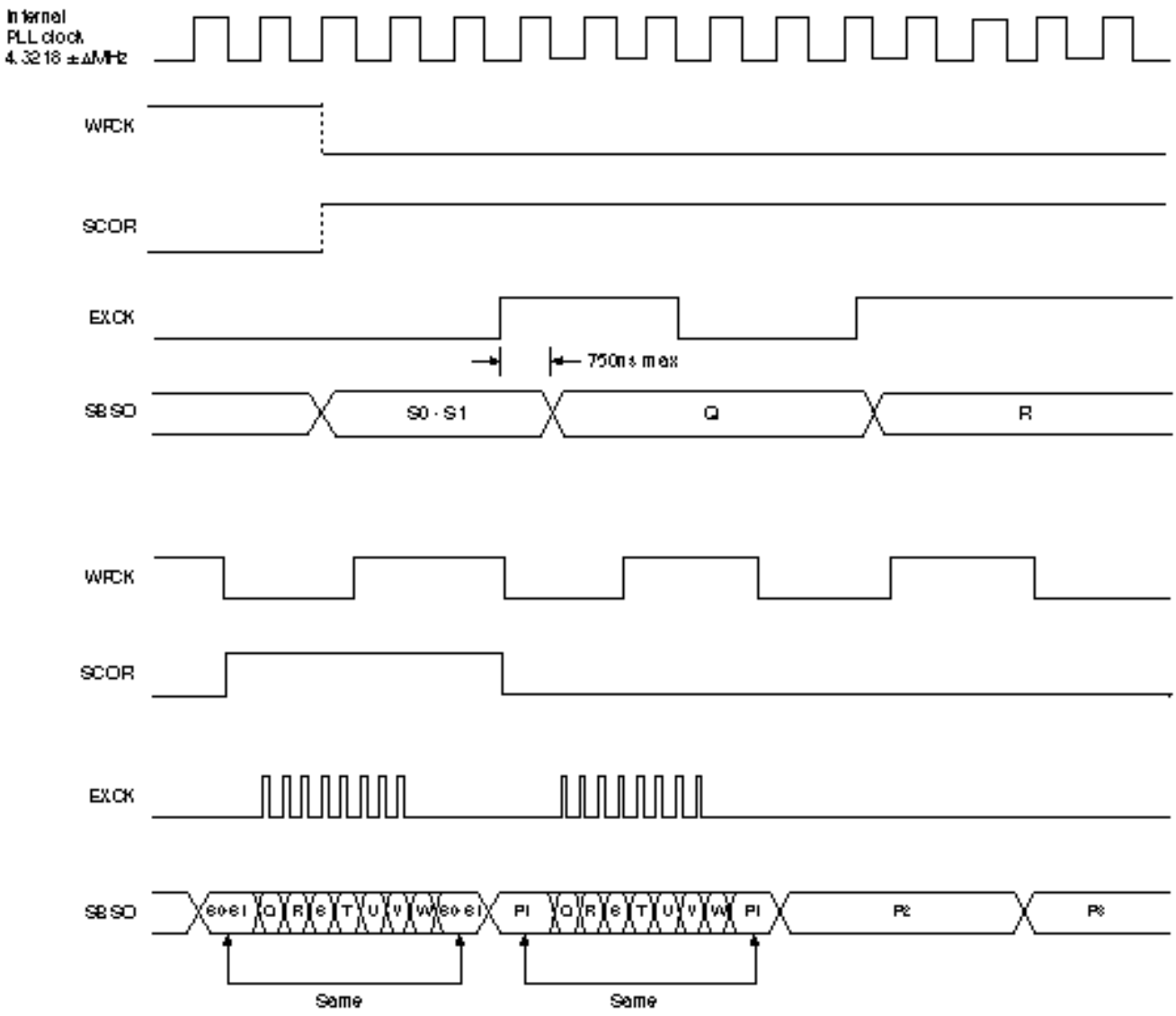
Data can be read out by inputting EXCK immediately after WFCK falls. (See Timing Chart 2-1.)

§ 2-2. 80-bit Sub-Q Readout

Fig. 2-2 shows the peripheral block of the 80-bit Sub-Q register.

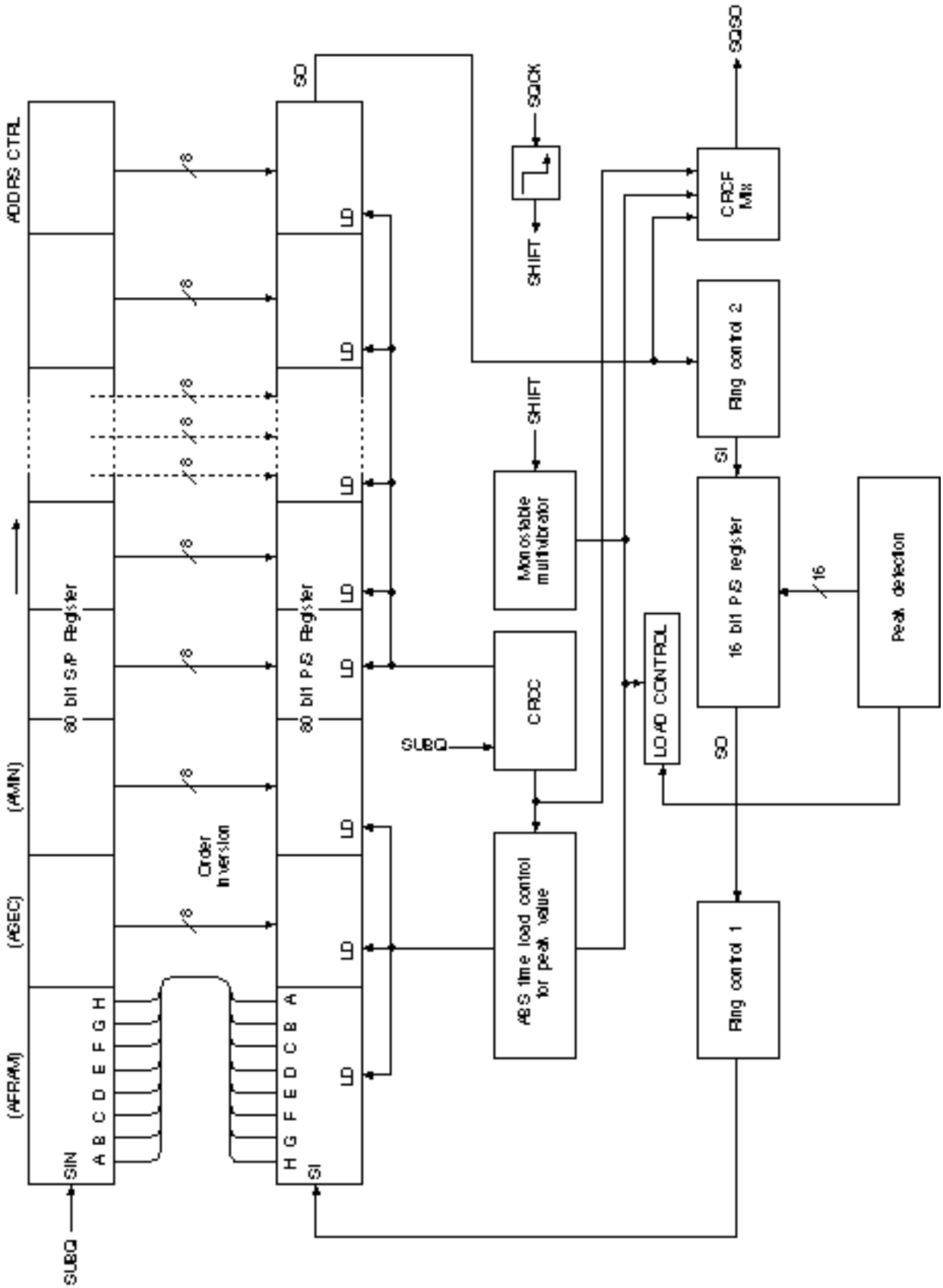
- First, Sub-Q, regenerated at one bit per frame, is input to the 80-bit serial/parallel register and the CRC check circuit.
- 96-bit Sub-Q is input, and if the CRC is OK, it is output to SQSO with CRCF = 1. In addition, 80 bits are loaded into the parallel/serial register.
  When SQSO goes high after SCOR is output, the CPU determines that new data (which passed the CRC check) has been loaded.
- When the 80-bit data is loaded, the order of the MSB and LSB is inverted within each byte. As a result, although the sequence of the bytes is the same, the bits within the bytes are now ordered LSB first.
- Once the 80-bit data load is confirmed, SQCK is input so that the data can be read.
  The SQCK input is detected, and the retriggerable monostable multivibrator is reset while the input is low.
- The retriggerable monostable multivibrator has a time constant from 270 to 400µs. When the duration when SQCK is high is less than this time constant, the monostable multivibrator is kept reset; during this interval, the serial/parallel register is not loaded into the parallel/serial register.
- While the monostable multivibrator is being reset, data cannot be loaded in the peak detection parallel/serial register or the 80-bit parallel/serial register.
  In other words, while reading out with a clock cycle shorter than this time constant, the register will not be rewritten by CRCOK and others.
- The previously mentioned peak detection register can be connected to the shift-in of the 80-bit parallel/serial register.
  For ring control 1, input and output are shorted during peak meter and level meter modes.
  For ring control 2, input and output are shorted during peak meter mode.
  This is because the register is reset with each readout in level meter mode, and to prevent readout destruction in peak meter mode.
  As a result, the 96-bit clock must be input in peak meter mode.
- The absolute time after peak is stored in the memory in peak meter mode. (See Timing Chart 2-3.)
- The high and low intervals for SQCK should be between 750ns and 120µs.

Timing Chart 2-1

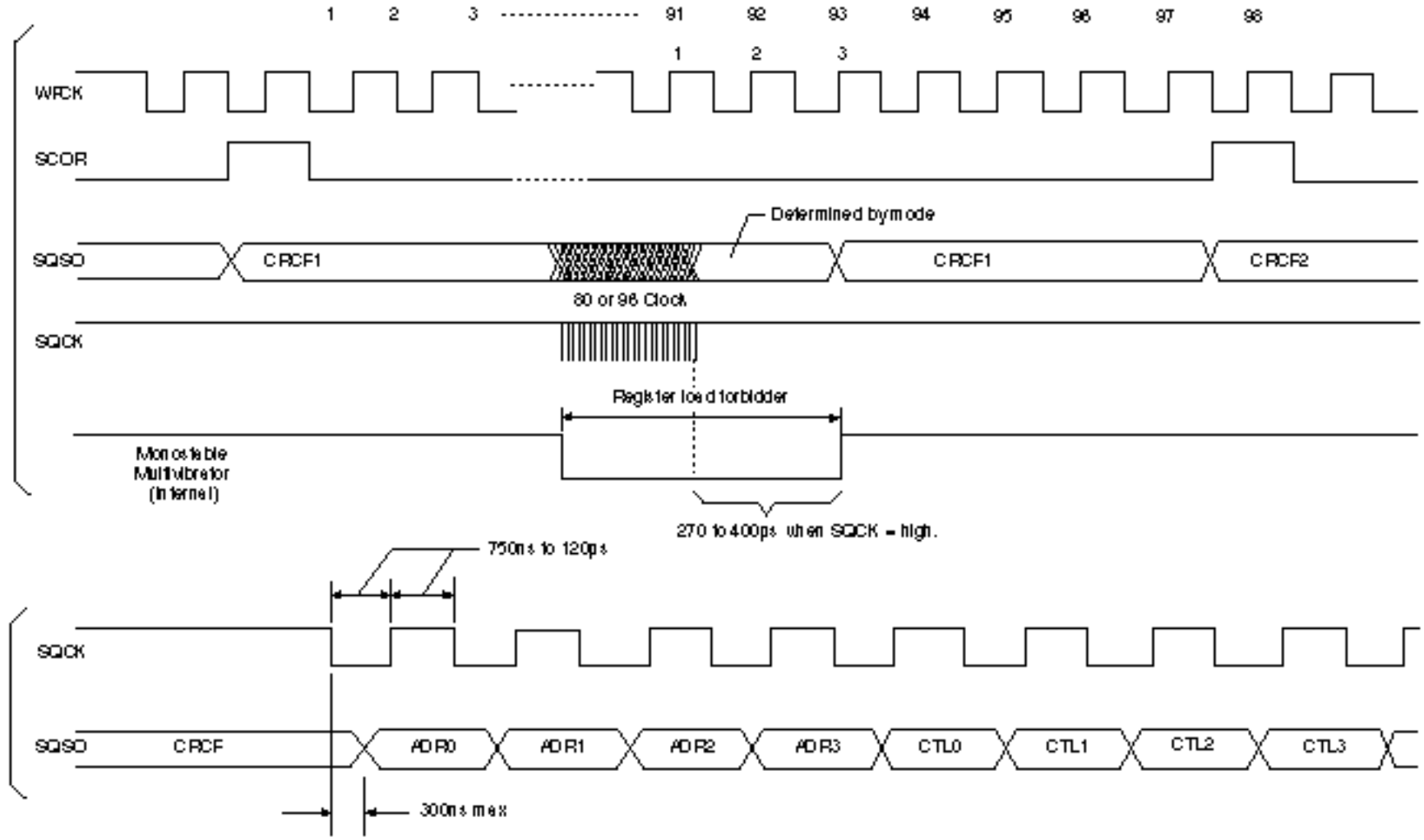


Subcode P, Q, R, S, T, U, V, W Read Timing

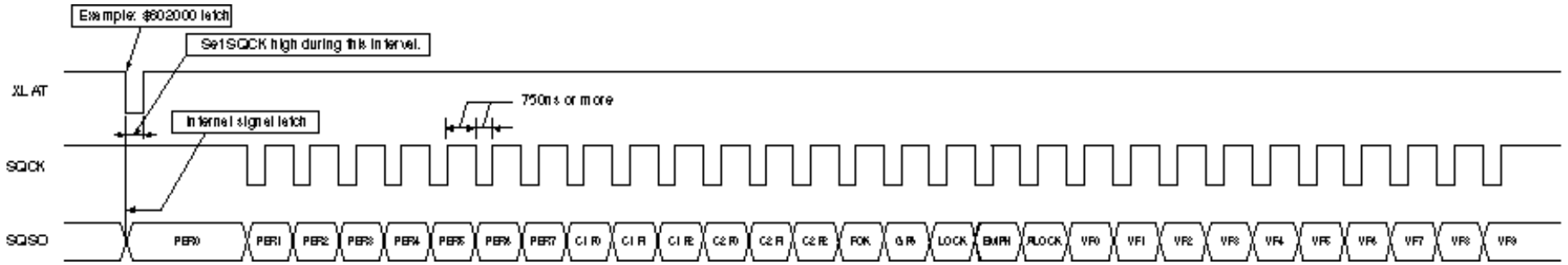
Block Diagram 2-2



Timing Chart 2-3



Timing Chart 2-4

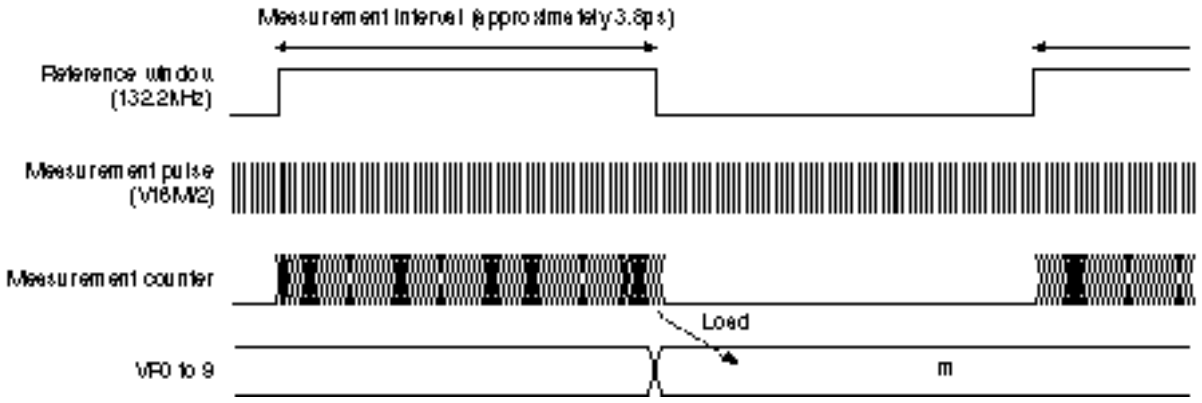


Signal	Description
PER0 to 7	RF jitter amount (used to adjust the focus bias). 8-bit binary data in PER0 = LSB, PER7 = MSB.
FOK	Focus OK.
GFS	High when the frame sync and the insertion protection timing match.
LOCK	GFS is sampled at 460Hz; when GFS is high, this pin outputs a high signal. If GFS is low eight consecutive samples, this pin outputs low.
EMPH	High when the playback disc has emphasis.
ALOCK	GFS is sampled at 460Hz; when GFS is high eight consecutive samples, this pin outputs a high signal. If GFS is low eight consecutive samples, this pin outputs low.
VF0 to 9	Used in CAV-W mode. The result obtained by measuring the rotational velocity of the disc. (See Timing Chart 2-5.) VF0 = LSB, VF9 = MSB.

C1F2	C1F1	C1F0	Description
0	0	0	No C1 errors; C1 pointer reset
0	0	1	One C1 error corrected; C1 pointer reset
0	1	0	—
0	1	1	—
1	0	0	No C1 errors; C1 pointer set
1	0	1	One C1 error corrected; C1 pointer set
1	1	0	Two C1 errors corrected; C1 pointer set
1	1	1	C1 correction impossible; C1 pointer set

C2F2	C2F1	C2F0	Description
0	0	0	No C2 errors; C2 pointer reset
0	0	1	One C2 error corrected; C2 pointer reset
0	1	0	Two C2 errors corrected; C2 pointer reset
0	1	1	Three C2 errors corrected; C2 pointer reset
1	0	0	Four C2 errors corrected; C2 pointer reset
1	0	1	—
1	1	0	C2 correction impossible; C1 pointer copy
1	1	1	C2 correction impossible; C2 pointer set

Timing Chart 2-5

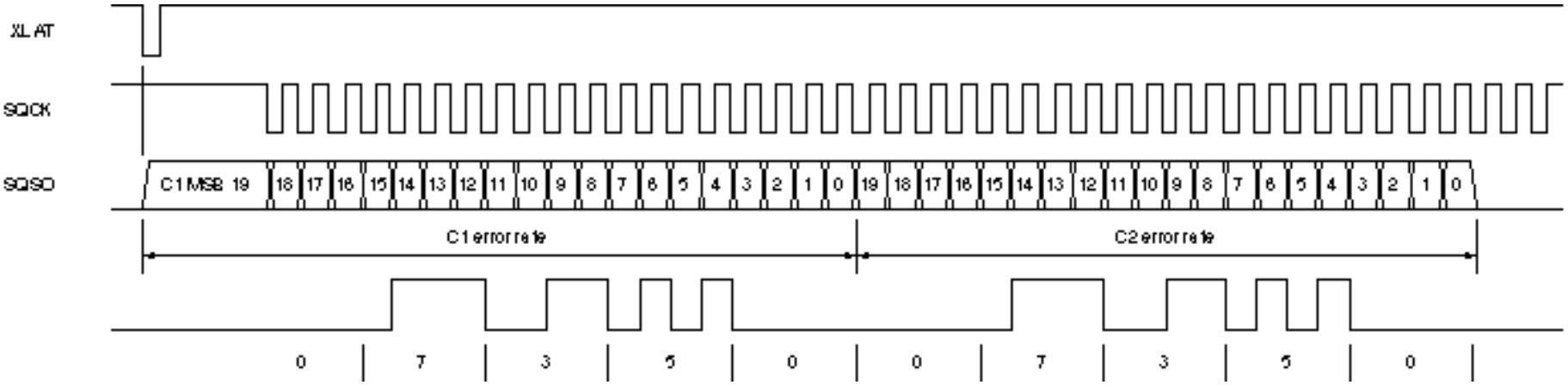


The relative velocity of the disc can be obtained with the following equation.

$$R = \frac{(m + 1)}{32}$$ (R: Relative velocity, m: Measurement results)

VF0 to 9 is the result obtained by counting V16M/2 pulses while the reference signal (132.2kHz) generated from XTAL (XTAI, XTAO) (384Fs) is high. This value is 31 when the disc is rotating at normal speed and 63 when it is rotating at double speed (when DSPB is low).

Timing Chart 2-6



[3] Description of Modes

This LSI has three basic operating modes using a combination of spindle control and the PLL. The operations for each mode are described below.

§ 3-1. CLV-N Mode

This mode is compatible with the CXD2510Q, and operation is the same as for conventional control. The PLL capture range is ±150kHz.

§ 3-2. CLV-W Mode

This is the wide capture range mode. This mode allows the PLL to follow the rotational velocity of the disc. This rotational following control has two types: using the built-in VCO2 or providing an external VCO. The spindle is the same CLV servo as for the conventional series. Operation using the built-in VCO2 is described below. (When using an external VCO, input the signal from the VPCO pin to the low-pass filter, use the output from the low-pass filter as the control voltage for the external VCO, and input the oscillation from the VCO to the V16M pin.)

When starting to rotate the disc and/or speeding up to the lock range from the condition where the disc is stopped, CAV-W mode should be used. Specifically, first send $E665X to set CAV-W mode and kick the disc, then send $E60CX to set CLV-W mode if ALOCK is high, which can be read out serially from the SQSO pin. CLV-W mode can be used while ALOCK is high. The microcomputer monitors the serial data output, and must return the operation to the speed adjusting state (CAV-W mode) when ALOCK becomes low. The control flow according to the microcomputer software in CLV-W mode is shown in Fig. 3-2.

In CLV-W mode (normal), low power consumption is achieved by setting LPWR to high. Control was formerly performed by applying acceleration and deceleration pulses to the spindle motor. However, when LPWR is set high, deceleration pulses are not output, thereby achieving low power consumption mode.

Note) The capture range for this mode is theoretically up to the signal processing limit.

§ 3-3. CAV-W Mode

This is CAV mode. In this mode, the external clock is fixed and it is possible to control the spindle to the desired rotational velocity. The rotational velocity is determined by the VP0 to VP7 setting values or the external PWM. When controlling the spindle with VP0 to VP7, setting CAV-W mode with the $E665X command and controlling VP0 to VP7 with the $DX commands allows the rotational velocity to be varied from low speed to 4× speed. (See "$DX commands".) Also, when controlling the spindle with the external PWM, the PWMI pin is binary input which becomes KICK during high intervals and BRAKE during low intervals.

The microcomputer can know the rotational velocity using V16M. The reference frequency for the velocity measurement is a signal of 132.3kHz obtained by dividing XTAL (XTAI, XTAO) (384Fs) by 128. The velocity is obtained by counting the half of V16M pulses while the reference is high, and the result is output from the new CPU interface as 10 bits (VP0 to VP9). These measurement results are 31 when the disc is rotating at normal speed or 127 when it is rotating at 4× speed. These values match those of the 256 - n for control with VP0 to VP7. (See Table 2-5 and Fig. 2-6.)

In CAV-W mode, the spindle is set to the desired rotational velocity and the operation speed for the entire system follows this rotational velocity. Therefore, the cycles for the Fs system clock, PCM data and others output from this LSI change according to the rotational velocity of the disc.

Note) The capture range for this mode is theoretically up to the signal processing limit.
Note) Set FLFC to 1 for this mode

§ 3-4. VCO-C Mode

This is VCO control mode. In this mode, the V16M oscillation frequency can be controlled by setting $D commands VP0 to VP7 and VPCTL0, 1. The V16M oscillation frequency can be expressed by the following equation.

$$V16M = \frac{l\ (256 - n)}{32}$$

n: VP0 to 7 setting value
l: VPCTL0, 1 setting value

The VCO1 oscillation frequency is determined by V16M. The VCO1 frequency can be expressed by the following equation.

• When DSPB = 0

$$VCO1 = V16M \times \frac{49}{24}$$

• When DSPB = 1

$$VCO1 = V16M \times \frac{49}{16}$$

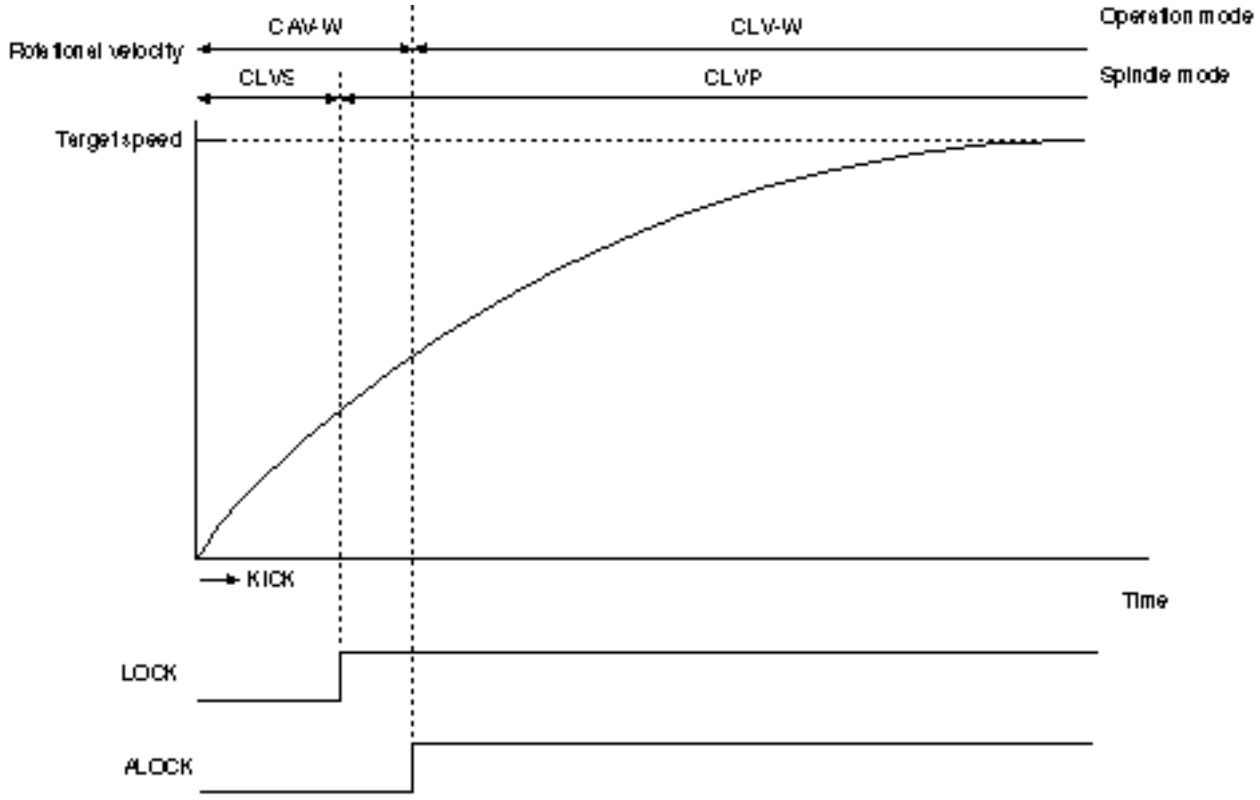


Fig. 3-1. Disc Stop to Regular Playback in CLV-W Mode

CLV-W Mode

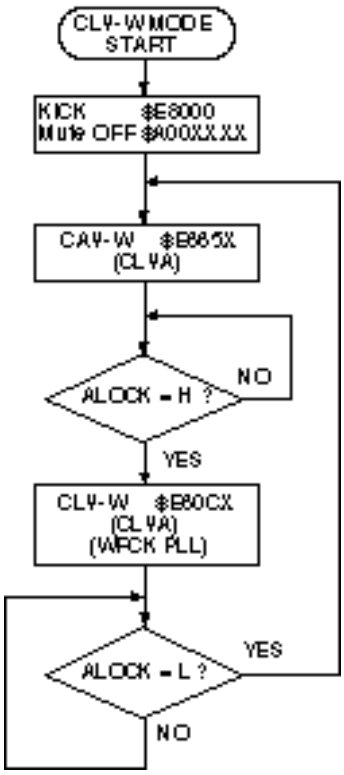


Fig. 3-2. CLV-W Mode Flow Chart

VCO-C Mode

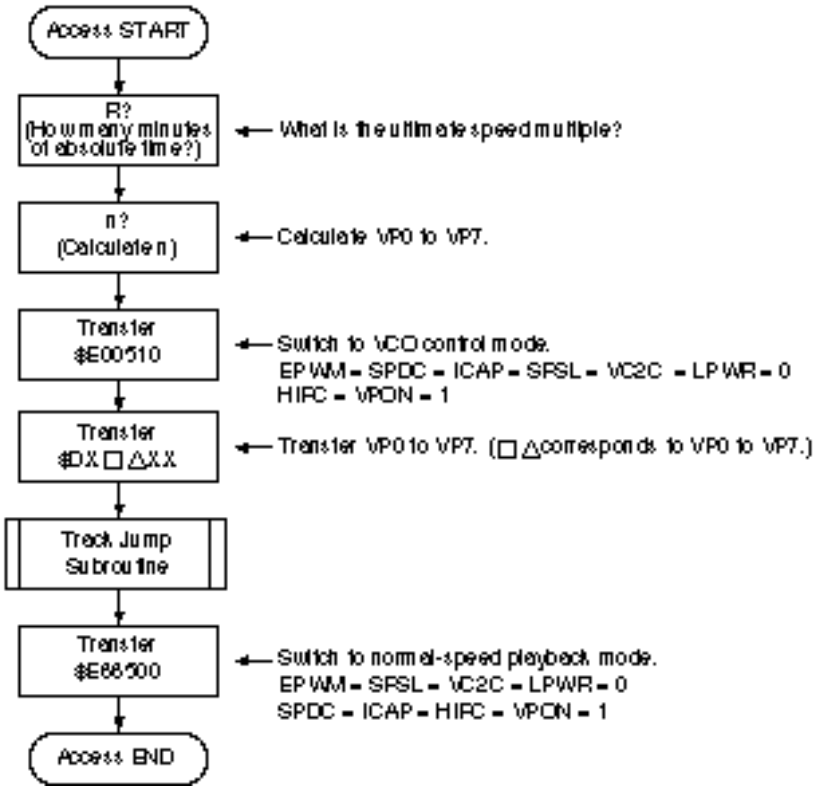


Fig. 3-3. Access Flow Chart Using VCO Control

[4] Description of other functions

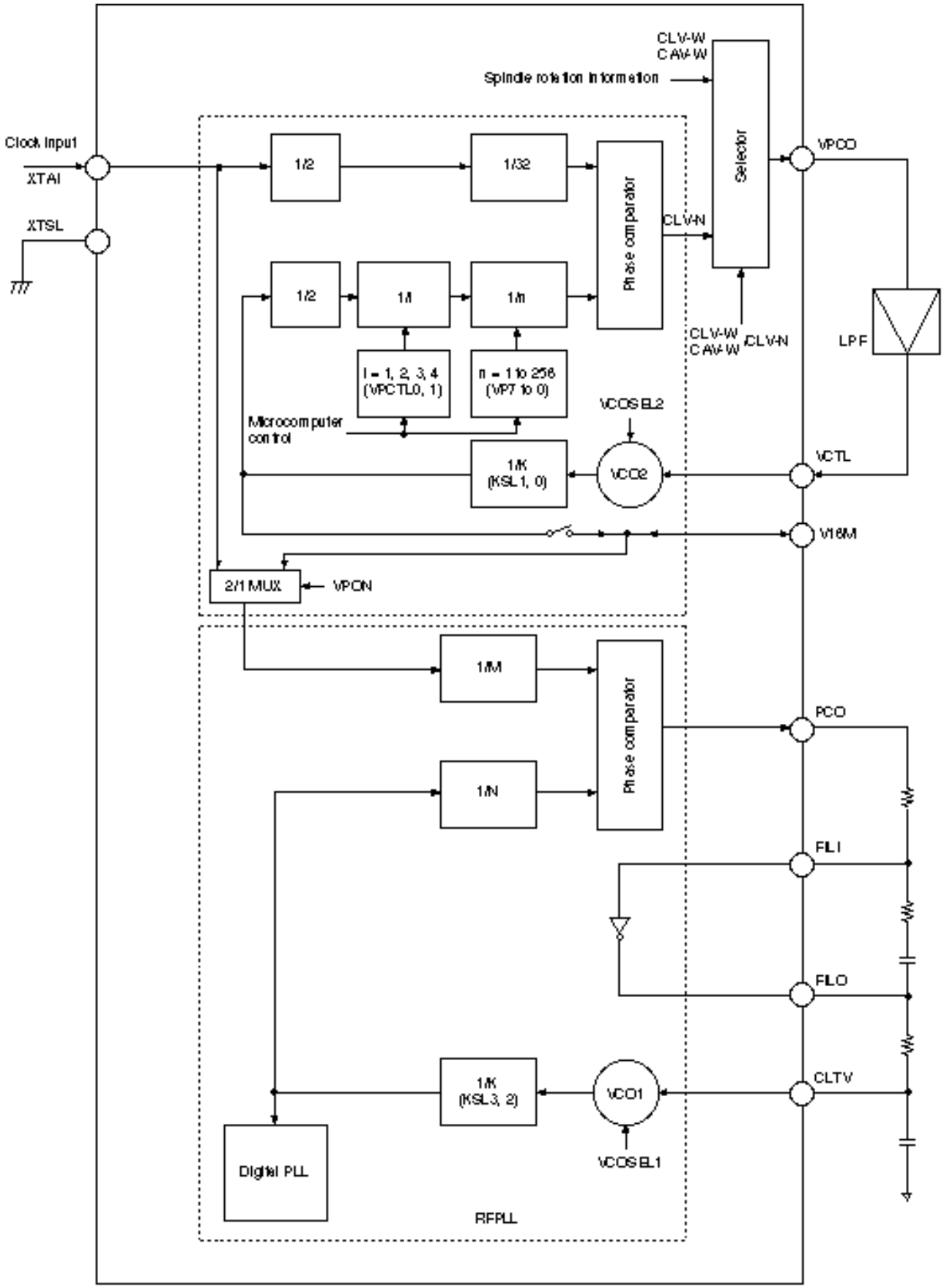
§ 4-1. Channel Clock Regeneration by Digital PLL Circuit

- The channel clock is necessary for demodulating the EFM signal regenerated by the optical system.
  Assuming T as the channel clock cycle, the EFM signal is modulated in an integer multiple of T from 3T to 11T. In order to read the information in the EFM signal, this integer value must be read correctly. As a result, T, that is the channel clock, is necessary.
  In an actual player, a PLL is necessary for regenerating the channel clock because the fluctuation in the spindle rotation alters the width of the EFM signal pulses.

The block diagram of this PLL is shown in Fig. 4-1.
The CXD3068Q has a built-in three-stage PLL.

- The first-stage PLL is a wide-band PLL. When using the internal VCO2, an external LPF is necessary; when not using the internal VCO2, external LPF and VCO are necessary.
  The output of this first-stage PLL is used as a reference for all clocks within the LSI.
- The second-stage PLL regenerates the high-frequency clock needed by the third-stage digital PLL.
- The third-stage PLL is a digital PLL that regenerates the actual channel clock.
- The digital PLL in CLV-N mode has a secondary loop, and is controlled by the primary loop (phase) and the secondary loop (frequency). When FLFC = 1, the secondary loop can be turned off. High frequency components such as 3T and 4T may contain deviations. In such cases, turning the secondary loop off yields better playability. However, in this case the capture range becomes ±50kHz.
- A new digital PLL has been provided for CLV-W mode to follow the rotational velocity of the disc in addition to the conventional secondary loop.

Block Diagram 4-1



§ 4-2. Frame sync protection

- In normal speed playback, a frame sync is recorded approximately every 136µs (7.35kHz). This signal is used as a reference to recognize the data within a frame. Conversely, if the frame sync cannot be recognized, the data is processed as error data because the data cannot be recognized. As a result, recognizing the frame sync properly is extremely important for improving playability.
- In the CXD3068Q, window protection and forward protection/backward protection have been adopted for frame sync protection. These functions achieve very powerful frame sync protection. There are two window widths; one for cases where a rotational disturbance affects the player and the other for cases where there is no rotational disturbance (WSEL = 0/1). In addition, the forward protection counter is set to 13*, and the backward protection counter to 3*. Concretely, when the frame sync is being played back normally and then cannot be detected due to scratches, a maximum of 13 frames are inserted. If the frame sync cannot be detected for 13 frames or more, the window opens to resynchronize the frame sync.
  In addition, immediately after the window opens and the resynchronization is executed, if a proper frame sync cannot be detected within 3 frames, the window opens immediately.
  * Default values. These values can be set as desired by $C commands SFP0 to SFP3 and SRP0 to SRP3.

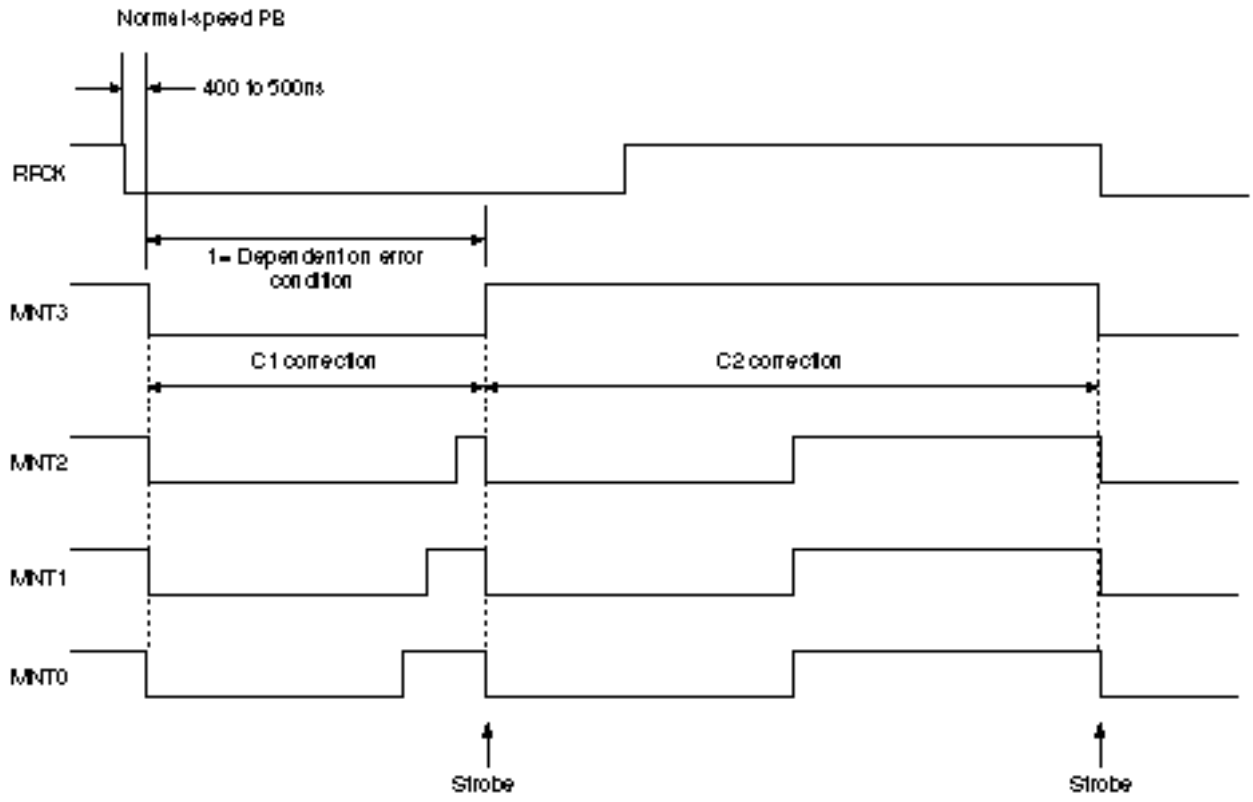
§ 4-3. Error Correction

- In the CD format, one 8-bit data contains two error correction codes, C1 and C2. For C1 correction, the code is created with 28-byte information and 4-byte C1 parity.
  For C2 correction, the code is created with 24-byte information and 4-byte parity.
  Both C1 and C2 are Reed Solomon codes with a minimum distance of 5.
- The CXD3068Q uses refined super strategy to achieve double correction for C1 and quadruple correction for C2.
- In addition, to prevent C2 miscorrection, a C1 pointer is attached to data after C1 correction according to the C1 error status, the playback status of the EFM signal, and the operating status of the player.
- The correction status can be monitored externally.
  See Table 4-2.
- When the C2 pointer is high, the data in question was uncorrectable. Either the pre-value was held or an average value interpolation was made for the data.

MNT3	MNT2	MNT1	MNT0	Description
0	0	0	0	No C1 errors; C1 pointer reset
0	0	0	1	One C1 error corrected; C1 pointer reset
0	0	1	0	—
0	0	1	1	—
0	1	0	0	No C1 errors; C1 pointer set
0	1	0	1	One C1 error corrected; C1 pointer set
0	1	1	0	Two C1 errors corrected; C1 pointer set
0	1	1	1	C1 correction impossible; C1 pointer set
1	0	0	0	No C2 errors; C2 pointer reset
1	0	0	1	One C2 error corrected; C2 pointer reset
1	0	1	0	Two C2 errors corrected; C2 pointer reset
1	0	1	1	Three C2 errors corrected; C2 pointer reset
1	1	0	0	Four C2 errors corrected; C2 pointer reset
1	1	0	1	—
1	1	1	0	C2 correction impossible; C1 pointer copy
1	1	1	1	C2 correction impossible; C2 pointer set

Table 4-2.

Timing Chart 4-3



§ 4-4. DA Interface

• The CXD3068Q supports the 48-bit slot interface as the DA interface.

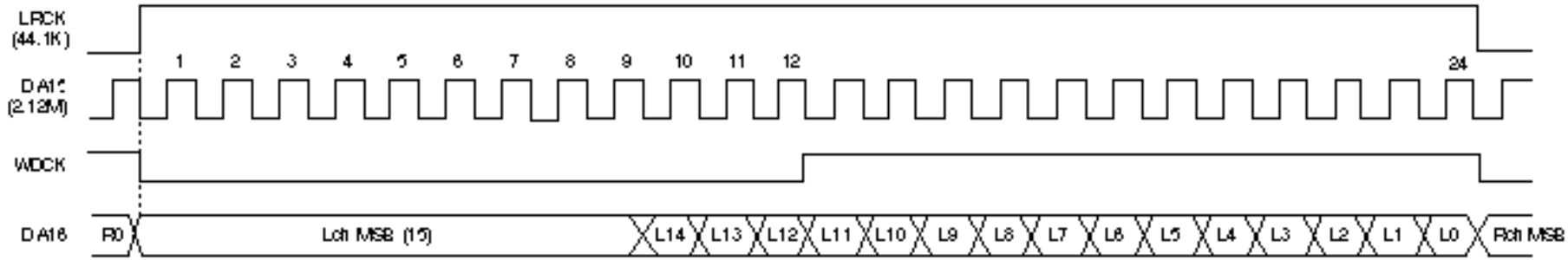
48-bit slot interface

This interface includes 48 cycles of the bit clock within one LRCK cycle, and is MSB first.

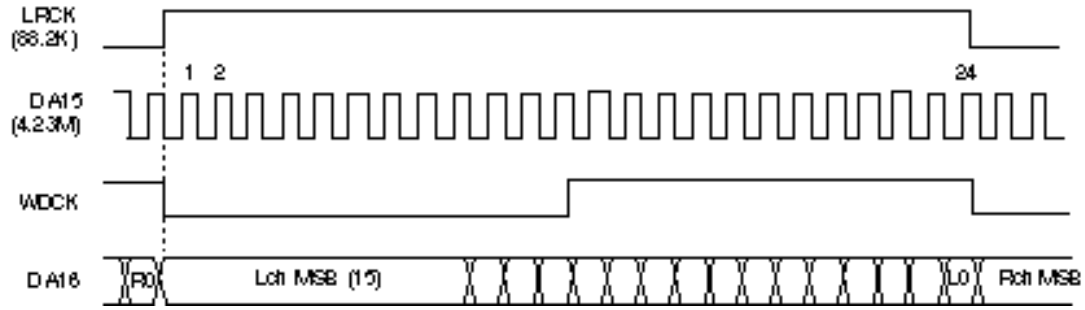
When LRCK is high, the data is for the left channel.

Timing Chart 4-4

48bit slot Normal-Speed Playback PSSL = L



48bit slot Double-Speed Playback



§ 4-5. Digital Out

There are three Digital Out: the type 1 format for broadcasting stations, the type 2 form 1 format for home use, and the type 2 form 2 format for the manufacture of software.

The CXD3068Q supports type 2 form 1.

The channel status clock accuracy is automatically set to level II when using the crystal clock and to level III in CAV-W mode or variable pitch mode. In addition, Sub-Q data which are matched twice in succession after a CRC check are input to the first four bits (bits 0 to 3).

DOUT is output when the crystal is 34MHz and DSPB is set to 1 with XTSL high in CLV-N or CLV-W mode. Therefore, set MD2 to 0 and turn DOUT off.

Digital Out1 C bit

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	From sub Q				0	0	0	0	1	0	0	0	0	0	0	0
	ID0	ID1	COPY	Emph												
16	0	0	0	0	0	0	0	0	0	0	0	0	0	0/1	0	0
32																
48																
								0								
176																

bit0 to 3 Sub-Q control bits that matched twice with CRCOK

bit29 VPON or VARION: 1 X'tal 0

Table 4-5.

§ 4-6. Servo Auto Sequence

This function performs a series of controls, including auto focus and track jumps. When the auto sequence command is received from the CPU, auto focus, 1-track jump, 2N-track jump, fine search and M-track move are executed automatically.

The servo block operates according to the built-in program during the auto sequence execution (when XBUSY = low), so that commands from the CPU, that is $0, 1, 2 and 3 commands, are not accepted. ($4 to E commands are accepted.)

In addition, when using the auto sequence, turn the A.SEQ of register 9 on.

When CLOK goes from low to high while XBUSY is low, XBUSY does not become high for a maximum of 100µs after that point. This is to prevent the transfer of erroneous data to the servo when XBUSY changes from low to high by the monostable multivibrator, which is reset by CLOK being low (when XBUSY is low).

In addition, a MAX timer is built into this LSI as a countermeasure against abnormal operation due to external disturbances, etc. When the auto sequence command is sent from the CPU, this command assumes a $4XY format, in which X specifies the command and Y sets the MAX timer value and timer range. If the executed auto sequence command does not terminate within the set timer value, the auto sequence is interrupted (like $40). See [1] "$4X commands" concerning the timer value and range. Also, the MAX timer is invalidated by inputting $4X0.

Although this command is explained in the format of $4X in the following command descriptions, the timer value and timer range are actually sent together from the CPU.

(a) Auto focus ($47)

Focus search-up is performed, FOK and FZC are checked, and the focus servo is turned on.

If $47 is received from the CPU, the focus servo is turned on according to Fig. 4-6. The auto focus starts with focus search-up, and note that the pickup should be lowered beforehand (focus search-down). In addition, blind E of register 5 is used to eliminate FZC chattering. Concretely, the focus servo is turned on at the falling edge of FZC after FZC has been continuously high for a longer time than E.

(b) Track jump

1, 10 and 2N-track jumps are performed respectively. Always use this when the focus, tracking, and sled servos are on. Note that tracking gain-up and braking-on ($17) should be sent beforehand because they are not involved in this sequence.

- 1-track jump

  When $48 ($49 for REV) is received from the CPU, a FWD (REV) 1-track jump is performed in accordance with Fig. 4-7. Set blind A and brake B with register 5.

- 10-track jump

  When $4A ($4B for REV) is received from the CPU, a FWD (REV) 10-track jump is performed an accordance with Fig. 4-8. The principal difference from the 1-track jump is to kick the sled. In addition, after kicking the actuator, when 5 tracks have been counted through COUT, the brake is applied to the actuator. Then, when the actuator speed is found to have slowed up enough (determined by the COUT cycle becoming longer than the overflow C set with register 5), the tracking and sled servos are turned on.

• 2N-track jump

When $4C ($4D for REV) is received from the CPU, a FWD (REV) 2N-track jump is performed in accordance with Fig. 4-9. The track jump count N is set with register 7. Although N can be set to 2^{16} tracks, note that the setting is actually limited by the actuator. COUT is used for counting the number of jumps when N is less than 16, and MIRR is used with N is 16 or more.

Although the 2N-track jump basically follows the same sequence as the 10-track jump, the one difference is that after the tracking servo is turned on, the sled continues to move only for "D", set with register 6.

• Fine search

When $44 ($45 for REV) is received from the CPU, a FWD (REV) fine search (N-track jump) is performed in accordance with Fig. 4-10. The differences from a 2N-track jump are that a higher precision is achieved by controlling the traverse speed, and a longer distance jump is achieved by controlling the sled. The track jump count is set with register 7. N can be set to 2^{16} tracks. After kicking the actuator and sled, the traverse speed is controlled based on the overflow G. Set kick D and F with register 6 and overflow G with register 5. Also, sled speed control during traverse can be turned off by causing COMP to fall. Set the number of tracks during which COMP falls with register B. After N tracks have been counted through COUT, the brake is applied to the actuator and sled. (This is performed by turning on the tracking servo for the actuator, and by kicking the sled in the opposite direction during the time for kick D set with register 6.) Then, the tracking and sled servos are turned on.

Set overflow G to the speed required to slow up just before the track jump terminates. (The speed should be such that it will come on-track when the tracking servo turns on at the termination of the track jump.) For example, set the target track count N – α for the traverse monitor counter which is set with register B, and COMP will be monitored. When the falling edge of this COMP is detected, overflow G can be reset.

• M-track move

When $4E ($4F for REV) is received from the CPU, a FWD (REV) M-track move is performed in accordance with Fig. 4-11. M can be set to 2^{16} tracks. Like the 2N-track jump, COUT is used for counting the number of moves when M is less than 16, and MIRR is used when M is 16 or more. The M-track move is executed by moving only the sled, and is therefore suited for moving across several thousand to several ten-thousand tracks. In addition, the track and sled servos are turned off after M tracks have been counted through COUT or MIRR unlike for the other jumps. Transfer $25 from the microcomputer after the actuator has stabilized.

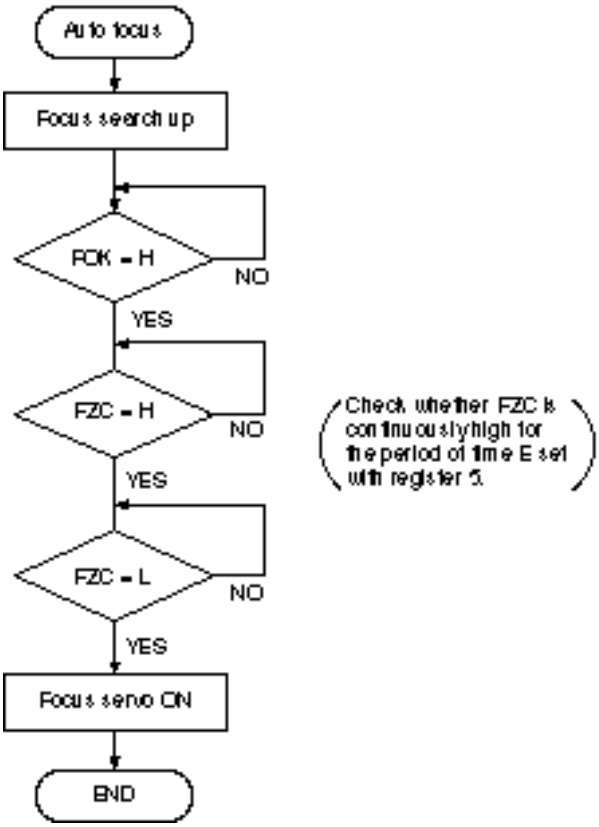


Fig. 4-6-(a). Auto Focus Flow Chart

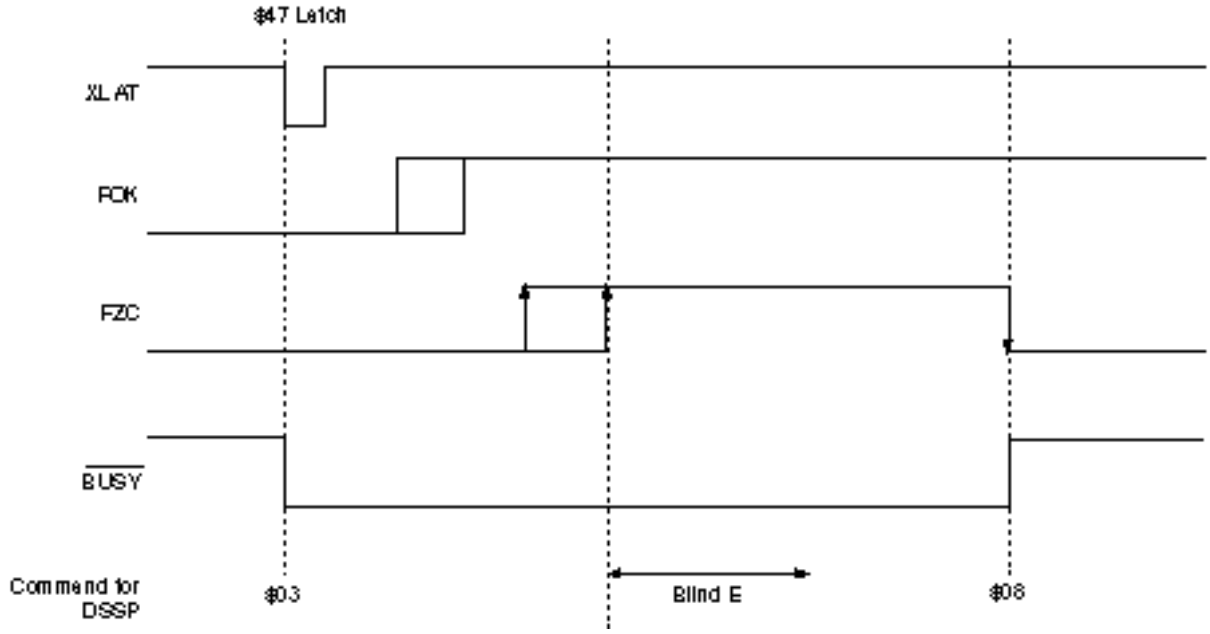


Fig. 4-6-(b). Auto Focus Timing Chart

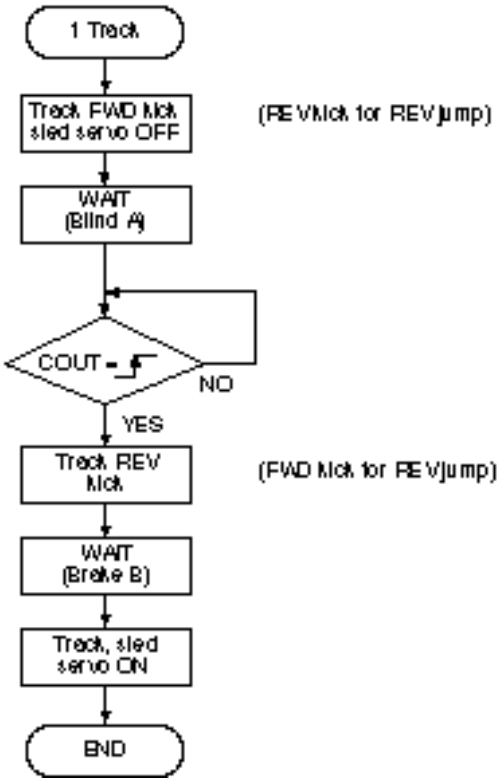


Fig. 4-7-(a). 1-Track Jump Flow Chart

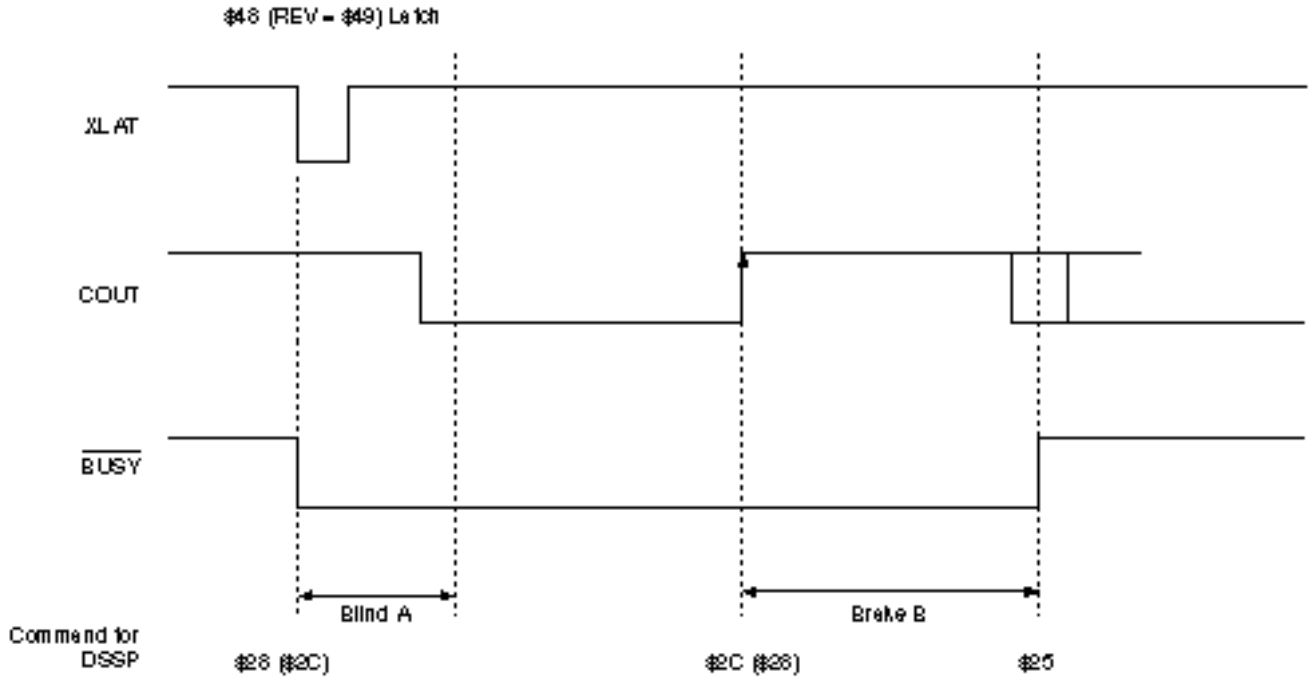


Fig. 4-7-(b). 1-Track Jump Timing Chart

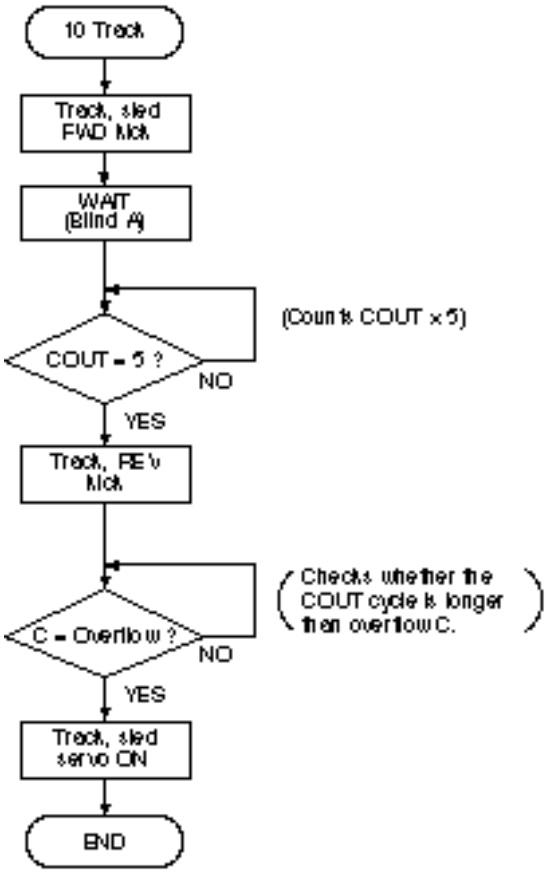


Fig. 4-8-(a). 10-Track Jump Flow Chart

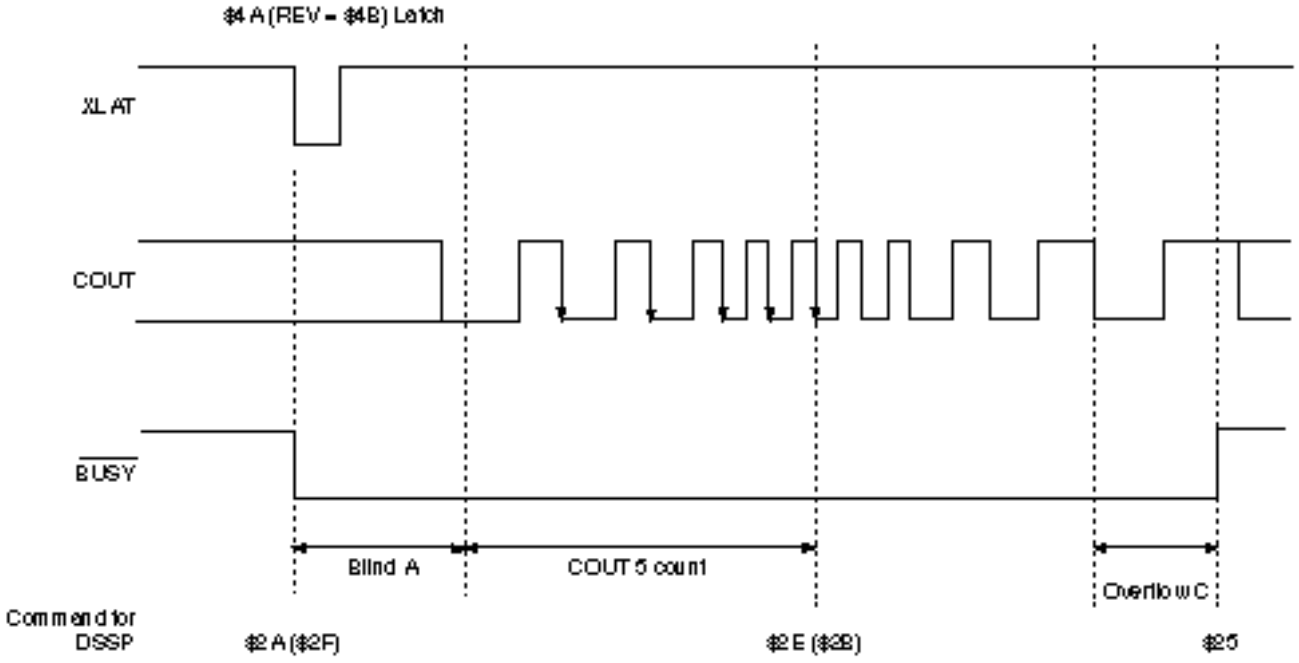


Fig. 4-8-(b). 10-Track Jump Timing Chart

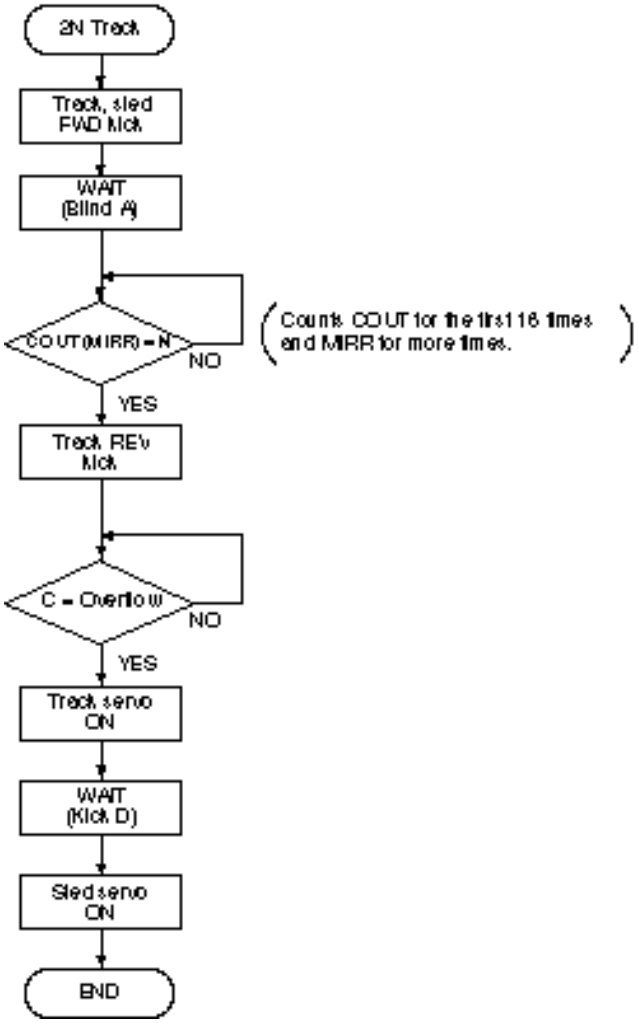


Fig. 4-9-(a). 2N-Track Jump Flow Chart

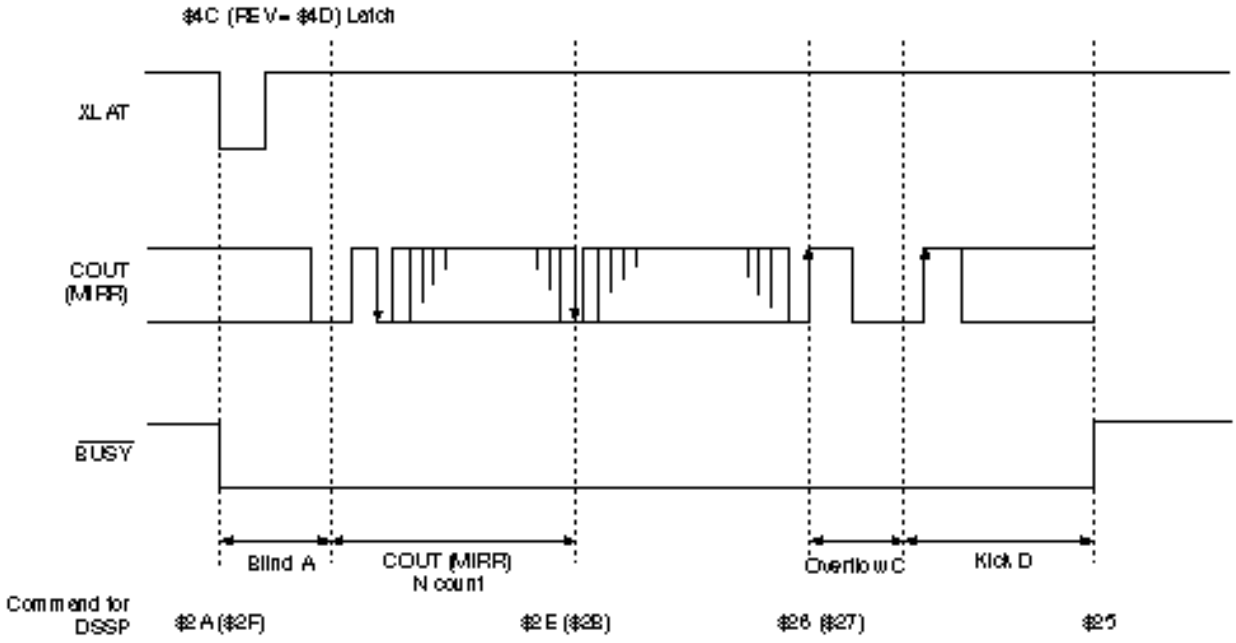


Fig. 4-9-(b). 2N-Track Jump Timing Chart

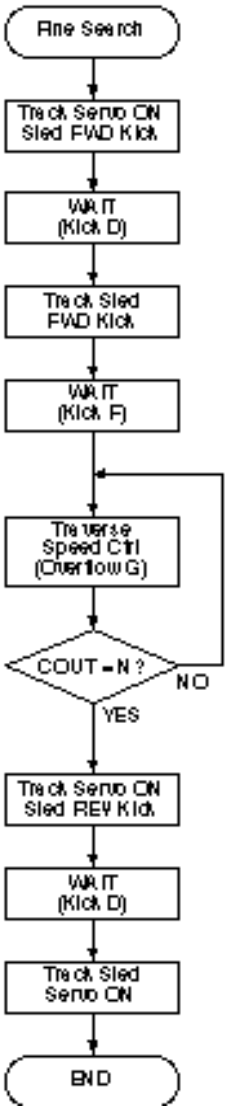


Fig. 4-10-(a). Fine Search Flow Chart

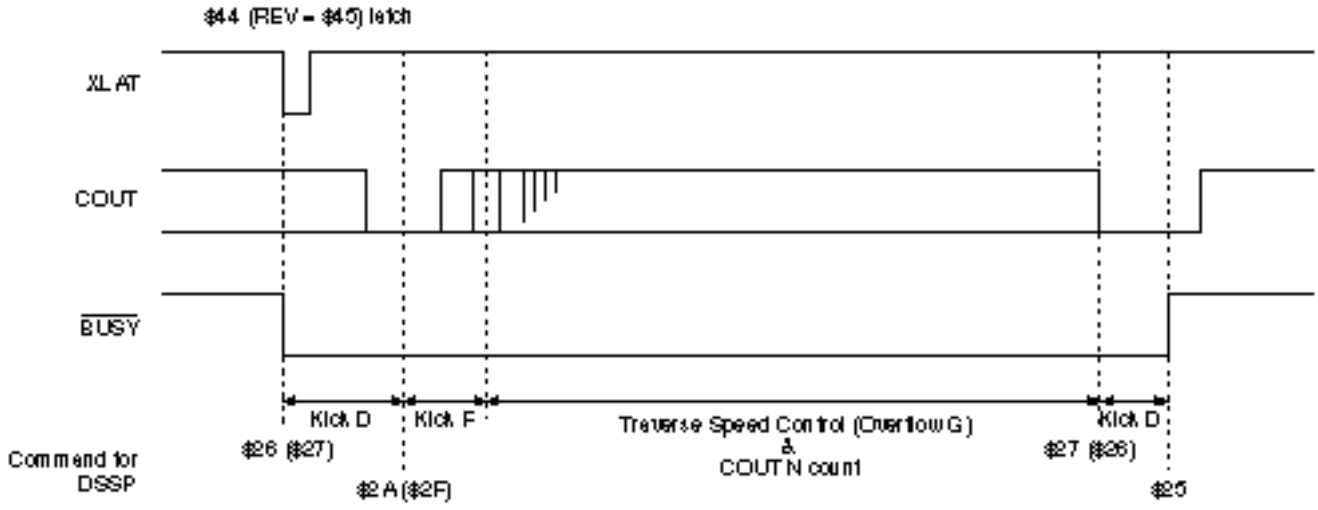


Fig. 4-10-(b). Fine Search Timing Chart

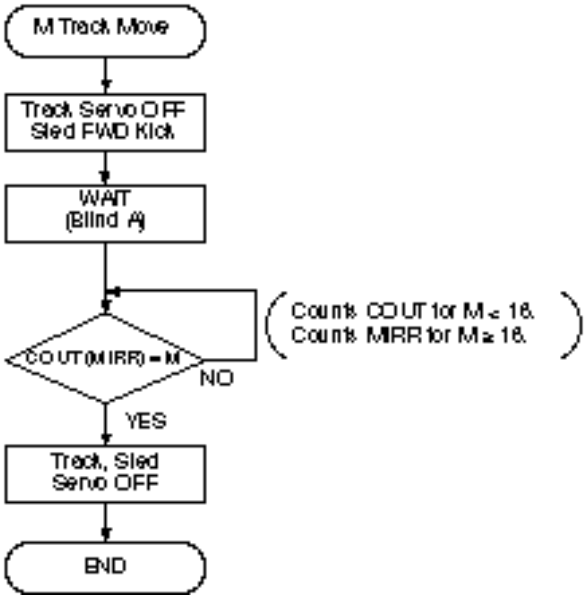


Fig. 4-11-(a). M-Track Move Flow Chart

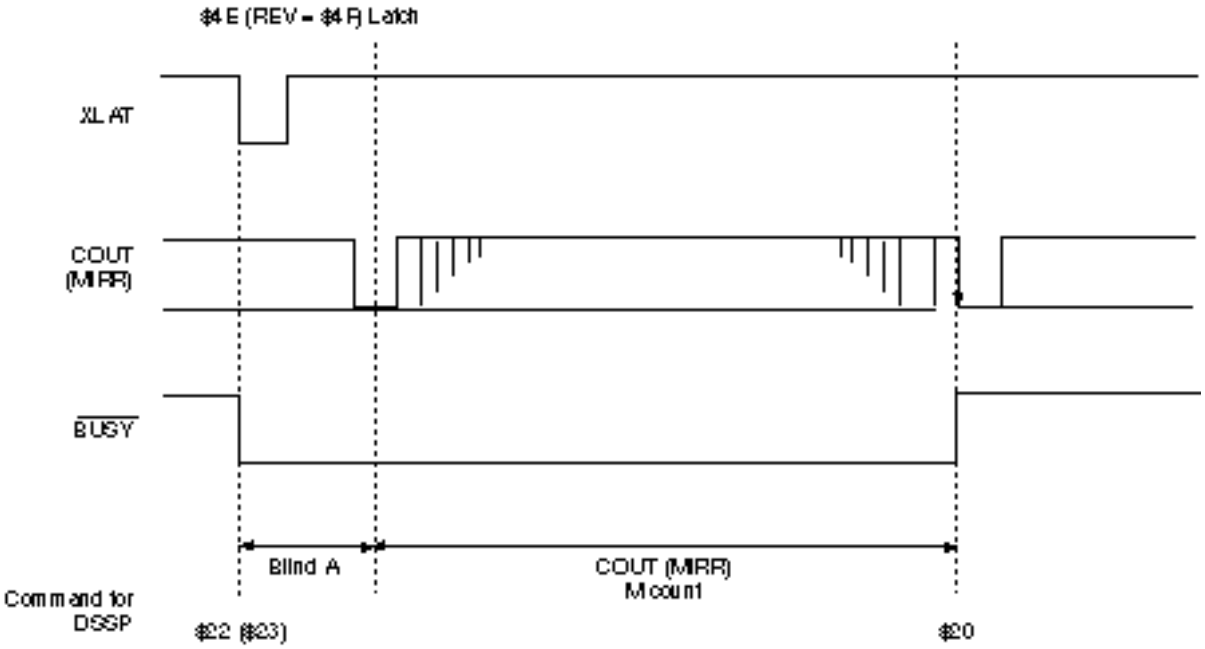
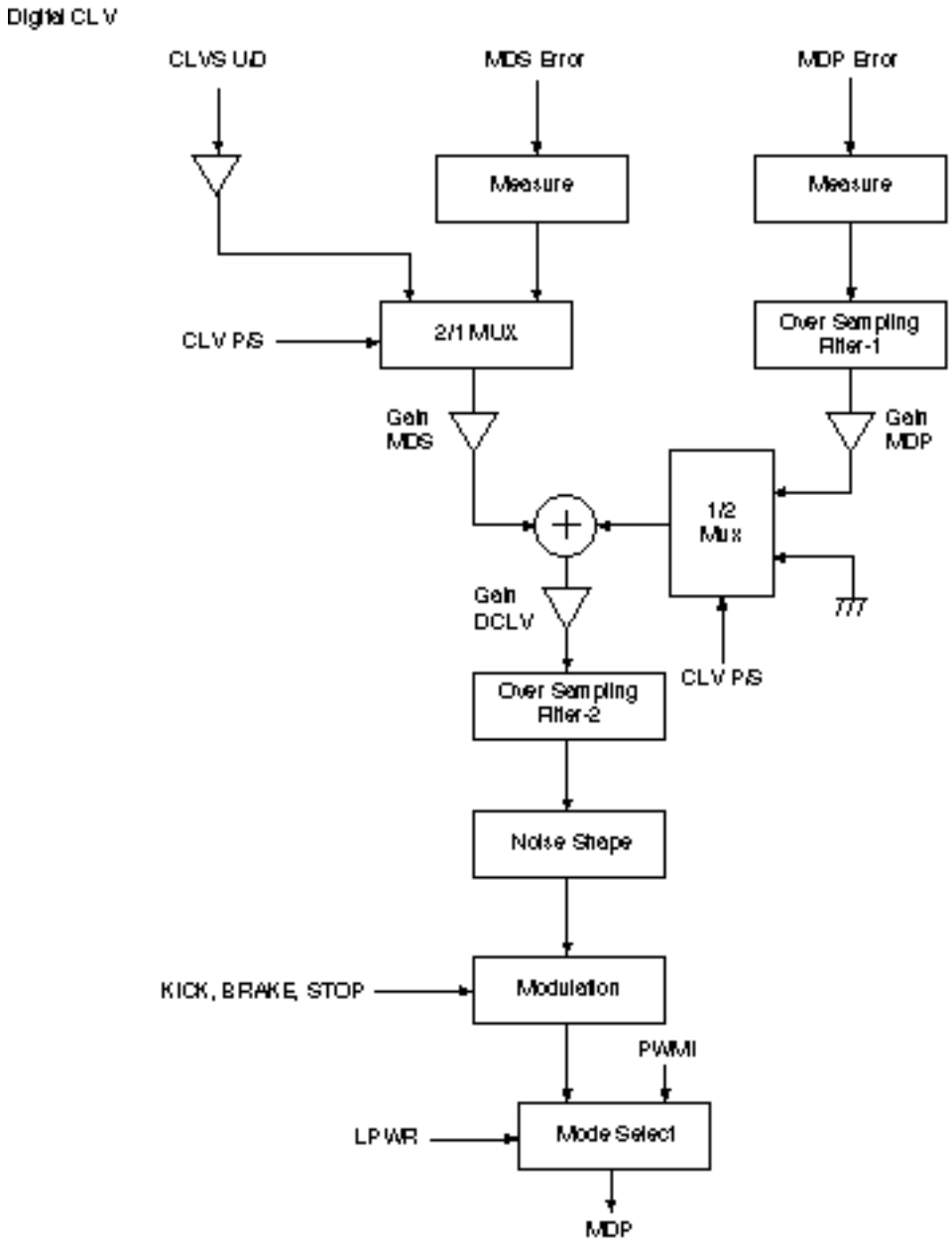


Fig. 4-11-(b). M-Track Move Timing Chart

§ 4-7. Digital CLV

Fig. 4-12 shows the block diagram. Digital CLV outputs MDS error and MDP error signals with PWM, with the sampling frequency increased up to 130kHz during normal-speed playback in CLVS, CLVP and other modes. In addition, the digital spindle servo gain is variable.



CLVS U/D: Up/down signal from CLVS servo

MDS error: Frequency error for CLVP servo

MDP error: Phase error for CLVP servo

PWMI: Spindle drive signal from the microcomputer for CAV servo

Fig. 4-12. Block Diagram

§ 4-8. Playback Speed

In the CXD3068Q, the following playback modes can be selected through different combinations of XTAI, XTSL pin, double-speed command (DSPB), VCO1 selection command (VCOSEL1), VCO1 frequency division commands (KSL3, KSL2) and command transfer rate selector (ASHS) in CLV-N or CLV-W mode.

Mode	XTAI	XTSL	DSPB	VCOSEL1*1	ASHS	Playback speed	Error correction*2
1	768Fs	1	0	0/1	0	1×	C1: double; C2: quadruple
2	768Fs	1	1	0/1	0	2×	C1: double; C2: double
3	768Fs	0	0	1	1	2×	C1: double; C2: quadruple
4	768Fs	0	1	1	1	4×	C1: double; C2: double
5	384Fs	0	0	0/1	0	1×	C1: double; C2: quadruple
6	384Fs	0	1	0/1	0	2×	C1: double; C2: double
7	384Fs	1	1	0/1	0	1×	C1: double; C2: double

*1 Actually, the optimal value should be used together with KSL3 and KSL2.

*2 When $8 ERC4 = 1, C2 is for quadruple correction with DSPB = 1.

The playback speed can be varied by setting VP0 to VP7 in CAV-W mode. See "[3] Description of Modes" for details.

§ 4-9. Asymmetry Correction

Fig. 4-13 shows the block diagram and circuit example.

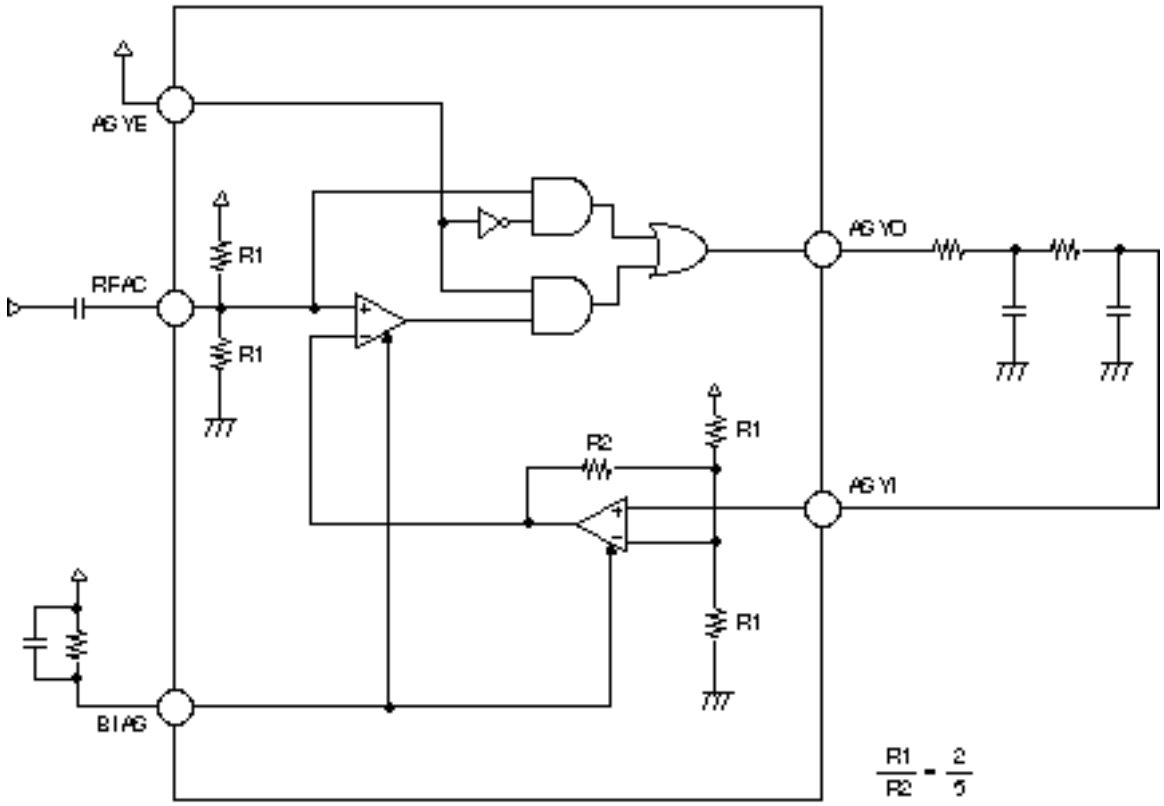


Fig. 4-15. Asymmetry Correction Application Circuit

§4-10. CD TEXT Data Demodulation

- In order to demodulate the CD TEXT data, set the command $8 Data 6 D3 TXON to 1. During TXON = 1, connect EXCK to low and do not use the data output from SBSO because the CD TEXT demodulation circuit uses EXCK and the SBSO pin exclusively.
  It requires 26.7ms (max.) to demodulate the CD TEXT data correctly after TXON is set to 1.
- The CD TEXT data is output by switching the SQSO pin with the command. The CD TEXT data output is enabled by setting the command $8 Data 6 D2 TXOUT to 1. To read data, the readout clock should be input to SQCK.
- The readable data are the CRC counting results for the each pack and the CD TEXT data (16 bytes) except for CRC data.
- When the CD TEXT data is read, the order of the MSB and LSB is inverted within each byte. As a result, although the sequence of the bytes is the same, the bits within the bytes are now ordered LSB first.
- Data which can be stored in the LSI is 1 packet (4 packs).

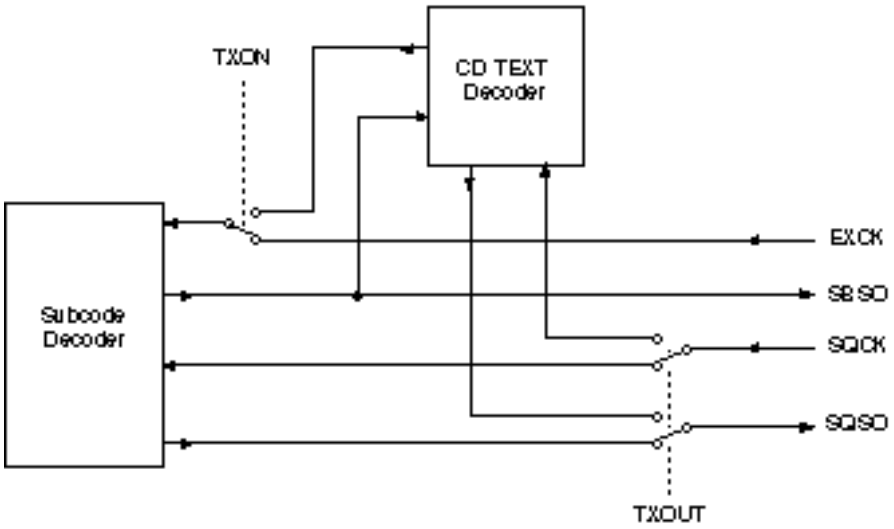


Fig. 4-14. Block Diagram of CD TEXT Demodulation Circuit

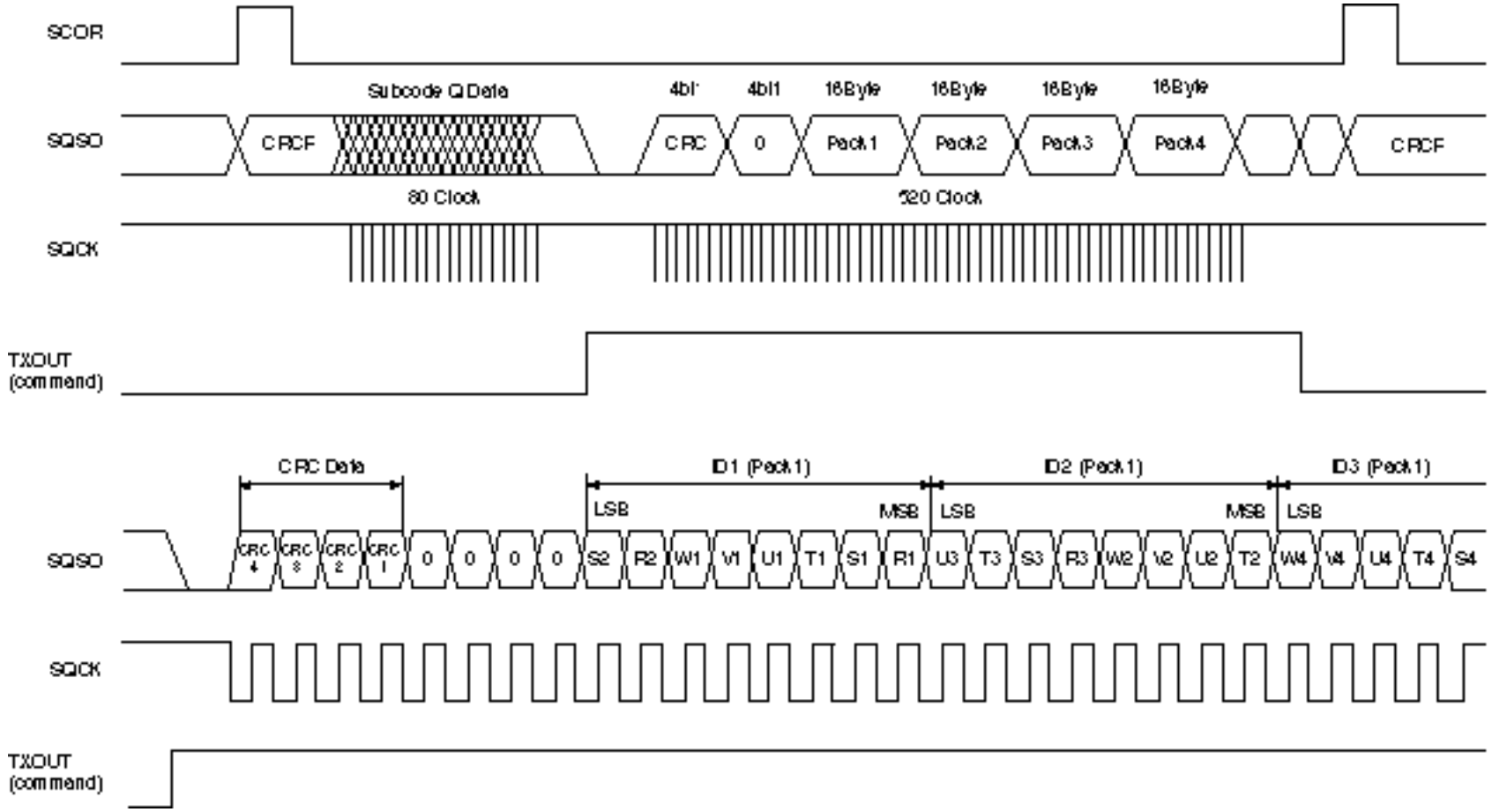


Fig. 4-15. CD TEXT Data Timing Chart

[5] Description of Servo Signal Processing System Functions and Commands

§5-1. General Description of Servo Signal Processing System (V_{DD}: Supply voltage)

Focus servo

Sampling rate:	88.2kHz (when MCK = 128Fs)
Input range:	1／4V_{DD} to 3／4V_{DD}
Output format:	7-bit PWM
Other:	Offset cancel
	Focus bias adjustment
	Focus search
	Gain-down function
	Defect countermeasure
	Auto gain control

Tracking servo

Sampling rate:	88.2kHz (when MCK = 128Fs)
Input range:	1／4V_{DD} to 3／4V_{DD}
Output format:	7-bit PWM
Other:	Offset cancel
	E:F balance adjustment
	Track jump
	Gain-up function
	Defect countermeasure
	Drive cancel
	Auto gain control
	Vibration countermeasure

Sled servo

Sampling rate:	345Hz (when MCK = 128Fs)
Input range:	1／4V_{DD} to 3／4V_{DD}
Output format:	7-bit PWM
Other:	Sled move

FOK, MIRR, DFCT signal generation

RF signal sampling rate:	1.4MHz (when MCK = 128Fs)
Input range:	1／4V_{DD} to 3／4V_{DD}
Other:	RF zero level automatic measurement

§5-2. Digital Servo Block Master Clock (MCK)

The clock with the 2/3 frequency of the crystal is supplied to the digital servo block.

XT4D and XT2D are $3F commands, and XT1D is $3E command. (Default = 0)

The digital servo block is designed with an MCK frequency of 5.6448MHz (128Fs) as typical.

Mode	XTAI	FSTO	XTSL	XT4D	XT2D	XT1D	Frequency division ratio	MCK
1	384Fs	256Fs	*	*	*	1	1	256Fs
2	384Fs	256Fs	*	*	1	0	1/2	128Fs
3	384Fs	256Fs	0	0	0	0	1/2	128Fs
4	768Fs	512Fs	*	*	*	1	1	512Fs
5	768Fs	512Fs	*	*	1	0	1/2	256Fs
6	768Fs	512Fs	*	1	0	0	1/4	128Fs
7	768Fs	512Fs	1	0	0	0	1/4	128Fs

Fs = 44.1kHz, *: Don't care

Table 5-1.

§ 5-3. DC Offset Cancel [AVRG (Average) Measurement and Compensation] (See Fig. 5-3.)

The CXD3068Q can measure the average of RFDC, VC, FE and TE and compensate these signals using the measurement results to control the servo effectively. This AVRG measurement and compensation is necessary to initialize the CXD3068Q, and is able to cancel the DC offset.

AVRG measurement takes the levels applied to the VC, FE, RFDC and TE pins as the digital average of 256 samples, and then loads these values into each AVRG register.

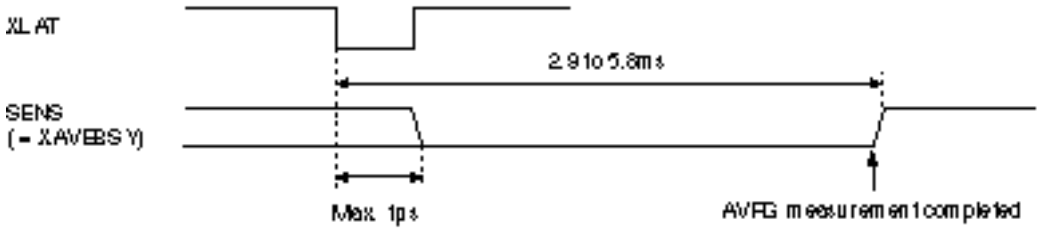
The AVRG measurement commands are D15 (VCLM), D13 (FLM), D11 (RFLM) and D4 (TLM) of $38.

Measurement is on when the respective command is set to 1.

AVRG measurement requires approximately 2.9ms to 5.8ms (when MCK = 128Fs) after the command is received.

The completion of AVRG measurement operation can be monitored by the SENS pin. (See Timing Chart 5-2.)

Monitoring requires that the upper 8 bits of the command register are 38 (Hex).



Timing Chart 5-2.

<Measurement>

VC AVRG: The VC DC offset (VC AVRG) which is the center voltage for the system is measured and used to compensate the FE, TE and SE signals.

FE AVRG: The FE DC offset (FE AVRG) is measured and used to compensate the FE and FZC signals.

TE AVRG: The TE DC offset (TE AVRG) is measured and used to compensate the TE and SE signals.

RF AVRG: The RF DC offset (RF AVRG) is measured and used to compensate the RFDC signal.

<Compensation>

RFLC: (RF signal – RF AVRG) is input to the RF In register.
"00" is input when the RF signal is lower than RF AVRG.

TLC0: (TE signal – VC AVRG) is input to the TRK In register.

TLC1: (TE signal – TE AVRG) is input to the TRK In register.

VCLC: (FE signal – VC AVRG) is input to the FCS In register.

FLC1: (FE signal – FE AVRG) is input to the FCS In register.

FLC0: (FE signal – FE AVRG) is input to the FZC register.

Two methods of canceling the DC offset are assumed for the CXD3068Q. These methods are shown in Figs. 5-3a and 5-3b.

An example of AVRG measurement and compensation commands is shown below.

$38 08 00 (RF AVRG measurement)

$38 20 00 (FE AVRG measurement)

$38 00 10 (TE AVRG measurement)

$38 14 0A (Compensation on [RFLC, FLC0, FLC1, TLC1], corresponds to Fig. 5-3a.)

See the description of $38 for these commands.

§ 5-4. E:F Balance Adjustment Function (See Fig. 5-3.)

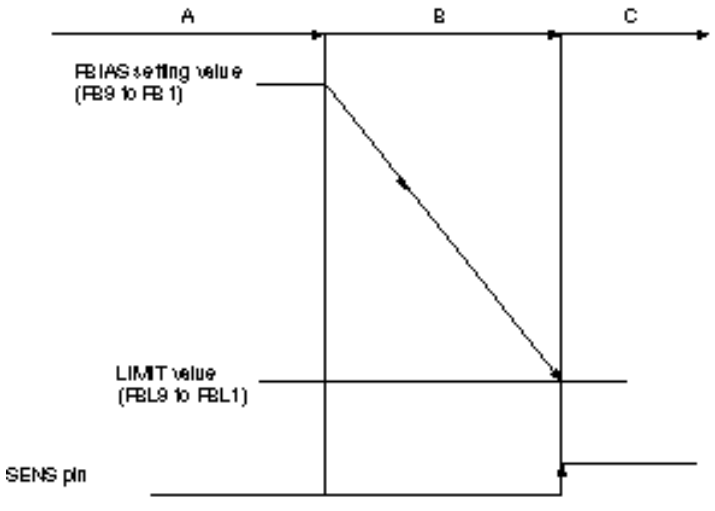
When the disc is rotated with the laser on, and with the FCS (focus) servo on via FCS Search (focus search), the traverse waveform appears in the TE signal due to disc eccentricity.
In this condition, the low-frequency component can be extracted from the TE signal using the built-in TRK hold filter by setting D5 (TBLM) of $38 to 1.
The extracted low-frequency component is loaded into the TRVSC register as a digital value, and the TRVSC register value is established when TBLM returns to "0".
Next, setting D2 (TLC2) of $38 to 1 compensates the values obtained from the TE and SE input pins with the TRVSC register value (subtraction), allowing the E:F balance offset to be adjusted. (See Fig. 5-3.)

§ 5-5. FCS Bias (Focus Bias) Adjustment Function

The FBIAS register value can be added to the FCS servo filter input by setting D14 (FBON) of $3A to 1. (See Fig. 5-3.)
When D11 = 0 and D10 = 1 is set by $34F, the FBIAS register value can be written using the 9-bit value of D9 to D1 (D9: MSB).
In addition, the RF jitter can be monitored by setting the $8 command SOCT to 1. (See "DSP Block Timing Chart".)

The FBIAS register can be used as a counter by setting D13 (FBSS) of $3A to 1. The FBIAS register functions as an up counter when D12 (FBUP) of $3A = 1, and as a down counter when D12 (FBUP) of $3A = 0.
The number of up and down steps can be changed by setting D11 and D10 (FBV1 and FBV0) of $3A.

When using the FBIAS register as a counter, the counter stops when the value set beforehand in FBL9 to FBL1 of $34 matches the FCSBIAS value. Also, if the upper 8 bits of the command register are $3A at this time, SENS goes to high and the counter stop can be monitored.



Here, assume the FBIAS setting value FB9 to FB1 and the FBIAS LIMIT value FBL9 to FBL1 are set in status A. For example, if command registers FBUP = 0, FBV1 = 0, FBV0 = 0 and FBSS = 1 are set from this status, down count starts from status A and approaches the set LIMIT value. When the LIMIT value is reached and the FBIAS value matches FBL9 to FBL1, the counter stops and the SENS pin goes to high. Note that the up/down counter counts at each sampling cycle of the focus servo filter. The number of steps by which the count value changes can be selected from 1, 2, 4 or 8 steps by FBV1 and FBV0. When converted to FE input, 1 step corresponds to $1/512 \times V_{DD} \times 0.4$.

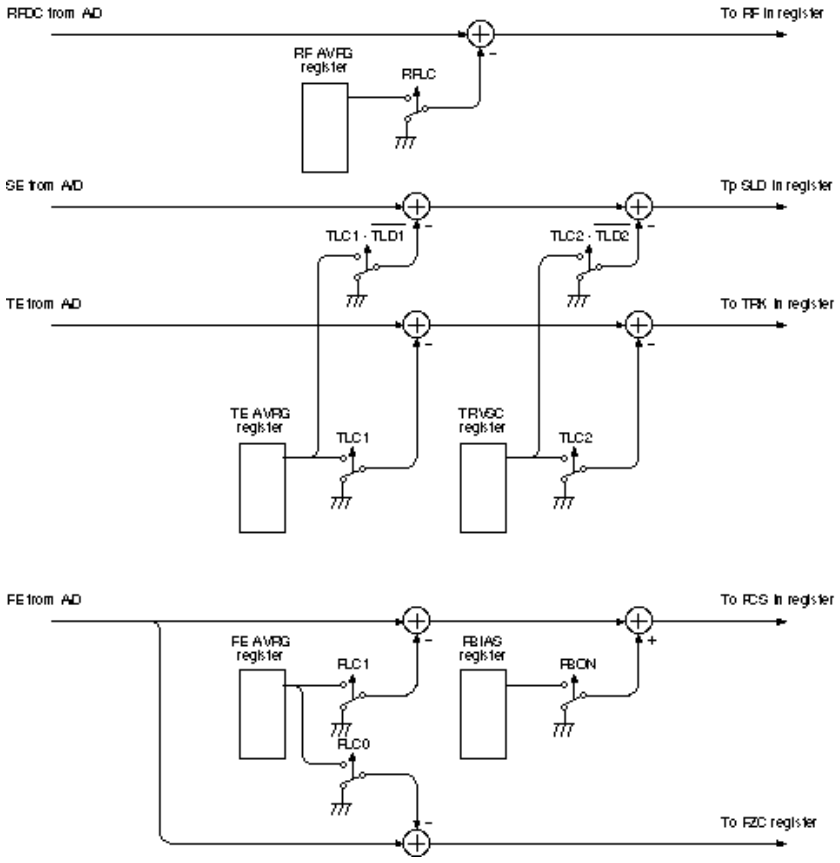


Fig. 5-3a.

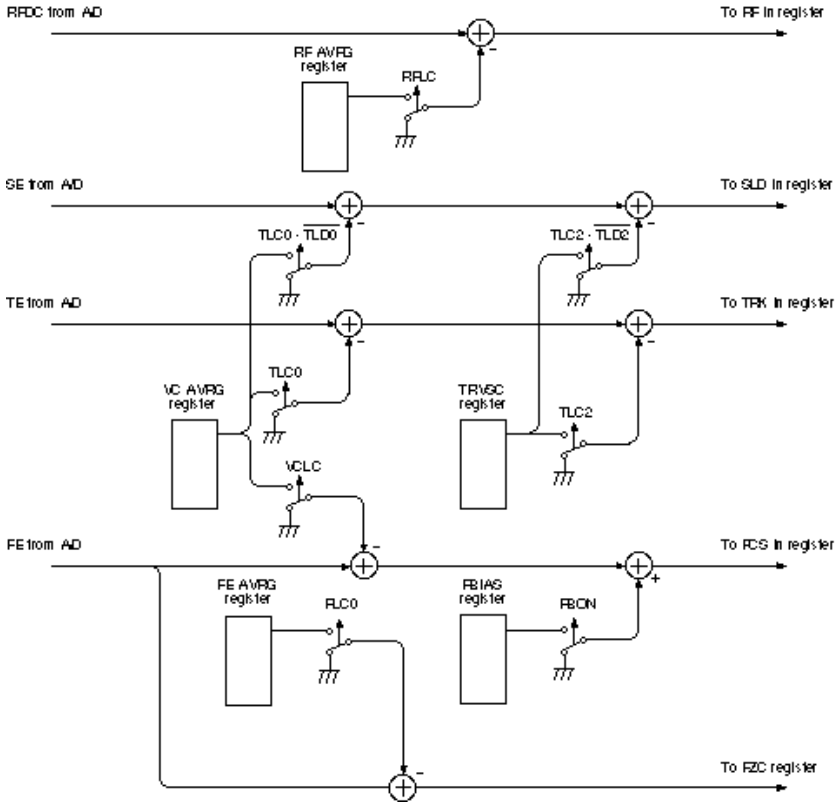


Fig. 5-3b.

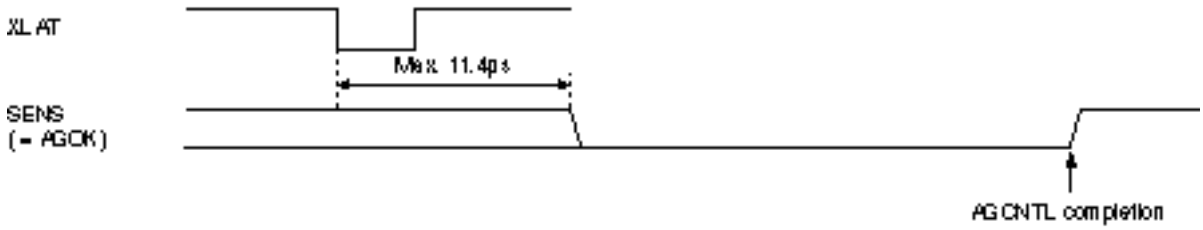
§ 5-6. AGCNTL (Automatic Gain Control) Function

The AGCNTL function automatically adjusts the filter internal gain in order to obtain the appropriate servo loop gain. AGCNTL not only copes with the sensitivity variation of the actuator and photo diode, etc., but also obtains the optimal gain for each disc.

The AGCNTL command is sent when each servo is turned on. During AGCNTL operation, if the upper 8 bits of the command register are 38 (Hex), the completion of AGCNTL operation can be confirmed by monitoring the SENS pin. (See Timing Chart 5-4 and "Description of SENS Signals".)

Setting D9 and D8 of $38 to 1 set FCS (focus) and TRK (tracking) respectively to AGCNTL operation.

Note) During AGCNTL operation, each servo filter gain must be normal, and the anti-shock circuit (described hereafter) must be disabled.



Timing Chart 5-4.

Coefficient K13 changes for AGF (focus AGCNTL) and coefficients K23 and K07 change for AGT (tracking AGCNTL) due to AGCNTL.

These coefficients change from 01 to 7F (Hex), and they must also be set within this range when written externally.

After AGCNTL operation has completed, these coefficient values can be confirmed by reading them out from the SENS pin with the serial readout function (described hereafter).

AGCNTL related settings

The following settings can be changed with $35, $36 and $37.

FG6 to FG0; AGF convergence gain setting, effective setting range: 00 to 57 (Hex)

TG6 to TG0; AGT convergence gain setting, effective setting range: 00 to 57 (Hex)

AGS; Self-stop on/off

AGJ; Convergence completion judgment time

AGGF; Internally generated sine wave amplitude (AGF)

AGGT; Internally generated sine wave amplitude (AGT)

AGV1; AGCNTL sensitivity 1 (during rough adjustment)

AGV2; AGCNTL sensitivity 2 (during fine adjustment)

AGHS; Rough adjustment on/off

AGHT; Fine adjustment time

Note) Converging servo loop gain values can be changed with the FG6 to FG0 and TG6 to TG0 setting values. In addition, these setting values must be within the effective setting range. The default settings aim for 0dB at 1kHz. However, since convergence values vary according to the characteristics of each constituent element of the servo loop, FG and TG values should be set as necessary.

AGCNTL and default operation have two stages.
In the first stage, rough adjustment is performed with high sensitivity for a certain period of time (select 256/128ms with AGHT, when MCK = 128Fs), and the AGCNTL coefficient approaches the appropriate value. The sensitivity at this time can be selected from two types with AGV1.
In the second stage, the AGCNTL coefficient is finely adjusted with relatively low sensitivity to further approach the appropriate value. The sensitivity for the second stage can be selected from two types with AGV2. In the second stage of default operation, when the AGCNTL coefficient reaches the appropriate value and stops changing, the CXD3068Q confirms that the AGCNTL coefficient has not changed for a certain period of time (select 63/31ms with AGHJ, when MCK = 128Fs), and then completes AGCNTL operation. (Self stop mode)
This self-stop mode can be canceled by setting AGS to 0.
In addition, the first stage is omitted for AGCNTL operation when AGHS is set to 0.
An example of AGCNTL coefficient transitions during AGCNTL operation with various settings is shown in Fig. 5-5.

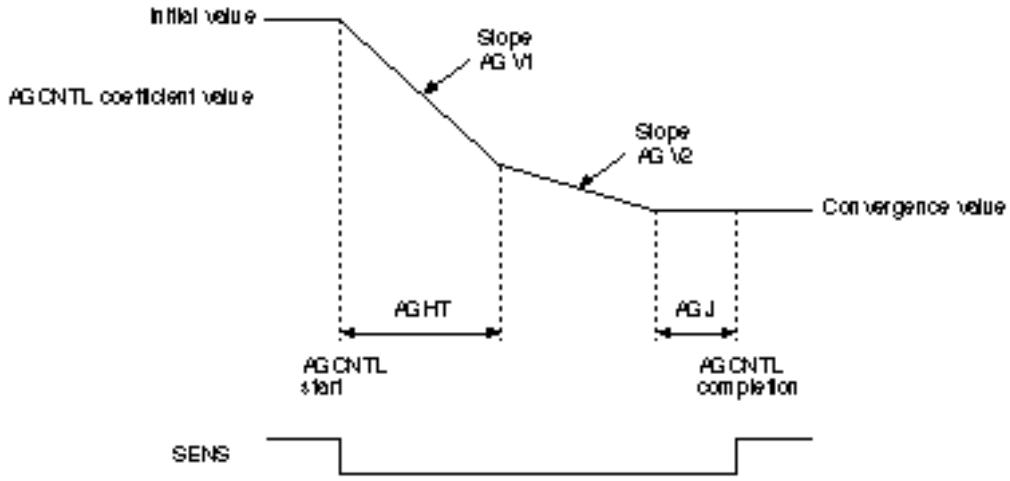


Fig. 5-5.

Note) Fig. 5-5 shows the case where the AGCNTL coefficient converges from the initial value to a smaller value.

§ 5-7. FCS Servo and FCS Search (Focus Search)

The FCS servo is controlled by the 8-bit serial command $0X. (See Table 5-6.)

Register name	Command	D23 to D20	D19 to D16	
0	FOCUS CONTROL	0 0 0 0	1 0 ∗ ∗	FOCUS SERVO ON (FOCUS GAIN NORMAL)
			1 1 ∗ ∗	FOCUS SERVO ON (FOCUS GAIN DOWN)
			0 ∗ 0 ∗	FOCUS SERVO OFF, 0V OUT
			0 ∗ 1 ∗	FOCUS SERVO OFF, FOCUS SEARCH VOLTAGE OUT
			0 ∗ 1 0	FOCUS SEARCH VOLTAGE DOWN
			0 ∗ 1 1	FOCUS SEARCH VOLTAGE UP

∗: Don't care

Table 5-6.

FCS Search

FCS search is required in the course of turning on the FCS servo.

Fig. 5-7 shows the signals for sending commands $00 → $02 → $03 and performing only FCS search operation.
Fig. 5-8 shows the signals for sending $08 (FCS on) after that.

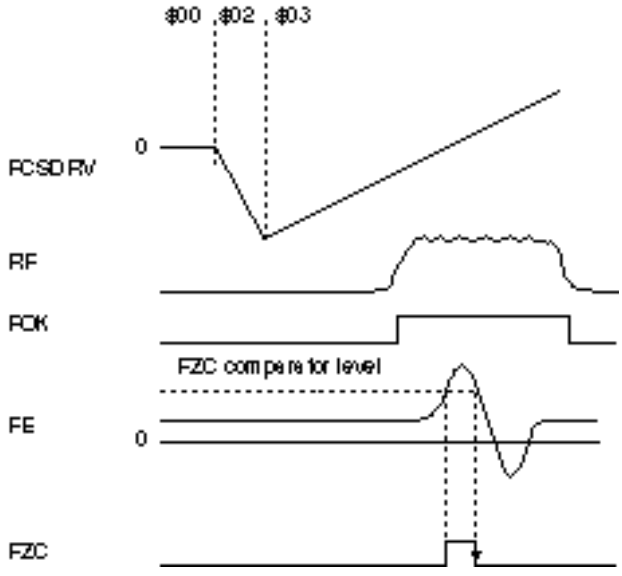


Fig. 5-7.

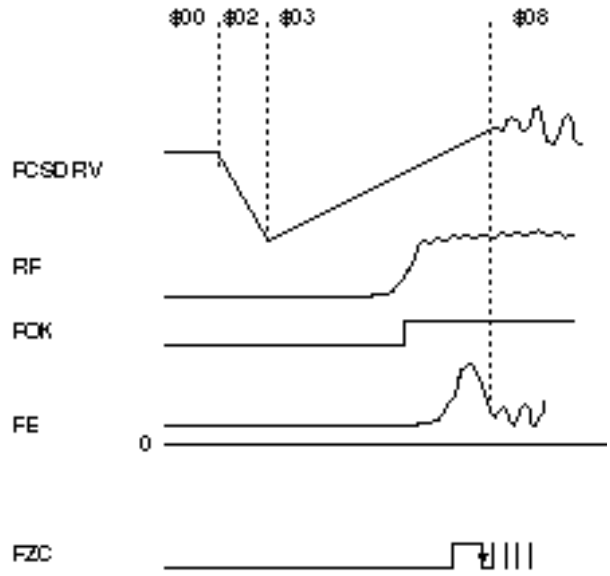


Fig. 5-8.

§ 5-8. TRK (Tracking) and SLD (Sled) Servo Control

The TRK and SLD servos are controlled by the 8-bit command $2X. (See Table 5-9.)
When the upper 4 bits of the serial data are 2 (Hex), TZC is output to the SENS pin.

Register name	Command	D23 to D20	D19 to D16	
2	TRACKING MODE	0 0 1 0	0 0 ∗ ∗	TRACKING SERVO OFF
			0 1 ∗ ∗	TRACKING SERVO ON
			1 0 ∗ ∗	FORWARD TRACK JUMP
			1 1 ∗ ∗	REVERSE TRACK JUMP
			∗ ∗ 0 0	SLED SERVO OFF
			∗ ∗ 0 1	SLED SERVO ON
			∗ ∗ 1 0	FORWARD SLED MOVE
			∗ ∗ 1 1	REVERSE SLED MOVE

Table 5-9. ∗: Don't care

TRK Servo

The TRK JUMP (track jump) level can be set with 6 bits (D13 to D8) of $36.
In addition, when the TRK servo is on and D17 of $1 is set to 1, the TRK servo filter switches to gain-up mode. The filter also switches to gain-up mode when the LOCK signal goes low or when vibration is detected with the anti-shock circuit (described hereafter) enabled.
The CXD3068Q has 2 types of gain-up filter structures in TRK gain-up mode which can be selected by setting D16 of $1. (See Table 5-17.)

SLD Servo

The SLD MOV (sled move) output, composed of a basic value from 6 bits (D13 to D8) of $37, is determined by multiplying this value by 1×, 2×, 3×, or 4× magnification set using D17 and D16 when D18 = D19 = 0 is set with $3. (See Table 5-10.)
SLD MOV must be performed continuously for 50µs or more. In addition, if the LOCK input signal goes low when the SLD servo is on, the SLD servo turns off.

Note) When the LOCK signal is low, the TRK servo switches to gain-up mode and the SLD servo is turned off. These operations are disabled by setting D6 (LKSW) of $38 to 1.

Register name	Command	D23 to D20	D19 to D16	
3	SELECT	0 0 1 1	0 0 0 0	SLED KICK LEVEL (basic value × ±1)
			0 0 0 1	SLED KICK LEVEL (basic value × ±2)
			0 0 1 0	SLED KICK LEVEL (basic value × ±3)
			0 0 1 1	SLED KICK LEVEL (basic value × ±4)

Table 5-10.

§ 5-9. MIRR and DFCT Signal Generation

The RF signal obtained from the RFDC pin is sampled at approximately 1.4MHz (when MCK = 128Fs) and loaded. The MIRR and DFCT signals are generated from this RF signal.

MIRR Signal Generation

The loaded RF signal is applied to peak hold and bottom hold circuits.
An envelope is generated from the waveforms generated in these circuits, and the MIRR comparator level is generated from the average of this envelope waveform.
The MIRR signal is generated by comparing the waveform generated by subtracting the bottom hold value from the peak hold value with this MIRR comparator level. (See Fig. 5-11.)
The bottom hold speed and mirror sensitivity can be selected from 4 values using D7 and D6, and D5 and D4, respectively, of $3C.

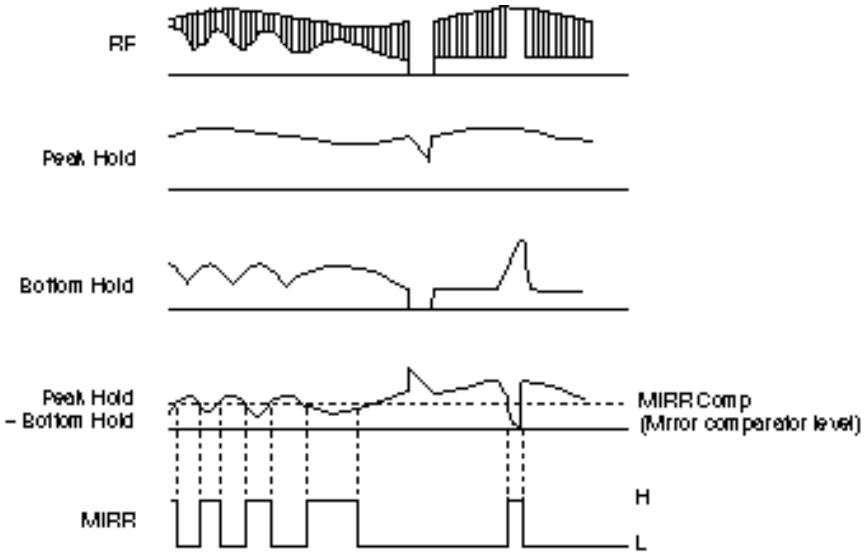


Fig. 5-11.

DFCT Signal Generation

The loaded RF signal is input to two peak hold circuits with different time constants, and the DFCT signal is generated by comparing the difference between these two peak hold waveforms with the DFCT comparator level. (See Fig. 5-12.)
The DFCT comparator level can be selected from four values using D13 and D12 of $3B.

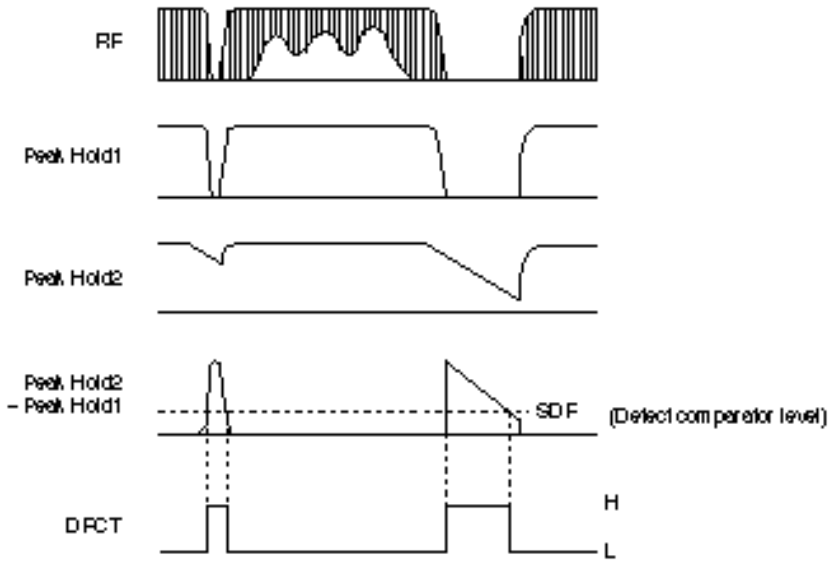


Fig. 5-12.

§ 5-10. DFCT Countermeasure Circuit

The DFCT countermeasure circuit maintains the directionality of the servo so that the servo does not become easily dislocated due to scratches or defects on discs.

Specifically, these operations are achieved by detecting scratches and defects with the DFCT signal generation circuit, and when DFCT goes high, applying the low frequency component of the error signal before DFCT went high to the FCS and TRK servo filter inputs. (See Fig. 5-13.)

In addition, these operations are activated by the default. They can be disabled by setting D7 (DFSW) of $38 to 1.

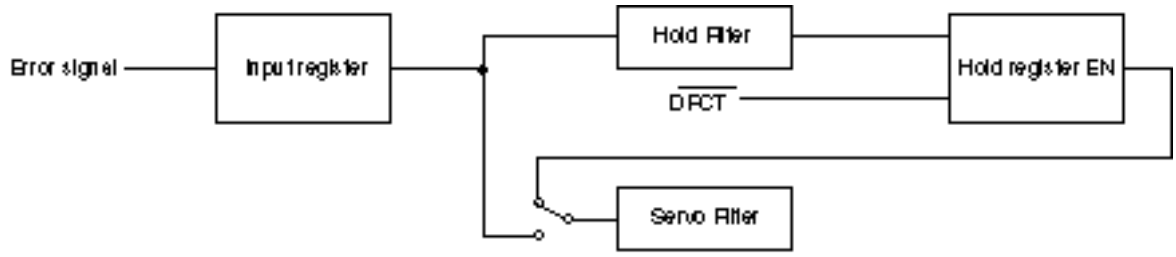


Fig. 5-13.

§ 5-11. Anti-Shock Circuit

When vibrations occur in the CD player, this circuit forces the TRK filter to switch to gain-up mode so that the servo does not become easily dislocated. This circuit is for systems which require vibration countermeasures.

Concretely, vibrations are detected using an internal anti-shock filter and comparator circuit, and the gain is increased. (See Fig. 5-14.)

The comparator level is fixed to 1/16 of the maximum comparator input amplitude. However, the comparator level is practically variable by adjusting the value of the anti-shock filter output coefficient K35.

This function can be turned on and off by D19 of $1 when the brake circuit (described hereafter) is off. (See Table 5-17.)

This circuit can also support an external vibration detection circuit, and can set the TRK servo filter to gain-up mode by inputting high level to the ATSK pin.

When the upper 4 bits of the command register are 1 (Hex), vibration detection can be monitored from the SENS pin.

It also can be monitored from the ATSK pin by setting the ASOT command of $3F to 0.

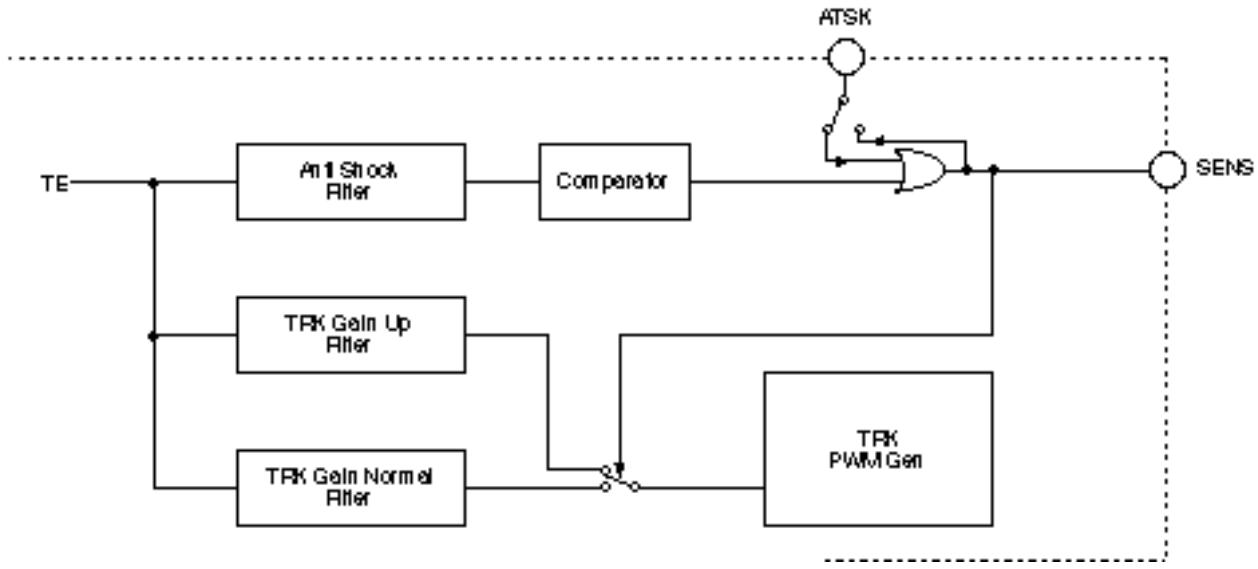


Fig. 5-14.

§ 5-12. Brake Circuit

Immediately after a long distance track jump it tends to be hard for the actuator to settle and for the servo to turn on.

The brake circuit prevents these phenomenon.

In principle, the brake circuit uses the tracking drive as a brake by cutting the unnecessary portions utilizing the 180° offset in the RF envelope and tracking error phase relationship which occurs when the actuator traverses the track in the radial direction from the inner track to the outer track and vice versa. (See Figs. 5-15 and 5-16.)

Concretely, this operation is achieved by masking the tracking drive using the TRKCNCL signal generated by loading the MIRR signal at the edge of the TZC (Tracking Zero Cross) signal.

The brake circuit can be turned on and off by D18 of $1. (See Fig. 5-17.)

In addition, the low frequency for the tracking drive after masking can be boosted. (SFBK1, 2 of $34B)

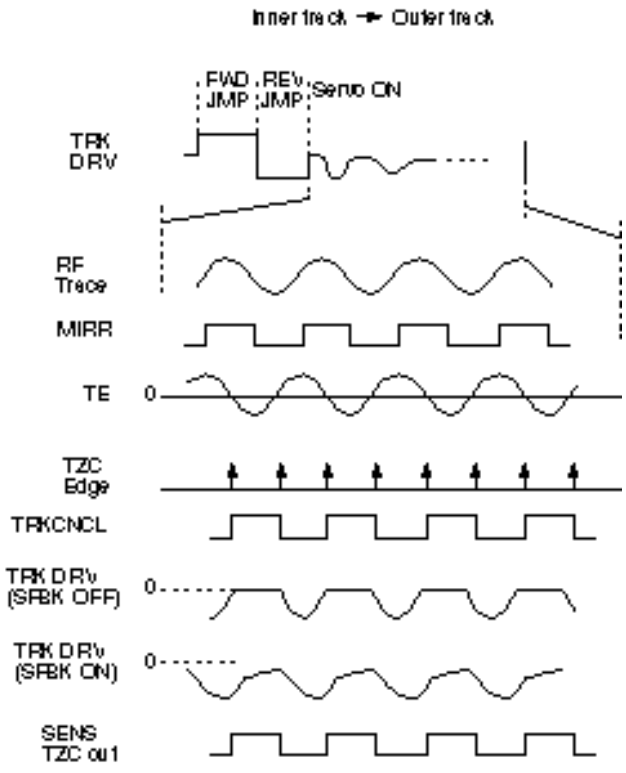


Fig. 5-15.

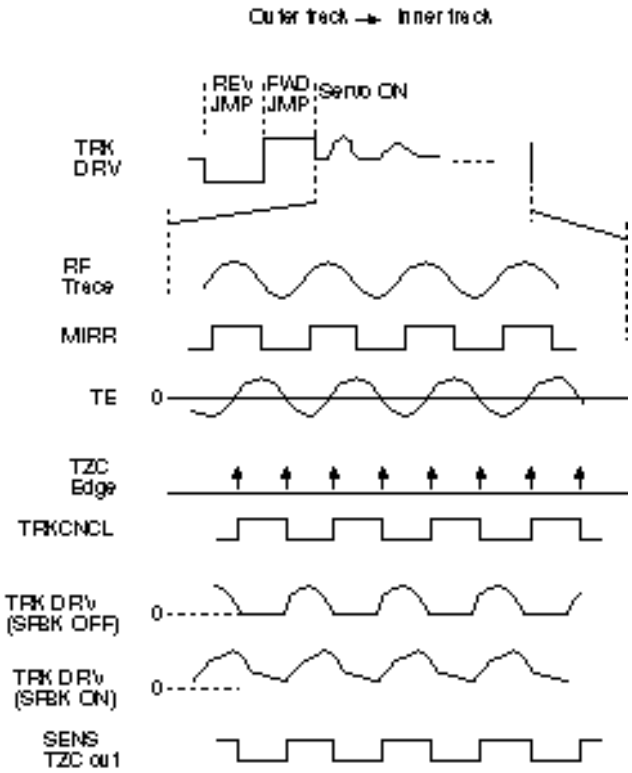


Fig. 5-16.

Register name	Command	D23 to D20	D19 to D16	
1	TRACKING CONTROL	0 0 0 1	1 0 * *	ANTI SHOCK ON
			0 * * *	ANTI SHOCK OFF
			* 1 * *	BRAKE ON
			* 0 * *	BRAKE OFF
			* * 0 *	TRACKING GAIN NORMAL
			* * 1 *	TRACKING GAIN UP
			* * * 1	TRACKING GAIN UP FILTER SELECT 1
			* * * 0	TRACKING GAIN UP FILTER SELECT 2

*: Don't care

Table 5-17.

§ 5-13. COUT Signal

The COUT signal is output to count the number of tracks during traverse, etc. It is basically generated by loading the MIRR signal at both edges of the TZC signal. The used TZC signal can be selected from among three different phases according to the COUT signal application.

- HPTZC: For 1-track jumps
  Fast phase COUT signal generation with a fast phase TZC signal. (The TZC phase is advanced by a cutoff 1kHz digital HPF; when MCK = 128Fs.)
- STZC: For COUT generation when MIRR is externally input and for applications other than COUT generation.
  This is generated by sampling the TE signal at 700kHz. (when MCK = 128Fs)
- DTZC: For high-speed traverse
  Reliable COUT signal generation with a delayed phase STZC signal.

Since it takes some time to generate the MIRR signal, it is necessary to delay the TZC signal in accordance with the MIRR signal delay during high-speed traverse.
The COUT signal output method is switched with D15 and D14 of $3C.

When D15 = 1: STZC
When D15 = 0 and D14 = 0: HPTZC
When D15 = 0 and D14 = 1: DTZC
When DTZC is selected, the delay can be selected from two values with D14 of $36.

§ 5-14. Serial Readout Circuit

The following measurement and adjustment results can be read out from the SENS pin by inputting the readout clock to the SCLK pin by $39. (See Fig. 5-18, Table 5-19 and "Description of SENS Signals".)

Specified commands

$390C: VC AVRG measurement result	$3953: FCS AGCNTL coefficient result
$3908: FE AVRG measurement result	$3963: TRK AGCNTL coefficient result
$3904: TE AVRG measurement result	$391C: TRVSC adjustment result
$391F: RF AVRG measurement result	$391D: FBIAS register value

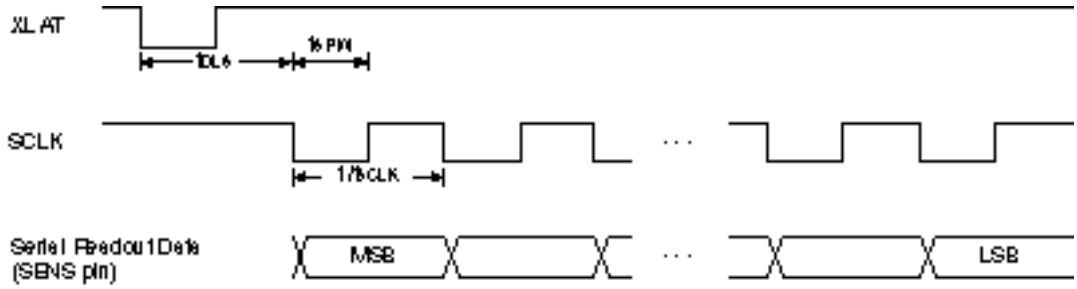


Fig. 5-18.

Item	Symbol	Min.	Typ.	Max.	Unit
SCLK frequency	f_{SCLK}			16	MHz
SCLK pulse width	t_{SPW}	31.3			ns
Delay time	t_{DLS}	15			µs

Table 5-19.

During readout, the upper 8 bits of the command register must be 39 (Hex).

§ 5-15. Writing to Coefficient RAM

The coefficient RAM can be rewritten by $34. All coefficients have default values in the built-in ROM, and transfer from the ROM to the RAM is completed approximately 40µs (when MCK = 128Fs) after the XRST pin rises. (The coefficient RAM cannot be rewritten during this period.)

After that, the characteristics of each built-in filter can be finely adjusted by rewriting the data for each address of the coefficient RAM.

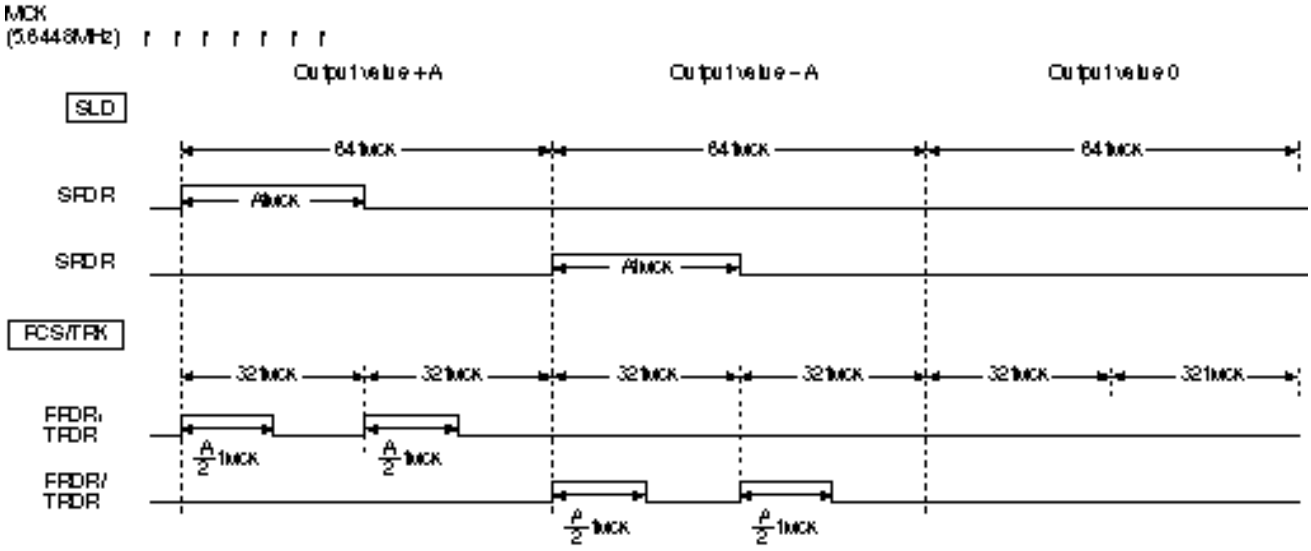
The coefficient rewrite command is comprised of 24 bits, with D14 to D8 of $34 as the address (D15 = 0) and D7 to D0 as data. Coefficient rewriting is completed 11.3µs (when MCK = 128Fs) after the command is received. When rewriting multiple coefficients, be sure to wait 11.3µs (when MCK = 128Fs) before sending the next rewrite command.

§ 5-16. PWM Output

FCS, TRK and SLD PWM format outputs are described below.

In particular, FCS and TRK use a double oversampling noise shaper.

Timing Chart 5-20 and Fig. 5-21 show examples of output waveforms and drive circuits.



$$t_{MCK} = \frac{1}{5.6448MHz} \approx 180ns$$

Timing Chart 5-20.

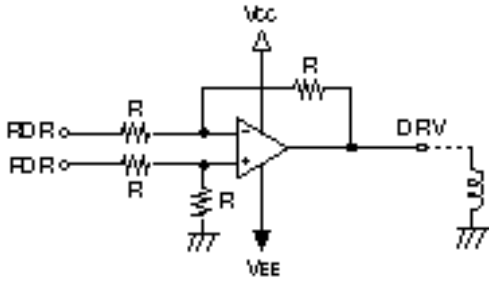


Fig. 5-21. Drive Circuit

§ 5-17. Servo Status Changes Produced by LOCK Signal

When the LOCK signal becomes low, the TRK servo switches to the gain-up mode and the SLD servo turns off in order to prevent SLD free-running.
Setting D6 (LKSW) of $38 to 1 deactivates this function.
In other words, neither the TRK servo nor the SLD servo change even when the LOCK signal becomes low. This enables microcomputer control.

§ 5-18. Description of Commands and Data Sets

$34

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	KA6	KA5	KA4	KA3	KA2	KA1	KA0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0

When D15 = 0.
KA6 to KA0: Coefficient address
KD7 to KD0: Coefficient data

$348 (preset: $348000)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	PGFS1	PGFS0	PFOK1	PFOK0	0	0	0	MRS	MRT1	MRT0	0	0

These commands set the GFS pin hold time. The hold time is inversely proportional to the playback speed.

PGFS1	PGFS0	Processing
0	0	High when the frame sync is of the correct timing, low when not the correct timing.
0	1	High when the frame sync is of the correct timing, low when continuously not the correct timing for 2ms or longer.
1	0	High when the frame sync is of the correct timing, low when continuously not the correct timing for 4ms or longer.
1	1	High when the frame sync is the correct timing, low when continuously not the correct timing for 8ms or longer.

These commands set the FOK hold time. See $3B for the FOK slice level.
These are the values when MCK = 128Fs, and the hold time is inversely proportional to the MCK setting.

PFOK1	PFOK0	Processing
0	0	High when the RFDC value is higher than the FOK slice level, low when lower than the FOK slice level.
0	1	High when the RFDC value is higher than the FOK slice level, low when continuously lower than the FOK slice level for 4.35ms or more.
1	0	High when the RFDC value is higher than the FOK slice level, low when continuously lower than the FOK slice level for 10.16ms or more.
1	1	High when the RFDC value is higher than the FOK slice level, low when continuously lower than the FOK slice level for 21.77ms or more.

MRS: Switches the time constant for the MIRR comparator level generation of the MIRR generation circuit.
When MRS = 0, the time constant is set to normal. (default)
When MRS = 1, the time constant is delayed compared to the normal state.
The duration of MIRR = high, which is caused by the affection of the RFDC signal pulse-formed noise and the like, is suppressed by setting MRS to 1.

MRT1, 0: These commands limit the time while MIRR = high.

	MRT1	MRT0	MIRR maximum time [ms]
*	0	0	No time limit
	0	1	1.10
	1	0	2.20
	1	1	4.00

*: preset

$34B (preset: $34B000)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	SFBK1	SFBK2	0	0	0	0	0	0	0	0	0	0

The low frequency can be boosted for brake operation.
See "§ 5-12 for brake operation".

SFBK1: When 1, brake operation is performed by setting the LowBooster-1 input to 0.
This is valid only when TLB1ON = 1. The preset is 0.
SFBK2: When 1, brake operation is performed by setting the LowBooster-2 input to 0.
This is valid only when TLB2ON = 1. The preset is 0.

$34C (preset: $34C000)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	THB ON	FHB ON	TLB1 ON	FLB1 ON	TLB2 ON	0	HBST1	HBST0	LB1S1	LB1S0	LB2S1	LB2S0

These commands turn on the boost function. (See "§ 5-20. Filter Composition".)
There are five boosters (three for the TRK filter and two for the FCS filter) which can be turned on and off independently.

THBON: When 1, the high frequency is boosted for the TRK filter. Preset when 0.
FHBON: When 1, the high frequency is boosted for the FCS filter. Preset when 0.
TLB1ON: When 1, the low frequency is boosted for the TRK filter. Preset when 0.
FLB1ON: When 1, the low frequency is boosted for the FCS filter. Preset when 0.
TLB2ON: When 1, the low frequency is boosted for the TRK filter. Preset when 0.

The difference between TLB1ON and TLB2ON is the position where the low frequency is boosted.
For TLB1ON, the low frequency is boosted before the TRK jump, and for TLB2ON, after the TRK jump.

The following commands set the boosters. (See "§ 5-20. Filter Composition".)

HBST1, HBST0: TRK and FCS HighBooster setting.
HighBooster has the configuration shown in Fig. 5-24a, and can select three different combinations of coefficients BK1, BK2 and BK3. (See Table 5-25a.)
An example of characteristics is shown in Fig. 5-26a.
These characteristics are the same for both the TRK and FCS filters.
The sampling frequency is 88.2kHz (when MCK = 128Fs).

LB1S1, LB1S0: TRK and FCS LowBooster-1 setting.
LowBooster-1 has the configuration shown in Fig. 5-24b, and can select three different combinations of coefficients BK4, BK5 and BK6. (See Table 5-25b.)
An example of characteristics is shown in Fig. 5-26b.
These characteristics are the same for both the TRK and FCS filters.
The sampling frequency is 88.2kHz (when MCK = 128Fs).

LB2S1, LB2S0: TRK LowBooster-2 setting.
LowBooster-2 has the configuration shown in Fig. 5-24c, and can select three different combinations of coefficients BK7, BK8 and BK9. (See Table 5-25c.)
An example of characteristics is shown in Fig. 5-26c.
This booster is used exclusively for the TRK filter.
The sampling frequency is 88.2kHz (when MCK = 128Fs).

Note) Fs = 44.1kHz

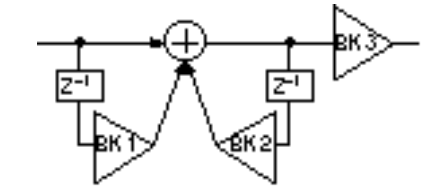


Fig. 5-24a.

HBST1	HBST0	HighBooster setting		
		BK1	BK2	BK3
0	—	–120/128	96/128	2
1	0	–124/128	112/128	2
1	1	–126/128	120/128	2

Table 5-25a.

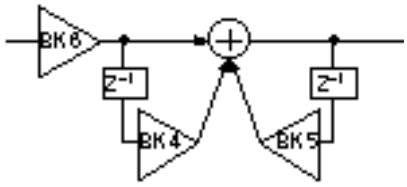


Fig. 5-24b.

LB1S1	LB1S0	LowBooster-1 setting		
		BK4	BK5	BK6
0	—	–255/256	1023/1024	1/4
1	0	–511/512	2047/2048	1/4
1	1	–1023/1024	4095/4096	1/4

Table 5-25b.

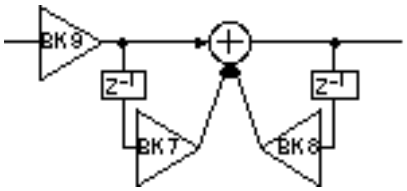


Fig. 5-24c.

LB2S1	LB2S0	LowBooster-2 setting		
		BK7	BK8	BK9
0	—	–255/256	1023/1024	1/4
1	0	–511/512	2047/2048	1/4
1	1	–1023/1024	4095/4096	1/4

Table 5-25c.

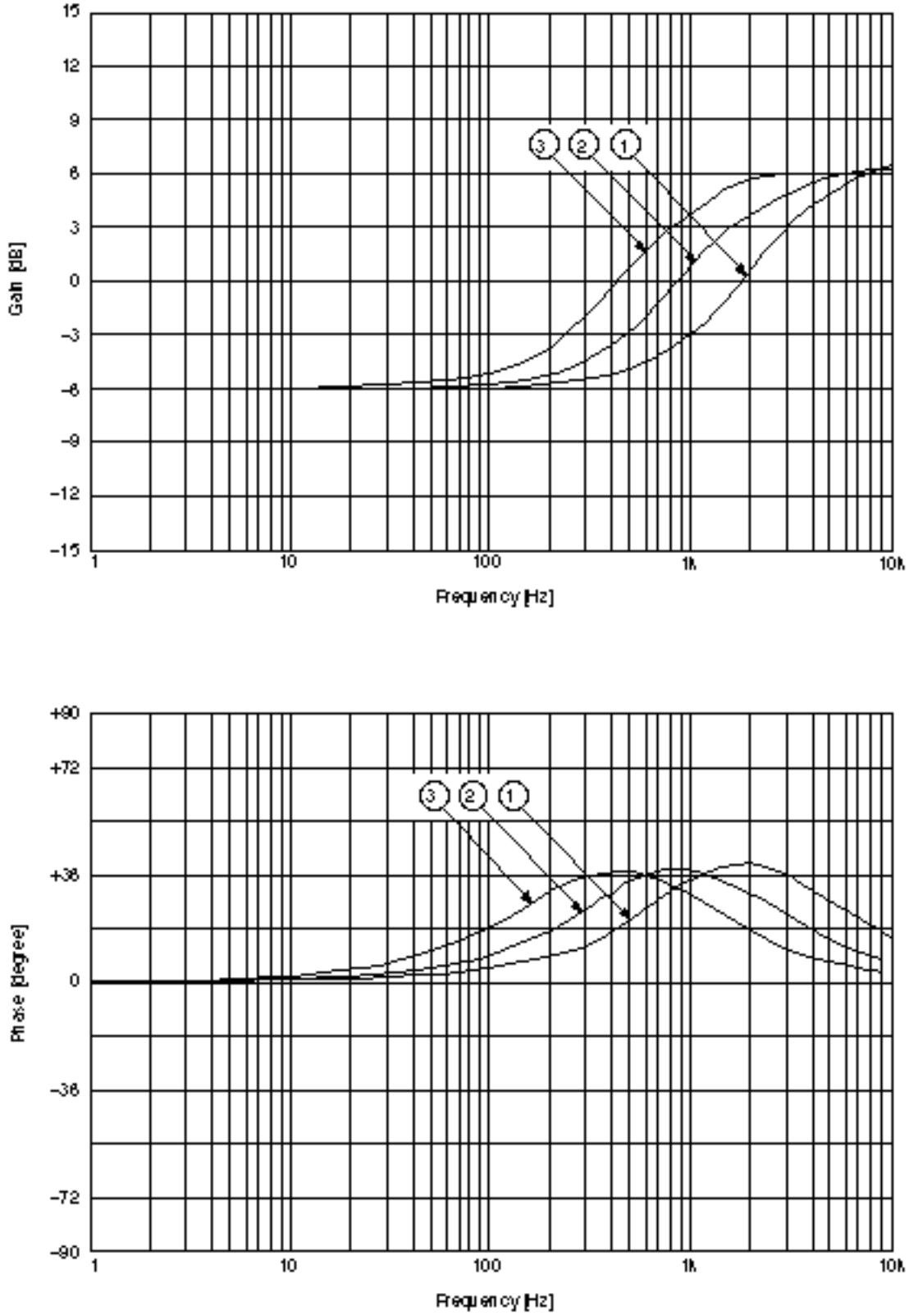


Fig. 5-26a. Servo HighBooster Characteristics [FCS, TRK] (MCK = 128Fs)

① HBST1 = 0 ② HBST1 = 1, HBST0 = 0 ③ HBST1 = 1, HBST0 = 1

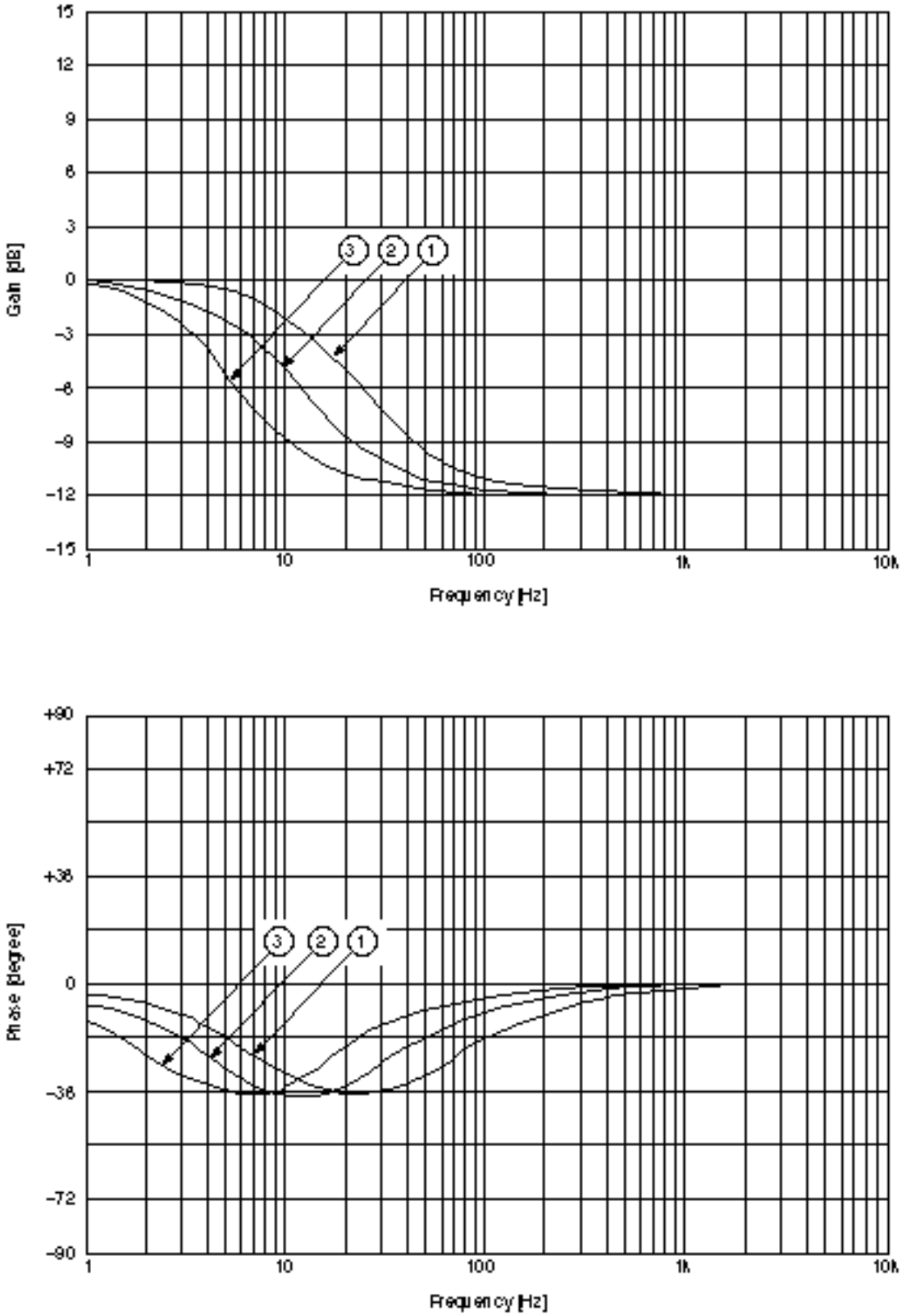


Fig. 5-26b. Servo LowBooster1 Characteristics [FCS, TRK] (MCK = 128Fs)

① LB1S1 = 0 ② LB1S1 = 1, LB1S0 = 0 ③ LB1S1 = 1, LB1S0 = 1

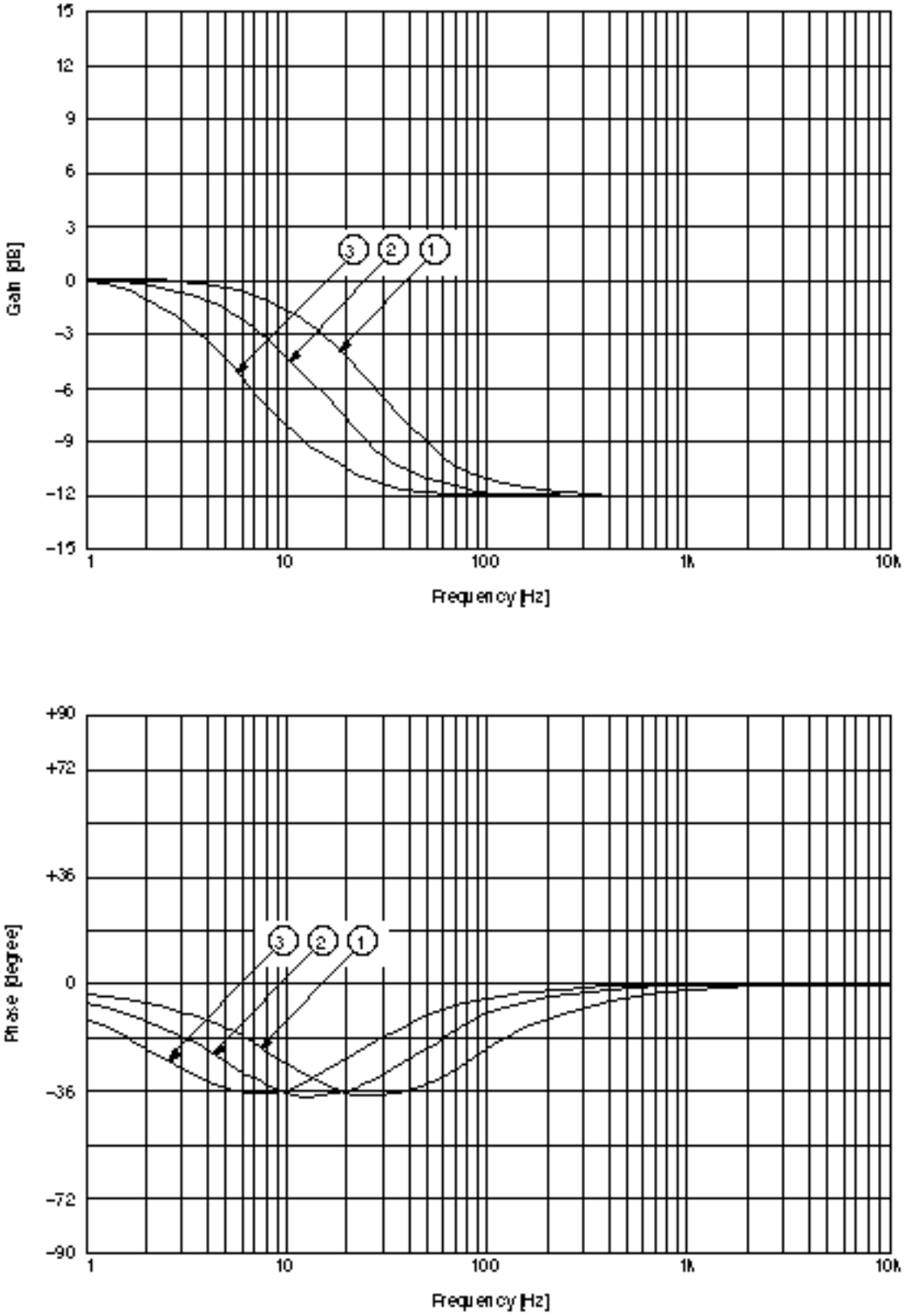


Fig. 5-26c. Servo LowBooster2 Characteristics [FCS, TRK] (MCK = 128Fs)

① LB2S1 = 0 ② LB2S1 = 1, LB2S0 = 0 ③ LB2S1 = 1, LB2S0 = 1

$34E (preset: $34E000)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	0	IDFSL3	IDFSL2	IDFSL1	IDFSL0	0	0	IDFT1	IDFT0	0	0	0	0

IDFSL3: The new DFCT detection is output.
When IDFSL3 = 0, only DFCT in §5-9 is detected and the signal is output from the DFCT pin. (default)
When IDFSL3 = 1, DFCT in §5-9 and new DFCT are switched and the resulting signal is output from the DFCT pin.
The timing for switching is as follows;
When DFCT in §5-9 = low, the new DFCT signal is output from the DFCT pin.
When DFCT in §5-9 = high, DFCT in $5-9 is output from the DFCT pin.
After DFCT in §5-9 is switched to low, the time when the new DFCT output is enabled can be set. (See IDFT1 and IDFT0 of $34E.)

IDFSL3	DFCT in $5-9	DFCT pin
0	L	DFCT in §5-9
0	H	DFCT in §5-9
1	L	New DFCT
1	H	DFCT in §5-9

IDFSL2: The new DFCT detection time is set.
After the new DFCT is detected, DFCT=high is held for a specific time. This time is set.
When IDFSL2 = 0, long hold time. (default)
When IDFSL2 = 1, short hold time.

IDFSL1: The new DFCT detection sensitivity is set.
When IDFSL1 = 0, high detection sensitivity. (default)
When IDFSL1 = 1, low detection sensitivity.

IDFSL0: The new DFCT cancel sensitivity is set.
When IDFSL0 = 0, high cancel sensitivity is set. (default)
When IDFSL0 = 1, low cancel sensitivity is set.

IDFT1, 0: After DFCT in §5-9 is switched to low, the time when the new DFCT output is enabled (output prohibit time) is set.

	IDFT1	IDFT0	New DFCT signal output prohibit time
*	0	0	204.08µs
	0	1	294.78µs
	1	0	408.16µs
	1	1	612.24µs

*: preset

$34F

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	0	FBL9	FBL8	FBL7	FBL6	FBL5	FBL4	FBL3	FBL2	FBL1	—

When D15 = D14 = D13 = D12 = D11 = 1 ($34F)

D10 = 0

FBIAS LIMIT register write

FBL9 to FBL1: Data; data compared with FB9 to FB1, FBL9 = MSB.

When using the FBIAS register in counter mode, counter operation stops when the value of FB9 to FB1 matches with FBL9 to FBL1.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	0	1	FB9	FB8	FB7	FB6	FB5	FB4	FB3	FB2	FB1	—

When D15 = D14 = D13 = D12 = 1 ($34F)

D11 = 0, D10 = 1

FBIAS register write

FB9 to FB1: Data; two's complement data, FB9 = MSB.

For FE input conversion, FB9 to FB1 = 011111111 corresponds to 255/256 × V_{DD}/4 and FB9 to FB1 = 100000000 to –256/256 × V_{DD}/4 respectively. (V_{DD}: supply voltage)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	0	0	TV9	TV8	TV7	TV6	TV5	TV4	TV3	TV2	TV1	TV0

When D15 = D14 = D13 = D12 = 1 ($34F)

D11 = 0, D10 = 0

TRVSC register write

TV9 to TV0: Data; two's complement data, TV9 = MSB.

For TE input conversion, TV9 to TV0 = 0011111111 corresponds to 255/256 × V_{DD}/4 and TV9 to TV0 = 1100000000 to –256/256 × V_{DD}/4 respectively. (V_{DD}: supply voltage)

Note) • When the TRVSC register is read out, the data length is 9 bits. At this time, data corresponding to each bit TV8 to TV0 during external write are read out.

• When reading out internally measured values and then writing these values externally, set TV9 the same as TV8.

$35 (preset: $35 58 2D)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
FT1	FT0	FS5	FS4	FS3	FS2	FS1	FS0	FTZ	FG6	FG5	FG4	FG3	FG2	FG1	FG0

FT1, FT0, FTZ: Focus search-up speed
Default value: 010 (0.673 × V_{DD} V/s)
Focus drive output conversion

	FT1	FT0	FTZ	Focus search speed [V/s]
	0	0	0	1.35 × V_{DD}
*	0	1	0	0.673 × V_{DD}
	1	0	0	0.449 × V_{DD}
	1	1	0	0.336 × V_{DD}
	0	0	1	1.79 × V_{DD}
	0	1	1	1.08 × V_{DD}
	1	0	1	0.897 × V_{DD}
	1	1	1	0.769 × V_{DD}

*: preset, V_{DD}: PWM driver supply voltage

FS5 to FS0: Focus search limit voltage
Default value: 011000 ((1±24/64) × V_{DD}/2, V_{DD}: PWM driver supply voltage)
Focus drive output conversion
FG6 to FG0: AGF convergence gain setting value
Default value: 0101101

$36 (preset: $36 0E 2E)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TDZC	DTZC	TJ5	TJ4	TJ3	TJ2	TJ1	TJ0	SFJP	TG6	TG5	TG4	TG3	TG2	TG1	TG0

TDZC: Selects the TZC signal for generating the TRKCNCL signal during brake circuit operation.
TDZC = 0: The edge of the HPTZC or STZC signal, whichever has the faster phase, is used.
TDZC = 1: The edge of the HPTZC or STZC signal or the tracking drive signal zero-cross, whichever has the fastest phase, is used. (See § 5-12.)
DTZC: DTZC delay (8.5/4.25µs, when MCK = 128Fs)
Default value: 0 (4.25µs)
TJ5 to TJ0: Track jump voltage
Default value: 001110 ((1±14/64) × V_{DD}/2, V_{DD}: PWM driver supply voltage)
Tracking drive output conversion
SFJP: Surf jump mode on/off
The tracking PWM output is generated by adding the tracking filter output and TJReg (TJ5 to 0), by setting D7 to 1 (on)
TG6 to TG0: AGT convergence gain setting value
Default value: 0101110

$37 (preset: $37 50 BA)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
FZSH	FZSL	SM5	SM4	SM3	SM2	SM1	SM0	AGS	AGJ	AGGF	AGGT	AGV1	AGV2	AGHS	AGHT

FZSH, FZSL: FZC (Focus Zero Cross) slice level
Default value: 01 (1/8 × V_{DD}/2, V_{DD}: supply voltage); FE input conversion

	FZSH	FZSL	Slice level
*	0	0	1/4 × V_{DD}/2
	0	1	1/8 × V_{DD}/2
	1	0	1/16 × V_{DD}/2
	1	1	1/32 × V_{DD}/2

*: preset

SM5 to SM0: Sled move voltage
Default value: 010000 ((1±16/64) × V_{DD}/2, V_{DD}: PWM driver supply voltage)
Sled drive output conversion

AGS: AGCNTL self-stop on/off
Default value: 1 (on)

AGJ: AGCNTL convergence completion judgment time during low sensitivity adjustment (31/63ms, when MCK = 128Fs)
Default value: 0 (63ms)

AGGF: Focus AGCNTL internally generated sine wave amplitude (small/large)
Default value: 1 (large)

AGGT: Tracking AGCNTL internally generated sine wave amplitude (small/large)
Default value: 1 (large)

		FE/TE input conversion
AGGF	0 (small)	1/32 × V_{DD}/2
	1 (large)*	1/16 × V_{DD}/2
AGGT	0 (small)	1/16 × V_{DD}/2
	1 (large)*	1/8 × V_{DD}/2

*: preset

AGV1: AGCNTL convergence sensitivity during high sensitivity adjustment; high/low
Default value: 1 (high)

AGV2: AGCNTL convergence sensitivity during low sensitivity adjustment; high/low
Default value: 0 (low)

AGHS: AGCNTL high sensitivity adjustment on/off
Default value: 1 (on)

AGHT: AGCNTL high sensitivity adjustment time (128/256ms, when MCK = 128Fs)
Default value: 0 (256ms)

$38 (preset: $38 00 00)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
VCLM	VCLC	FLM	FLC0	RFLM	RFLC	AGF	AGT	DFSW	LKSW	TBLM	TCLM	FLC1	TLC2	TLC1	TLC0

DC offset cancel. See §5-3.

*VCLM: VC level measurement (on/off)

VCLC: VC level compensation for FCS In register (on/off)

*FLM: Focus zero level measurement (on/off)

FLC0: Focus zero level compensation for FZC register (on/off)

*RFLM: RF zero level measurement (on/off)

RFLC: RF zero level compensation (on/off)

Automatic gain control. See §5-6.

AGF: Focus auto gain adjustment (on/off)

AGT: Tracking auto gain adjustment (on/off)

Misoperation prevention circuit

DFSW: Defect disable switch (on/off)
Setting this switch to 1 (on) disables the defect countermeasure circuit.

LKSW: Lock switch (on/off)
Setting this switch to 1 (on) disables the sled free-running prevention circuit.

DC offset cancel. See §5-3.

TBLM: Traverse center measurement (on/off)

*TCLM: Tracking zero level measurement (on/off)

FLC1: Focus zero level compensation for FCS In register (on/off)

TLC2: Traverse center compensation (on/off)

TLC1: Tracking zero level compensation (on/off)

TLC0: VC level compensation for TRK/SLD In register (on/off)

Note) Commands marked with * are accepted every 2.9ms. (when MCK = 128Fs)
All commands are on when 1.

$39 (preset: $39 0000)

D15	D14	D13	D12	D11	D10	D9	D8
DAC	SD6	SD5	SD4	SD3	SD2	SD1	SD0

DAC: Serial data readout DAC mode (on/off)

SD6 to SD0: Serial readout data select

SD6	SD5	Readout data			Readout data length	
1	Coefficient RAM data for address = SD5 to SD0				8 bits	
0	1	Data RAM data for address = SD4 to SD0			16 bits	
0	0	SD4	SD3 to SD0			
		1	1 1 1 1	RF AVRG register	8 bits	$399F
			1 1 1 0	RFDC input signal	8 bits	$399E
			1 1 0 1	FBIAS register	9 bits	$399D
			1 1 0 0	TRVSC register	9 bits	$399C
			0 0 1 1	RFDC envelope (bottom)	8 bits	$3993
			0 0 1 0	RFDC envelope (peak)	8 bits	$3992
			0 0 0 1	RFDC envelope (peak) – (bottom)	8 bits	$3991
		0	1 1 * *	VC AVRG register	9 bits	$398C
			1 0 * *	FE AVRG register	9 bits	$3988
			0 1 * *	TE AVRG register	9 bits	$3984
			0 0 1 1	FE input signal	8 bits	$3983
			0 0 1 0	TE input signal	8 bits	$3982
			0 0 0 1	SE input signal	8 bits	$3981
			0 0 0 0	VC input signal	8 bits	$3980

*: Don't care

Note) Coefficients K40 to K4F cannot be read out.
See the Description for "Data Readout" concerning readout methods for the above data.

$3A (preset: $3A 00 00)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	FBON	FBSS	FBUP	FBV1	FBV0	FIFZC	TJD0	FPS1	FPS0	TPS1	TPS0	0	SJHD	INBK	MTI0

FBON: FBIAS (focus bias) register addition (on/off)
The FBIAS register value is added to the signal loaded into the FCS In register by setting FBON = 1 (on).

FBSS: FBIAS (focus bias) register/counter switching
FBSS = 0: register, FBSS = 1: counter.

FBUP: FBIAS (focus bias) counter up/down operation switching
This performs counter up/down control when FBSS = 1. FBUP = 0: down counter, FBUP = 1: up counter.

FBV1, FBV0: FBIAS (focus bias) counter voltage switching
The number of FCS BIAS count-up/-down steps per cycle is decided by these bits.

	FBV1	FBV0	Number of steps per cycle
*	0	0	1
	0	1	2
	1	0	4
	1	1	8

*: preset

The counter changes once for each sampling cycle of the focus servo filter. When MCK is 128Fs, the sampling frequency is 88.2kHz. When converted to FE input, 1 step is approximately $1/2^9 \times V_{DD} \times 0.4$, V_{DD} = supply voltage.

TJD0: This sets the tracking servo filter data RAM to 0 when switched from track jump to servo on only when SFJP = 1 (during surf jump operation).

FPS1, FPS0: Gain setting when transferring data from the focus filter to the PWM block.

TPS1, TPS0: Gain setting when transferring data from the tracking filter to the PWM block.
These are effective for increasing the overall gain in order to widen the servo band.
Operation when FPS1, FPS0 (TPS1, TPS0) = 00 is the same as usual (7-bit shift). However, 6dB, 12dB and 18dB can be selected independently for focus and tracking by setting the relative gain to 0dB when FPS1, FPS0 (TPS1, TPS0) = 00.

	FPS1	FPS0	Relative gain
*	0	0	0dB
	0	1	+6dB
	1	0	+12dB
	1	1	+18dB

TPS1	TPS0	Relative gain	
0	0	0dB	*
0	1	+6dB	
1	0	+12dB	
1	1	+18dB	

*: preset

SJHD: This holds the tracking filter output at the value when surf jump starts during surf jump.

INBK: When INBK = 0 (off), the brake circuit masks the tracking drive signal with TRKCNCL which is generated by fetching the MIRR signal at the TZC edge. When INBK = 1 (on), the tracking filter input is masked instead of the drive output.

MTI0: The tracking filter input is masked when the MIRR signal is high by setting MTI0 = 1 (on).

FIFZC: This selects the FZC slice level setting command.
When 0, the FZC slice level is determined by the $37 FZSH and FZSL setting values. (default)
When 1, the FZC slice level is determined by the $3F8 FIFZB3 to FIFZB0 and FIFZA3 to FIFZA0 setting values.
This allows more detailed setting and the addition of hysteresis compared to the $37 FZSH and FZSL setting.

$3B (preset: $3B E0 50)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SFO2	SFO1	SDF2	SDF1	MAX2	MAX1	SFOX	BTF	D2V2	D2V1	D1V2	D1V1	RINT	0	0	0

SFOX, SFO2, SFO1: FOK slice level

Default value: 011 (28/256 × V_{DD}/2, V_{DD} = supply voltage)

RFDC input conversion

	SFOX	SFO2	SFO1	Slice level
	0	0	0	16/256 × V_{DD}/2
	0	0	1	20/256 × V_{DD}/2
	0	1	0	24/256 × V_{DD}/2
*	0	1	1	28/256 × V_{DD}/2
	1	0	0	32/256 × V_{DD}/2
	1	0	1	40/256 × V_{DD}/2
	1	1	0	48/256 × V_{DD}/2
	1	1	1	56/256 × V_{DD}/2

*: preset

SDF2, SDF1: DFCT slice level

Default value: 10 (0.0313 × V_{DD})

RFDC input conversion

	SDF2	SDF1	Slice level
	0	0	0.0156 × V_{DD}
	0	1	0.0234 × V_{DD}
*	1	0	0.0313 × V_{DD}
	1	1	0.0391 × V_{DD}

*: preset, V_{DD}: supply voltage

MAX2, MAX1: DFCT maximum time (MCK = 128Fs)

Default value: 00 (no timer limit)

	MAX2	MAX1	DFCT maximum time
*	0	0	No timer limit
	0	1	2.00ms
	1	0	2.36
	1	1	2.72

*: preset

BTF: Bottom hold double-speed count-up mode for MIRR signal generation

On/off (default: off)

On when set to 1.

D2V2, D2V1: Peak hold 2 for DFCT signal generation
Count-down speed setting
Default value: 01 (0.086 × V_{DD}/ms, 44.1kHz)
[V/ms] unit items indicate RFDC input conversion; [kHz] unit items indicate the operating frequency of the internal counter.

	D2V2	D2V1	Count-down speed	
			[V/ms]	[kHz]
	0	0	0.0431 × V_{DD}	22.05
*	0	1	0.0861 × V_{DD}	44.1
	1	0	0.172 × V_{DD}	88.2
	1	1	0.344 × V_{DD}	176.4

*: preset, V_{DD}: supply voltage

D1V2, D1V1: Peak hold 1 for DFCT signal generation
Count-down speed setting
Default value: 01 (0.688 × V_{DD}/ms, 352.8kHz)
[V/ms] unit items indicate RFDC input conversion; [kHz] unit items indicate the operating frequency of the internal counter.

	D1V2	D2V1	Count-down speed	
			[V/ms]	[kHz]
	0	0	0.344 × V_{DD}	176.4
*	0	1	0.688 × V_{DD}	352.8
	1	0	1.38 × V_{DD}	705.6
	1	1	2.75 × V_{DD}	1411.2

*: preset, V_{DD}: supply voltage

RINT: This initializes the initial-state registers of the circuits which generate MIRR, DFCT and FOK.

$3C (preset: $3C 00 80)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
COSS	COTS	CETZ	CETF	COT2	COT1	MOT2	0	BTS1	BTS0	MRC1	MRC0	0	0	0	0

COSS, COTS: This selects the TZC signal used when generating the COUT signal.
Preset = HPTZC.

	COSS	COTS	TZC
	1	—	STZC
*	0	0	HPTZC
	0	1	DTZC

*: preset, —: don't care

STZC is the TZC generated by sampling the TE signal at 700kHz. (when MCK = 128Fs)
DTZC is the delayed phase STZC. (The delay time can be selected by D14 of $36.)
HPTZC is the fast phase TZC passed through a HPF with a cut-off frequency of 1kHz.
See § 5-13.

CETZ: The input from the TE pin normally enters the TRK filter and is used to generate the TZC signal. However, the input from the CE pin can also be used. This function is for the center error servo.
When 0, the TZC signal is generated by using the signal input to the TE pin.
When 1, the TZC signal is generated by using the signal input to the CE pin.

CETF: When 0, the signal input to the TE pin is input to the TRK servo filter.
When 1, the signal input to the CE pin is input to the TRK servo filter.

These commands output the TZC signal.
COT2, COT1: This outputs the TZC signal from the COUT pin.

	COT2	COT1	COUT pin output
	1	—	STZC
	0	1	HPTZC
*	0	0	COUT

*: preset, —: don't care

MOT2: The STZC signal is output from the MIRR pin by setting MOT2 to 1.

These commands set the MIRR signal generation circuit.

BTS1, BTS0: This sets the count-up speed for the bottom hold value of the MIRR generation circuit.
The time per step is approximately 708ns (when MCK = 128Fs). The preset value is BTS1 = 1, BTS0 = 0 like the CXD2586R. This is valid only when BTF of $3B is 0.

MRC1, MRC0: This sets the minimum pulse width for masking the MIRR signal of the MIRR generation circuit.
As noted in § 5-9, the MIRR signal is generated by comparing the waveform obtained by subtracting the bottom hold value from the peak hold value with the MIRR comparator level. Strictly speaking, however, for MIRR to become high, these levels must be compared continuously for a certain time. This sets that time.
The preset value is MRC1 = 0, MRC0 = 0 like the CXD2586R.

	BTS1	BTS0	Number of count-up steps per cycle
	0	0	1
	0	1	2
*	1	0	4
	1	1	8

MRC1	MRC0	Setting time [µs]
0	0	5.669*
0	1	11.338
1	0	22.675
1	1	45.351

*: preset (when MCK = 128Fs)

$3D (preset: $3D 00 00)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SFID	SFSK	THID	THSK	0	TLD2	TLD1	TLD0	0	0	0	0	0	0	0	0

SFID: SLED servo filter input can be obtained not from SLD in Reg, but from M0D, which is the TRK filter second-stage output.
When the low frequency component of the tracking error signal obtained from the RF amplifier is attenuated, the low frequency can be amplified and input to the SLD servo filter.

SFSK: Only during TRK servo gain up2 operation, coefficient K30 is used instead of K00. Normally, the DC gain between the TE input pin and M0D changes for TRK filter gain normal and gain up2, creating a difference in the DC level at M0D. In this case, the DC level of the signal transmitted to M00 can be kept uniform by adjusting the K30 value even during the above switching.

THID: TRK hold filter input can be obtained not from SLD in Reg, but from M0D, which is the TRK filter second-stage output.
When signals other than the tracking error signal from the RF amplifier are input to the SE input pin, the signal transmitted from the TE pin can be obtained as the TRK hold filter input.

THSK: Only during TRK servo gain up2 operation, coefficient K46 is used instead of K40. Normally, the DC gain between the TE input pin and M0D changes for TRK filter gain normal and gain up2, creating a difference in the DC level at M0D. In this case, the DC level of the signal transmitted to M18 can be kept uniform by adjusting the K46 value even during the above switching.

∗ See "§ 5-20. Filter Composition" regarding the SFID, SFSK, THID and THSK commands.

TLD0 to 2: This turns on and off SLD filter correction independently of the TRK filter.
See $38 (TLC0 to 2) and Fig. 5-3.

	TLC2	TLD2	Traverse center correction	
			TRK filter	SLD filter
∗	0	—	OFF	OFF
	1	0	ON	ON
		1	ON	OFF

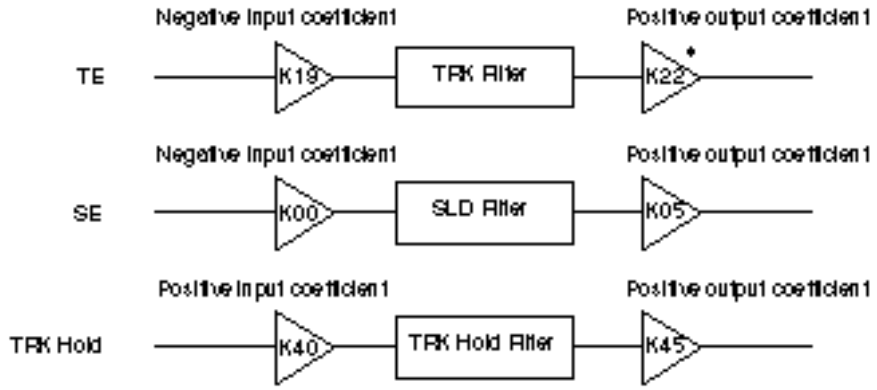
	TLC1	TLD1	Tracking zero level correction	
			TRK filter	SLD filter
∗	0	—	OFF	OFF
	1	0	ON	ON
		1	ON	OFF

	TLC0	TLD0	VC level correction	
			TRK filter	SLD filter
∗	0	—	OFF	OFF
	1	0	ON	ON
		1	ON	OFF

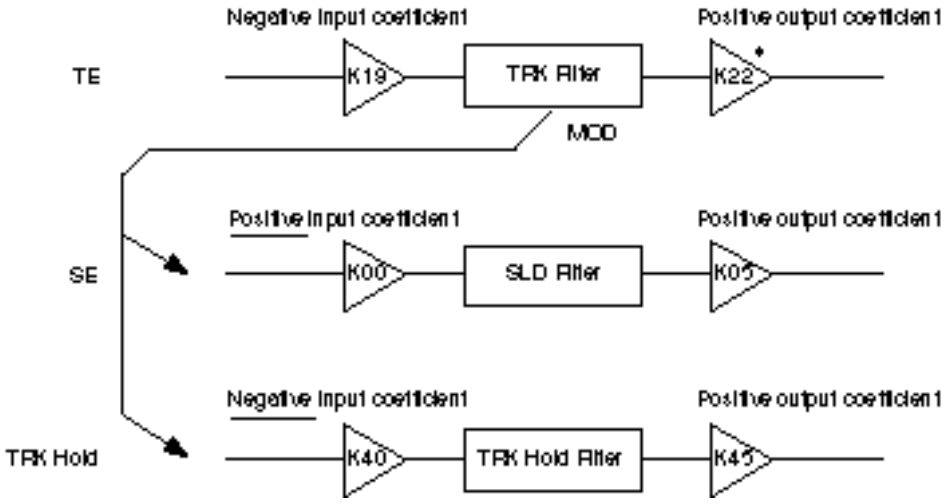
∗: preset, —: don't care

• Input coefficient sign inversion when SFID = 1 and THID = 1

The preset coefficients for the TRK filter are negative for input and positive for output. With this, the CXD3068Q outputs the servo drives which have the reversed phase to the error inputs..



When SFID = 1, the TRK filter negative input coefficient is applied to the SLD filter, so invert the SLD input coefficient (K00) sign. (For example, inverting the sign for coefficient K00: E0Hex results in 20Hex.)
For the same reason, when THID = 1, invert the TRK hold input coefficient (K40) sign.



* for TRK servo gain normal
See "§ 5-20. Filter Composition".

$3E (preset: $3E 00 00)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
F1NM	F1DM	F3NM	F3DM	T1NM	T1UM	T3NM	T3UM	DFIS	TLCD	0	LKIN	COIN	MDFI	MIRI	XT1D

F1NM, F1DM: Quasi double accuracy setting for FCS servo filter first-stage
On when 1; default when 0.
F1NM: Gain normal
F1DM: Gain down

T1NM, T1UM: Quasi double accuracy setting for TRK servo filter first-stage
On when 1; default when 0.
T1NM: Gain normal
T1UM: Gain up

F3NM, F3DM: Quasi double accuracy setting for FCS servo filter third-stage
On when 1; default when 0.
Generally, the advance amount of the phase becomes large by partially setting the FCS servo third-stage filter which is used as the phase compensation filter to double accuracy.
F3NM: Gain normal
F3DM: Gain down

T3NM, T3UM: Quasi double accuracy setting for TRK servo filter third-stage
On when 1; default when 0.
Generally, the advance amount of the phase becomes large by partially setting the TRK servo third-stage filter which is used as the phase compensation filter to double accuracy.
T3NM: Gain normal
T3UM: Gain up

Note) Filter first- and third-stage quasi double accuracy settings can be set individually.
See "§ 5-20 Filter Composition" at the end of this specification concerning quasi double accuracy.

DFIS: FCS hold filter input extraction node selection
0: M05 (Data RAM address 05); default
1: M04 (Data RAM address 04)

TLCD: This command masks the TLC2 command set by D2 of $38 only when FOK is low.
On when 1; default when 0

LKIN: When 0, the internally generated LOCK signal is output to the LOCK pin. (default)
When 1, the LOCK signal can be input from an external source to the LOCK pin.

COIN: When 0, the internally generated COUT signal is output to the COUT pin. (default)
When 1, the COUT signal can be input from an external source to the COUT pin.

The MIRR, DFCT and FOK signals can also be input from an external source.

MDFI: When 0, the MIRR, DFCT and FOK signals are generated internally. (default)
When 1, the MIRR, DFCT and FOK signals can be input from an external source through the MIRR, DFCT and FOK pins.

MIRI: When 0, the MIRR signal is generated internally. (default)
When 1, the MIRR signal can be input from an external source through the MIRR pin.

	MDFI	MIRI	
*	0	0	MIRR, DFCT and FOK are all generated internally.
	0	1	MIRR only is input from an external source.
	1	—	MIRR, DFCT and FOK are all input from an external source.

*: preset, —: don't care

XT1D: When XT1D = 1, the input to the servo master clock can be used without dividing its frequency. This command takes precedence over the XTSL pin, XT2D and XT4D. See the description of $3F for XT2D and XT4D.

$3F (preset: $3F 00 00)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	AGG4	XT4D	XT2D	0	DRR2	DRR1	DRR0	0	ASFG	FTQ	1	0	0	AGHF	0

Note) Be sure to set D4 of $3F to 1 for CXD3068Q.

AGG4: This varies the amplitude of the internally generated sine wave using the AGGF and AGGT commands during AGC. When AGG4 = 0, the default is used. When AGG4 = 1, the setting is as shown in the table below.

AGG4	AGGF	AGGT	Sine wave amplitude	
			FE input conversion	TE input conversion
0	0	—	$1/32 \times V_{DD}/2$	—
	1	—	$1/16 \times V_{DD}/2$	—
	—	0	—	$1/16 \times V_{DD}/2$
	—	1	—	$1/8 \times V_{DD}/2$*
1	0	0	$1/64 \times V_{DD}/2$	
	0	1	$1/32 \times V_{DD}/2$	
	1	0	$1/16 \times V_{DD}/2$	
	1	1	$1/8 \times V_{DD}/2$	

See $37 for AGGF and AGGT.
The presets are AGG4 = 0, AGGF = 1 and AGGT = 1.
*: preset, —: don't care

XT4D, XT2D: MCK (digital servo master clock) frequency division setting
This command forcibly sets the frequency division ratio to 1/4, 1/2 or 1/1 when MCK is generated. See the description of $3E for XT1D. Also, see the decription of "§5-2. Digital Servo Block Master Clock (MCK)".

XT1D	XT2D	XT4D	Frequency division ratio
* 0	0	0	According to XTSL
1	—	—	1/1
0	1	—	1/2
0	0	1	1/4

*: preset, —: don't care

DRR2 to DRR0: Partially clears the Data RAM values (0 write).
The following values are cleared when 1 (on) respectively; default = 0
DRR2: M08, M09, M0A
DRR1: M00, M01, M02
DRR0: M00, M01, M02 only when LOCK = low
Note) Set DRR1 and DRR0 on for 50µs or more.

ASFG: When vibration detection is performed during anti-shock circuit operation, the FCS servo filter is forcibly set to gain normal status.
On when 1; default when 0

AGHF: This halves the frequency of the internally generated sine wave during AGC.

FTQ: The slope of the output during focus search is 1/4 of the conventional output slope.
On when 1; default when 0 .

ASOT: The anti-shock signal, which is internally detected, is output from the ATSK pin.
Output when set to 1; default = 0
Vibration detection when a high signal is output for the anti-shock signal output.

$3F8 (preset: $3F8800)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	SYG3	SYG2	SYG1	SYG0	FIFZB3	FIFZB2	FIFZB1	FIFZB0	FIFZA3	FIFZA2	FIFZA1	FIFZA0

SYG3 to SYG0: These simultaneously set the focus drive, tracking drive and sled drive output gains. See the $CX command for the spindle drive output gain setting.

	SYG3	SYG2	SYG1	SYG0	GAIN
	0	0	0	0	0 (–∞dB)
	0	0	0	1	0.125 (–18.1dB)
	0	0	1	0	0.250 (–12.0dB)
	0	0	1	1	0.375 (–8.5dB)
	0	1	0	0	0.500 (–6.0dB)
	0	1	0	1	0.625 (–4.1dB)
	0	1	1	0	0.750 (–2.5dB)
	0	1	1	1	0.875 (–1.2dB)
*	1	0	0	0	1.000 (0.0dB)
	1	0	0	1	1.125 (+1.0dB)
	1	0	1	0	1.250 (+1.9dB)
	1	0	1	1	1.375 (+2.8dB)
	1	1	0	0	1.500 (+3.5dB)
	1	1	0	1	1.625 (+4.2dB)
	1	1	1	0	1.750 (+4.9dB)
	1	1	1	1	1.875 (+5.5dB)

*: preset

FIFZB3 to FIFZB0:

This sets the slice level at which FZC changes from high to low.

FIFZA3 to FIFZA0:

This sets the slice level at which FZC changes from low to high.

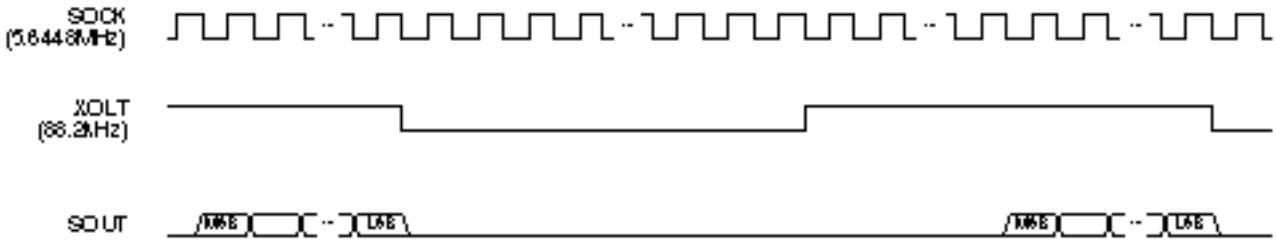
The FIFZB3 to FIFZB0 and FIFZA3 to FIFZA0 setting values are valid only when $3A FIFZC is 1.

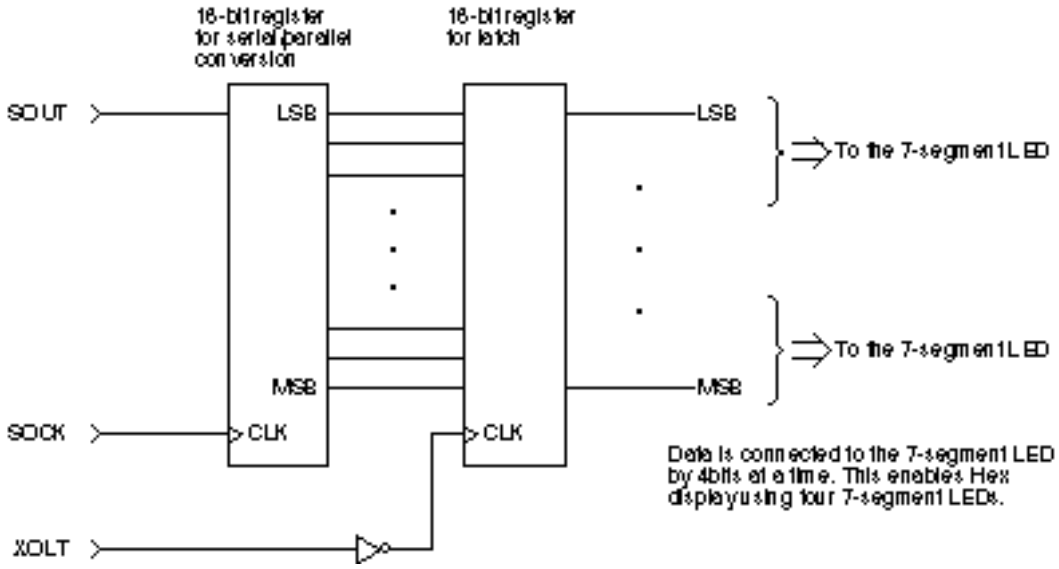
Set so that the FIFZB3 to FIFZB0 ≤ FIFZA3 to FIFZA0.

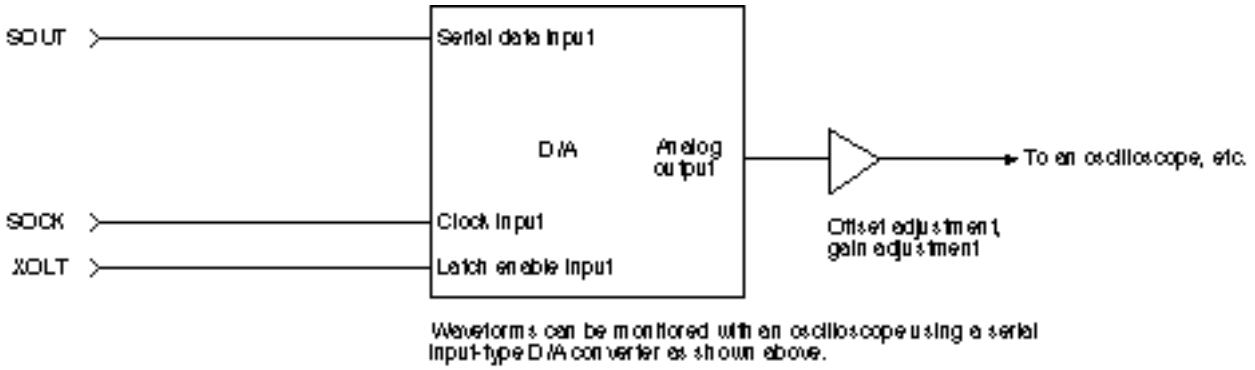
Hysteresis can be added to the slice level by setting FIFZB3 to FIFZB0 < FIFZA3 to FIFZA0.

$$\text{FZC slice level} = \frac{\text{FIFZB3 to FIFZB0 or FIFZA3 to FIFZA0 setting value}}{32} \times 0.5 \times V_{DD}\ [V]$$

Description of Data Readout







§ 5-19. List of Servo Filter Coefficients

<Coefficient Preset Value Table (1)>

ADDRESS	DATA	CONTENTS
K00	E0	SLED INPUT GAIN
K01	81	SLED LOW BOOST FILTER A-H
K02	23	SLED LOW BOOST FILTER A-L
K03	7F	SLED LOW BOOST FILTER B-H
K04	6A	SLED LOW BOOST FILTER B-L
K05	10	SLED OUTPUT GAIN
K06	14	FOCUS INPUT GAIN
K07	30	SLED AUTO GAIN
K08	7F	FOCUS HIGH CUT FILTER A
K09	46	FOCUS HIGH CUT FILTER B
K0A	81	FOCUS LOW BOOST FILTER A-H
K0B	1C	FOCUS LOW BOOST FILTER A-L
K0C	7F	FOCUS LOW BOOST FILTER B-H
K0D	58	FOCUS LOW BOOST FILTER B-L
K0E	82	FOCUS PHASE COMPENSATE FILTER A
K0F	7F	FOCUS DEFECT HOLD GAIN
K10	4E	FOCUS PHASE COMPENSATE FILTER B
K11	32	FOCUS OUTPUT GAIN
K12	20	ANTI SHOCK INPUT GAIN
K13	30	FOCUS AUTO GAIN
K14	80	HPTZC / Auto Gain HIGH PASS FILTER A
K15	77	HPTZC / Auto Gain HIGH PASS FILTER B
K16	80	ANTI SHOCK HIGH PASS FILTER A
K17	77	HPTZC / Auto Gain LOW PASS FILTER B
K18	00	Fix*
K19	F1	TRACKING INPUT GAIN
K1A	7F	TRACKING HIGH CUT FILTER A
K1B	3B	TRACKING HIGH CUT FILTER B
K1C	81	TRACKING LOW BOOST FILTER A-H
K1D	44	TRACKING LOW BOOST FILTER A-L
K1E	7F	TRACKING LOW BOOST FILTER B-H
K1F	5E	TRACKING LOW BOOST FILTER B-L
K20	82	TRACKING PHASE COMPENSATE FILTER A
K21	44	TRACKING PHASE COMPENSATE FILTER B
K22	18	TRACKING OUTPUT GAIN
K23	30	TRACKING AUTO GAIN
K24	7F	FOCUS GAIN DOWN HIGH CUT FILTER A
K25	46	FOCUS GAIN DOWN HIGH CUT FILTER B
K26	81	FOCUS GAIN DOWN LOW BOOST FILTER A-H
K27	3A	FOCUS GAIN DOWN LOW BOOST FILTER A-L
K28	7F	FOCUS GAIN DOWN LOW BOOST FILTER B-H
K29	66	FOCUS GAIN DOWN LOW BOOST FILTER B-L
K2A	82	FOCUS GAIN DOWN PHASE COMPENSATE FILTER A
K2B	44	FOCUS GAIN DOWN DEFECT HOLD GAIN
K2C	4E	FOCUS GAIN DOWN PHASE COMPENSATE FILTER B
K2D	1B	FOCUS GAIN DOWN OUTPUT GAIN
K2E	00	NOT USED
K2F	00	NOT USED

* Fix indicates that normal preset values should be used.

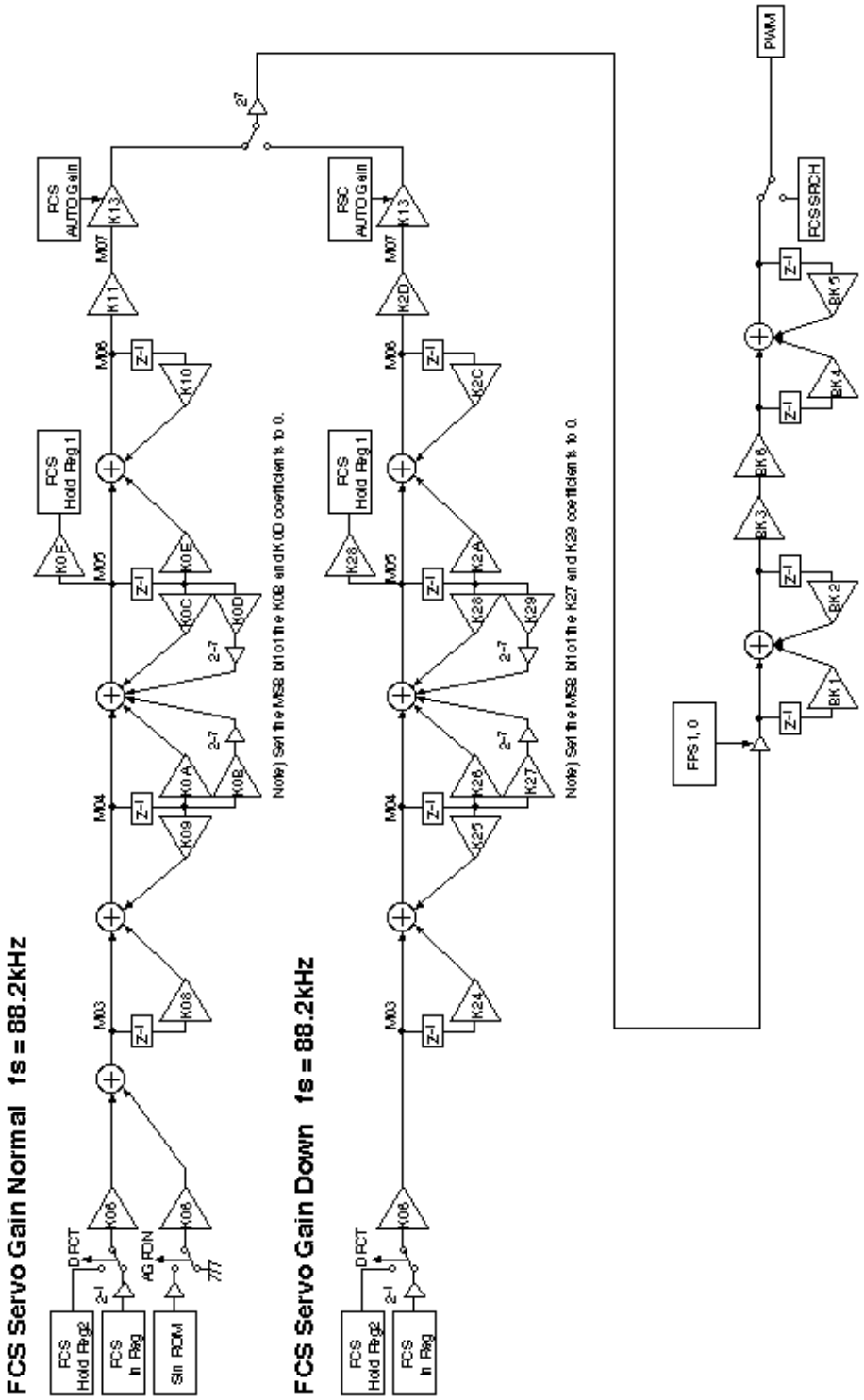
<Coefficient Preset Value Table (2)>

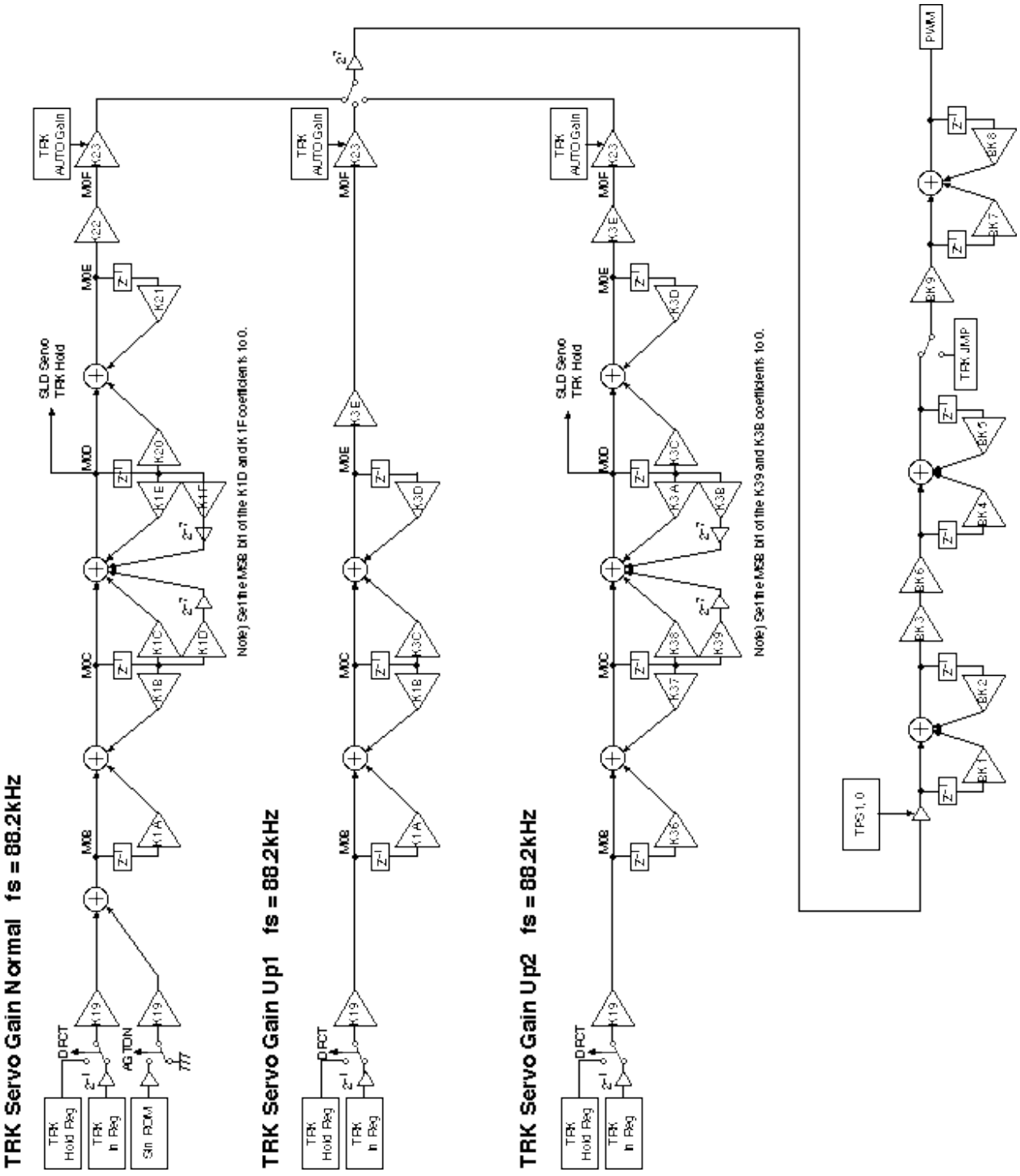
ADDRESS	DATA	CONTENTS
K30	80	SLED INPUT GAIN (Only when TRK Gain Up2 is accessed with SFSK = 1.)
K31	66	ANTI SHOCK LOW PASS FILTER B
K32	00	NOT USED
K33	7F	ANTI SHOCK HIGH PASS FILTER B-H
K34	6E	ANTI SHOCK HIGH PASS FILTER B-L
K35	20	ANTI SHOCK FILTER COMPARATE GAIN
K36	7F	TRACKING GAIN UP2 HIGH CUT FILTER A
K37	3B	TRACKING GAIN UP2 HIGH CUT FILTER B
K38	80	TRACKING GAIN UP2 LOW BOOST FILTER A-H
K39	44	TRACKING GAIN UP2 LOW BOOST FILTER A-L
K3A	7F	TRACKING GAIN UP2 LOW BOOST FILTER B-H
K3B	77	TRACKING GAIN UP2 LOW BOOST FILTER B-L
K3C	86	TRACKING GAIN UP PHASE COMPENSATE FILTER A
K3D	0D	TRACKING GAIN UP PHASE COMPENSATE FILTER B
K3E	57	TRACKING GAIN UP OUTPUT GAIN
K3F	00	NOT USED
K40	04	TRACKING HOLD FILTER INPUT GAIN
K41	7F	TRACKING HOLD FILTER A-H
K42	7F	TRACKING HOLD FILTER A-L
K43	79	TRACKING HOLD FILTER B-H
K44	17	TRACKING HOLD FILTER B-L
K45	6D	TRACKING HOLD FILTER OUTPUT GAIN
K46	00	TRACKING HOLD FILTER INPUT GAIN (Only when TRK Gain Up2 is accessed with THSK = 1.)
K47	00	NOT USED
K48	02	FOCUS HOLD FILTER INPUT GAIN
K49	7F	FOCUS HOLD FILTER A-H
K4A	7F	FOCUS HOLD FILTER A-L
K4B	79	FOCUS HOLD FILTER B-H
K4C	17	FOCUS HOLD FILTER B-L
K4D	54	FOCUS HOLD FILTER OUTPUT GAIN
K4E	00	NOT USED
K4F	00	NOT USED

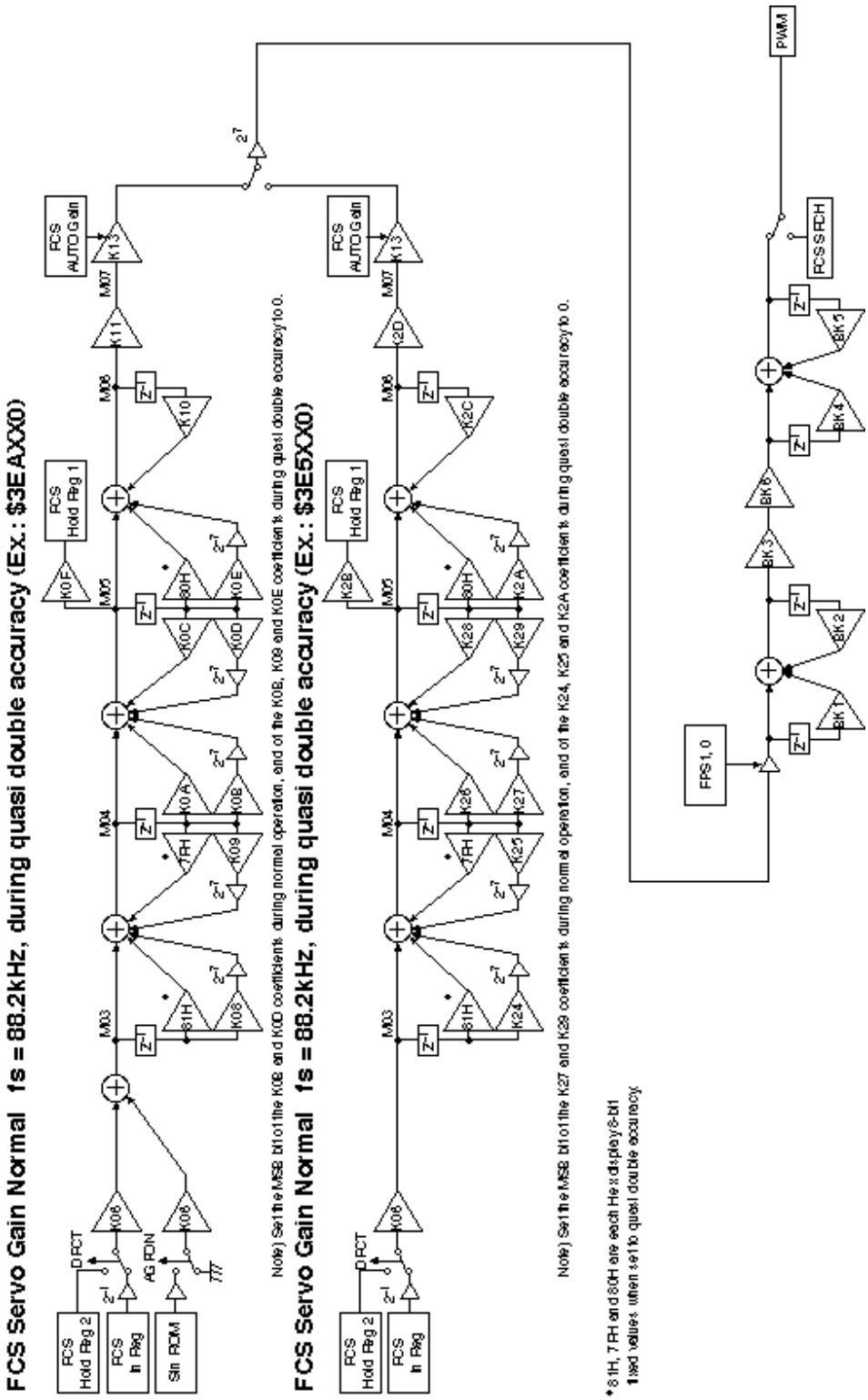
§ 5-20. Filter Composition

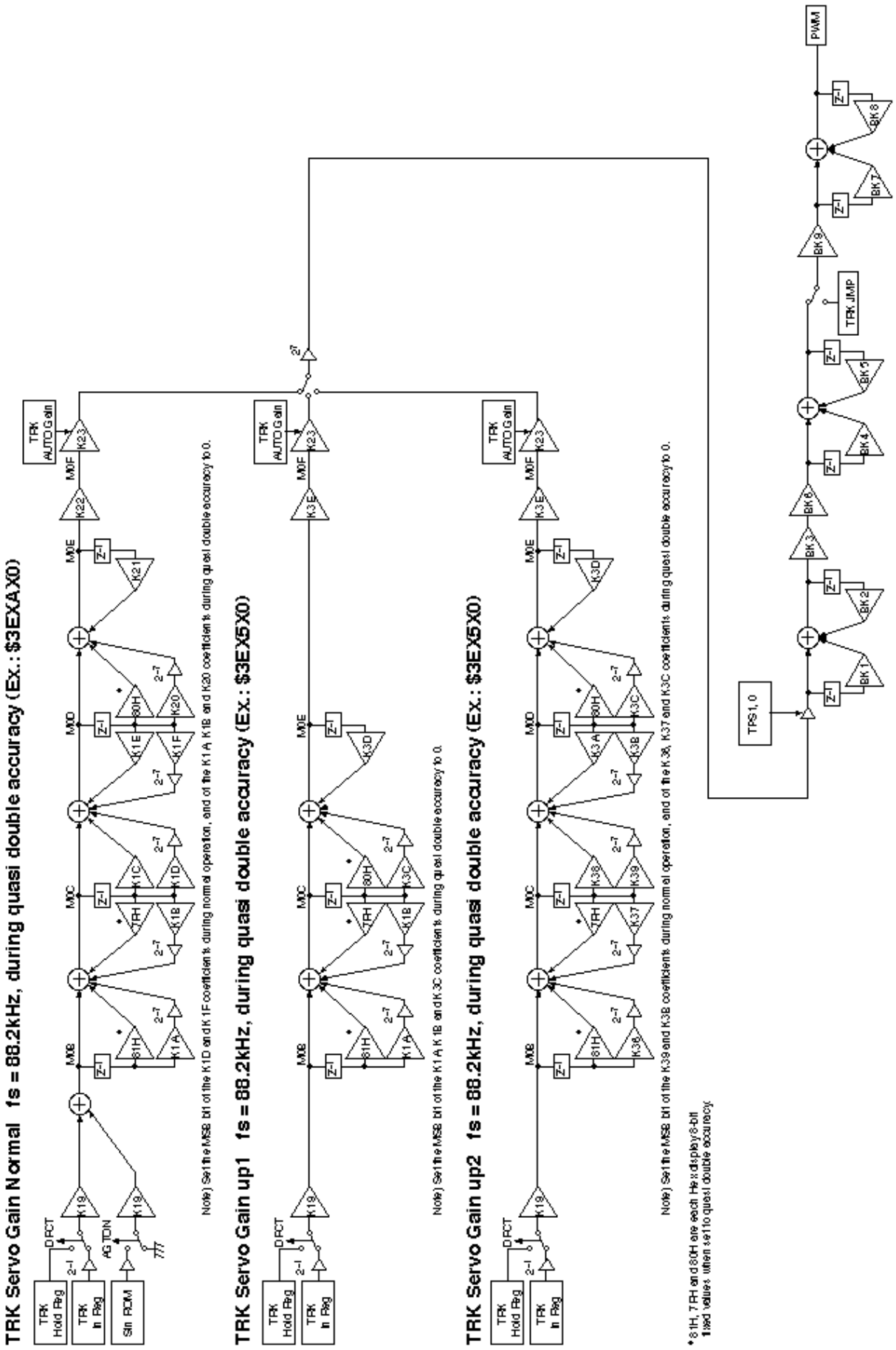
The internal filter composition is shown below.

K** and M** indicate coefficient RAM and Data RAM address values respectively.

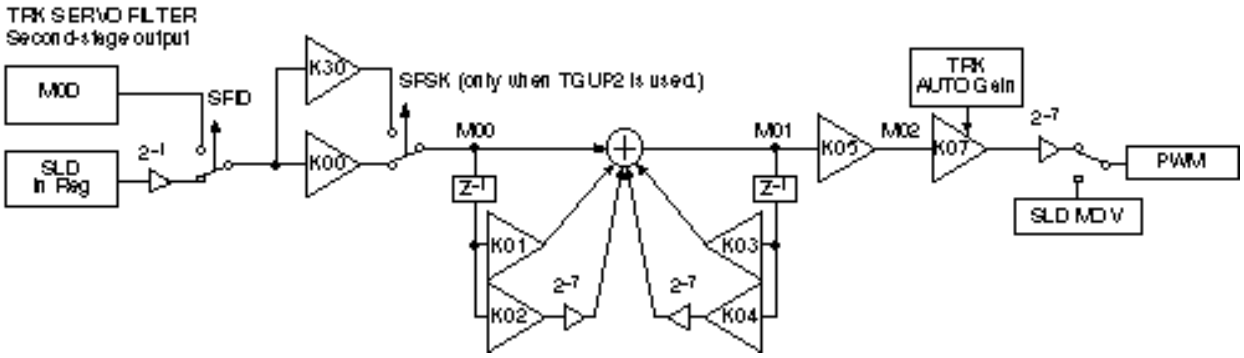



TRK Servo Gain Normal fs = 88.2kHz
TRK Servo Gain Up1 fs = 88.2kHz
TRK Servo Gain Up2 fs = 88.2kHz
TRK Hold Reg
TRK In Reg
Sin ROM
DCT
AGTON
TRK AUTO Gain
SLD Servo TRK Hold
TRK JMP
PWM
TPS1, 0
Note) Set the MSB bit of the K1D and K1F coefficients to 0.
Note) Set the MSB bit of the K39 and K3B coefficients to 0.


FCS Servo Gain Normal 1s = 88.2kHz, during quasi double accuracy (Ex.: $3EAXX0)
FCS Hold Reg 2
FCS In Reg
Sin ROM
DRCT
AG RDIN
K06
Z-1
M03
81H
K08
M04
7FH
K09
K0A
K0B
M05
80H
K0C
K0D
K0E
FCS Hold Reg 1
K0F
M06
K10
M07
K11
FCS AUTO Gain
K13
Note) Set the MSB bit of the K08 and K0D coefficients during normal operation, and of the K0B, K09 and K0E coefficients during quasi double accuracy to 0.
FCS Servo Gain Normal 1s = 88.2kHz, during quasi double accuracy (Ex.: $3E5XX0)
K24
K25
K26
K27
K28
K29
K2A
K2C
K2D
Note) Set the MSB bit of the K27 and K29 coefficients during normal operation, and of the K24, K25 and K2A coefficients during quasi double accuracy to 0.
* 81H, 7FH and 80H are each Hex displayed 6-bit
fixed values when set to quasi double accuracy.
FPS1, 0
BK1
BK2
BK3
BK4
BK5
BK6
FCS SRDH
PWM

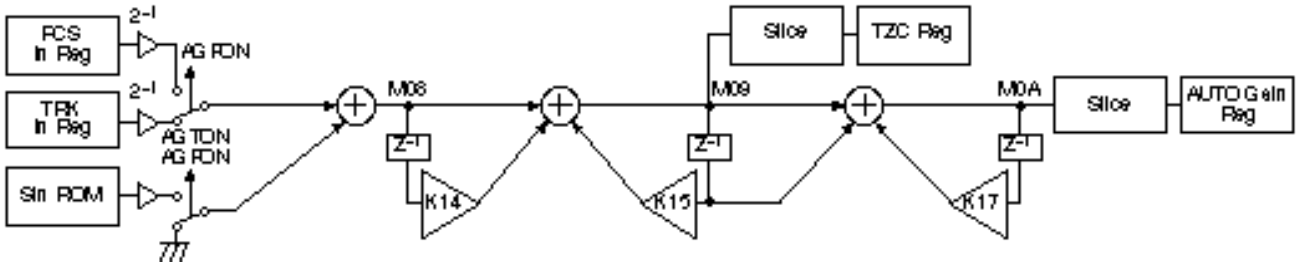

TRK Servo Gain Normal fs = 88.2kHz, during quasi double accuracy (Ex.: $3EXA0)
TRK Servo Gain up1 fs = 88.2kHz, during quasi double accuracy (Ex.: $3EX50)
TRK Servo Gain up2 fs = 88.2kHz, during quasi double accuracy (Ex.: $3EX50)
TRK Hold Reg
TRK In Reg
Sin ROM
DRCT
AGTON
TRK AUTO Gain
TPS1, 0
TRK JMP
PWM
Note) Set the MSB bit of the K1D and K1F coefficients during normal operation, and of the K1A, K1B and K20 coefficients during quasi double accuracy to 0.
Note) Set the MSB bit of the K1A, K1B and K3C coefficients during quasi double accuracy to 0.
Note) Set the MSB bit of the K39 and K3B coefficients during normal operation, and of the K38, K37 and K3C coefficients during quasi double accuracy to 0.
*81H, TRH and 80H are each Hex display 8-bit fixed values when set to quasi double accuracy.

SLD Servo fs = 345Hz

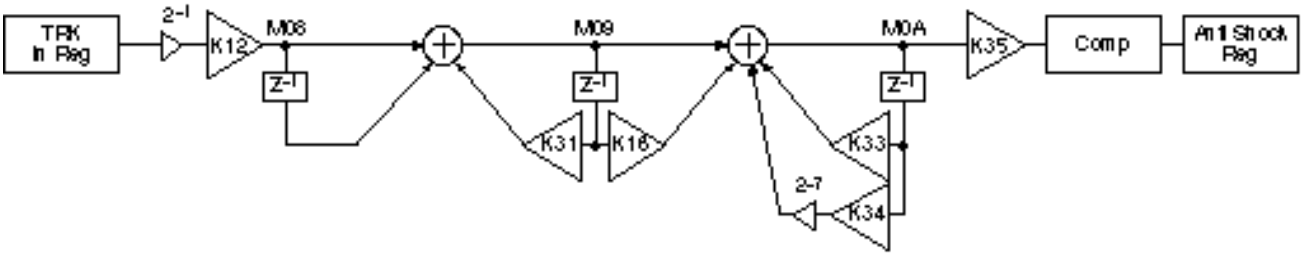


Note) Set the MSB bit of the K02 and K04 coefficients to 0.

HPTZC/Auto Gain fs = 88.2kHz

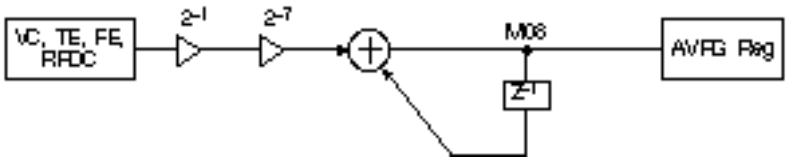


Anti Shock fs = 88.2kHz

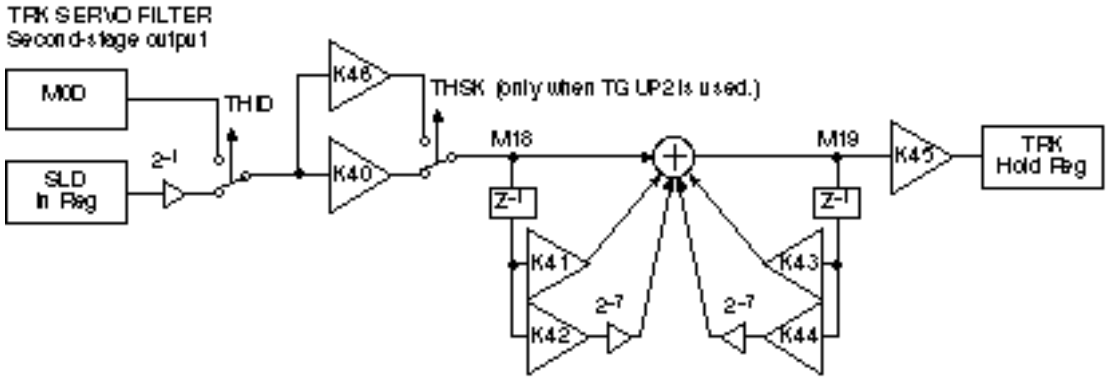


Note) Set the MSB bit of the K34 coefficient to 0.
The comparator level is 1/16 the maximum amplitude of the comparator input.

AVRG fs = 88.2kHz

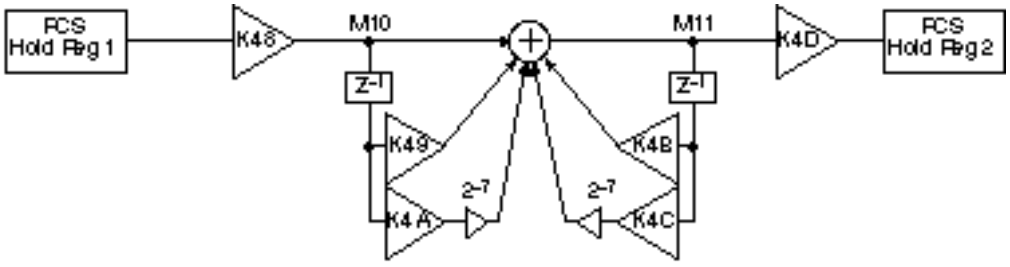


TRK Hold fs = 345Hz



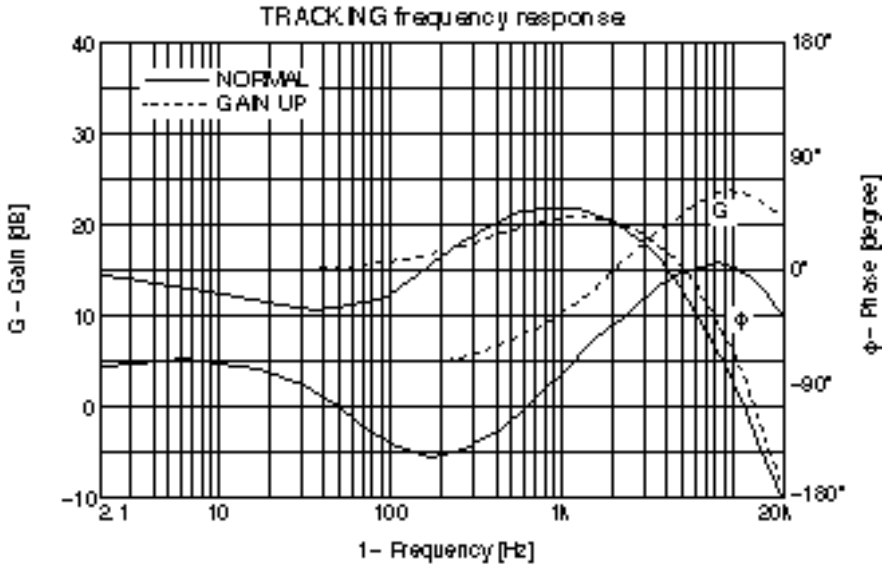
Note) Set the MSB bit of the K42 and K44 coefficients to 0.

FCS Hold fs = 345Hz

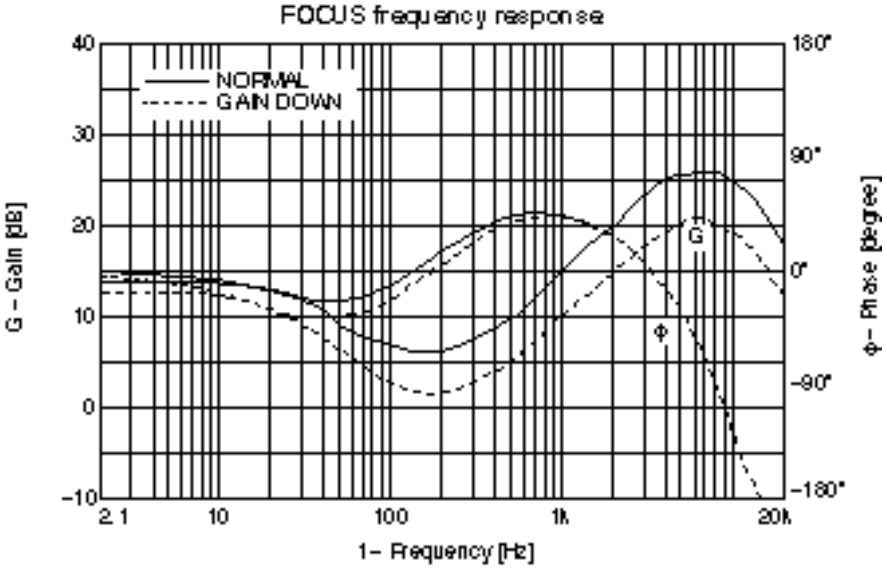


Note) Set the MSB bit of the K4A and K4C coefficients to 0.

§ 5-21. TRACKING and FOCUS Frequency Response

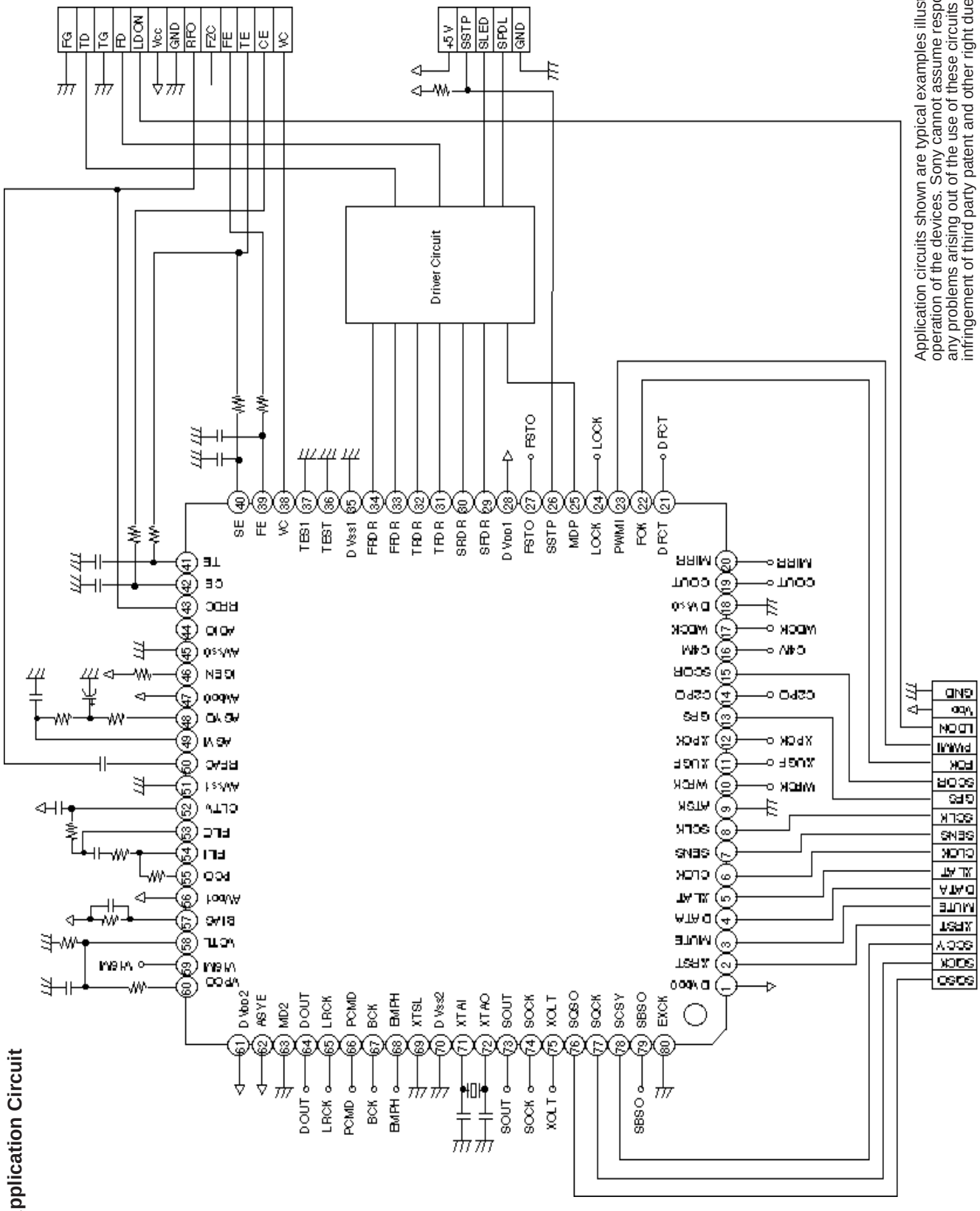


When using the preset coefficients with the boost function off.



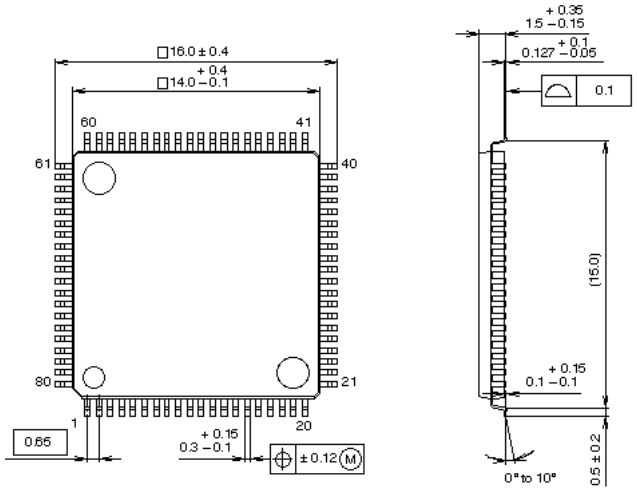
When using the preset coefficients with the boost function off.

[6] Application Circuit



Package Outline Unit: mm

80PIN QFP (PLASTIC)

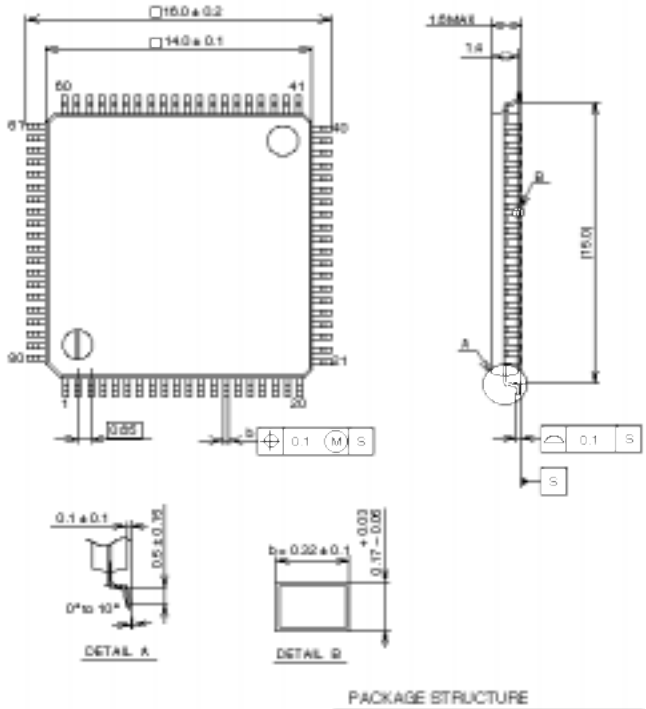


PACKAGE STRUCTURE

SONY CODE	QFP-80P-L03
EIAJ CODE	LQFP080-P-1414
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.6g

80PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-80P-L052
EIAJ CODE	P-QFP80-14X14-0.65
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	1.6 g

2 Megabit (256K x 8) Multi-Purpose Flash
SST39VF020

Preliminary Specifications

FEATURES:

- **Organized as 256K X 8**
- **Single 2.7-3.6V Read and Write Operations**
- **Superior Reliability**
  - Endurance: 100,000 Cycles (typical)
  - Greater than 100 years Data Retention
- **Low Power Consumption:**
  - Active Current: 10 mA (typical)
  - Standby Current: 10 µA (typical)
- **Sector Erase Capability**
  - Uniform 4 KByte sectors
- **Fast Read Access Time:**
  - 70 and 90 ns
- **Latched Address and Data**
- **Fast Sector Erase and Byte Program:**
  - Sector Erase Time: 18 ms typical
  - Chip Erase Time: 70 ms typical
  - Byte Program time: 14 µs typical
  - Chip Rewrite Time: 4 seconds typical
- **Automatic Write Timing**
  - Internal V_{pp} Generation
- **End of Write Detection**
  - Toggle Bit
  - Data# Polling
- **CMOS I/O Compatibility**
- **JEDEC Standard**
  - EEPROM Pinouts and command set
- **Packages Available**
  - 32-Pin PDIP
  - 32-Pin PLCC
  - 32-Pin TSOP (8x14mm)

PRODUCT DESCRIPTION

The SST39VF020 is a 256K x 8 CMOS Multi-Purpose Flash (MPF) manufactured with SST's proprietary, high performance CMOS SuperFlash technology. The split gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST39VF020 device writes (Program or Erase) with a 2.7-3.6V power supply. The SST39VF020 device conforms to JEDEC standard pinouts for x8 memories.

Featuring high performance byte program, the SST39VF020 device provides a maximum byte-program time of 20 µsec. The entire memory can be erased and programmed byte by byte typically in 4 seconds, when using interface features such as Toggle Bit or Data# Polling to indicate the completion of Program operation. To protect against inadvertent write, the SST39VF020 device has on-chip hardware and software data protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, the SST39VF020 device is offered with a guaranteed endurance of 10,000 cycles. Data retention is rated at greater than 100 years.

The SST39VF020 device is suited for applications that require convenient and economical updating of program, configuration, or data memory. For all system applications, the SST39VF020 device significantly improves performance and reliability, while lowering power consumption. The SST39VF020 inherently uses less energy during erase and program than alternative flash technologies. The total energy consumed is a function of the applied voltage, current, and time of application. Since for any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative flash technologies. The SST39VF020 device also improves flexibility while lowering the cost for program, data, and configuration storage applications.

The SuperFlash technology provides fixed Erase and Program times, independent of the number of endurance cycles that have occurred. Therefore the system software or hardware does not have to be modified or derated as is necessary with alternative flash technologies, whose erase and program times increase with accumulated endurance cycles.

To meet high density, surface mount requirements, the SST39VF020 device is offered in 32-pin TSOP and 32-pin PLCC packages. A 600 mil, 32-pin PDIP is also available. See Figures 1 and 2 for pinouts.

Device Operation

Commands are used to initiate the memory operation functions of the device. Commands are written to the device using standard microprocessor write sequences. A command is written by asserting WE# low while

keeping CE# low. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first.

Read

The Read operation of the SST39VF020 device is controlled by CE# and OE#, both have to be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high. Refer to the Read cycle timing diagram for further details (Figure 3).

Byte Program Operation

The SST39VF020 device is programmed on a byte-by-byte basis. The Program operation consists of three steps. The first step is the three-byte-load sequence for Software Data Protection. The second step is to load byte address and byte data. During the Byte Program operation, the addresses are latched on the falling edge of either CE# or WE#, whichever occurs last. The data is latched on the rising edge of either CE# or WE#, whichever occurs first. The third step is the internal Program operation which is initiated after the rising edge of the fourth WE# or CE#, whichever occurs first. The Program operation, once initiated, will be completed, within 20 µs. See Figures 4 and 5 for WE# and CE# controlled Program operation timing diagrams and Figure 14 for flowcharts. During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands written during the internal Program operation will be ignored.

Sector Erase Operation

The Sector Erase operation allows the system to erase the device on a sector by sector basis. The sector architecture is based on uniform sector size of 4 KByte. The Sector Erase operation is initiated by executing a six-byte-command load sequence for software data protection with sector erase command (30H) and sector address (SA) in the last bus cycle. The address lines A12-A17 will be used to determine the sector address. The sector address is latched on the falling edge of the sixth WE# pulse , while the command (30H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. The end of Erase can be determined using either Data# Polling or Toggle Bit methods. See Figure 8 for timing waveforms. Any commands written during the Sector Erase operation will be ignored.

Chip Erase Operation

The SST39VF020 device provides a Chip Erase operation, which allows the user to erase the entire memory array to the “1’s” state. This is useful when the entire device must be quickly erased.

The Chip Erase operation is initiated by executing a six-byte software data protection command sequence with Chip Erase command (10H) with address 5555H in the last byte sequence. The internal Erase operation begins with the rising edge of the sixth WE# or CE#, whichever occurs first. During the internal Erase operation, the only valid read is Toggle Bit or Data# Polling. See Table 4 for the command sequence, Figure 9 for timing diagram, and Figure 17 for the flowchart. Any commands written during the Chip Erase operation will be ignored.

Write Operation Status Detection

The SST39VF020 device provides two software means to detect the completion of a Write (Program or Erase) cycle, in order to optimize the system write cycle time. The software detection includes two status bits : Data# Polling (DQ_7) and Toggle Bit (DQ_6). The end of write detection mode is enabled after the rising edge of WE# which initiates the internal Program or Erase operation.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ_7 or DQ_6. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

Data# Polling (DQ_7)

When the SST39VF020 device is in the internal Program operation, any attempt to read DQ_7 will produce the complement of the true data. Once the Program operation is completed, DQ_7 will produce true data. The device is then ready for the next operation. During internal Erase operation, any attempt to read DQ7 will produce a ‘0’. Once the internal Erase operation is completed, DQ7 will produce a ‘1’. The Data# Polling is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For sector or chip erase, the Data# Polling is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 6 for Data# Polling timing diagram and Figure 15 for a flowchart.

Toggle Bit (DQ_6)

During the internal Program or Erase operation, any consecutive attempts to read DQ_6 will produce alternating 0's and 1's, i.e., toggling between 0 and 1. When the internal Program or Erase operation is completed, the toggling will stop. The device is then ready for the next operation. The Toggle Bit is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector or Chip Erase, the Toggle Bit is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 7 for Toggle Bit timing diagram and Figure 15 for a flowchart.

Data Protection

The SST39VF020 device provides both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# or CE# pulse of less than 5 ns will not initiate a write cycle.

V_{DD} Power Up/Down Detection: The Write operation is inhibited when V_{DD} is less than 1.5V.

Write Inhibit Mode: Forcing OE# low, CE# high, or WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.

Software Data Protection (SDP)

The SST39VF020 provides the JEDEC approved software data protection scheme for all data alteration operation, i.e., program and erase. Any Program operation requires the inclusion of a series of three byte sequence. The three byte-load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. Any Erase operation requires the inclusion of six byte load sequence. The SST39VF020 device is shipped with the software data protection permanently enabled. See Table 4 for the specific software command codes. During SDP command sequence, invalid commands will abort the device to read mode, within T_{RC}.

Product Identification

The product identification mode identifies the device as the SST39VF020 and manufacturer as SST. This mode may be accessed by hardware or software operations. The hardware operation is typically used by a programmer to identify the correct algorithm for the SST39VF020 device. Users may wish to use the software product identification operation to identify the part (i.e., using the device code) when using multiple manufacturers in the same socket. For details, see Table 3 for hardware operation or Table 4 for software operation, Figure 10 for the software ID entry and read timing diagram and Figure 16 for the ID entry command sequence flowchart.

TABLE 1: PRODUCT IDENTIFICATION TABLE

	Address	Data
Manufacturer's Code	0000H	BF H
Device Code	0001H	D6 H

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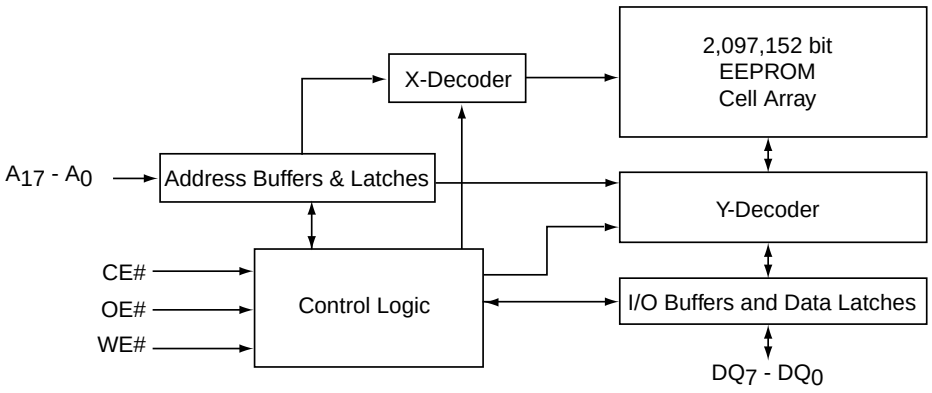
Product Identification Mode Exit/Reset

In order to return to the standard read mode, the Software Product Identification mode must be exited. Exiting is accomplished by issuing the Exit ID command sequence, which returns the device to the Read operation. Please note that the software reset command is ignored during an internal Program or Erase operation. See Table 4 for software command codes, Figure 11 for timing waveform and Figure 16 for a flowchart.

FUNCTIONAL BLOCK DIAGRAM OF SST39VF020



336 ILL B1.0

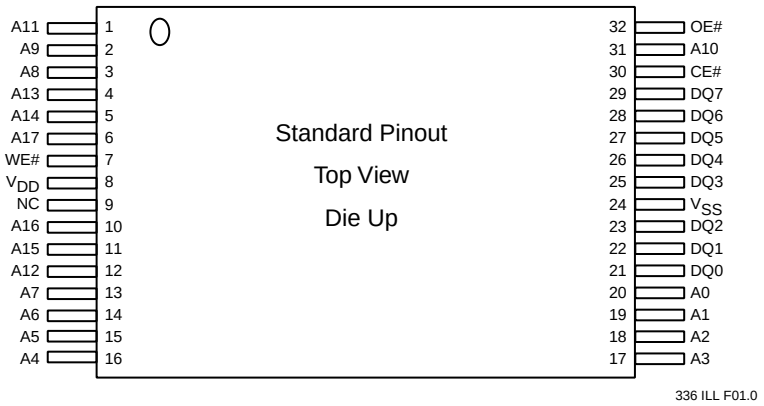


FIGURE 1: PIN ASSIGNMENTS FOR 32-PIN TSOP PACKAGE (8mm x 14mm)

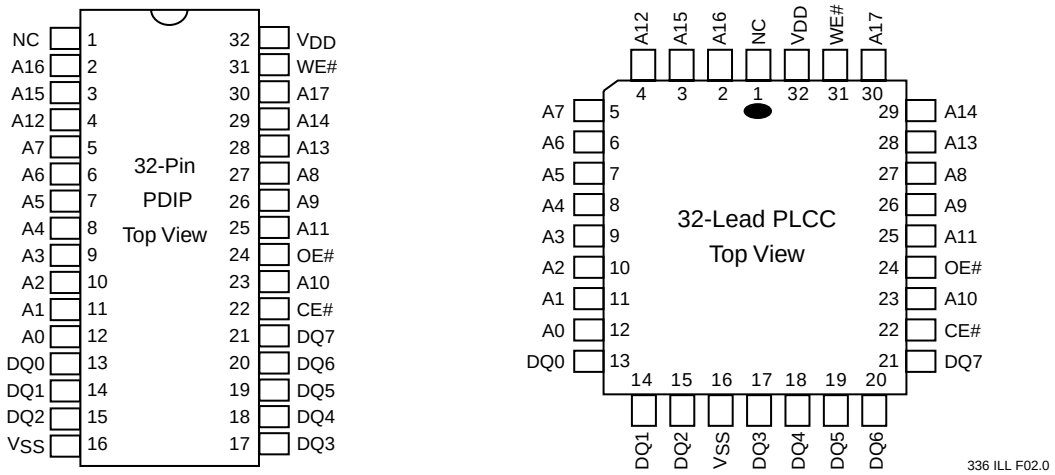


FIGURE 2: PIN ASSIGNMENTS FOR 32-PIN PLASTIC DIPS AND 32-LEAD PLCCS

TABLE 2: PIN DESCRIPTION

Symbol	Pin Name	Functions
A_{17}-A_0	Address Inputs	To provide memory addresses. During sector erase A_{17}-A_{12} address lines will select the sector.
DQ_7-DQ_0	Data Input/output	To output data during read cycles and receive input data during write cycles. Data is internally latched during a write cycle. The outputs are in tri-state when OE# or CE# is high.
CE#	Chip Enable	To activate the device when CE# is low.
OE#	Output Enable	To gate the data output buffers.
WE#	Write Enable	To control the write operations.
V_{DD}	Power Supply	To provide 2.7-3.6V supply
Vss	Ground	
NC	No Connection	Unconnected pins

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TABLE 3: OPERATION MODES SELECTION

Mode	CE#	OE#	WE#	A9	DQ	Address
Read	V_{IL}	V_{IL}	V_{IH}	A_{IN}	D_{OUT}	A_{IN}
Program	V_{IL}	V_{IH}	V_{IL}	A_{IN}	D_{IN}	A_{IN}
Erase	V_{IL}	V_{IH}	V_{IL}	X	X	Sector address, XXh for chip erase
Standby	V_{IH}	X	X	X	High Z	X
Write Inhibit	X	V_{IL}	X	X	High Z/D_{OUT}	X
	X	X	V_{IH}	X	High Z/D_{OUT}	X
Product Identification						
Hardware Mode	V_{IL}	V_{IL}	V_{IH}	V_H	Manufacturer Code (BF) Device Code (D6)	A_{17} - A_1 = V_{IL}, A_0 = V_{IL} A_{17} - A_1 = V_{IL}, A_0 = V_{IH}
Software Mode	V_{IL}	V_{IL}	V_{IH}	A_{IN}	ID Code	See Table 4

336 PGM T3.0

TABLE 4: SOFTWARE COMMAND SEQUENCE

Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data	Addr[1]	Data
Byte Program	5555H	AAH	2AAAH	55H	5555H	A0H	BA[3]	Data				
Sector Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA_x[2]	30H
Chip Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Software ID Entry	5555H	AAH	2AAAH	55H	5555H	90H						
Software ID Exit	XXH	F0H										
Software ID Exit	5555H	AAH	2AAAH	55H	5555H	F0H						

336 PGM T4.0

Notes:

(1) Address format A_{14}-A_0 (Hex), Addresses A_{15}, A_{16} and A_{17} are a "Don't Care" for the Command sequence.

(2) SA_x for sector erase; uses A_{17}-A_{12} address lines

(3) BA = Program Byte address

(4) Both Software ID Exit operations are equivalent

Notes for Software ID Entry Command Sequence

1. With A_{17} -A_1 =0; SST Manufacturer Code = BFH, is read with A_0 = 0,
   SST39VF020 Device Code = D6H, is read with A_0 = 1.
2. The device does not remain in Software Product ID Mode if powered down.

Preliminary Specifications

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential ..... -0.5V to V_{DD}+ 0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential ..... -1.0V to V_{DD}+ 1.0V
Voltage on A_9 Pin to Ground Potential ..... -0.5V to 13.2V
Package Power Dissipation Capability (Ta = 25°C) 1.0W
Through Hole Lead Soldering Temperature (10 Seconds) ..... 300°C
Surface Mount Lead Soldering Temperature (3 Seconds) ..... 240°C
Output Short Circuit Current(1) ..... 50 mA

Note: (1) Outputs shorted for no more than one second. No more than one output shorted at a time.

OPERATING RANGE

Range	Ambient Temp	V_{DD}
Commercial	0 °C to +70 °C	2.7 - 3.6V
Industrial	-40 °C to +85 °C	2.7 - 3.6V

AC CONDITIONS OF TEST

Input Rise/Fall Time ..... 10 ns
Output Load ..... C_L = 100 pF
See Figures 12 and 13

TABLE 5: DC OPERATING CHARACTERISTICS V_{DD} = 2.7-3.6V

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{DD}	Power Supply Current Read		12	mA	CE#=OE#=V_{IL},WE#=V_{IH} , all I/Os open, Address input = V_{IL}/V_{IH}, at f=1/T_{RC} Min., V_{DD}=V_{DD} Max
	Write		15	mA	CE#=WE#=V_{IL}, OE#=V_{IH}, V_{DD} =V_{DD} Max.
I_{SB}	Standby V_{DD} Current		15	µA	CE#=V_{IHC}, V_{DD} = V_{DD} Max.
I_{LI}	Input Leakage Current		1	µA	V_{IN} =GND to V_{DD}, V_{DD} = V_{DD} Max.
I_{LO}	Output Leakage Current		1	µA	V_{OUT} =GND to V_{DD}, V_{DD} = V_{DD} Max.
V_{IL}	Input Low Voltage		0.8	V	V_{DD} = V_{DD} Min.
V_{IH}	Input High Voltage	2.0		V	V_{DD} = V_{DD} Max.
V_{IHC}	Input High Voltage (CMOS)	V_{DD}-0.3		V	V_{DD} = V_{DD} Max.
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 100 µA, V_{DD} = V_{DD} Min.
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -100µA, V_{DD} = V_{DD} Min.
V_H	Supervoltage for A_9 pin	11.4	12.6	V	CE# = OE# =V_{IL}, WE# = V_{IH}
I_H	Supervoltage Current for A_9 pin		200	µA	CE# = OE# = V_{IL}, WE# = V_{IH}, A_9 = V_H Max.

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TABLE 6: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$(1)	Power-up to Read Operation	100	µs
$T_{PU-WRITE}$(1)	Power-up to Write Operation	100	µs

336 PGM T6.0

TABLE 7: CAPACITANCE (Ta = 25 °C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$(1)	I/O Pin Capacitance	$V_{I/O}$ = 0V	12 pF
C_{IN}(1)	Input Capacitance	V_{IN} = 0V	6 pF

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Note: (1)This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 8: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}(1)	Endurance	10,000	Cycles	JEDEC Standard A117
T_{DR}(1)	Data Retention	100	Years	JEDEC Standard A103
V_{ZAP_HBM}(1)	ESD Susceptibility Human Body Model	1000	Volts	JEDEC Standard A114
V_{ZAP_MM}(1)	ESD Susceptibility Machine Model	200	Volts	JEDEC Standard A115
I_{LTH}(1)	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

336 PGM T8.1

Note: (1)This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

AC CHARACTERISTICS

TABLE 9: READ CYCLE TIMING PARAMETERS V_{DD} = 2.7-3.6V

		SST39VF020-70		SST39VF020-90		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
T_{RC}	Read Cycle time	70		90		ns
T_{CE}	Chip Enable Access Time		70		90	ns
T_{AA}	Address Access Time		70		90	ns
T_{OE}	Output Enable Access Time		35		45	ns
T_{CLZ}(1)	CE# Low to Active Output	0		0		ns
T_{OLZ}(1)	OE# Low to Active Output	0		0		ns
T_{CHZ}(1)	CE# High to High-Z Output		15		20	ns
T_{OHZ}(1)	OE# High to High-Z Output		15		20	ns
T_{OH}(1)	Output Hold from Address Change	0		0		ns

336 PGM T9.1

TABLE 10: PROGRAM/ERASE CYCLE TIMING PARAMETERS

Symbol	**Parameter**	**Min**	**Max**	**Units**
T_{BP}	Byte Program time		20	µs
T_{AS}	Address Setup Time	0		ns
T_{AH}	Address Hold Time	30		ns
T_{CS}	WE# and CE# Setup Time	0		ns
T_{CH}	WE# and CE# Hold Time	0		ns
T_{OES}	OE# High Setup Time	0		ns
T_{OEH}	OE# High Hold Time	10		ns
T_{CP}	CE# Pulse Width	40		ns
T_{WP}	WE# Pulse Width	40		ns
T_{WPH}	WE# Pulse Width High	30		ns
T_{CPH}	CE# Pulse Width High	30		ns
T_{DS}	Data Setup Time	40		ns
T_{DH}	Data Hold Time	0		ns
T_{IDA}	Software ID Access and Exit Time		150	ns
T_{SE}	Sector Erase		25	ms
T_{SCE}	Chip Erase		100	ms

336 PGM T10.2

Note: (1)This parameter is measured only for initial qualification and after the design or process change that could affect this parameter.

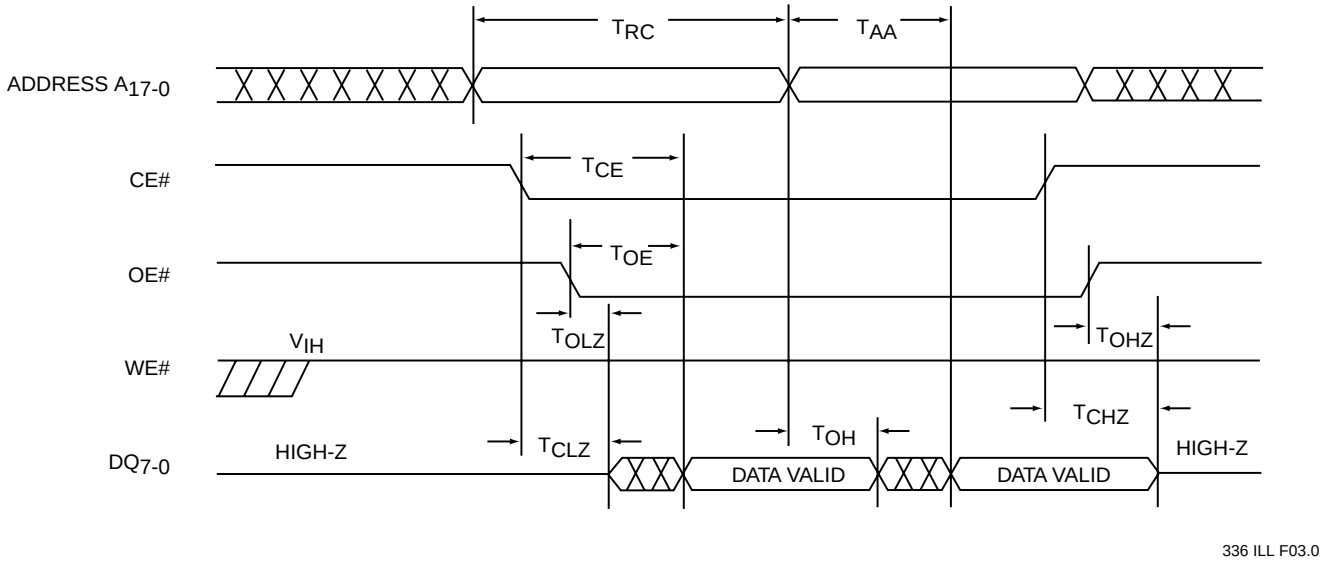


FIGURE 3: READ CYCLE TIMING DIAGRAM

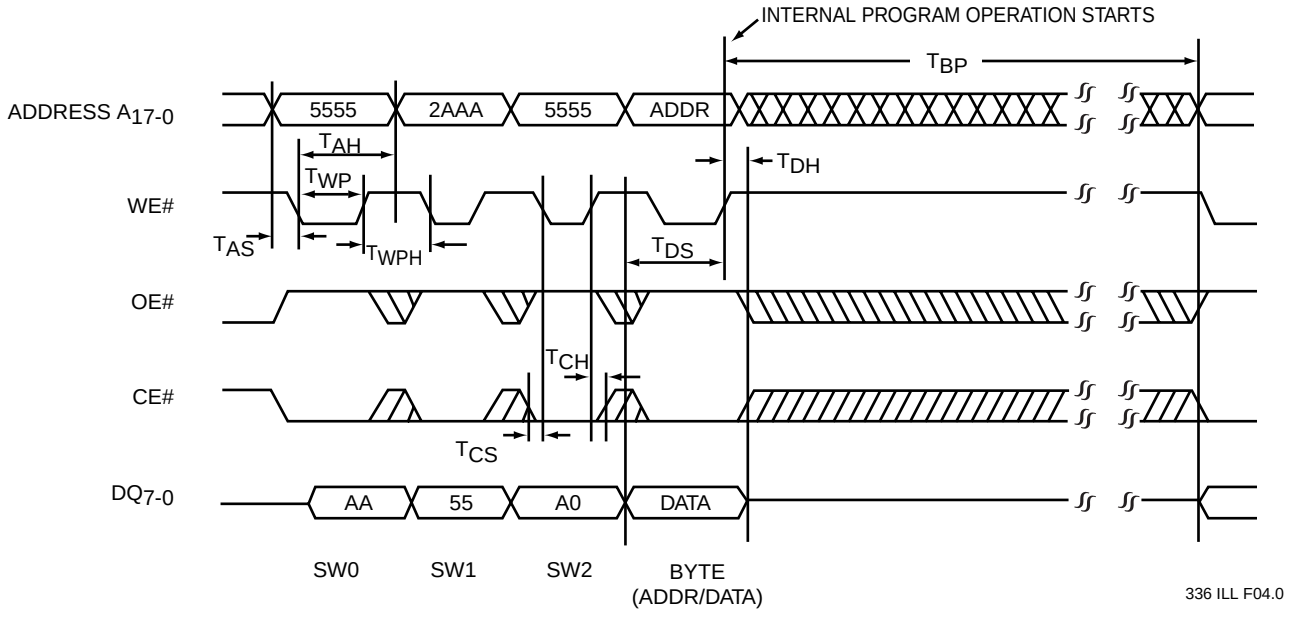


FIGURE 4: WE# CONTROLLED PROGRAM CYCLE TIMING DIAGRAM

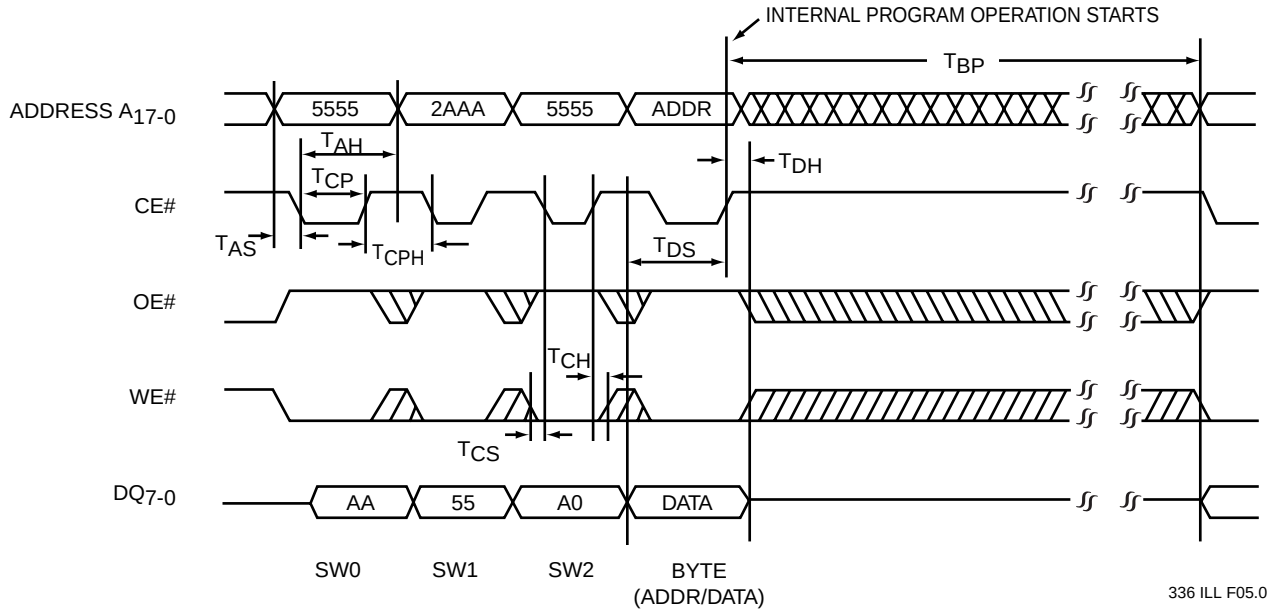


FIGURE 5: CE# CONTROLLED PROGRAM CYCLE TIMING DIAGRAM

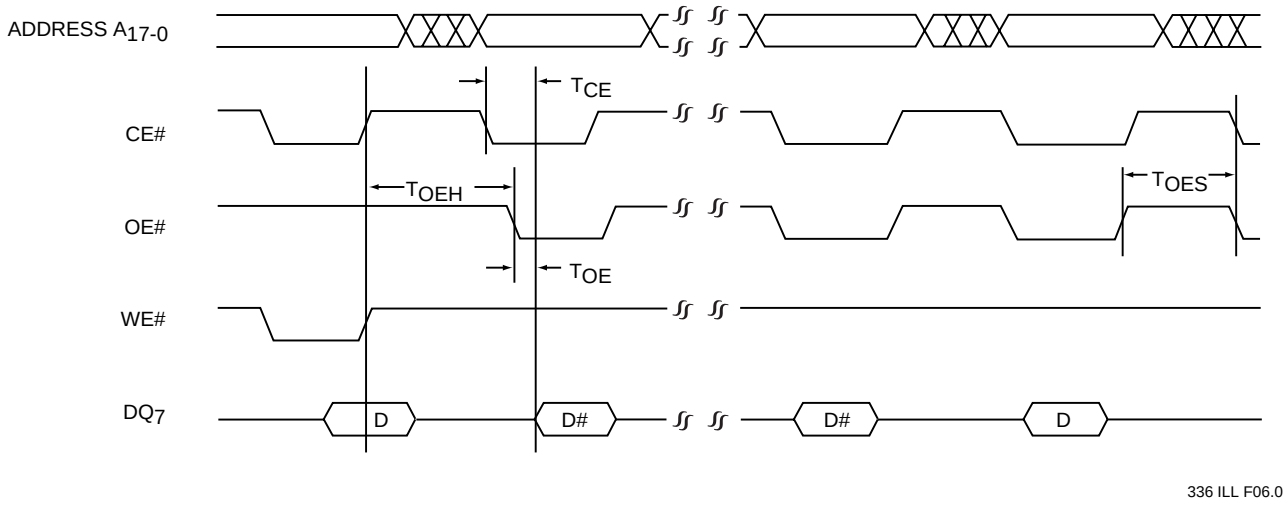


FIGURE 6: DATA# POLLING TIMING DIAGRAM

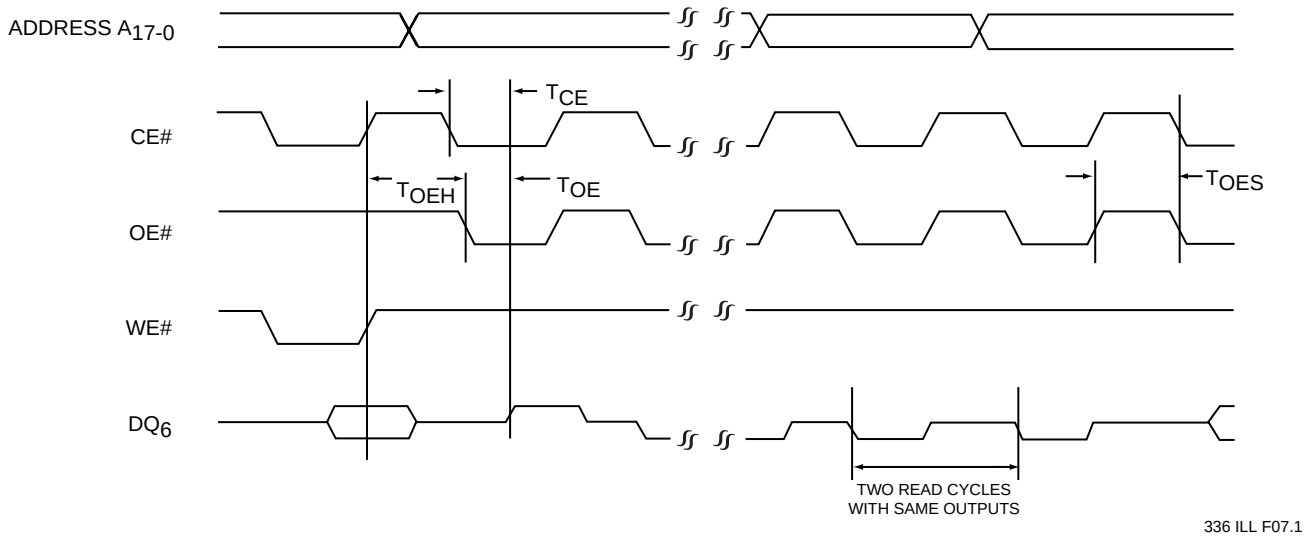
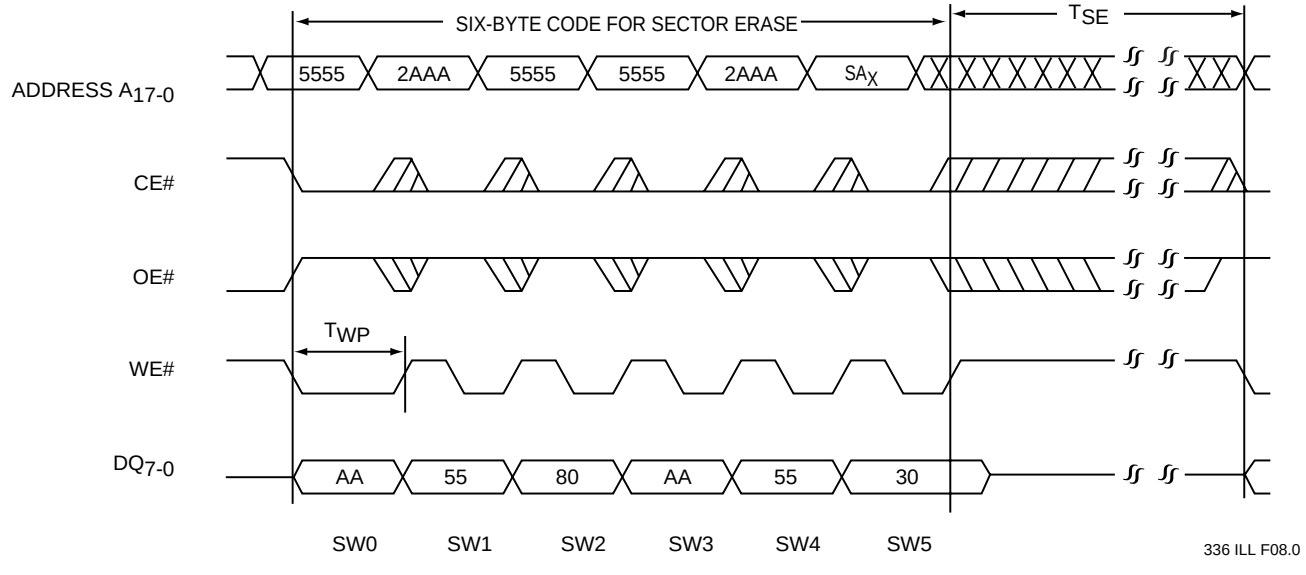
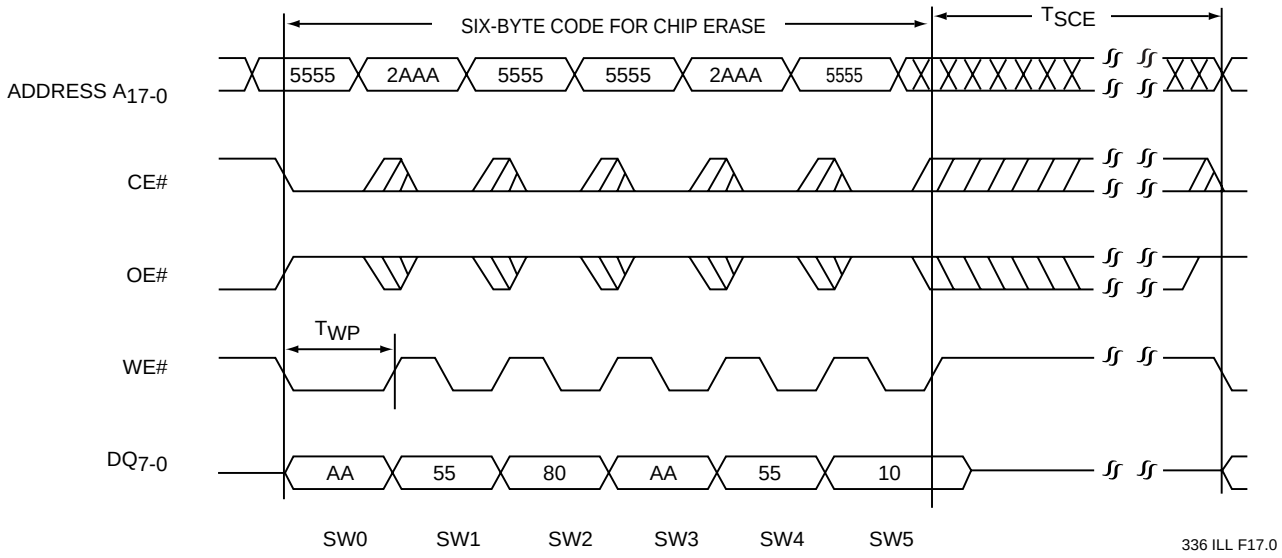


FIGURE 7: TOGGLE BIT TIMING DIAGRAM



Note: The device also supports CE# controlled sector erase operation. The WE# and CE# signals are interchangeable as long as minimum timings are met. (See Table 10)
SA_X = Sector Address

FIGURE 8: WE# CONTROLLED SECTOR ERASE TIMING DIAGRAM



Note: The device also supports CE# controlled chip erase operation. The WE# and CE# signals are interchangeable as long as minimum timings are met. (See Table 10)

FIGURE 9: WE# CONTROLLED CHIP ERASE TIMING DIAGRAM

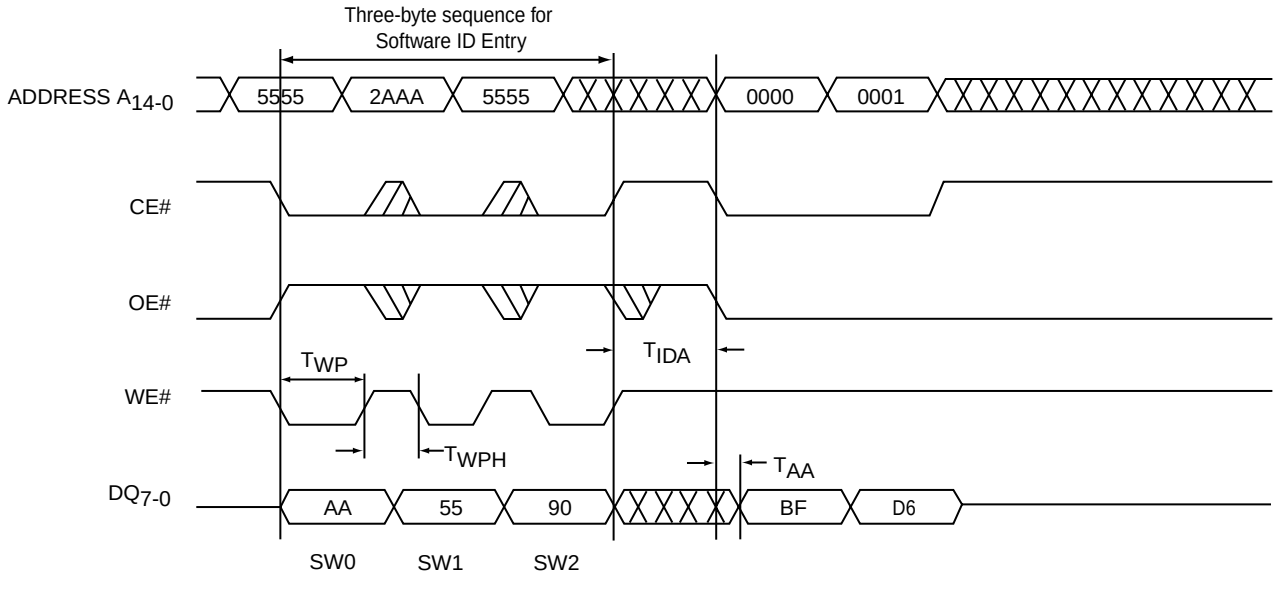


FIGURE 10: SOFTWARE ID ENTRY AND READ

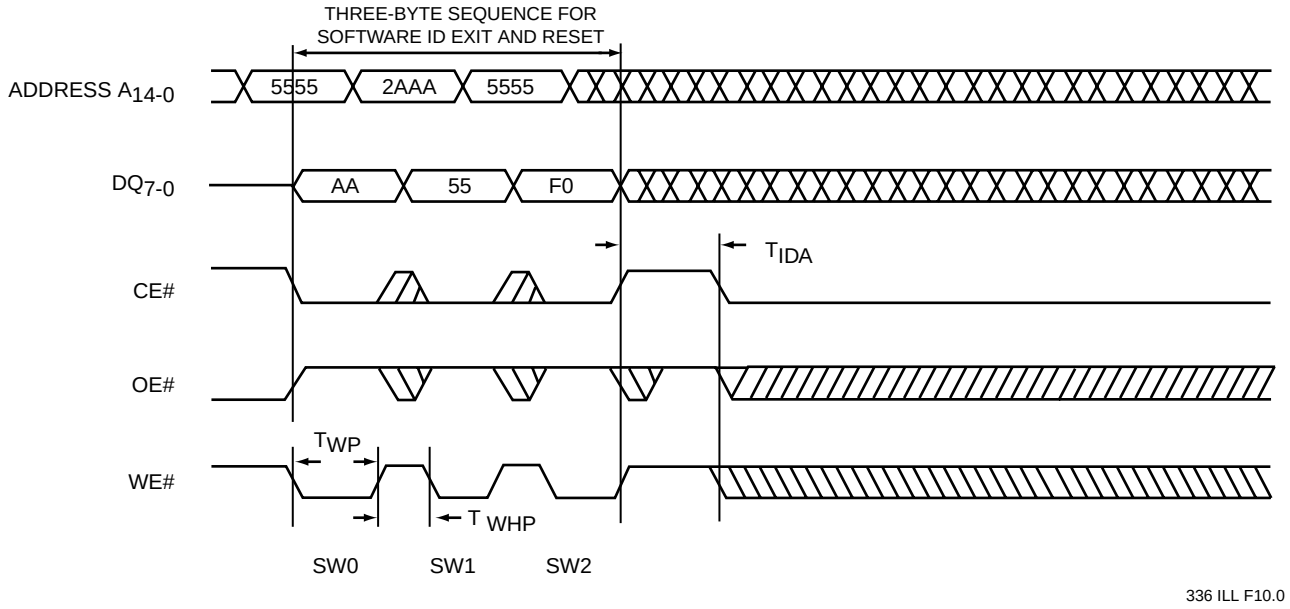
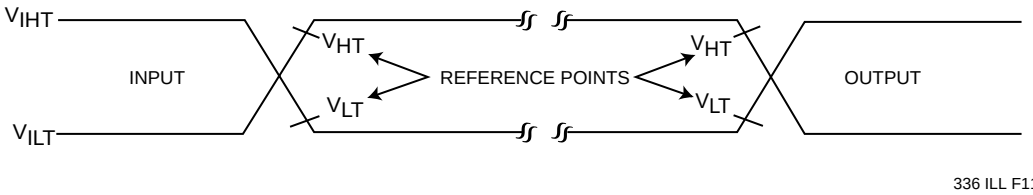


FIGURE 11: SOFTWARE ID EXIT AND RESET



AC test inputs are driven at V_{IHT} (2.4 V) for a logic "1" and V_{ILT} (0.4 V) for a logic "0".
Measurement reference points for inputs and outputs are at V_{HT} (2.0 V) and V_{LT} (0.8 V)
Input rise and fall times (10% ↔ 90%) are <10 ns.

Note: V_{HT}–V_{HIGH} Test
V_{LT}–V_{LOW} Test
V_{IHT}–V_{INPUT} HIGH Test
V_{ILT}–V_{INPUT} LOW Test

FIGURE 12: AC INPUT/OUTPUT REFERENCE WAVEFORMS

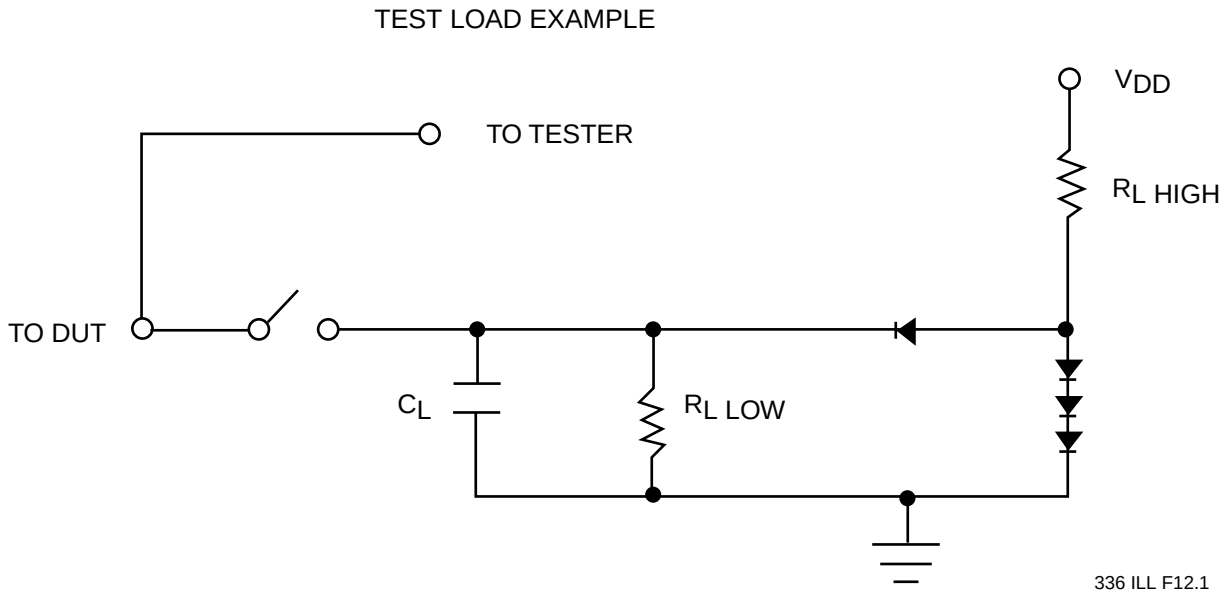


FIGURE 13: A TEST LOAD EXAMPLE

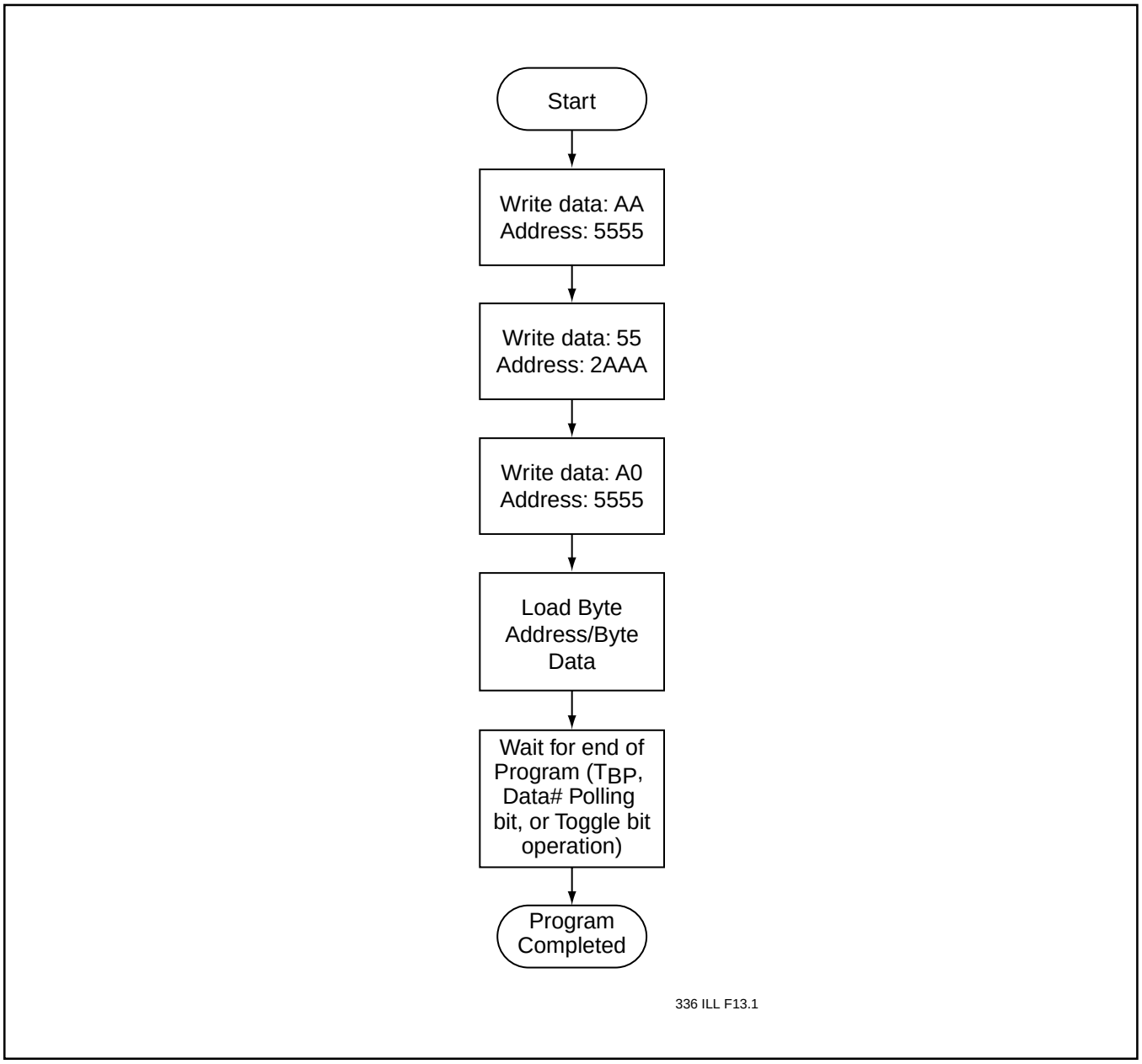


FIGURE 14: BYTE PROGRAM ALGORITHM

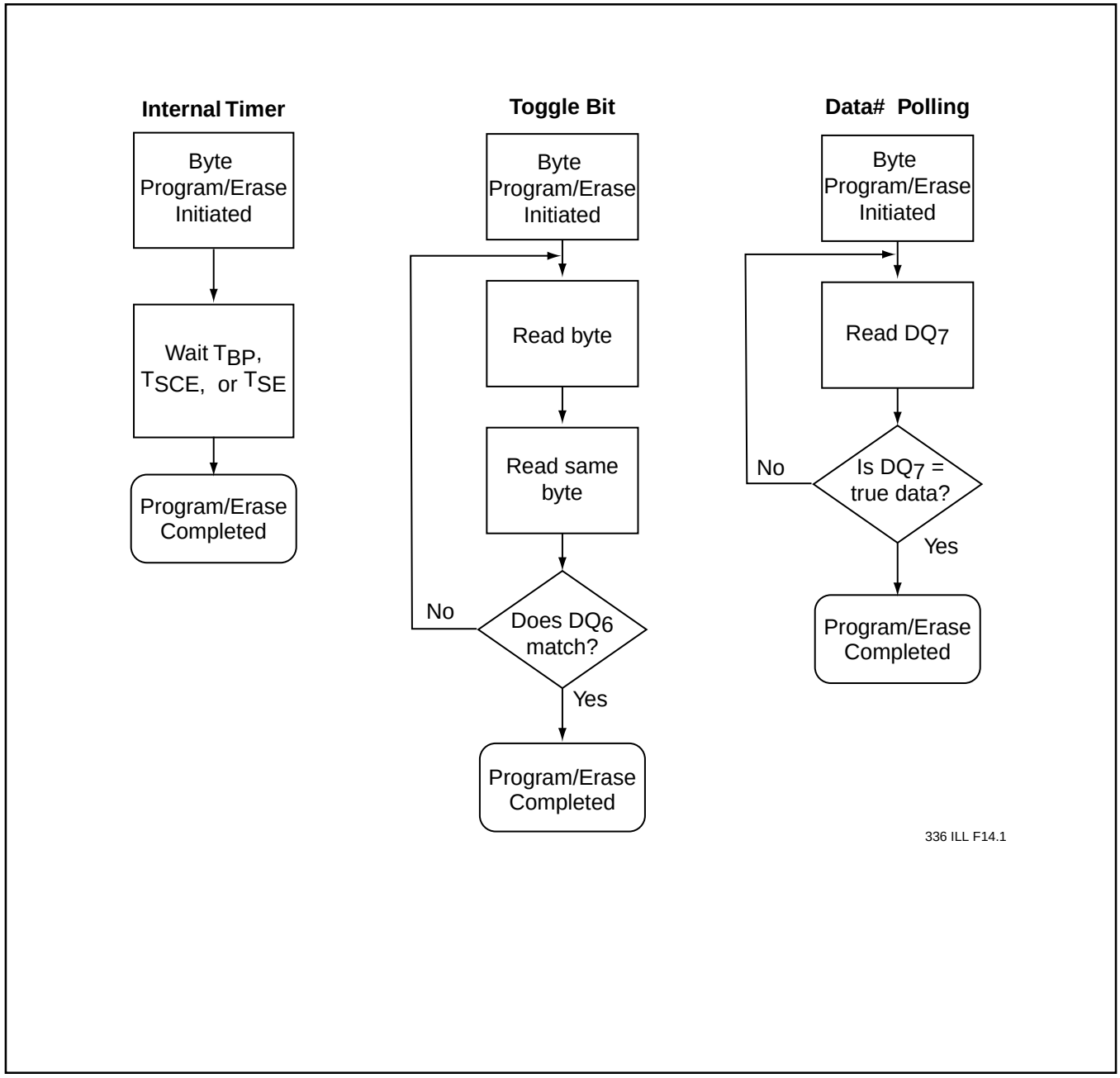


FIGURE 15: WAIT OPTIONS

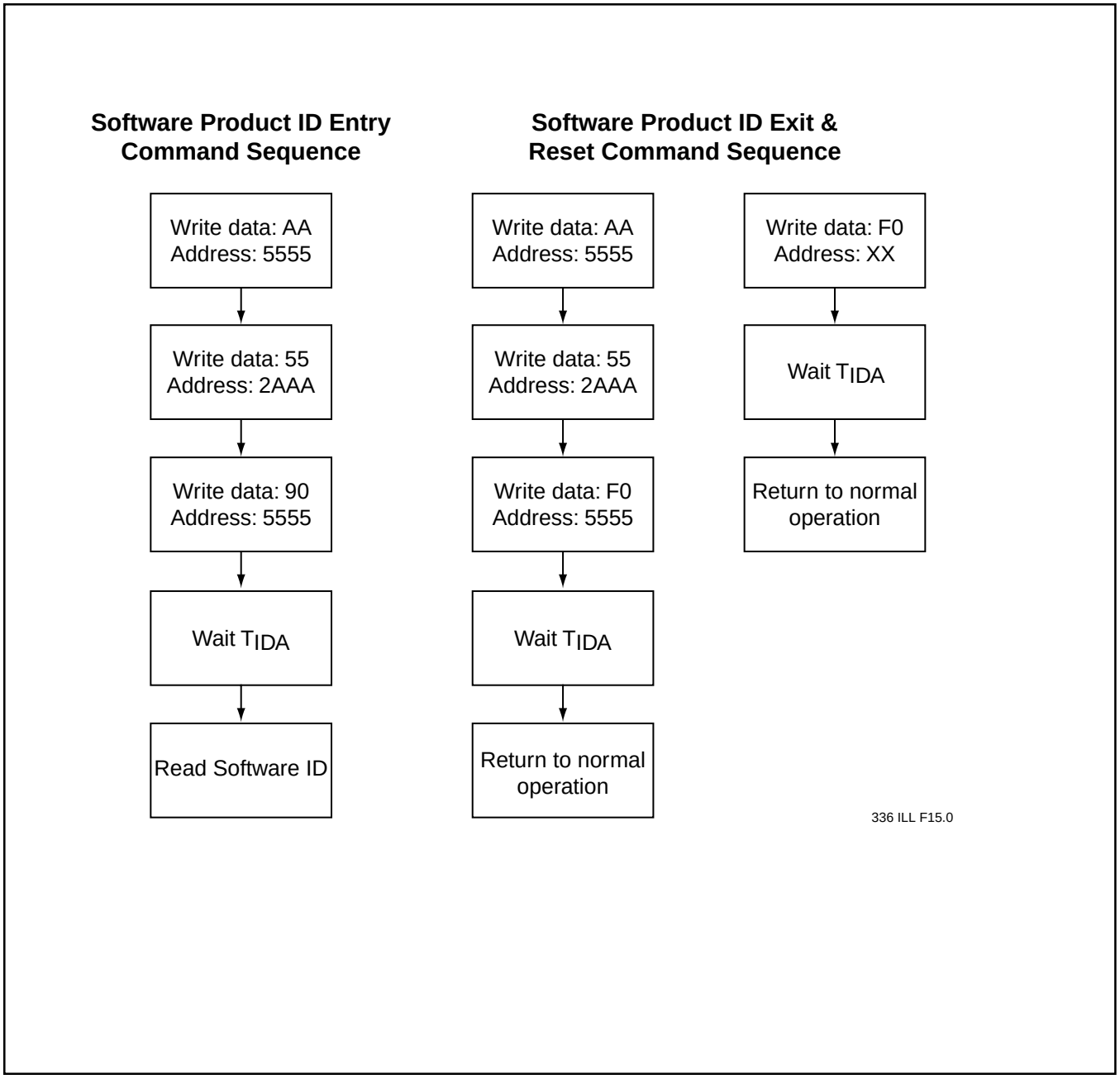


FIGURE 16: SOFTWARE PRODUCT COMMAND FLOWCHARTS

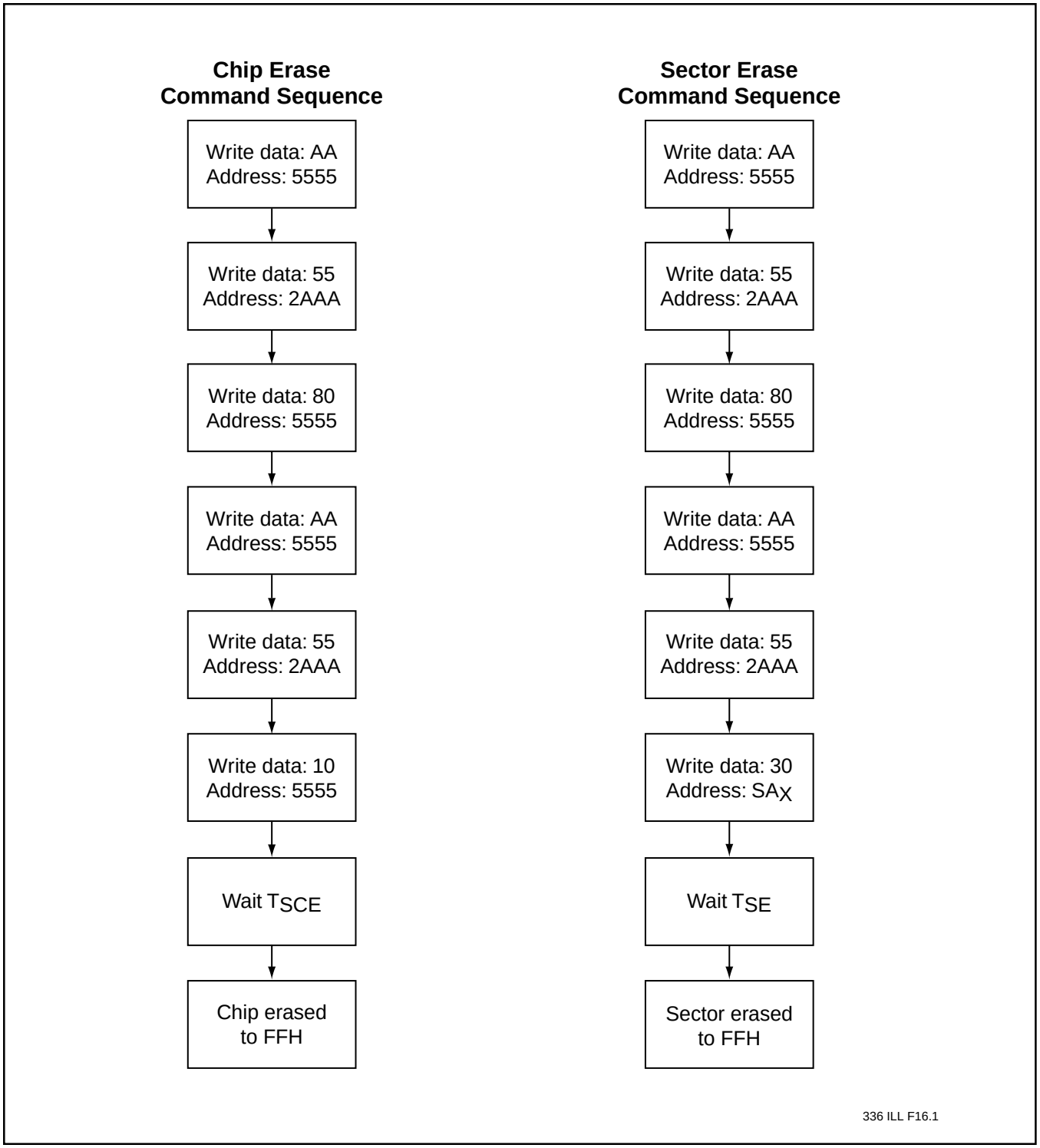
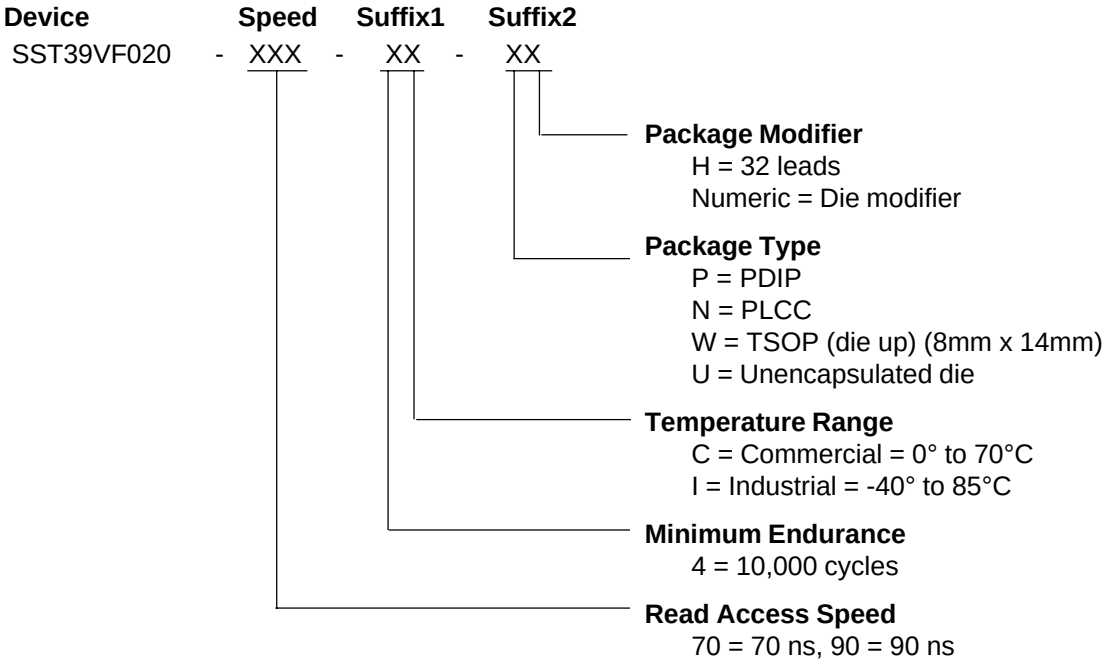


FIGURE 17: ERASE COMMAND SEQUENCE

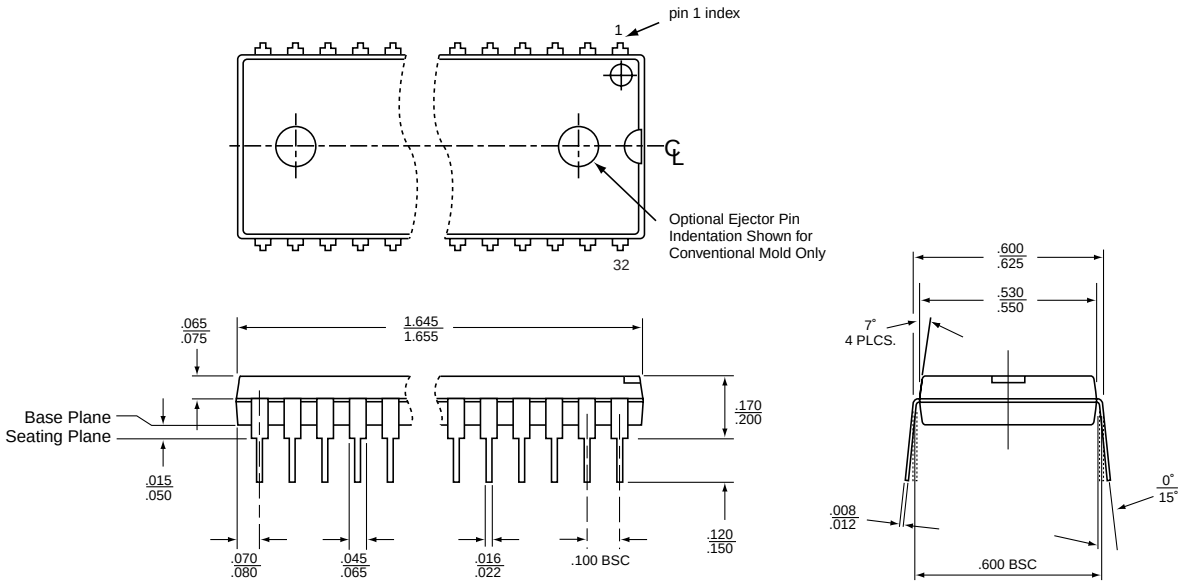


SST39VF020 Valid combinations

SST39VF020-70-4C-WH	SST39VF020-70-4C-NH	SST39VF020-70-4C-PH
SST39VF020-90-4C-WH	SST39VF020-90-4C-NH	SST39VF020-90-4C-PH
SST39VF020-90-4C-U1		
SST39VF020-70-4I-WH	SST39VF020-70-4I-NH	
SST39VF020-90-4I-WH	SST39VF020-90-4I-NH	

Example : Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

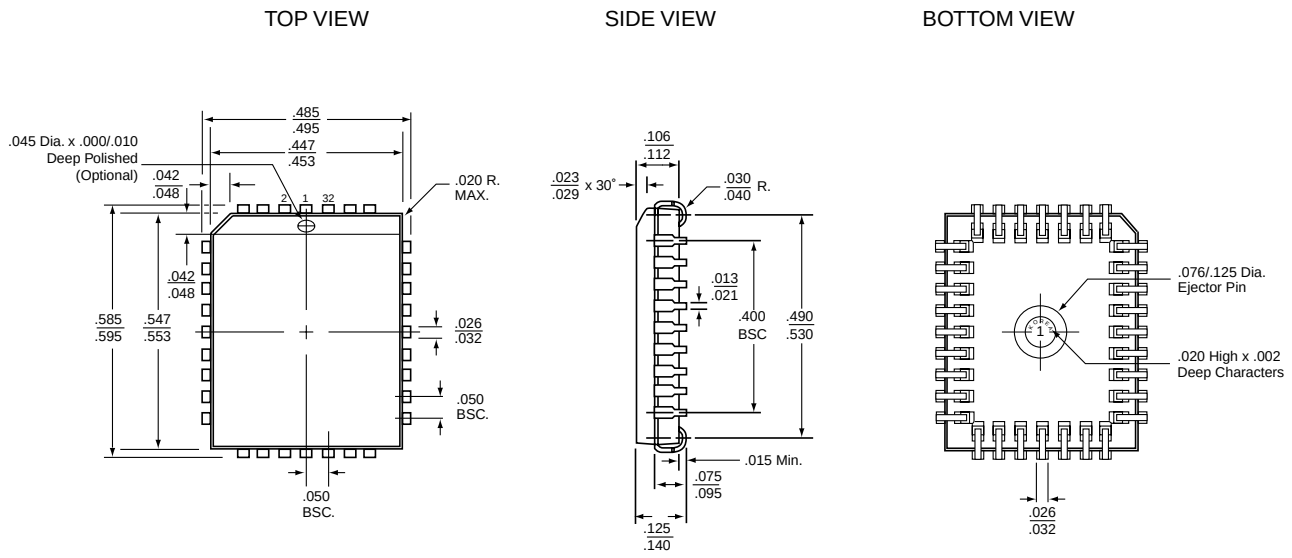
PACKAGING DIAGRAMS



Note: 1. Complies with JEDEC publication 95 MO-015 AP dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in inches (min/max).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .010 inches.

32.pdipPH-ILL.0

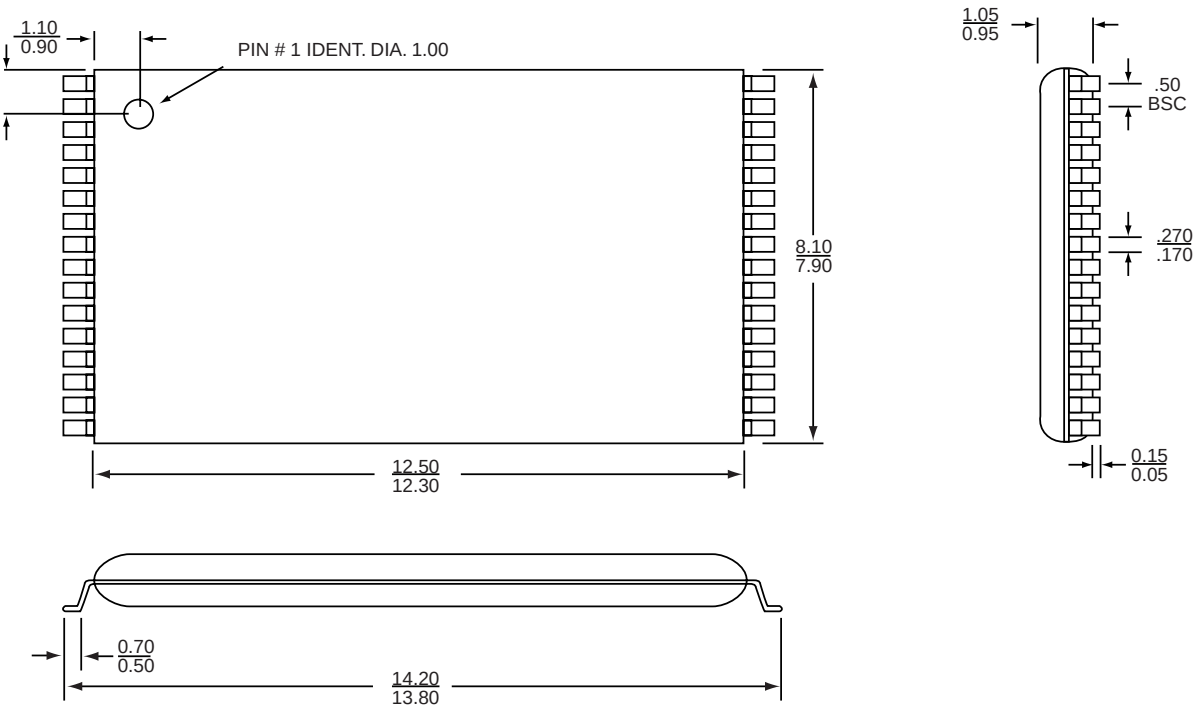
32-LEAD PLASTIC DUAL-IN-LINE PACKAGE (PDIP)
SST PACKAGE CODE: PH



Note: 1. Complies with JEDEC publication 95 MS-016 AE dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in inches (min/max).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .008 inches.

32.PLCC.NH-ILL.0

32-LEAD PLASTIC LEAD CHIP CARRIER (PLCC)
SST PACKAGE CODE: NH



Note: 1. Complies with JEDEC publication 95 MO-142 BA dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in metric (min/max).
3. Coplanarity: 0.1 (±.05) mm.

32.TSOP-WH-ILL.0

32-LEAD THIN SMALL OUTLINE PACKAGE (TSOP)
SST PACKAGE CODE: WH

(Waslin Group . since 1992)
Website: http://www.waslin.cn, http://www.metatech.com.tw

HongKong
Tel: 852-24212379 Fax: 852-24212479
Address: Unit 3503, Metroplaza Tower II, 223 Hing Fong Rd., Kwai Fong, Hong Kong.
Email: service@meta.com.hk

Beijing
Tel: 86-10-68582188 Fax: 86-10-68583188
Address: Rm. 210, China Hall of Science & Technology, No. 3 FuXing Road, Beijing, China 100038

Shanghai
Tel: 86-21-64857530 Fax:86-21-64852237
Address: No. 507, New Cao He Jing Tower, No. 509 Cao Bao Road, Shanghai, China 200233

Chengdu
Tel: 86-28-5577415 Fax:86-28-5577415
Address: Rm. 1405, 14/F Dong Fu Da Xia, Yu Lin Bei Jie, Chengdu, Sichuan, China 610041

Fuzhou
Tel: 86-591-3781033 Fax: 86-591-3781033
Address: Room 1512, Block 2, Xi Hong Xiao Qiu, Gu Lou Qiu, FuZhou, China

Shenzhen
Tel: 86-755-3219726 Fax: 86-755-3219736
Address: Room 1105, 11/F, Bei Fang Da Xia, Shen Nan Zhong Lu, Shenzhen, China.

Customer Service Center
Tel:86-756-8117078 Fax:86-756-8117078
Address: 20 Qiao Guang Rd., Kuns Bei , Zhuhai, China 519020

DATA SHEET

凌陽科技 SUNPLUS

SPCA717A

Digital Video Encoder for Video CD

Preliminary

NOV. 11, 2002

Version 0.1

Table of Contents

PAGE

DIGITAL VIDEO ENCODER FOR VIDEO CD

1.GENERAL DESCRIPTION

The SPCA717A is designed specifically for VideoCD, video games and other digital video systems, which require the conversion of digital YCrCb (MPEG) data to analog NTSC/PAL video. The device supports a glue-less interface to most popular MPEG decoders. The SPCA717A supports worldwide video standards, including NTSC (N America, Japan) PAL-B, D, G, H, I (Europe, Asia), PAL-M (Brazil), PAL-N (Uruguay, Paraguay), and PAL-Nc (Argentina). Furthermore, the SPCA717A operates with a single 2x clock and can be powered with a single 3.3V supply. The composite analog video signal is output simultaneously onto two outputs. Therefore, it allows one output to provide base-band composite video while the other drives a RF modulator. As a slave, the SPCA717A automatically detects the input data formats (PAL/NTSC, CCIR601) and switches internally to provide the proper format on the outputs. This feature, along with the on-board voltage reference and single clock interface, makes the SPCA717A extremely simple to use. In addition, use of 2x over-sampling on-chip simplifies external filter design resulting in reduced overall system cost.

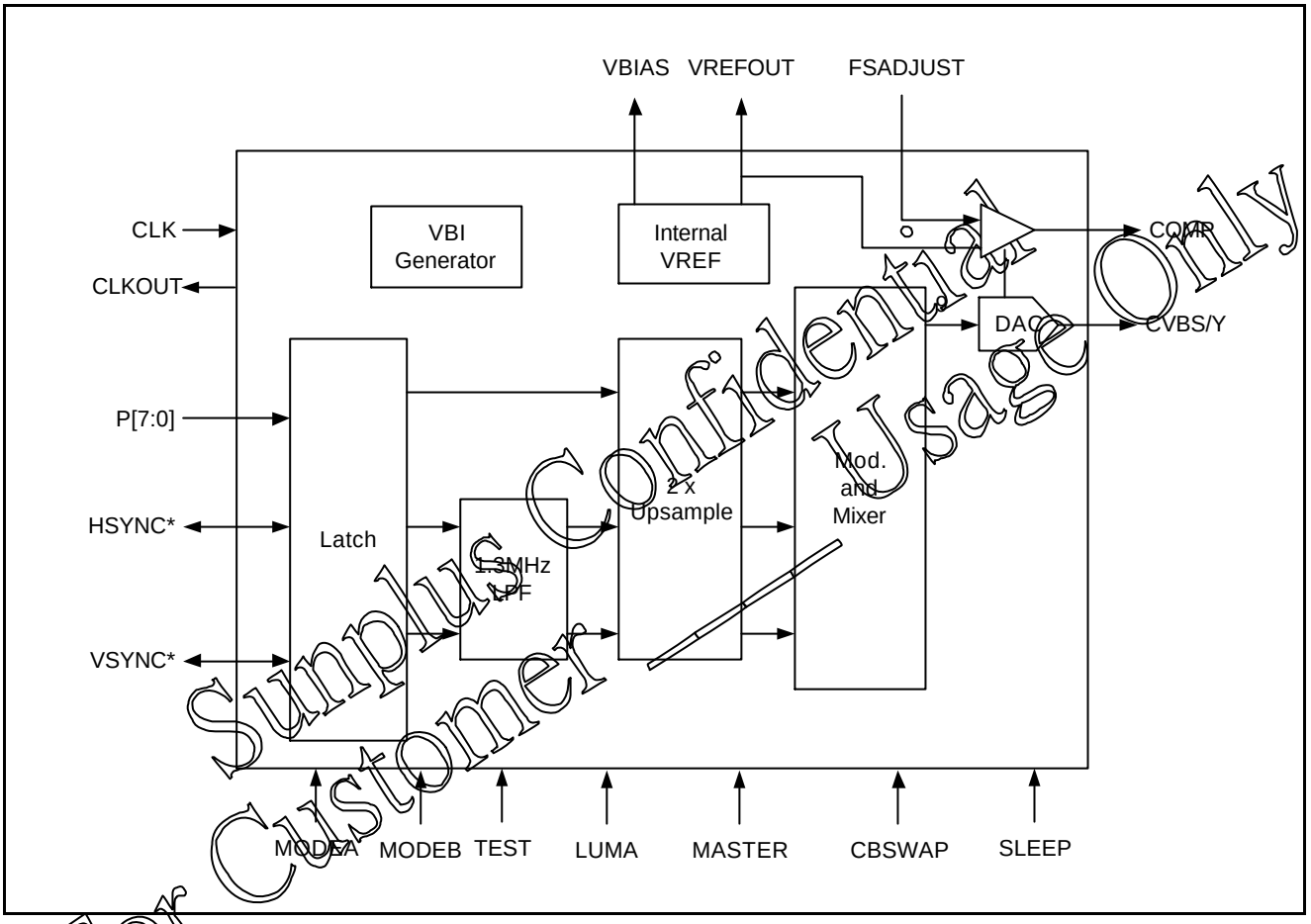
2.FEATURES

- 8-bit 4:2:2 YCrCb inputs for glue-less interface to MPEG decoders
- NTSC/PAL/PAL-M/PAL-Nc composite video outputs
- 3.3 V supply voltage
- ITU-R BT601/656 operation
- 2x over-sampling simplifies external filtering
- One 9-bit DAC
- Master or slave video timing
- Interlaced or non-interlaced operation
- Automatic mode detection/switching in slave mode
- 27MHz crystal oscillator input
- Power-down mode of chip
- On-board voltage reference
- 32-pin LQFP package

3.APPLICATIONS

- VideoCD
- Karaoke/video games
- Digital Video Disk (DVD)
- Digital VCR
- Digital set top box

4.BLOCK DIAGRAM

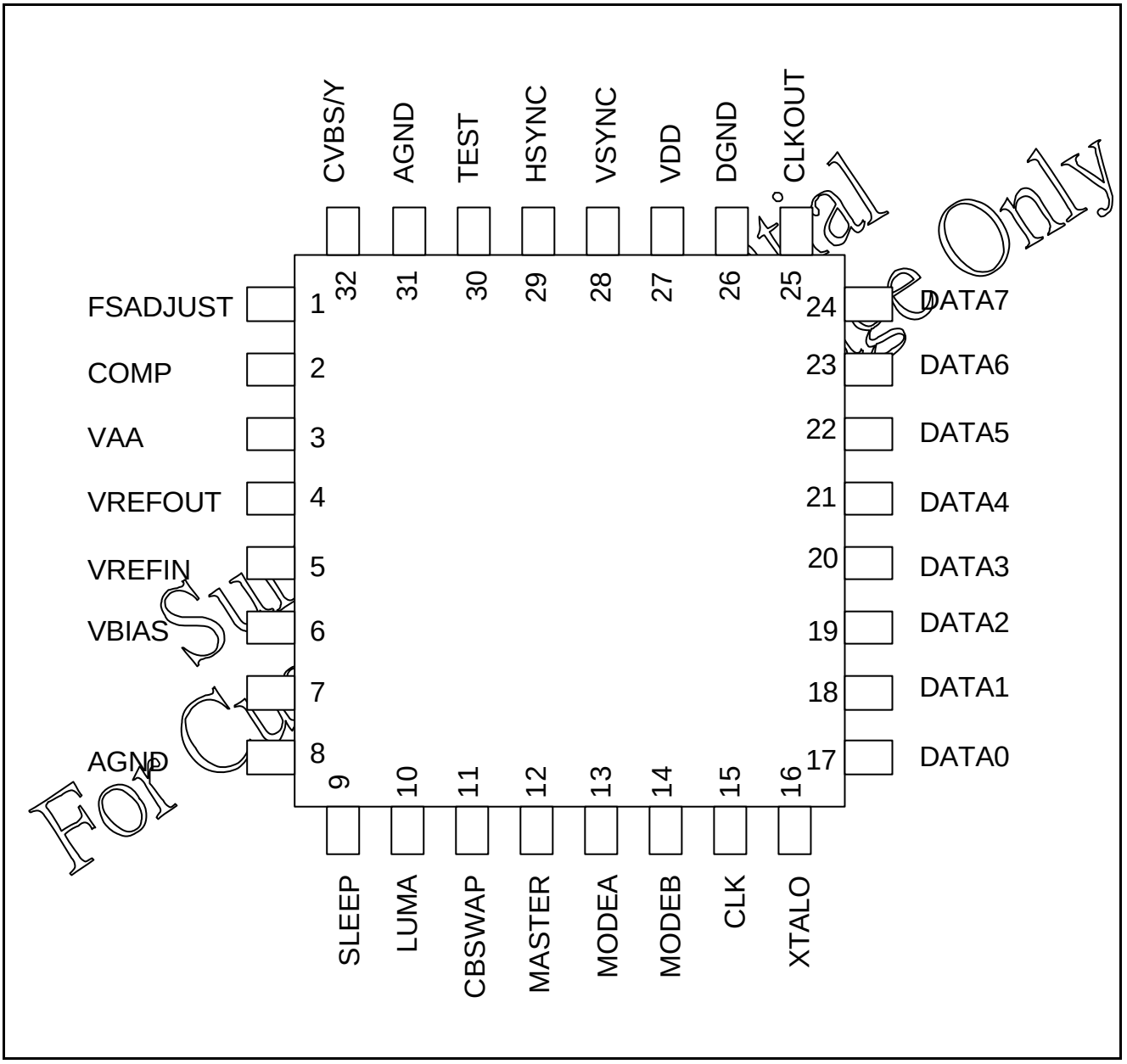


5.SIGNAL DESCRIPTIONS

5.1. PIN Description

Mnemonic	PIN No.	Type	Description
DATA[7:0]	17 - 24	I	YCrCb pixel inputs. They are latched on the rising edge of CLK. YCrCb input data conform to CCIR 601.
CLKOUT	25	O	Pixel clock output
VSYNC	28	I/O	Vertical sync input/output. VSYNC is latched/output following the rising edge of CLK.
HSYNC	29	I/O	Horizontal sync input/output. HSYNC is latched/output following the rising edge of CLK.
MASTER	12	I	Master/slave mode selection. A logical high for master mode operation. A logical 0 for slave mode operation
CBSWAP	11	I	Cr and Cb pixel sequence configuration pin. A logic high swaps the Cr and Cb sequence.
LUMA	10	I	Luma output selection pin. A logic high selects Y output. A logic low selects composite video output.
SLEEP	9	I	Power save mode. A logic high on this pin puts the chip into power-down mode. This pin is equal to reset pin. An external logic high pulse should input to the pin when power on.
MODEA	13	I	Mode configuration pin.
MODEB	14	I	Mode configuration pin.
CLK	15	I	27MHz crystal oscillator input. A crystal with 27MHz clock frequency can be connected between this pin and XTALO.
XTALO	16	O	Crystal oscillator output.
TEST	30	I	Test pin. These pins must be connected to DGND.
VREFIN	5	I	Voltage reference input. An external voltage reference must supply typical 1.235V to this pin. A 0.1μF ceramic capacitor must be used to de-couple this input to GND. The decoupling capacitor must be as closed as possible to minimize the length of the load. This pin may be connected directly to VREFOUT.
VREFOUT	4	O	Voltage reference output. It generates typical 1.2V voltage reference and may be used to drive VREFIN pin directly.
FSADJ	1	-	Full-Scale adjust control pin. The Full-Scale current of D/A converters can be adjusted by connecting a resistor (RSET) between this pin and ground.
COMP	2	-	Compensation pin. A 0.1μF ceramic capacitor must be used to bypass this pin to VAA. The lead length must be kept as short as possible to avoid noise.
VBIAS	6	-	DAC bias voltage. Potential normally 0.7V less than COMP.
VDD	27	-	Digital power pin
DGND	26	-	Digital ground pin
CVBSY	32	O	Composite/Luminance output. This is a high-impedance current source output. The output format can be selected by the PAL pin. The CVBSY can drive a 37.5Ω load.
NO	7		-
VAA	3	-	Analog power pin
AGND	31,8	-	Analog ground pin

5.2. PIN Map



6.FUNCTIONAL DESCRIPTIONS

6.1. Mode Selection

Master mode is selected when MASTER = 1; slave mode is selected when MASTER = 0. Two pins, MODEA, MODEB, drive three different configuration registers. The most common operating modes can be selected with these pins while in master mode. In slave mode, the common operating modes are automatically determined from the timing of the incoming HSYNC* and VSYNC* signals.

Note:
The term "common operating mode" refers to North American NTSC and Western European PAL **Table 1** illustrates the multi-functionality of the mode pins during master and slave mode. To access the more exotic video formats, slave mode is preferred since the necessary registers are always accessible. If master mode is needed, the less common modes can still be programmed by first registering the modes as a slave, and then switching to a master. During power-up, the MODEA and MODEB pins configure the master registers, i.e., EFIELD, PAL625, are written. Also, during power-up, the slave registers are reset to zero, i.e., YCSWAP.

Table 1. Mode Selection

PIN Description		
The MASTER pin	**MODEA**	**MODEB**
0	YCSWAP	PALSA
1	EFIELD	PAL625

Table 2. Configuration Register Settings

Mode Register Name	Set to 0	Set to 1	Comments
EFIELD	The VSYNC pin will output normal vertical synchronization signal.	The VSYNC pin will output field signal. Low at VSYNC pin for even field, high for odd field	This is only used at master mode.
PAL625	525-line operation will be select	The 625-line operation will be select	This is only used at master mode
YCSWAP	Do not swap Y and Cr/Cb	Swap Y and Cr/Cb sequence	-
PALSA	When PAL625 register is set to high, PAL-BDGHI mode is selected. When PAL625 register is set to low, NTSC mode is selected.	When PAL625 register is set to high, PAL-Nc mode is selected. When PAL625 register is set to low, PAL-M mode is selected.	-

6.2. Clock Timing

A clock signal with a frequency twice the luminance sampling rate must be present at the CLK pin. All setup and hold timing specifications are measured with respect to the rising edge of this signal.

6.3. Pixel Input Timing

6.3.1. Pixel sequence

Multiplexed Y, Cb, and Cr data is input through the DATA[7:0] inputs. By default, the input sequence for active video pixels must be Cb0, Y0, Cr0, Y1, Cb2, Y2, Cr2, Y3, etc., in accordance with CCIR-656. This pattern begins during the first CLK period after the falling edge of HSYNC* (regardless of the setting of SLAVE/MASTER mode). The order of Cb and Cr can be reversed by setting the CBSWAP pin. **Figure 1** illustrates the timing. If the pixel stream input to the SPCA717A is off by one CLK period, the SPCA717A can lock to the pixel stream by setting the YCSWAP register. This would solve the problem of having the Y and Cr/Cb pixels swapped.

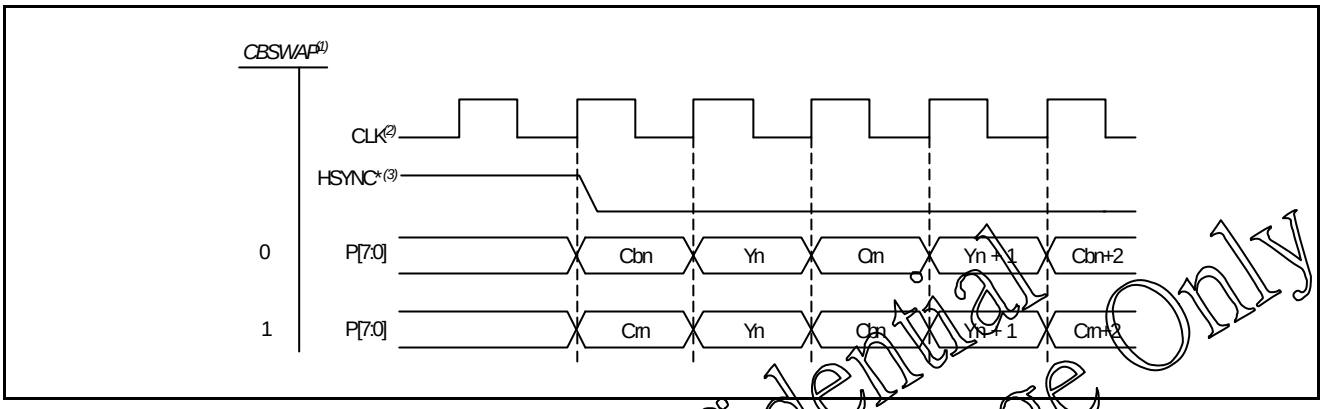


Figure 1. Pix Sequence

Note1: CBSWAP is pin 11.

Note2: Pixel transitions must occur observing setup and hold timing about the rising edge of CLK.

Note3: Pixel sequence will beging with Cbn at 4 x m clock periods following the falling edge of HSYNC*, when m is an integer.

6.4. Video Timing

The width of the analog horizontal sync pulses and the start and end of color burst is automatically calculated and inserted for each mode according to CCIR-624-4. Color burst is disabled on appropriate scan lines. Serration and equalization pulses are generated on appropriate scan lines. In addition, rise and fall times of sync, and the burst envelope are internally controlled. Video timing figures follow the next in this section.

6.4.1. Sync and burst timing

Table 3 lists the resolutions and clock rates for the various modes of operation.

Table 4 lists the horizontal counter values for the end of horizontal sync, start of color burst, end of color burst, front porch, back porch and the first active pixel for the various modes of operation. The front porch is the interval before the next expected falling HSYNC* when outputs are automatically blanked. The horizontal sync width is measured between the 50% points of the falling and rising edges of horizontal sync. The start of color burst is measured between the 50% point of the falling edge of horizontal sync and the first 50% point of the color burst amplitude (nominally +20 IRE for NTSC and 150 mV for PAL-B, D, G, H, I, Nc above the blanking level). The end of color burst is measured between the 50% point of the falling edge of horizontal sync and the last 50% point of the color burst envelope (nominally +20 IRE for NTSC and 150 mV for PAL-B, D, G, H, I, Nc above the blanking level).

Table 3. Field Resolutions and Clock Rates for Various Modes of Operation

Operating Mode	Active pixels	Total Pixels	CLK Frequency (MHz)
NTSC/PAL-M CCIR601	720 x 240	858 x 262	27
PAL-B,D,G,H,I, Nc	720 x 288	864 x 313	27

Table 4. Horizontal Counter Values for Various Video Timings

Operation Mode	Front porch (a)	Horizontal Sync Width (b)	Start of Burst (c)	Duration of Burst (d)	Back porch (e)
NTSC CCIR601	20	63	72	34	127
PAL-B CCIR601	20	63	76	30	142

Note: The unit is the number of luminance pixel.

6.4.2. Master mode

Horizontal sync (HSYNC*) and vertical sync (VSYNC*) are generated from internal timing and optional software bits. HSYNC*, and VSYNC* are output following the rising edge of CLK. The horizontal counter is incremented on every other rising edge of CLK. After reaching the appropriate value (determined by the mode of operation), it is reset to one, indicating the start of a new line. The vertical counter is incremented at the start of each new line. After reaching the appropriate value, determined by the mode of operation, it is reset to one, indicating the start of a new field. VSYNC* is asserted for 3 or 2.5 scan lines for 262/525 line and 312/625 line, respectively.

6.4.3. Slave mode

Horizontal sync (HSYNC*) and vertical sync (VSYNC*) are inputs that are registered on the rising edge of CLOCK. The horizontal counter is incremented on the rising edge of CLOCK. Two clock cycles after falling edge of HSYNC*, the counter is reset to one, indicating the start of a new line. The vertical counter is incremented on the falling edge of HSYNC*. A falling edge of VSYNC* resets it to one, indicating the start of a new field. A falling edge of VSYNC* occurring within ±1/4 of a scan line from the falling edge of HSYNC* cycle time (line time) indicates the beginning of Field 1. A falling edge of VSYNC* occurring within ±1/4 scan line from the mid-point of the line indicates the beginning of Field 2.

The operating mode (NTSC/PAL) can be programmed with the MODEA and MODEB bits when the SETMODE (MASTER pin) bit is set high. Alternatively, when SETMODE is low, the mode is automatically detected in slave mode. For example, 525-line operation is assumed, 625-line operation is detected by the number of HSYNC* edges between VSYNC* edges. The frequency of operation (CCIR 601) for both PAL and NTSC is detected by counting the number of clocks per line. The pixel rate is assumed to be 13.5 MHz, ±1 count which is detected in between two successive falling edges of HSYNC*.

6.4.4. Burst blanking

For NTSC, color burst information is automatically disabled on scan lines 1-9 and 264-272, inclusive. (SMPTE line numbering convention.) For PAL-B, D, G, H, I , Nc color burst information is automatically disabled on scan lines 1-6, 310-318, and 623-625, inclusive, for fields 1, 2, 5, and 6. During fields 3, 4, 7, and 8, color burst information is disabled on scan lines 1-5, 311-319, and 622-625, inclusive.

6.5. Vertical Blanking Intervals

For NTSC, scan lines 1-9 and 263-272, inclusive, are always blanked. There is no setup on scan lines 10-21 and 273-284 inclusive. All displayed lines in the vertical blanking interval (10-21 and 273-284 for interlaced NTSC; 7-13 and 320-335 for interlaced PAL-B, D, G, H, I) are forced to blank. For PAL-B, D, G, H, I, scan lines 1-6, 311-318, and 624-625, inclusive, during fields 1, 2, 5, and 6, are always blanked. During fields 3, 4, 7, and 8, scan lines 1-5, 311-319, and 624-625, inclusive, are always blanked.

6.6. Digital Processing

Once the input data is converted into internal YUV format, the UV components are low-pass filtered with a filter. The Y and filtered UV components are up-sampled to CLK frequency by a digital filter.

6.7. Subcarrier Generation

To maintain a synchronous sub-carrier relative to HSYNC*, the sub-carrier phase is reset every frame for NTSC and every 8 fields for PAL. The SCA phase is non-zero and depends upon the clock frequency and the video format.

For a perfect clock input, The burst frequency is 4.43361875 MHz for PAL-B, D, G, H, I, 3.57561149MHz for PAL-M, 3.58205625MHz for PAL-Nc (Argentina), 3.579545 MHz for NTSC interlaced.

6.8. Power-Down Mode

In power-down mode (SLEEP pin set to 1), the internal clock is stopped and also an internal reset is forced and the DACs are powered down. When returned low, the device starts from a reset state (horizontal and vertical counters = 0, which is the start of VSYNC in Field 1).

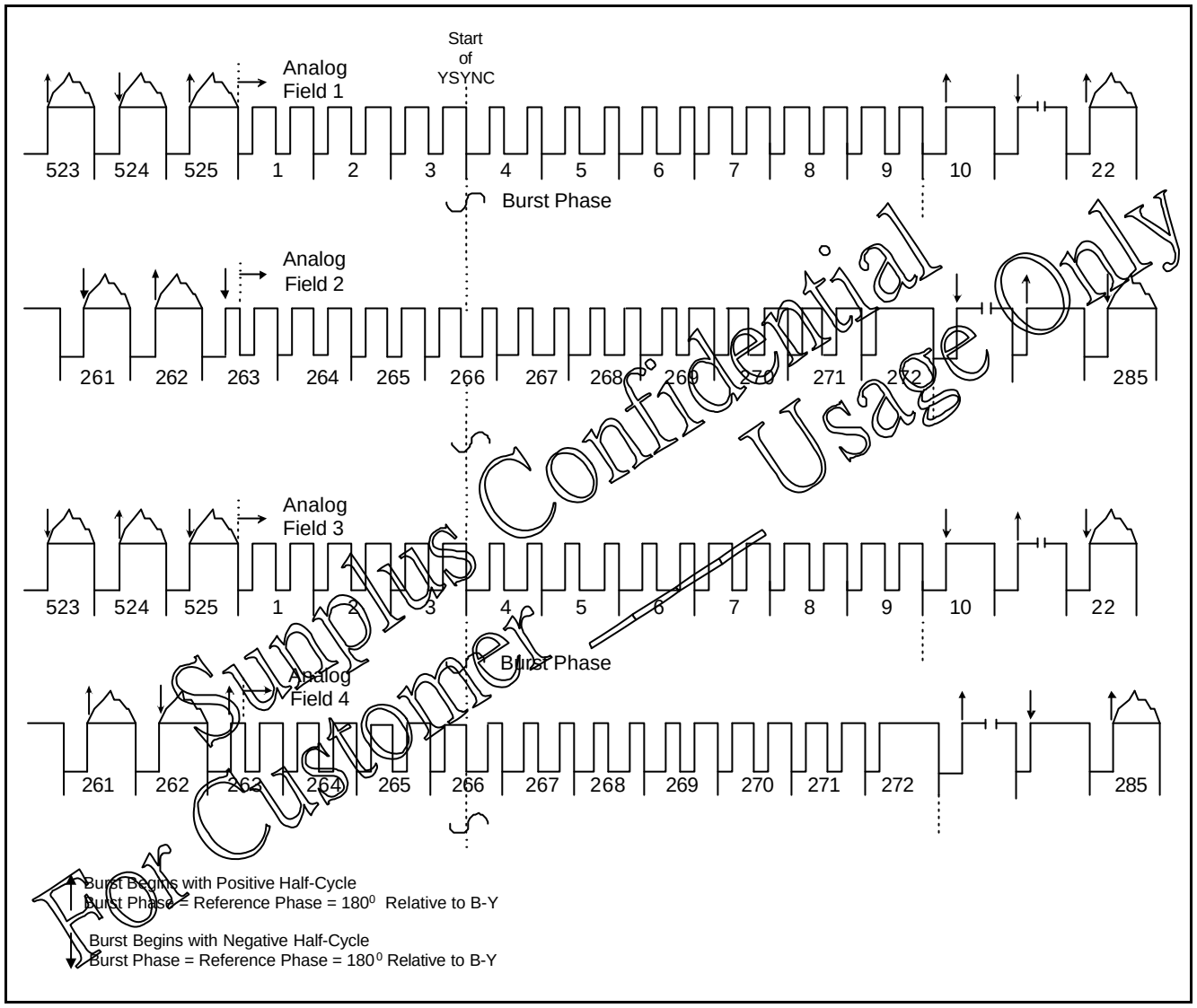


Figure 2. Interlaced 525-Line (NTSC) Video Timing

Note: SMPTE line numbering convention rather than CCIR-624 is used.

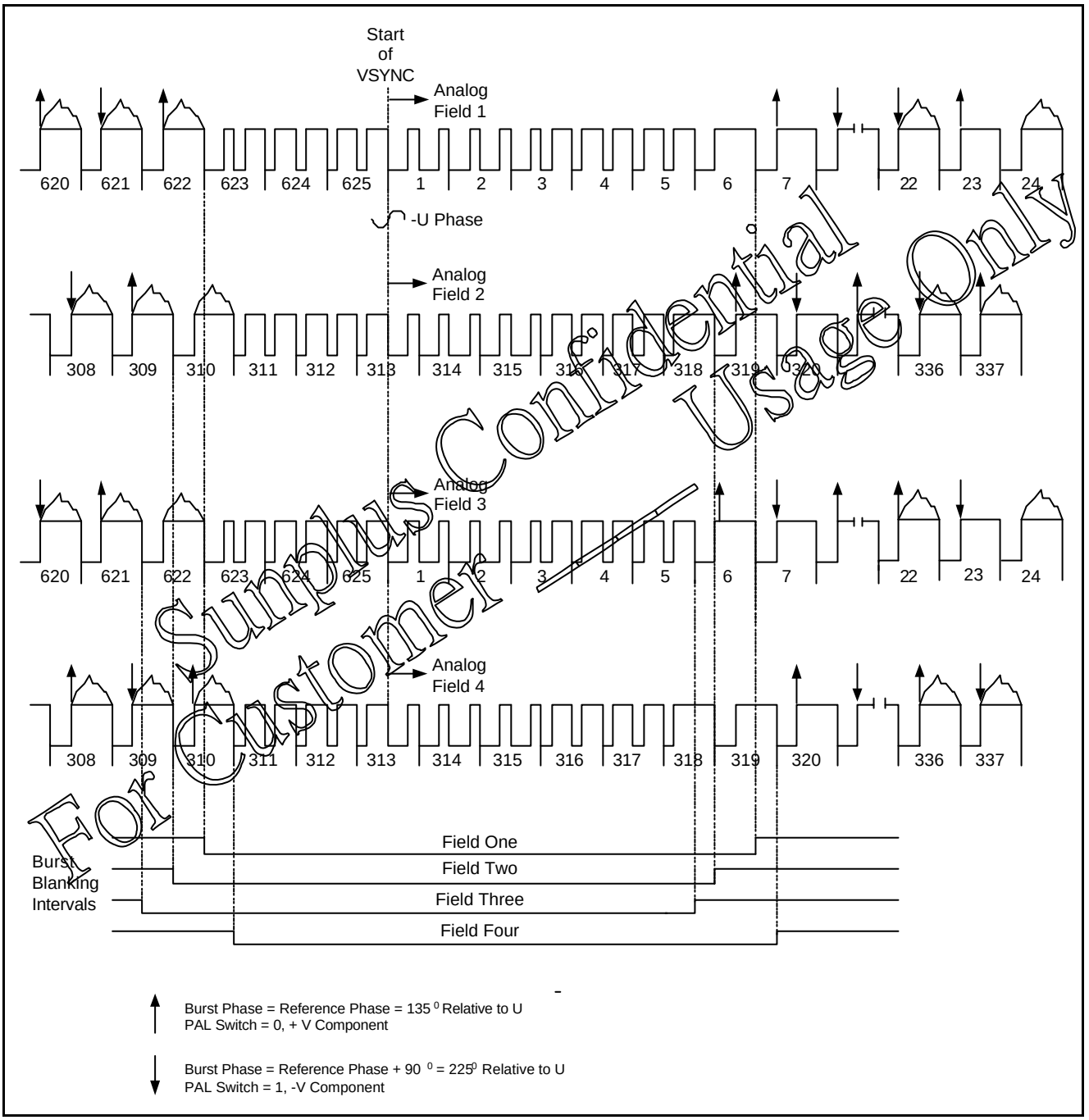


Figure 3a. Interlaced 625-Line (PAL) Video Timing

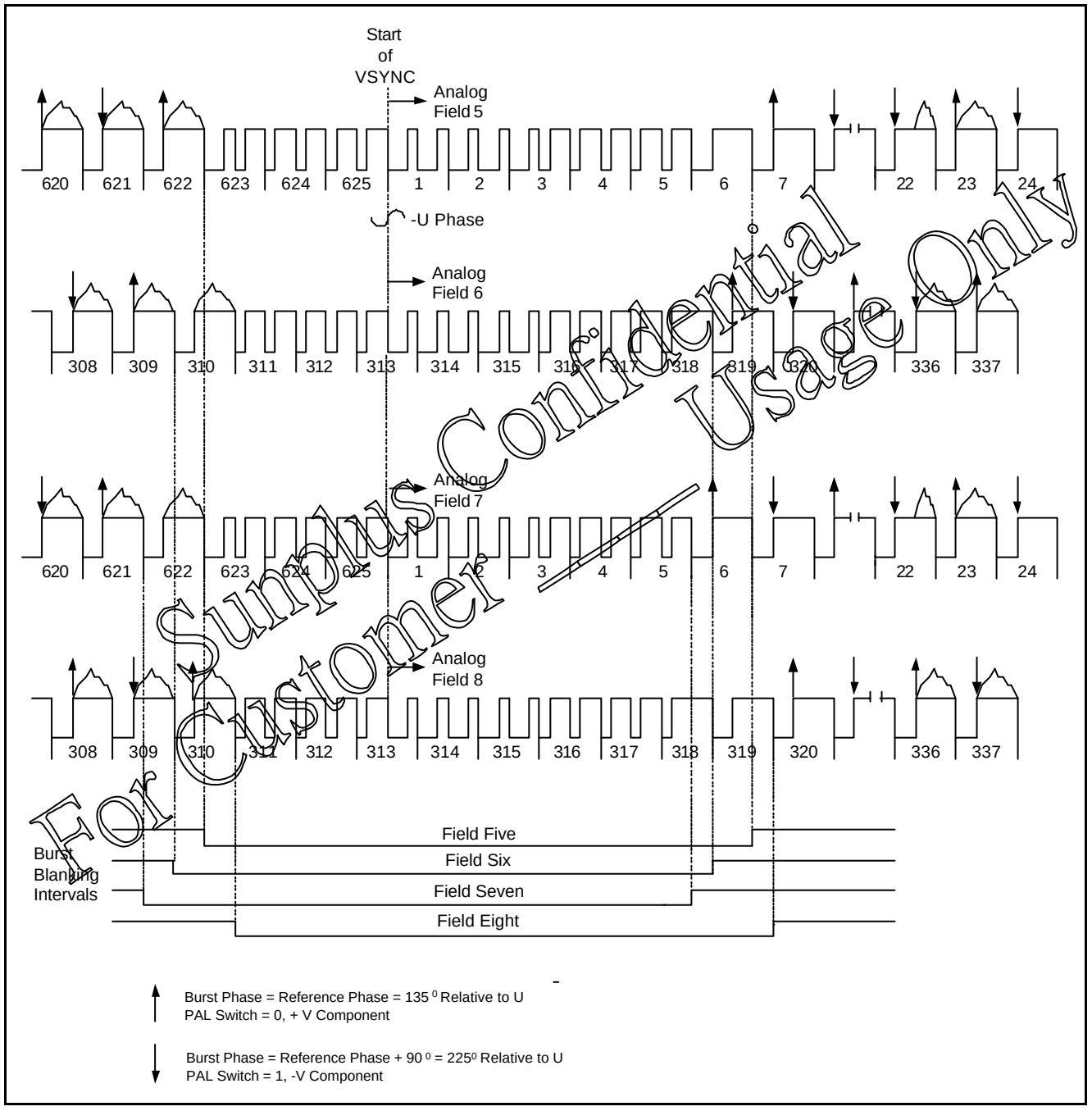


Figure 3b. Interlaced 625-Line (PA L) Video Timing

6.9. Pixel Input Ranges And Colorspace Conversion

6.10. YC inputs (4:2:2 YCRCB)

Y has a nominal range of 16-235; Cb and Cr have a nominal range of 16-240, with 128 equal to zero. Y values of 0-15 and 236-255 are interpreted as 16 and 235. CrCb values of 1-15 and 241-254, are interpreted as 16 and 240.

6.11. DAC coding

White is represented by a 9-bit DAC code of 400. For PAL-B, D, G, H, I, Nc the standard blanking level is represented by a DAC code of 126. For NTSC, the standard blanking level is represented by a DAC code of 120.

6.12. Outputs

All digital-to-analog converters are designed to drive standard video levels into an equivalent 37.5 Ω load. Either tone composite video outputs or Y outputs are available (selectable by the LUMA pin). If the SLEEP pin is high, the DAC are essentially turned off and only the leakage current is present.

6.12.1. Composite and luminance (CVBS/Y) analog output

When LUMA is a logical zero, digital composite video information drives the 9-bit D/A converter that generates the CVBS output. When LUMA is a logical one, digital luminance information drives the DAC that generates the analog Y video output.

7.ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Rating

Parameter	Symbol	Min.	Tpy.	Max.	Unit
Power Supply (Measured to ground)	VAA	-	-	4.5	V
Ambient Operating temperature	TA	-40	-	+125	°C
Voltage on Any Signal Pin	-	GND-0.5	-	VAA+0.5	V
Storage Temperature	TS	-65	-	+150	°C
Junction Temperature	TJ	-	-	+150	°C

Note: This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any pin that exceeds the power supply voltage by more than +0.5V can cause destructive latchup.

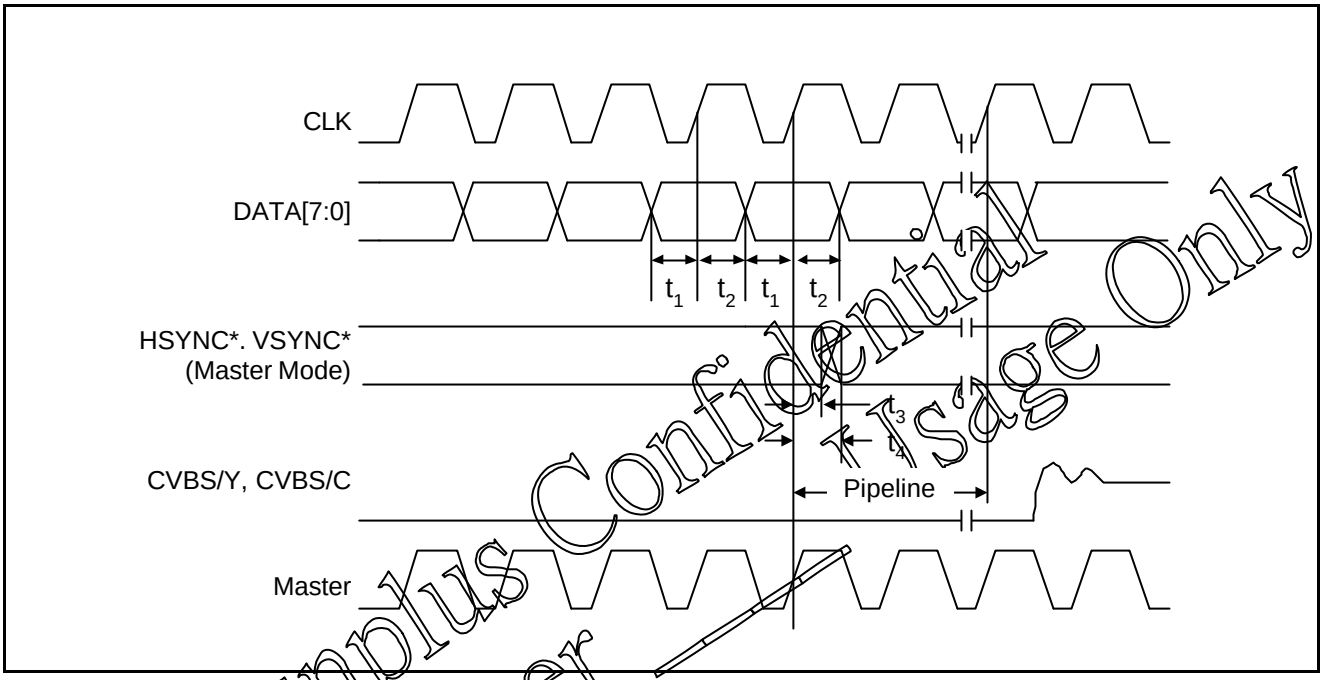
7.2. Recommended Operation Conditions

Parameter	Symbol	Min.	Tpy.	Max.	Unit
Power Supply	V_{AA}	3	3.3	3.6	V
Ambient Operating temperature	TA	0	-	+70	°C
DAC Output Load	RL	-	37.5	-	Ω
External Voltage Reference	VREFIN	-	1.27	-	V

7.3. DC Characteristics

Characteristics	Symbol	Limit			Unit
		Min.	Tpy.	Max.	
Analog Power Operating Voltage	V_{AA}	3.0	3.3	3.6	V
Digital Power Operating Voltage	VDD	3.0	3.3	3.6	V
Operating Current	I_{OP}	-	90	300	mA
Power Down Mode Current	-	-	20	-	mA
Input High Voltage (Digital Input)	V_{IH}	2.0	-	V_{AA}+0.5	V
Input Low Voltage (Digital Input)	V_{IL}	GND-0.5	-	0.8	V
Output High I (V_{OH}=2.4V) (Digital Output)	I_{OH}	-	-8	-	mA
Output Sink I (V_{OL}=0.8V) (Digital Output)	I_{OL}	-	8	-	mA
VREFOUT Output Voltage	VREFOUT	-	1.27	-	V
VREFOUT Current	IREFOUT	-	10	-	uA

7.4. AC Characteristics



Description	Symbol	Min.	Typ.	Max.	Units
Pixel/Control Setup Time	t1	-	20	-	ns
Pixel/Control Hold Time	t2	-	15	-	ns
Control Output Hold Time	t3	-	7	-	ns
Control Output Delay Time	t4	-	10	-	ns
HSYNC* to Analog Output (Master Mode)	-	-	26	-	CLK Periods
CLK Frequency	-	24.54	27	29.5	MHZ
CLK Pulse Width Low Time	-	-	10	-	ns
CLK Pulse Width High Time	-	-	10	-	ns

8. APPLICATION CIRCUITS

8.1. PC Board Considerations

The layout should be optimized for lowest noise on the power and ground planes by providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing. A well-designed power distribution network is critical to eliminate digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of four layers is recommended, with layers 1 (top) and 4 (bottom) for signals and layers 2 and 3 for ground and power, respectively.

8.2. Component Placement

Components should be placed as close as possible to the associated pin. The optimum layout enables the SPCA717A to be located as close as possible to the power supply connector and the video output connector.

8.3. Power And Ground Planes

For optimum performance, a common digital and analog ground plane is recommended. Separate digital and analog power planes are recommended. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all SPCA717A power pins, VREF circuitry, and COMP decoupling. At least a 1/8-inch gap is required in between the digital power plane and the analog power plane. The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in **Figure 4, Table 6**. This bead should be located within 3 inches of the SPCA717A. The bead provides resistance to switching-currents, acting as a resistance at high frequencies. A low-resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2723021447, or TDK BF45-4001.

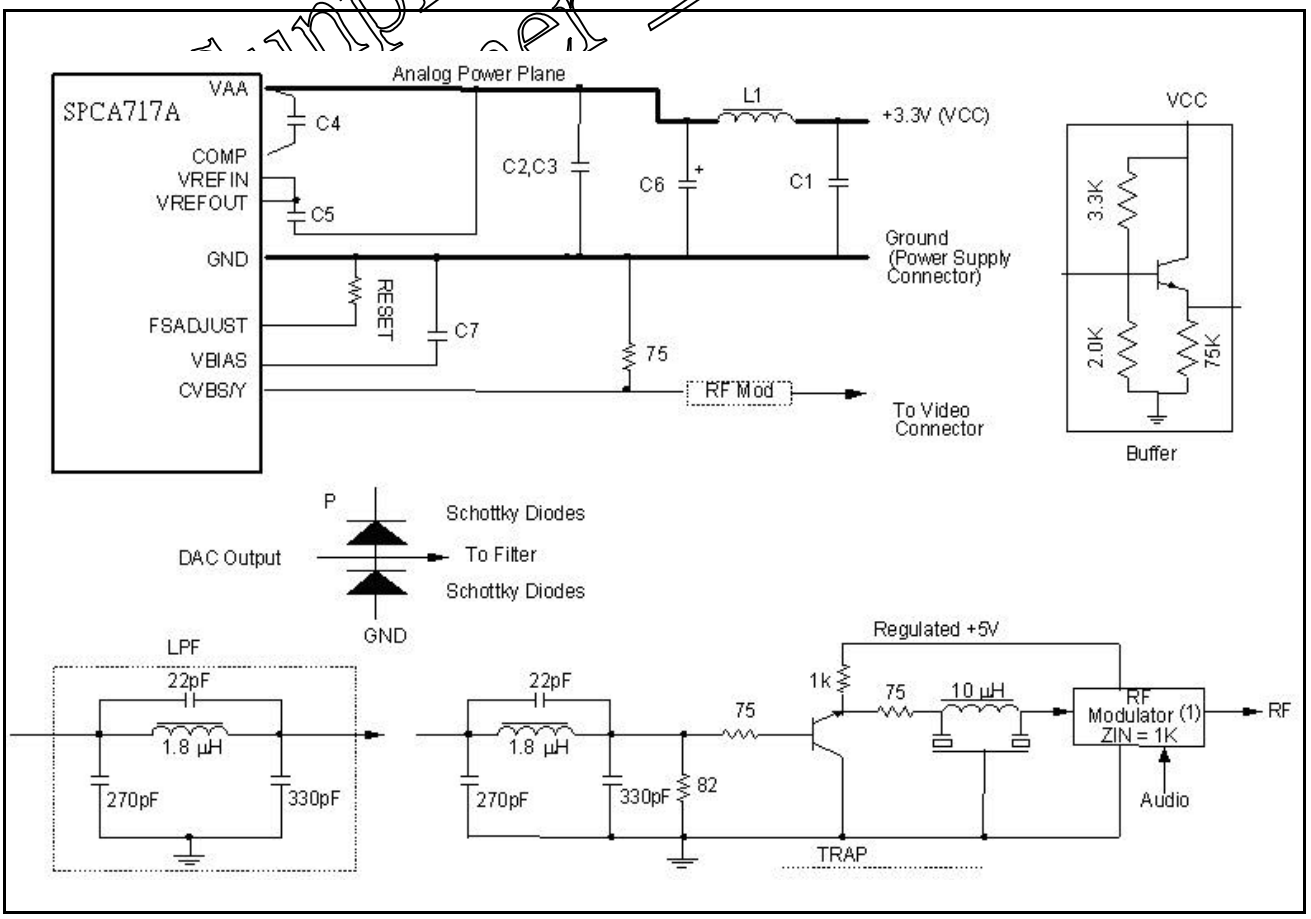


Figure 4. Typical Connection Diagram (Internal Voltage Reference)

Note1: Some modulators may require AC coupling capacitors (10µF).
Note2: Optional for chroma boost.
Note3: VREFIN must be connected to either VREFOUT or VBIAS.

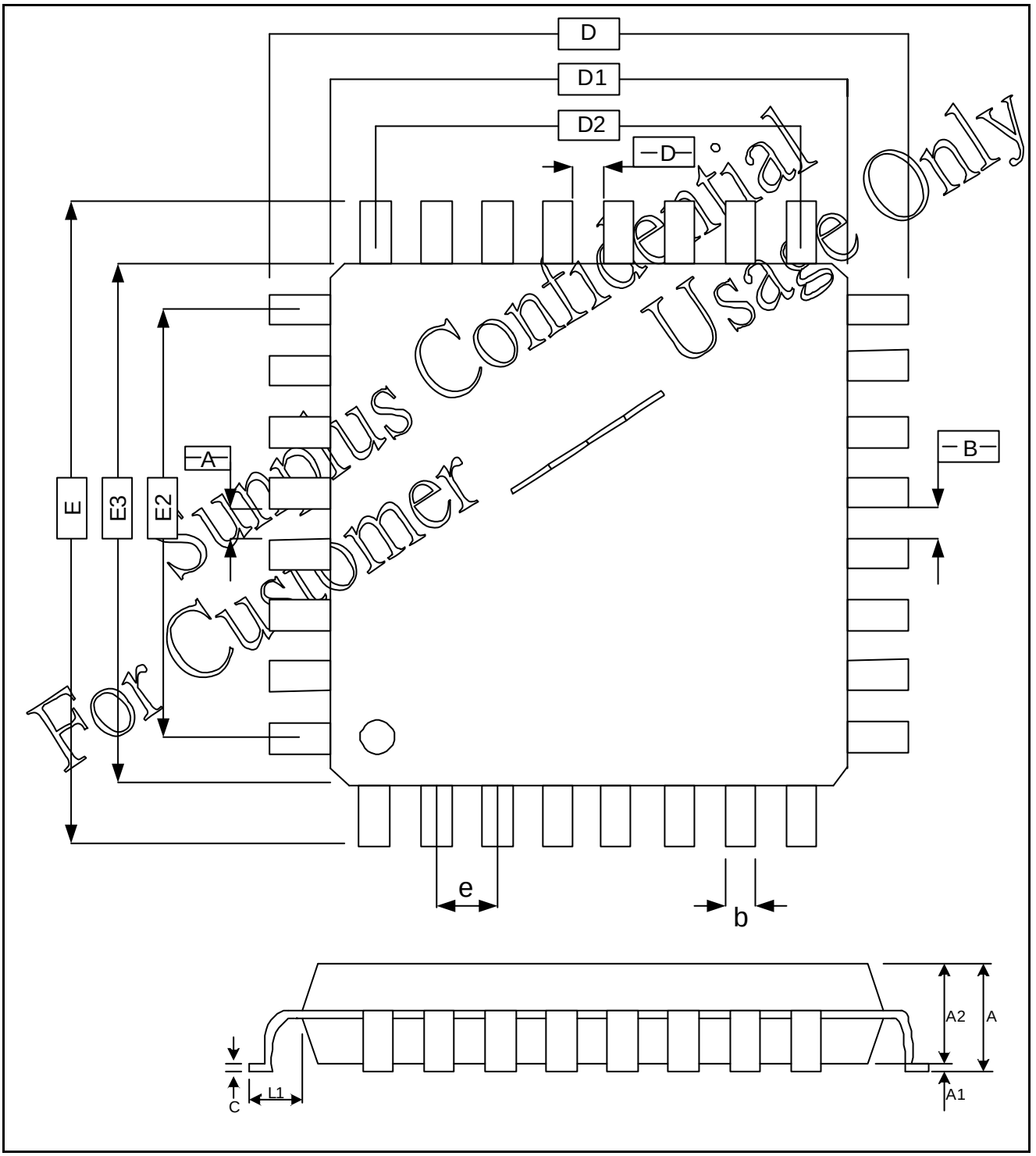
Table 6. Typical Parts List (Internal Voltage Reference)

Locations	Description	Vendor Part Number
C1 - 5, C7	0.1 µF Ceramic Capacitor	Erie RPE112Z5U104M50V
C6	47 µF Capacitor	Mallory CSR13F476KM
L1	Ferrite Bead - Surface Mount	Fair-Rite 2743021447
L2, L3	Ferrite Bead (z < 300Ω @ 5MHz)	ATC LCB0805, Taiyo Yuden BK2125LM182
RESET	470 or 560 Ω 1% Metal Film Resistor	Dale CMF-55C
TRAP	Ceramic Resonator	Murata TPSx.xMJ or MB2 (where x.x = sound carrier frequency in MHz)
-	Schottky Diodes	BAT85 (BAT54F Dual) HP 5082-2305 (1N6263) Siemens BAT 64-04 (Dual)

Note: Vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect SPCA717A performance.

9.PACKAGE/PAD LOCATIONS

9.1. Package Type: 32 pin LQFP



Note: Ambient temperature range: 0℃ - 70℃

9.2. Outline Dimensions

Symbol	MILLIMETER		
	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
D		9.00BSC.	
D1		7.00BSC.	
E		9.00BSC.	
E1		7.00BSC.	
R2	0.08	-	0.20
R1	0.08	-	-
θ	0°	3.5°	7°
θ1	0°	-	-
θ2	11°	12°	13°
θ3	11°	12°	13°
c	0.09	-	0.20
L	0.45	0.60	0.75
L1		1.00REF	
S	0.20	-	-

10. DISCLAIMER

The information appearing in this publication is believed to be accurate.

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凌陽科技
SUNPLUS

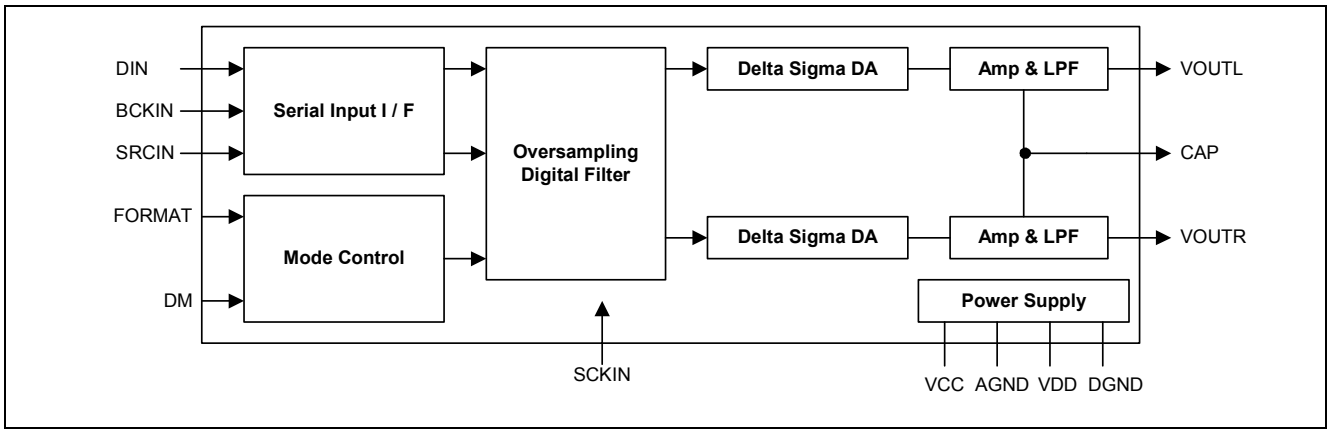
SPCA713A

Digital to Audio Converter

GENERAL DESCRIPTION

The SPCA713A is a low cost stereo digital to analog converter for consumer electronic applications such as MP3 player, Mini Disk, audio or video CD player, SVCD, DVD player, CD/DVD- ROM driver, MIDI applications, Karaoke system, and set-top box etc. The SPCA713A provides, not only the latest technology, but also the full commitment and technical support of Sunplus.

BLOCK DIAGRAM



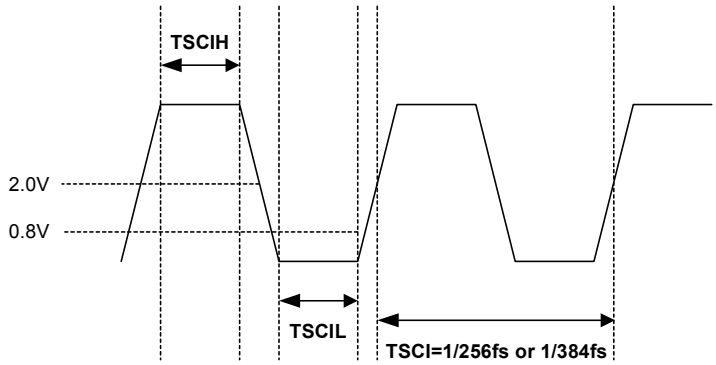
FEATURES

- High resolution:
  - —16 Bit Normal/IIS Format Selectable
- 14 pin SOP package
- High performance:
  - —THD+N: -90 dB
  - —Dynamic Range: 96dB
  - —S/N Ratio: 100db
- High integration:
  - —Oversampling Digital Filter
  - —High-Resolution Delta Sigma DAC
  - —Analog Low Pass Filter
  - —Output Amplifier
  - —On-Chip Digital Filters for:
  - —De-emphasis at 44.1kHz

FUNCTION DESCRIPTION

1. SYSTEM CLOCK

The system clock is either 256fs or 384fs where fs is the standard audio frequency including 32Khz, 44.1Khz, and 48KhZ. The system clock is used to operate the digital filter and delta sigma modulator. The system clock is input through SCKIN (pin14).



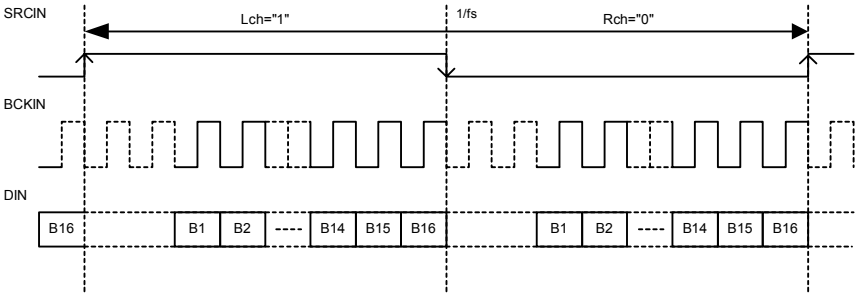
System Clock		
fs	TSCI=1/256fs	TSCI=1/384fs
32kHz	8.192mHz	12.288MHz
44.1kHz	11.2896mHz	16.934MHz
48kHz	12.288mHz	18.432MHz

System Clock High Level TSCIH > 13nsec
System Clock Low Level TSCIL > 13nsec

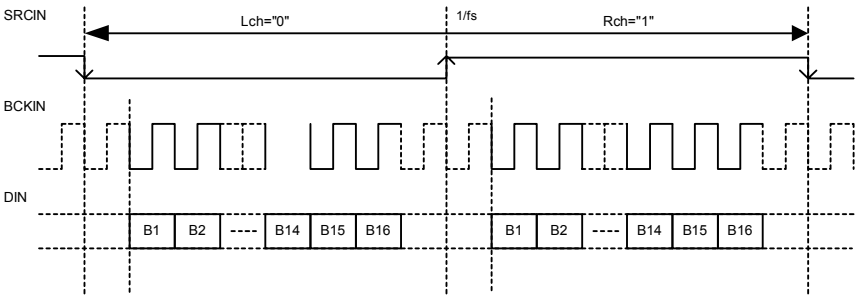
2. SERIAL DIGITAL AUDIO DATA INPUT INTERFACE

Digital audio information is input to the SPCA713A via the DIN (pin2) for audio data input, the SRCIN (pin1) for sampling rate clock, and the BCKIN (pin3) for the bit clock. The SPCA713A can accept both normal and IIS data formats. The normal data format is MSB first, two's complement and right justified; on the other hand, the IIS data format, which is compatible with Philips serial data protocol, is left justified. The relationship of the three input signals is illustrated in the following figures:

Normal Data Format (right justified):



IIS Data format (Left Justified):



Note: Logic high is denoted as either "H" or "1"; logic low is denoted as either "L" or "0" in this document.

3. INTERNAL RESET

When the power supply voltage VCC reaches 2.2V, the internal reset function is initialized. The power-on reset initialization period is 1,024 SCKIN cycles during which the analog out puts are forced to VCC/2.

4. MODE CONTROL

The SPCA713A provides two control functions – Input Format Select and De-emphasis through FORMAT (pin 13) and DM (pin12). They are illustrated in following table:

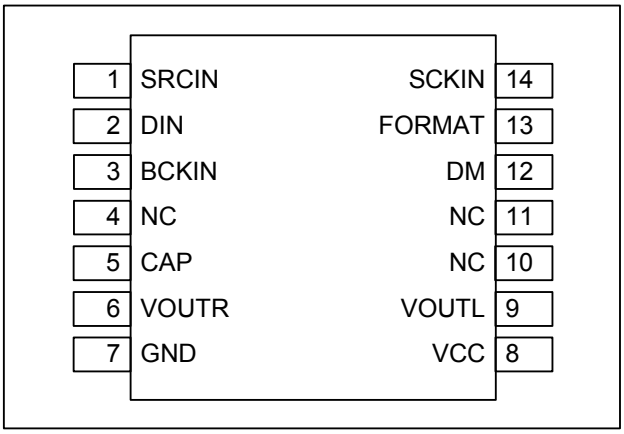
Table1: Selectable Functions

Function	Control
Digital Audio input Format Selection	FORMAT (pin13) = ”0” Normal format selected. FORMAT (pin13) = ”1” IIS format selected
De-emphasis Control at 44.1kHz	DM (pin12) = ”0” De-emphasis OFF DM (pin12) = “1” De-emphasis ON

PIN ASSIGNMENTS

Mnemonic	PIN NO.	I/O	Description
SRCIN	1	IN	Sample Rate Clock Input
DIN	2	IN	Audio Data Input
BCKIN	3	IN	Bit Clock Input for Audio Data
NC	4	-	No Connection
CAP	5	-	R-Channel & L-Channel Output Amp Common Node
VOUTR	6	OUT	R-Channel Output
GND	7	-	Ground
VCC	8	-	Power Supply
VOUTL	9	OUT	L-Channel Output
NC	10	-	No Connection
NC	11	-	No Connection
DM	12	IN	De-emphasis Control, “H”: ON, “L”: OFF
FORMAT	13	IN	Data Format Select, ”H”: IIS Format, ”L”: Normal Format.
SCKIN	14	IN	System Clock Input

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATING

Power Supply Voltage	+ 6.5V
+VCC to VDD Difference	+/- 0.1V
Input Logic Voltage	-0.3V to (VDD + 0.3V)
Power Dissipation	250mW
Operating Temperature Range	-25 C to +85 C
Storage Temperature	-55 C to +125 C

PACKAGE INFORMATION*

Model	Package	Package Drawing No.
SPCA713A	14 pin SOP	114-D

Note: See Package drawing at the end of this data sheet.

ELECTRICAL CHARACTERISTICS

At 25°C, VCC=VDD=5V/3.3V, fs=44.1kHz, 16Bit input data, System Clock = 384/256fs

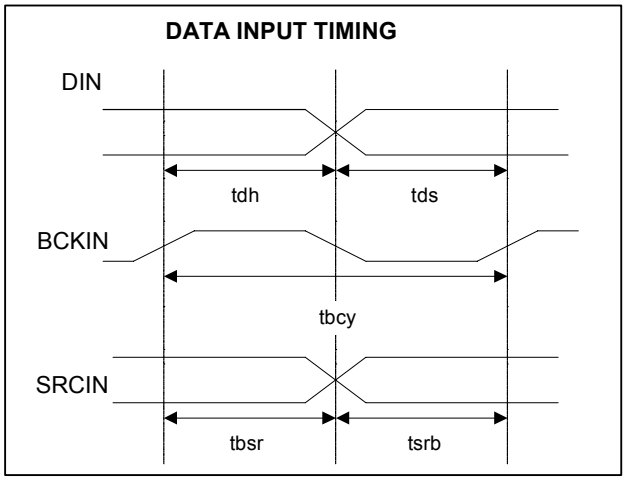
Parameter	Conditions	Min.	Type	Max.	Unit
Resolution			16		Bits
Sampling Frequency		16	44.1	96	kHz
System Clock Frequency			256/384fs		
Audio Data Format			Normal/IIS		
Data Bit Length			16		
Power Supply					
Voltage Range: VDD	VDD=5V	4.5	5	5.5	V
	VDD=3.3V	3.0	3.3	3.7	V
Supply Current: IDD	VDD=5V		13	18	mA
	VDD=3.3V		6	10	mA
Power Dissipation:	VDD=5V		65	90	mW
	VDD=3.3V		20	33	mW
Digital Input/Output					
Input Logic Level					
VIH	Pin14	60%			VDD
VIL				16%	VDD
VIH	Pin1,2,3,12,13	60%			VDD
VIL	--Schmitt Trigger			25%	VDD
Output Logic Level					
VOH		90%			VDD
VOL				10%	VDD
DC Accuracy					
Gain Error			+/- 1	+/- 5	%FSR
Gain Mismatch Ch to Ch			+/- 1	+/- 5	%FSR
Analog Output			VDD		
			5V / 3.3V		
Voltage Range	Vout=0dB		1.1 / 0.7		Vrms
Center Voltage			2.5 / 1.65		V
Load Impedance	AC Load	10			KOhm
Frequency Response		0		20	KHz
Dynamic Performance			VDD		
			5V / 3.3V		
THD+N at FS(0dB)	Fout=1kHz		.003 / .0035	0.006	%
THD+N at –60dB	Fout=1kHz		1.8 / 2.0	5	%
Dynamic Range	EIAJ, A-weighted	90	96 / 94		dB
SNR	EIAJ, A-weighted	92	100 / 97		dB
Channel Separation	Fout=1kHz	90	97 / 95		dB

TIMING CHARACTERISTICS

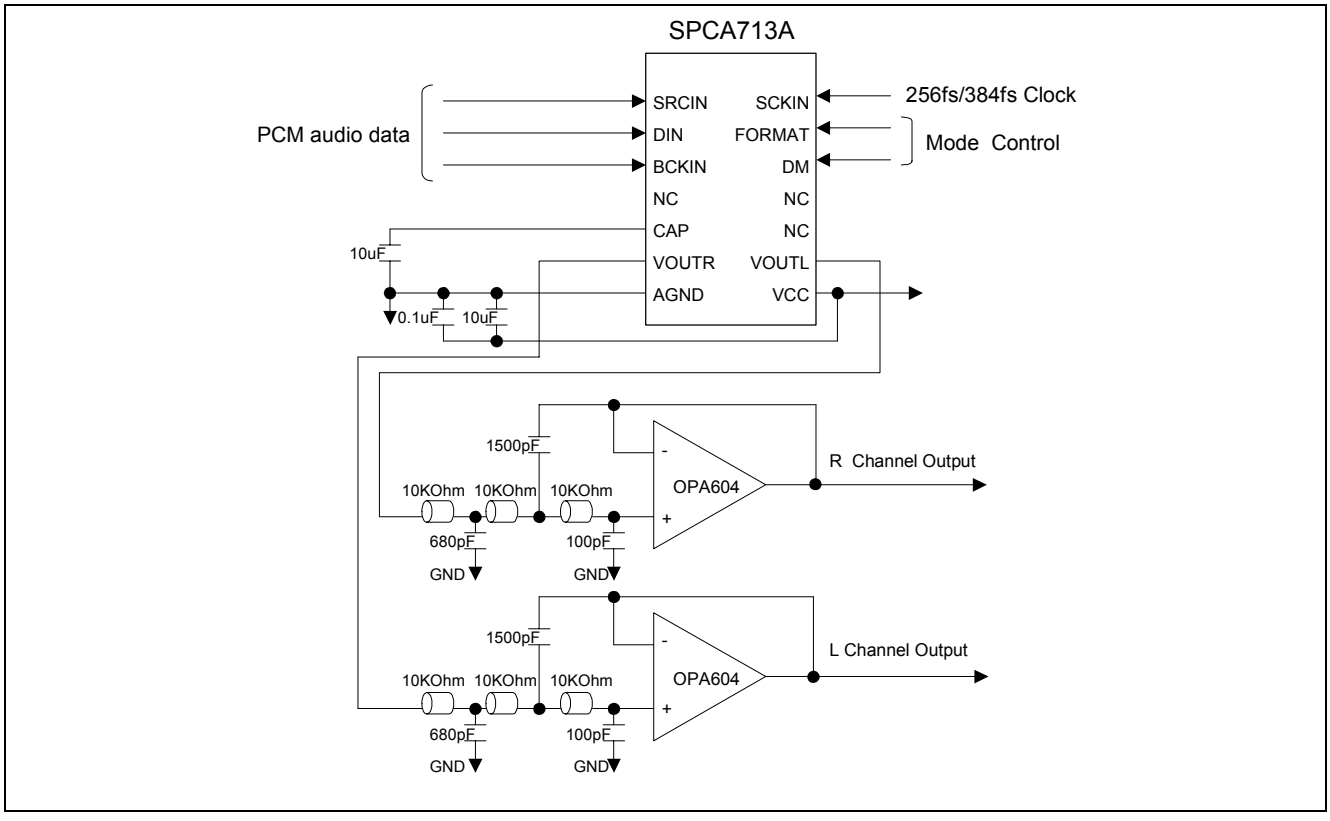
At 25°C, VCC = VDD = 5V/3.3V, fs = 44.1kHz, 16Bit input data, System Clock = 384/256fs

Parameter	Symbol	Value	Unit
Data Input Timing			
DIN setup time	tds	>30	ns
DIN hold time	tdh	>30	ns
BCKIN high-level, low-level	Tbcwh, tbcwl	>50	ns
BCKIN pulse cycle time	tbcy	>100	ns
BCKIN rising edge to SRCIN	tbsr	>30	ns
SRCIN to BCKIN rising edge	tsrb	>30	ns

TIMING DIAGRAM



APPLICATION CIRCUIT NOTE



1. BYPASSING POWER SUPPLY

A 10uF tantalum capacitor can be used for bypassing the power supplies. The bypass capacitor should be connected as close as possible to the unit and a 0.1uF ceramic capacitor is recommended to connect in parallel with it.

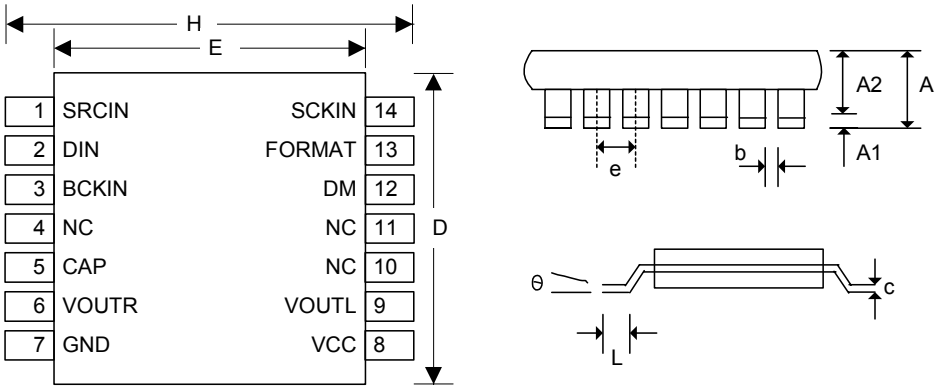
2. OUTPUT FILTERING

The internal low pass filter is designed to have a 3dB band width at 100kHz. To limit out of band noise, an external 3rd order filter, as shown in the application circuit diagram, is recommended, especially when the chip is to drive a wide band amplifier.

PACKAGE DRAWING NO. 114-S

Model	Package	Package Drawing No.
SPCA713A	14 pin SOP	114-S

Package outline drawing is shown below:



Symbols	Dimensions In Milimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	-	0.25	0.004	-	0.010
A2	-	1.45	-	-	0.057	-
b	0.33	0.41	0.51	0.013	0.016	0.020
c	0.19	0.20	0.25	0.0075	0.008	0.0098
D	8.53	8.64	8.74	0.336	0.340	0.344
H	5.79	5.99	6.20	0.228	0.236	0.244
E	3.81	3.91	3.99	0.150	0.154	0.157
e	-	1.27	-	-	0.050	-
L	0.38	0.71	1.27	0.015	0.028	0.050
θ	0°		8°	0°		8°

DISCLAIMER

REVISION HISTORY

Date	Revision #	Description	Page
APR. 03, 2001	1.0	Original	7

11. REVISION HISTROY

Date	Revision #	Description	Page
NOV. 11, 2002	0.1	Original	21

CD-ROM 用ヘッドホンアンプ

BH3541F / BH3544F

BH3541F、BH3544F はデジタルソース向けのデュアルヘッドホンアンプです。BH3541F はゲイン 0dB、BH3544F はゲイン 6dB 固定で、外付けゲイン設定が不要です。BH3541F、BH3544F ともミュート機能を内蔵することによって電源 ON-OFF 時のボツ音防止対策が簡単に行えます。また、サーマルシャットダウン回路の内蔵により、短絡などによる IC 破壊を防止します。

品 名	固定ゲイン
BH3541F	0dB
BH3544F	6dB

●用途

CD-ROM、CD、MD、パソコン、ノートパソコン、カムコーダなどヘッドホン出力を有する機器

●特長

1）ミュート機能内蔵によって電源 ON-OFF 時のボツ音防止対策が可能。
2）サーマルシャットダウン回路（150°C）内蔵によって短絡による IC 破壊を防止。
3）SOP8pin の小型パッケージである。

●絶対最大定格（Ta = 25°C）

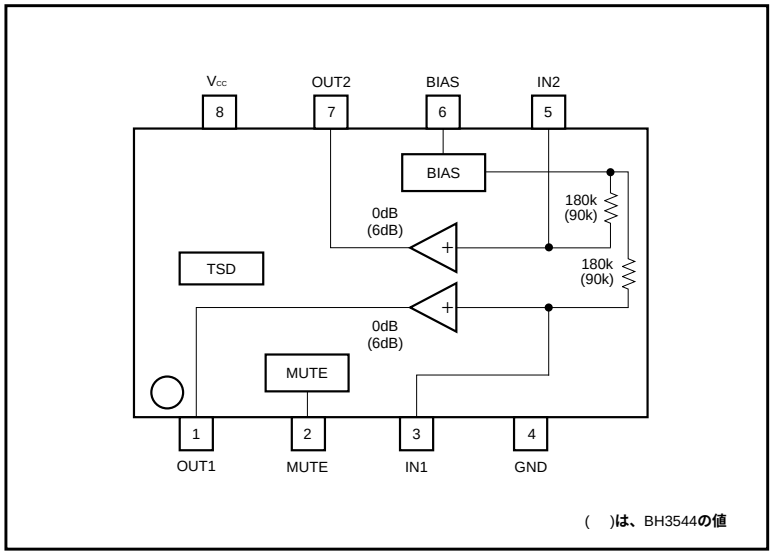
Parameter	Symbol	Limits	Unit
印加電圧	V_{Max}	7.0	V
許容損失	Pd	450 ＊	mW
動作温度範囲	Topr	–25 ~ +75	°C
保存温度範囲	Tstg	–55 ~ +125	°C

＊Ta=25°C以上で使用する場合は、1°Cにつき4.5mWを減じる。

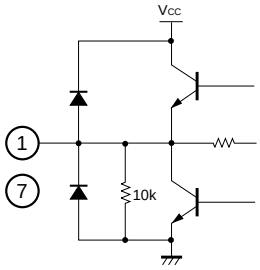
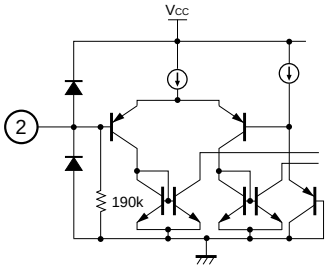
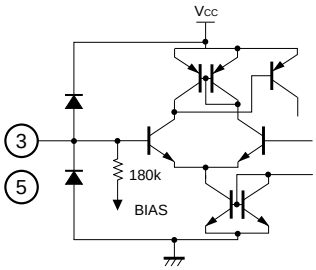
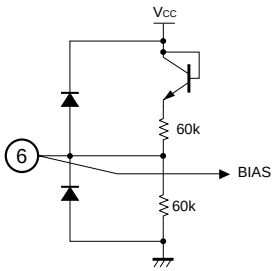
●推奨動作条件（Ta = 25°C）

Parameter	Symbol	Min.	Typ.	Max.	Unit
電源電圧	V_{CC}	2.8	–	6.5	V

●ブロックダイアグラム


Vcc
OUT2
BIAS
IN2
8
7
6
5
BIAS
180k
(90k)
0dB
(6dB)
TSD
180k
(90k)
0dB
(6dB)
MUTE
1
2
3
4
OUT1
MUTE
IN1
GND
( )は、BH3544の値

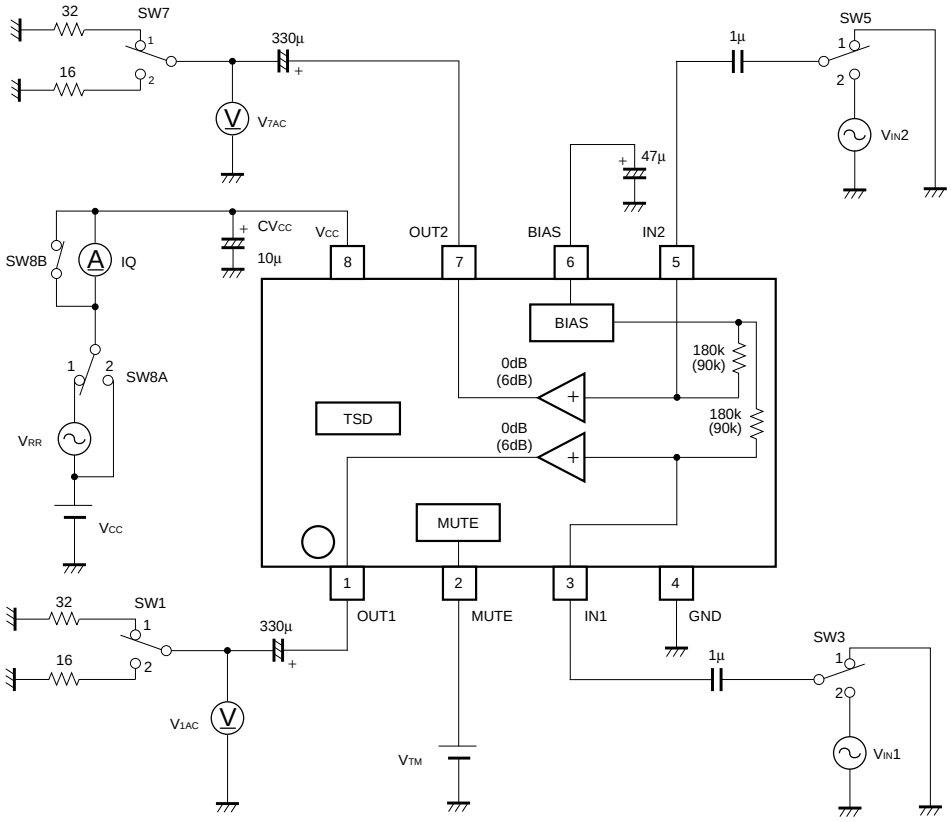
●各端子説明

Pin No.	端子名	I / O	端子電圧	内部等価回路図	機　能
1	OUT1	O	2.1V		出力端子
7	OUT2	O	2.1V (Vcc=5V)		
2	MUTE	I	0.1V (Open時)		ミュートコントロール端子 (電源ON・OFF時はポツ音対策としてLoにする。) 動作　：Hi MUTE ：Lo（Open）
3	IN1	I	2.1V		入力端子
5	IN2	I	2.1V (Vcc=5V)		
6	BIAS	I / O	2.1V (Vcc=5V)		バイアス端子 (外付けコンデンサの47μFはポツ音対策用の時定数を兼用していますので、変更の際は十分評価の程お願いします。)
4	GND	I	–	―――	―――
8	Vcc	I	–	―――	―――

●**電気的特性**（特に指定のない限り Ta = 25°C, V_{CC} = 5.0V, R_L = 32Ω, f = 1kHz,
BH3541F : V_{IN} = 0dBV, BH3544F : V_{IN} = –6dBV）

Parameter		Symbol	Min.	Typ.	Max.	Unit	Conditions
無信号時回路電流		I_Q	4	7	10	mA	V_{IN}=0Vrms
ミュート端子制御電圧		V_{TM}	0.3	0.7	1.6	V	–
電圧利得	BH3541F	G_{VC}	–2	0	2	dB	–
	BH3544F		4	6	8	dB	–
チャンネル間電圧利得差		ΔG_{VC}	–0.5	0	0.5	dB	–
全高調波歪率		THD	–	0.02	0.1	%	BW=20~20kHz
定格出力1		P_{O1}	25	31	–	mW	R_L=32Ω, THD < 0.1%
定格出力2		P_{O2}	50	62	–	mW	R_L=16Ω, THD < 0.1%
出力雑音電圧		V_{NO}	–	–93	–85	dBV	BW=20~20kHz, Rg=0Ω
チャンネルセパレーション		CS	82	90	–	dB	Rg=0Ω
ミュート減衰量		ATT	70	80	–	dB	Rg=0Ω
リップルリジェクション		RR	50	57	–	dB	f_{RR}=100Hz, V_{RR}=–20dBV

●**測定回路図**



( )は、BH3544の値

Fig.1

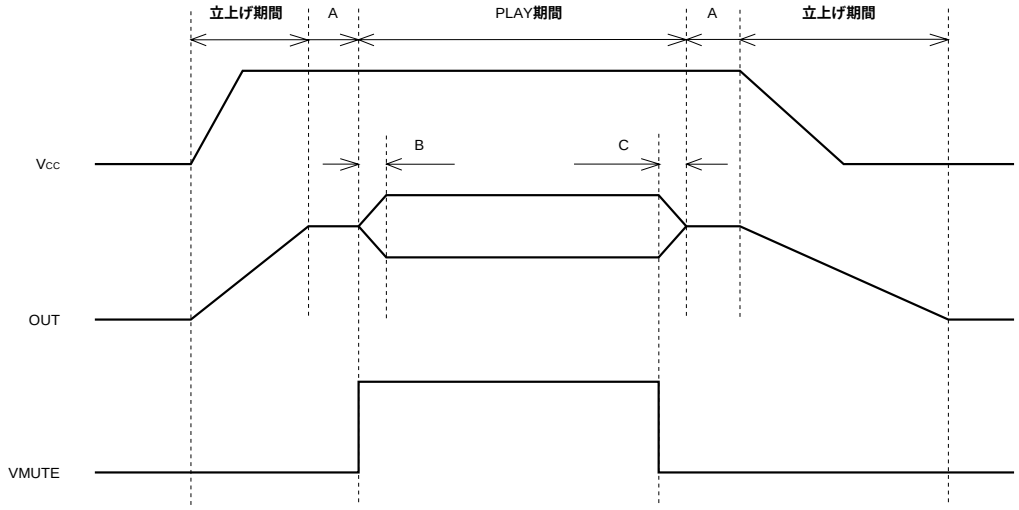
●測定条件表

記号	SW表						Monitor	Conditions
	SW1	SW3	SW5	SW7	SW8A	SW8B		
I_Q	1	1	1	1	2	OFF	IQ	–
V_{TM}	–	–	–	–	–	–	–	–
G_{VC}	1	2	2	1	2	ON	V1AC, V2AC	f=1kHz, V_{IN}1/2=0dBV (V_{IN}1/2=–6dBV), VTM=1.6V
ΔG_{VC}	–	–	–	–	–	–	–	GVC1–GVC2
THD	1	2	2	1	2	ON	V1AC, V2AC	fin=1kHz, V_{IN}1/2=0dBV (V_{IN}1/2=–6dBV), VTM=1.6V
P_{O1}	1	2	2	1	2	ON	V1AC, V2AC	fin=1kHz, V_{IN}1/2=0dBV (V_{IN}1/2=–6dBV), VTM=1.6V
P_{O2}	2	2	2	2	2	ON	V1AC, V2AC	fin=1kHz, V_{IN}1/2=0dBV (V_{IN}1/2=–6dBV), VTM=1.6V
V_{NO}	1	1	1	1	2	ON	V1AC, V2AC	–
CS	1 1	1 2	2 1	1 1	2 2	ON ON	V1AC, V2AC V1AC, V2AC	fin=1kHz, V_{IN}2=0dBV (V_{IN}2=–6dBV), VTM=1.6V fin=1kHz, V_{IN}1=0dBV (V_{IN}1=–6dBV), VTM=1.6V
ATT	1	2	2	1	2	ON	V1AC, V2AC	fin=1kHz, V_{IN}1/2=0dBV (V_{IN}1/2=–6dBV), VTM=0.3VB
RR	1	1	1	1	1	ON	V1AC, V2AC	V_{RR}=–20dBV, f_{RR}=100Hz

*( )は、BH3544Fの値。

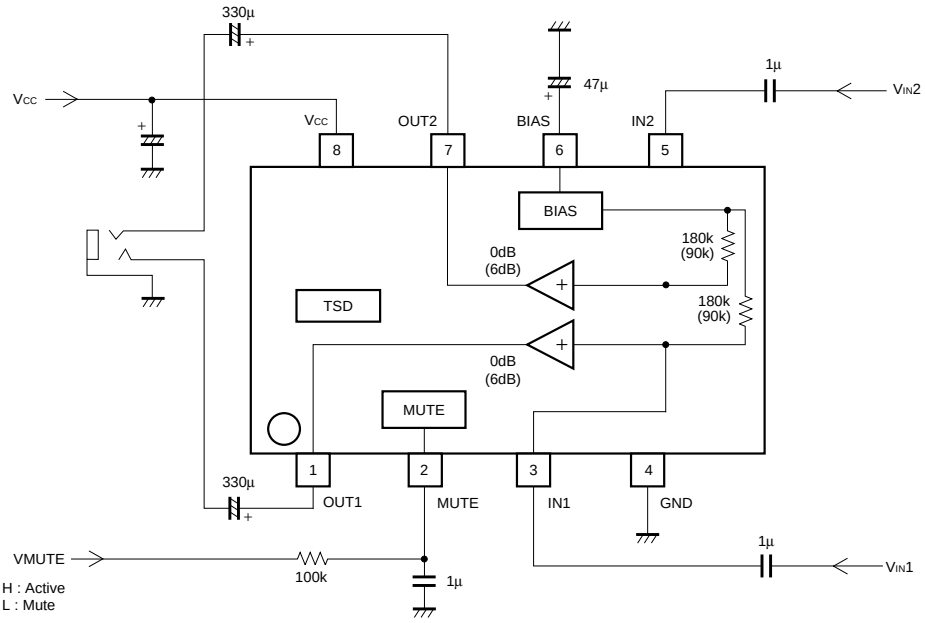
●動作説明

立上げタイミング



A：ミュート期間（電源ON/OFF時はボツ音対策としてV_{MUTE}=Loにてご使用ください。）
B：ミュート解除時間（外付けC2,R2により、ミュート解除時のボツ音対策としているため、時定数を持ちますのでタイミングにはご注意ください。）
C：ミュート開始時間（解除時と同様に時定数を持ちます。）

●応用例



( )は、BH3544の値

Fig.2

●外付け部品の説明

(1) 入力カップリングコンデンサ（C3、C5）

低域のカットオフ周波数により決定されます。本 IC の入力インピーダンスは 180kΩのため、下記の式から求められますが、バラツキ、温特等の考慮を必要とします。（積層セラミックコンデンサを推奨します。）

$$C3\ (C5) = 1 / (2\pi \times 180k\Omega \times f)$$

(2) バイアスコンデンサ（C6）

V_{CC} = 5V の時は 47µF、V_{CC} = 3V の時は 33µF を推奨します。容量値をあまり下げますと、電気的特性の悪化やボツ音の発生原因となりますので、変更の際は十分ご確認のうえ、決定してください。

(3) ミュート端子ボツ音対策（R2、C2）

GND に対してインピーダンス（190kΩ）を持っているため、R2 を大きくしすぎますと、ミュートが解除できないことがありますのでご注意願います。

(4) 出力カップリングコンデンサ（C1、C7）

低域のカットオフ周波数により決定されます。出力の負荷抵抗値を R_L として（出力に保護または、電流制限のために抵抗 R_X を入れると仮定する）、下記の式から求められます。

$$C1\ (C7) = 1 / (2\pi \times (R_L + R_X) \times f)$$

(5) 入力ゲイン調整抵抗（R3、R4）（BH3544F のみ）

外付け抵抗（R3、R4）により、入力ゲインの調整ができます。下記の式から求められるゲインに設定できます。

$$G_{VC} = 6 + 20\log (90k\Omega / (90k\Omega + R3)) \ [dB]$$

●使用上の注意

応用例は推奨すべきものと確信しておりますが、ご使用にあたっては特性の確認を十分にお願いします。その他外付け回路定数を変更してご使用になる時は静特性のみならず、過渡特性も含め外付け部品及び当社 IC のバラツキ等を考慮して十分なマージンを見て決定してください。

●電気的特性曲線

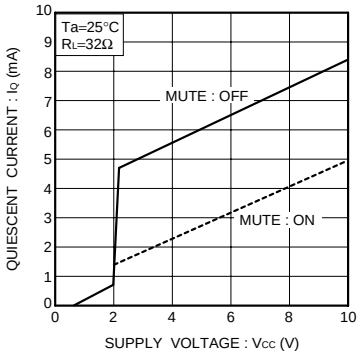


Fig.3 無信号時回路電流ー電源電圧特性

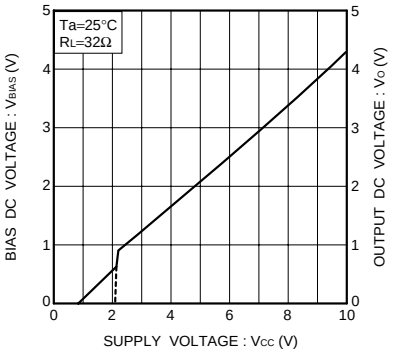


Fig.4 端子直流電圧ー電源電圧特性

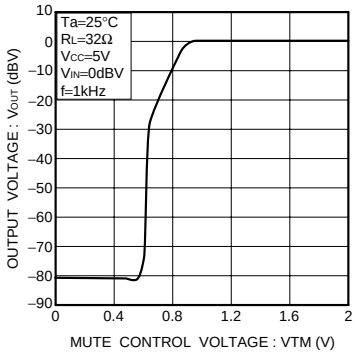


Fig.5 出力電圧ーミュート電圧特性

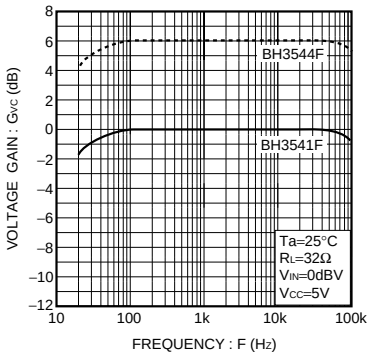


Fig.6 電圧利得ー周波数特性

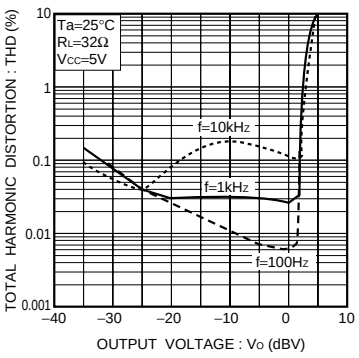


Fig.7 全高調波歪率ー出力電圧特性（Ⅰ）

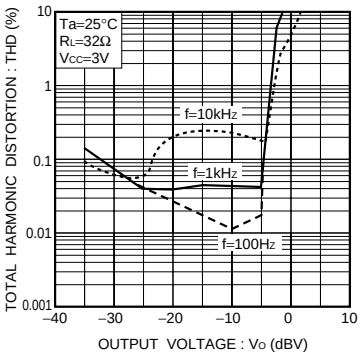


Fig.8 全高調波歪率ー出力電圧特性（Ⅱ）

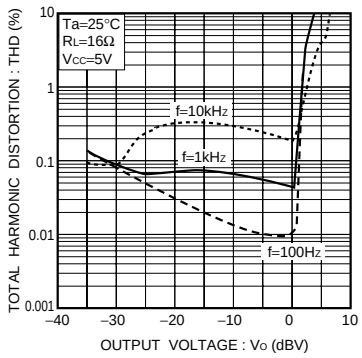


Fig.9 全高調波歪率ー出力電圧特性（Ⅲ）

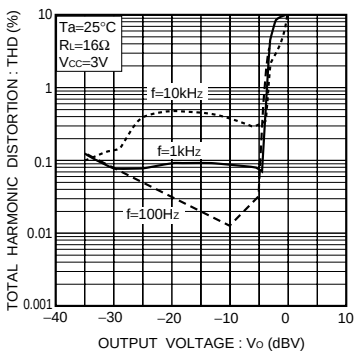


Fig.10 全高調波歪率ー出力電圧特性（Ⅳ）

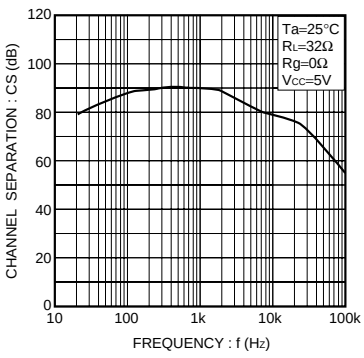


Fig.11 チャンネルセパレーション
ー周波数特性

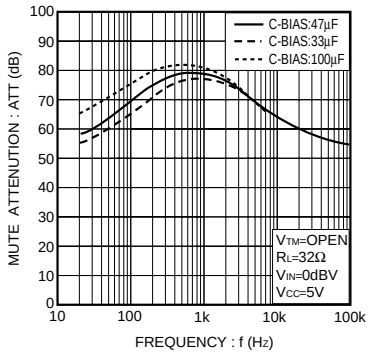


Fig.12 **ミュート減衰量ー周波数特性**

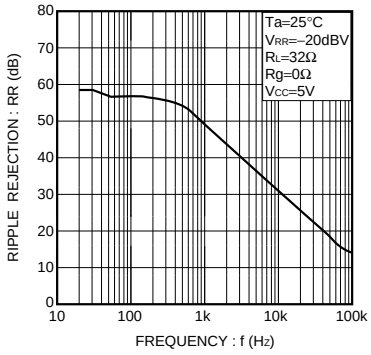


Fig.13 **リップルリジェクション ー周波数特性**

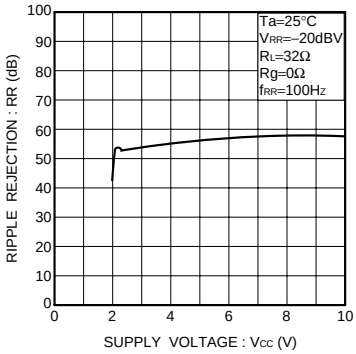
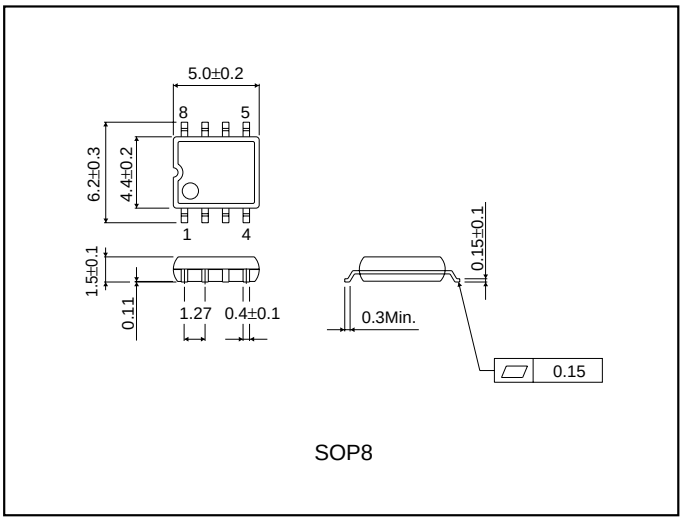


Fig.14 **リップルリジェクション ー電源電圧特性**

●**外形寸法図** (Units : mm)



SOP8

SINGLE-CHIP, LI-ION CHARGE MANAGEMENT IC FOR HANDHELD APPLICATIONS (bqTINY™)

FEATURES

- **Small 3 mm × 3 mm MLP (QFN) Package**
- **Ideal for Low-Dropout Designs for Single-Cell Li−Ion or Li−Pol Packs in Space Limited Applications**
- **Integrated Power FET and Current Sensor for Up to 1-A Charge Applications**
- **Reverse Leakage Protection Prevents Battery Drainage**
- **Integrated Current and Voltage Regulation**
- **± 0.5% Voltage Regulation Accuracy**
- **Charge Termination by Minimum Current and Time**
- **Precharge Conditioning With Safety Timer**
- **Status Outputs for LED or System Interface Indicates Charge and Fault Conditions**
- **Battery Insertion and Removal Detection**
- **Works With Regulated and Unregulated Supplies**
- **Short-Circuit Protection**

APPLICATIONS

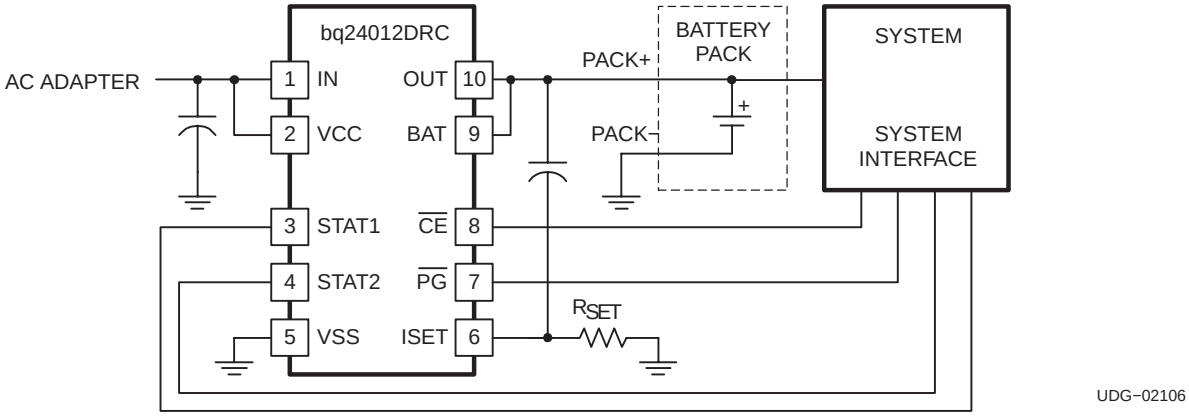
- **Cellular Phones**
- **PDAs, MP3 Players**
- **Digital Cameras**
- **Internet Appliances**

DESCRIPTION

The bqTINY™ series are highly integrated Li-Ion and Li-Pol linear charge management devices targeted at space limited portable applications. The bqTINY™ series offer integrated powerFET and current sensor, reverse blocking protection, high accuracy current and voltage regulation, charge status, and charge termination, in a small package.

The bqTINY™ charges the battery in three phases: conditioning, constant current, and constant voltage. Charge is terminated based on minimum current. An internal charge timer provides a backup safety feature for charge termination. The bqTINY™ automatically re-starts the charge if the battery voltage falls below an internal threshold. The bqTINY™ automatically enters sleep mode when V_{CC} supply is removed.

In addition to the standard features, different versions of the bqTINY™ offer a multitude of additional features. These include temperature sensing input for detecting hot or cold battery packs; power good ($\overline{PG}$) output indicating the presence of input power; a TTL−level charge-enable input ($\overline{CE}$) used to disable or enable the charge process; and a TTL-level timer and termination enable ($\overline{TTE}$) input used to disable or enable the fast-charge timer and charge termination.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

bqTINYis a trademark of Texas Instruments Incorporated.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	CHARGE REGULATION VOLTAGE (V)(1)	OPTIONAL FUNCTIONS(1)	PART NUMBER(2)	MARKINGS
−40°C to 125°C	4.2	$\overline{PG}$ and TS	bq24010DRC	AZN
	4.2	$\overline{PG}$ and $\overline{CE}$	bq24012DRC	AZP
	4.2	$\overline{CE}$ and $\overline{TTE}$	bq24013DRC	AZQ
	4.2	$\overline{CE}$ and TS	bq24014DRC	AZR

(1) Contact Texas Instruments for other options.
(2) The DRC package is available only taped and reeled. Add R suffix to device type (e.g. bq24210DRCR) to order. Quantities are 3,000 devices per reel.

DISSIPATION RATINGS

PACKAGE	θ_{JA}	T_A < 40°C POWER RATING	DERATING FACTOR ABOVE T_A = 40°C
DRC(1)	47 °C/W	1.5 W	0.021 W/°C

(1) This data is based on using the JEDEC High-K board and the exposed die pad is connected to a copper pad on the board. This is connected to the ground plane by a 2x3 via matrix.

ABSOLUTE MAXIMUM RATINGS(1)

			UNIT
Supply voltage range, (V_{CC} all with respect to V_{SS})		−0.3 to 18	V
Input voltage range(2)	IN, STAT1, STAT2, TS, $\overline{PG}$, $\overline{CE}$, $\overline{TTE}$	−0.3 to VCC	
	BAT, OUT, ISET	−0.3 to 7	VDC
Voltage difference between V_{CC} and IN inputs $V_{CC} - V_{IN}$		± 0.5	V
Output sink/source current	STAT1, STAT2, $\overline{PG}$	15	mA
Output current	IN, OUT	1.5	A
Operating free−air temperature range, T_A		−40 to 125	°C
Junction temperature range, T_J			
Storage temperature, T_{stg}		−65 to 150	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are DC and with respect to V_{SS}.

RECOMMENDED OPERATING CONDITIONS(1)

	MIN	NOM	MAX	UNIT
Supply voltage(1), V_{CC}	3.0		16.5	V
Input voltage(1), V_{IN}	3.0		16.5	
Operating junction temperature range, T_J	−40		125	°C

(1) Pins VCC and IN must be tied together.

ELECTRICAL CHARACTERISTICS

over $0°C \le T_J \le 125°C$ and recommended supply voltage, unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CURRENT					
VCC current, $I_{CC(VCC)}$	$V_{CC} > V_{CC(min)}$, STATx pins in OFF state	0	3.5	5	mA
Sleep current, $I_{CC(SLP)}$	Sum of currents into OUT and BAT pins, $V_{CC} < V_{(SLP)}$			5	µA
Input bias current on BAT pin, $I_{IB(BAT)}$				500	nA
Input current on TS pin, $I_{IB(TS)}$	$V_{I(TS)} \le 10$ V			1	µA
Input current on $\overline{CE}$ pin, $I_{IB(CE)}$				1	
Input bias current on $\overline{TTE}$ pin, $I_{IB(TTE)}$				1	
VOLTAGE REGULATION $V_{O(REG)} + V_{(DO-MAX)} \le V_{CC}$, $I_{(TERM)} < I_{O(OUT)} \le 1$ A					
Output voltage, $V_{O(REG)}$			4.20		V
Voltage regulation accuracy	$T_A = 25°C$	−0.5%		0.5%	
		−1%		1%	
Dropout voltage ($V_{(IN)} - V_{(OUT)}$), $V_{(DO)}$	$V_{O(REG)} + V_{(DO-MAX)}) \le V_{CC}$, $I_{O(OUT)} = 1$A		650	790	mV
CURRENT REGULATION					
Output current range, $I_{O(OUT)}$ (1)	$V_{CC} \ge 4.5$ V, $V_{IN} \ge 4.5$ V, $V_{I(BAT)} > V_{(LOWV)}$, $V_{IN} - V_{I(BAT)} > V_{(DO-MAX)}$	100		1000	mA
Output current set voltage, $V_{(SET)}$	Voltage on ISET pin, $V_{CC} \ge 4.5$ V, $V_{IN} \ge 4.5$ V, $V_{I(BAT)} > V_{(LOWV)}$, $V_{IN} - V_{I(BAT)} > V_{(DO-MAX)}$ $V_{O(REG)} = 4.2$ V	2.45	2.50	2.55	V
Output current set factor, $K_{(SET)}$	50 mA ≤ $I_{O(OUT)}$ ≤ 1000 mA, $V_{I(ISET)} \ge V_{(TAPER)}$	315	335	355	
	10 mA ≤ $I_{O(OUT)}$ < 50 mA, $V_{I(ISET)} \ge V_{(TAPER)}$	315	372	430	
	10 mA ≤ $I_{O(OUT)}$ < 50 mA, $V_{I(ISET)} < V_{(TAPER)}$	350		1000	
PRECHARGE AND SHORT-CIRCUIT CURRENT REGULATION					
Precharge to fast-charge transition threshold, $V_{(LOWV)}$	Voltage on BAT pin	2.80	2.95	3.10	V
Precharge to short-circuit transition threshold, $V_{(SC)}$	Voltage on BAT pin	1.0	1.4	1.8	
Precharge range, $I_{O(PRECHG)}$ (2)	$V_{(SC)} < V_{I(BAT)} < V_{(LOWV)}$, $t < t_{(PRECHG)}$	10		100	mV
Precharge set voltage, $V_{(PRECHG)}$	Voltage on ISET pin, $V_{(SC)} < V_{I(BAT)} < V_{(LOWV)}$	225	250	280	
Short circuit current, I_{SC}	$V_{(SC)} > V_{I(BAT)}$	660	900	1200	µA
CHARGE TAPER AND TERMINATION DETECTION					
Charge taper detection range, $I_{(TAPER)}$ (3)	$V_{I(BAT)} > V_{(RCH)}$, $t < t_{(TAPER)}$	10		100	mA
Charge taper detection set voltage, $V_{(TAPER)}$	Voltage on ISET pin, $V_{I(BAT)} > V_{(RCH)}$, $t < t_{(TAPER)}$, $V_{I(BAT)} = V_{O(REG)}$	225	250	275	mV
Charge termination detection set voltage, $V_{(TERM)}$	Voltage on ISET pin, $V_{I(BAT)} = V_{O(REG)}$, $V_{I(BAT)} > V_{(RCH)}$, $I_{(TERM)} = K_{(SET)} \times V_{(TERM)} / R_{(SET)}$	5.0	17.5	30.0	
TEMPERATURE COMPARATOR					
Lower threshold, $V_{(TS1)}$	Voltage on TS pin	29	30	31	%VCC
Upper threshold, $V_{(TS2)}$	Voltage on TS pin	60	61	62	
Hysteresis			1		

(1)
$$I_{O(OUT)} = \frac{\left(K_{(SET)} \times V_{(SET)}\right)}{R_{SET}}$$

(2)
$$I_{O(PRECHG)} = \frac{\left(K_{(SET)} \times V_{(PRECHG)}\right)}{R_{SET}}$$

(3)
$$I_{O(TAPER)} = \frac{\left(K_{(SET)} \times V_{(TAPER)}\right)}{R_{SET}}$$

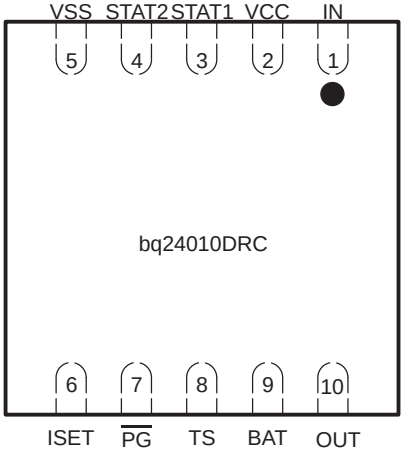
ELECTRICAL CHARACTERISTICS (continued)

over $0°C \le T_J \le 125°C$ and recommended supply voltage, unless otherwise noted

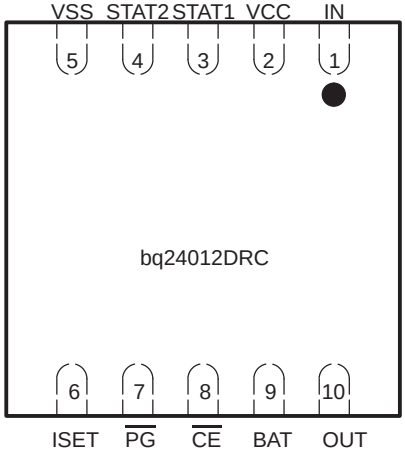
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
BATTERY RECHARGE THRESHOLD					
Recharge threshold, $V_{(RCH)}$		$V_{O(REG)}$ −0.135	$V_{O(REG)}$ −0.1	$V_{O(REG)}$ −0.075	V
STAT1, STAT2, and $\overline{PG}$ OUTPUTS					
Output (low) saturation voltage, V_{OL}	I_O = 10 mA			0.5	V
CHARGE ENABLE ($\overline{CE}$) AND TIMER AND TERMINATION ENABLE ($\overline{TTE}$) INPUTS					
Low-level input voltage, V_{IL}	I_{IL} = 1 µA	0		0.8	V
High-level input voltage, V_{IH}	I_{IH} = 1 µA	2.0			
TIMERS					
Precharge time, $t_{(PRECHG)}$		1,548	2,065	2,581	s
Taper time, $t_{(TAPER)}$		1,548	2,065	2,581	
Charge time, $t_{(CHG)}$		15,480	20,650	25,810	
SLEEP COMPARATOR					
Sleep mode entry threshold voltage, V_{SLP}	$V_{POR} \le V_{(IBAT)} \le V_{O(REG)}$			$V_{CC} \le V_{I(BAT)}$ +30 mV	V
Sleep mode exit threshold voltage	$V_{POR} \le V_{(IBAT)} \le V_{O(REG)}$	$V_{CC} \ge V_{I(BAT)}$ +22 mV			
Sleep mode deglitch time	VCC decreasing below threshold, 100 ns fall time, 10 mV overdrive	250		650	ms
BATTERY DETECTION THRESHOLDS					
Battery detection current, $I_{(DETECT)}$	$2 V \le V_{(IBAT)} \le V_{(RCH)}$	−3.1	−4.6	−6.1	mA
Battery detection time, $t_{(DETECT)}$	$2 V \le V_{(IBAT)} \le V_{(RCH)}$	100	125	150	ms
Fault current, $I_{(FAULT)}$	$V_{(IBAT)} < V_{(RCH)}$ and/or $t > t_{(PRECHG)}$	660	900	1200	µA
POWER−ON RESET AND INPUT VOLTAGE RAMP RATE					
Power−on reset threshold voltage, V_{POR}(4)		2.25	2.5	2.75	V

(4) Ensured by design. Not production tested.

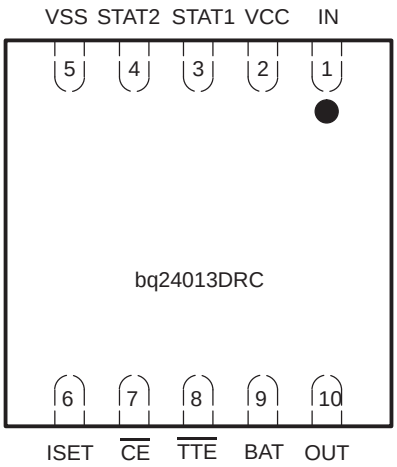
DRC PACKAGE
(TOP VIEW)



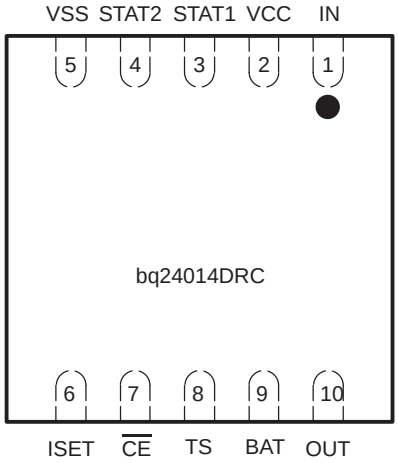
DRC PACKAGE
(TOP VIEW)



DRC PACKAGE
(TOP VIEW)



DRC PACKAGE
(TOP VIEW)

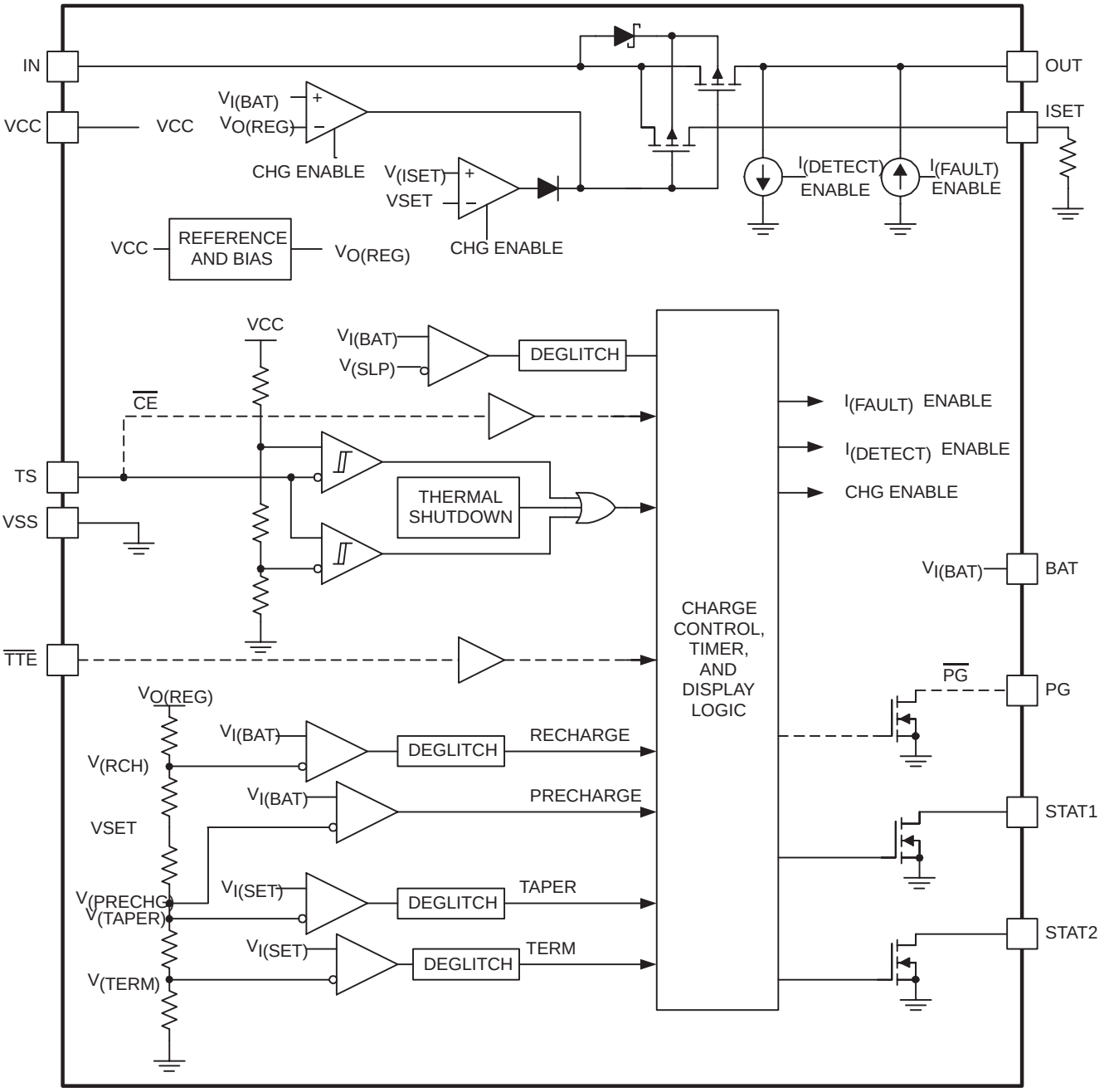


TERMINAL FUNCTIONS

NAME	TERMINAL				I/O	DESCRIPTION
	bq24010	bq24012	bq24013	bq24014		
BAT	9	9	9	9	I	Battery voltage sense input
$\overline{CE}$	−	8	7	7	I	Charge enable input (active low)
IN	1	1	1	1	I	Charge input voltage. This input must be tied to the VCC pin.
ISET	6	6	6	6	O	Charge current set point
OUT	10	10	10	10	O	Charge current output
$\overline{PG}$	7	7	−	−	O	Power good status output (open collector)
STAT1	3	3	3	3	O	Charge status output 1 (open collector)
STAT2	4	4	4	4	O	Charge status output 2 (open collector)
$\overline{TTE}$	−	−	8	−	I	Timer and termination enable input (active low)
TS	8	−	−	8	I	Temperature sense input
VCC	2	2	2	2	I	VCC supply input

VSS	5	5	5	5	−	Ground input
Exposed Thermal PAD	pad	pad	pad	pad	−	There is an internal electrical connection between the exposed thermal pad and V_{SS} pin of the device. The exposed thermal pad must be connected to the same potential as the Vss pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. V_{SS} pin must be connected to ground at all times.

FUNCTIONAL BLOCK DIAGRAM



Dotted lines represent optional features

UDG−02108

TYPICAL CHARACTERISTICS

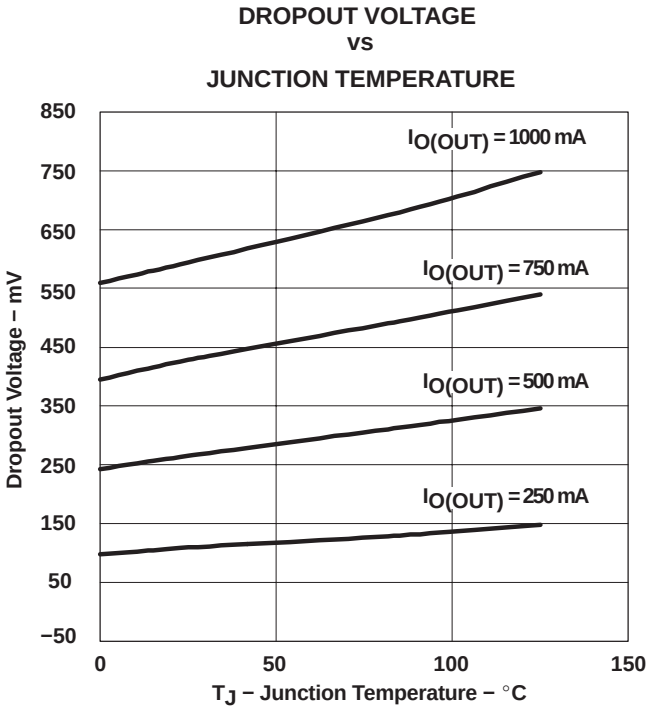


Figure 1

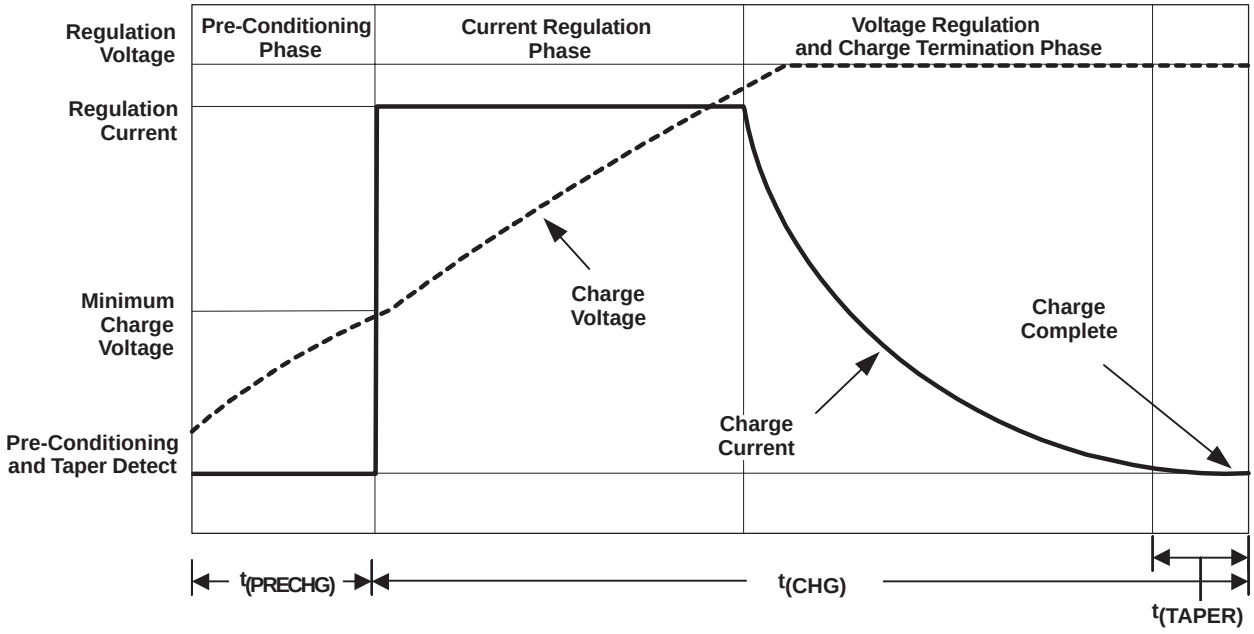


Figure 2. Typical Charging Profile

FUNCTIONAL DESCRIPTION

The bqTINY™ supports a precision Li-Ion, Li-Pol charging system suitable for single-cells . Figure 2 shows a typical charge profile, application circuit and Figure 5 shows an operational flow chart.

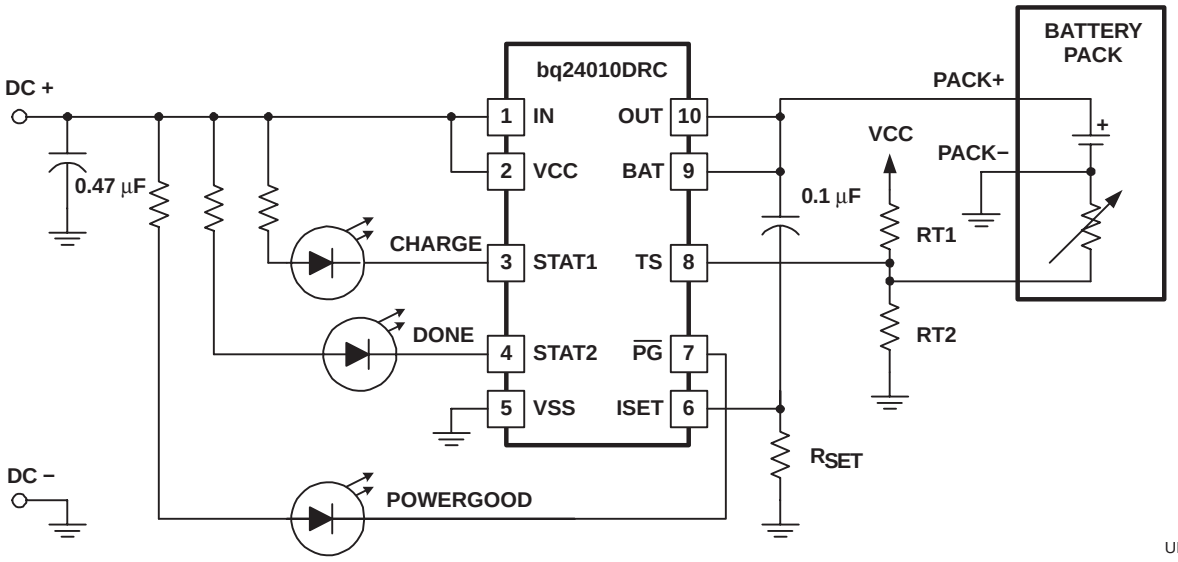


Figure 3. Typical Application Circuit

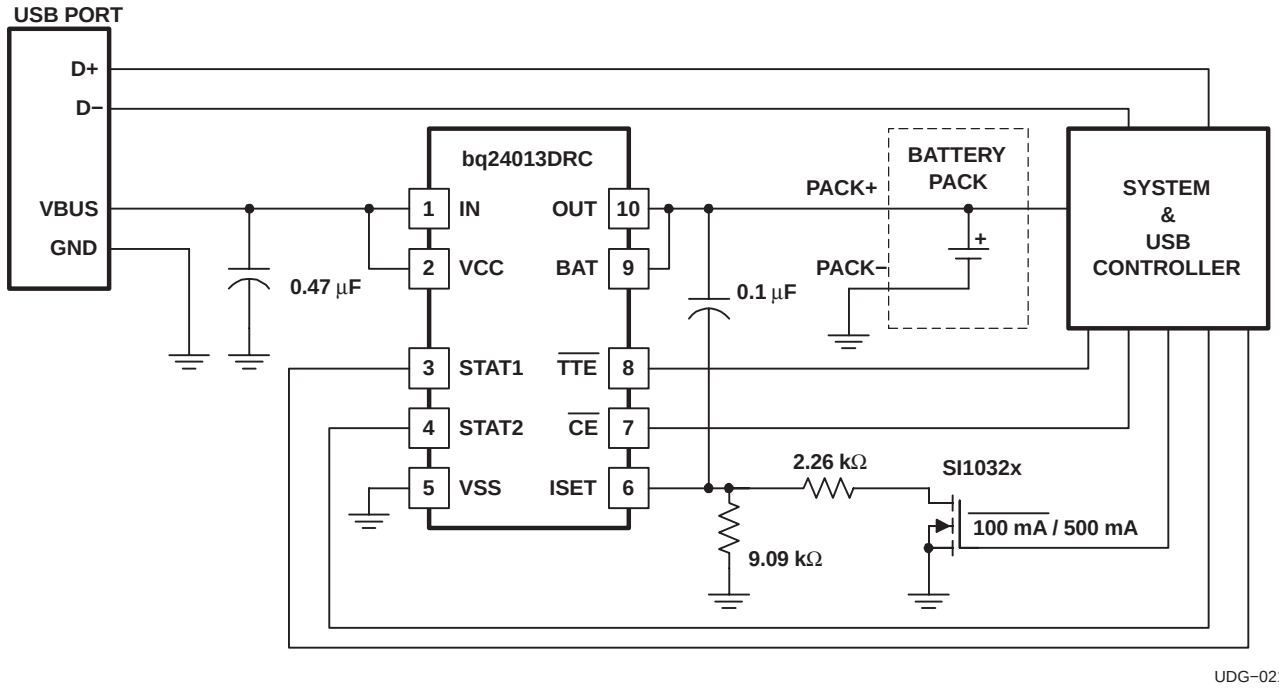


Figure 4. USB Charger Circuit

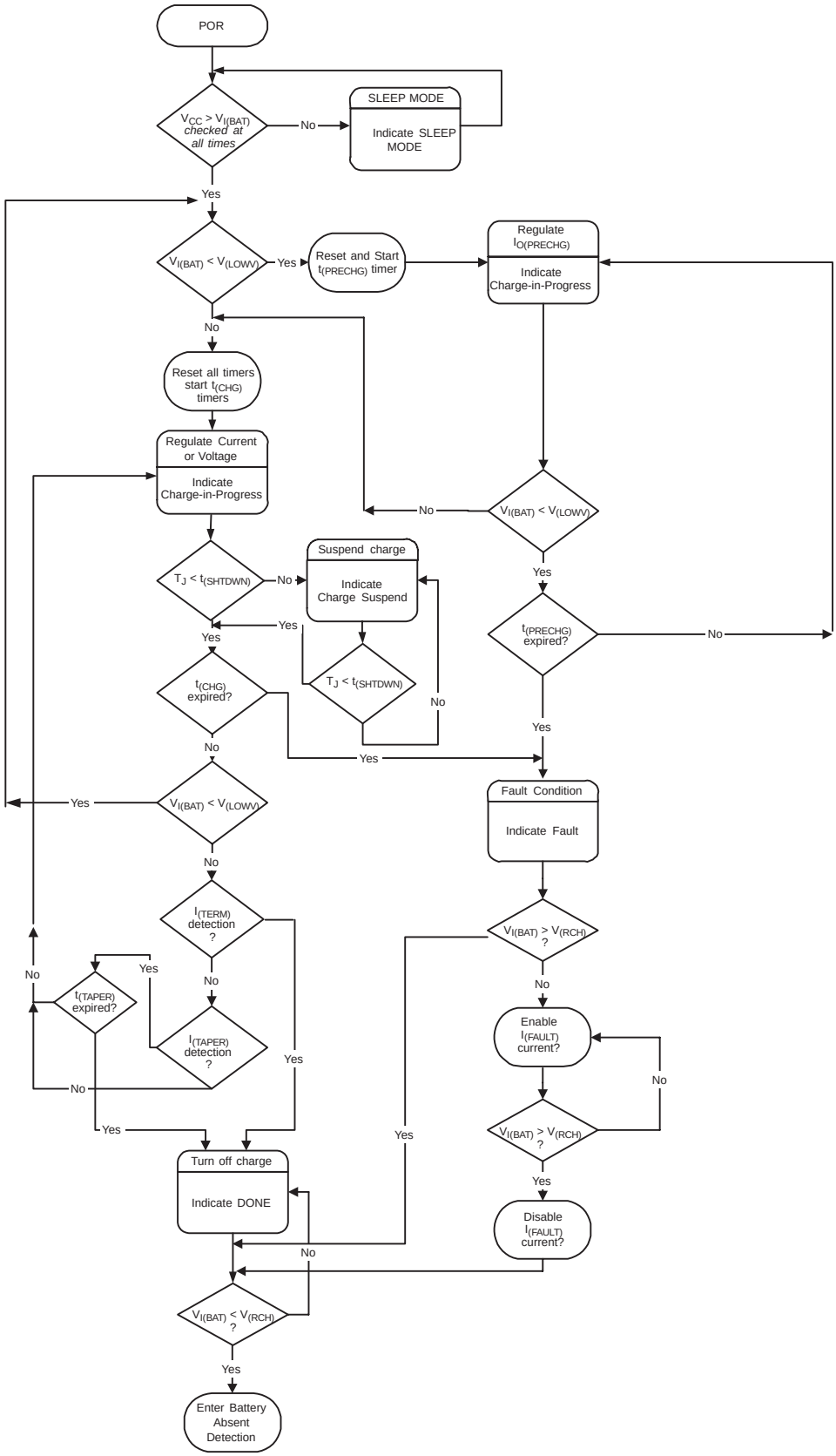


Figure 5. Operational Flow Chart

FUNCTIONAL DESCRIPTION

TEMPERATURE QUALIFICATION

NOTE: The temperature qualifications apply only to versions with temperature sense input (TS) pin option (bq24010 and bq24014).

Versions of the bqTINY with the TS pin option, continuously monitor battery temperature by measuring the voltage between the TS and VSS pins. A negative temperature coefficient thermistor (NTC) and an external voltage divider typically develops this voltage (see Figure 3). The bqTINY compare this voltage against the internal $V_{(TS1)}$ and $V_{(TS2)}$ thresholds to determine if charging is allowed (see Figure 6). The temperature sensing circuit is immune to any fluctuation in V_{CC} since both the external voltage divider and the internal thresholds are ratiometric to V_{CC}.

Once a temperature outside the $V_{(TS1)}$ and $V_{(TS2)}$ thresholds is detected the bqTINY immediately suspend the charge. The bqTINY suspends charge by turning off the powerFET and holding the timer value (i.e. timers are NOT reset). Charge is resumed when the temperature returns to the normal range.

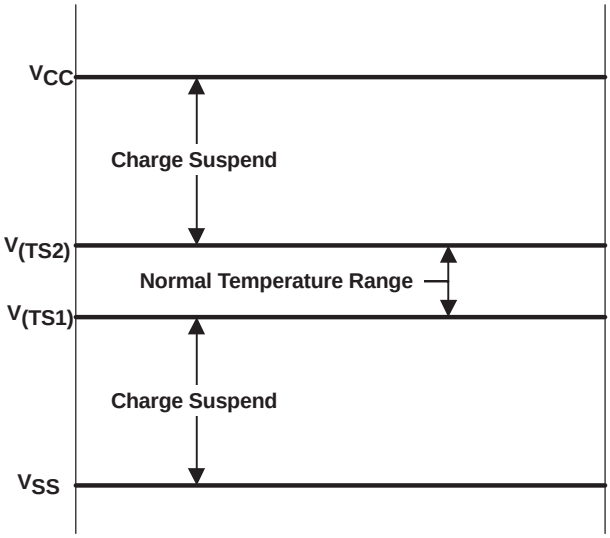


Figure 6. TS Pin Thresholds

The resistor values of R_{T1} and R_{T2} are calculated by equations (1) and (2) (for NTC Thermistors)

$$R_{T1} = \frac{\left(5 \times R_{TH} \times R_{TC}\right)}{\left(3 \times \left(R_{TC} - R_{TH}\right)\right)} \quad (1)$$

$$R_{T2} = \frac{\left(5 \times R_{TH} \times R_{TC}\right)}{\left(2 \times R_{TC}\right) - \left(7 \times R_{TH}\right)} \quad (2)$$

Where R_{TC} is the cold temperature resistance and R_{TH} is the hot temperature resistance of thermistor, as specified by the thermistor manufacturer.

R_{T1} or R_{T2} can be omitted If only one temperature (hot or cold) setting is required. Applying a constant voltage between the V_{TS1} and V_{TS2} thresholds to pin TS disables the temperature-sensing feature.

FUNCTIONAL DESCRIPTION

BATTERY PRE-CONDITIONING

During a charge cycle if the battery voltage is below the $V_{(LOWV)}$ threshold, the bqTINY applies a precharge current, $I_{O(PRECHG)}$, to the battery. This feature revives deeply discharged cells. The resistor connected between the ISET and V_{SS}, R_{SET}, determines the precharge rate. The $V_{(PRECHG)}$ and $K_{(SET)}$ parameters are specified in the specifications table.

$$I_{O\ (PRECHG)} = \frac{V_{(PRECHG)} \times K_{(SET)}}{R_{SET}} \quad (3)$$

The bqTINY activates a safety timer, $t_{(PRECHG)}$, during the conditioning phase. If $V_{(LOWV)}$ threshold is not reached within the timer period, the bqTINY turns off the charger and enunciates FAULT on the STAT1 and STAT2 pins. Refer to *Timer Fault Recovery* section for additional details.

BATTERY CHARGE CURRENT

The bqTINY offers on-chip current regulation with programmable set point. The resistor connected between the ISET and V_{SS}, R_{SET}, determines the charge rate. The $V_{(SET)}$ and $K_{(SET)}$ parameters are specified in the specifications table.

$$I_{O\ (OUT)} = \frac{V_{(SET)} \times K_{(SET)}}{R_{SET}} \quad (4)$$

BATTERY VOLTAGE REGULATION

Voltage regulation feedback is accomplished through the BAT pin. This input is tied directly and close to the positive side of the battery pack. The bqTINY monitors the battery-pack voltage between the BAT and VSS pins. When the battery voltage rises to $V_{O(REG)}$ threshold, the voltage regulation phase begins and the charging current begins to taper down.

As a safety backup, the bqTINY also monitors the charge time in the charge mode. If termination does not occur within this time period, $t_{(CHG)}$, the bqTINY turns off the charger and enunciates FAULT on the STAT1 and STAT1 pins. Refer to the *Timer Fault Recovery* section for additional details.

CHARGE TAPER DETECTION, TERMINATION AND RECHARGE

The bqTINY monitors the charging current during the voltage regulation phase. Once the taper threshold, $I_{(TAPER)}$, is detected the bqTINY initiates the taper timer, $t_{(TAPER)}$. Charge is terminated after the timer expires. The resistor connected between the ISET and V_{SS}, R_{SET}, determines the taper detection level. The $V_{(TAPER)}$ and $K_{(SET)}$ parameters are specified in the specifications table.

$$I_{(TAPER)} = \frac{V_{(TAPER)} \times K_{(SET)}}{R_{SET}} \quad (5)$$

The bqTINY resets the taper timer in the event that the charge current returns above the taper threshold, $I_{(TAPER)}$.

In addition to the taper current detection, the bqTINY terminates charge in the event that the charge current falls below the $I_{(TERM)}$ threshold. This feature allows for quick recognition of a battery removal condition or insertion of a fully charged battery. Note that taper timer is not used for $I_{(TERM)}$ detection. The resistor connected between the ISET and V_{SS}, R_{SET}, determines the taper detection level. The $V_{(TERM)}$ and $K_{(SET)}$ parameters are specified in the specifications table.

$$I_{(TERM)} = \frac{V_{(TERM)} \times K_{(SET)}}{R_{SET}} \quad (6)$$

FUNCTIONAL DESCRIPTION

After charge termination, the bqTINY restarts the charge once the voltage on the BAT pin falls below the $V_{(RCH)}$ threshold. This feature keeps the battery at full capacity at all times. Please see *Battery Absent Detection* section for additional details.

SLEEP MODE

The bqTINY enters the low-power sleep mode if the V_{CC} is removed from the circuit. This feature prevents draining the battery during the absence of V_{CC}.

CHARGE STATUS OUTPUTS

The open-collector STAT1 and STAT2 outputs indicate various charger operations as shown in the following table. These status pins can be used to drive LEDs or communicate to the host processor. Note that OFF indicates the open-collector transistor is turned off.

Table 1. Status Pins Summary

CHARGE STATE	STAT1	STAT2
Battery absent	OFF(†)	OFF
Charge-in-progress	ON	OFF
Charge done	OFF	ON
Charge suspend (temperature)	OFF	OFF
Timer fault	OFF	OFF
Sleep mode	OFF	OFF

(†) OFF means the open-collector output transistor on the STAT1 or STAT2 pins is in an off state.

$\overline{PG}$ OUTPUT

The open-drain $\overline{PG}$ (power good) indicates when the ac adapter (i.e. V_{CC}) is present. The output turns ON when a valid V_{CC} is detected. This output is turned off in the sleep mode. The $\overline{PG}$ pin can be used to drive an LED or communicate to the host processor.

$\overline{CE}$ INPUT (CHARGE ENABLE)

The $\overline{CE}$ digital input is used to disable or enable the charge process. A low-level signal on this pin enables the charge and a high-level signal disables the charge. A high-to-low transition on this pin also resets all timers and fault conditions and starts a new charge cycle.

$\overline{TTE}$ INPUT (TIMER AND TERMINATION ENABLE)

The $\overline{TTE}$ digital input is used to disable or enable the fast-charge timer and charge termination. A low-level signal on this pin enables the fast-charge timer and termination and a high-level signal disables this feature. A high-to-low transition on this pin also resets all timers.

THERMAL SHUTDOWN AND PROTECTION

The bqTINY monitors the junction temperature, T_J, of the die and suspends charging if T_J exceeds 155°C. Charging resumes when T_J falls below approximately 130°C.

FUNCTIONAL DESCRIPTION

BATTERY ABSENT DETECTION

For applications with removable battery packs, bqTINY provides a battery absent detection scheme to reliably detect insertion and/or removal of battery packs.

The voltage at the BAT pin is held above the battery recharge threshold, $V_{(RCH)}$, by the charged battery following fast charging. When the voltage at the BAT pin falls to the recharge threshold, either by a load on the battery or due to battery removal, the bqTINY begins a battery absent detection test. This test involves enabling a detection current, $I_{(DETECT)}$, for a period of $t_{(DETECT)}$ and checking to see if the battery voltage is below the pre-charge threshold, $V_{(LOWV)}$. Following this, the precharge current, $I_{O(PRECHG)}$ is applied for a period of $t_{(DETECT)}$ and the battery voltage checked again to be above the recharge threshold. The purpose is to attempt to *close* a battery pack with an open protector, if one is connected to the bqTINY. Passing both of the discharge and charging tests indicates a battery absent fault at the STAT pins. Failure of either test starts a new charge cycle. For the absent battery condition the voltage on the BAT pin rises and falls between the $V_{(LOWV)}$ and $V_{O(REG)}$ thresholds indefinitely. See Figure 7.

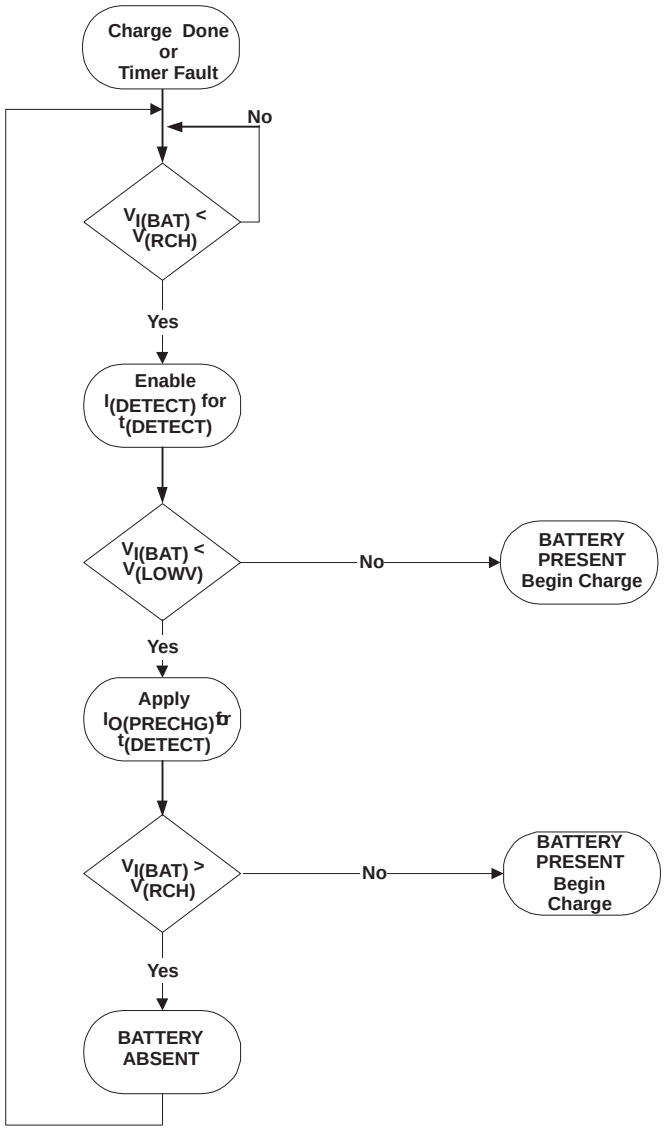


Figure 7. Battery Absent Detection

FUNCTIONAL DESCRIPTION

TIMER FAULT RECOVERY

As shown in Figure 5, bqTINY provides a recovery method to deal with timer fault conditions. The following conditions summarize this method.

Condition #1: Charge voltage above recharge threshold ($V_{(RCH)}$) and timeout fault occurs

Recovery method: bqTINY waits for the battery voltage to fall below the recharge threshold. This could happen as a result of a load on the battery, self-discharge or battery removal. Once the battery falls below the recharge threshold, the bqTINY clears the fault and enters the battery absent detection routine. A POR or $\overline{CE}$ toggle also clears the fault.

Condition #2: Charge voltage below recharge threshold ($V_{(RCH)}$) and timeout fault occurs

Recovery method: Under this scenario, the bqTINY applies the $I_{(FAULT)}$ current. This small current is used to detect a battery removal condition and remains on as long as the battery voltage stays below the recharge threshold. If the battery voltage goes above the recharge threshold, then the bqTINY disables the $I_{(FAULT)}$ current and executes the recovery method described for condition #1. Once the battery falls below the recharge threshold, the bqTINY clears the fault and enters the battery absent detection routine. A POR or $\overline{CE}$ toggle also clears the fault.

APPLICATION INFORMATION

SELECTING INPUT CAPACITOR

In most applications, all that is needed is a high-frequency decoupling capacitor. A 0.47-µF ceramic, placed in close proximity to V_{CC} and V_{SS} pins, works well. The bqTINY is designed to work with both regulated and unregulated external dc supplies. If a non-regulated supply is chosen, the supply unit should have enough capacitance to hold up the supply voltage to the minimum required input voltage at maximum load. If not, more capacitance has to be added to the input of the charger.

SELECTING OUTPUT CAPACITOR

The bqTINY requires only a small output capacitor for loop stability. A 0.1-µF ceramic capacitor placed between the BAT and ISET pins is typically sufficient for embedded applications (i.e. non-removable battery packs). For application with removable battery packs a 1-µF ceramic capacitor ensure proper operation of the battery detection circuitry. Note that the output capacitor can also be placed between BAT and VSS pins.

THERMAL CONSIDERATIONS

The bqTINY is packaged in a thermally enhanced MLP (also referred to as QFN) package. The package includes a thermal pad to provide an effective thermal contact between the device and the printed circuit board (PCB). Full PCB design guidelines for this package are provided in the application note entitled, *QFN/SON PCB Attachment Application Note* (TI Literature No. SLUA271).

The most common measure of package thermal performance is thermal impedance (θ_{JA}) measured (or modeled) from the device junction to the air surrounding the package surface (ambient). The mathematical expression for θ_{JA} is:

$$\theta_{JA} = \frac{T_J - T_A}{P} \quad (7)$$

Where:

- T_J = device junction temperature
- T_A = ambient temperature
- P = device power dissipation

Factors that can greatly influence the measurement and calculation of θ_{JA} include:

- whether or not the device is board mounted
- trace size, composition, thickness, and geometry
- orientation of the device (horizontal or vertical)
- volume of the ambient air surrounding the device under test and airflow
- whether other surfaces are in close proximity to the device being tested

The device power dissipation, P, is a function of the charge rate and the voltage drop across the internal PowerFET. It can be calculated from the following equation:

$$P = V_{IN} - V_{I(BAT)} \times I_{O(OUT)} \quad (8)$$

Due to the charge profile of Li-xx batteries, the maximum power dissipation is typically seen at the beginning of the charge cycle when the battery voltage is at it's lowest. See Figure 2.

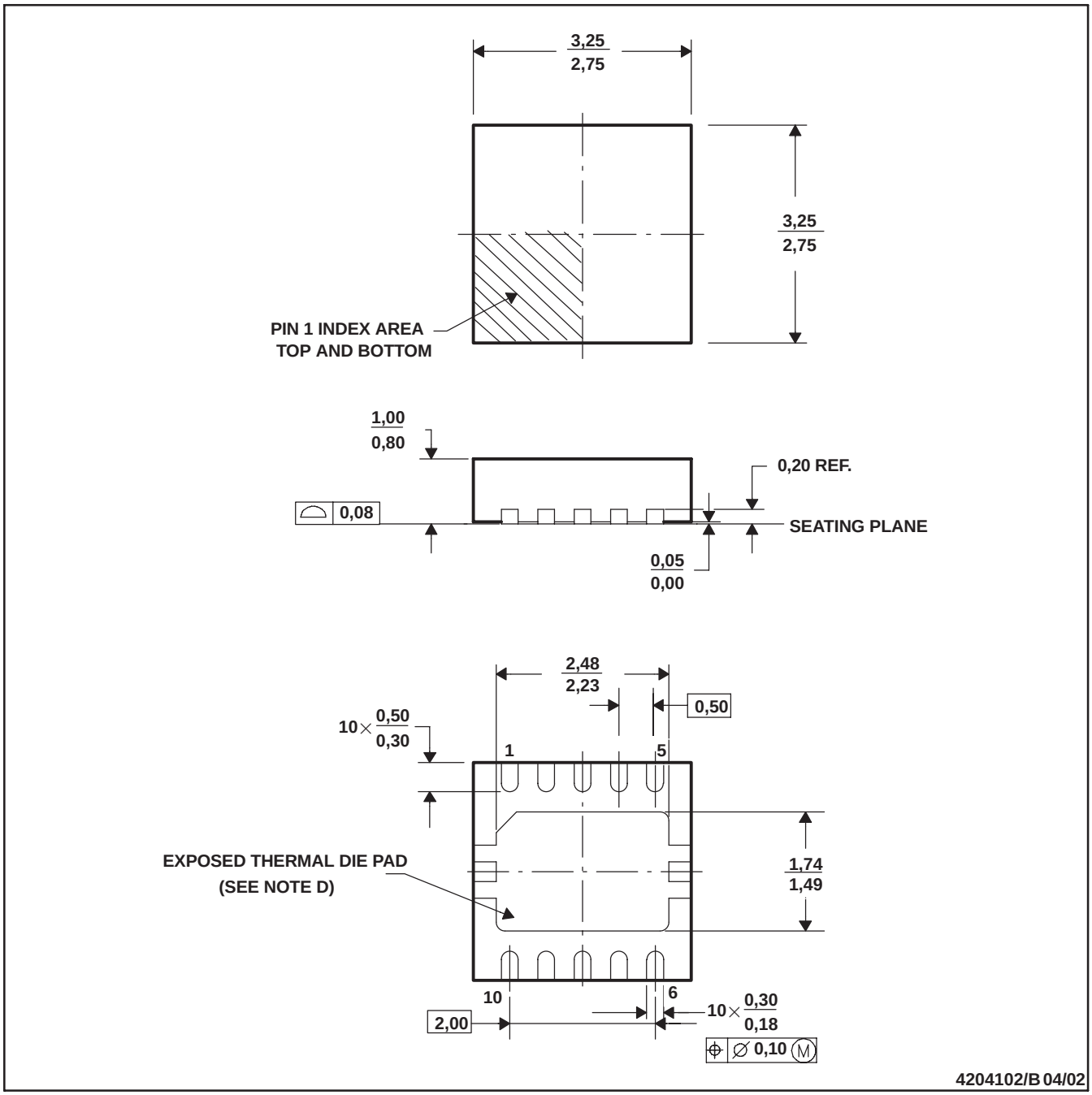
APPLICATION INFORMATION

PCB LAYOUT CONSIDERATIONS

It is important to pay special attention to the PCB layout. The following provides some guidelines:

- To obtain optimal performance, the decoupling capacitor from V_{CC} to V_{SS} and the output filter capacitors from BAT to ISET should be placed as close as possible to the bqTINY, with short trace runs to both signal and V_{SS} pins.
- All low-current V_{SS} connections should be kept separate from the high-current charge or discharge paths from the battery. Use a single-point ground technique incorporating both the small signal ground path and the power ground path.
- The BAT pin is the voltage feedback to the device and should be connected with its trace as close to the battery pack as possible.
- The high current charge paths into IN and from the OUT pins must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces.
- The bqTINY is packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the device and the printed circuit board (PCB). Full PCB design guidelines for this package are provided in the application note entitled: *QFN/SON PCB Attachment Application Note* (TI Literature No. SLUA271).
- There is an internal electrical connection between the exposed thermal pad and V_{SS} pin of the device. The exposed thermal pad must be connected to the same potential as the V_{SS} pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. V_{SS} pin must be connected to ground at all times.

DRC (S−PDSO−N10) **CUSTOM DEVICE** **PLASTIC SMALL OUTLINE**



NOTES:A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Small Outline No-Lead (SON) package configuration.
D. The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane.

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DSP	dsp.ti.com	Broadband	www.ti.com/broadband
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Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-20	0.039 @ V_{GS} = -4.5 V	-4.7
	0.052 @ V_{GS} = -2.5 V	- 4.1
	0.068 @ V_{GS} = -1.8 V	- 3.5

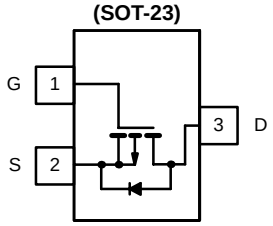
FEATURES

- TrenchFET® Power MOSFET

APPLICATIONS

- Load Switch
- PA Switch

TO-236
(SOT-23)



Top View
Si2323DS (D3)*
*Marking Code

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	5 sec	Steady State	Unit
Drain-Source Voltage		V_{DS}	-20		V
Gate-Source Voltage		V_{GS}	±8		
Continuous Drain Current (T_J = 150°C)[a, b]	T_A = 25°C	I_D	- 4.7	-3.7	A
	T_A = 70°C		-3.8	-2.9	
Pulsed Drain Current		I_{DM}	-20		
Continuous Source Current (Diode Conduction)[a, b]		I_S	-1.0	-0.6	
Maximum Power Dissipation[a, b]	T_A = 25°C	P_D	1.25	0.75	W
	T_A = 70°C		0.8	0.48	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 5 sec	R_{thJA}	75	100	°C/W
	Steady State		120	166	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	40	50	

Notes
a. Surface Mounted on 1" x 1" FR4 Board.
b. Pulse width limited by maximum junction temperature.

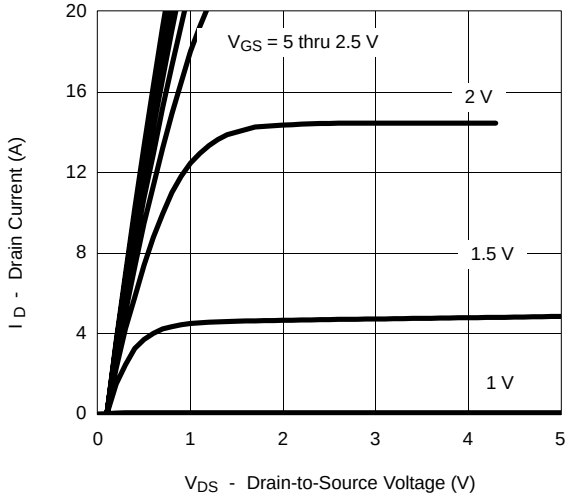
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Conditions	Limits Min	Limits Typ	Limits Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = -250 µA	-20			V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250 µA	-0.40		-1.0	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±8 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -16 V, V_{GS} = 0 V			-1	µA
		V_{DS} = -16 V, V_{GS} = 0 V, T_J = 55°C			-10	µA
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≤ -5 V, V_{GS} = -4.5 V	-20			A
Drain-Source On-Resistance[a]	$r_{DS(on)}$	V_{GS} = -4.5 V, I_D = -4.7 A		0.031	0.039	Ω
		V_{GS} = -2.5 V, I_D = -4.1 A		0.041	0.052	Ω
		V_{GS} = -1.8 V, I_D = -2.0 A		0.054	0.068	Ω
Forward Transconductance[a]	g_{fs}	V_{DS} = -5 V, I_D = -4.7 A		16		S
Diode Forward Voltage	V_{SD}	I_S = -1.0 A, V_{GS} = 0 V		0.7	-1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = -10 V, V_{GS} = -4.5 V I_D ≅ -4.7 A		12.5	19	nC
Gate-Source Charge	Q_{gs}			1.7		nC
Gate-Drain Charge	Q_{gd}			3.3		nC
Input Capacitance	C_{iss}	V_{DS} = -10 V, V_{GS} = 0, f = 1 MHz		1020		pF
Output Capacitance	C_{oss}			191		pF
Reverse Transfer Capacitance	C_{rss}			140		pF
Switching[c]						
Turn-On Time	$t_{d(on)}$	V_{DD} = -10 V, R_L = 10 Ω I_D ≅ -1.0 A, V_{GEN} = -4.5 V R_G = 6 Ω		25	40	ns
	t_r			43	65	ns
Turn-Off Time	$t_{d(off)}$			71	110	ns
	t_f			48	75	ns

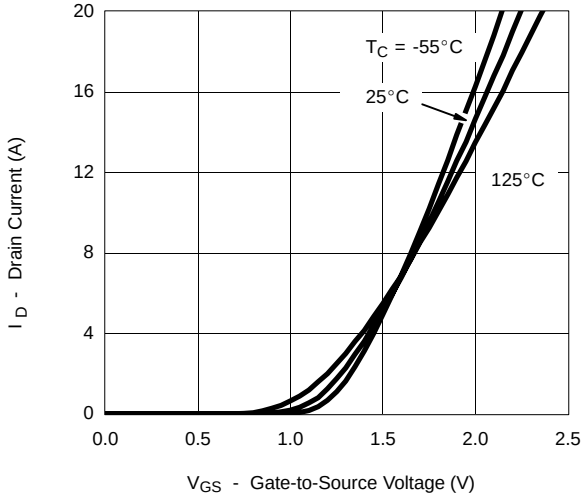
Notes
a. Pulse test: PW ≤300 µs duty cycle ≤2%.
b. For DESIGN AID ONLY, not subject to production testing.
c. Switching time is essentially independent of operating temperature.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

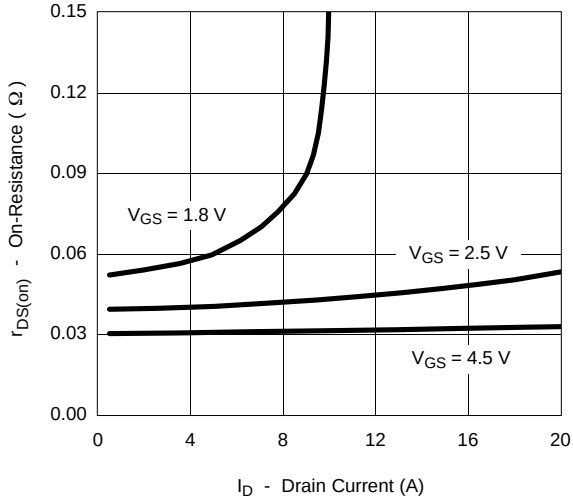
Output Characteristics



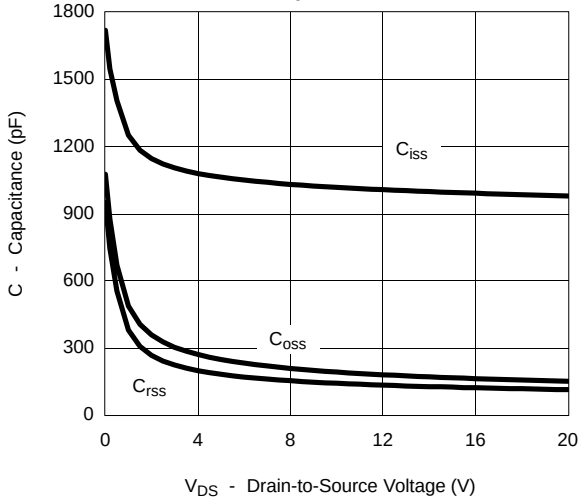
Transfer Characteristics



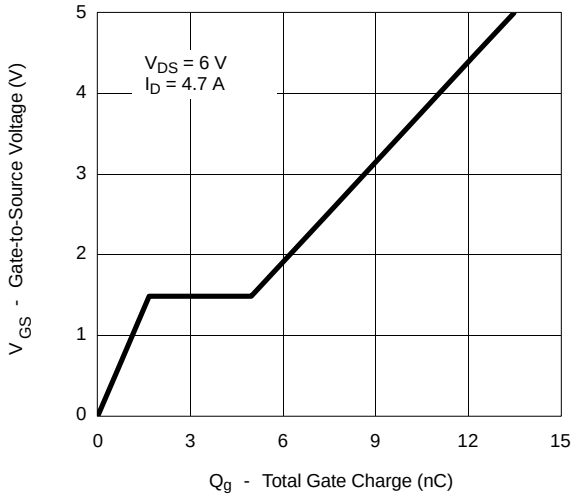
On-Resistance vs. Drain Current



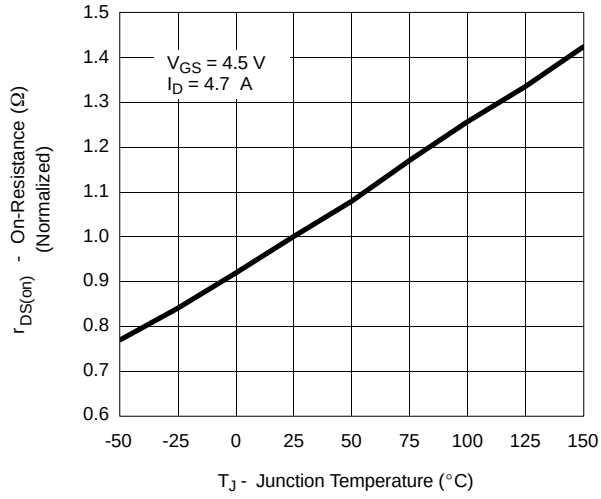
Capacitance



Gate Charge

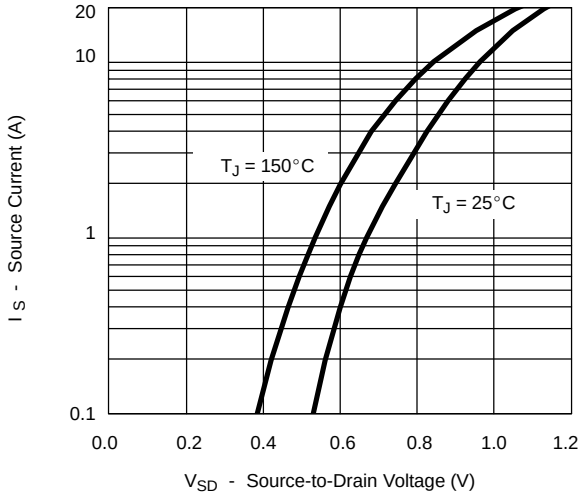


On-Resistance vs. Junction Temperature

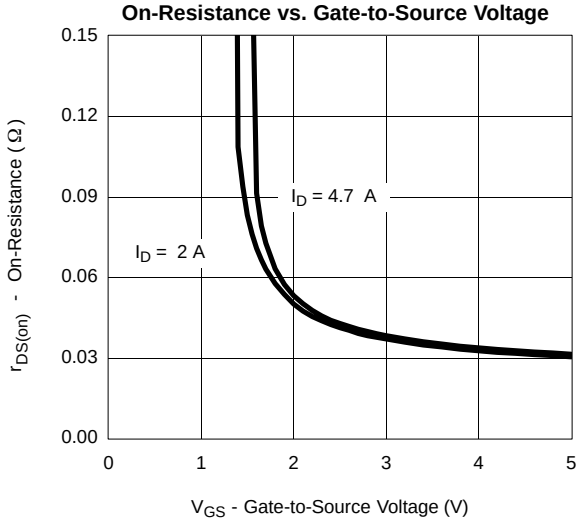


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

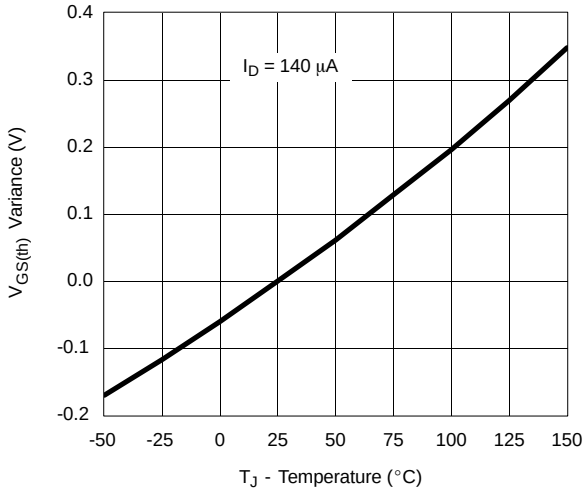
Source-Drain Diode Forward Voltage



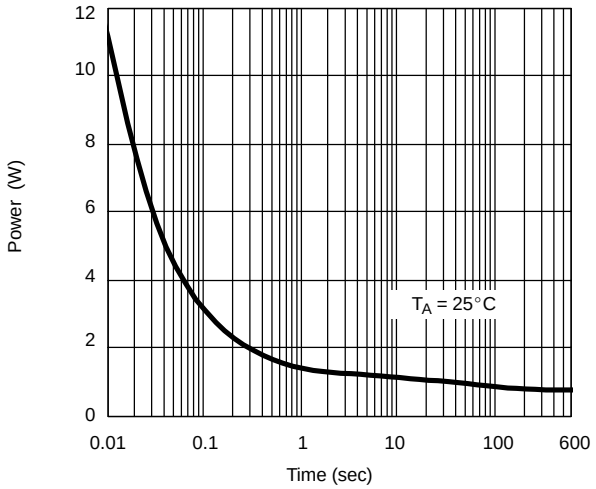
On-Resistance vs. Gate-to-Source Voltage



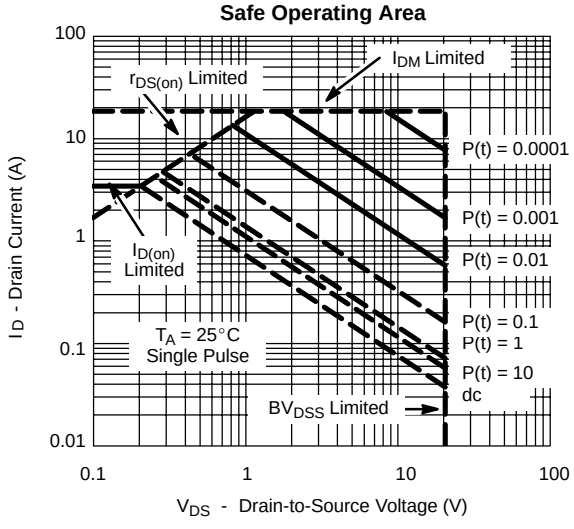
Threshold Voltage



Single Pulse Power



Safe Operating Area



DATA SHEET

TEA5768HL
Low-power FM stereo radio for handheld applications

Preliminary specification

2002 Mar 12

Philips
Semiconductors

PHILIPS

Low-power FM stereo radio for handheld applications TEA5768HL

FEATURES

- High sensitivity due to integrated low-noise RF input amplifier
- FM mixer for conversion of the US/Europe (87.5 to 108 MHz) and Japanese FM band (76 to 91MHz) to IF
- Preset tuning to receive Japanese TV audio up to 108 MHz
- RF Automatic Gain Control (AGC) circuit
- LC tuner oscillator operating with low cost fixed chip inductors
- FM IF selectivity completely done internal
- No external discriminator needed due to fully integrated FM demodulator
- Crystal reference frequency oscillator; the oscillator operates with a 32.768 kHz clock crystal or with a 13 MHz crystal and with an externally applied 6.5 MHz reference frequency
- PLL synthesizer tuning system
- 7-bit IF counter output via bus
- 4-bit level information output via bus
- Soft mute
- Signal dependent mono/stereo blend [Stereo Noise Cancelling (SNC)]
- Signal dependent High Cut Control (HCC)
- Soft mute, SNC and HCC can be switched off via bus
- Adjustment-free stereo decoder
- I^2C-bus
- Autonomous search tuning function
- Standby mode
- Two software programmable ports
- Bus enable line to switch bus input and output lines into 3-state mode
- Automotive temperature range (at V_{CCA}, $V_{CC(VCO)}$ and V_{CCD} = 5 V).

GENERAL DESCRIPTION

The TEA5768HL is a single-chip electronically tuned FM stereo radio for low-voltage application with fully integrated IF selectivity and demodulation. The radio is completely adjustment-free and does only require a minimum of small and low cost external components. The radio can tune the European, US and Japan FM bands.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA5768HL	LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1

QUICK REFERENCE DATA

$V_{CCA} = V_{CC(VCO)} = V_{CCD}$.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		2.5	3.0	5.0	V
$V_{CC(VCO)}$	voltage controlled oscillator supply voltage		2.5	3.0	5.0	V
V_{CCD}	digital supply voltage		2.5	3.0	5.0	V
I_{CCA}	analog supply current	operational; V_{CCA} = 3 V	6.0	8.4	10.5	mA
		standby mode; V_{CCA} = 3 V	–	3	6	µA
$I_{CC(VCO)}$	voltage controlled oscillator supply current	operational; $V_{VCOTANK1} = V_{VCOTANK2}$ = 3 V	560	750	940	µA
		standby mode; $V_{VCOTANK1} = V_{VCOTANK2}$ = 3 V	–	1	2	µA
I_{CCD}	digital supply current	operational; V_{CCD} = 3 V	2.1	3.0	3.9	mA
		standby mode; V_{CCD} = 3 V				
		bus enable line HIGH	30	56	80	µA
		bus enable line LOW	11	19	26	µA
$f_{FM(ant)}$	FM input frequency		76	–	108	MHz
T_{amb}	ambient temperature	$V_{CCA} = V_{CC(VCO)} = V_{CCD}$ = 2.5 V	–10	–	+75	°C
		$V_{CCA} = V_{CC(VCO)} = V_{CCD}$ = 5 V	–40	–	+85	°C
FM overall system parameters; see Fig.5						
V_{RF}	RF sensitivity input voltage	f_{RF} = 76 to 108 MHz; Δf = 22.5 kHz; f_{mod} = 1 kHz; (S+N)/N = 26 dB; de-emphasis = 75 µs; L = R; BAF = 300 Hz to 15 kHz	–	2	3.5	µV
S_{-200}	LOW side 200 kHz selectivity	Δf = –200 kHz; f_{RF} = 76 to 108 MHz; note 1	32	36	–	dB
S_{+200}	HIGH side 200 kHz selectivity	Δf = +200 kHz; f_{RF} = 76 to 108 MHz; note 1	39	43	–	dB
V_{AFL}; V_{AFR}	left and right audio frequency output voltage	V_{RF} = 1 mV; L = R; Δf = 22.5 kHz; f_{mod} = 1 kHz; de-emphasis = 75 µs	60	75	90	mV
(S+N)/N	maximum signal plus noise-to-noise ratio	V_{RF} = 1 mV; L = R; Δf = 22.5 kHz; f_{mod} = 1 kHz; de-emphasis = 75 µs; BAF = 300 Hz to 15 kHz	54	60	–	dB
$\alpha_{cs(stereo)}$	stereo channel separation	V_{RF} = 1 mV; R = L = 0 or R = 0 and L = 1 including 9% pilot; Δf = 75 kHz; f_{mod} = 1 kHz; data byte 3: bit 3 = 0; data byte 4: bit 1 = 1	24	30	–	dB
THD	total harmonic distortion	V_{RF} = 1 mV; L = R; Δf = 75 kHz; f_{mod} = 1 kHz; de-emphasis = 75 µs	–	0.4	1	%

Note

1. LOW side and HIGH side selectivity can be switched by changing the mixer from HIGH side to LOW side LO injection.

BLOCK DIAGRAM

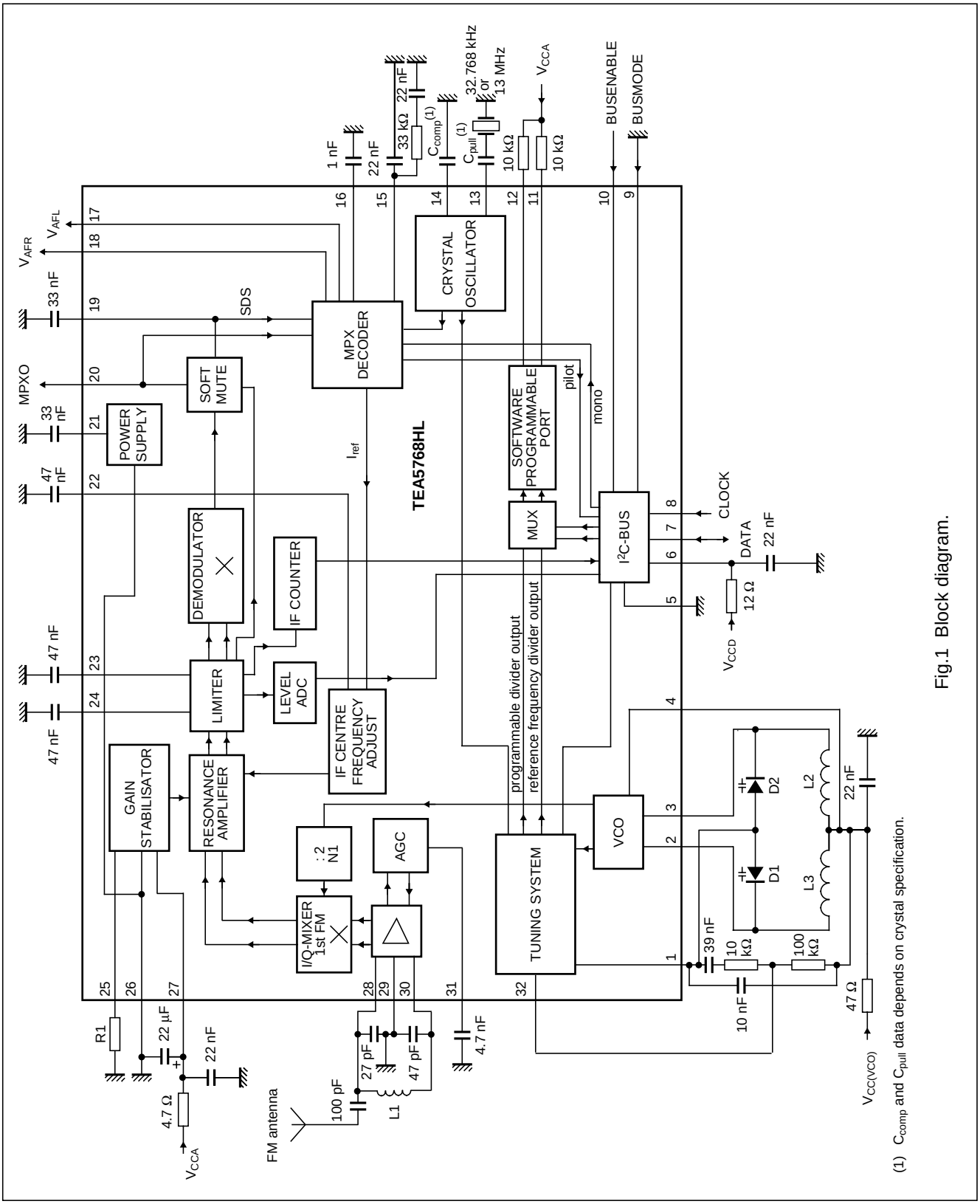


Fig.1 Block diagram.

(1) C_{comp} and C_{pull} data depends on crystal specification.

Table 1 Component list for Figs 1 and 5

COMPONENT	PARAMETER	VALUE	TOLERANCE	TYPE	MANUFACTURER
R1	resistor with low temperature coefficient	18 kΩ	±1%	RC12G	Philips
D1 and D2	varicap for VCO tuning	–	–	BB202	Philips
L1	RF band filter coil	120 nH	±2%	Q_{min} = 40	
L2 and L3	VCO coil	33 nH	±2%	Q_{min} = 40	
XTAL13	13 MHz crystal	–	–	NX4025GA	
C_{pull}	pulling capacitor for NX4025GA	10 pF	–		
XTAL32.768	32.768 kHz crystal	–	–		

PINNING

SYMBOL	PIN	DESCRIPTION
CPOUT	1	charge pump output of synthesizer PLL
VCOTANK1	2	voltage controlled oscillator tuned circuit output 1
VCOTANK2	3	voltage controlled oscillator tuned circuit output 2
$V_{CC(VCO)}$	4	voltage controlled oscillator supply voltage
DGND	5	digital ground
V_{CCD}	6	digital supply voltage
DATA	7	bus data line input/output
CLOCK	8	bus-clock line input
BUSMODE	9	bus mode select input
BUSENABLE	10	bus enable input
SWPORT1	11	software programmable port 1
SWPORT2	12	software programmable port 2
XTAL1	13	crystal oscillator input 1
XTAL2	14	crystal oscillator input 2
PHASEFIL	15	phase detector loop filter
PILFIL	16	pilot detector low-pass filter
V_{AFL}	17	left audio frequency output voltage
V_{AFR}	18	right audio frequency output voltage
TMUTE	19	time constant for soft mute
MPXO	20	FM demodulator MPX signal output
V_{ref}	21	reference voltage
TIFC	22	time constant for IF centre adjust
LIMDEC1	23	decoupling IF limiter 1
LIMDEC2	24	decoupling IF limiter 2
I_{gain}	25	gain control current for IF filter
AGND	26	analog ground
V_{CCA}	27	analog supply voltage
RFI1	28	RF input 1
RFGND	29	RF ground

SYMBOL	PIN	DESCRIPTION
RFI2	30	RF input 2
TAGC	31	time constant RF AGC
LOOPSW	32	switch output of synthesizer PLL loop filter

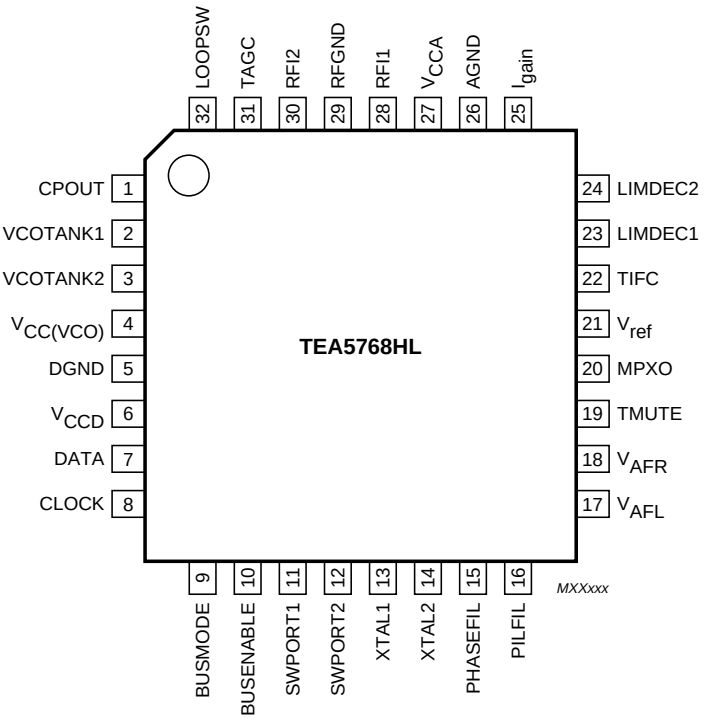


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Low-noise RF amplifier

The LNA input impedance together with the LC RF input circuit defines an FM band filter. The gain of the LNA is controlled by the RF AGC circuit.

FM mixer

FM quadrature mixer converts FM RF (76 to 108 MHz) to an IF of 225 kHz.

VCO

The varactor tuned LC VCO provides the Local Oscillator (LO) signal for the FM quadrature mixer. The VCO frequency range is 150 to 217 MHz.

Crystal oscillator

The crystal oscillator can operate with a 32.768 kHz clock crystal or a 13 MHz crystal. The temperature drift of standard 32.768 kHz clock crystals limits the operational temperature range from –10 to +60 °C.

Via pin XTAL2 the PLL synthesizer can be clocked externally with a 32.768 kHz, a 6.5 MHz or a 13 MHz signal.

The crystal oscillator generates the reference frequency for

- The reference frequency divider for synthesizer PLL
- The timing for the IF counter
- The free-running frequency adjust of the stereo decoder VCO
- The centre frequency adjust of the IF filters.

PLL tuning system

The PLL synthesizer tuning system is suitable to operate with a 32.768 kHz or a 13 MHz reference frequency generated by the crystal oscillator or fed into the IC. The synthesizer can also be clocked via pin XTAL2 with 6.5 MHz. The PLL tuning system can perform an autonomous search tuning function.

RF AGC

The RF AGC prevents overloading and limits the amount of intermodulation products created by strong adjacent channels.

IF filter

Fully integrated IF filter.

FM demodulator

The FM quadrature demodulator has an integrated resonator to perform the phase shift of the IF signal.

Level voltage generator and analog-to-digital converter

The level voltage is analog-to-digital converted with 4 bits and output via the bus.

IF counter

The IF counter outputs a 7-bit count result via the bus.

Soft mute

The low-pass filtered level voltage drives the soft mute attenuator at low RF input levels. The soft mute function can also be switched off via bus.

MPX decoder

The PLL stereo decoder is adjustment-free. The stereo decoder can be switched to mono via bus.

Signal dependent mono/stereo blend

With decreasing RF input level the MPX decoder blends from stereo to mono to limit the output noise. The continuous mono-to-stereo blend can also be programmed by bus to an RF level depending switched mono-to-stereo transition. Stereo Noise Cancelling (SNC) can be switched off via bus.

Signal dependent AF response

With decreasing RF input level the audio bandwidth is reduced. The function can also be switched off via bus.

Software programmable ports

Two software programmable ports (open-collector) can be addressed via bus.

With write data byte 4 bit 0 the port 1 (pin SWPORT1) function can be changed (see Table 14). Pin SWPORT1 is then output for the ready flag of read byte 1.

I²C-BUS AND BUS CONTROLLED FUNCTIONS

I²C-bus specification

Information about the I²C-bus can be found in the brochure *"The I²C-bus and how to use it"* (order number 9398 393 40011).

The standard I²C-bus specification is expanded by the following definitions.

IC address C0: 1100000.

Structure of the I²C-bus logic: slave transceiver.

Subaddresses are not used.

The maximum LOW-level input and the minimum HIGH-level input are specified to $0.2V_{CCD}$ respectively $0.45V_{CCD}$.

The pin BUSMODE must be connected to ground.

Hint: The bus operates at a maximum clock frequency of 400 kHz. It is not allowed to connect the IC to a bus operating at a higher clock rate.

DATA TRANSFER FOR THE TEA5768HL

Data sequence: address, byte 1, byte 2, byte 3, byte 4, and byte 5. The data transfer has to be in this order. The LSB = 0 of the address indicates a WRITE operation to the TEA5768HL.

Bit 7 of each byte is considered the MSB and has to be transferred as the first bit of the byte.

The data becomes valid bitwise at the appropriate falling edge of the clock. A STOP condition after any byte can shorten transmission times.

When writing to the transceiver by using the STOP condition before completion of the whole transfer:

- The remaining bytes will contain the old information
- If the transfer of a byte is not completed, the new bits will be used, but a new tuning cycle will not be started.

With the standby bit the IC can be switched in a low current standby mode. The bus is then still active. The standby current can be reduced by deactivation of the bus interface (pin BUSENABLE LOW). Is the bus interface deactivated (pin BUSENABLE LOW) without programmed standby mode, the IC keeps its normal operation, but is isolated from the bus lines.

The software programmable output (SWPORT1) can be programmed to operate as tuning indicator output. As long as the IC has not completed a tuning action, the SWPORT1 pin is LOW. The pin becomes HIGH, when a preset or search tuning was completed or when a band limit was reached.

With the MSB in byte 5 set to logic 1 the reference frequency divider of the synthesizer PLL is changed. The tuning system can then be clocked via pin XTAL2 with 6.5 MHz.

POWER-ON RESET

The mute is set, all other bits are set to LOW. To initialize the IC all bytes have to be transferred.

I²C-bus protocol

Table 2 Write mode

S(1)	address (write)	A(2)	data byte(s)	A(2)	P(3)

Table 3 Read mode

S(1)	address (read)	A(2)	data byte 1

Notes to Tables 2 and 3

1. S = START condition.
2. A = acknowledge.
3. P = STOP condition.

Table 4 IC address byte

IC ADDRESS							MODE
1	1	0	0	0	0	0	R/$\overline{W}$(1)

Note

1. Read or write mode:
   a) 0 = write operation to TEA5768HL
   b) 1 = read operation from TEA5768HL.

Writing data

Table 5 Write mode

DATA BYTE 1	DATA BYTE 2	DATA BYTE 3	DATA BYTE 4	DATA BYTE 5

Table 6 Format of 1st data byte

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
MUTE	SM	PLL13	PLL12	PLL11	PLL10	PLL9	PLL8

Table 7 Description of 1st data byte bits

BIT	SYMBOL	DESCRIPTION
7	MUTE	If MUTE = 1, then L and R audio muted. If MUTE = 0, then audio not muted.
6	SM	**Search Mode.** If SM = 1, then search mode. If SM = 0, then no search mode.
5 to 0	PLL[13:8]	Setting of synthesizer programmable counter for search or preset.

Table 8 Format of 2nd data byte

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
PLL7	PLL6	PLL5	PLL4	PLL3	PLL2	PLL1	PLL0

Table 9 Description of 2nd data byte bits

BIT	SYMBOL	DESCRIPTION
7 to 0	PLL[7:0]	Setting of synthesizer programmable counter for search or preset.

Table 10 Format of 3rd data byte

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
SUD	SSL1	SSL0	HLSI	MS	ML	MR	SWP1

Table 11 Description of 3rd data byte bits

BIT	SYMBOL	DESCRIPTION
7	SUD	**Search up/down.** If SUD = 1, then search up. If SUD = 0, then search down.
6 and 5	SSL[1:0]	**Search Stop Level.** See Table 12.
4	HLSI	**HIGH/LOW Side Injection.** If HLSI = 1, then HIGH side LO injection. If HLSI = 0, then LOW side LO injection.
3	MS	**Mono/Stereo.** If MS = 1, then forced mono. If MS = 0, then stereo ON.
2	ML	**Mute Left.** If ML = 1, then left audio channel muted and forced mono. If ML = 0, then not muted.
1	MR	**Mute Right.** If MR = 1, then right audio channel muted and forced mono. If MR = 0, then not muted.
0	SWP1	**Software programmable port 1.** If SWP1 = 1, then port 1 is HIGH. If SWP1 = 0, then port 1 is LOW.

Table 12 Search stop level setting

SSL1	SSL0	SEARCH STOP LEVEL
0	0	not allowed in search mode
0	1	low; level ADC output = 5
1	0	mid; level ADC output = 7
1	1	high; level ADC output = 10

Table 13 Format of 4th data byte

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
SWP2	STBY	BL	XTAL	SMUTE	HCC	SNC	SI

Table 14 Description of 4th data byte bits

BIT	SYMBOL	DESCRIPTION
7	SWP2	**Software programmable port 2.** If SWP2 = 1, then port 2 is HIGH. If SWP2 = 0, then port 2 is LOW.
6	STBY	**Standby.** If STBY = 1, then standby. If STBY = 0, then no standby.
5	BL	**Band Limits.** If BL = 1, then Japan FM band. If BL = 0, then US/Europe FM band.
4	XTAL	If XTAL = 1, then f_{xtal} = 32.768 kHz. If XTAL = 0, then f_{xtal} = 13 MHz.
3	SMUTE	**Soft Mute.** If SMUTE = 1, then soft mute is ON. If SMUTE = 0, then soft mute is OFF.
2	HCC	**High Cut Control.** If HCC = 1, then high cut control is ON. If HCC = 0, then high cut control is OFF.
1	SNC	**Stereo noise cancelling.** If SNC = 1, then stereo noise cancelling is ON. If SNC = 0, then stereo noise cancelling is OFF.
0	SI	**Search indicator.** If SI = 1, then pin SWPORT1 is output for the ‘ready flag’. If SI = 0, then pin SWPORT1 is software programmable port 1.

Table 15 Format of 5th data byte

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
PLLREF	DTC	–	–	–	–	–	–

Table 16 Description of 5th data byte bits

BIT	SYMBOL	DESCRIPTION
7	PLLREF	If PLLREF = 1, then 6.5 MHz reference for PLL enabled. If PLLREF = 0, then not enabled.
6	DTC	If DTC = 1, then de-emphasis time constant is 75 μs. If DTC = 0, then de-emphasis time constant is 50 μs.
5 to 0	–	Not used; position don't care.

Reading data

Table 17 Read mode

DATA BYTE 1	DATA BYTE 2	DATA BYTE 3	DATA BYTE 4	DATA BYTE 5

Table 18 Format of 1st data byte

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
RF	BLF	PLL13	PLL12	PLL11	PLL10	PLL9	PLL8

Table 19 Description of 1st data byte bits

BIT	SYMBOL	DESCRIPTION
7	RF	**Ready Flag.** If RF = 1, then a station has been found or the band limit has been reached. If RF = 0, then no station has been found.
6	BLF	**Band Limit Flag.** If BLF = 1, then the band limit has been reached. If BLF = 0, then the band limit has not been reached.
5 to 0	PLL[13:8]	Setting of synthesizer programmable counter after search or preset.

Table 20 Format of 2nd data byte

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
PLL7	PLL6	PLL5	PLL4	PLL3	PLL2	PLL1	PLL0

Table 21 Description of 2nd data byte bits

BIT	SYMBOL	DESCRIPTION
7 to 0	PLL[7:0]	Setting of synthesizer programmable counter after search or preset.

Table 22 Format of 3rd data byte

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
STEREO	IF6	IF5	IF4	IF3	IF2	IF1	IF0

Table 23 Description of 3rd data byte bits

BIT	SYMBOL	DESCRIPTION
7	STEREO	**Stereo indication.** If STEREO = 1, then stereo reception. If STEREO = 0, then mono reception.
6 to 0	PLL[13:8]	IF counter result.

Table 24 Format of 4th data byte

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
LEV3	LEV2	LEV1	LEV0	CI3	CI2	CI1	0

Table 25 Description of 4th data byte bits

BIT	SYMBOL	DESCRIPTION
7 to 4	LEV[3:0]	Level ADC output.
3 to 1	CI[3:1]	**Chip Identification.** These bits have to be set to logic 0.
0	–	This bit is internally set to logic 0.

Table 26 Format of 5th data byte

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
0	0	0	0	0	0	0	0

Table 27 Description of 5th data byte bits

BIT	SYMBOL	DESCRIPTION
7 to 0	–	Reserved for future extensions; these bits are internally set to logic 0.

Bus timing

Table 28 Digital levels and timing

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Digital inputs					
V_{IH}	HIGH-level input voltage		$0.45V_{CCD}$	–	V
V_{IL}	LOW-level input voltage		–	$0.2V_{CCD}$	V
Digital outputs					
$I_{sink(L)}$	LOW-level sink current		500	–	µA
V_{OL}	LOW-level output voltage	I_{OL} = 500 µA	–	450	mV
Timing (I^2C-bus enabled)					
f_{clk}	clock input		–	400	kHz
t_{HIGH}	clock HIGH time		1	–	µs
t_{LOW}	clock LOW time		1	–	µs

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{VCOTANK1}$	VCO tuned circuit output voltage 1		–0.3	+8	V
$V_{VCOTANK2}$	VCO tuned circuit output voltage 2		–0.3	+8	V
V_{CCD}	digital supply voltage		–0.3	+5	V
V_{CCA}	analog supply voltage		–0.3	+8	V
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–40	+85	°C
V_{es}	electrostatic handling voltage				
	for all pins except pin DATA	note 1	–200	+200	V
		note 2	–2000	+2000	V
	for pin DATA	note 1	–150	+200	V
		note 2	–2000	+2000	V

Notes

1. Machine model (R = 0 Ω, C = 200 pF).
2. Human body model (R = 1.5 kΩ, C = 100 pF).

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	80	K/W

DC CHARACTERISTICS

$V_{CCA} = V_{VCOTANK1} = V_{VCOTANK2} = V_{CCD} = 2.7$ V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply voltage						
PIN V_{CCA}						
V_{CCA}	analog supply voltage		2.5	3.0	5.0	V
PINS VCOTANK1 AND VCOTANK2						
$V_{CC(VCO)}$	voltage controlled oscillator supply voltage		2.5	3.0	5.0	V
PIN V_{CCD}						
V_{CCD}	digital supply voltage		2.5	3.0	5.0	V
Supply current						
PIN V_{CCA}						
I_{CCA}	analog supply current	operational				
		$V_{CCA} = 3$ V	6.0	8.4	10.5	mA
		$V_{CCA} = 5$ V	6.2	8.6	10.7	mA
		standby mode				
		$V_{CCA} = 3$ V	–	3	6	µA
		$V_{CCA} = 5$ V	–	3.2	6.2	µA
PINS VCOTANK1 AND VCOTANK2						
$I_{CC(VCO)}$	voltage controlled oscillator supply current	operational				
		$V_{VCOTANK1} = V_{VCOTANK2} = 3$ V	560	750	940	µA
		$V_{VCOTANK1} = V_{VCOTANK2} = 5$ V	570	760	950	µA
		standby mode				
		$V_{VCOTANK1} = V_{VCOTANK2} = 3$ V	–	1	2	µA
		$V_{VCOTANK1} = V_{VCOTANK2} = 5$ V	–	1.2	2.2	µA
PIN V_{CCD}						
I_{CCD}	digital supply current	operational				
		$V_{CCD} = 3$ V	2.1	3.0	3.9	mA
		$V_{CCD} = 5$ V	2.25	3.15	4.05	mA
		standby mode; $V_{CCD} = 3$ V				
		bus enable line HIGH	30	56	80	µA
		bus enable line LOW	11	19	26	µA
		standby mode; $V_{CCD} = 5$ V				
		bus enable line HIGH	50	78	105	µA
		bus enable line LOW	20	33	45	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC operating points						
V_{CPOUT}	unloaded DC voltage		0.1	–	$V_{CC(VCO)}$ – 0.1	V
V_{XTAL1}		data byte 4: bit 4 = 1	1.64	1.72	1.8	V
		data byte 4: bit 4 = 0	1.68	1.75	1.82	V
V_{XTAL2}		data byte 4: bit 4 = 1	1.64	1.72	1.8	V
		data byte 4: bit 4 = 0	1.68	1.75	1.82	V
$V_{PHASEFIL}$			0.4	1.2	V_{CCA} – 0.4	V
V_{PILFIL}			0.65	0.9	1.3	V
V_{VAFL}		f_{RF} = 98 MHz; V_{RF} = 1 mV	720	850	940	mV
V_{VAFR}		f_{RF} = 98 MHz; V_{RF} = 1 mV	720	850	940	mV
V_{TMUTE}		V_{RF} = 0 V	1.5	1.65	1.8	V
V_{MPXO}		f_{RF} = 98 MHz; V_{RF} = 1 mV	680	815	950	mV
V_{Vref}			1.45	1.55	1.65	V
V_{TIFC}			1.34	1.44	1.54	V
$V_{LIMDEC1}$			1.86	1.98	2.1	V
$V_{LIMDEC2}$			1.86	1.98	2.1	V
V_{Igain}			480	530	580	mV
V_{RFI1}			0.93	1.03	1.13	V
V_{RFI2}			0.93	1.03	1.13	V
V_{TAGC}		V_{RF} = 0 V	1	1.57	2	V

AC CHARACTERISTICS

$V_{CCA} = V_{VCOTANK1} = V_{VCOTANK2} = V_{CCD} = 2.7$ V; $T_{amb} = 25$ °C; see Fig.5; all AC values are given in RMS; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Voltage controlled oscillator						
f_{osc}	oscillator frequency		150	–	217	MHz
Crystal oscillator						
CIRCUIT INPUT: PIN XTAL2						
$V_{i(osc)}$	oscillator input voltage	oscillator externally clocked	140	–	350	mV
R_i	input resistance	oscillator externally clocked				
		with 13 MHz	2	3	4	kΩ
		with 32.768 kHz	230	330	430	kΩ
C_i	input capacitance	oscillator externally clocked				
		with 13 MHz	3.9	5.6	7.3	pF
		with 32.768 kHz	5	6	7	pF
CRYSTAL: 32.768 kHz						
f_r	series resonance frequency	data byte 4: bit 4 = 1	–	32.768	–	kHz
$\Delta f/f_r$	frequency deviation		-20×10^{-6}	–	$+20 \times 10^{-6}$	
C_0	shunt capacitance		–	–	3.5	pF
R_S	series resistance		–	–	80	kΩ
$\Delta f_r/f_{r(25\ °C)}$	temperature drift	–10 °C < T_{amb} < +60 °C	-50×10^{-6}	–	$+50 \times 10^{-6}$	
CRYSTAL: 13 MHz						
f_r	series resonance frequency	data byte 4: bit 4 = 0	–	13	–	MHz
$\Delta f/f_r$	frequency deviation		-30×10^{-6}	–	$+30 \times 10^{-6}$	
C_0	shunt capacitance		–	–	4.5	pF
C_{mot}	motional capacitance		1.5	–	3.0	fF
R_S	series resistance		–	–	100	Ω
$\Delta f_r/f_{r(25\ °C)}$	temperature drift	–40 °C < T_{amb} < +85 °C	-30×10^{-6}	–	$+30 \times 10^{-6}$	
Synthesizer						
PROGRAMMABLE DIVIDER						
N_{prog}	programmable divider ratio	data byte 1 = XX111111; data byte 2 = 11111111	–	–	8191	
		data byte 1 = XX001000; data byte 2 = 00000000	2048	–	–	
ΔN_{step}	programmable divider step size		–	1	–	
REFERENCE FREQUENCY DIVIDER						
N_{ref}	crystal oscillator divider ratio	data byte 4: bit 4 = 0	–	260	–	
		data byte 5: bit 7 = 1; data byte 4: bit 4 = 0	–	130	–	
		data byte 4: bit 4 = 1	–	1	–	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CHARGE PUMP: PIN CPOUT						
I_{sink}	charge pump peak sink current	0.2 V < V_{CPOUT} < $V_{VCOTANK2}$ − 0.2 V; $f_{VCO} > f_{ref} \times N_{prog}$	–	0.5	–	μA
I_{source}	charge pump peak source current	0.2 V < V_{CPOUT} < $V_{VCOTANK2}$ − 0.2 V; $f_{VCO} < f_{ref} \times N_{prog}$	–	–0.5	–	μA
IF counter						
V_{RF}	RF input voltage for correct IF count		–	12	18	μV
N_{IF}	IF counter length		–	7	–	bit
$N_{precount}$	IF counter prescaler ratio		–	64	–	
$T_{count(IF)}$	IF counter period	f_{xtal} = 32.768 kHz	–	15.625	–	ms
		f_{xtal} = 13 MHz	–	15.754	–	ms
$RES_{count(IF)}$	IF counter resolution	f_{xtal} = 32.768 kHz	–	4.096	–	kHz
		f_{xtal} = 13 MHz	–	4.0625	–	kHz
IF_{count}	IF counter result for search tuning stop	f_{xtal} = 32.768 kHz	31	–	3E	HEX
		f_{xtal} = 13 MHz	32	–	3D	HEX
Pins DATA, CLOCK, BUSMODE and BUSENABLE						
R_i	input resistance		10	–	–	MΩ
Software programmable ports						
PIN SWPORT1						
$I_{sink(max)}$	maximum sink current	data byte 4: bit 0 = 0; data byte 5: bit 0 = 0; $V_{SWPORT1}$ < 0.5 V	500	–	–	μA
$I_{leak(max)}$	maximum leakage current	data byte 4: bit 0 = 1; $V_{SWPORT1}$ < 5 V	–1	–	+1	μA
PIN SWPORT2						
$I_{sink(max)}$	maximum sink current	data byte 5: bit 7 = 0; $V_{SWPORT1}$ < 0.5 V	500	–	–	μA
$I_{leak(max)}$	maximum leakage current	data byte 5: bit 1 = 1; $V_{SWPORT1}$ < 5 V	–1	–	+1	μA
FM signal channel						
FM RF INPUT						
R_i	input resistance (pins RFIN1 and RFIN2 to RFGND)		75	100	125	Ω
C_i	input capacitance (pins RFIN1 and RFIN2 to RFGND)		2.5	4	6	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{RF}	RF sensitivity input voltage	f_{RF} = 76 to 108 MHz; Δf = 22.5 kHz; f_{mod} = 1 kHz; (S+N)/N = 26 dB; de-emphasis = 75 μs; BAF = 300 Hz to 15 kHz	–	2	3.5	μV
$IP3_{in}$	in-band 3rd-order intercept point related to $V_{RFIN1-RFIN2}$ (peak value)	Δf_1 = 200 kHz; Δf_2 = 400 kHz; f_{tuned} = 76 to 108 MHz	81	84	–	dBμV
$IP3_{out}$	out-band 3rd-order intercept point related to $V_{RFIN1-RFIN2}$ (peak value)	Δf_1 = 4 MHz; Δf_2 = 8 Hz; f_{tuned} = 76 to 108 MHz	82	85	–	dBμV
RF AGC						
V_{RF1}	RF input voltage for start of AGC	f_{RF1} = 93 MHz; f_{RF2} = 98 MHz; V_{RF2} = 50 dBμV; $\left\|\frac{\Delta V_{TMUTE}}{V_{RF1}}\right\| < \frac{14\ mV}{3\ dB\mu V}$; note 1	66	72	78	dBμV
IF filter						
f_{IF}	IF filter centre frequency		215	225	235	kHz
B_{IF}	IF filter bandwidth		85	94	102	kHz
S_{+200}	HIGH side 200 kHz selectivity	Δf = +200 kHz; f_{tuned} = 76 to 108 MHz; note 2	39	43	–	dB
S_{-200}	LOW side 200 kHz selectivity	Δf = –200 kHz; f_{tuned} = 76 to 108 MHz; note 2	32	36	–	dB
S_{+100}	HIGH side 100 kHz selectivity	Δf = +100 kHz; f_{tuned} = 76 to 108 MHz; note 2	8	12	–	dB
S_{-100}	LOW side 100 kHz selectivity	Δf = –100 kHz; f_{tuned} = 76 to 108 MHz; note 2	8	12	–	dB
IR	image rejection	f_{tuned} = 76 to 108 MHz; V_{RF} = 50 dBμV	24	30	–	dB
FM IF level detector and mute voltage						
V_{RF}	RF input voltage for start of level ADC	read mode data byte 4: bit 4 = 1	2	3	5	μV
ΔV_{step}	level ADC step size		2	3	5	dB
PIN TMUTE						
V_{level}	level output DC voltage	V_{RF} = 0 μV	1.55	1.65	1.80	V
		V_{RF} = 3 μV	1.60	1.70	1.85	V
$V_{level(slope)}$	slope of level voltage	V_{RF} = 10 to 500 μV	150	165	180	$\frac{mV}{20\ dB}$
R_o	output resistance		280	400	520	kΩ

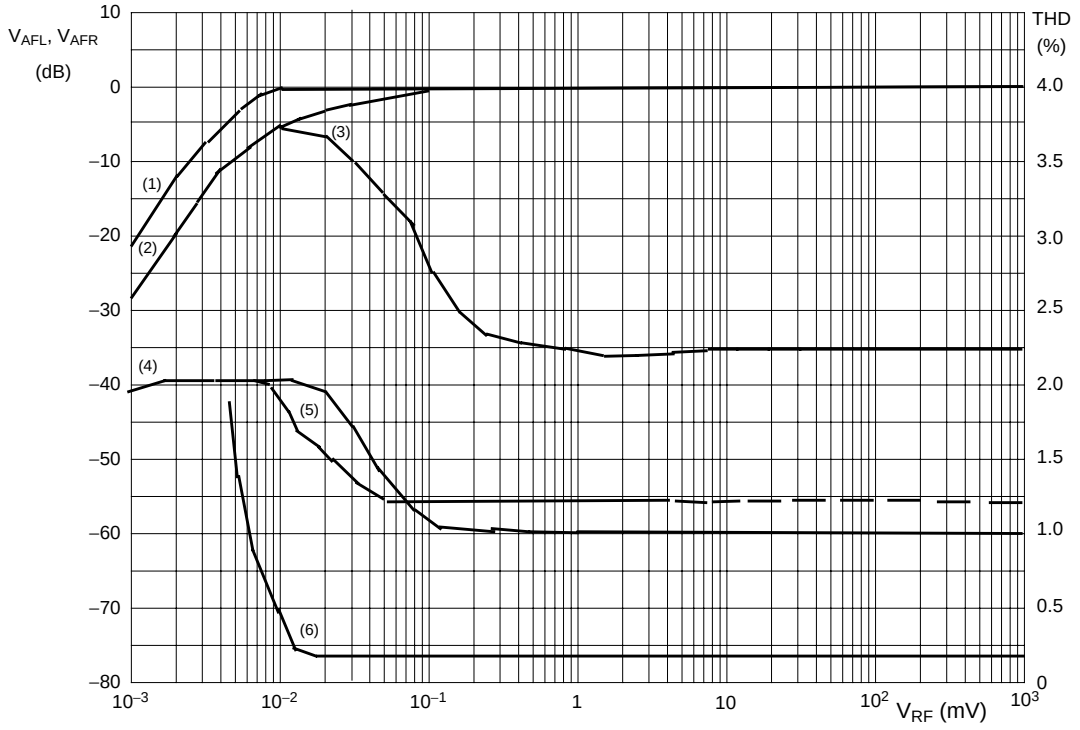
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FM demodulator: pin MPXO						
V_{MPXO}	demodulator output voltage	V_{RF} = 1 mV; L = R; Δf = 22.5 kHz; f_{mod} = 1 kHz; de-emphasis = 75 µs; BAF = 300 Hz to 15 kHz	60	75	90	mV
(S+N)/N	maximum signal plus noise-to-noise ratio	V_{RF} = 1 mV; L = R; Δf = 22.5 kHz; f_{mod} = 1 kHz; de-emphasis = 75 µs; BAF = 300 Hz to 15 kHz	54	60	–	dB
THD	total harmonic distortion	V_{RF} = 1 mV; L = R; Δf = 75 kHz; f_{mod} = 1 kHz; de-emphasis = 75 µs	–	0.5	1.5	%
α_{AM}	AM suppression	V_{RF} = 300 µV; L = R; Δf = 22.5 kHz; f_{mod} = 1 kHz; m = 0.3; de-emphasis = 75 µs; BAF = 300 Hz to 15 kHz	40	–	–	dB
R_o	demodulator output resistance		–	–	500	Ω
I_{sink}	demodulator output sink current		–	–	30	µA
Soft mute						
V_{RF}	RF input voltage for soft mute start	α_{mute} = 3 dB; data byte 4: bit 3 = 1	3	5	10	µV
α_{mute}	mute attenuation	V_{RF} = 1 µV; L = R; Δf = 22.5 kHz; f_{mod} = 1 kHz de-emphasis = 75 µs; BAF = 300 Hz to 15 kHz; data byte 4: bit 3 = 1	10	20	30	dB
MPX decoder						
V_{AFL}; V_{AFR}	left and right audio frequency output voltage	V_{RF} = 1 mV; L = R; Δf = 22.5 kHz; f_{mod} = 1 kHz; de-emphasis = 75 µs	60	75	90	mV
R_{AFL}; R_{AFR}	left and right audio frequency output resistance		–	–	50	Ω
$I_{sink(AFL)}$; $I_{sink(AFR)}$	left and right audio frequency output sink current		170	–	–	µA
$V_{MPXIN(max)}$	input overdrive margin	THD < 3%	4	–	–	dB
V_{AFL}/V_{AFR}	left and right audio frequency output voltage difference	V_{RF} = 1 mV; L = R; Δf = 75 kHz; f_{mod} = 1 kHz; de-emphasis = 75 µs	–1	–	+1	dB
$\alpha_{cs(stereo)}$	stereo channel separation	V_{RF} = 1 mV; R = L = 0 or R = 0 and L = 1 including 9% pilot; Δf = 75 kHz; f_{mod} = 1 kHz; data byte 3: bit 3 = 0; data byte 4: bit 1 = 1	24	30	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
(S+N)/N	maximum signal plus noise-to-noise ratio	V_{RF} = 1 mV; L = R; Δf = 22.5 kHz; f_{mod} = 1 kHz; de-emphasis = 75 µs; BAF = 300 Hz to 15 kHz	54	60	–	dB
THD	total harmonic distortion	V_{RF} = 1 mV; L = R; Δf = 75 kHz; f_{mod} = 1 kHz; de-emphasis = 75 µs	–	0.4	1	%
α_{pilot}	pilot suppression measured at pins V_{AFL} and V_{AFR}	related to Δf = 75 kHz; f_{mod} = 1 kHz; de-emphasis = 75 µs	40	50	–	dB
Δf_{pilot}	stereo pilot frequency deviation	V_{RF} = 1 mV; read mode; data byte 3:				
		bit 7 = 1	–	3.6	5.8	kHz
		bit 7 = 0	1	3	–	kHz
$\frac{\Delta f_{pilot1}}{\Delta f_{pilot2}}$	pilot switch hysteresis	V_{RF} = 1 mV	2	–	–	dB
HIGH CUT CONTROL						
$T_{de\text{-}em}$	de-emphasis time constant	V_{RF} = 1 mV				
		data byte 5: bit 2 = 0	38	50	62	µs
		data byte 5: bit 2 = 1	57	75	93	µs
		V_{RF} = 1 µV				
		data byte 5: bit 2 = 0	114	150	186	µs
		data byte 5: bit 2 = 1	171	225	279	µs
MONO/STEREO BLEND CONTROL						
$\alpha_{cs(stereo)}$	stereo channel separation	V_{RF} = 45 µV; R = L = 0 or R = 0 and L = 1 including 9% pilot; Δf = 75 kHz; f_{mod} = 1 kHz; data byte 3: bit 3 = 0; data byte 4: bit 1 = 1	4	10	16	dB
MONO/STEREO SWITCHED						
$\alpha_{cs(stereo)}$	stereo channel separation switching from mono to stereo with increasing RF input level	V_{RF} = 1 mV; R = L = 0 or R = 0 and L = 1 including 9% pilot; Δf = 75 kHz; f_{mod} = 1 kHz; data byte 3: bit 3 = 0; data byte 4: bit 1 = 0	24	–	–	dB
$\alpha_{cs(stereo)}$	stereo channel separation switching from stereo to mono with decreasing RF input level	V_{RF} = 20 µV; R = L = 0 or R = 0 and L = 1 including 9% pilot; Δf = 75 kHz; f_{mod} = 1 kHz; data byte 3: bit 3 = 0; data byte 4: bit 1 = 0	–	–	1	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
BUS DRIVEN MUTE FUNCTIONS						
Tuning mute						
α_{mute}	V_{AFL} and V_{AFR} muting depth	data byte 1: bit 7 = 1	–60	–	–	dB
$\alpha_{mute(R)}$	V_{AFR} muting depth	data byte 3: bit 1 = 1	–80	–	–	dB
$\alpha_{mute(L)}$	V_{AFL} muting depth	data byte 3: bit 2 = 1	–80	–	–	dB

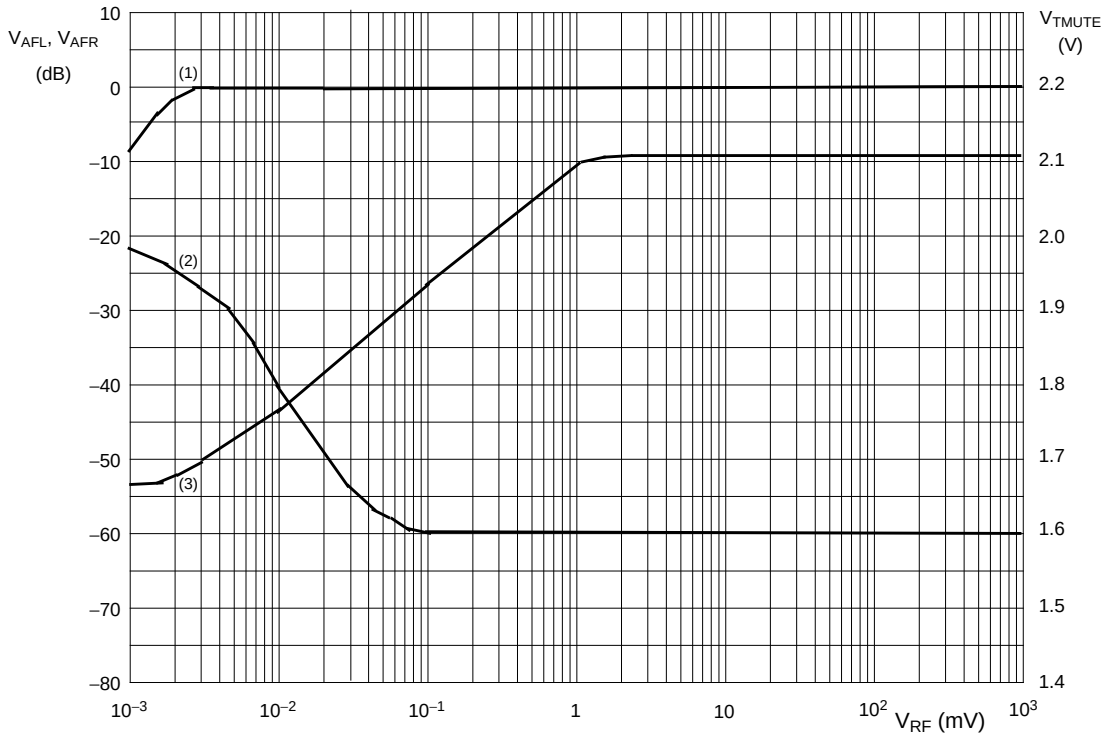
Notes

1. V_{RF} in Fig.5 is replaced by V_{RF1} + V_{RF2}. The radio is tuned to 98 MHz (HIGH side injection).
2. LOW side and HIGH side selectivity can be switched by changing the mixer from HIGH side to LOW side LO injection.



(1) Mono signal; soft mute on.
(2) Left channel with modulation left; SNC on.
(3) Right channel with modulation left; SNC on.
(4) Noise in mono mode; soft mute on.
(5) Noise in stereo mode; SNC on.
(6) Total harmonic distortion; Δf = 75 kHz; L = R; f_{mod} = 1 kHz.

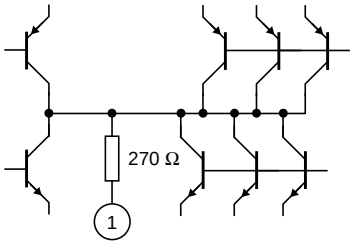
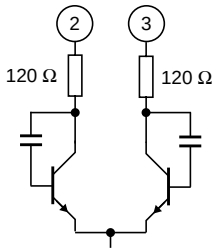
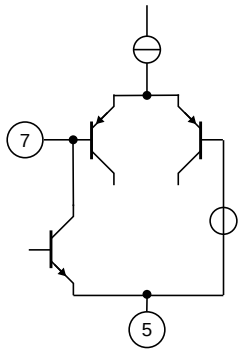
Fig.3 FM characteristics 1.

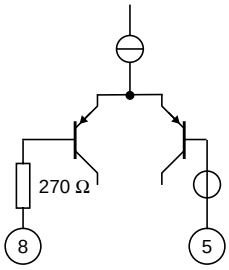
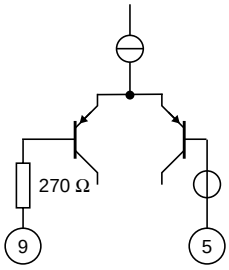
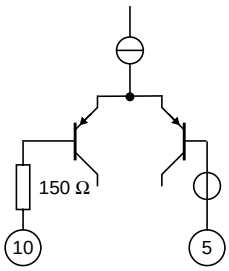
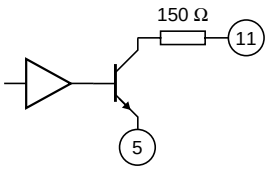
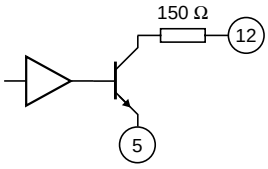


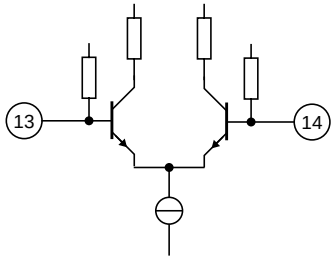
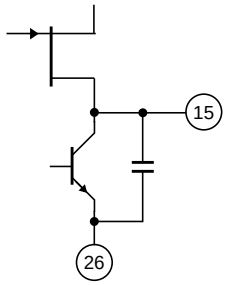
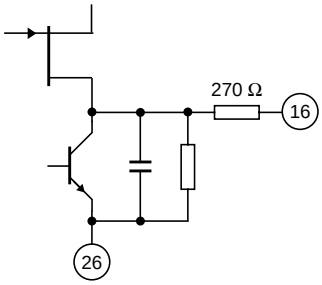
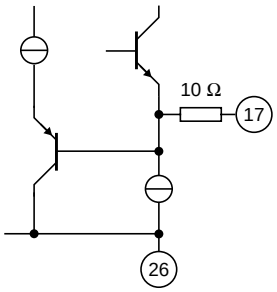
(1) Mono signal; no soft mute.
(2) Noise in mono mode; no soft mute.
(3) Level voltage; V_{CCA} = 2.7 V.

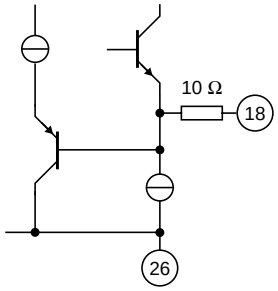
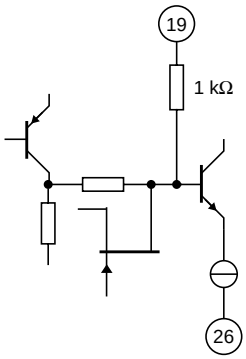
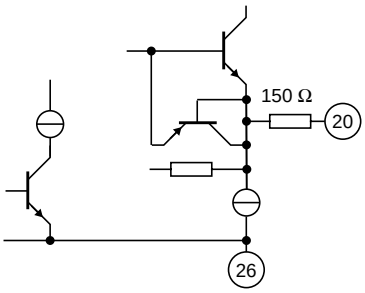
Fig.4 FM characteristics 2.

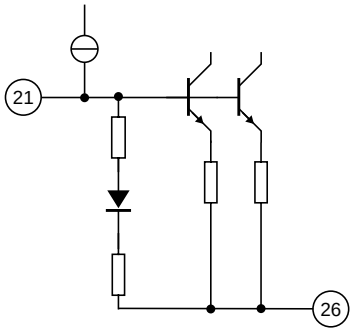
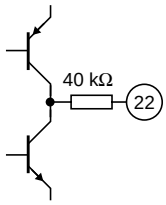
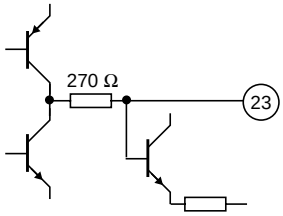
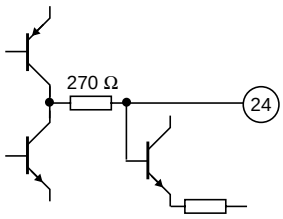
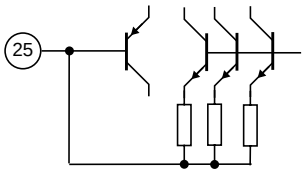
INTERNAL PIN CONFIGURATION

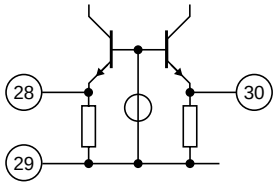
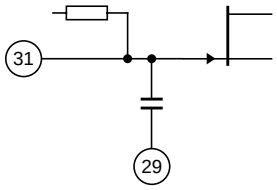
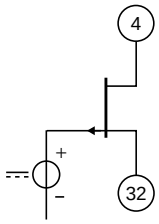
PIN	SYMBOL	EQUIVALENT CIRCUIT
1	CPOUT	
2	VCOTANK1	
3	VCOTANK2	
4	$V_{CC(VCO)}$	
5	DGND	
6	V_{CCD}	
7	DATA	

PIN	SYMBOL	EQUIVALENT CIRCUIT
8	CLOCK	
9	BUSMODE	
10	BUSENABLE	
11	SWPORT1	
12	SWPORT2	

PIN	SYMBOL	EQUIVALENT CIRCUIT
13	XTAL1	
14	XTAL2	
15	PHASEFIL	
16	PILFIL	
17	V_{AFL}	

PIN	SYMBOL	EQUIVALENT CIRCUIT
18	V_{AFR}	
19	TMUTE	
20	MPXO	

PIN	SYMBOL	EQUIVALENT CIRCUIT
21	V_{ref}	
22	TIFC	
23	LIMDEC1	
24	LIMDEC2	
25	I_{gain}	

PIN	SYMBOL	EQUIVALENT CIRCUIT
26	AGND	
27	V_{CCA}	
28	RFI1	
29	RFGND	
30	RFI2	
31	TAGC	
32	LOOPSW	

APPLICATION INFORMATION

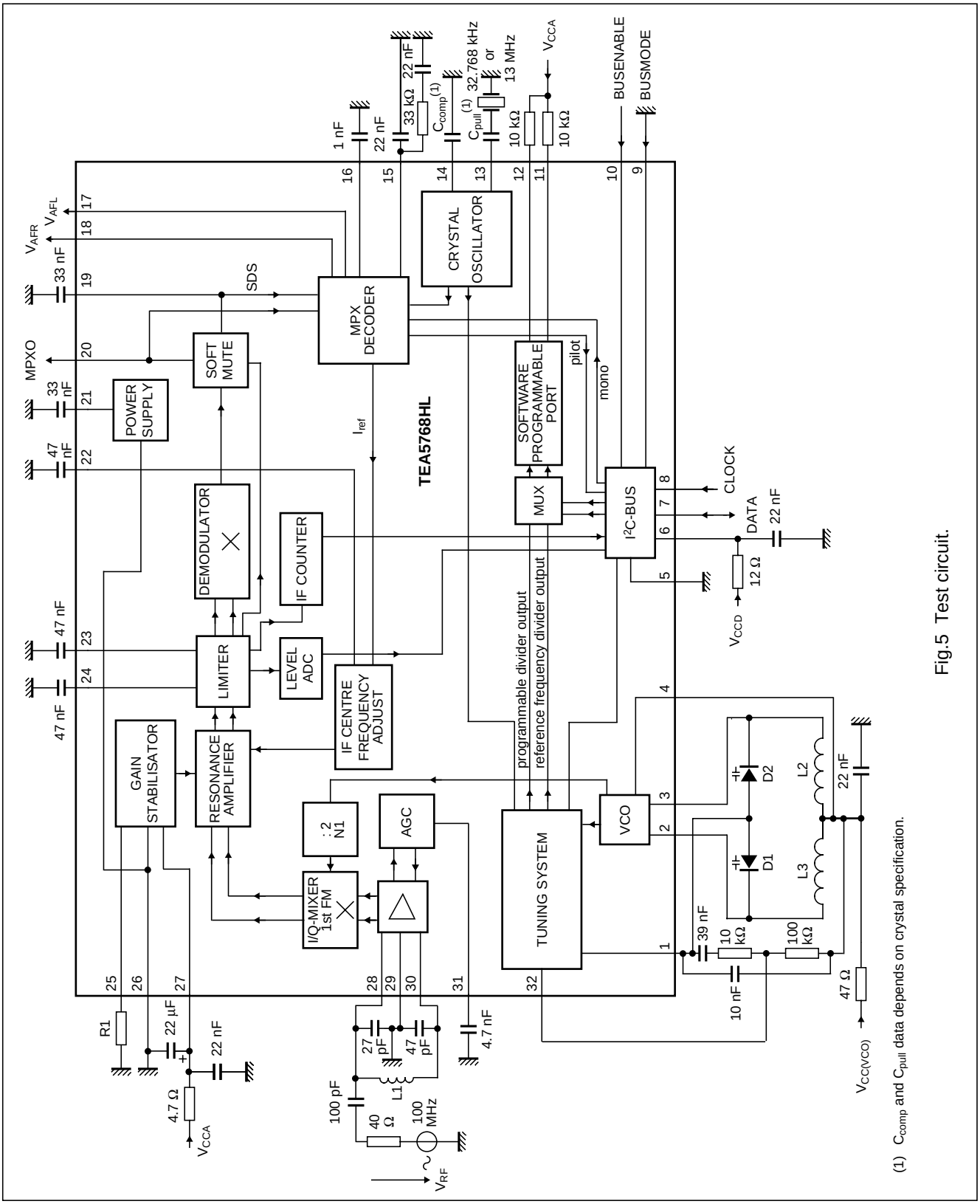
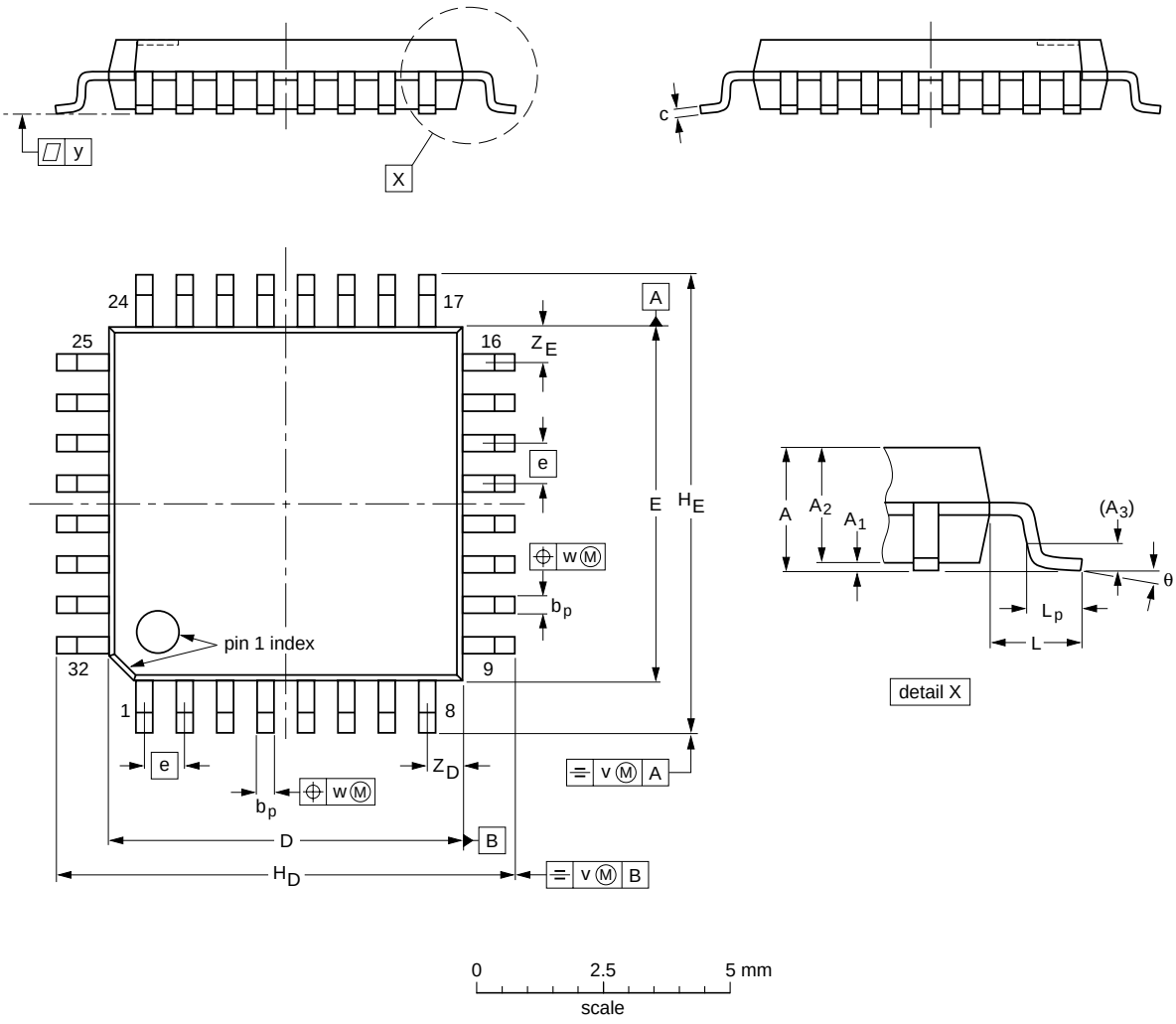


Fig.5 Test circuit.

PACKAGE OUTLINE

LQFP32: plastic low profile quad flat package; 32 leads; body 7 x 7 x 1.4 mm **SOT358-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.4 0.3	0.18 0.12	7.1 6.9	7.1 6.9	0.8	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.25	0.1	0.9 0.5	0.9 0.5	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT358 -1	136E03	MS-026				~~99-12-27~~ 00-01-19

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW[1]
BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable[2]	suitable
PLCC[3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[3][4]	suitable
SSOP, TSSOP, VSO	not recommended[5]	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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PURCHASE OF PHILIPS I²C COMPONENTS

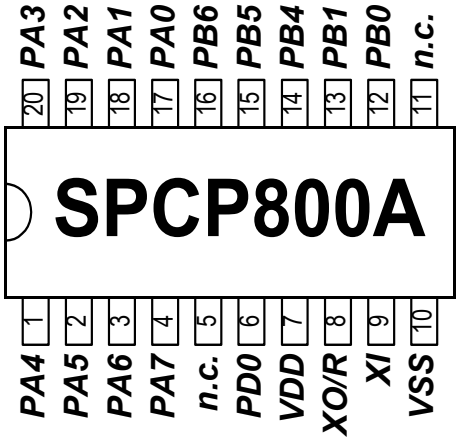
Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

PIN DESCRIPTION

Name	*20 Pin SOP*	*Functional Description*
VSS	10	*System Ground*.
PB0:1	12:13	*GPIO Port B0:1*. General-purpose I/Os. Using internal setting can configure it. In addition, PB0 is the serial data input and PB1 is the clock input for programming mode.
PB4:5	14:15	*GPIO Port B4:5*. General-purpose inputs/output. Using internal setting can configure it. In addition, PB4 can be used as the Main nRESET input. PB5 can be used as the external Main IRQ input.
PB6	16	*GPIO Port B6*. General-purpose I/O. Using internal setting can configure it. In addition, PB6 is a selective clock input for Timer 2.
PA0:3	17:20	*GPIO Port A0:3*. General-purpose I/Os. Using internal setting can configure it.
PA4:7	1:4	*GPIO Port A4:7*. General-purpose I/Os. Using internal setting can configure it.
PD0	6	*GPIO Port D0 (LED Output 0)*. This I/O channel can be LED high current driven output or general I/O. Using internal setting can configure it. In programming mode, PD0 is a VPP pin for programming interface.
VDD	7	*System Power Supply*.
XO/R	8	*Crystal In or Resistor In Input*. An external resistive pull-up is used to connect with internal OSC circuitry for generating the internal clock and the related time base in R-Oscillation mode. It will be connected with external crystal for a crystal oscillation circuitry in crystal mode.
XI	9	*Crystal Output or External Clock Input*. External clock input is used to connect with internal clock circuitry to generate the internal clock and the related time base in External clock mode. It will be connected with external crystal for a crystal oscillation circuitry in crystal mode.

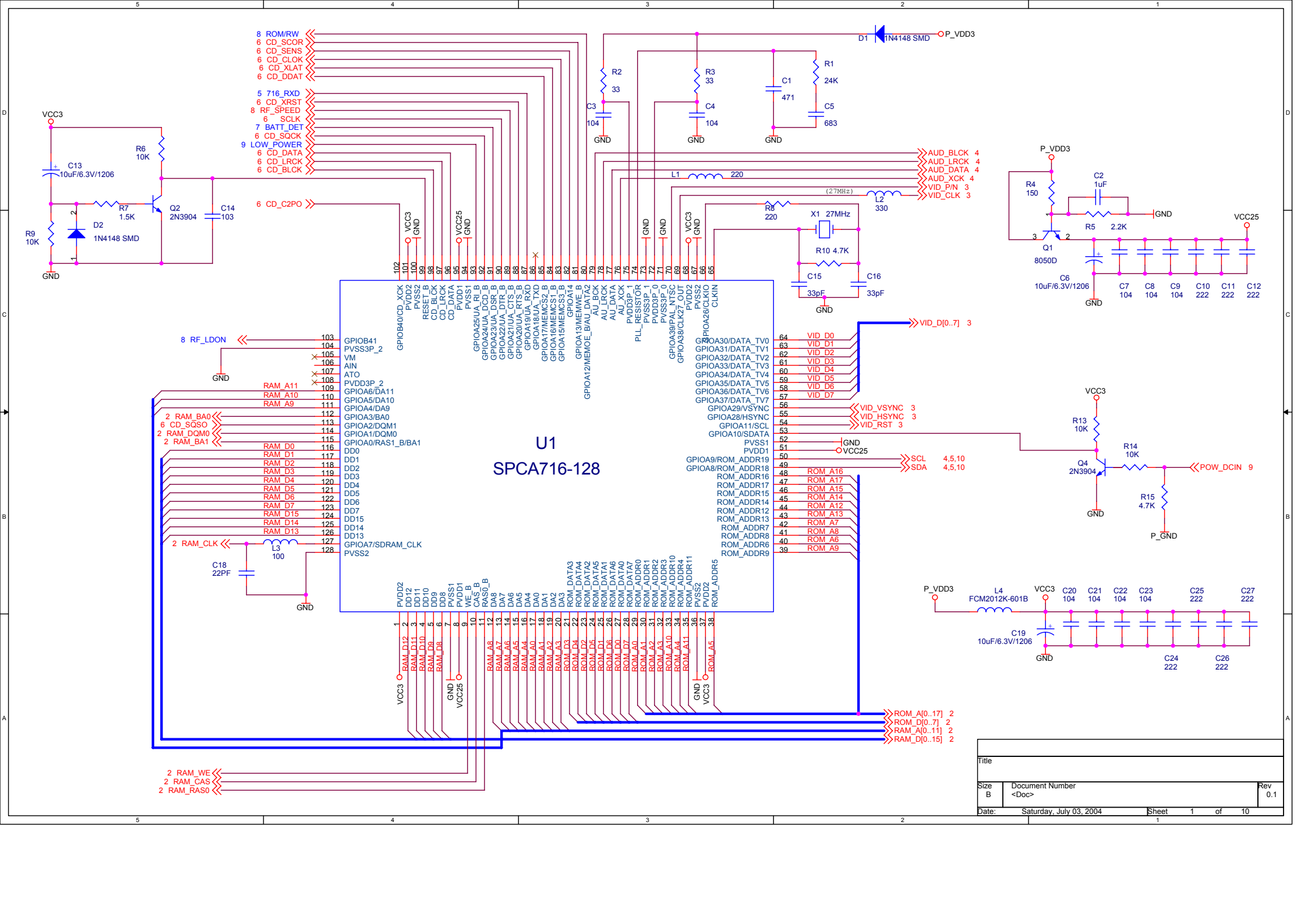
Note: Pin 5 and Pin 11 are No Connection (n.c.).

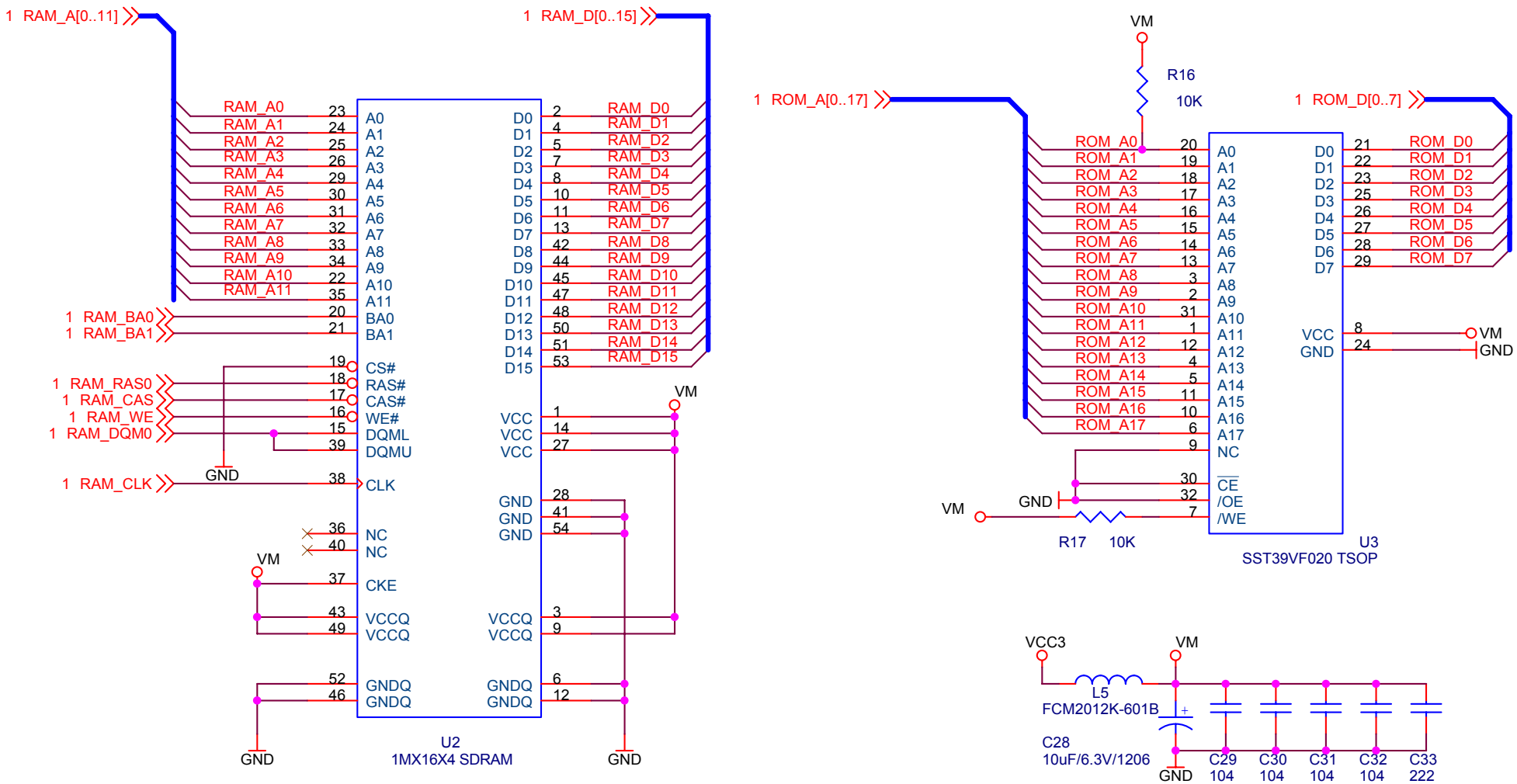
PIN ASSIGNMENT



REVISION CONTROL

Revision	*Date*	*Update History*
0.10		1. Create this document. 2. Released as revision 0.10.


U1
SPCA716-128
8 ROM/RW
6 CD_SCOR
6 CD_SENS
6 CD_CLOK
6 CD_XLAT
6 CD_DDAT
5 716_RXD
6 CD_XRST
8 RF_SPEED
6 SCLK
7 BATT_DET
6 CD_SQCK
9 LOW_POWER
6 CD_DATA
6 CD_LRCK
6 CD_BLCK
6 CD_C2PO
8 RF_LDON
2 RAM_BA0
6 CD_SQSO
2 RAM_DQM0
2 RAM_BA1
2 RAM_CLK
2 RAM_WE
2 RAM_CAS
2 RAM_RAS0
D1 1N4148 SMD
P_VDD3
R1 24K
R2 33
R3 33
C1 471
C3 104
C4 104
C5 683
VCC3
R6 10K
C13 10uF/6.3V/1206
R7 1.5K
Q2 2N3904
C14 103
D2 1N4148 SMD
R9 10K
GND
L1 220
L2 330
(27MHz)
R8 220
X1 27MHz
R10 4.7K
C15 33pF
C16 33pF
AUD_BLCK 4
AUD_LRCK 4
AUD_DATA 4
AUD_XCK 4
VID_P/N 3
VID_CLK 3
VID_D[0..7] 3
VID_VSYNC 3
VID_HSYNC 3
VID_RST 3
SCL 4,5,10
SDA 4,5,10
ROM_A[0..17] 2
ROM_D[0..7] 2
RAM_A[0..11] 2
RAM_D[0..15] 2
P_VDD3
R4 150
C2 1uF
R5 2.2K
Q1 8050D
C6 10uF/6.3V/1206
C7 104
C8 104
C9 104
C10 222
C11 222
C12 222
VCC25
VCC3
R13 10K
R14 10K
Q4 2N3904
R15 4.7K
POW_DCIN 9
P_GND
L3 100
C18 22PF
L4 FCM2012K-601B
C19 10uF/6.3V/1206
C20 104
C21 104
C22 104
C23 104
C24 222
C25 222
C26 222
C27 222
Title
Size B
Document Number <Doc>
Rev 0.1
Date: Saturday, July 03, 2004
Sheet 1 of 10



Title		
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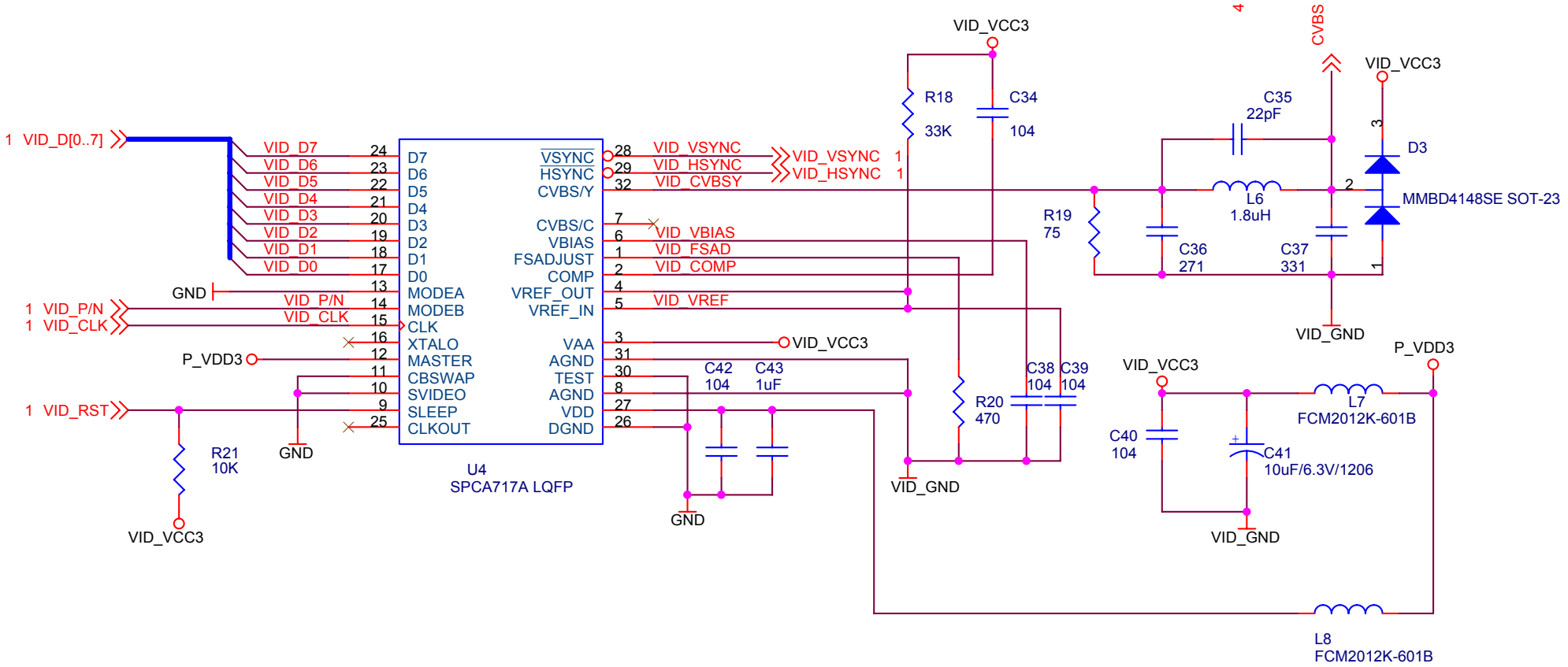

Title		
Size A	Document Number <Doc>	Rev 0.1
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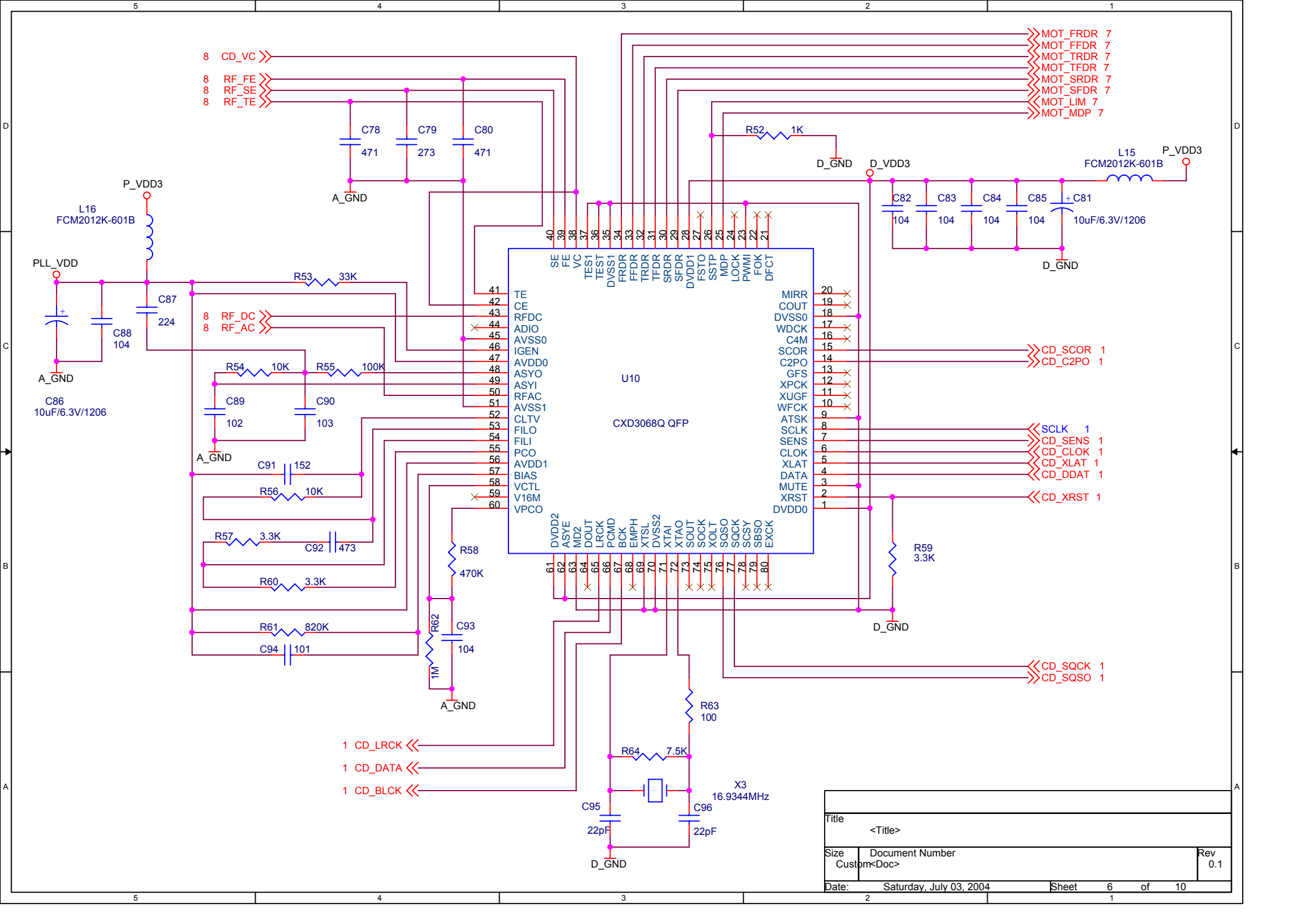
8 CD_VC
8 RF_FE
8 RF_SE
8 RF_TE
C78 471
C79 273
C80 471
A_GND
P_VDD3
L16 FCM2012K-601B
PLL_VDD
C87 224
C88 104
C86 10uF/6.3V/1206
R53 33K
8 RF_DC
8 RF_AC
R54 10K
R55 100K
C89 102
C90 103
C91 152
R56 10K
R57 3.3K
C92 473
R60 3.3K
R58 470K
R61 820K
C94 101
R62 1M
C93 104
U10
CXD3068Q QFP
TE CE RFDC ADIO AVSS0 IGEN AVDD0 ASYO ASYI RFAC AVSS1 CLTV FILO FILI PCO AVDD1 BIAS VCTL V16M VPCO
SE FE VC TES1 TEST DVSS1 FRDR FFDR TRDR TFDR SRDR SFDR DVDD1 FSTO SSTP MDP LOCK PWMI FOK DFCT
MIRR COUT DVSS0 WDCK C4M SCOR C2PO GFS XPCK XUGF WFCK ATSK SCLK SENS CLOK XLAT DATA MUTE XRST DVDD0
DVDD2 ASYE MD2 DOUT LRCK PCMD BCK EMPH XTSL DVSS2 XTAI XTAO SOUT SOCK XOLT SQSO SQCK SCSY SBSO EXCK
MOT_FRDR 7
MOT_FFDR 7
MOT_TRDR 7
MOT_TFDR 7
MOT_SRDR 7
MOT_SFDR 7
MOT_LIM 7
MOT_MDP 7
R52 1K
D_GND
D_VDD3
L15 FCM2012K-601B
C82 104
C83 104
C84 104
C85 104
C81 10uF/6.3V/1206
CD_SCOR 1
CD_C2PO 1
SCLK 1
CD_SENS 1
CD_CLOK 1
CD_XLAT 1
CD_DDAT 1
CD_XRST 1
R59 3.3K
CD_SQCK 1
CD_SQSO 1
R63 100
R64 7.5K
X3 16.9344MHz
C95 22pF
C96 22pF
1 CD_LRCK
1 CD_DATA
1 CD_BLCK
Title <Title>
Size Custom<Doc>
Document Number
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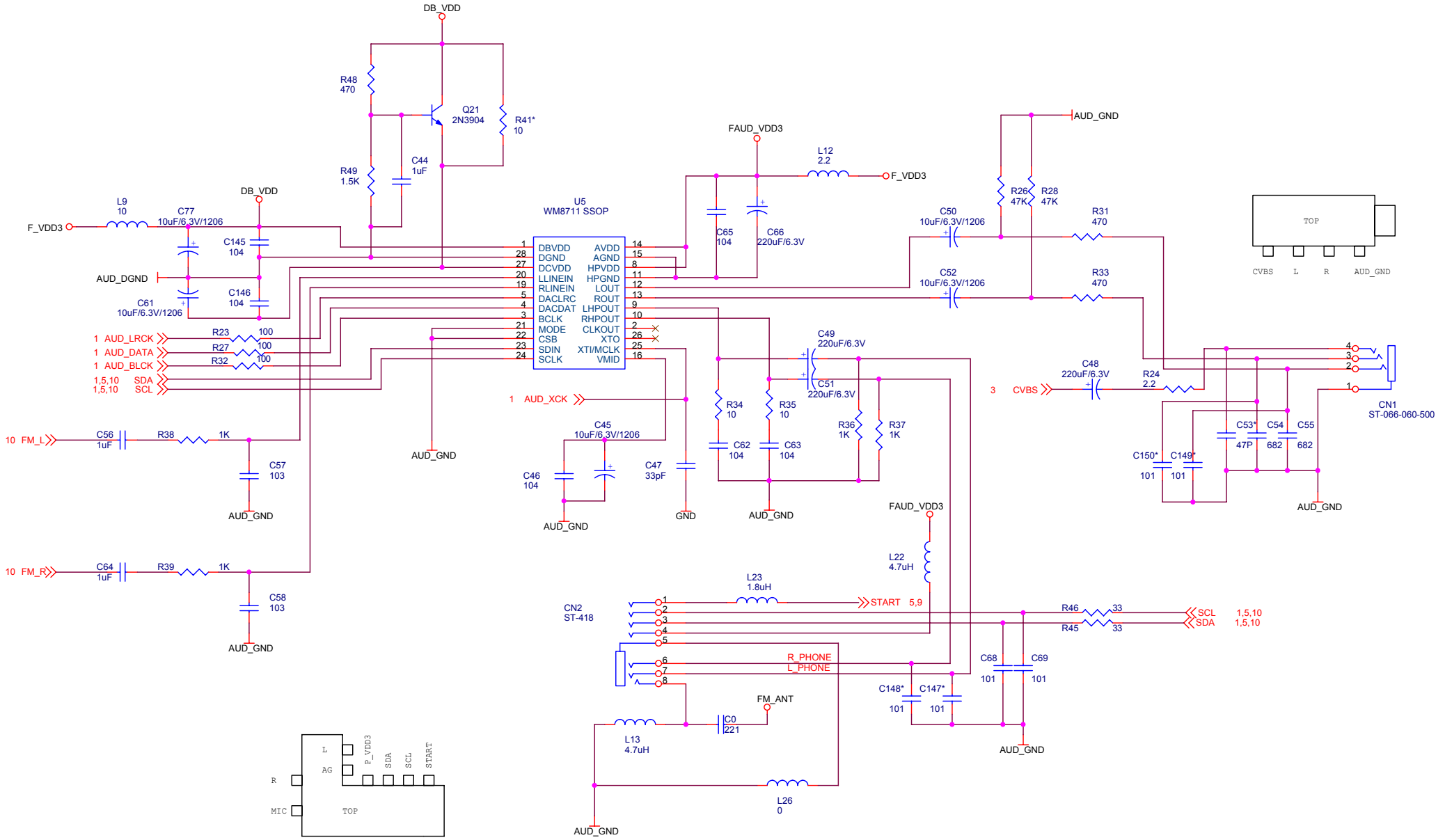

1 MIC连线既是线控器的系统地(通过L13) 又是FM的天线

2 AG在主板上通过L26连地 在线控器上是音频地

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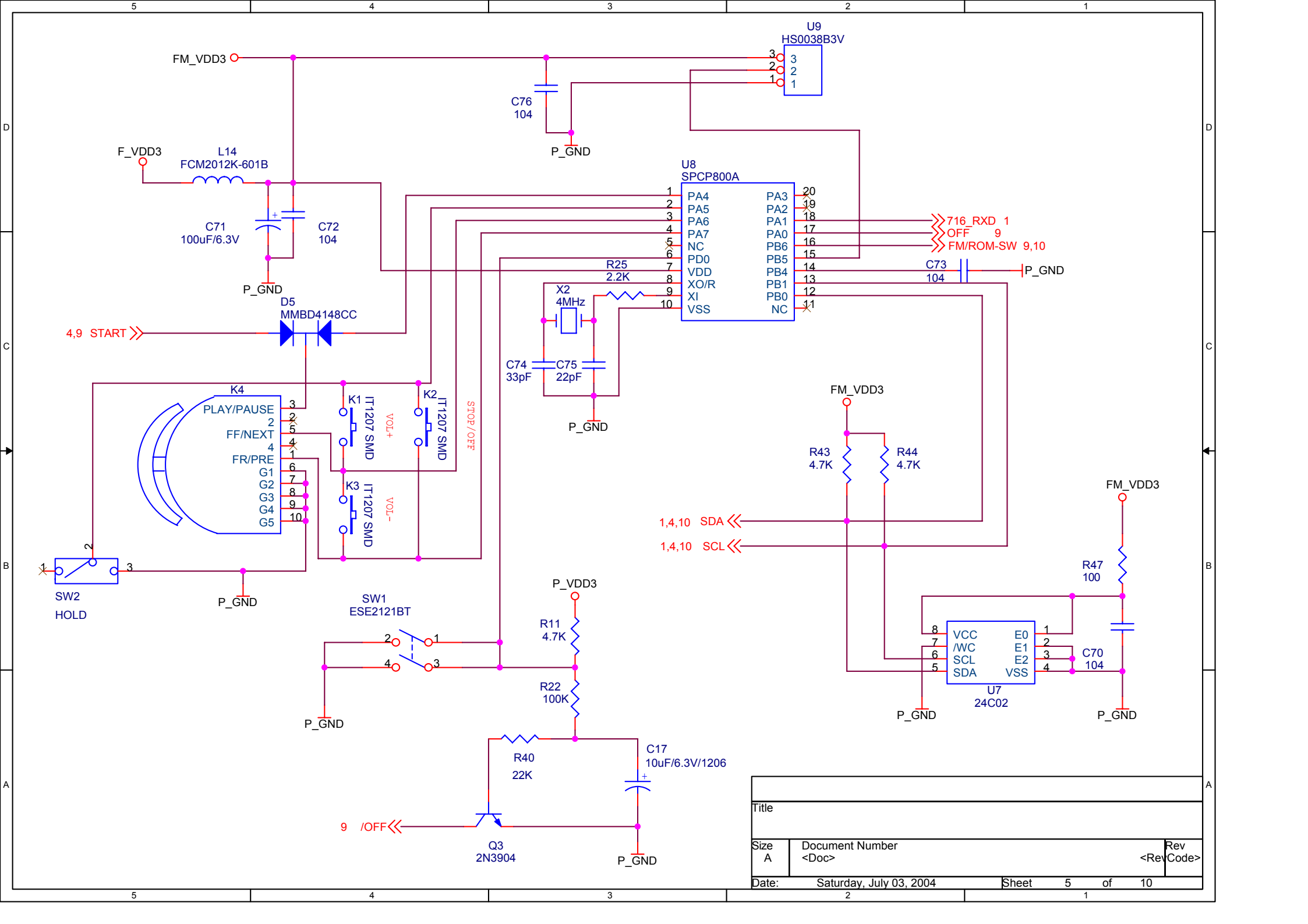
U9
HS0038B3V
FM_VDD3
C76
104
P_GND
F_VDD3
L14
FCM2012K-601B
C71
100uF/6.3V
C72
104
P_GND
U8
SPCP800A
PA4
PA5
PA6
PA7
NC
PD0
VDD
XO/R
XI
VSS
PA3
PA2
PA1
PA0
PB6
PB5
PB4
PB1
PB0
NC
716_RXD 1
OFF 9
FM/ROM-SW 9,10
R25
2.2K
X2
4MHz
C73
104
P_GND
D5
MMBD4148CC
4,9 START
C74
33pF
C75
22pF
P_GND
K4
PLAY/PAUSE
FF/NEXT
FR/PRE
G1
G2
G3
G4
G5
K1 IT1207 SMD
K2 IT1207 SMD
K3 IT1207 SMD
VOL+
VOL-
STOP/OFF
FM_VDD3
R43
4.7K
R44
4.7K
1,4,10 SDA
1,4,10 SCL
FM_VDD3
R47
100
SW2
HOLD
P_GND
SW1
ESE2121BT
P_VDD3
R11
4.7K
R22
100K
P_GND
U7
24C02
VCC
/WC
SCL
SDA
E0
E1
E2
VSS
C70
104
P_GND
P_GND
R40
22K
C17
10uF/6.3V/1206
9 /OFF
Q3
2N3904
P_GND
Title
Size
A
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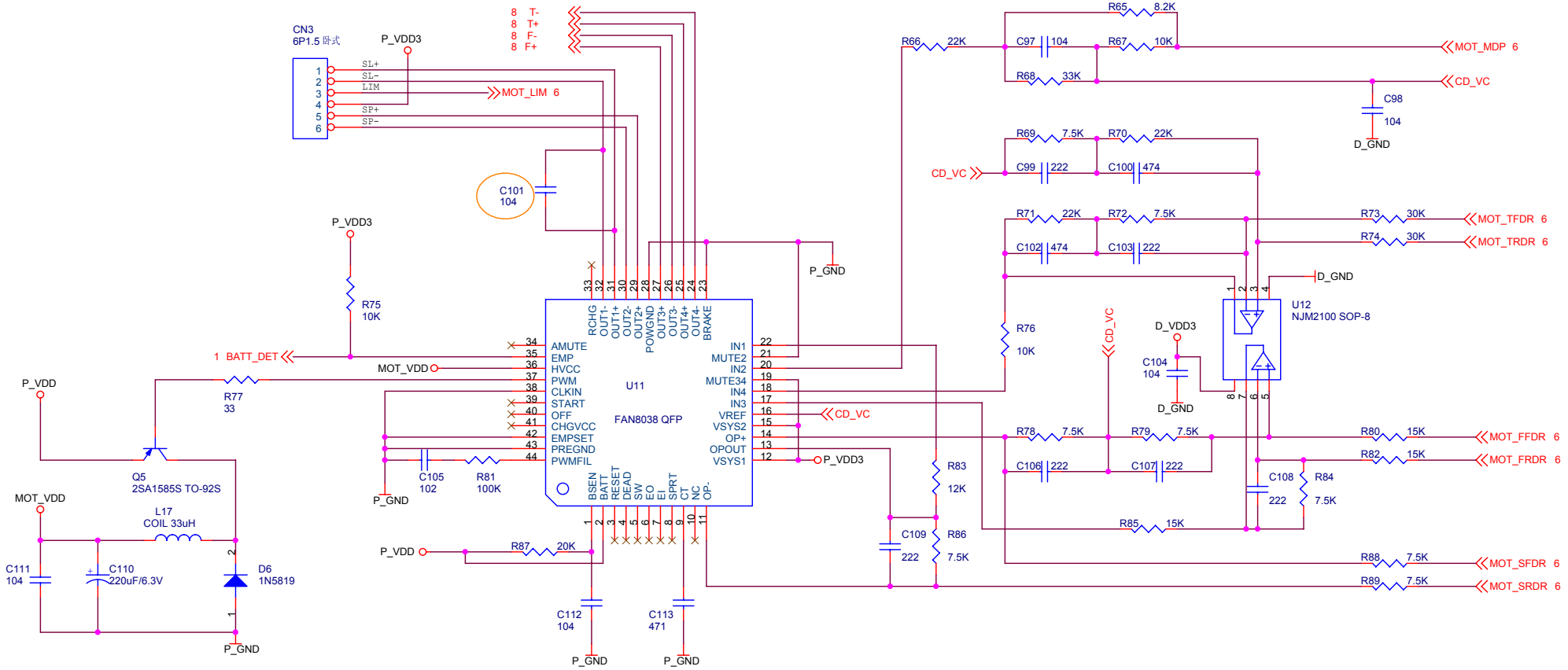

Title	<Title>	
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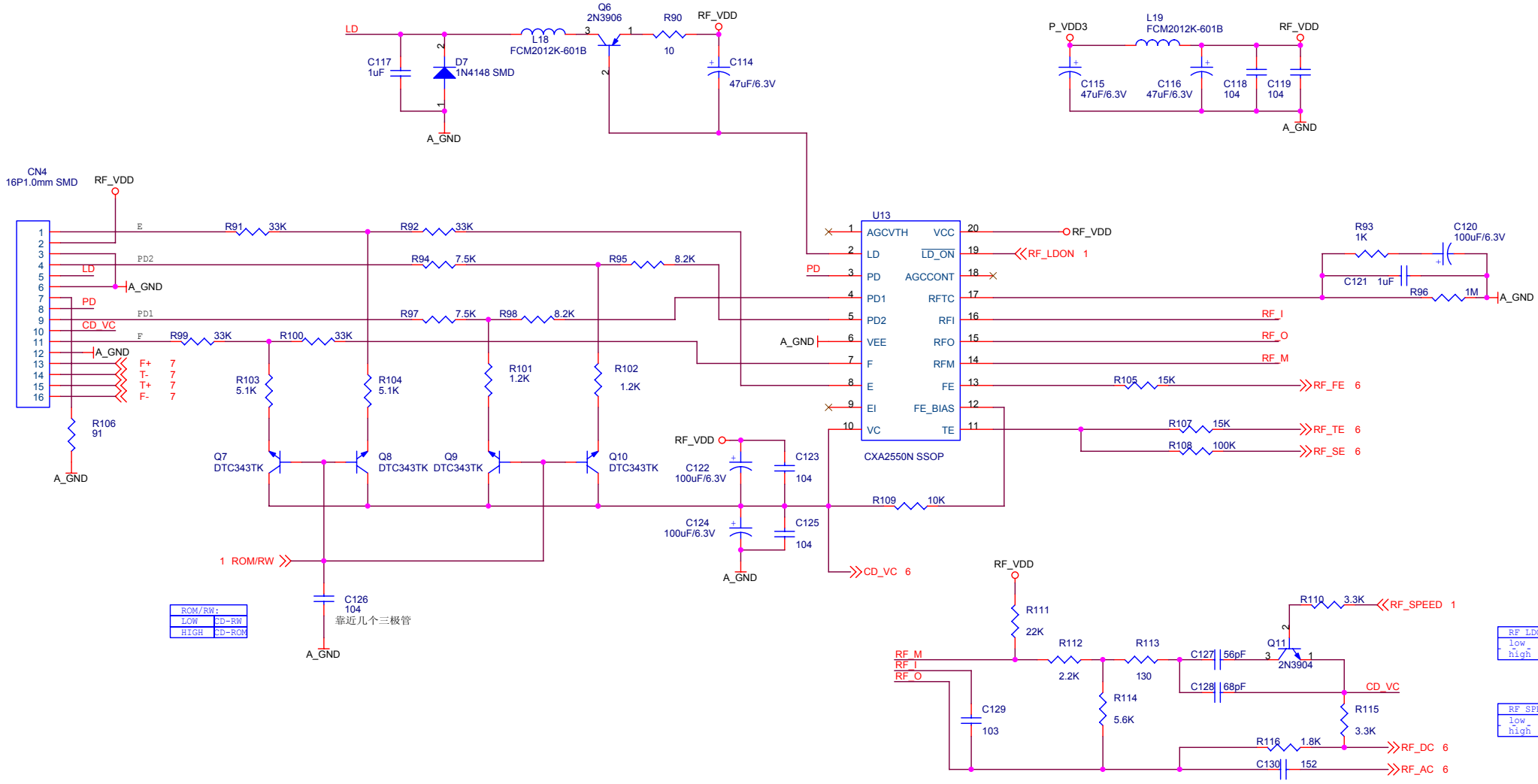

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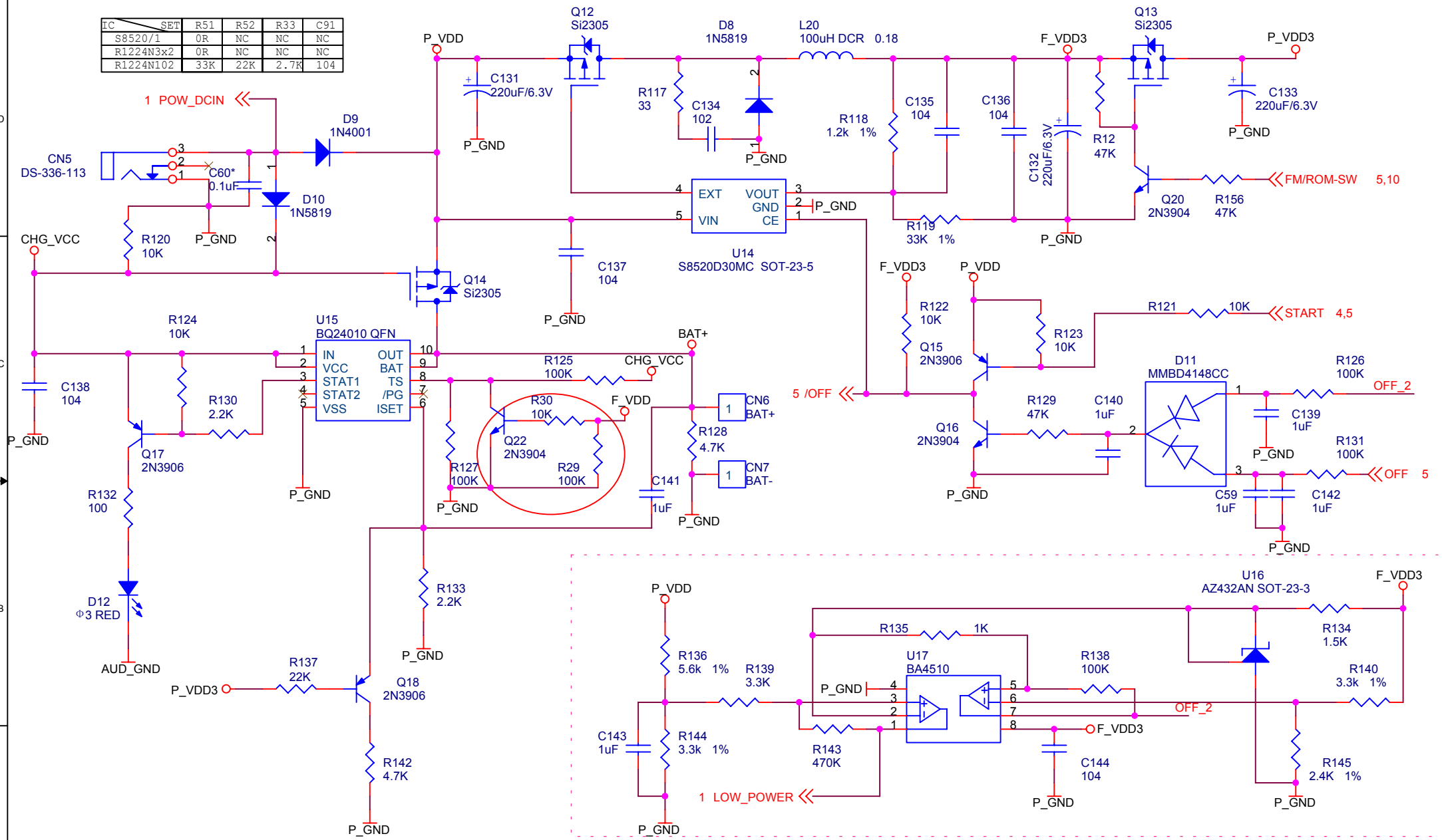
IC \ SET	R51	R52	R33	C91
S8520/1	0R	NC	NC	NC
R1224N3x2	0R	NC	NC	NC
R1224N102	33K	22K	2.7K	104



Title		
Size: Custom<Doc>	Document Number	Rev: <RevCode>
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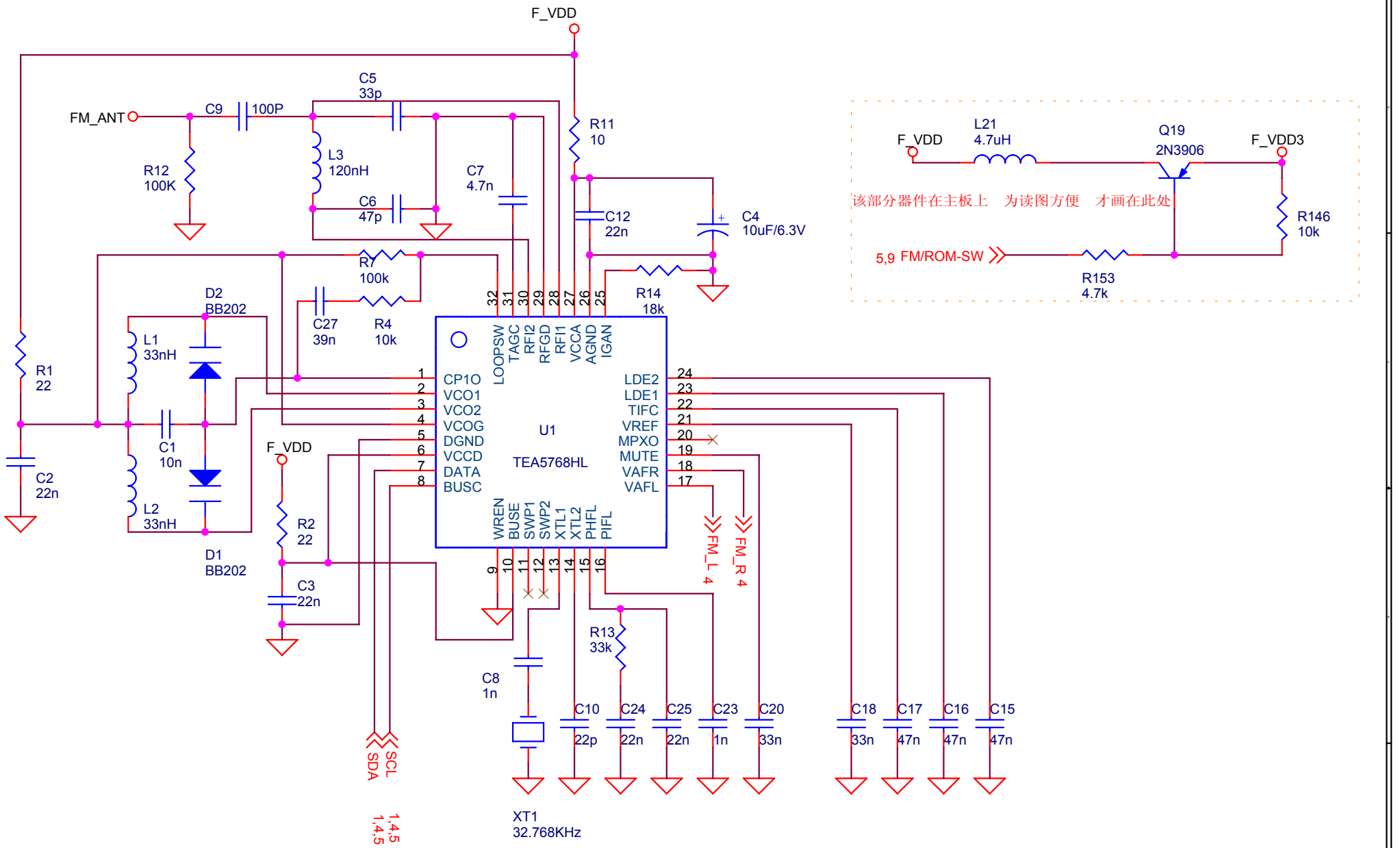

Title <Title>		
Size Custom<Doc>	Document Number	Rev <RevCod
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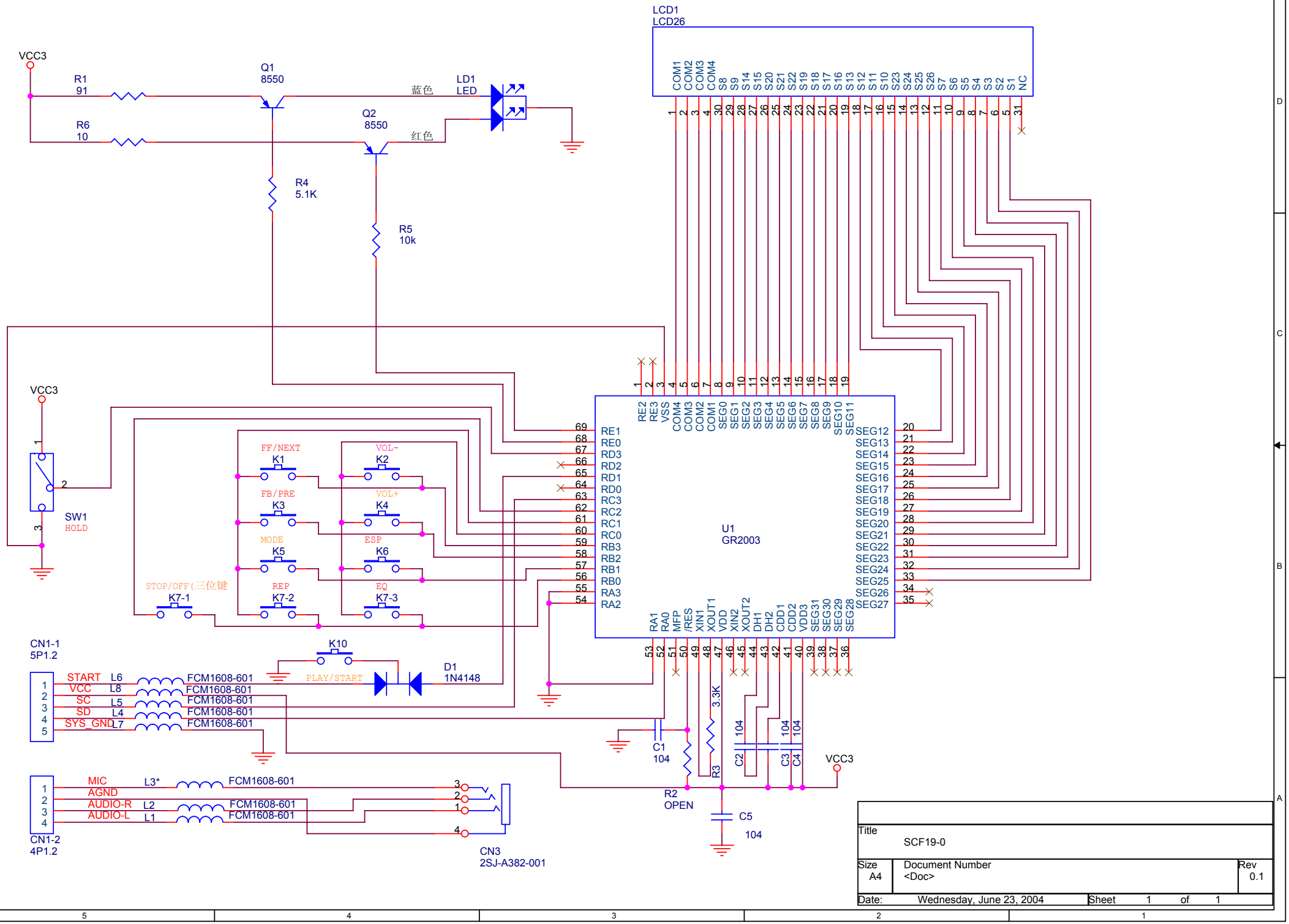

Title	SCF19-0	
Size A4	Document Number <Doc>	Rev 0.1
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