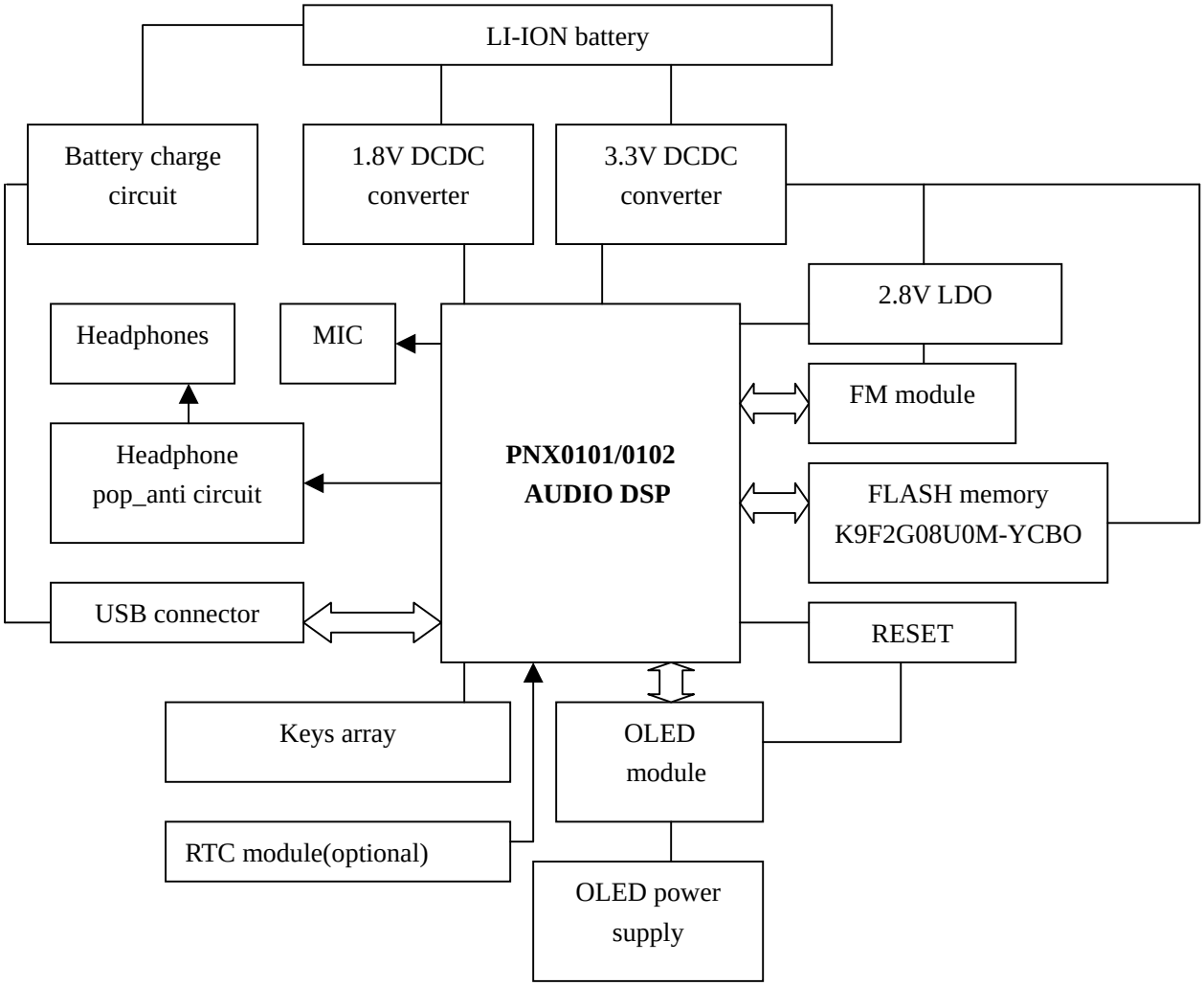
X7-2 block diagram



G690/G691

Microprocessor Reset IC

Features

- **Precision Monitoring of +3V, +3.3V, and +5V Power-Supply Voltages**
- **Fully Specified Over Temperature**
- **Available in Three Output Configurations**
  - **Push-Pull $\overline{\text{RESET}}$ Output (G690L)**
  - **Push-Pull RESET Output (G690H)**
  - **Open-Drain $\overline{\text{RESET}}$ Output (G691L)**
- **140ms min Power-On Reset Pulse Width**
- **10µA Supply Current**
- **Guaranteed Reset Valid to V_{CC} = +1V**
- **Power Supply Transient Immunity**
- **No External Components**
- **3-Pin SOT-23 Packages**

Applications

- **Computers**
- **Controllers**
- **Intelligent Instruments**
- **Critical µP and µC Power Monitoring**
- **Portable / Battery-Powered Equipment**
- **Automotive**

General Description

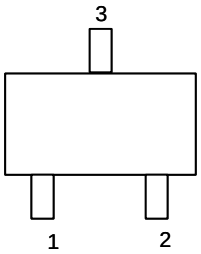
The G690/G691 are microprocessor (µP) supervisory circuits used to monitor the power supplies in µP and digital systems. They provide excellent circuit reliability and low cost by eliminating external components and adjustments when used with +5V, +3.3V, +3.0V- powered circuits.

These circuits perform a single function: they assert a reset signal whenever the V_{CC} supply voltage declines below a preset threshold, keeping it asserted for at least 140ms after V_{CC} has risen above the reset threshold. Reset thresholds suitable for operation with a variety of supply voltages are available.

The G691L has an open-drain output stage, while the G690 have push-pull outputs. The G691L's open-drain $\overline{\text{RESET}}$ output requires a pull-up resistor that can be connected to a voltage higher than V_{CC}. The G690L have an active-low $\overline{\text{RESET}}$ output, while the G690H has an active-high RESET output. The reset comparator is designed to ignore fast transients on V_{CC}, and the outputs are guaranteed to be in the correct logic state for V_{CC} down to 1V.

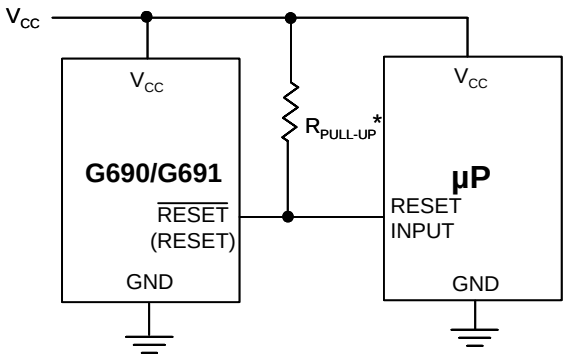
Low supply current makes the G690/G691 ideal for use in portable equipment. The G690/G691 are available in 3-pin SOT-23 packages.

Pin Configuration



SOT-23

Typical Application Circuit



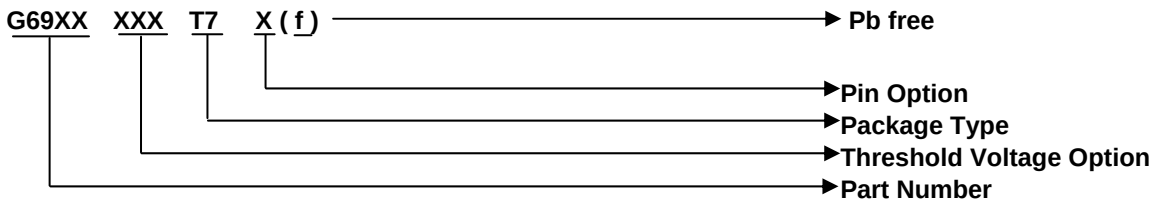
*G691 ONLY

Ordering Information

ORDER NUMBER	ORDER NUMBER (Pb free)	TEMP. RANGE	OUTPUT TYPE	PACKAGE
G690LxxxT7xU	G690LxxxT7xUf	-40°C ~ +105°C	Push-Pull Active Low	SOT-23
G690HxxxT7xU	G690HxxxT7xUf	-40°C ~ +105°C	Push-Pull Active High	SOT-23
G691LxxxT7xU	G691LxxxT7xUf	-40°C ~ +105°C	Open-Drain	SOT-23

U: Tape & Reel

Order Number Identification



PART NUMBER

G690L : Push-Pull Active Low Output
G690H : Push-Pull Active High Output
G691L : Open-Drain Output

THRESHOLD VOLTAGE OPTION

* xxx specifies the threshold voltage.
e.g. 263 denotes the 2.63V threshold voltage.

PACKAGE TYPE

T7 : SOT-23

PIN OPTION

	1	2	3
1 :	$\overline{RESET}$	GND	V_{CC}
2 :	$\overline{RESET}$	V_{CC}	GND
3 :	GND	$\overline{RESET}$	V_{CC}
4 :	GND	V_{CC}	$\overline{RESET}$
5 :	V_{CC}	GND	$\overline{RESET}$
6 :	V_{CC}	$\overline{RESET}$	GND

*RESET for G690H

Selector Guide

ORDER NUMBER	ORDER NUMBER (Pb free)	RESET THRESHOLD (V)	OUTPUT TYPE	TOP MARK
				SOT-23
G691L463T71U	G691L463T71Uf	4.63	Open-Drain	689Fx
G691L438T71U	G691L438T71Uf	4.38	Open-Drain	689Ex
G691L400T71U	G691L400T71Uf	4.00	Open-Drain	689Dx
G691L308T71U	G691L308T71Uf	3.08	Open-Drain	689Cx
G691L293T71U	G691L293T71Uf	2.93	Open-Drain	689Bx
G691L263T71U	G691L263T71Uf	2.63	Open-Drain	689Ax
G690H463T71U	G690H463T71Uf	4.63	Push-Pull RESET	688Lx
G690H438T71U	G690H438T71Uf	4.38	Push-Pull RESET	688Kx
G690H400T71U	G690H400T71Uf	4.00	Push-Pull RESET	688Jx
G690H308T71U	G690H308T71Uf	3.08	Push-Pull RESET	688Ix
G690H293T71U	G690H293T71Uf	2.93	Push-Pull RESET	688Hx
G690H263T71U	G690H263T71Uf	2.63	Push-Pull RESET	688Gx
G690L463T71U	G690L463T71Uf	4.63	Push-Pull	688Fx
G690L438T71U	G690L438T71Uf	4.38	Push-Pull	688Ex
G690L400T71U	G690L400T71Uf	4.00	Push-Pull	688Dx
G690L308T71U	G690L308T71Uf	3.08	Push-Pull	688Cx
G690L293T71U	G690L293T71Uf	2.93	Push-Pull	688Bx
G690L263T71U	G690L263T71Uf	2.63	Push-Pull	688Ax

Note: T7: SOT-23

Not all product options are ready for mass production, please contact factory for availability.

Selector Guide

ORDER NUMBER	ORDER NUMBER (Pb free)	RESET THRESHOLD (V)	OUTPUT TYPE	TOP MARK
				SOT-23
G691L463T72U	G691L463T72Uf	4.63	Open-Drain	687Fx
G691L438T72U	G691L438T72Uf	4.38	Open-Drain	687Ex
G691L400T72U	G691L400T72Uf	4.00	Open-Drain	687Dx
G691L308T72U	G691L308T72Uf	3.08	Open-Drain	687Cx
G691L293T72U	G691L293T72Uf	2.93	Open-Drain	687Bx
G691L263T72U	G691L263T72Uf	2.63	Open-Drain	687Ax
G690H463T72U	G690H463T72Uf	4.63	Push-Pull RESET	686Lx
G690H438T72U	G690H438T72Uf	4.38	Push-Pull RESET	686Kx
G690H400T72U	G690H400T72Uf	4.00	Push-Pull RESET	686Jx
G690H308T72U	G690H308T72Uf	3.08	Push-Pull RESET	686Ix
G690H293T72U	G690H293T72Uf	2.93	Push-Pull RESET	686Hx
G690H263T72U	G690H263T72Uf	2.63	Push-Pull RESET	686Gx
G690L463T72U	G690L463T72Uf	4.63	Push-Pull	686Fx
G690L438T72U	G690L438T72Uf	4.38	Push-Pull	686Ex
G690L400T72U	G690L400T72Uf	4.00	Push-Pull	686Dx
G690L308T72U	G690L308T72Uf	3.08	Push-Pull	686Cx
G690L293T72U	G690L293T72Uf	2.93	Push-Pull	686Bx
G690L263T72U	G690L263T72Uf	2.63	Push-Pull	686Ax

Note: T7: SOT-23

Not all product options are ready for mass production, please contact factory for availability.

Selector Guide

ORDER NUMBER	ORDER NUMBER (Pb free)	RESET THRESHOLD (V)	OUTPUT TYPE	TOP MARK
				SOT-23
G691L463T73U	G691L463T73Uf	4.63	Open-Drain	691Fx
G691L438T73U	G691L438T73Uf	4.38	Open-Drain	691Ex
G691L400T73U	G691L400T73Uf	4.00	Open-Drain	691Dx
G691L308T73U	G691L308T73Uf	3.08	Open-Drain	691Cx
G691L293T73U	G691L293T73Uf	2.93	Open-Drain	691Bx
G691L263T73U	G691L263T73Uf	2.63	Open-Drain	691Ax
G690H463T73U	G690H463T73Uf	4.63	Push-Pull RESET	690Lx
G690H438T73U	G690H438T73Uf	4.38	Push-Pull RESET	690Kx
G690H400T73U	G690H400T73Uf	4.00	Push-Pull RESET	690Jx
G690H308T73U	G690H308T73Uf	3.08	Push-Pull RESET	690Ix
G690H293T73U	G690H293T73Uf	2.93	Push-Pull RESET	690Hx
G690H263T73U	G690H263T73Uf	2.63	Push-Pull RESET	690Gx
G690L463T73U	G690L463T73Uf	4.63	Push-Pull	690Fx
G690L438T73U	G690L438T73Uf	4.38	Push-Pull	690Ex
G690L400T73U	G690L400T73Uf	4.00	Push-Pull	690Dx
G690L308T73U	G690L308T73Uf	3.08	Push-Pull	690Cx
G690L293T73U	G690L293T73Uf	2.93	Push-Pull	690Bx
G690L263T73U	G690L263T73Uf	2.63	Push-Pull	690Ax

Note: T7: SOT-23

Not all product options are ready for mass production, please contact factory for availability.

Absolute Maximum Ratings

Terminal Voltage (with respect to GND)
V_{CC}.....-0.3V to 6.0V
RESET, $\overline{RESET}$ (push-pull).....-0.3V to (V_{CC} + 0.3V)
$\overline{RESET}$ (open drain).....-0.3V to 6.0V
Input Current, V_{CC} 20mA
Output Current, RESET, $\overline{RESET}$ 20mA
Operating Temperature Range .....-40°C to 105°C
Storage Temperature Range.....-65°C to 150°C
Reflow Temperature (soldering, 10sec) .....260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{CC} = full range, T_A = -40°C to 105°C, unless otherwise noted. Typical values are at T_A = 25°C, V_{CC} = 5V for 463/438/400 versions, V_{CC}= 3.3V for 308/293 versions, and V_{CC} = 3V for 263 version.) (Note 1)

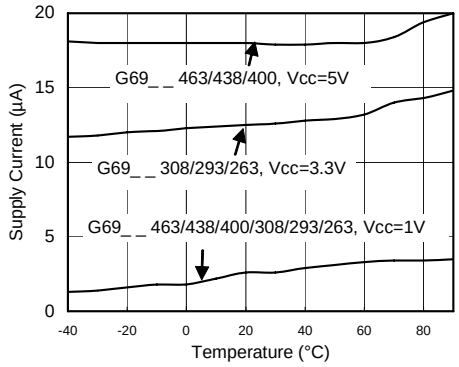
PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
V_{CC} Range		T_A = 0°C +70°C	1.0	---	5.5	V
		T_A = -40°C +105°C	1.2	---	5.5	
Supply Current (SOT-23)	I_{CC}	V_{CC}<5.5V, G69_ _463/438/400_	---	22	30	µA
		V_{CC}<3.6V, G69_ _308/293/263_	---	10	23	
Reset Threshold	V_{TH}	G69_ _463_	4.56	4.63	4.70	V
		G69_ _438_	4.31	4.38	4.45	
		G69_ _400_	3.93	4.00	4.06	
		G69_ _308_	3.04	3.08	3.11	
		G69_ _293_	2.89	2.93	2.96	
		G69_ _263_	2.59	2.63	2.66	
Reset Threshold Tempco			---	40	---	ppm/°C
V_{CC} to Reset Delay (Note 2)		V_{CC} = V_{TH} to (V_{TH} – 100mV)	---	7	---	µs
Reset Active Timeout Period		V_{CC} = V_{TH} max, G69_ _463/438/400	280	---	640	ms
		V_{CC} = V_{TH} max, G69_ _308/293/263	150	---	550	
$\overline{RESET}$ Output Current Low (push-pull active low, and open-drain active-low, G690L and G691L)	I_{OL}	V_{CC} = 2.5V, $V_{\overline{RESET}}$ = 0.5V	8	---	---	mA
$\overline{RESET}$ Output Current High (push-pull active low, G690L)	I_{OH}	V_{CC} = 5V, $V_{\overline{RESET}}$ = 4.5V, G690L463/438/400	4.5	---	---	mA
		V_{CC} = 3.3V, $V_{\overline{RESET}}$ = 2.8V, G690L308/293	3	---	---	
		V_{CC} = 3V, $V_{\overline{RESET}}$ = 2.5V, G690L263	2	---	---	
RESET Output Current Low (push-pull active high, G690H)	I_{OL}	V_{CC} = 5V, V_{RESET} = 0.5V, G690H463/438/400	16	---	---	mA
		V_{CC} = 3.3V, V_{RESET} = 0.5V, G690H308/293	12	---	---	
		V_{CC} = 3V, V_{RESET} = 0.5V, G690H263	10	---	---	
RESET Output Current High (push-pull active high, G690H)	I_{OH}	V_{CC} = 2.5V, V_{RESET} = 2V	2	---	---	mA
$\overline{RESET}$ Open-Drain Output Leakage Current (G691L)		V_{CC} > V_{TH}, $\overline{RESET}$ deasserted	---	---	1	µA

Note 1: Production testing done at T_A = +25°C; limits over temperature guaranteed by design.
Note 2: $\overline{RESET}$ output is for G690L/G691L; While RESET output is for G690H.

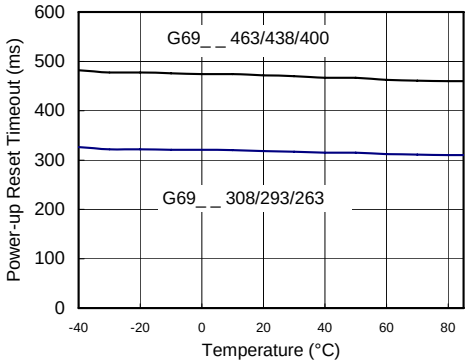
Typical Operating Characteristics

(V_{CC} = full range, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{CC} = 5V for 463/438/400 versions, V_{CC}= 3.3V for 308/293 versions, and V_{CC} = 3V for 263 version.)

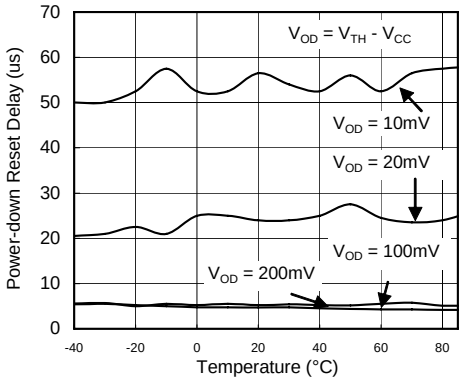
Supply Current vs.Temperature (No Load)



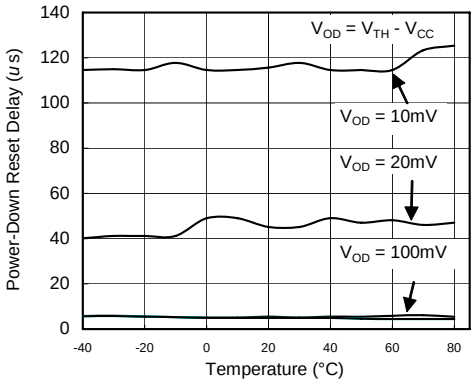
Power-up Reset Timeout vs. Temperature



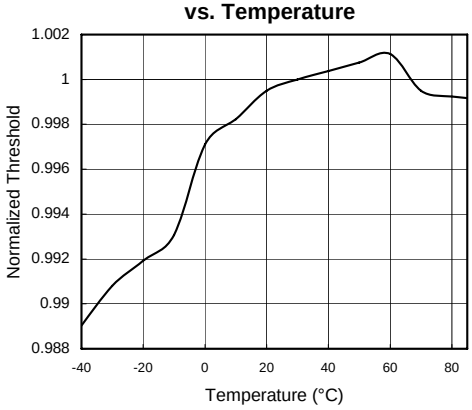
Power-down Reset Delay vs. Temperature (G69_ _308/293/263)



Power-down Reset Delay vs. Temperature (G68_ _463/438/400)

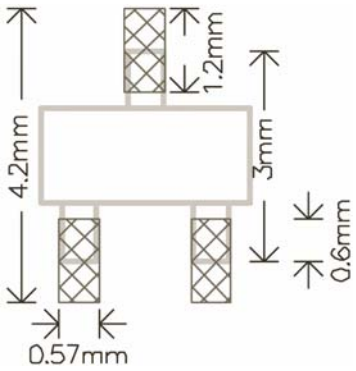


Normalized Reset Threshold vs. Temperature



Recommended Minimum Footprint

SOT-23



Pin Description

PIN	NAME	FUNCTION
1	GND	Ground
2	(G691L/G690L)	$\overline{\text{RESET}}$ Output remains low while V_{CC} is below the reset threshold, and for at least 140ms after V_{CC} rises above the reset threshold.
	RESET (G690H)	RESET Output remains high while V_{CC} is below the reset threshold, and for at least 140ms after V_{CC} rises above the reset threshold.
3	V_{CC}	Supply Voltage (+5V, +3.3V, +3.0V)

Detailed Description

A microprocessor's (µP's) reset input starts the µP in a known state. The G691L/G690L/G690H assert reset to prevent code-execution errors during power-up, power-down, or brownout conditions. They assert a reset signal whenever the V_{CC} supply voltage declines below a preset threshold, keeping it asserted for at least 140ms after V_{CC} has risen above the reset threshold. The G691L uses an open-drain output, and the G690L/G690H have a push-pull output stage. Connect a pull-up resistor on the G691L's $\overline{\text{RESET}}$ output to any supply between 0 and 5.5V.

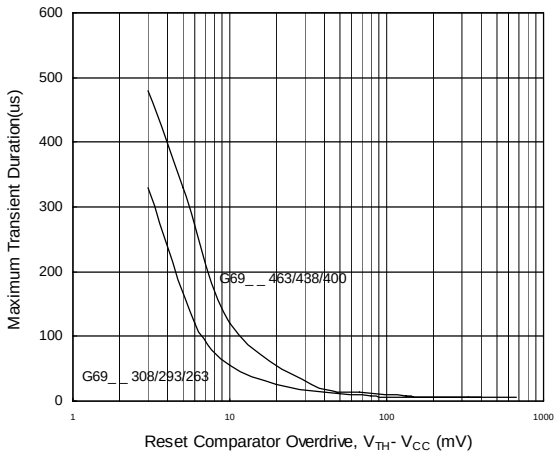


Figure 1. Maximum Transient Duration Without Causing a Reset Pulse vs. Reset Comparator Overdrive

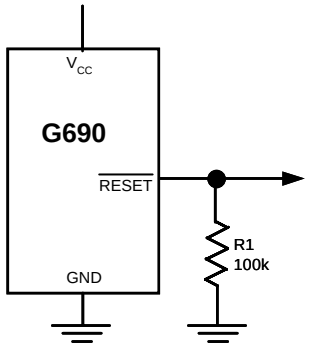


Figure 2. $\overline{\text{RESET}}$ Valid to V_{CC} = Ground Circuit

Applications Information

Negative-Going V_{CC} Transients

In addition to issuing a reset to the µP during power-up, power-down, and brownout conditions, the G691L/G690H/G690L are relatively immune to short-duration negative-going V_{CC} transients (glitches).

Figure 1 shows typical transient duration vs. reset comparator overdrive, for which the G691L/G690H/G690L do not generate a reset pulse. The graph was generated using a negative-going pulse applied to V_{CC}, starting 0.5V above the actual reset threshold and ending below it by the magnitude indicated (reset comparator overdrive). The graph indicates the maximum pulse width a negative-going V_{CC} transient can have without causing a reset pulse. As the magnitude of the transient increases (goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, for the G69_ _463 and G69_ _438, a V_{CC} transient that goes 100mV below the reset threshold and lasts 7µs or less will not cause a reset pulse. A 0.1µF bypass capacitor mounted as close as possible to the V_{CC} pin provides additional transient immunity.

Ensuring a Valid Reset Output Down to V_{CC} = 0

When V_{CC} falls below 1V, the G690 $\overline{\text{RESET}}$ output no longer sinks current—it becomes an open circuit. Therefore, high-impedance CMOS logic inputs connected to $\overline{\text{RESET}}$ can drift to undetermined voltages. This presents no problem in most applications since most µP and other circuitry is inoperative with VCC below 1V. However, in applications where $\overline{\text{RESET}}$ must be valid down to 0V, adding a pull-down resistor to $\overline{\text{RESET}}$ causes any stray leakage currents to flow to ground, holding $\overline{\text{RESET}}$ low (Figure 2). R1's value is not critical; 100kΩ is large enough not to load $\overline{\text{RESET}}$ and small enough to pull $\overline{\text{RESET}}$ to ground.

A 100kΩ pull-up resistor to VCC is also recommended for the G691L if $\overline{\text{RESET}}$ is required to remain valid for V_{CC} < 1V.

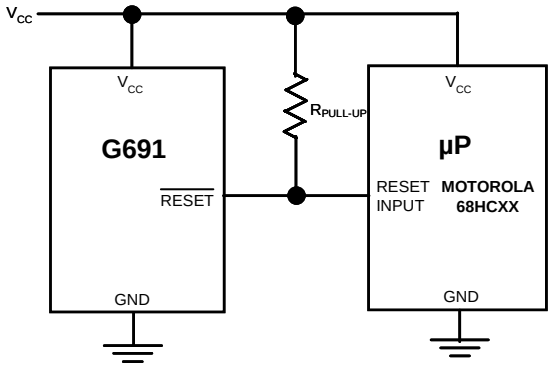


Figure 3. Interfacing to µPs with Bidirectional Reset I/O

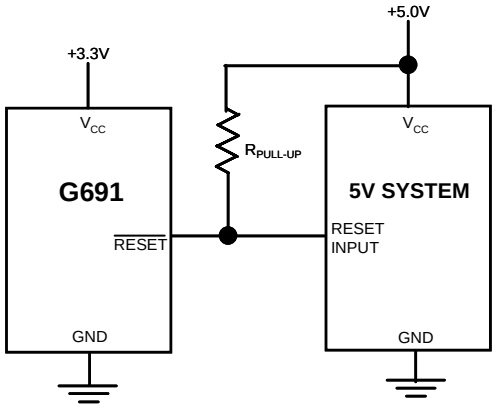


Figure 4. G691L Open-Drain $\overline{\text{RESET}}$ Output Allows Use with Multiple Supplies

Interfacing to µPs with Bidirectional Reset Pins

Since the $\overline{\text{RESET}}$ output on the G691L is open drain, this device interfaces easily with µPs that have bidirectional reset pins, such as the Motorola 68HC11. Connecting the µP supervisor's $\overline{\text{RESET}}$ output directly to the microcontroller's (µC's) $\overline{\text{RESET}}$ pin with a single pull-up resistor allows either device to assert reset (Figure 3).

G691L Open-Drain $\overline{\text{RESET}}$ Output Allows Use with Multiple Supplies

Generally, the pull-up connected to the G691L will connect to the supply voltage that is being monitored at the IC's V_{CC} pin. However, some systems may use the open-drain output to level-shift from the monitored supply to reset circuitry powered by some other supply (Figure 4). Note that as the G691L's V_{CC} decreases below 1V, so does the IC's ability to sink current at $\overline{\text{RESET}}$. Also, with any pull-up, $\overline{\text{RESET}}$ will be pulled high as VCC decays toward 0. The voltage where this occurs depends on the pull-up resistor value and the voltage to which it is connected.

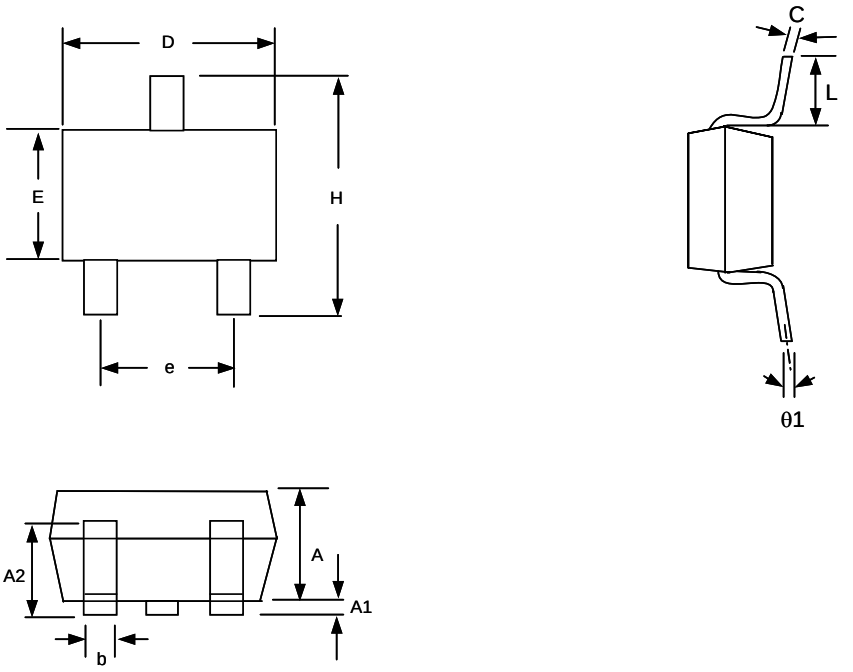
Benefits of Highly Accurate Reset Threshold

Most µP supervisor ICs have reset threshold voltages between 5% and 10% below the value of nominal supply voltages. This ensures a reset will not occur within 5% of the nominal supply, but will occur when the supply is 10% below nominal.

When using ICs rated at only the nominal supply ±5%, this leaves a zone of uncertainty where the supply is between 5% and 10% low, and where the reset may or may not be asserted.

The G69_ _463/G69_ _308 use highly accurate circuitry to ensure that reset is asserted close to the 5% limit, and long before the supply has declined to 10% below nominal.

Package Information

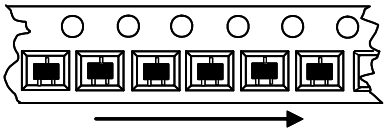


SOT-23 (T7) Package

Note:
1.Package body sizes exclude mold flash protrusions or gate burrs
2.Tolerance ±0.1000 mm (4mil) unless otherwise specified
3.Coplanarity: 0.1000mm
4.Dimension L is measured in gage plane

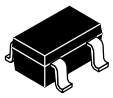
SYMBOL	DIMENSIONS IN MILLIMETER		
	MIN	NOM	MAX
A	1.00	1.10	1.30
A1	0.00	-----	0.10
A2	0.70	0.80	0.90
b	0.35	0.40	0.50
C	0.10	0.15	0.25
D	2.70	2.90	3.10
E	1.40	1.60	1.80
e	-----	1.90(TYP)	-----
H	2.60	2.80	3.00
L	0.37	------	-----
θ1	1º	5º	9º

Taping Specification



Feed Direction
SOT-23 Package Orientation

PACKAGE	Q'TY/REEL
SOT-23	3,000 ea



HIGH-EFFICIENCY, SOT23 STEP-DOWN, DC-DC CONVERTER

FEATURES

- **High Efficiency Synchronous Step-Down Converter With up to 95% Efficiency**
- **2.5 V to 6.0 V Input Voltage Range**
- **Adjustable Output Voltage Range From 0.7 V to V_I**
- **Fixed Output Voltage Options Available**
- **Up to 300 mA Output Current**
- **1 MHz Fixed Frequency PWM Operation**
- **Highest Efficiency Over Wide Load Current Range Due to Power Save Mode**
- **15-µA Typical Quiescent Current**
- **Soft Start**
- **100% Duty Cycle Low-Dropout Operation**
- **Dynamic Output-Voltage Positioning**
- **Available in a Tiny 5-Pin SOT23 Package**

APPLICATIONS

- **PDAs and Pocket PC**
- **Cellular Phones, Smart Phones**
- **Low Power DSP Supply**
- **Digital Cameras**
- **Portable Media Players**
- **Portable Equipment**

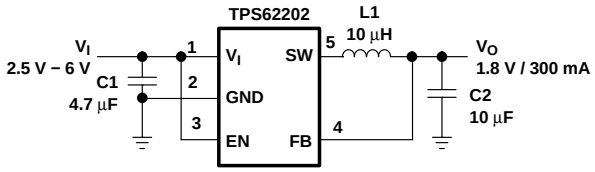
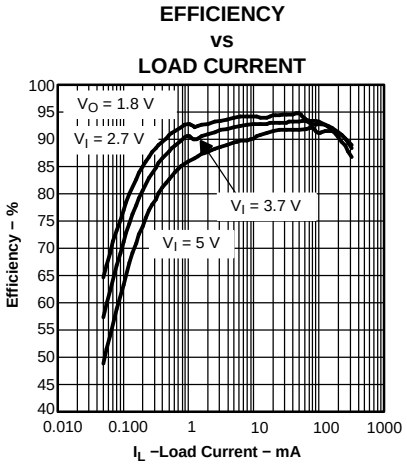


Figure 1. Typical Application (Fixed Output Voltage Version)

DESCRIPTION

The TPS6220x devices are a family of high-efficiency synchronous step-down converters ideally suited for portable systems powered by 1-cell Li-Ion or 3-cell NiMH/NiCd batteries. The devices are also suitable to operate from a standard 3.3-V or 5-V voltage rail.

With an output voltage range of 6.0 V down to 0.7 V and up to 300 mA output current, the devices are ideal to power low voltage DSPs and processors used in PDAs, pocket PCs, and smart phones. Under nominal load current, the devices operate with a fixed switching frequency of typically 1 MHz. At light load currents, the part enters the power save mode operation; the switching frequency is reduced and the quiescent current is typically only 15 µA; therefore it achieves the highest efficiency over the entire load current range. The TPS6220x needs only three small external components. Together with the tiny SOT23 package, a minimum system solution size can be achieved. An advanced fast response voltage mode control scheme achieves superior line and load regulation with small ceramic input and output capacitors.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

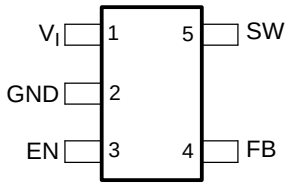
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION (1)

T_A	OUTPUT VOLTAGE	SOT23 PACKAGE	SYMBOL
-40°C to 85°C	Adjustable	TPS62200DBV	PHKI
	1.2 V	TPS62207DBV	PJGI
	1.5 V	TPS62201DBV	PHLI
	1.6 V	TPS62204DBV	PHSI
	1.8 V	TPS62202DBV	PHMI
	1.875 V	TPS62208DBV	ALW
	2.5 V	TPS62205DBV	PHTI
	3.3 V	TPS62203DBV	PHNI

(1) The DBV package is available in tape and reel. Add R suffix (DBVR) to order quantities of 3000 parts. Add T suffix (DBVT) to order quantities of 250 parts

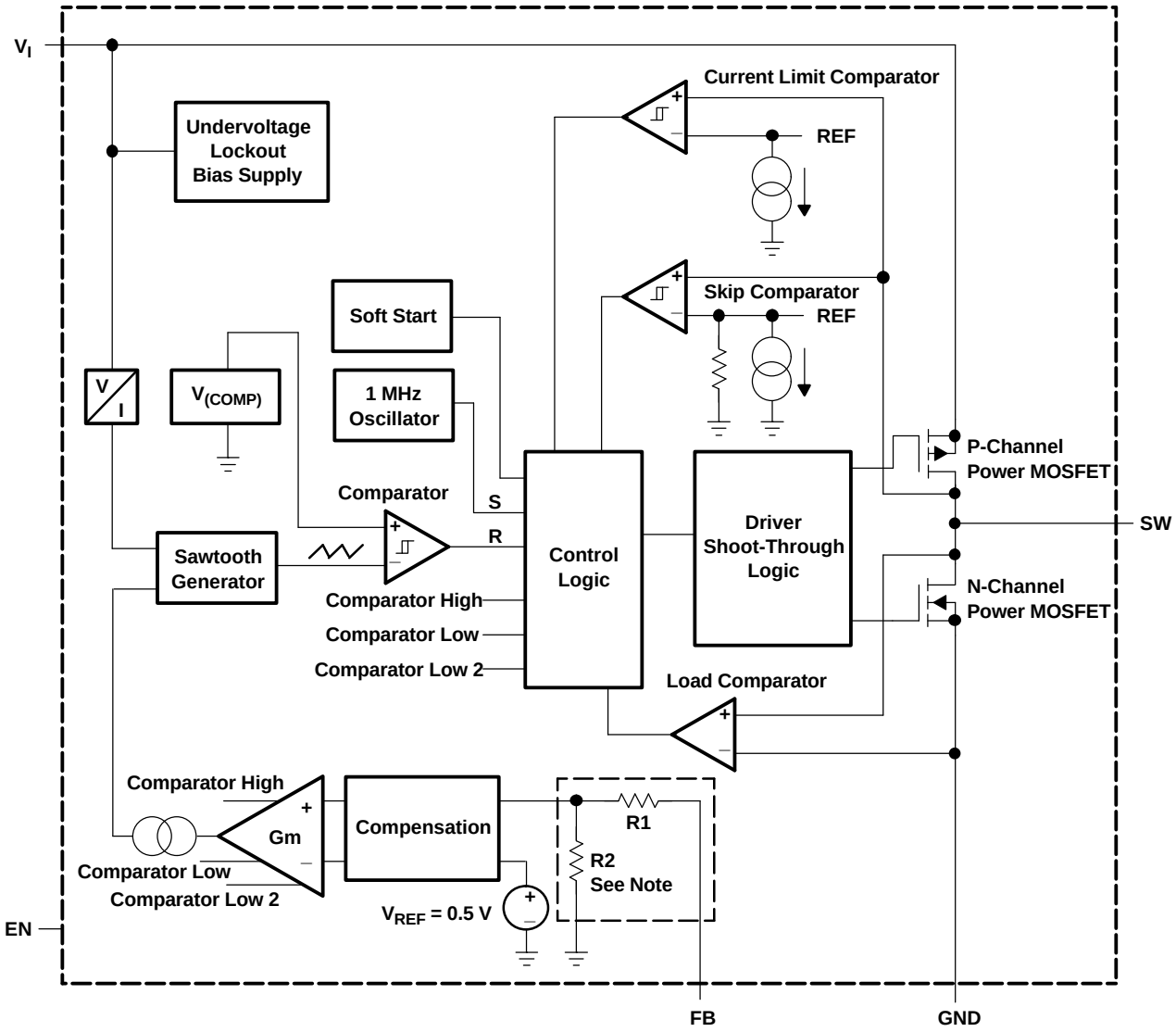
DBV PACKAGE
(TOP VIEW)



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
EN	3	I	This is the enable pin of the device. Pulling this pin to ground forces the device into shutdown mode. Pulling this pin to Vin enables the device. This pin must not be left floating and must be terminated.
FB	4	I	This is the feedback pin of the device. Connect this pin directly to the output if the fixed output voltage version is used. For the adjustable version an external resistor divider is connected to this pin. The internal voltage divider is disabled for the adjustable version.
GND	2		Ground
SW	5	I/O	Connect the inductor to this pin. This pin is the switch pin and is connected to the internal MOSFET switches.
V_I	1	I	Supply voltage pin

FUNCTIONAL BLOCK DIAGRAM



#IMPLIED. For the adjustable version (TPS62200) the internal feedback divider is disabled and the FB pin is directly connected to the internal GM amplifier

DETAILED DESCRIPTION

OPERATION

The TPS6220x is a synchronous step-down converter operating with typically 1MHz fixed frequency pulse width modulation (PWM) at moderate to heavy load currents and in power save mode operating with pulse frequency modulation (PFM) at light load currents.

During PWM operation the converter uses a unique fast response, voltage mode, controller scheme with input voltage feed forward. This achieves good line and load regulation and allows the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal (S), the P-channel MOSFET switch is turned on, and the inductor current ramps up until the comparator trips and the control logic turns off the switch. The current limit comparator also turns off the switch in case the current limit of the P-channel switch is exceeded. Then the N-channel rectifier switch is turned on and the inductor current ramps down. The next cycle is initiated by the clock signal again turning off the N-channel rectifier and turning on the P-channel switch.

DETAILED DESCRIPTION (continued)

The GM amplifier and input voltage determines the rise time of the Sawtooth generator; therefore any change in input voltage or output voltage directly controls the duty cycle of the converter. This gives a very good line and load transient regulation.

POWER SAVE MODE OPERATION

As the load current decreases, the converter enters the power save mode operation. During power save mode, the converter operates with reduced switching frequency in PFM mode and with a minimum quiescent current to maintain high efficiency.

Two conditions allow the converter to enter the power save mode operation. One is when the converter detects the discontinuous conduction mode. The other is when the peak switch current in the P-channel switch goes below the skip current limit. The typical skip current limit can be calculated as

$$I_{skip} \leq 66\ mA + \frac{Vin}{160\ \Omega}$$

During the power save mode the output voltage is monitored with the comparator by the thresholds comp low and comp high. As the output voltage falls below the comp low threshold set to typically 0.8% above Vout nominal, the P-channel switch turns on. The P-channel switch is turned off as the peak switch current is reached. The typical peak switch current can be calculated:

$$I_{peak} = 66\ mA + \frac{Vin}{80\ \Omega}$$

The N-channel rectifier is turned on and the inductor current ramps down. As the inductor current approaches zero the N-channel rectifier is turned off and the P-channel switch is turned on again, starting the next pulse. The converter continues these pulses until the comp high threshold (set to typically 1.6% above Vout nominal) is reached. The converter enters a sleep mode, reducing the quiescent current to a minimum. The converter wakes up again as the output voltage falls below the comp low threshold again. This control method reduces the quiescent current typically to 15 µA and reduces the switching frequency to a minimum, thereby achieving the high converter efficiency. Setting the skip current thresholds to typically 0.8% and 1.6% above the nominal output voltage at light load current results in a dynamic output voltage achieving lower absolute voltage drops during heavy load transient changes. This allows the converter to operate with a small output capacitor of just 10 µF and still have a low absolute voltage drop during heavy load transient changes. Refer to Figure 2 for detailed operation of the power save mode.

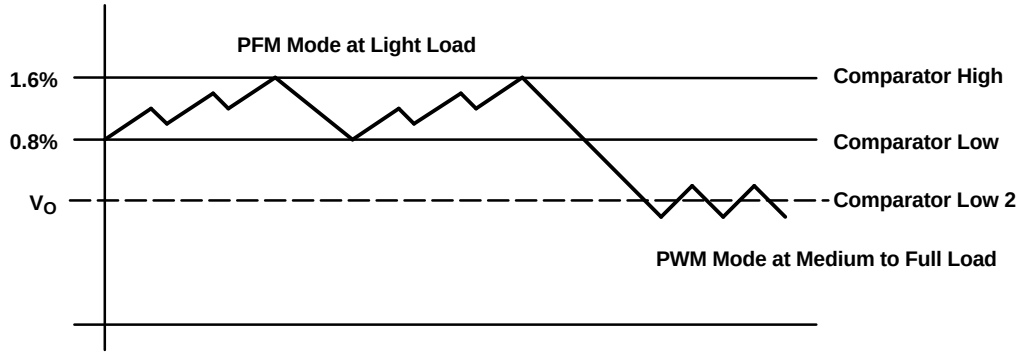


Figure 2. Power Save Mode Thresholds and Dynamic Voltage Positioning

The converter enters the fixed frequency PWM mode again as soon as the output voltage falls below the comp low 2 threshold.

DETAILED DESCRIPTION (continued)

DYNAMIC VOLTAGE POSITIONING

As described in the power save mode operation sections and as detailed in Figure 2, the output voltage is typically 0.8% above the nominal output voltage at light load currents, as the device is in power save mode. This gives additional headroom for the voltage drop during a load transient from light load to full load. During a load transient from full load to light load, the voltage overshoot is also minimized due to active regulation turning on the N-channel rectifier switch.

SOFT START

The TPS6220x has an internal soft start circuit that limits the inrush current during start-up. This prevents possible voltage drops of the input voltage in case a battery or a high impedance power source is connected to the input of the TPS6220x.

The soft start is implemented as a digital circuit increasing the switch current in steps of typically 60 mA,120 mA, 240 mA and then the typical switch current limit of 480 mA. Therefore the start-up time mainly depends on the output capacitor and load current. Typical start-up time with 10 µF output capacitor and 200 mA load current is 800 µs.

LOW DROPOUT OPERATION 100% DUTY CYCLE

The TPS6220x offers a low input to output voltage difference, while still maintaining operation with the 100% duty cycle mode. In this mode, the P-channel switch is constantly turned on. This is particularly useful in battery powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain regulation, depending on the load current and output voltage, can be calculated as

$$Vin_{min} = Vout_{max} + Iout_{max} \times \left(r_{ds}(ON)_{max} + R_L \right)$$

$Iout_{max}$ = maximum output current plus inductor ripple current
$r_{ds}(ON)_{max}$ = maximum P-channel switch $r_{ds}(ON)$
R_L = DC resistance of the inductor
$Vout_{max}$ = nominal output voltage plus maximum output voltage tolerance

ENABLE

Pulling the enable low forces the part into shutdown, with a shutdown quiescent current of typically 0.1 µA. In this mode, the P-channel switch and N-channel rectifier are turned off, the internal resistor feedback divider is disconnected, and the whole device is in shutdown mode. If an output voltage, which could be an external voltage source or super cap, is present during shutdown, the reverse leakage current is specified under electrical characteristics. For proper operation the enable pin must be terminated and must not be left floating.

Pulling the enable high starts up the TPS6220x with the soft start as previously described.

UNDERVOLTAGE LOCKOUT

The undervoltage lockout circuit prevents the device from misoperation at low input voltages. It prevents the converter from turning on the switch or rectifier MOSFET under undefined conditions.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature (unless otherwise noted) (1)

	UNIT
Supply voltages, V_I (2)	-0.3 V to 7.0 V
Voltages on pins SW, EN, FB (2)	-0.3 V to V_{CC} +0.3 V
Continuous power dissipation, P_D	See Dissipation Rating Table
Operating junction temperature range, T_J	-40°C to 150°C
Storage temperature, T_{stg}	-65°C to 150°C
Lead temperature (soldering, 10 sec)	260°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$R_{\theta JA}$	$T_A \le 25°C$ POWER RATING	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DBV	250°/W	400 mW	220 mW	160 mW

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage, V_I	2.5		6.0	V
Output voltage range for adjustable output voltage version, V_O	0.7		V_I	V
Output current, I_O			300	mA
Inductor, L (1)	4.7	10		µH
Input capacitor, C_I (1)		4.7		µF
Output capacitor, C_O (1)		10		µF
Operating ambient temperature, T_A	40		85	°C
Operating junction temperature, T_J	40		125	°C

(1) See the application section for further information.

ELECTRICAL CHARACTERISTICS

V_I = 3.6 V, V_O = 1.8 V, I_O = 200 mA, EN = VIN, T_A = -40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_I	Input voltage range		2.5		6.0	V
I_Q	Operating quiescent current	I_O = 0 mA, Device is not switching		15	30	µA
	Shutdown supply current	EN = GND		0.1	1	µA
	Undervoltage lockout threshold		1.5		2.0	V
ENABLE						
$V_{(EN)}$	EN high level input voltage		1.3			V
	EN low level input voltage				0.4	V
$I_{(EN)}$	EN input bias current	EN = GND or VIN		0.01	0.1	µA
POWER SWITCH						
r_{ds}(ON)	P-channel MOSFET on-resistance	$V_{IN} = V_{GS}$ = 3.6 V		530	690	mΩ
		$V_{IN} = V_{GS}$ = 2.5 V		670	850	
	N-channel MOSFET on-resistance	$V_{IN} = V_{GS}$ = 3.6 V		430	540	mΩ
		$V_{IN} = V_{GS}$ = 2.5 V		530	660	

ELECTRICAL CHARACTERISTICS (continued)

V_I = 3.6 V, V_O = 1.8 V, I_O = 200 mA, EN = VIN, T_A = -40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
$I_{lkg\_(P)}$	P-channel leakage current		V_{DS} = 6.0 V		0.1	1	µA
$I_{lkg\_(N)}$	N-channel leakage current		V_{DS} = 6.0 V		0.1	1	µA
$I_{(LIM)}$	P-channel current limit		2.5 V < Vin < 6.0 V	380	480	670	mA
OSCILLATOR							
f_S	Switching frequency			650	1000	1500	kHz
OUTPUT							
V_O	Adjustable output voltage range	TPS62200		0.7		V_{IN}	V
V_{ref}	Reference voltage				0.5		V
	Feedback voltage (1)	TPS62200	V_I = 3.6 V to 6.0 V, I_O = 0 mA	0%		3%	
		Adjustable	V_I = 3.6 V to 6.0 V, 0 mA≤ I_O ≤ 300 mA	-3%		3%	
V_O	Fixed output voltage(1)	TPS62207	V_I = 2.5 V to 6.0 V, I_O = 0 mA	0%		3%	
		1.2 V	V_I = 2.5 V to 6.0 V, 0 mA≤ I_O ≤ 300 mA	0%		3%	
		TPS62201	V_I = 2.5 V to 6.0 V, I_O = 0 mA	0%		3%	
		1.5 V	V_I = 2.5 V to 6.0 V, 0 mA≤ I_O ≤ 300 mA	-3%		3%	
		TPS62204	V_I = 2.5 V to 6.0 V, I_O = 0 mA	0%		3%	
		1.6 V	V_I = 2.5 V to 6.0 V, 0 mA≤ I_O ≤ 300 mA	-3%		3%	
		TPS62202	V_I = 2.5 V to 6.0 V, I_O = 0 mA	0%		3%	
		1.8 V	V_I = 2.5 V to 6.0 V, 0 mA≤ I_O ≤ 300 mA	-3%		3%	
		TPS62208	V_I = 2.5 V to 6.0 V, I_O = 0 mA	0%		3%	
		1.875 V	V_I = 2.5 V to 6.0 V, 0 mA≤ I_O ≤ 300 mA	-3%		3%	
		TPS62205	V_I = 2.7 V to 6.0 V, I_O = 0 mA	0%		3%	
		2.5 V	V_I = 2.7 V to 6.0 V, 0 mA≤ I_O ≤ 300 mA	-3%		3%	
		TPS62203	V_I = 3.6 V to 6.0 V, I_O = 0 mA	0%		3%	
		3.3 V	V_I = 3.6 V to 6.0 V, 0 mA≤ I_O ≤ 300 mA	-3%		3%	
	Line regulation		V_I = 2.5 V to 6.0 V, I_O = 10 mA		0.26		%/V
	Load regulation		I_O = 100 mA to 300 mA		0.0014		%/mA
I_{lkg}	Leakage current into SW pin		Vin > Vout, 0 V ≤ Vsw≤ Vin		0.1	1	µA
I_{lkg}(Rev)	Reverse leakage current into pin SW		Vin = open, EN=GND, V_{SW} = 6.0 V		0.1	1	µA

(1) For output voltages ≤ 1.2 V a 22 µF output capacitor value is required to achieve a maximum output voltage accuracy of 3% while operating in power save mode (PFM mode)

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURES
η	Efficiency	vs Load current	3,4,5
		vs Input voltage	6
I_Q	No load quiescent current	vs Input voltage	7
f_s	Switching frequency	vs Temperature	8
V_o	Output voltage	vs Output current	9
r_{ds}(on)	r_{ds}(on) - P-channel switch,	vs Input voltage	10
	r_{ds}(on) - N-Channel rectifier switch	vs Input voltage	11
	Line transient response		12
	Load transient response		13
	Power save mode operation		14
	Start-up		15

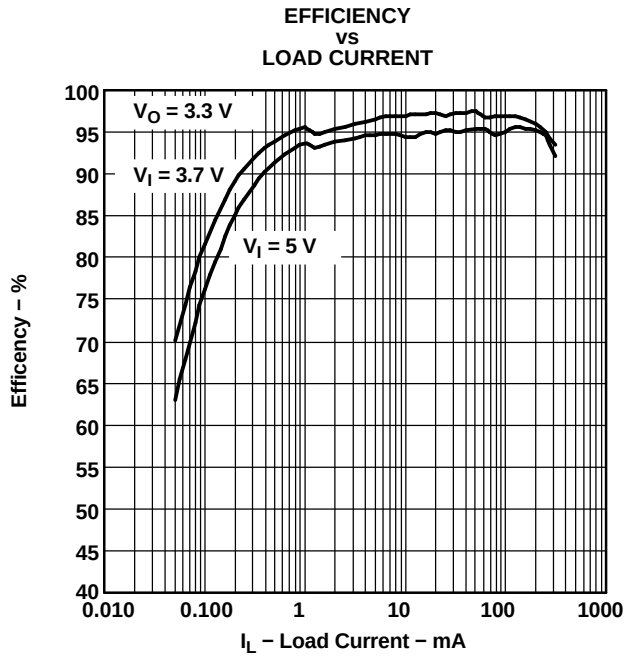


Figure 3.

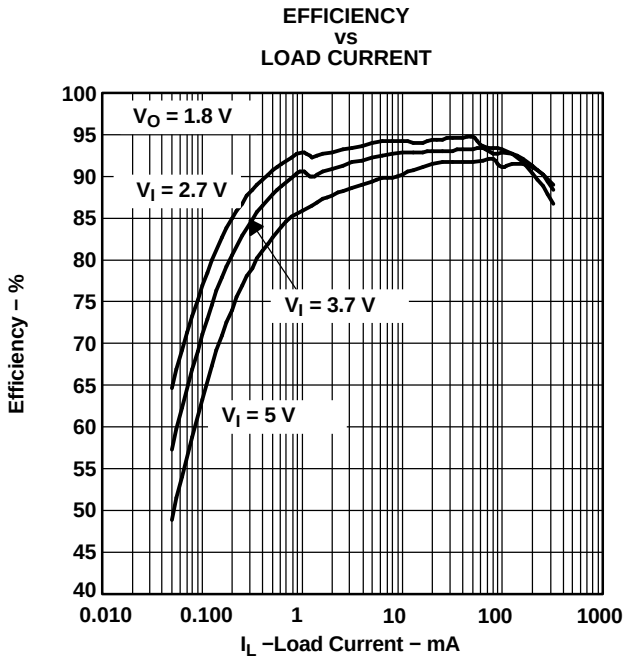


Figure 4.

TYPICAL CHARACTERISTICS (continued)

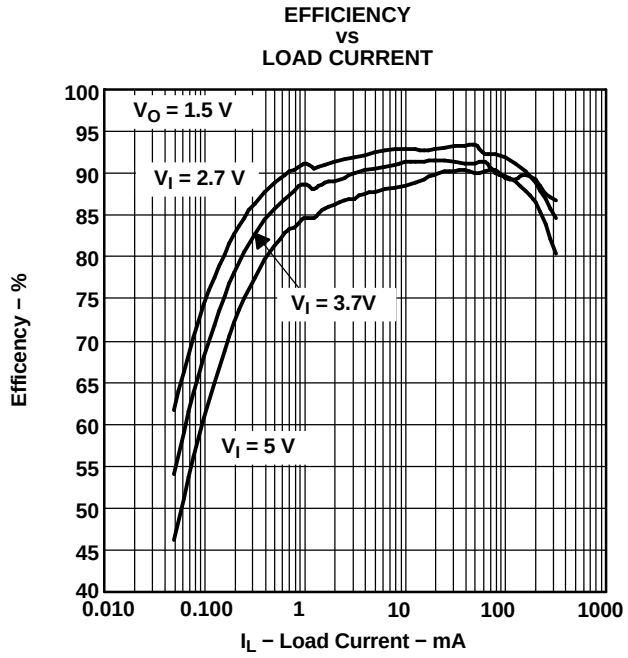


Figure 5.

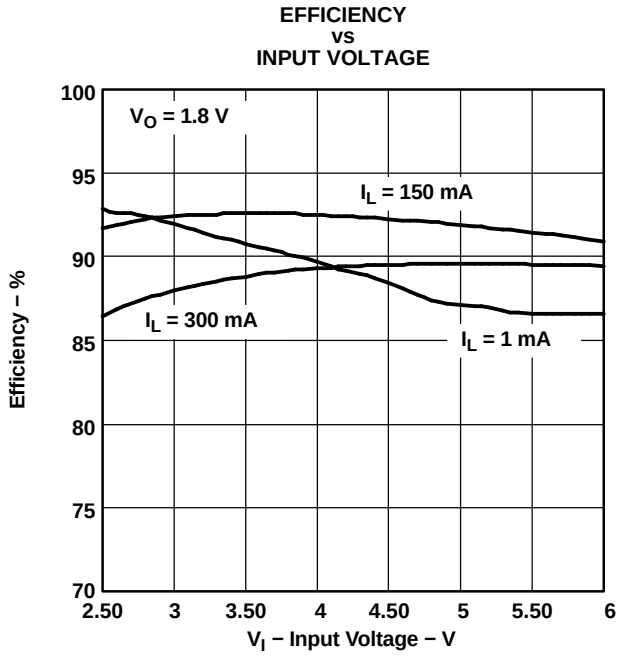


Figure 6.

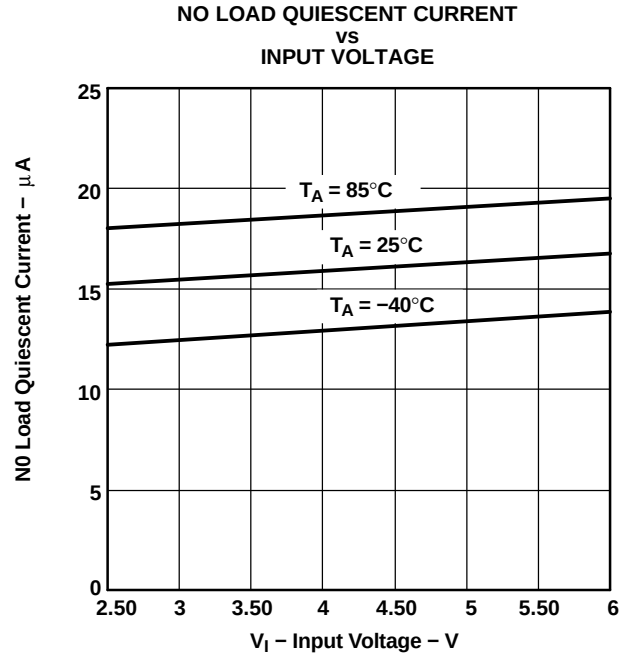


Figure 7.

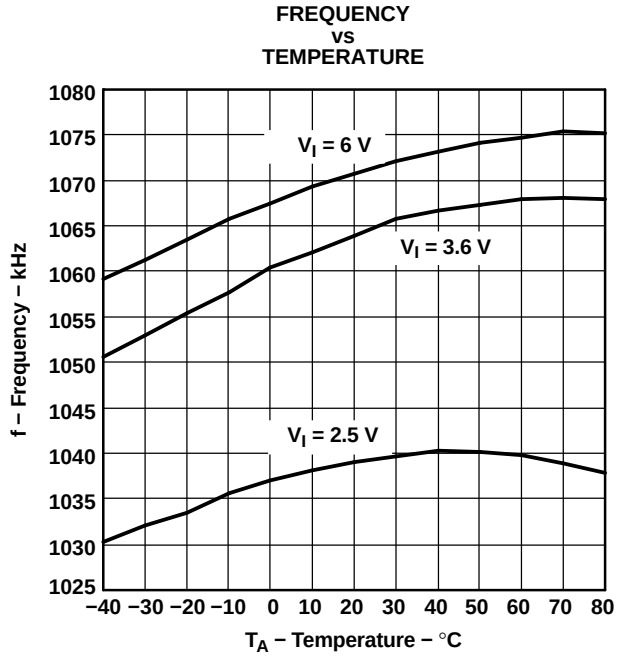


Figure 8.

TYPICAL CHARACTERISTICS (continued)

OUTPUT VOLTAGE
vs
OUTPUT CURRENT

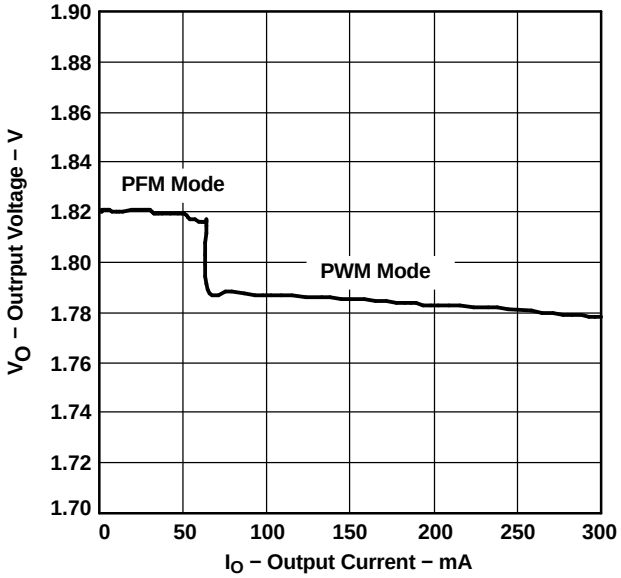


Figure 9.

r_{ds}(on) P-CHANNEL SWITCH
vs
INPUT VOLTAGE

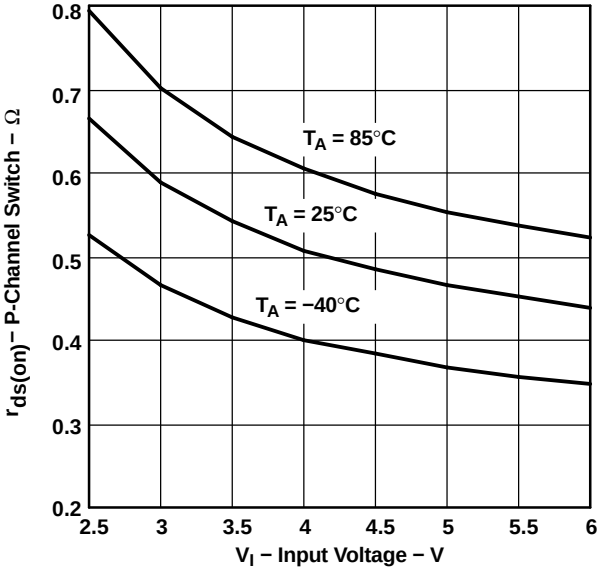


Figure 10.

r_{ds}(on) P-CHANNEL SWITCH
vs
INPUT VOLTAGE

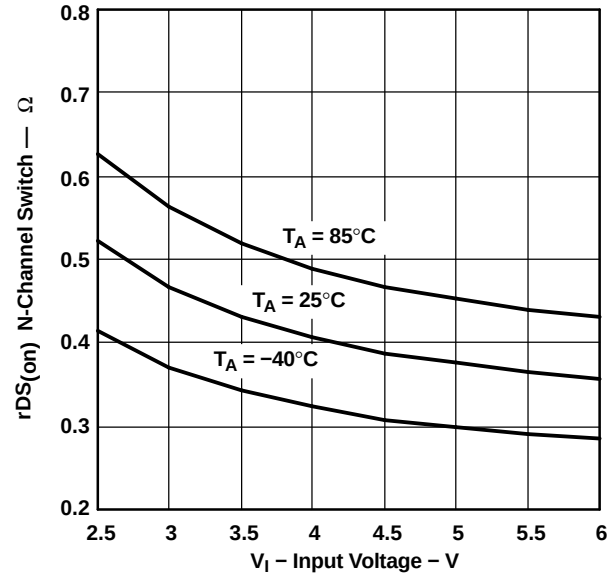


Figure 11.

LINE TRANSIENT RESPONSE

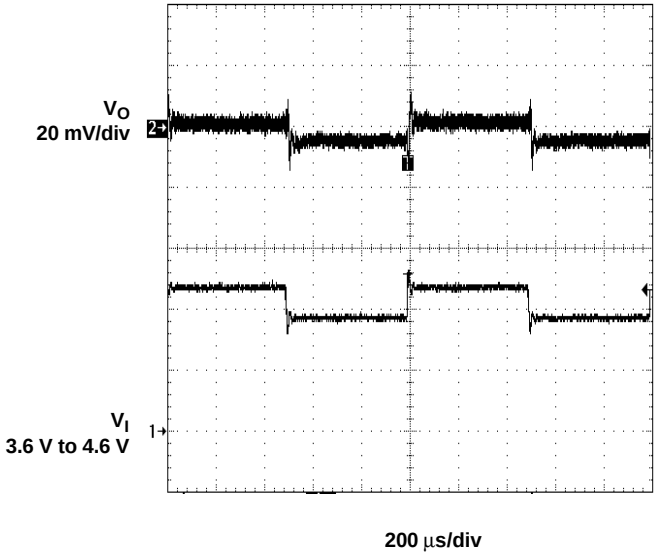


Figure 12.

TYPICAL CHARACTERISTICS (continued)

LOAD TRANSIENT RESPONSE

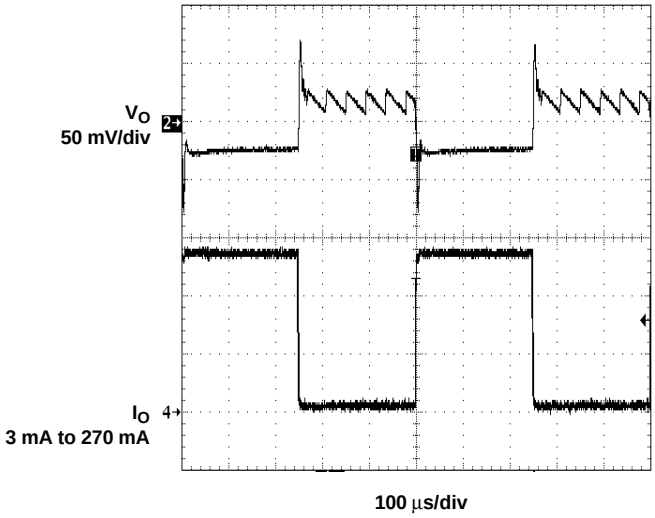


Figure 13.

POWER SAVE MODE OPERATION

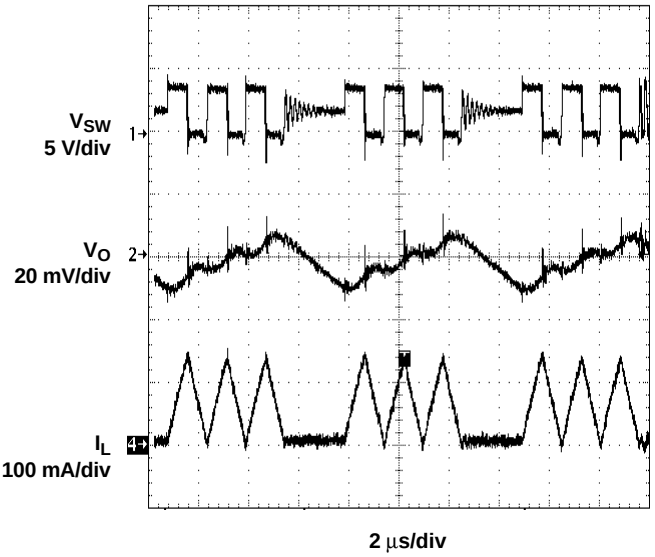


Figure 14.

START-UP

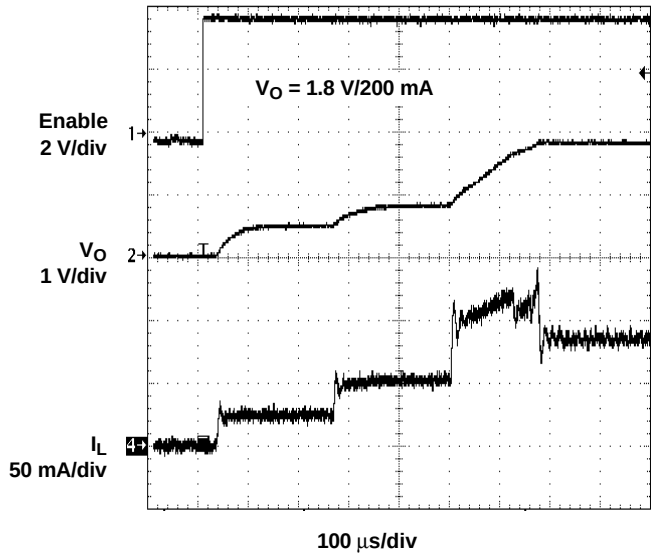


Figure 15.

APPLICATION INFORMATION

ADJUSTABLE OUTPUT VOLTAGE VERSION

When the adjustable output voltage version TPS62200 is used, the output voltage is set by the external resistor divider. See Figure 16.

The output voltage is calculated as

$$V_{out} = 0.5\ V \times \left(1 + \frac{R1}{R2}\right)$$

- R1 + R2 ≤ 1 MΩ and internal reference voltage V(ref)typ = 0.5 V

R1 + R2 should not be greater than 1 MΩ for reasons of stability. To keep the operating quiescent current to a minimum, the feedback resistor divider should have high impedance with R1+R2 ≤ 1 MΩ. Because of the high impedance and the low reference voltage of V_{ref} = 0.5 V, the noise on the feedback pin (FB) needs to be minimized. Using a capacitive divider C1 and C2 across the feedback resistors minimizes the noise at the feedback without degrading the line or load transient performance.

C1 and C2 should be selected as

$$C1 = \frac{1}{2 \times \pi \times 10\ kHz \times R1}$$

- R1 = upper resistor of voltage divider
- C1 = upper capacitor of voltage divider

For C1 a value should be chosen that comes closest to the calculated result.

$$C2 = \frac{R1}{R2} \times C1$$

- R2 = lower resistor of voltage divider
- C2 = lower capacitor of voltage divider

For C2 the selected capacitor value should always be selected larger than the calculated result. For example, in Figure 16 for C2, 100 pF are selected for a calculated result of C2 = 86.17 pF.

If quiescent current is not a key design parameter, C1 and C2 can be omitted, and a low-impedance feedback divider must be used with R1+R2 <100 kΩ. This design reduces the noise available on the feedback pin (FB) as well, but increases the overall quiescent current during operation.

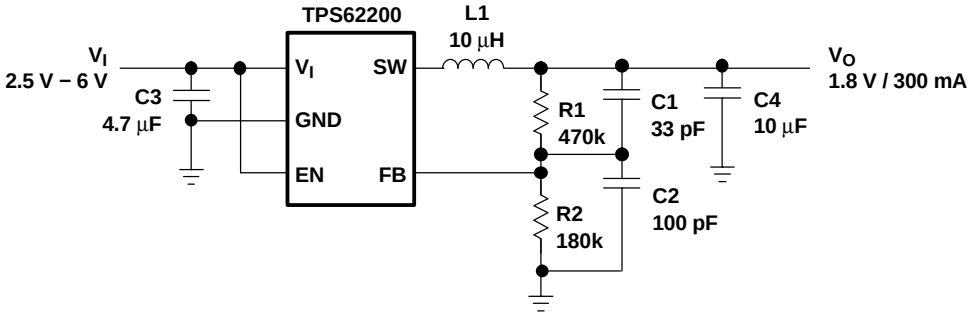


Figure 16. Typical Application Circuit for the Adjustable Output Voltage

INDUCTOR SELECTION

The TPS6220x device is optimized to operate with a typical inductor value of 10 µH.

For high efficiencies, the inductor should have a low dc resistance to minimize conduction losses. Although the inductor core material has less effect on efficiency than its dc resistance, an appropriate inductor core material must be used.

APPLICATION INFORMATION (continued)

The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current, and the lower the conduction losses of the converter. On the other hand, larger inductor values cause a slower load transient response. Usually the inductor ripple current, as calculated below, is around 20% of the average output current.

In order to avoid saturation of the inductor, the inductor should be rated at least for the maximum output current of the converter plus the inductor ripple current that is calculated as

$$\Delta I_L = Vout \times \frac{1-\frac{Vout}{Vin}}{L \times f} \qquad I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2}$$

f = switching frequency (1 MHz typical, 650 kHz minimal)

L = inductor valfue

ΔI_L = peak-to-peak inductor ripple current

I_{Lmax} = maximum inducator current

The highest inductor current occurs at maximum Vin.

A more conservative approach is to select the inductor current rating just for the maximum switch current of 670 mA. Refer to Table 1 for inductor recommendations.

Table 1. Recommended Inductors

INDUCTOR VALUE	COMPONENT SUPPLIER	COMMENTS
10 µH 10 µH 10 µH 10 µH	Sumida CDRH5D28-100 Sumida CDRH5D18-100 Sumida CDRH4D28-100 Coilcraft DO1608-103	High efficiency
6.8 µH 10 µH 10 µH 10 µH 10 µH	Sumida CDRH3D16-6R8 Sumida CDRH4D18-100 Sumida CR32-100 Sumida CR43-100 Murata LQH4C100K04	Smallest solution

INPUT CAPACITOR SELECTION

Because the buck converter has a pulsating input current, a low ESR input capacitor is required. This results in the best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. Also the input capacitor must be sufficiently large to stabilize the input voltage during heavy load transients. For good input voltage filtering, usually a 4.7 µF input capacitor is sufficient. It can be increased without any limit for better input-voltage filtering. If ceramic output capacitors are used, the capacitor RMS ripple current rating always meets the application requirements.

Ceramic capacitors show a good performance because of the low ESR value, and they are less sensitive against voltage transients and spikes compared to tantalum capacitors.

Place the input capacitor as close as possible to the input pin of the device for best performance (refer to Table 2 for recommended components).

OUTPUT CAPACITOR SELECTION

The advanced fast response voltage mode control scheme of the TPS6220x allows the use of tiny ceramic capacitors with a value of 10 µF without having large output voltage under and overshoots during heavy load transients.

Ceramic capacitors with low ESR values have the lowest output voltage ripple and are therefore recommended. If required, tantalum capacitors may be used as well (refer to Table 2 for recommended components).

At nominal load current the device operates in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta Vout = Vout \times \frac{1-\frac{Vout}{Vin}}{L \times f} \times \left(\frac{1}{8 \times Cout \times f} + ESR\right)$$

where the highest output voltage ripple occurs at the highest input voltage Vin.

At light load currents, the device operates in power save mode, and the output voltage ripple is independent of the output capacitor value. The output voltage ripple is set by the internal comparator thresholds. The typical output voltage ripple is 1% of the output voltage Vo.

Table 2. Recommended Capacitors

CAPACITOR VALUE	CASE SIZE	COMPONENT SUPPLIER	COMMENTS
4.7 µF	0805	Taiyo Yuden JMK212BY475MG	Ceramic
10 µF	0805	Taiyo Yuden JMK212BJ106MG TDK C12012X5ROJ106K	Ceramic Ceramic
10 µF	1206	Taiyo Yuden JMK316BJ106KL TDK C3216X5ROJ106M	Ceramic
22 µF	1210	Taiyo Yuden JMK325BJ226MM	Ceramic

LAYOUT CONSIDERATIONS

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator shows stability problems as well as EMI problems.

Therefore use wide and short traces for the main current paths, as indicated in bold in Figure 17. The input capacitor, as well as the inductor and output capacitor, should be placed as close as possible to the IC pins

The feedback resistor network must be routed away from the inductor and switch node to minimize noise and magnetic interference. To further minimize noise from coupling into the feedback network and feedback pin, the ground plane or ground traces must be used for shielding. This becomes very important especially at high switching frequencies of 1 MHz.

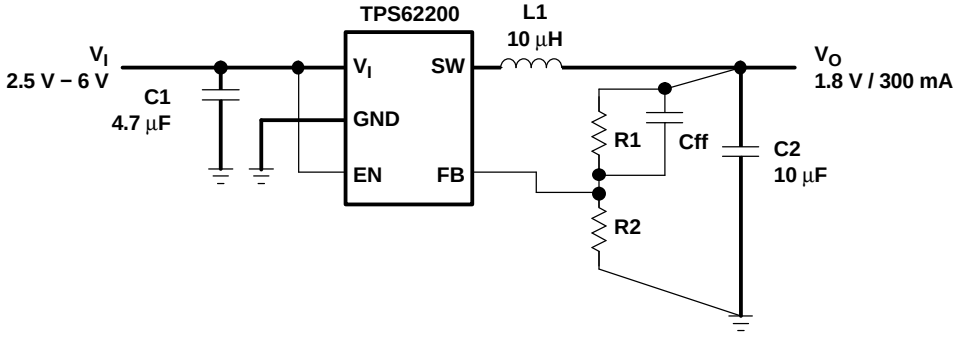


Figure 17. Layout Diagram

TYPICAL APPLICATIONS

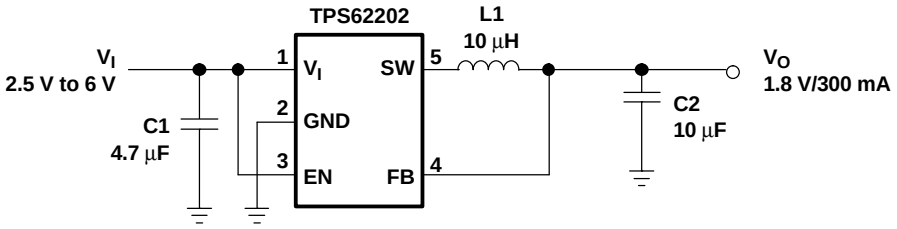


Figure 18. Li-Ion to 1.8 V Fixed Output Voltage Version

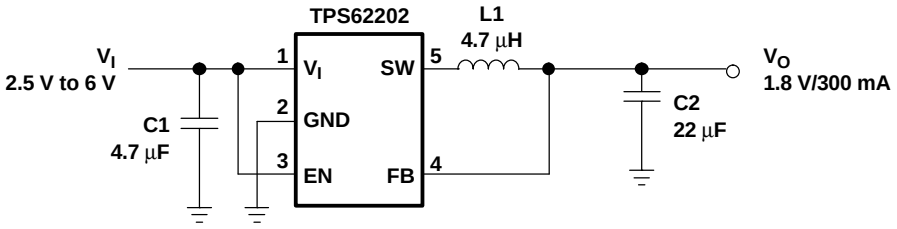


Figure 19. 1.8 V Fixed Output Voltage version Using 4.7µH Inductor

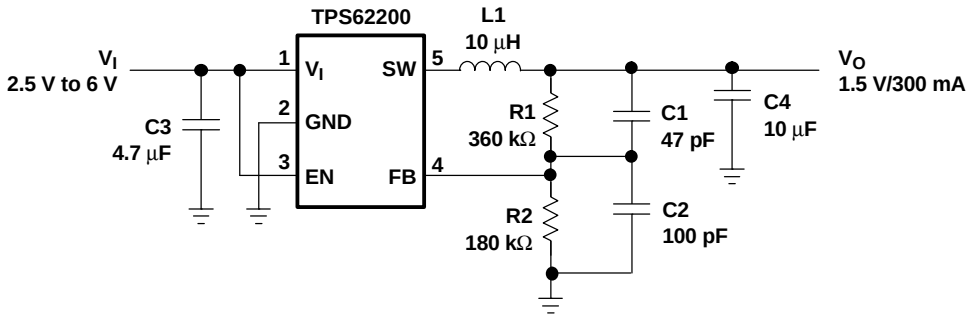


Figure 20. Adjustable Output Voltage Version Set to 1.5 V

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS62200DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS62200DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS62200DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS62200DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS62201DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS62201DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS62201DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS62201DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS62202DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS62202DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS62202DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS62202DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS62203DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS62203DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS62203DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS62203DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS62204DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS62204DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS62204DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS62205DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS62205DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS62205DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS62207DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS62207DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS62207DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

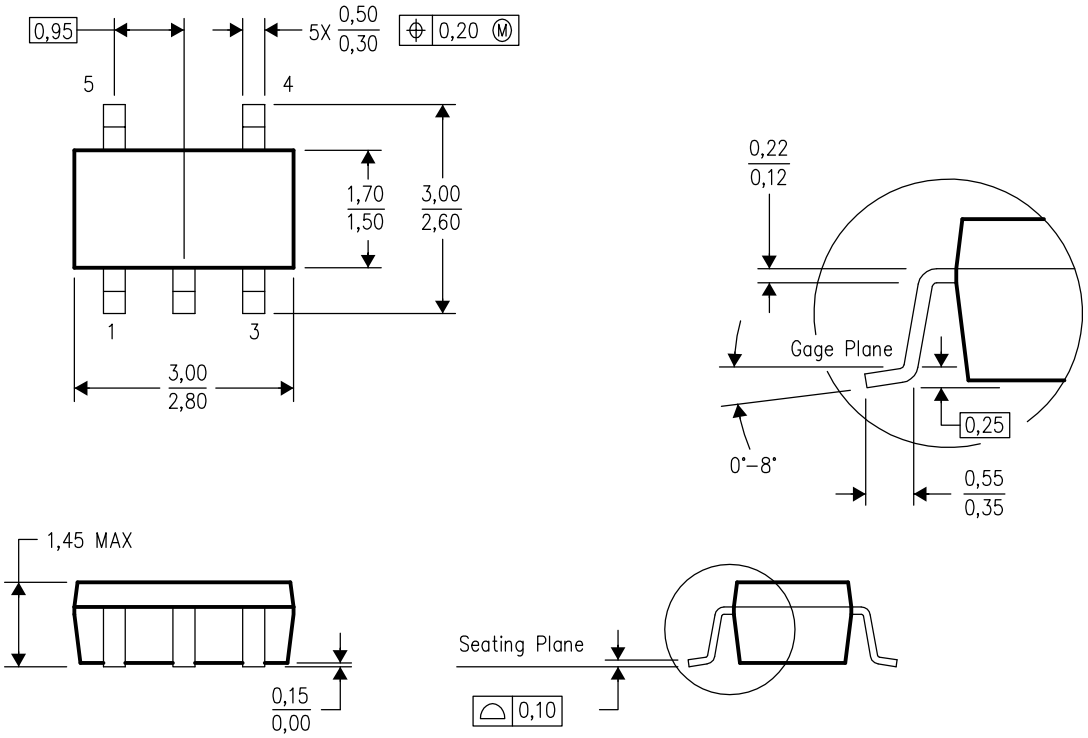
Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TPS62207DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS62208DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS62208DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/H 10/2003

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–178 Variation AA.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

Application Note
PNX0101ET/PNX0102ET

RNB-C/3252/2003IX-0655
RELEASE 2.0

2004 Jul 15

Philips
Components

PHILIPS

REVISION HISTORY

RELEASE	REMARKS
2.0	Updated Release

TABLE OF CONTENTS

1 INTRODUCTION

Thank you for choosing the Philips PNX0101 or PNX0102 for your application.

This Application Note describes the function of the device and how to form a complete system in terms of hardware.

1.1 PNX0101ET

The PNX0101 is a single chip solution based on an ARM7TMDI CPU core, which is a 32-bit RISC processor integrated with 8 kbyte dedicated cache, 4Mbit of Flash memory an ultra low power Audio DSP and Audio AD/DA Converters.

The high level of integration, low power consumption and high processor performance make the PNX0101 very suitable for portable hand-held devices.

1.2 PNX0102ET

The PNX0102 is the extended version of the PNX0101 and contains the following extras 8Mbit of Flash memory instead of 4Mbit and a High Speed USB2.0 Interface instead of a Full Speed.

1.3 Applications

- Portable MP3 Solid State Audio player (e.g. NAND-FLASH, Multi Media Card etc.)
- Home audio
- Mobile phone
- PDA

1.4 General Notice

This document is intended as an application guideline, this means that in some cases depending on the requirements of the application in some of the schematics there is room for change by the application designer.

2 BLOCK DIAGRAM

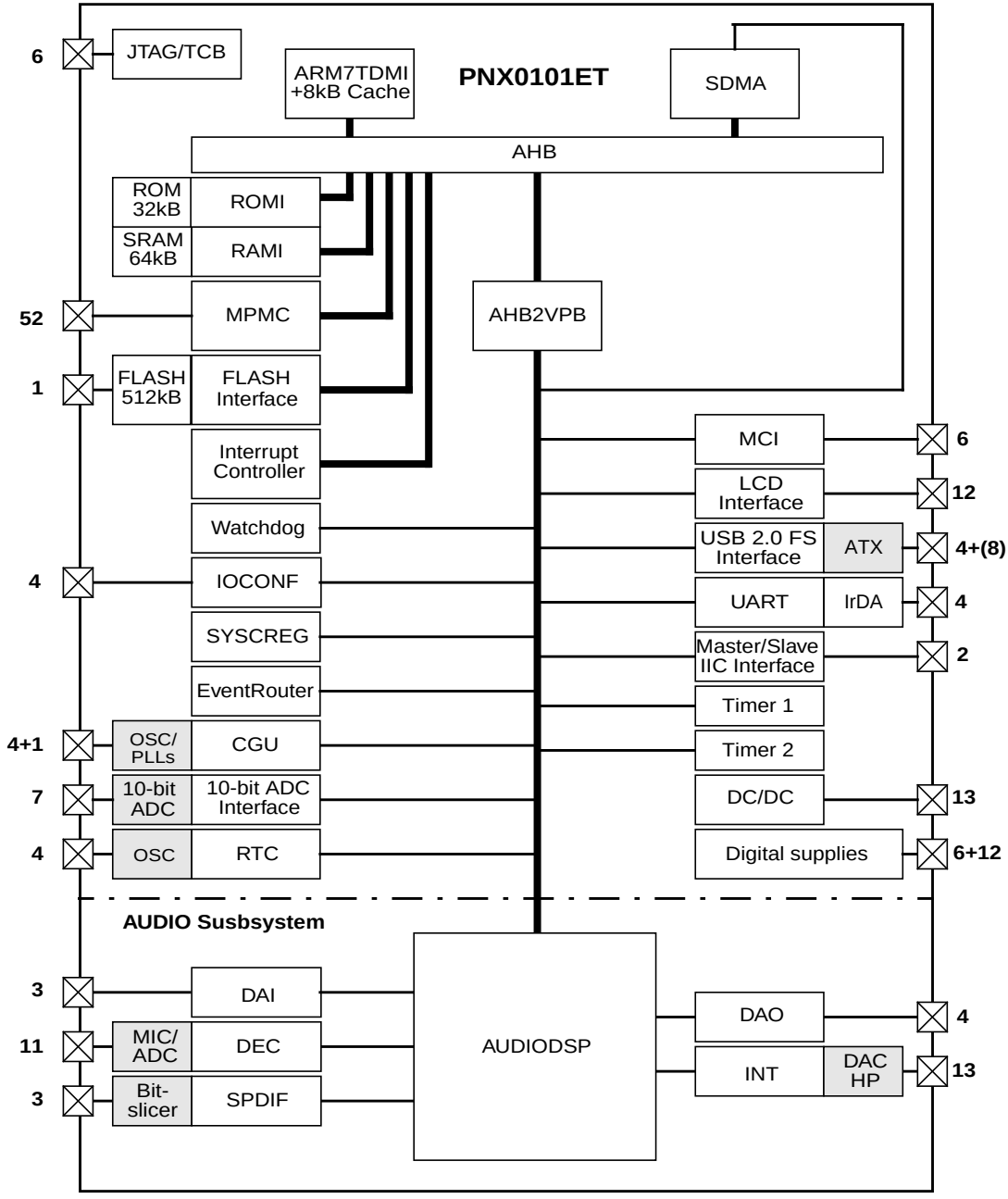


Fig. 1 Block diagram PNX0101

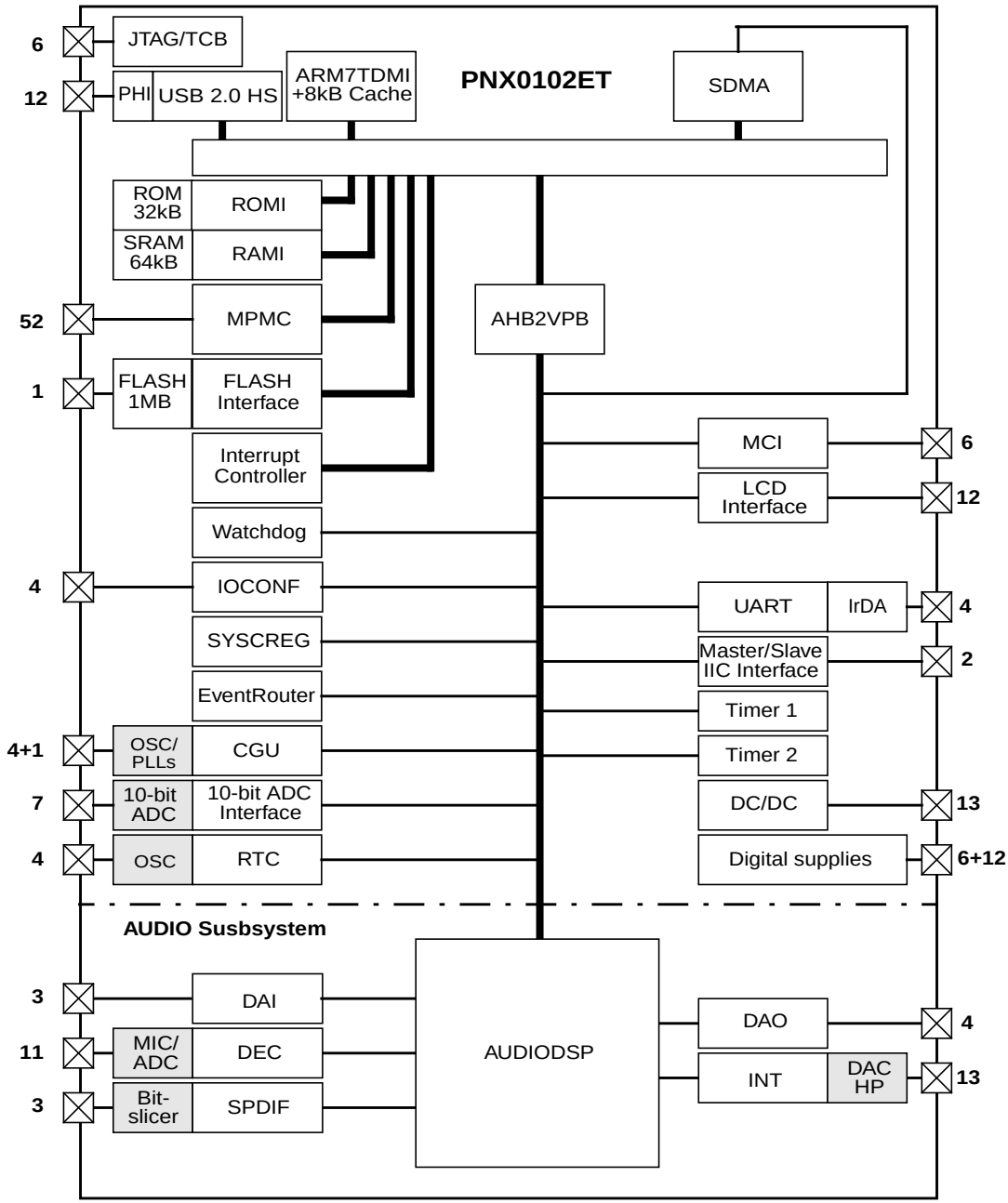


Fig. 2 Block diagram PNX0102

3 PINNING

3.1 Pin Description PNX0101/PNX0102

Table 1 Pin list PNX0101/PNX0102

SYMBOL[1]	BGA BALL	DIGITAL I/O LEVEL	APPL. FUNC	PIN STATE AFTER RESET	CELL TYPE	DESCRIPTION
12 MHz oscillator (fixed: 4 pins)						
XTALH_IN	T10		A	input	apio (ZI)	12 MHz clock input
XTALH_OUT	V9		A	output	apio (IO)	12 MHz clock output
XTALH_VDDA18	U9				vddco	Analog supply Oscillator
XTALH_VSSA	T9				vssco	Analog ground Oscillators
32.768 kHz oscillator (fixed: 4 pins)						
XTALL_IN	V7		A	input	apio (ZI)	32.768 kHz clock input
XTALL_OUT	T8		A	output	apio (ZI)	32.768 kHz clock output
XTALL_VDDA18	U8				vddco	Analog supply Oscillators/PLL's
XTALL_GNDA	V8				vssco	Analog ground Oscillators/PLL's
bitslicer/SPDIF (fixed: 3pins)						
SPDIF_IN	T12		A	input	apio (IO)	SPDIF input
SPDIF_VDDA33	U11				vddco	Analog supply SPDIF input
SPDIF_GNDA	T11				vssco	Analog ground SPDIF input
10-bit ADC (fixed: 7 pins)						
ADC10B_GPA4	U5		A	input	apio (ZI)	Analog General Purpose pins
ADC10B_GPA3	T6		A	input	apio (ZI)	Analog General Purpose pins
ADC10B_GPA2	U6		A	input	apio (ZI)	Analog General Purpose pins
ADC10B_GPA1	T7		A	input	apio (ZI)	Analog General Purpose pins
ADC10B_GPA0	U7		A	input	apio (ZI)	Analog General Purpose pins
ADC10B_VDDA33	V10				vddco	Analog supply 10-bit ADC
ADC10B_GNDA	U10				vssco	Analog ground 10-bit ADC
DAC (fixed: 13 pins)						
DAC_VOUTR	M3		A	output	apio (IO)	SDAC Right Analog Output
DAC_VOUTL	M2		A	output	apio (IO)	SDAC Left Analog Output
DAC_VDDA33	L1				vddco	SDAC Positive Voltage
DAC_VREFP	L2		A	input	apio (IO)	SDAC Positive Reference Voltage
DAC_VREFN	M1		A	input	apio (IO)	SDAC Negative Reference Voltage
HP_OUTR	P3		A	output	apio (IO)	SDAC Right Headphone Output
HP_OUTL	N3		A	output	apio (IO)	SDAC Left Headphone Output
HP_OUTCA	N2		A	output	apio (IO)	Headphone common output reference
HP_OUTCB	N1		A	output	apio (IO)	Headphone common output reference
HP_VDDA33A	R1				vddco	Headphone analog supply
HP_VDDA33B	R2				vddco	Headphone analog supply
HP_GNDAA	P2				vssco	Headphone analog ground
HP_GNDAB	P1				vssco	Headphone analog ground
ADC (fixed: 11 pins)						
ADC_VCOM	T3		A	input	apio (IO)	ADC Common Reference Voltage
ADC_VREFP	U2		A	input	apio (IO)	ADC Positive Reference Voltage
ADC_VREFN	V1		A	input	apio (IO)	ADC Negative Reference Voltage
ADC_VDDA18	V3				vddco	Analog supply ADC
ADC_VDDA33	U3				vddco	Analog supply ADC
ADC_GNDA	V2				vssco	Analog ground ADC

SYMBOL[1]	BGA BALL	DIGITAL I/O LEVEL	APPL. FUNC	PIN STATE AFTER RESET	CELL TYPE	DESCRIPTION
ADC_VREF	U1		A	input	apio (IO)	ADC Reference Voltage
ADC_VINR	T1		A	input	apio (IO)	SADC Right Analog Input
ADC_VINL	T4		A	input	apio (IO)	SADC Left Analog Input
ADC_MIC	R3		A	input	apio (IO)	Microphone input
ADC_MIC_LNA	T2		A	output	apio (IO)	Output of LNA of Microphone input
HP_VCOM				input		HP Common Reference Voltage
LCD Interface (fixed: 12 pins)						
LCD_RW_WR	G2	0-5 VDC tolerant	I/O	output	bpts10tht5v	6800 read/write select 8080 active 'high' write enable
GPIO_LCD_11						General Purpose IO pin
LCD_E_RD	F2	0-5 VDC tolerant	I/O	output	bpts10tht5v	6800 enable 8080 active 'high' read enable
GPIO_LCD_10						General Purpose IO pin
LCD_DB_7	E3	0-5 VDC tolerant	I/O	output	bpts10tht5v	Data input 7/Data output 7/Serial data output/4-bit data 3
GPIO_LCD_9						General Purpos IO pin
LCD_DB_6	E2	0-5 VDC tolerant	I/O	output	bpts10tht5v	Data input 6/Data output 6/Serial data input/4-bit data 2
GPIO_LCD_8						General Purpose IO pin
LCD_DB_5	D3	0-5 VDC tolerant	I/O	output	bpts10tht5v	Data input 5/Data output 5/Serial clock output/4-bit data 1
GPIO_LCD_7						General Purpos IO pin
LCD_DB_4	D1	0-5 VDC tolerant	I/O	output	bpts10tht5v	Data input 4/Data output 4/4-bit data 0
GPIO_LCD_6						General Purpose IO pin
LCD_DB_3	D2	0-5 VDC tolerant	I/O	output	bpts10tht5v	Data input 3/Data output 3
GPIO_LCD_5						General Purpose IO pin
LCD_DB_2	C3	0-5 VDC tolerant	I/O	output	bpts10tht5v	Data input 2/Data output 2
GPIO_LCD_4						General Purpose IO pin
LCD_DB_1	C1	0-5 VDC tolerant	I/O	output	bpts10tht5v	Data input 1/Data output 1
GPIO_LCD_3						General Purpose IO pin
LCD_DB_0	C2	0-5 VDC tolerant	I/O	output	bpts10tht5v	Data input 0/Data output 0
GPIO_LCD_2						General Purpose IO pin
LCD_CSB	B3	0-5 VDC tolerant	I/O	output	bpts10tht5v	Chip Select
GPIO_LCD_1						General Purpose IO pin
LCD_RS	F3	0-5 VDC tolerant	I/O	output	bpts10tht5v	'high' Data register select 'low' instruction register select
GPIO_LCD_0						General Purpose IO pin
Memory Card Interface (fixed: 6 pins)						
MCI_DAT_3	J3	0-5 VDC tolerant	I/O	input	bpts10tht5v	Data input/Data output
GPIO_MCI_5						General Purpose IO pin
MCI_DAT_2	J1	0-5 VDC tolerant	I/O	input	bpts10tht5v	Data input/Data output
GPIO_MCI_4						General Purpose IO pin
MCI_DAT_1	J2	0-5 VDC tolerant	I/O	input	bpts10tht5v	Data input/Data output
GPIO_MCI_3						General Purpose IO pin
MCI_DAT_0	H3	0-5 VDC tolerant	I/O	input	bpts10tht5v	Data input/Data output
GPIO_MCI_2						General Purpose IO pin
MCI_CLK	G3	0-5 VDC tolerant	I/O	output	bpts10tht5v	MCI clock output
GPIO_MCI_1						General Purpose IO pin

SYMBOL[1]	BGA BALL	DIGITAL I/O LEVEL	APPL. FUNC	PIN STATE AFTER RESET	CELL TYPE	DESCRIPTION
MCI_CMD	H2	0-5 VDC tolerant	I/O	input	bpts10tht5v	Command input/Command output
GPIO_MCI_0						General Purpose IO pin
USB Interface (fixed: 4 pins + (8 pins reserved for future use))						
USB_CONNECT_N	T15	0-5 VDC tolerant	I/O	output	bpts10tht5v	Soft connect output USB 2.0 FS
GPIO_USB_1						General Purpose IO pin
USB_RPU			A		apio (IO)	Reserved for USB 2.0 HS
USB_DP	U17		A	input	usb11	Positive USB data line USB 2.0 FS
USB_DP					apio	Positive USB data line USB 2.0 HS
USB_DM	T17		A	input	usb11	Negative USB data line USB 2.0 FS
USB_DM					apio	Negative USB data line USB 2.0 HS
USB_VBUS	U14	0-5 VDC tolerant	I/O	input	bpts10tht5v	USB Supply detection line USB 2.0 FS & USB 2.0 HS
GPIO_USB_0						General Purpose IO pin
USB_RREF	P16		I/O		bpts10tht5v	
USB_GNDA	R17				vssco	Reserved for USB 2.0 HS
USB_VSSA_REF	R16				vccso	Reserved for USB 2.0 HS
USB_VSSA_TERM	T16				vssco	Reserved for USB 2.0 HS
USB_VDDA18_PLL	U15				vddco	Reserved for USB 2.0 HS
USB_VDDA18_BG	U16				vddco	Reserved for USB 2.0 HS
USB_VDDA33	U18				vddco	Reserved for USB 2.0 HS
USB_VDDA33_DRV	V18				vddco	Reserved for USB 2.0 HS
DAI Interface (fixed: 3 pins)						
DAI_BCK	H17	0-5 VDC tolerant	I/O	input	bpts10tht5v	DAI Bitclock
GPIO_DAI_2						General Purpose IO pin
DAI_WS	G17	0-5 VDC tolerant	I/O	input	bpts10tht5v	DAI Wordselect
GPIO_DAI_1						General Purpose IO pin
DAI_DATA	G16	0-5 VDC tolerant	I/O	input	bpts10tht5v	DAI Serial data input
GPIO_DAI_0						General Purpose IO pin
DAO Interface (fixed: 4 pins)						
DAO_CLK	F16	0-5 VDC tolerant	I/O	output	bpts10tht5v	256 fs clock output
DAO_BCK	G18	0-5 VDC tolerant	I/O	output	bpts10tht5v	DAO Bitclock
GPIO_DAO_2						General Purpose IO pin
DAO_WS	F18	0-5 VDC tolerant	I/O	output	bpts10tht5v	DAO Wordselect
DAO_DATA	F17	0-5 VDC tolerant	I/O	output	bpts10tht5v	DAO Serial data output
GPIO_DAO_0						General Purpose IO pin
JTAG (fixed: 6 pins)						
JTAG_TRST_N	T13	0-5 VDC tolerant	I	input	ipthdt5v	JTAG Reset Input (pull-down)
JTAG_TCK	V4	0-5 VDC tolerant	I	input	ipthut5v	JTAG Clock Input (pull-up)
JTAG_TMS	U12	0-5 VDC tolerant	I	input	ipthut5v	JTAG Mode Select Input (external pull-up)
JTAG_TDI	T5	0-5 VDC tolerant	I	input	ipthut5v	JTAG Data Input (pull-up)
JTAG_TDO	U13	0-5 VDC tolerant	I/O	output	bpts10tht5v	JTAG Data output
JTAG_SEL_ARM	U4	0-5 VDC tolerant	I	input	ipthdt5v	JTAG selection (pull-down)
IIC master/slave Interface (fixed: 2 pins)						
IIC_SCL	H16	0-5 VDC tolerant	I/O	input	iic400kt5v	Serial clock IIC Slave
IIC_SDA	J17	0-5 VDC tolerant	I/O	input	iic400kt5v	Serial data IIC Slave
MPMC (fixed: 52 pins)						
MPMC_D_15	B8		I/O	input	bpts10th	MPMC data input/output 15
GPIO_MPMC_50						General Purpose IO pin

SYMBOL[1]	BGA BALL	DIGITAL I/O LEVEL	APPL. FUNC	PIN STATE AFTER RESET	CELL TYPE	DESCRIPTION
MPMC_D_14	C8		I/O	input	bpts10th	MPMC data input/output 14
GPIO_MPMC_49						General Purpose IO pin
MPMC_D_13	B7		I/O	input	bpts10th	MPMC data input/output 13
GPIO_MPMC_48						General Purpose IO pin
MPMC_D_12	C7		I/O	input	bpts10th	MPMC data input/output 12
GPIO_MPMC_47						General Purpose IO pin
MPMC_D_11	B6		I/O	input	bpts10th	MPMC data input/output 11
GPIO_MPMC_46						General Purpose IO pin
MPMC_D_10	C6		I/O	input	bpts10th	MPMC data input/output 10
GPIO_MPMC_45						General Purpose IO pin
MPMC_D_9	C5		I/O	input	bpts10th	MPMC data input/output 9
GPIO_MPMC_44						General Purpose IO pin
MPMC_D_8	C4		I/O	input	bpts10th	MPMC data input/output 8
GPIO_MPMC_43						General Purpose IO pin
MPMC_D_7	B5		I/O	input	bpts10th	MPMC data input/output 7
GPIO_MPMC_42						General Purpose IO pin
MPMC_D_6	A5		I/O	input	bpts10th	MPMC data input/output 6
GPIO_MPMC_41						General Purpose IO pin
MPMC_D_5	B4		I/O	input	bpts10th	MPMC data input/output 5
GPIO_MPMC_40						General Purpose IO pin
MPMC_D_4	A4		I/O	input	bpts10th	MPMC data input/output 4
GPIO_MPMC_39						General Purpose IO pin
MPMC_D_3	A3		I/O	input	bpts10th	MPMC data input/output 3
GPIO_MPMC_38						General Purpose IO pin
MPMC_D_2	B2		I/O	input	bpts10th	MPMC data input/output 2
GPIO_MPMC_37						General Purpose IO pin
MPMC_D_1	A2		I/O	input	bpts10th	MPMC data input/output 1
GPIO_MPMC_36						General Purpose IO pin
MPMC_D_0	A1		I/O	input	bpts10th	MPMC data input/output 0
GPIO_MPMC_35						General Purpose IO pin
MPMC_A_20	C13		I/O	output	bpts10th	MPMC address 20
GPIO_MPMC_34						General Purpose IO pin
MPMC_A_19	B13		I/O	output	bpts10th	MPMC address 19
GPIO_MPMC_33						General Purpose IO pin
MPMC_A_18	A13		I/O	output	bpts10th	MPMC address 18
GPIO_MPMC_32						General Purpose IO pin
MPMC_A_17	C14		I/O	output	bpts10th	MPMC address 17
GPIO_MPMC_31						General Purpose IO pin
MPMC_A_16	B14		I/O	output	bpts10th	MPMC address 16
GPIO_MPMC_30						General Purpose IO pin
MPMC_A_15	A14		I/O	output	bpts10th	MPMC address 15
GPIO_MPMC_29						General Purpose IO pin
MPMC_A_14	C15		I/O	output	bpts10th	MPMC address 14
GPIO_MPMC_28						General Purpose IO pin
MPMC_A_13	B15		I/O	output	bpts10th	MPMC address 13
GPIO_MPMC_27						General Purpose IO pin

SYMBOL[1]	BGA BALL	DIGITAL I/O LEVEL	APPL. FUNC	PIN STATE AFTER RESET	CELL TYPE	DESCRIPTION
MPMC_A_12	C16		I/O	output	bpts10th	MPMC address 12
GPIO_MPMC_26						General Purpose IO pin
MPMC_A_11	B16		I/O	output	bpts10th	MPMC address 11
GPIO_MPMC_25						General Purpose IO pin
MPMC_A_10	C17		I/O	output	bpts10th	MPMC address 10
GPIO_MPMC_24						General Purpose IO pin
MPMC_A_9	B17		I/O	output	bpts10th	MPMC address 9
GPIO_MPMC_23						General Purpose IO pin
MPMC_A_8	C18		I/O	output	bpts10th	MPMC address 8
GPIO_MPMC_22						General Purpose IO pin
MPMC_A_7	B18		I/O	output	bpts10th	MPMC address 7
GPIO_MPMC_21						General Purpose IO pin
MPMC_A_6	A18		I/O	output	bpts10th	MPMC address 6
GPIO_MPMC_20						General Purpose IO pin
MPMC_A_5	D18		I/O	output	bpts10th	MPMC address 5
GPIO_MPMC_19						General Purpose IO pin
MPMC_A_4	D17		I/O	output	bpts10th	MPMC address 4
GPIO_MPMC_18						General Purpose IO pin
MPMC_A_3	D16		I/O	output	bpts10th	MPMC address 3
GPIO_MPMC_17						General Purpose IO pin
MPMC_A_2	E18		I/O	output	bpts10th	MPMC address 2
GPIO_MPMC_16						General Purpose IO pin
MPMC_A_1	E17		I/O	output	bpts10th	MPMC address 1
GPIO_MPMC_15						General Purpose IO pin
MPMC_A_0	E16		I/O	output	bpts10th	MPMC address 0
GPIO_MPMC_14						General Purpose IO pin
MPMC_NSTCS_2	B11		I/O	output	bpts10th	Static memory chip select 2. Default active LOW (reprogrammable).
GPIO_MPMC_13						General Purpose IO pin
MPMC_NSTCS_1	A8		I/O	output	bpts10th	Static memory chip select 1. Default active LOW (reprogrammable).
GPIO_MPMC_12						General Purpose IO pin
MPMC_NSTCS_0	C9		I/O	output	bpts10th	Static memory chip select 0. Default active LOW (reprogrammable).
GPIO_MPMC_11						General Purpose IO pin
MPMC_NDYCS	B9		I/O	output	bpts10th	SDRAM chip select. Active LOW.
GPIO_MPMC_10						General Purpose IO pin
MPMC_CLKOUT	A10		O	output	bpt4mt	Memory clock output. Connect to the clock input of SDRAM and SyncFlash devices.
MPMC_CKE	B10		I/O	output	bpts10th	SDRAM clock enable. Active HIGH.
GPIO_MPMC_9						General Purpose IO pin
MPMC_NWE	C11		I/O	output	bpts10th	Write enable for SDRAM. Active LOW.
GPIO_MPMC_8						General Purpose IO pin
MPMC_NRAS	A9		I/O	output	bpts10th	Row address strobe for SDRAM and SyncFlash devices. Active LOW.
GPIO_MPMC_7						General Purpose IO pin

SYMBOL[1]	BGA BALL	DIGITAL I/O LEVEL	APPL. FUNC	PIN STATE AFTER RESET	CELL TYPE	DESCRIPTION
MPMC_NCAS	C10		I/O	output	bpts10th	Column address strobe for SDRAM and SyncFlash devices. Active LOW.
GPIO_MPMC_6						General Purpose IO pin
MPMC_DQM_1	A11		I/O	output	bpts10th	Data mask output to SDRAM. Active HIGH. The signal MPMCDQMOUT[1] mask byte [15:8] on the data bus. Used for SDRAM devices.
GPIO_MPMC_5						General Purpose IO pin
MPMC_DQM_0	C12		I/O	output	bpts10th	Data mask output to SDRAM. Active HIGH. The signal MPMCDQMOUT[0] mask byte [7:0] on the data bus. Used for SDRAM devices.
GPIO_MPMC_4						General Purpose IO pin
MPMC_NOE	A17		I/O	output	bpts10th	Output enable for static memories. Active LOW. Used for static memory devices.
GPIO_MPMC_3						General Purpose IO pin
MPMC_BLOUT1	B12		I/O	output	bpts10th	The signal nMPMCBLSOUT[1] selects byte lane [15:8] on the data bus. Used for static memory devices.
GPIO_MPMC_2						General Purpose IO pin
MPMC_BLOUT0	A12		I/O	output	bpts10th	The signal nMPMCBLSOUT[0] selects byte lane [7:0] on the data bus. Used for static memory devices.
GPIO_MPMC_1						General Purpose IO pin
MPMC_RPOUT	B1		I/O	output	bpts10th	Reset power down to SyncFlash memory. Active LOW. Used for static memory devices.
GPIO_MPMC_0						General Purpose IO pin
UART (fixed: 4 pins)						
UART_TXD	L3	0-5 VDC tolerant	I/O	output	bpts10tht5v	Serial output
GPIO_UART_3						General Purpose IO pin
UART_RXD	K3	0-5 VDC tolerant	I/O	input	bpts10tht5v	Serial input
GPIO_UART_2						General Purpose IO pin
UART_NCTS	K2	0-5 VDC tolerant	I/O	input	bpts10tht5v	Clear to send (active low)
GPIO_UART_1						General Purpose IO pin
UART_NRTS	K1	0-5 VDC tolerant	I/O	output	bpts10tht5v	Ready to send
GPIO_UART_0						General Purpose IO pin
Mode selection pins (fixed: 2 pins)						
GPIO_3	J16	0-5 VDC tolerant	I/O	input	bpts10thdt5v	Start up mode pin 2 (pull down) General Purpose IO pin
GPIO_2	K18	0-5 VDC tolerant	I/O	input	bpts10thdt5v	Start up mode pin 1 (pull down) General Purpose IO pin
GPIO (fixed: 2 pins)						
GPIO_1	K17	0-5 VDC tolerant	I/O	input output (Test Mode))	bpts10tht5v	General Purpose IO pin Toggled (Test Mode)
GPIO_0	K16	0-5 VDC tolerant	I/O	input	bpts10tht5v	General Purpose IO pin (stop)
Reset input pin (fixed: 1 pin)						
RSTIN_N	T14	0-5 VDC tolerant	I	input	ipthut5v	System Reset input (active low)
Flash pins (fixed: 1 pins)						
FLASH_VDD_HV	V15				vddco	
Digital supplies (fixed: 6 pins)						
VDDI1	H1				vddco	Core supply (Mem)

SYMBOL[1]	BGA BALL	DIGITAL I/O LEVEL	APPL. FUNC	PIN STATE AFTER RESET	CELL TYPE	DESCRIPTION
VDDI2	V11				vddco	Core supply (Core)
VDDI3	V16				vddi	Core supply (Flash)
VSSI1	G1				vssco	Core ground (Mem)
VSSI2	V12				vssco	Core ground (Core)
VSSI3	V17				vssis	Core ground (Flash)
Peripheral supplies (fixed: 12 pins)						
VDDE1	E1				vdde3v3	Peripherel (I/O) supply (3.3V)
VDDE2	V5				vdde3v3	Peripheral (I/O) supply (3.3V)
VDDE3	V14				vdde3v3	Peripheral (I/O) supply (3.3V)
VDDE4	J18				vdde3v3	Peripheral (I/O) supply (3.3V)
VSSE1	F1				vsse3v3	Peripheral (I/O) ground
VSSE2	V6				vsse3v3	Peripheral (I/O) ground
VSSE3	V13				vsse3v3	Peripheral (I/O) ground
VSSE4	H18				vsse3v3	Peripheral (I/O) ground
VDDE5	A16				vdde3v3	MPMC Peripheral (I/O) supply (1.8V .. 3.3V)
VDDE6	A7				vdde3v3	MPMC Peripheral (I/O) supply (1.8V .. 3.3V)
VSSE5	A15				vsse3v3	MPMC Peripheral (I/O) ground
VSSE6	A6				vsse3v3	MPMC Peripheral (I/O) ground
DC/DC pins (fixed: 13 pins)						
DCDC_PLAY	L17		A		apio	Play button input
DCDC_STOP	L18		A		apio	Stop signal input
DCDC_LX2	N17		A		apio	DC/DC connection to external coil 2
DCDC_LX1	P17		A		apio	DC/DC connection to external coil 1
DCDC_VUSB	T18		A		apio	USB supply voltage
DCDC_VBAT	M17				vddco	Battery supply voltage
DCDC_VOUT33A	R18				vddco	DC/DC 3.3V output voltage
DCDC_VOUT33B	M16				vddco	DC/DC 3.3V input voltage
DCDC_VOUT18	N18				vddco	DC/DC 1.8V output voltage
DCDC_VSS1	P18				vssco	DC/DC ground to N-switch 1
DCDC_VSS2	N16				vssco	DC/DC ground to N-switch 2
DCDC_GND	L16				vssco	Core ground and substrate
DCDC_CLEAN	M18				vssco	Reference circuit ground, not connected to substrate

1. Pin positions are fixed.

Table 2 : PNX0101/PNX0102 pinning diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	MPMC_D_0	MPMC_D_1	MPMC_D_3	MPMC_D_4	MPMC_D_6	VSSE6	VDDE6	MPMC_NSTCS_1	MPMC_NRAS	MPMC_CLKOUT	MPMC_DQM_1	MPMC_BLOUT_0	MPMC_A_18	MPMC_A_15	VSSE5	VDDE5	MPMC_NOE	MPMC_A_6
B	MPMC_RPOUT	MPMC_D_2	LCD_CSB	MPMC_D_5	MPMC_D_7	MPMC_D_11	MPMC_D_13	MPMC_D_15	MPMC_NDYCS	MPMC_CKE	MPMC_NSTCS_2	MPMC_BLOUT_1	MPMC_A_19	MPMC_A_16	MPMC_A_13	MPMC_A_11	MPMC_A_9	MPMC_A_7
C	LCD_DB_1	LCD_DB_0	LCD_DB_2	MPMC_D_8	MPMC_D_9	MPMC_D_10	MPMC_D_12	MPMC_D_14	MPMC_NSTCS_0	MPMC_NCAS	MPMC_NWE	MPMC_DQM_0	MPMC_A_20	MPMC_A_17	MPMC_A_14	MPMC_A_12	MPMC_A_10	MPMC_A_8
D	LCD_DB_4	LCD_DB_3	LCD_DB_5													MPMC_A_3	MPMC_A_4	MPMC_A_5
E	VDDE1	LCD_DB_6	LCD_DB_7													MPMC_A_0	MPMC_A_1	MPMC_A_2
F	VSSE1	LCD_E_RD	LCD_RS													DAO_CLK	DAO_DATA	DAO_WS
G	VSSI1	LCD_RW_WR	MCI_CLK													DAI_DATA	DAI_WS	DAO_BCK
H	VDDI1	MCI_CMD	MCI_DAT_0													IIC_SCL	DAI_BCK	VSSE4
J	MCI_DAT_2	MCI_DAT_1	MCI_DAT_3													GPIO_3	IIC_SDA	VDDE4
K	UART_NRTS	UART_NCTS	UART_RXD													GPIO_0	GPIO_1	GPIO_2
L	DAC_VDDA33	DAC_VREFP	UART_TXD													DCDC_GND	DCDC_PLAY	DCDC_STOP
M	DAC_VREFN	DAC_VOUTL	DAC_VOUTR													DCDC_VOUT33B	DCDC_VBAT	DCDC_CLEAN
N	HP_OUTCB	HP_OUTCA	HP_OUTL													DCDC_VSS2	DCDC_LX2	DCDC_VOUT18
P	HP_GNDAB	HP_GNDAA	HP_OUTR													USB_RREF	DCDC_LX1	DCDC_VSS1
R	HP_VDDA33A	HP_VDDA33B	ADC_MIC													USB_VSSA_REF	USB_GNDA	DCDC_VOUT33A
T	ADC_VINR	ADC_MIC_LNA	ADC_VCOM	ADC_VINL	JTAG_TDI	ADC10B_GPA3	ADC10B_GPA1	XTALL_OUT	XTALH_VSSA	XTALH_IN	SPDIF_GNDA	SPDIF_IN	JTAG_TRST_N	RSTIN_N	USB_CONNECT_N	USB_VSSA_TERM	USB_DM	DCDC_VUSB
U	ADC_VREF	ADC_VREFP	ADC_VDDA33	JTAG_SEL_ARM	ADC10B_GPA4	ADC10B_GPA2	ADC10B_GPA0	XTALL_VDDA18	XTALH_VDDA18	ADC10B_GNDA	SPDIF_VDDA33	JTAG_TMS	JTAG_TDO	USB_VBUS	USB_VDDA18_PLL	USB_VDDA18_BG	USB_DP	USB_VDDA33
V	ADC_VREFN	ADC_GNDA	ADC_VDDA18	JTAG_TCK	VDDE2	VSSE2	XTALL_IN	XTALL_GNDA	XTALH_OUT	ADC10B_VDDA33	VDDI2	VSSI2	VSSE3	VDDE3	FLASH_VDD_HV	VDDI3	VSSI3	USB_VDDA33_DRV

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 |

3.2 Cell Type

Table 3 Cell type explanation

CELL NAME	EXPLANATION
ipthtt5v	Input Pad; Push Pull; TTL with Hysteresis; 5 Volt Tolerant
ipthut5v	Input Pad; Push Pull; TTL with Hysteresis; Pull Up; 5 Volt Tolerant
ipthdt5v	Input Pad; Push Pull; TTL with Hysteresis; Pull Down; 5 Volt Tolerant
ots10ct5v	Output Pad; 3state; 10ns Slew Rate Control; 5 Volt Tolerant
bpt4mt	Bidirectional Pad; Plain Input; 3 state Output; 4mA Output Drive; **Not** 5 Volt Tolerant
bpts10tht5v	Bidirectional Pad; Plain Input; 3 state Output; 10ns Slew Rate Control; TTl with Hysteresis; 5 Volt Tolerant
bpts10thdt5v	Bidirectional Pad; Plain Input; 3 state Output; 10ns Slew Rate Control; TTl with Hysteresis; Pull Down; 5 Volt Tolerant
bpts10th	Bidirectional Pad; Plain Input; 3 state Output; 10ns Slew Rate Control; TTL with Hysteresis; **Not** 5 Volt Tolerant
iic400kt5v	IIC Pad; 400kHz IIC specification; 5 Volt Tolerant
usb11	Universal Serial Bus Pad; Revision 1.1 specification
vnex	AMDC special pads for flash
vpex	AMDC special pads for flash
apio	Analog Pad; Analog Input/Output
vddi	Vdd Pad Connected to Core Vdd and internal Vdd Supply Rail in IO Ring
vddco	Vdd Pad Connected to Core Vdd
vdde3v3	Vdd Pad Connected to External (Noisy) 3.3 Volt Vdd Supply Rail
vssi	Vss Pad Connected to Core Vss and internal Vss Supply Rail in IO ring
vssco	Vss Pad Connected to Core Vss
vsse3v3	Vss Pad Connected to External (Noisy) 3.3 Volt Vss Supply Rail
vssis	Vss Pad Connected to Core Vss, internal Vss Supply Rail in IO Ring and Substrate Rail in IO Ring

4 LIMITING VALUES

Table 4 Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
All digital I/Os						
V_{DDE}	Supply voltage, external rail		-0.5	-	4.6	V
V_I	DC input voltage range	Note 1	-0.5	-	V_{DDE}+0.5	V
V_O	DC output voltage range		-0.5	-	3.6	V
I_O	DC output current	$V_{DDE<1:6>}$ = 3.3V		4		mA
5 Volt tolerant I/Os only						
V_I	DC input voltage range		-0.5		6.0	V
Temperature values						
T_j	junction temperature		-20	-	+125	^oC
T_{stg}	storage temperature		-40	-	+125	^oC
T_{amb}	operating ambient temperature		-20	+25	+70	^oC
Electrostatic handling						
V_{es}	electrostatic handling	HBM	-2000	-	+2000	V
		MM	-250	-	+250	V

Note

1. Maximum may not exceed 4.6V

5 12.000MHZ OSCILLATOR

5.1 Overview

The PNX0101/PNX0102 consists of two Oscillators of which one is the 12.000MHz Oscillator. The 12.000MHz Oscillator is used in combination with two PLLs and clock dividers to generate the system frequencies.

The two system frequencies are generated by two PLLs:

- MASTER PLL - Generates the frequencies for the ARM core, DSP core and all related blocks.
- AUDIO PLL - Generates the audio sampling frequencies.

5.2 Application Description

5.2.1 Design Rules

The PNX0101/PNX0102 cannot function without the 12.000MHz oscillator so this part should always be connected. To guarantee correct operation use a crystal to drive the oscillator and do not use a ceramic resonator.

5.2.2 Application Schematic

The Application Schematic below shows how the 12.000MHz oscillator should be connected when used.

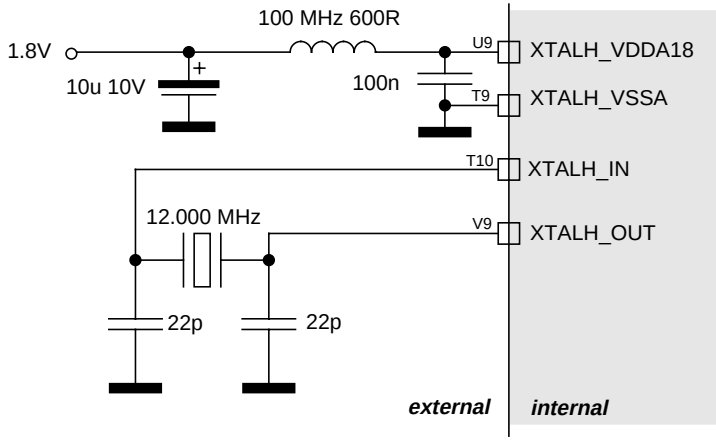


Fig.3 Application Schematic 12.000 MHz Oscillator

6 32.768KHZ OSCILLATOR

6.1 Overview

The other Oscillator of the two Oscillators of the PNX0101/PNX0102 is the 32.768kHz Oscillator. The 32.768KHz Oscillator is used to generate the frequency for the Real Time Clock (RTC) module.

6.2 Application Description

6.2.1 DESIGN RULES

The PNX0101/PNX0102 can function with or without the 32.768kHz oscillator, when using this part use a crystal to drive the oscillator to guarantee correct operation.

6.2.2 APPLICATION SCHEMATIC

The Application Schematic below shows how the 32.768kHz oscillator should be connected when used and when not used.

When this part is not used leave the supply on, and tie the input to ground. In software this part should be set in power down mode. The main reason why the supply should be left on, is because the internal PLLs are also supplied from this part.

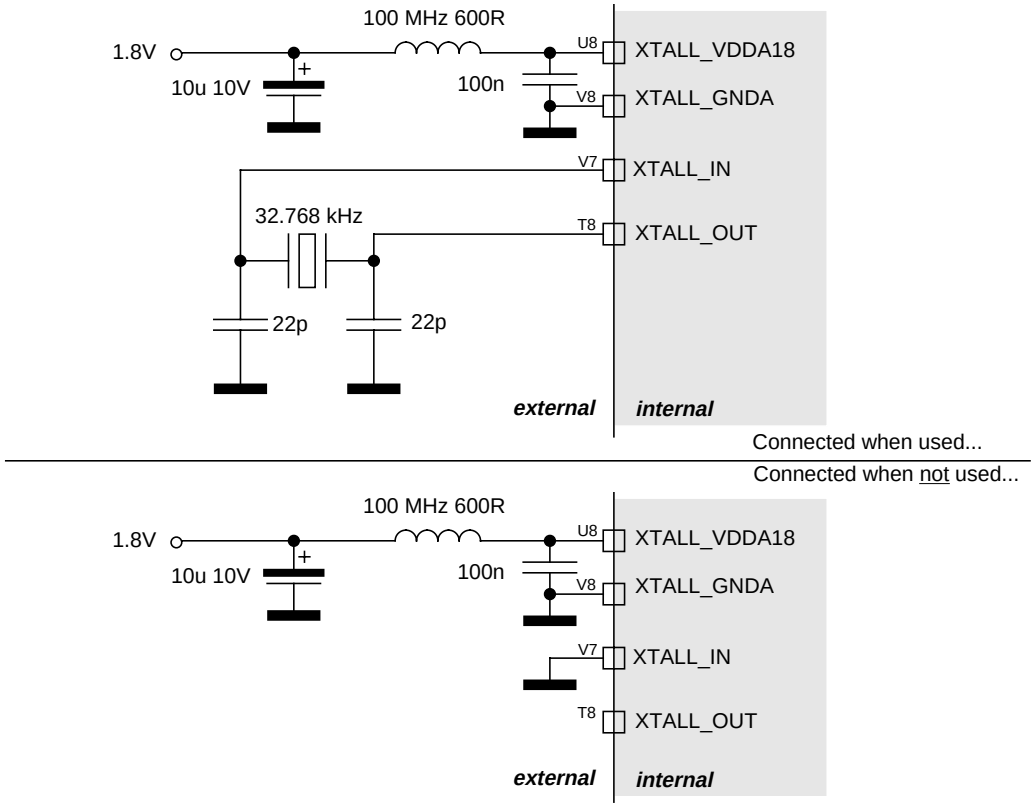


Fig.4 Application Schematic 32.768 kHz Oscillator

7 10-BIT ADC

7.1 Overview

The 10-bit ADC of the PNX0101/PNX0102 is a 10 bit succesive approximation analog to digital converter.

Features:

- Eight input channels (of which five available) selected through an analog multiplexer.
- From 2 to 10 bits conversion resolution.
- Maximum conversion rate 400ksamples/s for 10 bits resolution per channel.
- Power down mode.
- Reference voltage inputs are internally connected to the analog supply voltage.

7.2 Application Description

7.2.1 Design Rules

No advisable restrictions.

7.2.2 Application Schematic

The Application Schematic below shows how the 10-bit ADC should be connected when used and when not used.

When this part is not used the supply must be tied to ground, this to prevent floating outputs. Inputs can be left open and in software this part should be set in power down mode.

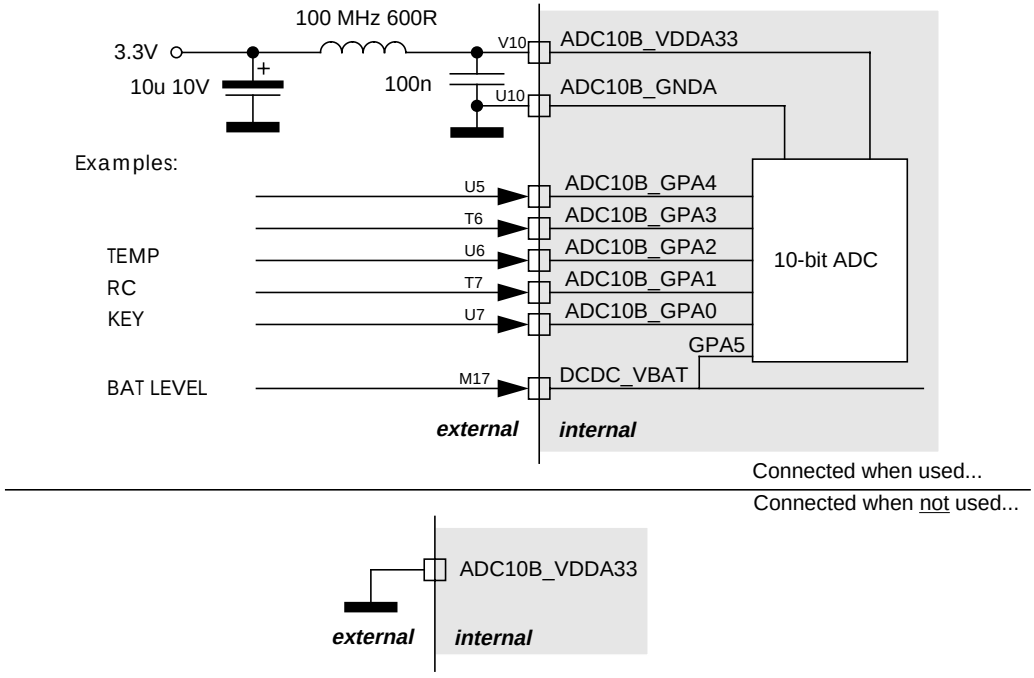


Fig.5 Application Schematic 10-bit ADC

8 LCD INTERFACE

8.1 Overview

The LCD Interface of the PNX0101/PNX0102 is compatible with the 6800 and the 8080 bus standard.

Features:

- 8/4 bit parallel interface mode: 6800-series or 8080-series.
- Supports multiple frequencies for the 6800/8080 bus, to support high and low speed controllers.
- Contains a serial interface.

8.2 Application Description

8.2.1 Design Rules

No advisable restrictions.

8.2.2 Application Schematic (8-bit parallel mode)

The Application Schematic below shows how the LCD Interface should be connected when used in 8-bit parallel mode.

When the LCD Interface is not used all pins can be left unconnected. In software this part should then be set to IOCONF and all pins as outputs.

Example:
VARITRONIX LTD. MOBI11264A

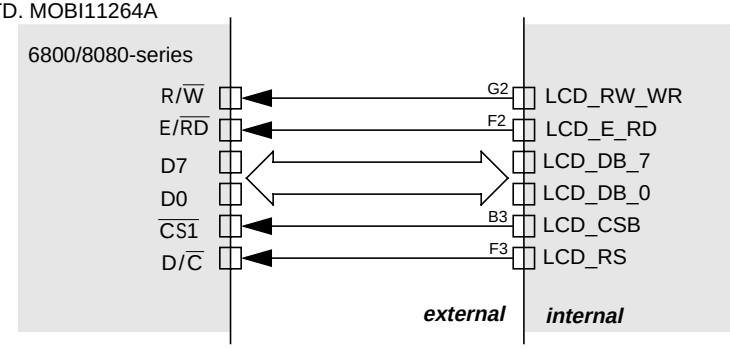


Fig.6 Application Schematic LCD Interface (8-bit Parallel Mode)

8.2.3 Application Schematic (4-bit parallel mode)

The Application Schematic on the next page shows how the LCD Interface should be connected when used in 4-bit parallel mode.

Example:
Not Available

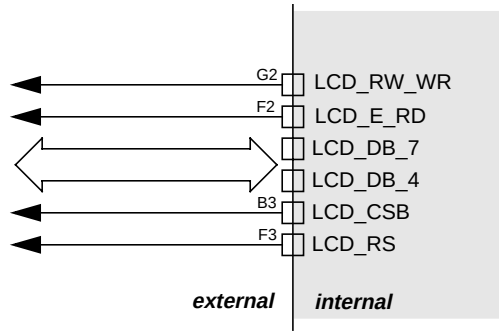


Fig.7 Application Schematic LCD Interface (4-bit Parallel Mode)

8.2.4 Application Schematic (serial mode)

The Application Schematic below shows how the LCD Interface should be connected when used in serial mode.

Example:
VARITRONIX LTD. MOBI11264A

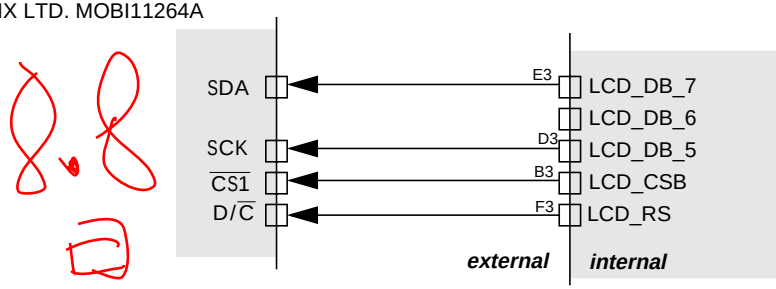


Fig.8 Application Schematic LCD Interface (Serial Mode)

9 MEMORY CARD INTERFACE

9.1 Overview

The PNX0101/PNX0102 Memory Card Interface (MCI) is used to connect to the Multi Media Card (MMC) or to the Secure Digital (SD) Card in non-secure mode. The Multi Media Card and Secure Digital are both NAND FLASH type serial data storage media.

Features:

- Conformance with the Multi Media Card specification V2.11.
- Possibility to connect up to 30 cards.

9.2 Application Description

9.2.1 Design Rules

The Memory Card Interface can only be used in combination with the following devices:

- PNX0101/N302
- PNX0102/N102

9.2.2 Application Schematic (Multi Media Card)

The Application Schematic below shows how the MCI should be connected when used as a Multi Media Card Interface.

When the MCI is not used all pins can be left unconnected. In software this part should then be set to IOCONF and all pins as outputs.

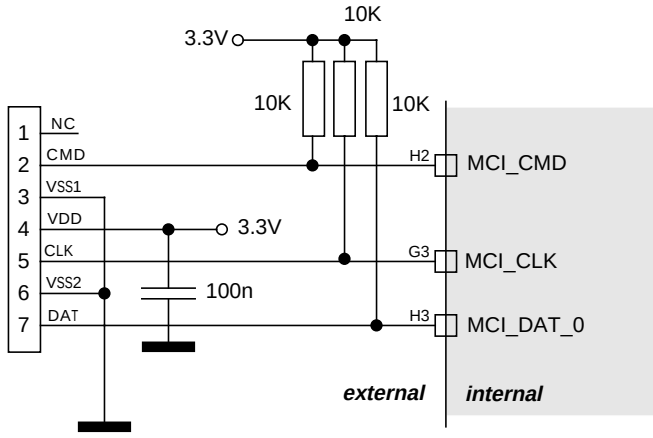


Fig.9 Application Schematic Memory Card Interface (Multi Media Card)

9.2.3 Application Schematic (Secure Digital)

The Application Schemaitc below shows how the MCI should be connected when used as a Secure Digital Card Interface.

When the MCI is not used all pins can be left unconnected. In software this part should then be set to IOCONF and all pins as outputs.

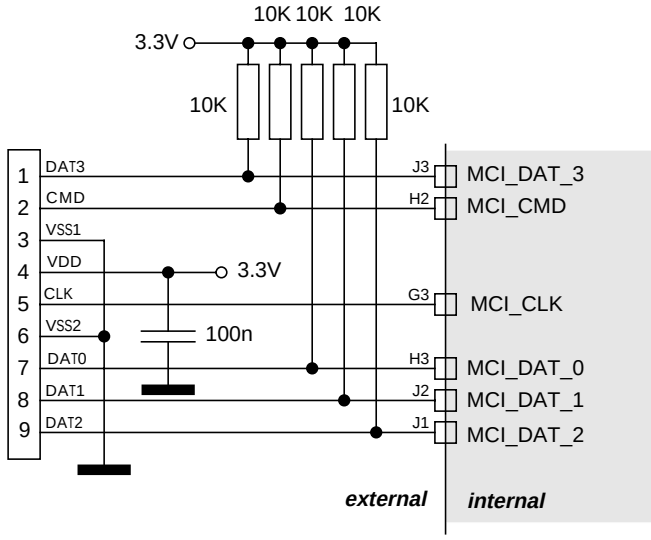


Fig.10 Application Schematic Memory Card Interface (Secure Digital)

10 USB INTERFACE

10.1 Overview

The USB Interface of the PNX0101 is a Full Speed USB Interface (12 Mbits/s) and is USB 2.0 compliant.

The USB Interface of the PNX0102 is a High Speed USB Interface (480 Mbits/s) and is USB 2.0 compliant.

10.2 Application Description

10.2.1 Design Rules

No advisable restrictions.

10.2.2 Application Schematic (Full Speed for PNX0101)

The Application Schematic below shows how the USB Interface should be connected when used as a Full Speed USB Interface (12 Mbits/s).

When the Full Speed USB Interface is not used all pins can be left unconnected. In software this part should be set to IOCONF and all digital I/O pins as outputs, USB_DP and USB_DM are analog pins and won't be affected by this setting.

Note:
The pins that are reserved for the High Speed USB Interface on the PNX0101 can be left unconnected, unless you want to design your Application with the possibility to easily adapt to the PNX0102.

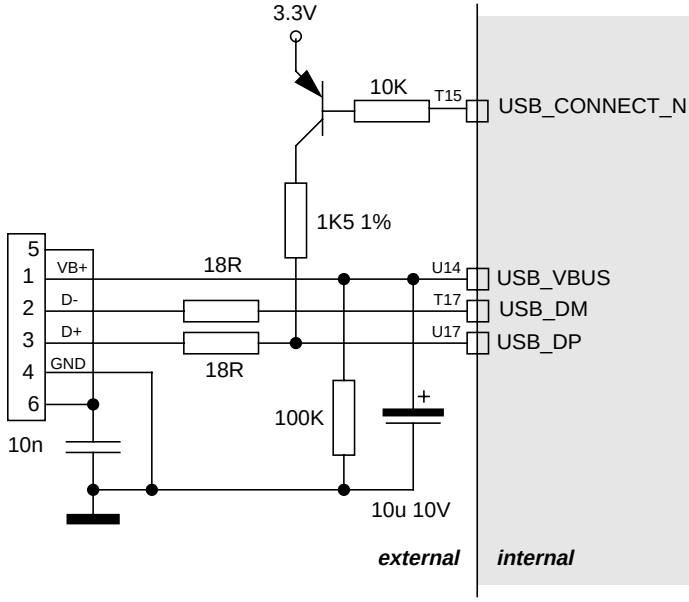


Fig.11 Application Schematic USB Interface (Full Speed)

10.2.3 Application Schematic (High Speed for PNX0102)

The Application Schematic below shows how the USB Interface should be connected when used as a High Speed USB Interface (480 Mbits/s).

The High Speed USB Interface also supports Full Speed (12 Mbits/s).

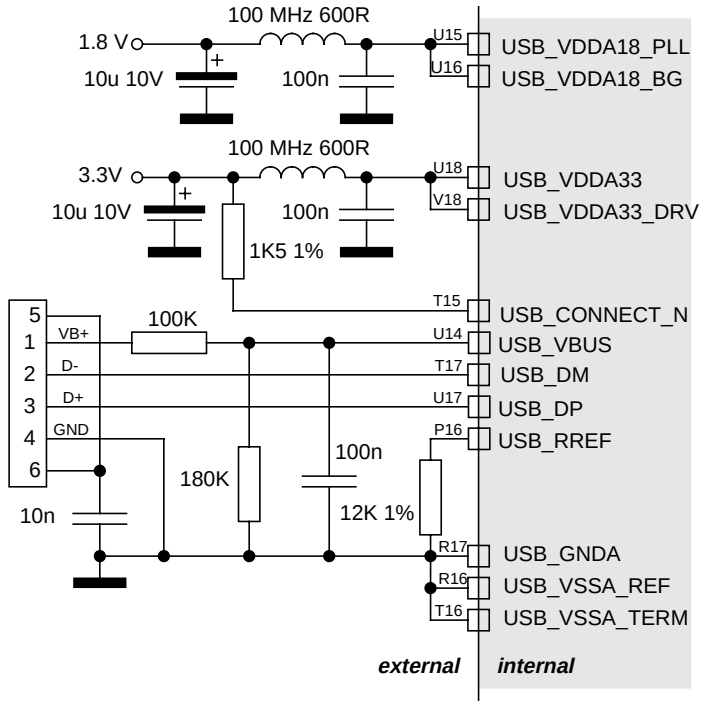


Fig.12 Application Schematic USB Interface (High Speed)

11 JTAG

11.1 Overview

The PNX0101/PNX0102 JTAG Interface can be used to connect the internal ARM7TDMI CPU core to the ARM Multi-ICE™ for software development and debugging.

Table 5 JTAG Selection

JTAG_SEL_ARM	SELECTION
LOW	Application Mode
HIGH	Multi-ICE™

11.2 Application Description

11.2.1 Design Rules

The JTAG Interface can only be used in combination with the following devices:

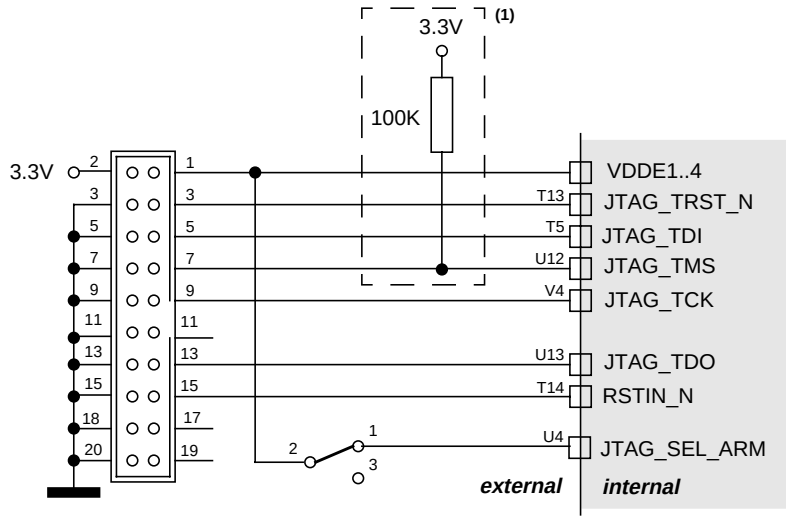
- PNX0101ET/N101, PNX0101ET/N103
- PNX0102ET/N100

11.2.2 Application Schematic (Multi-ICE™)

The Application Schematic below shows how the JTAG Interface should be connected when used with the ARM Multi-ICE™.

The connection between pin 1 of the Multi-ICE™ connector and VDDE1..4 needs to be provided to ensure that the level of the external pads of the PNX0101/PNX0102 is the same as that of the Multi-ICE™.

When the JTAG Interface is not used, for the PNX0101 only the pull up resistor on U12 is still needed, the rest of the components can be removed. The rest of the JTAG Interface is internally foreseen from pull up/down resistors.



(1) Applicable for the PNX0101ET/N101, PNX0101/N102, PNX0101/N103 and PNX0101ET/N202 only!

Fig.13 Application Schematic JTAG (Mullti-ICE™)

12 IIC MASTER/SLAVE INTERFACE

12.1 Overview

The PNX0101/PNX0102 I²C Master/Slave Interface provides a serial interface that meets the I²C bus specification and supports all transfer modes from and to the I²C bus.

Features:

- Supports both the normal mode (100kHz SCL) and the fast mode (400kHz SCL).
- Supports four modes of operation: master transmitter, master receiver, slave transmitter and slave receiver.

12.2 Application Description

12.2.1 Design Rules

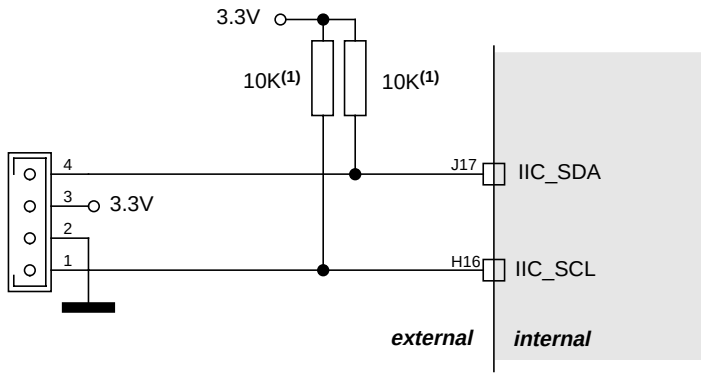
The value of the pull up resistors is not a fixed value, meaning that depending of the application, which can be using normal/fast mode this resistor value needs to be changed to meet the I²C signal specification. Also the load and layout of the I²C lines in the application can play a role in determining the resistor value.

12.2.2 Application Schematic

The Application Schematic below shows how the IIC Master/Slave Interface should be connected when used.

When the IIC Master/Slave Interface is not used the pull up resistors are still needed, the rest of the components can be removed.

For further details please refer to the I²C bus specification.



(1) The pull up resistor value is not a fixed value!

Fig.14 Application Schematic IIC Master/Slave Interface

13 MPMC (MULTI PURPOSE MEMORY CONTROLLER)

13.1 Overview

The Multi Purpose Memory Controller (MPMC) of the PNX0101/PNX0102 supports the interface to a lot of memory types.

- SDRAM, Low Power SDRAM (LPSDRAM)
- ROM, SRAM and FLASH

13.2 Application Description

13.2.1 Design Rules

The Application Schematics given in paragraph 13.2.2 untill 13.2.6 are in principle all based on the fact that only one type of memory is connected to the PNX0101, when making use of multiple types of memory connected to the PNX0101 there are some restrictions:

- **Not restricted:** SDRAM/SYNCFLASH in combination with SRAM(or ROM) or NOR-FLASH according given Application Schematics.
- **Restricted:** SDRAM in combination with NAND-FLASH where $\overline{CE}$ is GPIO driven: see paragraph 13.2.7
- **Restricted:** SRAM in combination with NAND-FLASH where $\overline{CE}$ is GPIO driven: see paragraph: 13.2.8

13.2.2 Application Schematic (SDRAM)

The Application Schematic below shows how the MPMC Interface should be connected when used with a 64 Mbit SDRAM.

The example given is based on a 64Mbit SDRAM, please refer to paragraph 13.3 for reference to documentation describing other configurations.

Example:
MICRON 1M x 16 x 4 SDRAM
MT48LC4M16A2
54-pin TSOP II

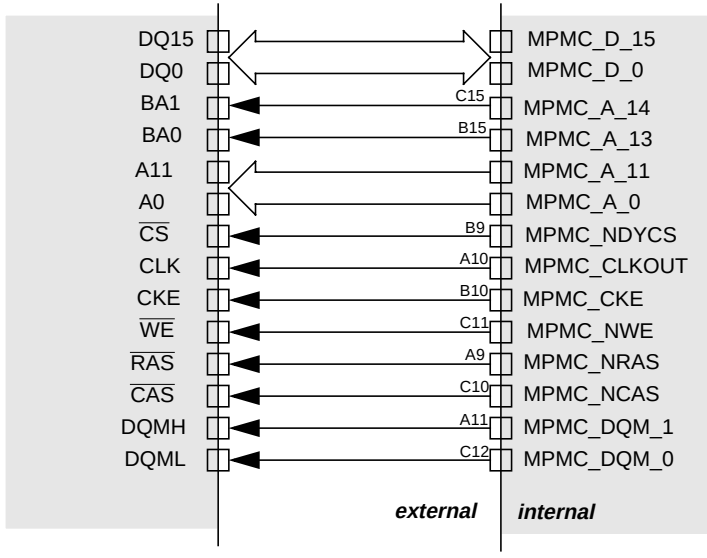


Fig.15 Application Schematic MPMC (SDRAM)

13.2.3 Application Schematic (SYNCFLASH)

The Application Schematic on the next page shows how the MPMC Interface should be connected when used with a 64 Mbit SYNCFLASH.

The example given is based on a 64Mbit SYNCFLASH, please refer to paragraph 13.3 for reference to documentation describing other configurations.

Example:
MICRON 1M x 16 x 4 SYNCFLASH(R) MEMORY
MT28S4M16LC
54-pin TSOP II

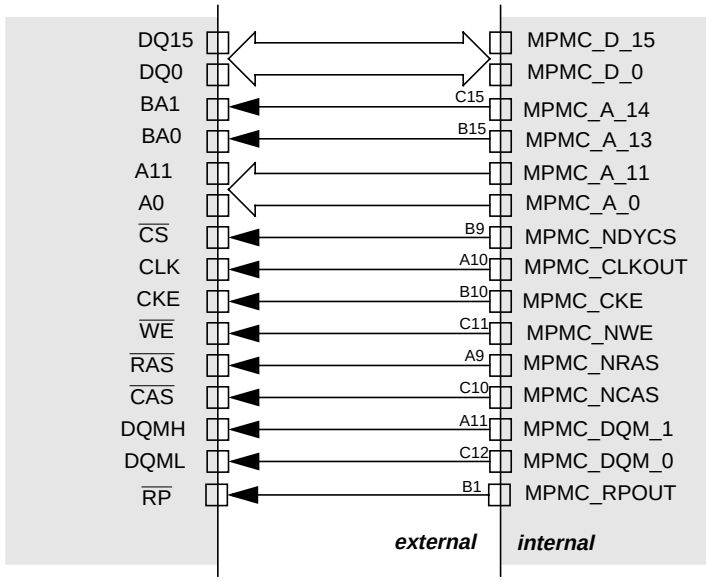


Fig.16 Application Schematic MPMC (SYNCFLASH)

13.2.4 Application Schematic (SRAM)

The Application Schematic on the next page shows how the MPMC Interface should be connected when used with SRAM.

The given example is based on a 16bit width SRAM, where A0 is not the byte/word select. In case of using another 16bit width memory device were A0 is used as byte/word select, MPMC_A_0 should be connected to A1 instead of A0.

Example:
SAMSUNG 1M x 16 Super Low Power SRAM
K6F1616U6A

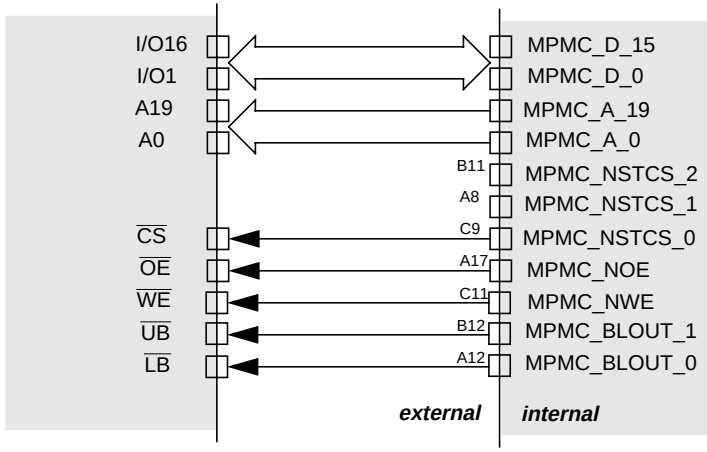


Fig.17 Application Schematic MPMC (SRAM)

13.2.5 APPLICATION SCHEMATIC (NOR-FLASH)

The Application Schematic below shows how the MPMC Interface should be connected when used with NOR-FLASH.

The example given is specific for this device, maybe it is applicable to more devices, but this has not been checked.

Example:
TOSHIBA 2M x 8 / 1M x 16 CMOS FLASH MEMORY
TC58FVT160/B160

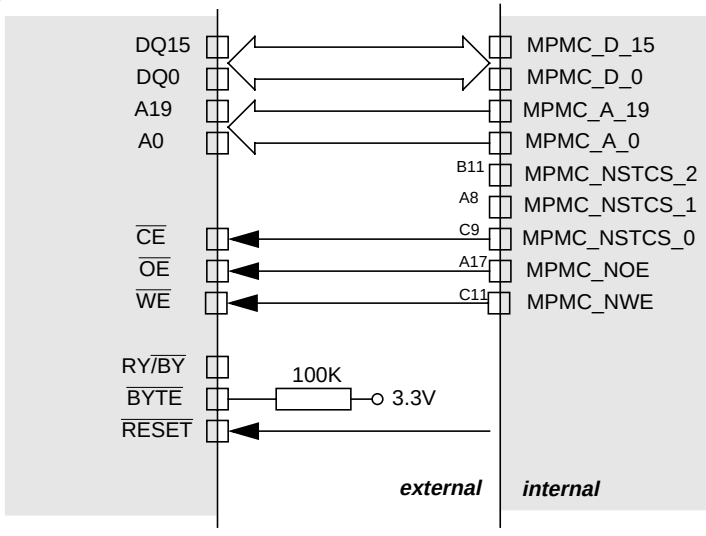


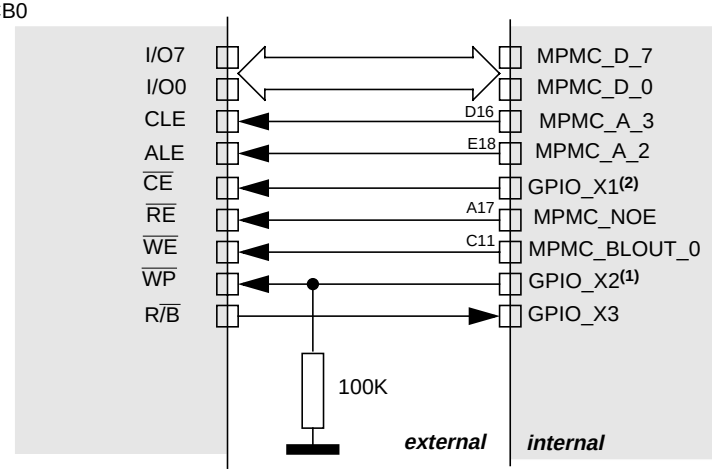
Fig.18 Application Schematic MPMC (NOR-FLASH)

13.2.6 Application Schematic (NAND-FLASH)

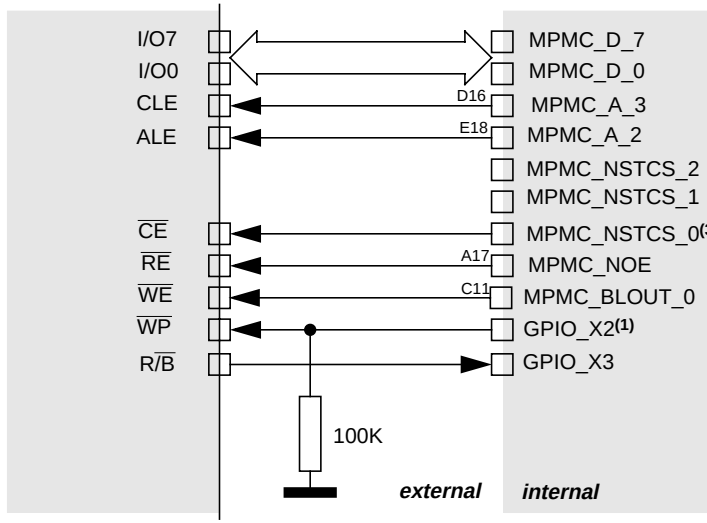
The Application Schematic below shows how the MPMC Interface can be connected when used with NAND-FLASH.

The schematic is very general in setup, and can be used for both Multi Level Cell (MLC) type or regular type of NAND-FLASH, which provide in this type of NAND-FLASH Interface. The use of a GPIO driven $\overline{CE}$ or one that is driven by the Chip Select is dependant of the timing requirements of the NAND-FLASH.

Example:
SAMSUNG 128M x 8 NAND FLASH MEMORY
K9K1G08U0M-YCB0



Example:



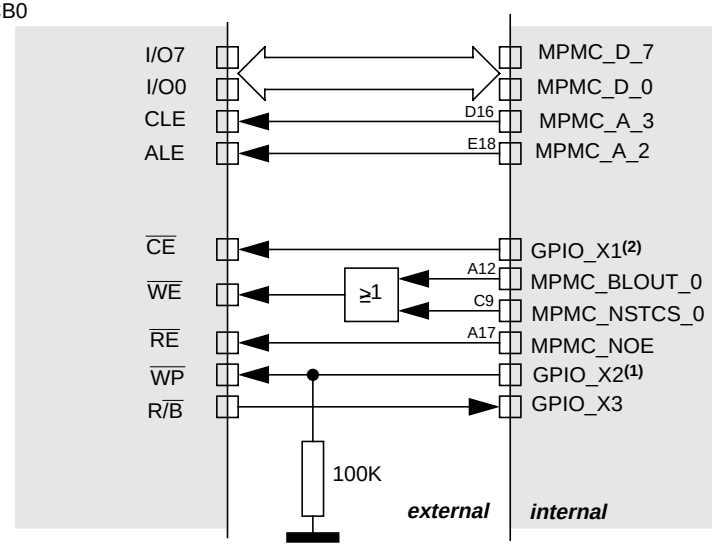
(1) This GPIO should be one which is default defined as an input (Example: UART_RXD)
(2) The $\overline{CE}$ of the NAND-FLASH is GPIO driven
(3) The $\overline{CE}$ of the NAND-FLASH is Chip Select driven

Fig.19 Application Schematic (NAND-FLASH)

13.2.7 Application Schematic (SDRAM and NAND-FLASH)

The Application Schematic on the next page shows how the MPMC Interface can be connected when used with a NAND-FLASH, in combination with an SDRAM. The schematic only shows the connection to the NAND-FLASH the connection to the SDRAM, can be found in paragraph 13.2.2.

Example:
SAMSUNG 128M x 8 NAND FLASH MEMORY
K9K1G08U0M-YCB0



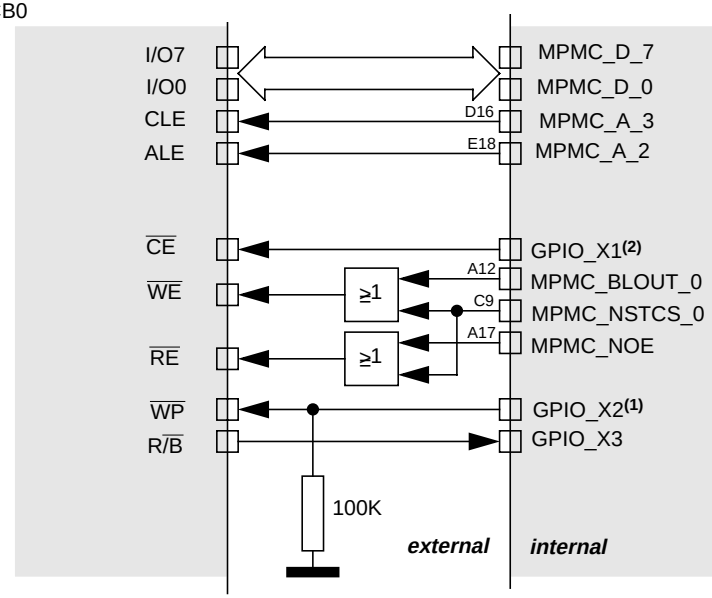
(1) This GPIO should be one which is default defined as an input (Example: UART_RXD)
(2) The $\overline{CE}$ of the NAND-FLASH is GPIO driven

Fig.20 Application Schematic (SDRAM and NAND-FLASH)

13.2.8 Application Schematic (SRAM and NAND-FLASH)

The Application Schematic on the next page shows how the MPMC Interface can be connected when used with a NAND-FLASH, in combination with an SRAM. The schematic only shows the connection to the NAND-FLASH the connection to the SRAM, can be found in paragraph 13.2.4.

Example:
SAMSUNG 128M x 8 NAND FLASH MEMORY
K9K1G08U0M-YCB0



(1) This GPIO should be one which is default defined as an input (Example: UART_RXD)
(2) The $\overline{CE}$ of the NAND-FLASH is GPIO driven

Fig.21 Application Schematic (SRAM and NAND-FLASH)

13.3 References

For more detailed information refer to: ARM Primecell™ MultiPort Memory Controller (PL172) Technical Reference Manual, which can be found at www.arm.com.

14 UART

14.1 Overview

The PNX0101/PNX01012 UART Interface is used to be implemented as a serial interface to for e.g. a modem and is compatible with the industry standards 16650 UARTs.

No full modem interface is included, only the CTS and RTS modem signals are available.

The UART Interface can also be configured as an IrDA (Infrared Digital Association) SIR (Serial InfraRed) Interface, which has a pulse and polarity compliancy with the IrDA Version 1.0 Physical Layer Specification.

14.2 Application Description

14.2.1 Design Rules

No advisable restrictions.

14.2.2 Application Schematic

The Application Schematic below shows how the UART should be connected when used.

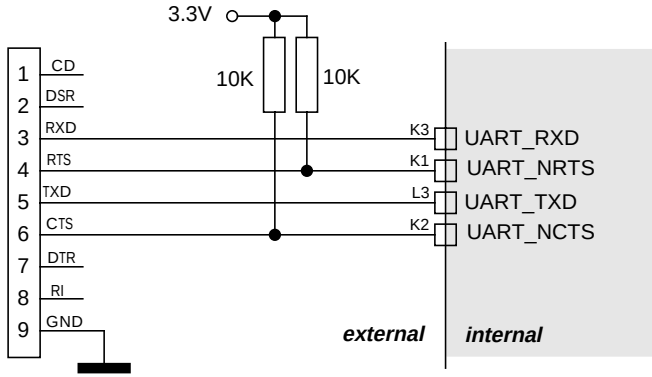


Fig.22 Application Schematic UART

The Application Schematic below shows how the UART should be connected when used as an IrDA SIR.

Example:
ZILOG SIR Transceiver
ZHX1010

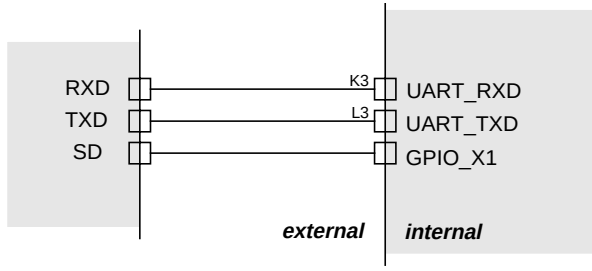


Fig.23 Application Schematic UART (IrDA SIR)

15 IOCONF: MODE SELECTION PINS

15.1 Overview

The Mode Selections pins of the PNX0101/PNX0102 have a double functionality:

- At start up the Mode Selection pins together with the ROMCODE determine in which mode the PNX0101 is going to start up.
- After start up the Mode Selection pins become GPIO pins.

Each mode has its own specific settings for the PNX0101, although it is possible that some modes have some settings in common (e.g. SDRAM initialisation, etc.).

Table 6 Mode Selection - PNX0101/PNX0102

GPIO_3	GPIO_2	SELECTION
LOW	LOW	Mode 0 (flash)
LOW	HIGH	Mode 1 (external SMC bank 0)
HIGH	LOW	Mode 2 (USB download)
HIGH	HIGH	Mode 3 (test mode)

15.2 Application Description

15.2.1 Design Rules

When using the Mode Selection pins as GPIO pins in the design take care of the fact that it is designed in that way that during start up the correct mode is selected.

15.2.2 Application Schematic

The Application Schematic below shows how the Mode Selections pins should be connected when used.

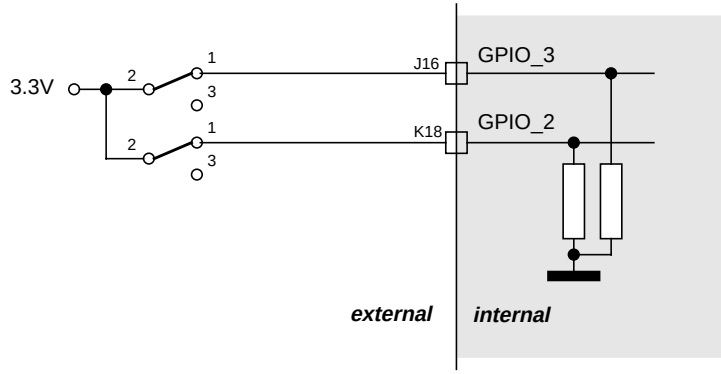


Fig.24 Application Schematic Mode Selection pins

16 IOCONF: GPIO

16.1 Overview

The IOCONF block of the PNX0101/PNX0102 is used to provide individual control and visibility for a relatively large set of pads. In conjunction with a set of pad multiplexers, individual pads can either be switch to normal operation mode, or in GPIO mode. In GPIO mode a pad is fully controllable. Through the IOCONF individual pad levels can be observed in both normal and GPIO mode.

16.2 Application Description

16.2.1 Design Rules

No advisable restrictions.

16.2.2 Application Schematic

The Application Schematic below shows how the IOCONF is build up internally. In software this part can be controlled and set-up. GPIOs can be used for many purposes: from simply controlling and detecting switches to simulating non-provided interfaces.

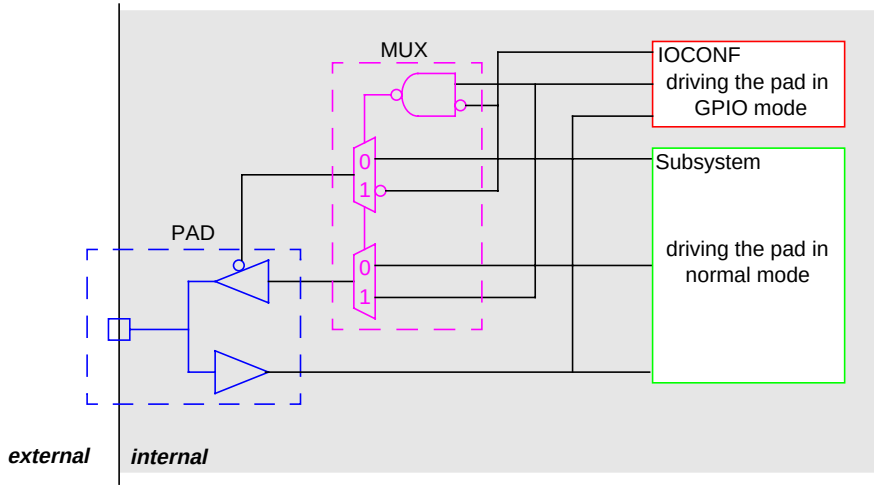


Fig.25 Application Schematic IOCONF

17 DIGITAL SUPPLIES

17.1 Overview

The following supplies of the PNX0101/PNX0102 are referred to as digital supplies:

- VDDI1, VDDI2, VDDI3 and FLASH_VDD_HV.
- VSSI1, VSSI2 and VSSI3.

These supplies are the core supplies to respectively the memory, core and flash.

17.2 Application Description

17.2.1 Design Rules

Decoupling of the digital supplies is done internally and should be sufficient so that for these supplies no external decoupling is needed.

17.2.2 Application Schematic

The Application Schematic below shows how the digital supplies can be connected to an external supply.

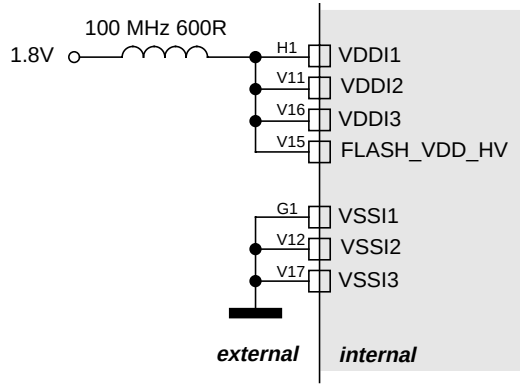


Fig.26 Application Schematic digital supplies

18 PERIPHERAL SUPPLIES

18.1 Overview

The following supplies of the PNX0101/PNX0102 are referred to as peripheral supplies:

- VDDE1, VDDE2, VDDE3 and VDDE4.
- VSSE1, VSSE2, VSSE3 and VSSE4.
- VDDE5 and VDDE6
- VSSE5 and VSSE6

These supplies are respectively the peripheral (I/O) supplies and the MPMC peripheral (I/O) supplies.

18.2 Application Description

18.2.1 Design Rules

Decoupling of the peripheral supplies needs to be done externally.

18.2.2 Application Schematic

The Application Schematic below shows how the peripheral supplies can be connected to an external supply.

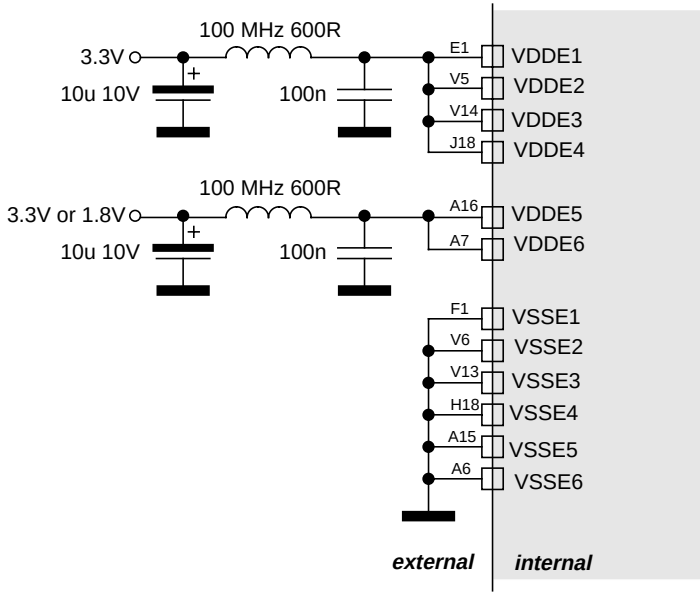


Fig.27 Application Schematic peripheral supplies

19 AUDIO DSP SUBSYSTEM: SPDIF

19.1 Overview

The SPDIF input is part of the Audio DSP Subsystem of the PNX0101/PNX0102.

19.2 Application Description

19.2.1 Design Rules

No advisable restrictions.

19.2.2 Application Schematic

The Application Schematic below shows how the SPDIF input should be connected when used.

When this part is not used the supply must be tied to ground. In software this part must be set in power down.

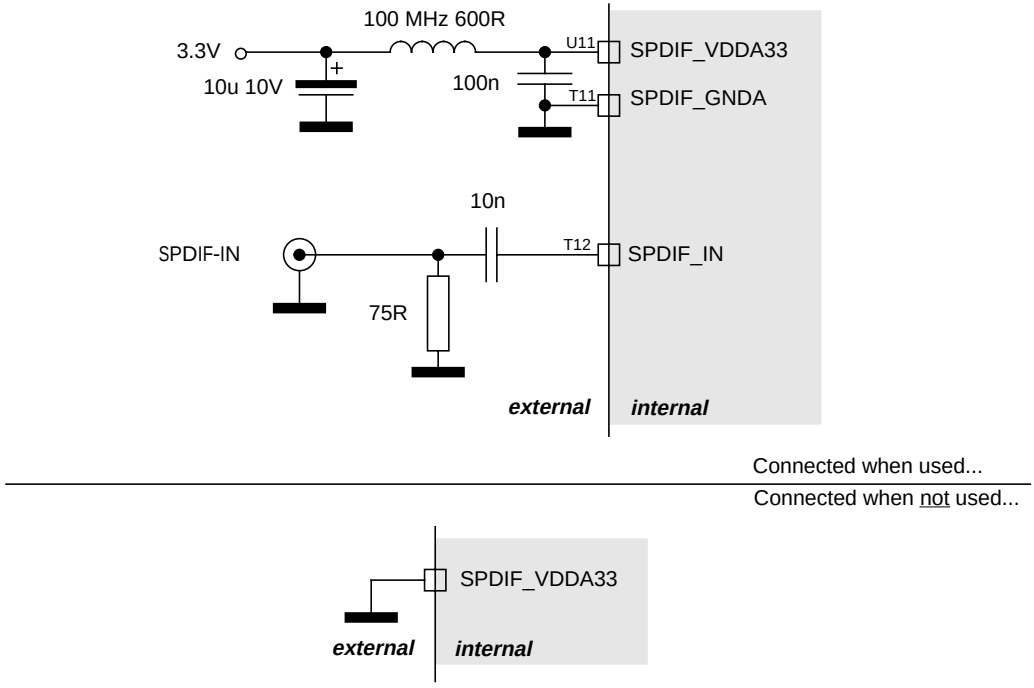


Fig.28 Application Schematic SPDIF/BITSLICER

20 AUDIO DSP SUBSYSTEM: DAI AND DAO INTERFACE

20.1 Overview

The IIS input and output are part of the Audio DSP Subsystem of the PNX0101/PNX0102.

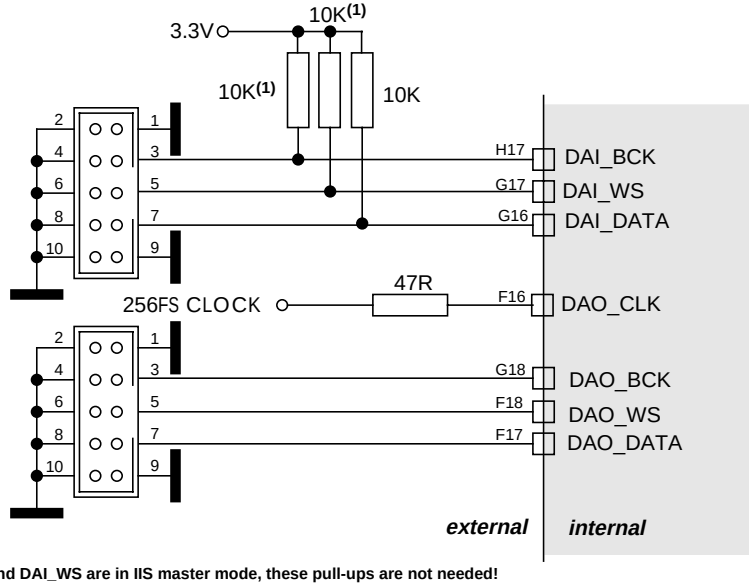
20.2 Application Description

20.2.1 Design Rules

The DAI_BCK and DAI_WS can also be used in IIS master mode, meaning that these inputs can also be switched as outputs to generate a bitclock and word select for a slave device. In this case the slave only returns the data.

20.2.2 Application Schematic

The Application Schematic below shows how the DAI and DAO Interface should be connected when used.



(1) When DAI_BCK and DAI_WS are in IIS master mode, these pull-ups are not needed!

Fig.29 Application Schematic DAI and DAO Interface

21 AUDIO DSP SUBSYSTEM: SDAC

21.1 Overview

The SDAC is a Stereo Digital-to-Analog Converter with interpolation filters and noise shaper for low frequency applications such as portable audio.

Features:

- Interpolation filter that increases the sample rate from $1f_s$ to $128f_s$.
- Third order noise shaper that runs on $128f_s$ or $256f_s$.
- Digital dB-linear volume control in 0.25dB steps.
- Digital de-emphasis for 32kHz, 44.1kHz, 48kHz and 96kHz.
- Selection for $2f_s$ to $8f_s$ upsampling filter characteristics(sharp/slow roll-off).
- Support for $2f_s$ and $8f_s$ input signals:
  - $1f_s$ with full feature support, being de-emphasis, master volume, control and soft mute
  - $2f_s$ with master volume and mute support: required for double speed mode
  - $8f_s$ input with no features supported
- Soft mute.
- Controlled power down sequence to avoid audible plops or clicks.
- Integrated digital silence detection for Left and Right with selectable silence detection time.
- Polarity control.

21.2 Application Description

21.2.1 Design Rules

Because of the low rejection ratio of DAC_VREFP and DAC_VREFN the supply to these pins needs to be very clean to prevent unwanted distorsion in the audio signal. One of the possibilities to do this is to provide a big capacitor between DAC_VREFP and DAC_VREFN.

If even higher audio performance is needed then it is advised to provide an external LDO which is going to provide the supply for the SDAC.

21.2.2 Application Schematic

The Application Schematic on the next page shows how the SDAC should be connected when used.

The schematic shows how to connect the Headphone when it needs to be DC decoupled. This DC decoupling is needed to prevent unwanted DC currents that start running due to the voltage drop over the 150R resistor in the DAC_VREFP supply.

The schematic also shows how to connect the Headphone when it needs to be DC coupled. In this situation DC currents start running due to the voltage drop over the 150R resistor in the DAC_VREFP supply.

Another possibility to prevent unwanted DC currents that start running due to the voltage drop over the 150R resistor is Headphone Reference biasing, this is only possible on the following device:

- PNX0102/N102

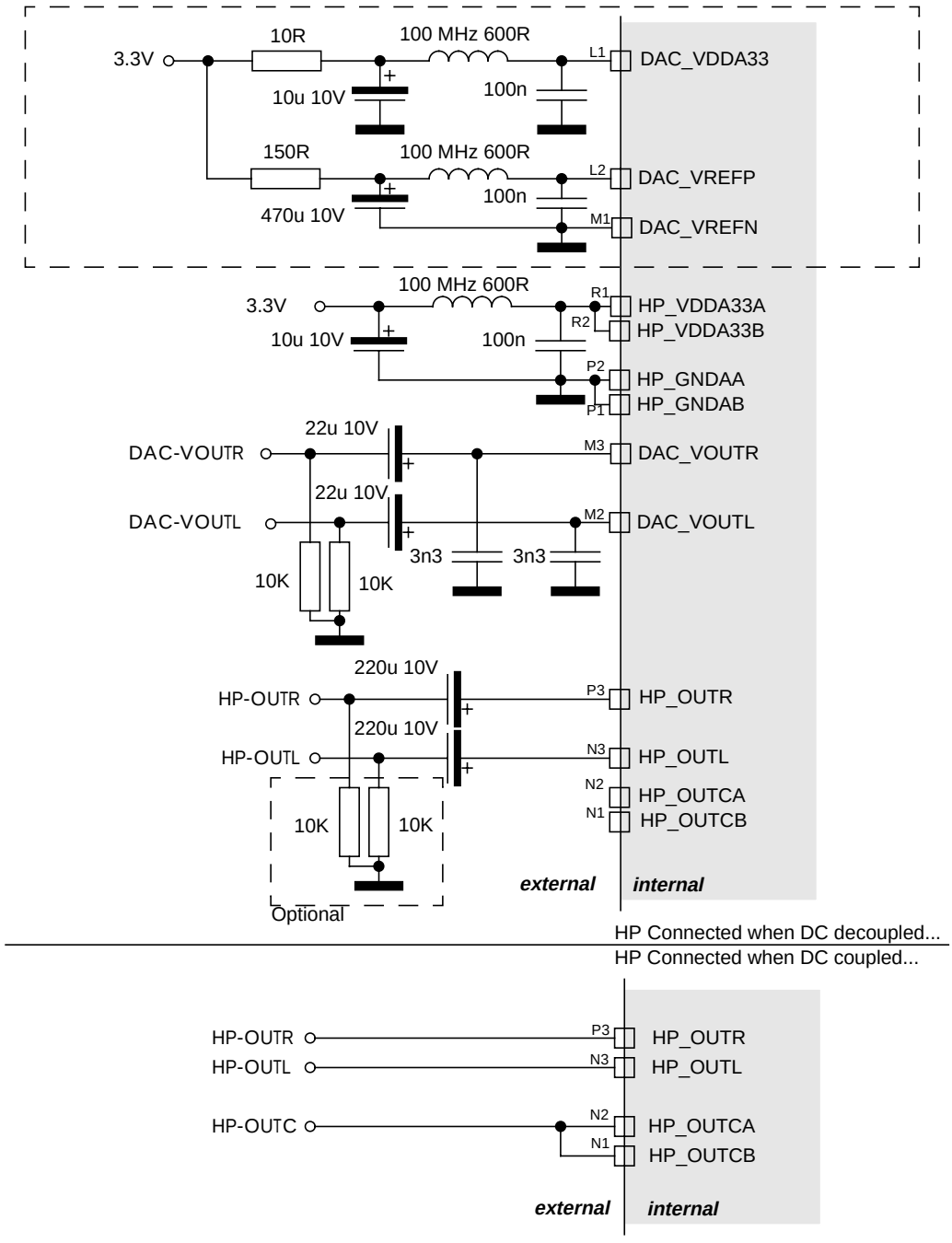
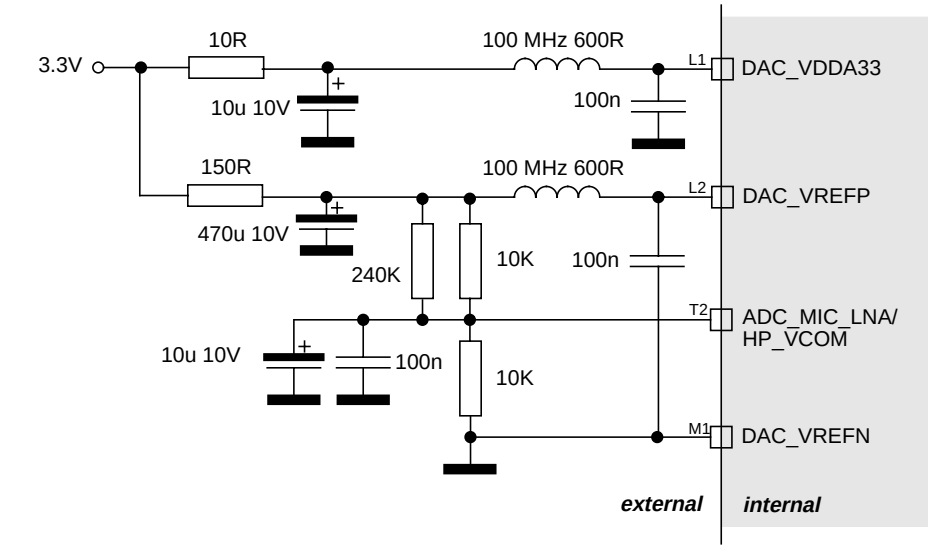


Fig.30 Application Schematic DAC

21.2.3 Application Schematic Headphone Reference biasing

The Application Schematic below shows another possibility to bias the Headphone Reference to prevent unwanted DC currents that start running due to the voltage drop over the 150R resistor.

This Application Schematic should always be used in combination with the previous Application Schematic see Fig.30 and advised is to use a DC decoupled Headphone in combination with a Headphone Reference without biasing and to use a DC coupled Headphone in combination with a Headphone Reference with biasing.



PNX0102/N102 Headphone Reference without biasing

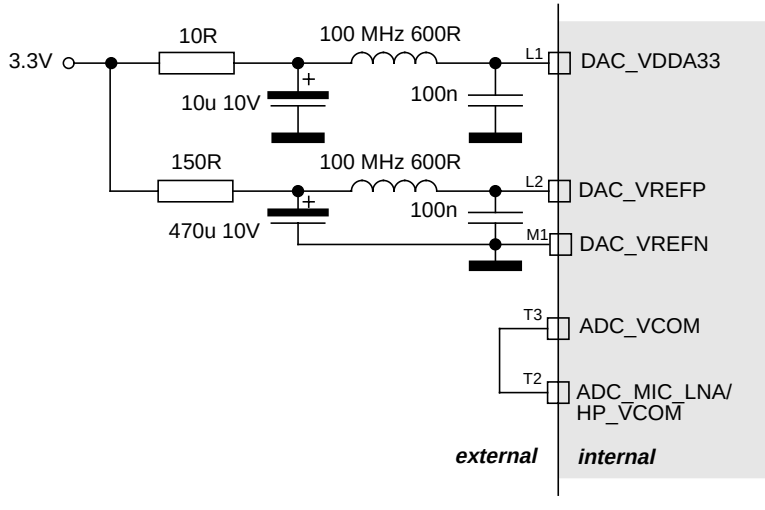


Fig.31 Application Schematic Headphone Reference biasing

22 AUDIO DSP SUBSYSTEM: SADC

22.1 Overview

The SADC is a Stereo Analog-to-Digital Converter with decimation filters for low frequencies applications such as portable audio.

Features:

- Decimation filter that decreases the sample rate from $128f_s$ to $1f_s$.
- Optional DC blocking filters.
- Digital dB-lineair volume control in 0.5dB steps.
- Soft mute with a dB-lineair function.
- Polarity control.

22.2 Application Description

22.2.1 Design Rules

ADC_VINL and ADC_VINR both need to be foreseen with a 1M pull-down resistor to ground. Both resistors need to be as close as possible to the inputs of the IC for the suppresion of idle tones.

22.2.2 Application Schematic

The Application Schematic on the next page shows how the SADC should be connected when used.

When this part is not used the supplies must be connected and the inputs can be left open. In software this part must be set in power down. Application Schematic below shows the connections when not used.

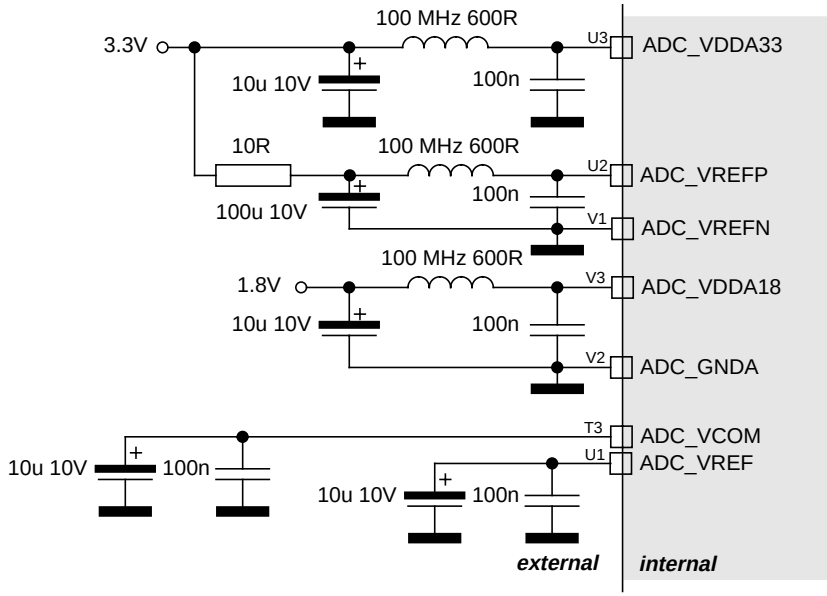


Fig.32 Application Schematic ADC (not used)

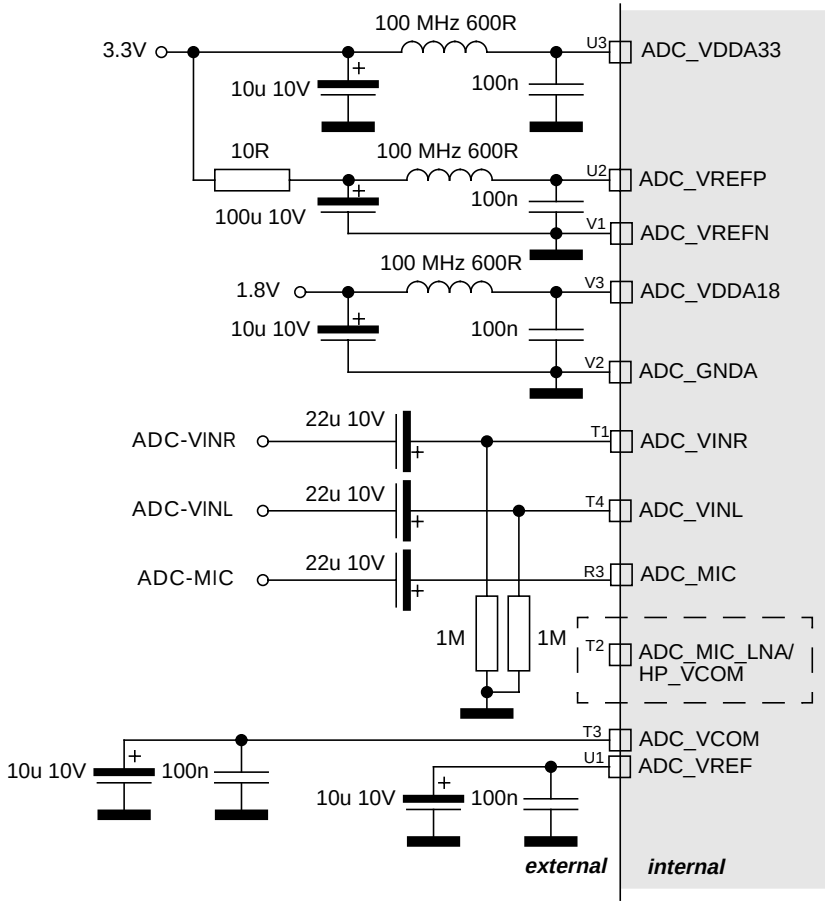


Fig.33 Application Schematic ADC

23 DC/DC CONVERTER

23.1 Overview

The DC/DC converter of the PNX0101/PNX0102 has been implemented to prevent the need of external DC/DC converters for FLASH based designs implementing the PNX0101/PNX0102 and can be powered from one single cell AA(A) battery as well as from USB.

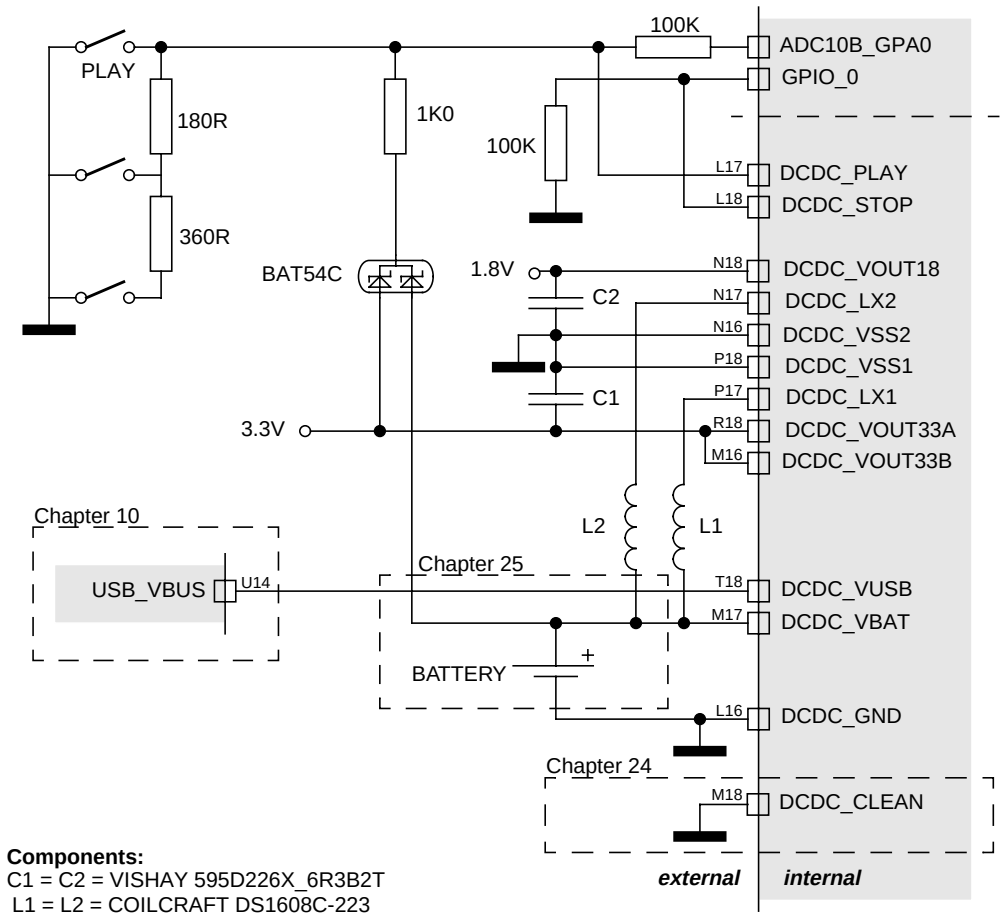
23.2 Application Description

23.2.1 Design Rules

No advisable restrictions.

23.2.2 Application Schematic Internal DC/DC converter

The Application Schematic below shows how the internal DC/DC converter can be connected when used.



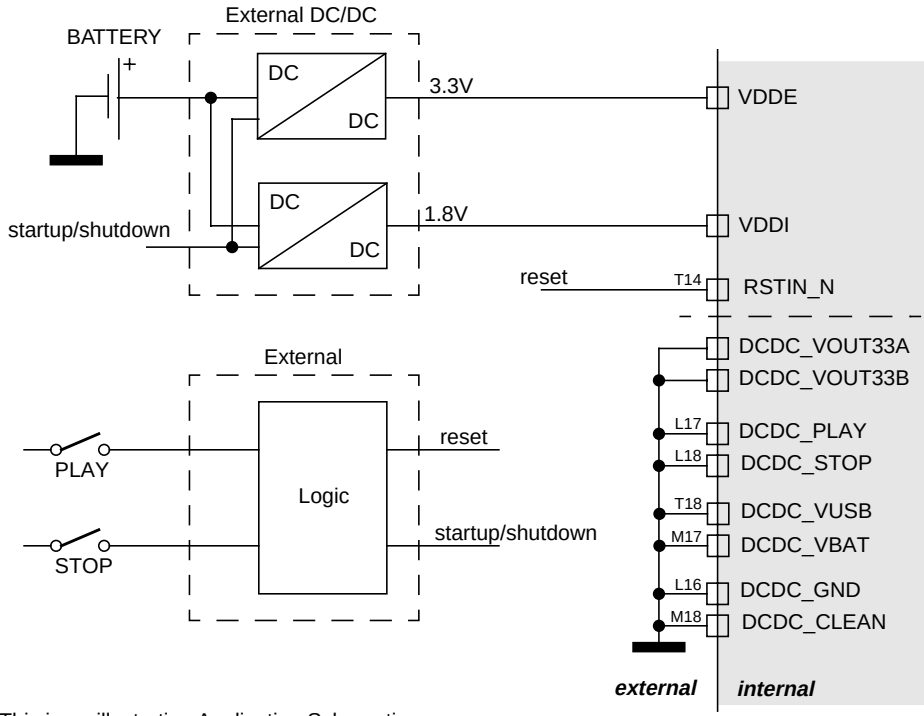
Components:
C1 = C2 = VISHAY 595D226X_6R3B2T
L1 = L2 = COILCRAFT DS1608C-223

Fig.34 Application Schematic internal DC/DC

23.2.3 Application Schematic External DC/DC converter

The Application Schematic below shows how the PNX0101/PNX0102 can be connected by using an external DC/DC converter. In this case some of the internal DCDC pins need to be grounded to prevent the internal DCDC converter from starting up, the rest of the internal DCDC pins which are not on the schematic can be left unconnected.

When applying an external DCDC converter also the startup and shutdown of this device must be handled and offcourse also the power up and down of the PNX0101/PNX0102, therefor a timing diagram has been added.



Note: This is an illustrative Application Schematic

Fig.35 Application Schematic external DC/DC

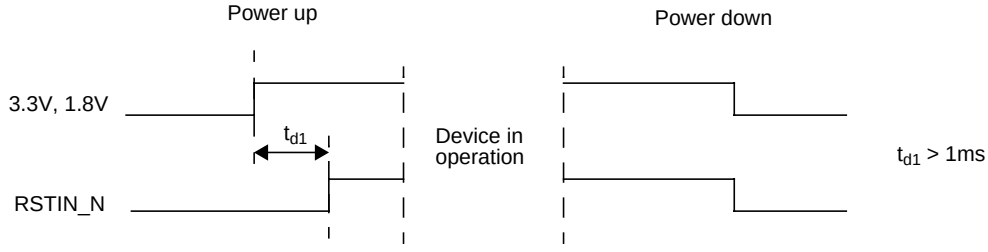


Fig.36 Timing diagram PNX0101/PNX0102 Power up & down procedure

23.2.4 Application Schematic External DCDC converter, with Li-Ion (preliminary)

The Application Schematic below shows how the PNX0101/PNX0102 can be connected by using an external DCDC converter and being powered from a Li-Ion battery.

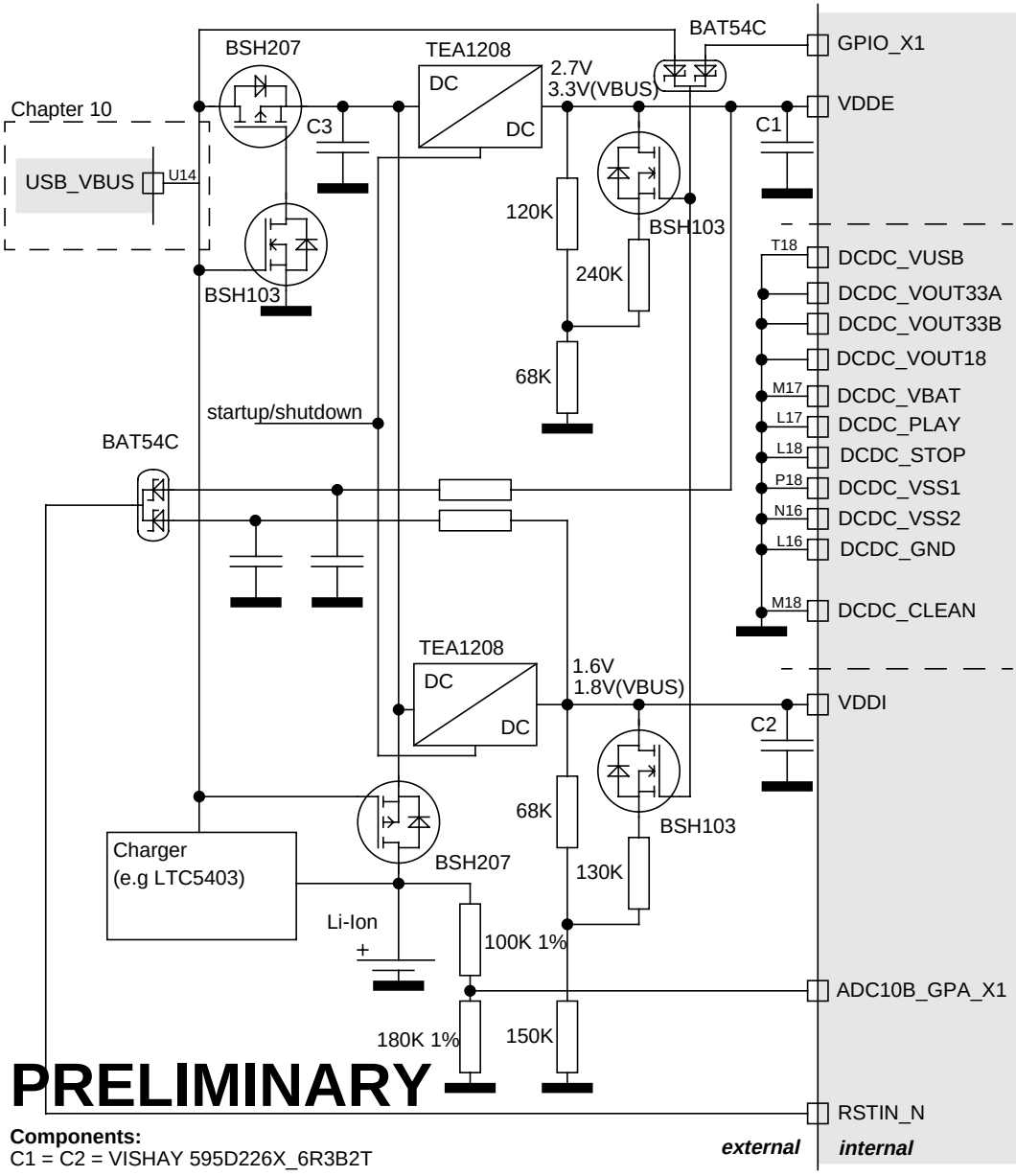


Fig.37 Application Schematic external DCDC for LiIon battery

23.3 Electrical Specification Internal DC/DC converter

The Electrical Specification of Revision 1 is applicable for the following devices:

- PNX0101/N101, PNX0101/N102, PNX0101/N103 and PNX0101/N202

The Electrical Specification of Revision 2 is applicable for the following device:

- PNX0102/N100

The Electrical Specification of Revision 3 is applicable for the following devices:

- PNX0101/N302 and PNX0102/N102

23.3.1 Electrical Specification Internal DC/DC converter Revision 1 (preliminary)

Table 7 Electrical specification Internal DC/DC converter Revision 1

PARAMETER	SYMBOL	MIN.	TYP	MAX	UNIT	NOTE
Junction temperature	Tj	-40	25	125	°C	1
Battery voltage range	Vbat	0.95	1.2	1.6	V	
Idle current Reference and RingOsc	I_idle_ref		500		uA	
Output voltage DC/DC1 max (adjust = 0)	VDC1max		3.5		V	IDC1L=0 Vbat=1.3V
Output voltage DC/DC1 min (adjust = 0)	VDC1min		3.3		V	IDC1L=50mA Vbat=0.9V
Start-up current DC/DC1	IDC1S			25	mA	Vbat=0.95
Load current DC/DC1	IDC1L			100	mA	Vbat=1.3V
DC/DC1 switching frequency	FSW1		1		MHz	
DC/DC1 clock frequency	FCLK1		12		MHz	
DC/DC1 efficiency	n	85		90	%	IDC1L=20mA
DC/DC1 efficiency	n		60		%	IDC1L=50mA Vbat = 0.9V
DC/DC1 Pswitch on resistance	RPON1		0.95		Ohm	
DC/DC1 Nswitch on resistance	RNON1		0.80		Ohm	
Maximum ESR_c	ESR1_max					
Output voltage DC/DC2 max (adjust =0)	VDC2max		1.75		V	IDC2L=0 Vbat=1.3V
Output voltage DC/DC2 min (adjust = 0)	VDC2min		1.68		V	IDC2L=50mA Vbat=0.9V
Start-up current DC/DC2	IDC2S			40	mA	Vbat=0.95V
Load current DC/DC2	IDC2L			100	mA	Vbat=1.3V
DC/DC2 switching frequency	FSW2		1		MHz	
DC/DC2 clock frequency	FCLK2		12		MHz	
DC/DC2 efficiency	n	85		90	%	IDC2L=30mA
DC/DC2 efficiency	n		60		%	IDC2L=75mA Vbat=0.9V
DC/DC2 Pswitch on resistance	RPON2		1.05		Ohm	
DC/DC2 Nswitch on resistance	RNON2		1.15		Ohm	
Maximum ESR_c	ESR2_max					
USB voltage range	Vusb	4.0	5.0	5.5	V	
Idle current	ILDO		700		uA	
Output voltage LDO1	VLDO1		3.33		V	

PARAMETER	SYMBOL	MIN.	TYP	MAX	UNIT	NOTE
Load current LDO1	ILDO1		100		mA	inc. sup. LDO2
Output voltage LDO2	VLDO2		1.78		V	
Load current LDO2	ILDO2		60		mA	

Note 1: Application commercial range (0-70ºC) use -10 to 85ºC as min/max, Tj limits causes problems.

23.3.2 ELECTRICAL SPECIFICATION INTERNAL DC/DC CONVERTER REVISION 2 (PRELIMINARY)

Table 8 Electrical specification Internal DC/DC converter Revision 2

PARAMETER	SYMBOL	MIN.	TYP	MAX	UNIT	NOTE
Junction temperature	Tj	-40	25	125	ºC	1
Battery voltage range	Vbat	tbf	1.2	1.6	V	
Idle current Reference and RingOsc	I_idle_ref		tbf		uA	
Output voltage DC/DC1 max (adjust = 0)	VDC1max		tbf		V	IDC1L=0 Vbat=tbf
Output voltage DC/DC1 min (adjust = 0)	VDC1min		tbf		V	IDC1L=tbf Vbat=0.9V
Start-up current DC/DC1	IDC1S			tbf	mA	Vbat=tbf
Load current DC/DC1	IDC1L			tbf	mA	Vbat=tbf
DC/DC1 switching frequency	FSW1		1		MHz	
DC/DC1 clock frequency	FCLK1		12		MHz	
DC/DC1 efficiency	n	tbf		tbf	%	IDC1L=tbf
DC/DC1 efficiency	n		tbf		%	IDC1L=tbf Vbat = 0.9V
DC/DC1 Pswitch on resistance	RPON1		tbf		Ohm	
DC/DC1 Nswitch on resistance	RNON1		tbf		Ohm	
Maximum ESR_c	ESR1_max					
Output voltage DC/DC2 max (adjust =0)	VDC2max		tbf		V	IDC2L=0 Vbat=tbf
Output voltage DC/DC2 min (adjust = 0)	VDC2min		tbf		V	IDC2L=tbf Vbat=0.9V
Start-up current DC/DC2	IDC2S			tbf	mA	Vbat=tbf
Load current DC/DC2	IDC2L			tbf	mA	Vbat=tbf
DC/DC2 switching frequency	FSW2		1		MHz	
DC/DC2 clock frequency	FCLK2		12		MHz	
DC/DC2 efficiency	n	tbf		tbf	%	IDC2L=tbf
DC/DC2 efficiency	n		tbf		%	IDC2L=tbf Vbat=0.9V
DC/DC2 Pswitch on resistance	RPON2		tbf		Ohm	
DC/DC2 Nswitch on resistance	RNON2		tbf		Ohm	
Maximum ESR_c	ESR2_max					
USB voltage range	Vusb	4.0	5.0	5.5	V	
Idle current	ILDO		tbf		uA	
Output voltage LDO1	VLDO1		tbf		V	

PARAMETER	SYMBOL	MIN.	TYP	MAX	UNIT	NOTE
Load current LDO1	ILDO1		tbf		mA	inc. sup. LDO2
Output voltage LDO2	VLDO2		tbf		V	
Load current LDO2	ILDO2		tbf		mA	

Note 1: Application commercial range (0-70ºC) use -10 to 85ºC as min/max, Tj limits causes problems.

23.3.3 Electrical Specification Internal DC/DC converter Revision 3 (preliminary)

Table 9 Electrical specification Internal DC/DC converter Revision 3

PARAMETER	SYMBOL	MIN.	TYP	MAX	UNIT	NOTE
Junction temperature	Tj	-40	25	125	ºC	1
Battery voltage range	Vbat	tbf	1.2	1.6	V	
Idle current Reference and RingOsc	I_idle_ref		tbf		uA	
Output voltage DC/DC1 max (adjust = 0)	VDC1max		tbf		V	IDC1L=0 Vbat=tbf
Output voltage DC/DC1 min (adjust = 0)	VDC1min		tbf		V	IDC1L=tbf Vbat=0.9V
Start-up current DC/DC1	IDC1S			tbf	mA	Vbat=tbf
Load current DC/DC1	IDC1L			tbf	mA	Vbat=tbf
DC/DC1 switching frequency	FSW1		1		MHz	
DC/DC1 clock frequency	FCLK1		12		MHz	
DC/DC1 efficiency	n	tbf		tbf	%	IDC1L=tbf
DC/DC1 efficiency	n		tbf		%	IDC1L=tbf Vbat = 0.9V
DC/DC1 Pswitch on resistance	RPON1		tbf		Ohm	
DC/DC1 Nswitch on resistance	RNON1		tbf		Ohm	
Maximum ESR_c	ESR1_max					
Output voltage DC/DC2 max (adjust =0)	VDC2max		tbf		V	IDC2L=0 Vbat=tbf
Output voltage DC/DC2 min (adjust = 0)	VDC2min		tbf		V	IDC2L=tbf Vbat=0.9V
Start-up current DC/DC2	IDC2S			tbf	mA	Vbat=tbf
Load current DC/DC2	IDC2L			tbf	mA	Vbat=tbf
DC/DC2 switching frequency	FSW2		1		MHz	
DC/DC2 clock frequency	FCLK2		12		MHz	
DC/DC2 efficiency	n	tbf		tbf	%	IDC2L=tbf
DC/DC2 efficiency	n		tbf		%	IDC2L=tbf Vbat=0.9V
DC/DC2 Pswitch on resistance	RPON2		tbf		Ohm	
DC/DC2 Nswitch on resistance	RNON2		tbf		Ohm	
Maximum ESR_c	ESR2_max					
USB voltage range	Vusb	4.0	5.0	5.5	V	
Idle current	ILDO		tbf		uA	
Output voltage LDO1	VLDO1		tbf		V	

PARAMETER	SYMBOL	MIN.	TYP	MAX	UNIT	NOTE
Load current LDO1	ILDO1		tbf		mA	inc. sup. LDO2
Output voltage LDO2	VLDO2		tbf		V	
Load current LDO2	ILDO2		tbf		mA	

Note 1: Application commercial range (0-70ºC) use -10 to 85ºC as min/max, Tj limits causes problems.

24 EFLASH

24.1 Overview

The so called eFlash is the internal Flash of the PNX0101 with a size of 4Mbit and 8Mbit for the PNX0102, which can be used to store program code or persistant parameters.

- Program code: the excution code of the application.
- Persistant parameters: settings which need to be kept stored before the application is turned off.

24.2 Application Description

24.2.1 Design Rules

The eFlash workaround is only needed in combination with the following devices:

- PNX0101/N101, PNX0101/N102 and PNX0101/N103

In principle there are three situations where the eFlash needs to be programmed::

- Device Firmware Upgrade (DFU): when the program code is downloaded via USB and stored in the eFlash.

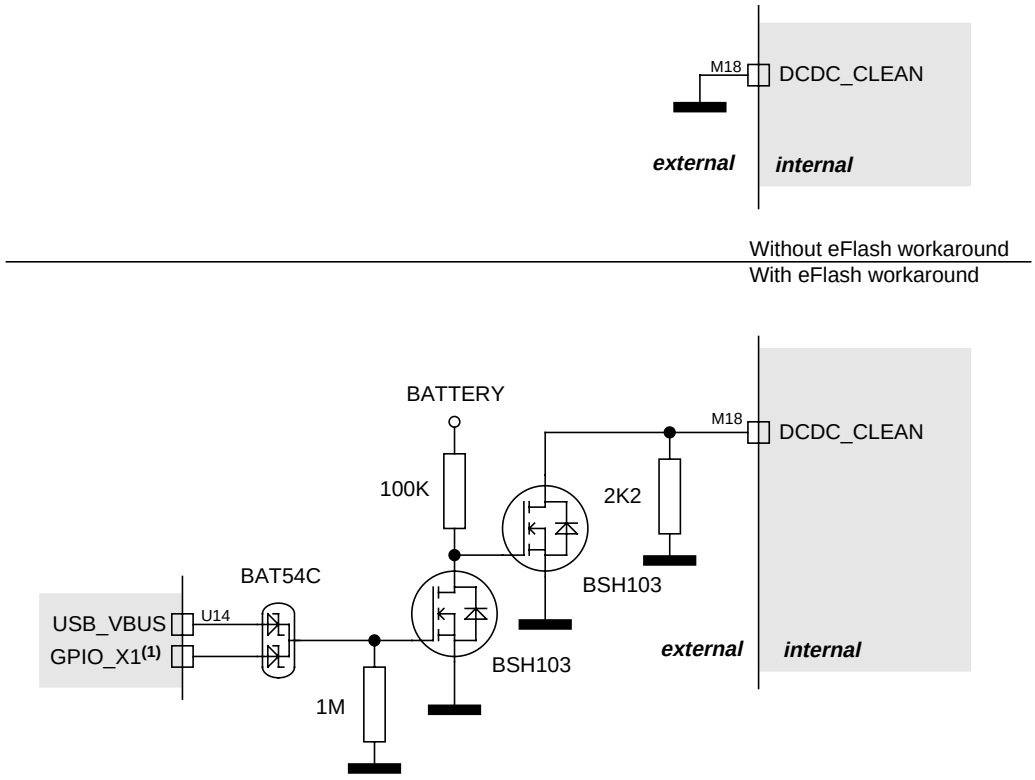
  DFU can be done in two situations, when the device is factory programmed or when the device is being upgraded at the Customer, in both situations this is done via USB. When the USB is connected and the PNX0101 works on its internal DC/DC converter, both LDOs take over, due to the minimal required programming voltage of the eFlash which is recommended at 1.85V the voltage level of LDO2 is to low. To lift this voltage level the DCDC_CLEAN needs to be foreseen with a 2K2 resistor to ground. Both voltage levels of LDO1 and LDO2 will be lifted approx. with 0.15V.
- Firmware Upgrade: when the program code is stored on for example the NAND-Flash and needs to be stored in the eFlash.

  This upgrade needs to be done when the PNX0101 is working on its internal DC/DC converter, then the DC/DC level settings need to be changed. These level settings need to be changed to the minimal required voltage level of 1.85V. The Internal DC/DC converter in not able to create this required voltage level.
- Application mode: when persistant parameters need to be stored in the eFlash

  When persistant parameters need to be stored in the eFlash, and the PNX0101 is working on its internal DC/DC converter, then the DC/DC level settings need to be changed. These level settings need to be changed to the minimal required voltage level of 1.85V. The Internal DC/DC converter is not able to create this required voltage level.

24.2.2 Application Schematic eFlash workaround

The Application Schematic on the next page shows how the PNX0101/PNX0102 can be connected when the eFlash workaround needs to be implemented or not, note that this schematic is additional to the Application Schematic of the Internal DCDC (Fig.34).



(1) This GPIO should be one which is default defined as an input (Example: GPIO_1)

Fig.38 Application Schematic eFlash workaround

25 BATTERY CHARGER

25.1 Overview

The PNX0101/PNX0102 is designed to operate on one single cell AA(A) battery, which can either be a rechargeable or a non-rechargeable type.

When a rechargeable battery is used, it is possible to use the PNX0101/PNX0102 to charge the battery either via the USB port or via an external DC supply. Both NiCd and NiMH rechargeable batteries are supported.

25.2 Application Description

25.2.1 Charging Principles

There are three types of charging principles:

- Slow charger - also known as ‘overnight charger’ or ‘normal charger’, the slow-charger applies a fixed charge rate of about 0.1C (one tenth of the rated capacity) for as long as the battery is connected. Typical charge time is 14 to 16 hours. In most cases, no full-charge detection occurs to switch the battery to a lower charge rate at the end of the charge cycle.
- Quick charger - or so called ‘rapid charger’, is one of the most popular. It is positioned between the slow charger and the fast charger, both in terms of charging time and price. Charging takes 3 to 6 hours and the charge rate is around 0.3C. Charge control is required to terminate the charge when the battery is ready. Batteries last longer if charged with higher currents, provided they remain cool and are not overcharged.
- Fast charger - The fast charger offers several advantages over the other chargers, the obvious one is shorter charge times. The charge time is based on the charge rate, the battery’s state of charge, it’s rating and the chemistry. At a 1C charge rate, an empty NiCd/NiMH typically charges in a little more than one hour. When a battery is fully charged, it is possible to switch to a topping charge mode governed by a timer that completes the charge cycle at a reduced charge current. Once fully charged, the charger switches to trickle charge. This maintenance charge compensates for the self-discharge of the battery.

The C-rate is a unit by which charge and discharge currents are scaled. A charge current of 1000mAh or 1C, will charge a 1000mAh battery in slightly more than one hour. A 1C discharge lasts one hour.

Full-charge detection is based on a combination of voltage drop at full charge (negative delta V), rate-of-temperature-increase (dT/dt), absolute temperature and timeout timers. The charger utilizes whatever comes first to terminate the fast-charge.

The PNX0101/PNX0102 can support all three types of charge methods mentioned above. However the intelligence must be build into the software code of the CPU which is controlling the charger.

25.2.2 Design Rules

Charge current calculation:

V_{usbmin}=4.75 volt $V_{olGPIO[x]}$=0.4 volt

V_{usbmax}=5.25 volt $V_{olGPIO[x]}$=0.0 volt

Minimum charge current:

V_{baseT1} = (470/(820+470)) * (4.75-0.4) + 0.4 = 1.98 V

$V_{Rc} = V_{usb} - V_{cTc}$ = 4.75 - (1.98 +1.4) = 1.37 V

I_{Rcmin} = 1.37/Rc

Maximum charge current:

V_{baseT1} = (470/(820+470)) * 5.25 = 1.91 V

$V_{Rc} = V_{usb} - V_{cTc} = 5.25 - (1.91 + 1.4) = 1.94$ V

$I_{Rcmax} = 1.94/Rc$

The absolute maximum current drawn from the USB port is 500mA. This means that when using USB only a slow and quick charger can be build for 1500mA rechargable batteries. In that case the value of Rc must be 3.9 ohm. The dissipation of the resistor Rc and transistor Tc must be taken into account when doing so.

25.2.3 Application Schematic

The Application Schematic below shows how the Battery Charger should be connected when used. Please note that this schematic is additional to the Application Schematic of the Internal DCDC (Fig.35).

Example:
Tc = PNP Darlington (e.g. Philips BST60)

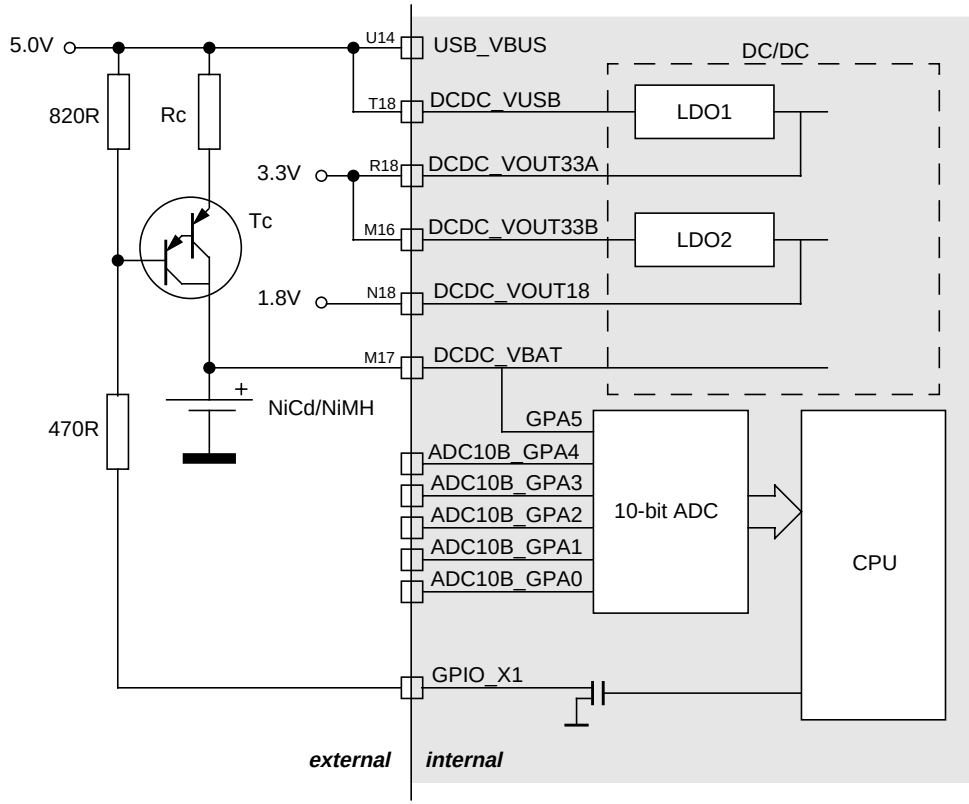


Fig.39 Application Schematic Battery Charger (USB)

25.2.4 Application Software

To be able to detect the voltage drop at a fully charged battery the voltage across the battery must be measured. The DCDC_VBAT pin is internally connected to the GPA5 input of the 10-bit AD Convertor, this can be used to measure the voltage across the battery. Each new measured voltage is compared with the old stored one. If the new sampled value

is higher than the stored one, this new value is stored. When the new measured value is lower than the stored one, between certain margins, the battery can be assumed full.

The 10-bit AD Convertor can detect voltage steps of 3.2 mV @ ADC10B_VDDA33 = 3.3V can be measured, also taken into account the accuracy of +/- 1 LSB, the voltage drop measured must be -10 mV below the peak voltage measured to detect the fully charged state. In this way ΔVbat/Vbat=-0.7%. The interval at which the voltage is measured can be set from 5 to 30 seconds, this is not so critical.

When measuring the voltage, the charging must be stopped, typical this time can be set to t_{sense}=50ms. After this t_{sense} time, the voltage must be measured and the charging can be continued.

When the full state is reached, the charger can go into trickle charge mode. This is done by changing the duty cycle of the GPIO signal which is driving the charge transistor. The recommended trickle charge for Nickel-Cadmium is between 0.05C and 0.1C. Because of memory concerns and compatibility with Nickel-Metal-Hydride, the trickle charge is set as low as possible.

One remark about the GPIO pin which is driving the base of the Tc transitor. This must be set to an open drain N type, otherwise the Tc transistor can not be switched off.

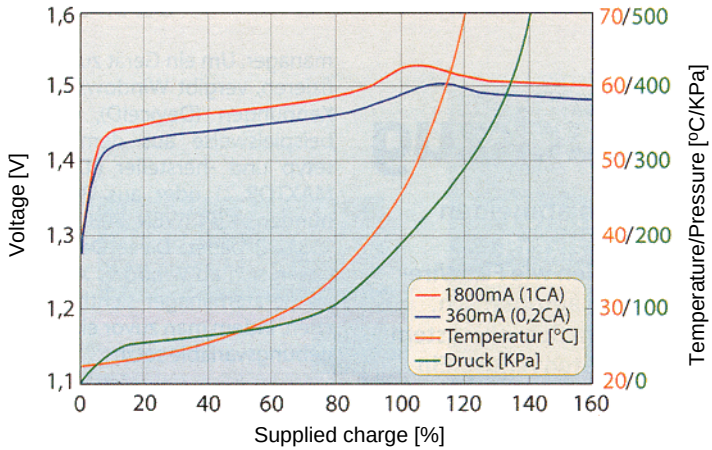


Fig.40 Typical charging curve of a NiHM battery

25.3 References

For more detailed information refer to: www.batteryuniversity.com

26 LIST OF REFERENCES

The following documents will be or will come available via Customer Support or your Local Support.

Table 10 Document references

	TYPE	TITLE	REV.	DATE OF ISSUE
1	Application Note	PNX0101 Li-ion batteries	1.1	27 October 2003
2	Application Note	PNX0101 connected to ISP1581 USB HS	-	-
3	Application Note	PNX0101 connected to ATA	1.0	9 April 2004
4	Application Note	PNX0101 connected to ISP1362 USB OTG	1.0	9 April 2004
5	Application Note	PNX0101 connected to ISP1582 USB HS	-	-

27 DC CHARACTERISTICS

$V_{DDE<1:6>}$ = 3.3 V; $V_{DDI<1:3>}$ = 1.8 V; T_{amb} = 25 ºC; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply Voltages						
$V_{DDE<1:4>}$	Peripheral (I/O) supply		3.0	3.3	3.6	V
$V_{DDE<5:6>}$	Peripheral (I/O) supply of the MPMC pads		1.8	3.3	3.6	V
$V_{DDI<1:3>}$	Core supply voltage		1.65	1.8	1.95	V
DCDC_VBAT	Battery input voltage range		0.9	1.2	1.6	V
FLASH_VDD_HV	Embedded flash supply		1.65	1.8	1.95	V
XTALL_VDDA18	Analog supply voltage for 32kHz XTAL osc. and PLLs		1.65	1.8	1.95	V
XTALH_VDDA18	Analog supply voltage for 12MHz XTAL osc.		1.65	1.8	1.95	V
SPDIF_VDDA33	Analog supply SPDIF input		3.0	3.3	3.6	V
ADC10B_VDDA33	Analog supply voltage, 10-bit measure/control ADC		3.0	3.3	3.6	V
ADC_VDDA33	Analog supply ADC		3.0	3.3	3.6	V
ADC_VDDA18	Analog supply ADC		1.65	1.8	1.95	V
DAC_VDDA33	Analog supply DAC		3.0	3.3	3.6	V
HP_VDDA33A/ HP_VDDA33B	Headphone analog supply		3.0	3.3	3.6	V
Supply Currents (depend heavily on the application)						
$I_{DDE<1:4>}$	Peripheral (I/O) supply current		-	tbf	-	mA
$I_{DDE<5:6>}$	Peripheral (I/O) supply current of the MPMC pads		-	tbf	-	mA
$I_{DDI<1:3>}$	Core supply current		-	tbf	-	mA
DCDC_VBAT	Battery input supply current		-	tbf	-	mA
XTALL_VDDA18	Analog supply current for 32kHz XTAL osc. and PLLs	Oscillation	-	300	-	uA
		Power down	-	-	10	nA
XTALH_VDDA18	Analog supply current for 12MHz XTAL osc.	Oscillation	-	300	-	uA
		Power down	-	-	10	nA
SPDIF_VDDA33	Analog supply current SPDIF input	Normal	-	tbf	-	mA
		Power down	-	-	-	uA
ADC10B_VDDA33	Analog supply current 10-bit measure/control ADC	Normal	-	-	400	uA
		Power down	-	-	< 1	uA
ADC_VDDA33	Analog supply current ADC	Normal	-	-	-	mA
		Power down	-	-	-	uA
DAC_VDDA33	Analog supply current DAC	Normal	-	tbf	-	mA
		Power down	-	tbf	-	uA
HP_VDDA33A/ HP_VDDA33B	Headphone analog supply current	Normal	-	-	-	mA
		Power down	-	-	-	uA

28 AC CHARACTERISTICS

$V_{DDE<1:6>}$ = 3.3 V; $V_{DDI<1:3>}$ = 1.8 V; T_{amb} = 25 ºC; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
10-bit ADC static characteristics					
n	resolution	2		10	bit
INL	integral non linearity			+/- 1	LSB
DNL	differential non linearity			+/- 1	LSB
OSe	offset error	-20		+20	mV
FSe	full scale error	-20		+20	mV
10-bit ADC dynamic characteristics					
ENOB	effective number of bits, f_{in} = 1 kHz		9.46		bit
	effective number of bits, f_{in} = 100 kHz		9.38		bit
F_{smpl}	sampling rate	400 (10-bit)	-	1500 (2-bit)	KS/s
t_{conv}	conversion time	3 (2-bit)	-	11 (10-bit)	clk cycles
SADC dynamic characteristics					
B	bandwidth			20	kHz
THD+N	THD+N at 0 dB, f_{in} = 1kHz		tbf		dB
DR	THD+N at -60 dB, f_{in} = 1kHZ, A-weighted		tbf		dB(A)
S/N	signal-to-noise ratio		tbf		dB(A)
SDAC dynamic characteristics					
R_{OUT}	output resistance	0.7	1	1.3	kΩ
R_L	load resistance	10			kΩ
THD+N	THD+N at 0 dB, f_{in} = 1kHz, uni-directional DWA		tbf		dB
DR	THD+N at -60 dB, f_{in} = 1kHz, uni-directional DWA, A-weighted		tbf		dB(A)
S/N	signal-to-noise ratio, uni-directional DWA, A-weighted		tbf		dB(A)
THD+N	THD+N at 0 dB, f_{in} = 1kHz, bi-directional DWA		tbf		dB
DR	THD+N at -60 dB, f_{in} = 1kHz, bi-directional DWA, A-weighted		tbf		dB(A)
S/N	signal-to-noise ratio, bi-directional DWA, A-weighted		tbf		dB(A)
α_{CS}	channel separation		tbf		dB

29 ABBREVIATIONS

Table 11 Abbreviations used in this document

ABBREVIATION	EXPLANATION
Hardware related	
ADPCM	Adaptive Delta Plus Code Modulation
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
ARM	Advanced RISC Machines
ATU	Audio Transfer Unit
ATX	Analog Transceiver
CTU	Control Transfer Unit
CTAG	Core Test Action Group
DAI	Digital Audio Input
DAO	Digital Audio Output
DMC	Dynamic Memory Controller
DMA	Direct Memory Access
DSP	Digital Signal Processor
EBI	External Bus Interface
EPICS	Economic Parameterised Integrated CoreS
ETU	Epics Transfer Unit
GPIO	General Purpose Input Output
IIC	Inter IC Communication
IIS	Inter IC Sound
INTC	Interrupt Controller
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
MCI	Memory Card Interface
MMC	Multi Media Card
MMU	Memory Management Unit
MPMC	Multi Purpose Memory Controller
PLL	Phase Locked Loop
PMU	Power Management Unit
RISC	Reduced Instruction Set Computer
RTC	Real Time Clock
SDAC	Switched Digital Analog Converter
SDRAM	Synchronous Dynamic RAM
SMC	Static Memory Controller
SPDIF	Sony Philips Digital Input Format
SSA	Solid State Audio
TIC	Test Interface Controller
TCB	Test Control Block

ABBREVIATION	EXPLANATION
UART	Universal Asynchronous Receiver Transmitter
VPB	Versatile Peripheral Bus
Software related	
AAC	Advanced Audio Compression
MP3	MPEG 1 Audio Layer 3
MPEG	Moving Pictures Expert Group
WMA	Windows Media Audio

30 DEFINITIONS

Short-form specification - The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant datasheet or data handbook.

Limiting values definition - Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect the device reliability.

Application information - Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

31 DISCLAIMERS

Life support applications - These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonable be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes - Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software described or contained herein in order to improve design and./or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

32 PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a licences under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

National Semiconductor

April 2003

LM2703
Micropower Step-up DC/DC Converter with 350mA Peak Current Limit

General Description

The LM2703 is a micropower step-up DC/DC in a small 5-lead SOT-23 package. A current limited, fixed off-time control scheme conserves operating current resulting in high efficiency over a wide range of load conditions. The 21V switch allows for output voltages as high as 20V. The low 400ns off-time permits the use of tiny, low profile inductors and capacitors to minimize footprint and cost in space-conscious portable applications. The LM2703 is ideal for LCD panels requiring low current and high efficiency as well as white LED applications for cellular phone back-lighting. The LM2703 can drive up to 4 white LEDs from a single Li-Ion battery.

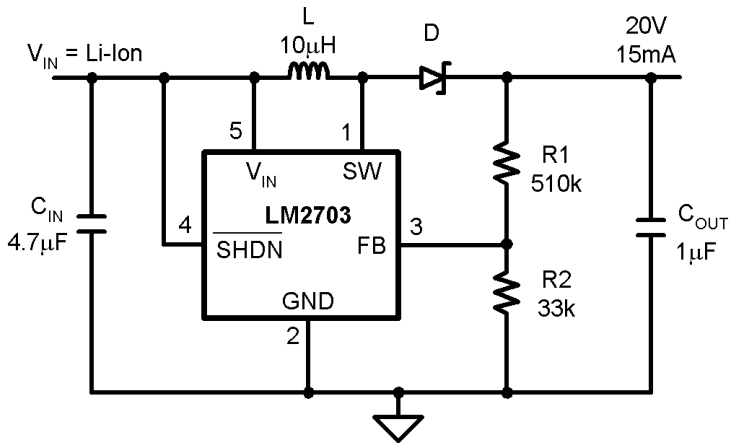
Features

- 350mA, 0.7Ω, internal switch
- Uses small surface mount components
- Adjustable output voltage up to 20V
- 2.2V to 7V input range
- Input undervoltage lockout
- 0.01µA shutdown current
- Small 5-Lead SOT-23 package

Applications

- LCD Bias Supplies
- White LED Back-Lighting
- Handheld Devices
- Digital Cameras
- Portable Applications

Typical Application Circuit



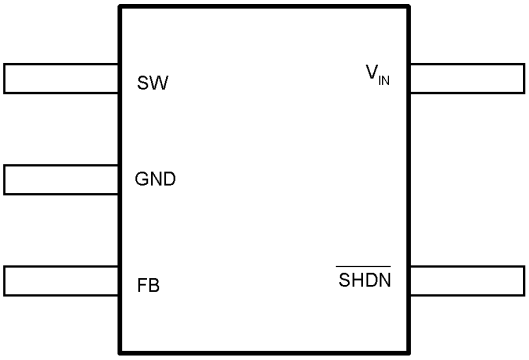
C_{IN}: Taiyo Yuden Ceramic
C_{OUT}: Taiyo Yuden Ceramic
L: Coilcraft DT1608C-103
D: Motorola MBRM130LT3

20030601

FIGURE 1. Typical 20V Application

Connection Diagram

Top View



SOT23-5

T_{Jmax} = 125˚C, θ_{JA} = 220˚C/W (Note 2)

Ordering Information

Order Number	Package Type	NSC Package Drawing	Top Mark	Supplied As
LM2703MF-ADJ	SOT23-5	MA05B	S48B	1000 Units, Tape and Reel
LM2703MFX-ADJ	SOT23-5	MA05B	S48B	3000 Units, Tape and Reel

Pin Description/Functions

Pin	Name	Function
1	SW	Power Switch input.
2	GND	Ground.
3	FB	Output voltage feedback input.
4	$\overline{SHDN}$	Shutdown control input, active low.
5	V_{IN}	Analog and Power input.

SW(Pin 1): Switch Pin. This is the drain of the internal NMOS power switch. Minimize the metal trace area connected to this pin to minimize EMI.

GND(Pin 2): Ground Pin. Tie directly to ground plane.

FB(Pin 3): Feedback Pin. Set the output voltage by selecting values for R1 and R2 using:

$$R1 = R2\left(\frac{V_{OUT}}{1.237V} - 1\right)$$

Connect the ground of the feedback network to an AGND plane which should be tied directly to the GND pin.

$\overline{SHDN}$(Pin 4): Shutdown Pin. The shutdown pin is an active low control. Tie this pin above 1.1V to enable the device. Tie this pin below 0.3V to turn off the device.

V_{IN}(Pin 5): Input Supply Pin. Bypass this pin with a capacitor as close to the device as possible.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{IN}	7.5V
SW Voltage	21V
FB Voltage	2V
$\overline{SHDN}$ Voltage	7.5V
Maximum Junction Temp. T_J (Note 2)	150˚C
Lead Temperature (Soldering 10 sec.)	300˚C
Vapor Phase (60 sec.)	215˚C
Infrared (15 sec.)	220˚C
ESD Ratings (Note 3)	
Human Body Model	2kV
Machine Model (Note 4)	200V

Operating Conditions

Junction Temperature (Note 5)	−40˚C to +125˚C
Supply Voltage	2.2V to 7V
SW Voltage Max.	20.5V

Electrical Characteristics

Specifications in standard type face are for T_J = 25˚C and those in **boldface type** apply over the full **Operating Temperature Range** (T_J = −40˚C to +125˚C). Unless otherwise specified. V_{IN} =2.2V.

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 6)	Max (Note 5)	Units
I_Q	Device Disabled	FB = 1.3V		40	**70**	µA
	Device Enabled	FB = 1.2V		235	**300**	
	Shutdown	$\overline{SHDN}$ = 0V		0.01	2.5	
V_{FB}	FeedbackTrip Point		**1.189**	1.237	**1.269**	V
I_{CL}	Switch Current Limit		275 **260**	350	400 **400**	mA
I_B	FB Pin Bias Current	FB = 1.23V (Note 7)		30	**120**	nA
V_{IN}	Input Voltage Range		**2.2**		**7.0**	V
R_{DSON}	Switch R_{DSON}			0.7	**1.6**	Ω
T_{OFF}	Switch Off Time			400		ns
I_{SD}	$\overline{SHDN}$ Pin Current	$\overline{SHDN}$ = V_{IN}, T_J = 25˚C		0	80	nA
		$\overline{SHDN}$ = V_{IN}, T_J = 125˚C		15		
		$\overline{SHDN}$ = GND		0		
I_L	Switch Leakage Current	V_{SW} = 20V		0.05	5	µA
UVP	Input Undervoltage Lockout	ON/OFF Threshold		1.8		V
V_{FB} Hysteresis	Feedback Hysteresis			8		mV
$\overline{SHDN}$ Threshold	$\overline{SHDN}$ low			0.7	**0.3**	V
	$\overline{SHDN}$ High		**1.1**	0.7		
θ_{JA}	Thermal Resistance			220		˚C/W

Note 1: Absolute maximum ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is intended to be functional, but device parameter specifications may not be guaranteed. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: The maximum allowable power dissipation is a function of the maximum junction temperature, T_J(MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. See the Electrical Characteristics table for the thermal resistance. The maximum allowable power dissipation at any ambient temperature is calculated using: P_D (MAX) = ($T_{J(MAX)}$ − T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature.

Note 3: The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.

Note 4: ESD susceptibility using the machine model is 150V for SW pin.

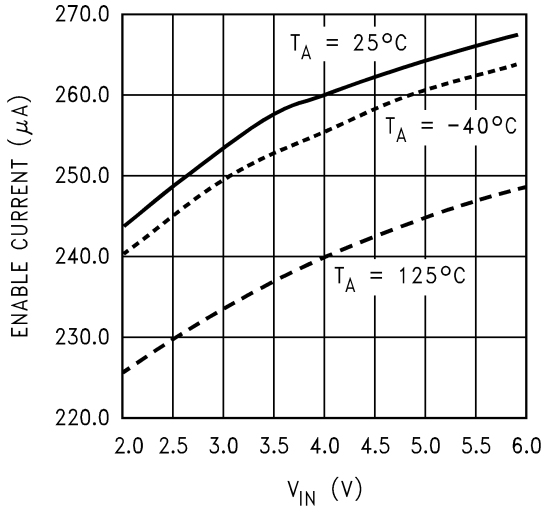
Note 5: All limits guaranteed at room temperature (standard typeface) and at temperature extremes (bold typeface). All room temperature limits are 100% production tested or guaranteed through statistical analysis. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Note 6: Typical numbers are at 25˚C and represent the most likely norm.

Note 7: Feedback current flows into the pin.

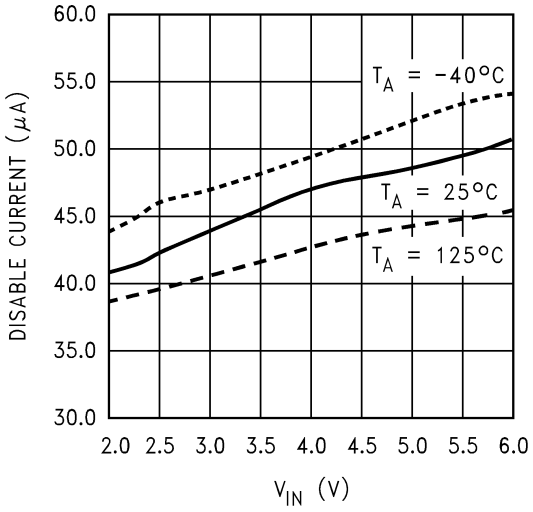
Typical Performance Characteristics

Enable Current vs V_{IN} (Part Switching)



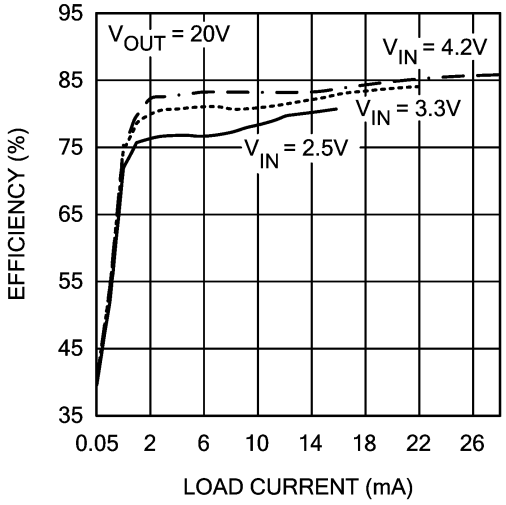
20030605

Disable Current vs V_{IN} (Part Not Switching)



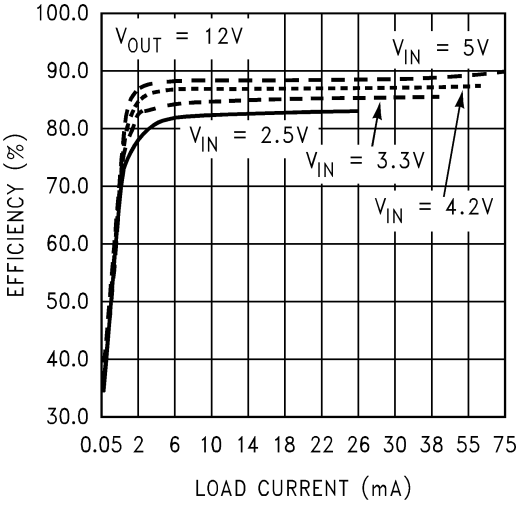
20030606

Efficiency vs Load Current



20030610

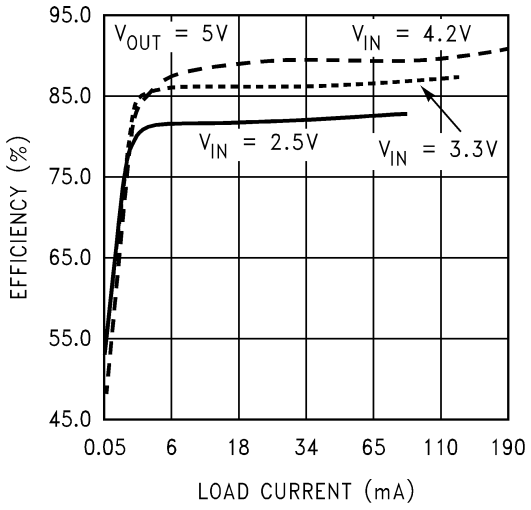
Efficiency vs Load Current



20030611

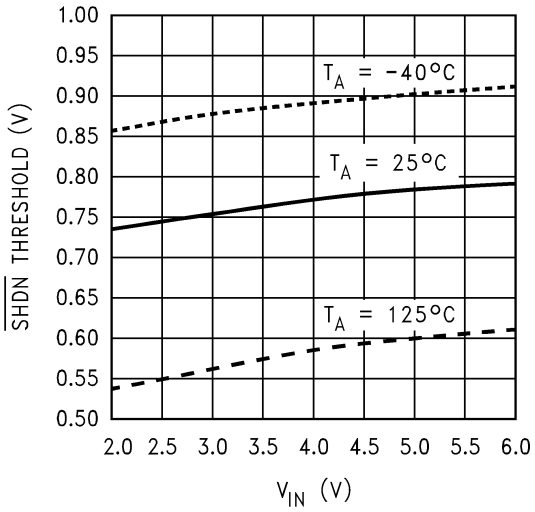
Typical Performance Characteristics (Continued)

Efficiency vs Load Current



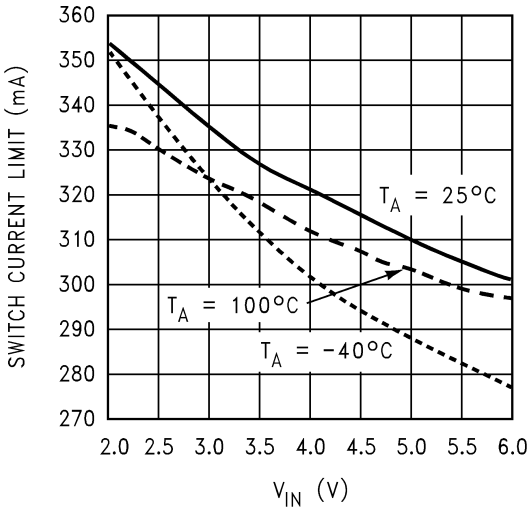
20030612

$\overline{SHDN}$ Threshold vs V_{IN}



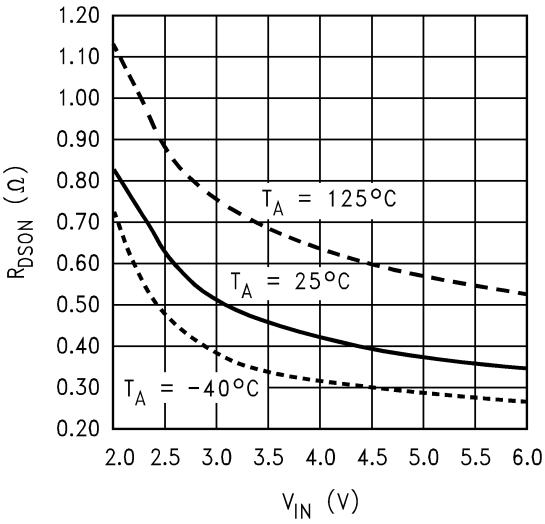
20030613

Switch Current Limit vs V_{IN}



20030614

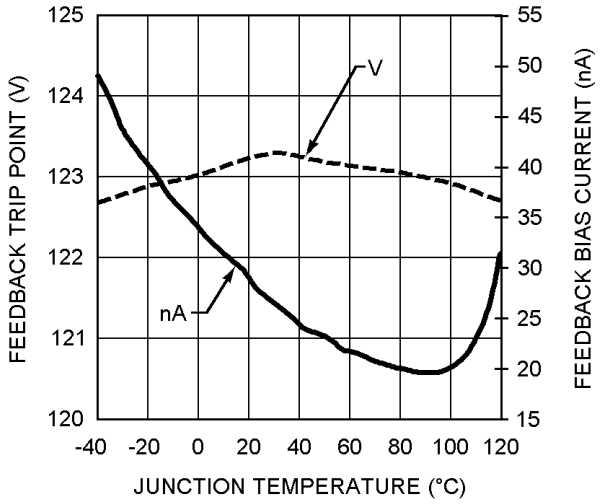
Switch R_{DSON} vs V_{IN}



20030615

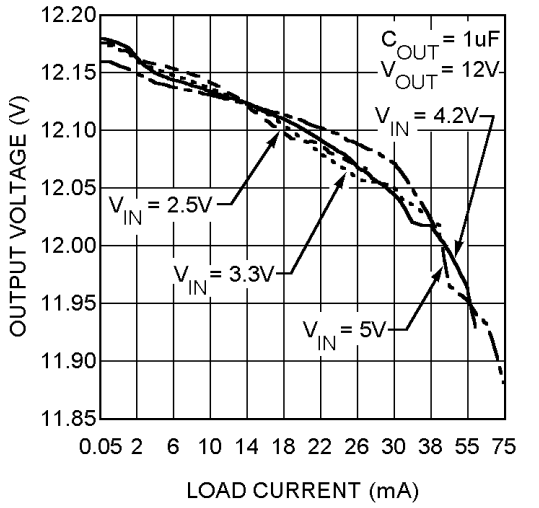
Typical Performance Characteristics (Continued)

FB Trip Point and FB Pin Current vs Temperature



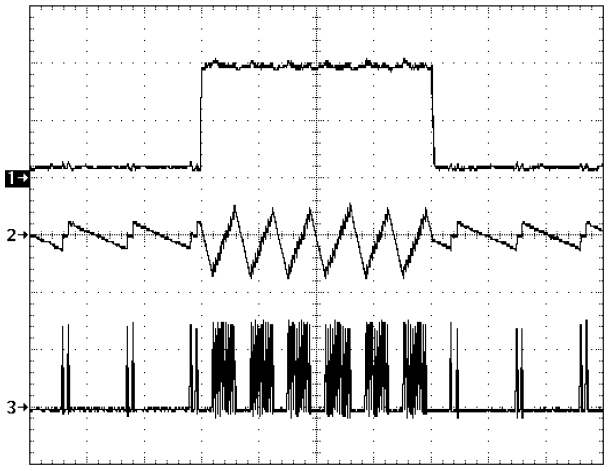
20030623

Output Voltage vs Load Current



20030622

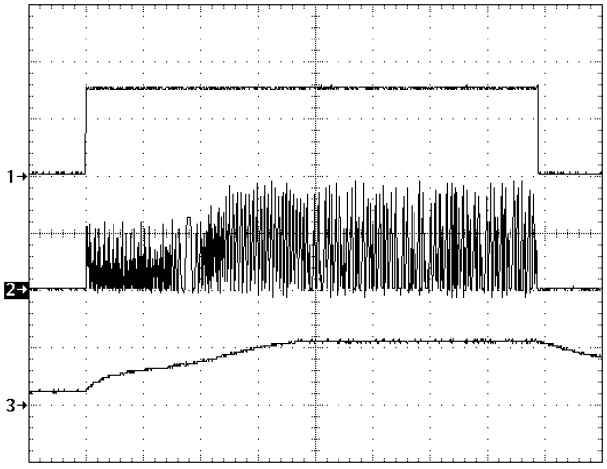
Step Response



20030616

V_{OUT} = 20V, V_{IN} = 2.5V
1) Load, 1mA to 10mA to 1mA, DC
2) V_{OUT}, 200mV/div, AC
3) I_L, 200mA/div, DC
T = 50µs/div

Start-Up/Shutdown



20030617

V_{OUT} = 20V, V_{IN} = 2.5V
1) $\overline{SHDN}$, 1V/div, DC
2) I_L, 200mA/div, DC
3) V_{OUT}, 20V/div, DC
T = 400µs/div
R_L = 1.8kΩ

Operation

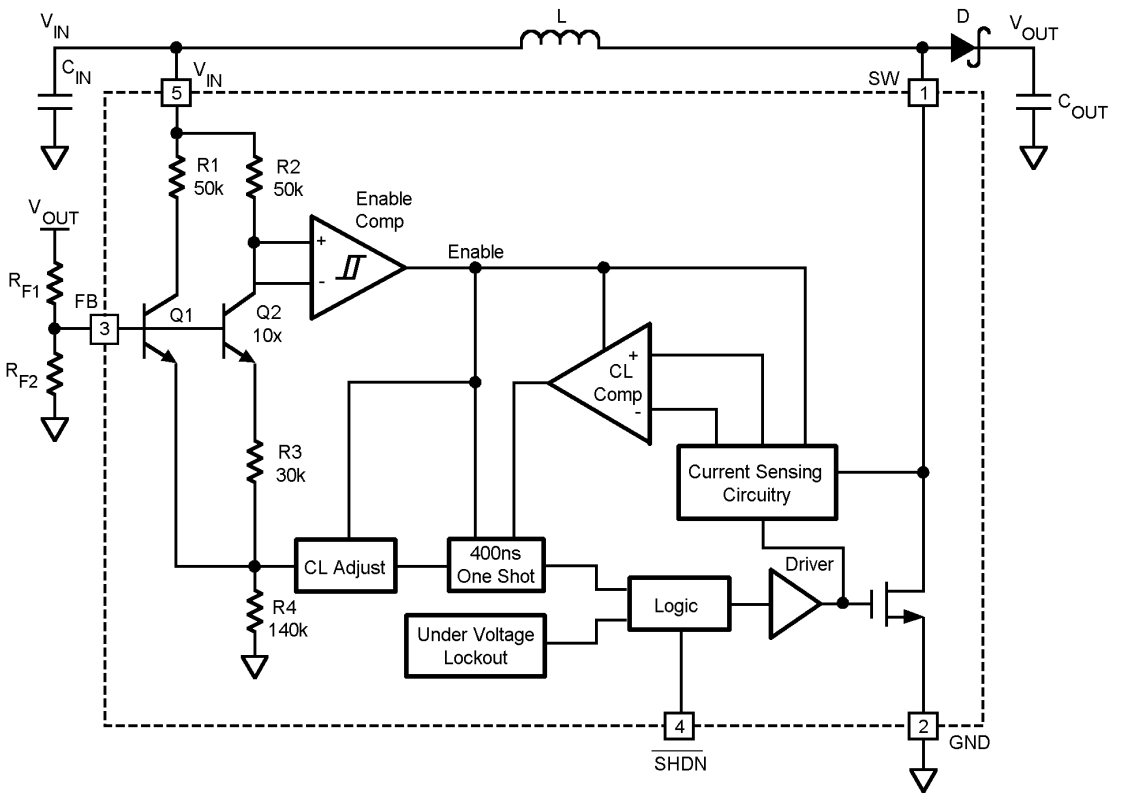
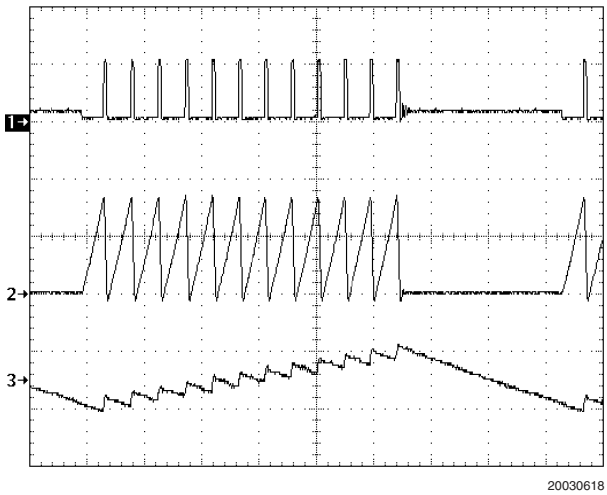


FIGURE 2. LM2703 Block Diagram



V_{OUT} = 20V, V_{IN} = 2.5V
1) V_{SW}, 20V/div, DC
2) Inductor Current, 200mA/div, DC
3) V_{OUT}, 200mV/div, AC
T = 4µs/div

FIGURE 3. Typical Switching Waveform

Operation (Continued)

The LM2703 features a constant off-time control scheme. Operation can be best understood by referring to *Figure 2* and *Figure 3*. Transistors Q1 and Q2 and resistors R3 and R4 of *Figure 2* form a bandgap reference used to control the output voltage. When the voltage at the FB pin is less than 1.237V, the Enable Comp in *Figure 2* enables the device and the NMOS switch is turned on pulling the SW pin to ground. When the NMOS switch is on, current begins to flow through inductor L while the load current is supplied by the output capacitor C_{OUT}. Once the current in the inductor reaches the current limit, the CL Comp trips and the 400ns One Shot turns off the NMOS switch.The SW voltage will then rise to the output voltage plus a diode drop and the inductor current will begin to decrease as shown in *Figure 3*. During this time the energy stored in the inductor is transferred to C_{OUT} and the load. After the 400ns off-time the NMOS switch is turned on and energy is stored in the inductor again. This energy transfer from the inductor to the output causes a stepping effect in the output ripple as shown in *Figure 3*.

This cycle is continued until the voltage at FB reaches 1.237V. When FB reaches this voltage, the enable comparator then disables the device turning off the NMOS switch and reducing the Iq of the device to 40uA. The load current is then supplied solely by C_{OUT} indicated by the gradually decreasing slope at the output as shown in *Figure 3*. When the FB pin drops slightly below 1.237V, the enable comparator enables the device and begins the cycle described previously. The $\overline{SHDN}$ pin can be used to turn off the LM2703 and reduce the I_q to 0.01µA. In shutdown mode the output voltage will be a diode drop lower than the input voltage.

Application Information

INDUCTOR SELECTION

The appropriate inductor for a given application is calculated using the following equation:

$$L = \left(\frac{V_{OUT} - V_{IN(min)} + V_D}{I_{CL}} \right) T_{OFF}$$

where V_D is the schottky diode voltage, I_{CL} is the switch current limit found in the *Typical Performance Characteristics* section, and T_{OFF} is the switch off time. When using this equation be sure to use the minimum input voltage for the application, such as for battery powered applications. For the LM2703 constant-off time control scheme, the NMOS power switch is turned off when the current limit is reached. There is approximately a 200ns delay from the time the current limit is reached in the NMOS power switch and when the internal logic actually turns off the switch. During this 200ns delay, the peak inductor current will increase. This increase in inductor current demands a larger saturation current rating for the inductor. This saturation current can be approximated by the following equation:

$$I_{PK} = I_{CL} + \left(\frac{V_{IN(max)}}{L} \right) 200ns$$

Choosing inductors with low ESR decrease power losses and increase efficiency.

Care should be taken when choosing an inductor. For applications that require an input voltage that approaches the output voltage, such as when converting a Li-Ion battery voltage to 5V, the 400ns off time may not be enough time to discharge the energy in the inductor and transfer the energy to the output capacitor and load. This can cause a ramping effect in the inductor current waveform and an increased ripple on the output voltage. Using a smaller inductor will cause the I_{PK} to increase and will increase the output voltage ripple further. This can be solved by adding a 4.7pF capacitor across the R_{F1} feedback resistor (*Figure 2*) and slightly increasing the output capacitor. A smaller inductor can then be used to ensure proper discharge in the 400ns off time.

DIODE SELECTION

To maintain high efficiency, the average current rating of the schottky diode should be larger than the peak inductor current, I_{PK}. Schottky diodes with a low forward drop and fast switching speeds are ideal for increasing efficiency in portable applications. Choose a reverse breakdown of the schottky diode larger than the output voltage.

CAPACITOR SELECTION

Choose low ESR capacitors for the output to minimize output voltage ripple. Multilayer ceramic capacitors are the best choice. For most applications, a 1µF ceramic capacitor is sufficient. For some applications a reduction in output voltage ripple can be achieved by increasing the output capacitor.

Local bypassing for the input is needed on the LM2703. Multilayer ceramic capacitors are a good choice for this as well. A 4.7µF capacitor is sufficient for most applications. For additional bypassing, a 100nF ceramic capacitor can be used to shunt high frequency ripple on the input.

LAYOUT CONSIDERATIONS

The input bypass capacitor C_{IN}, as shown in *Figure 1*, must be placed close to the IC. This will reduce copper trace resistance which effects input voltage ripple of the IC. For additional input voltage filtering, a 100nF bypass capacitor can be placed in parallel with C_{IN} to shunt any high frequency noise to ground. The output capacitor, C_{OUT}, should also be placed close to the IC. Any copper trace connections for the Cout capacitor can increase the series resistance, which directly effects output voltage ripple. The feedback network, resistors R1 and R2, should be kept close to the FB pin to minimize copper trace connections that can inject noise into the system. The ground connection for the feedback resistor network should connect directly to an analog ground plane. The analog ground plane should tie directly to the GND pin. If no analog ground plane is available, the ground connection for the feedback network should tie directly to the GND pin. Trace connections made to the inductor and schottky diode should be minimized to reduce power dissipation and increase overall efficiency.

Application Information (Continued)

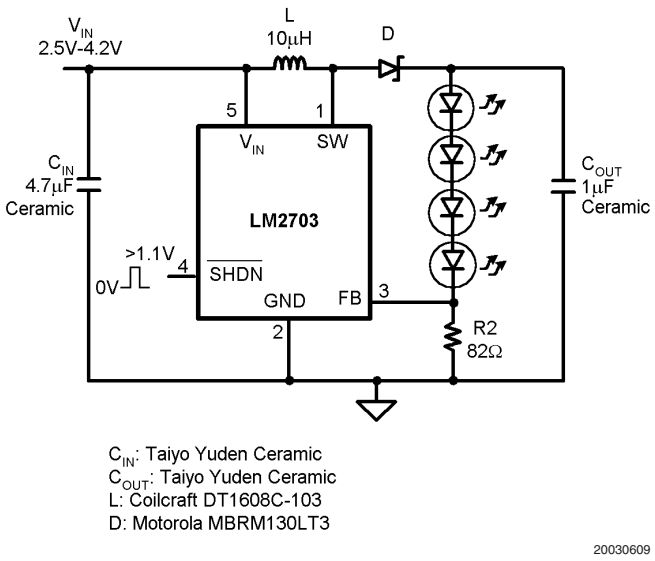


FIGURE 4. White LED Application

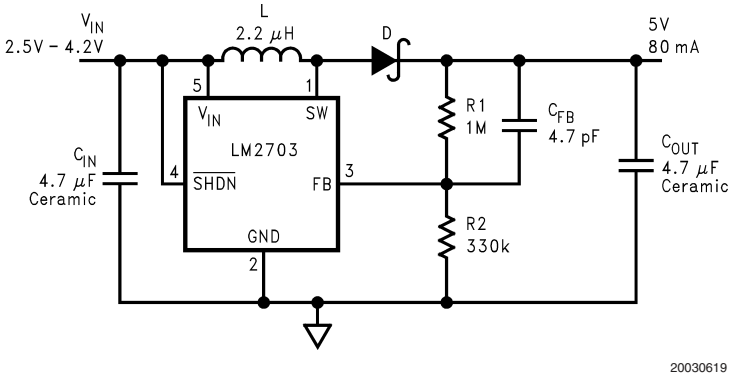


FIGURE 5. Li-Ion 5V Application

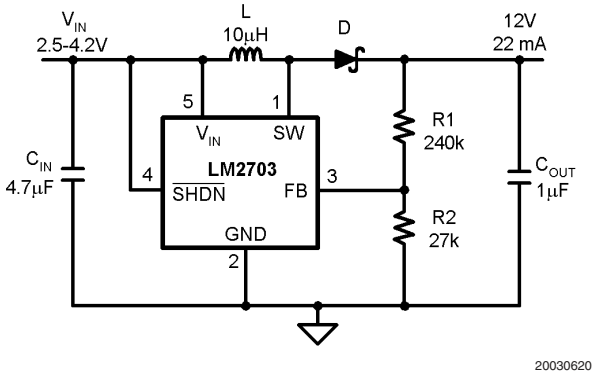


FIGURE 6. Li-Ion 12V Application

Application Information (Continued)

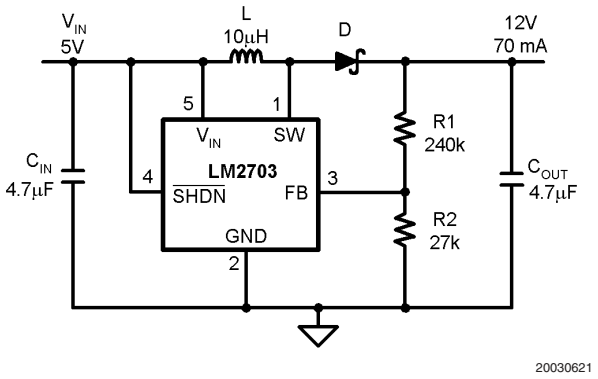
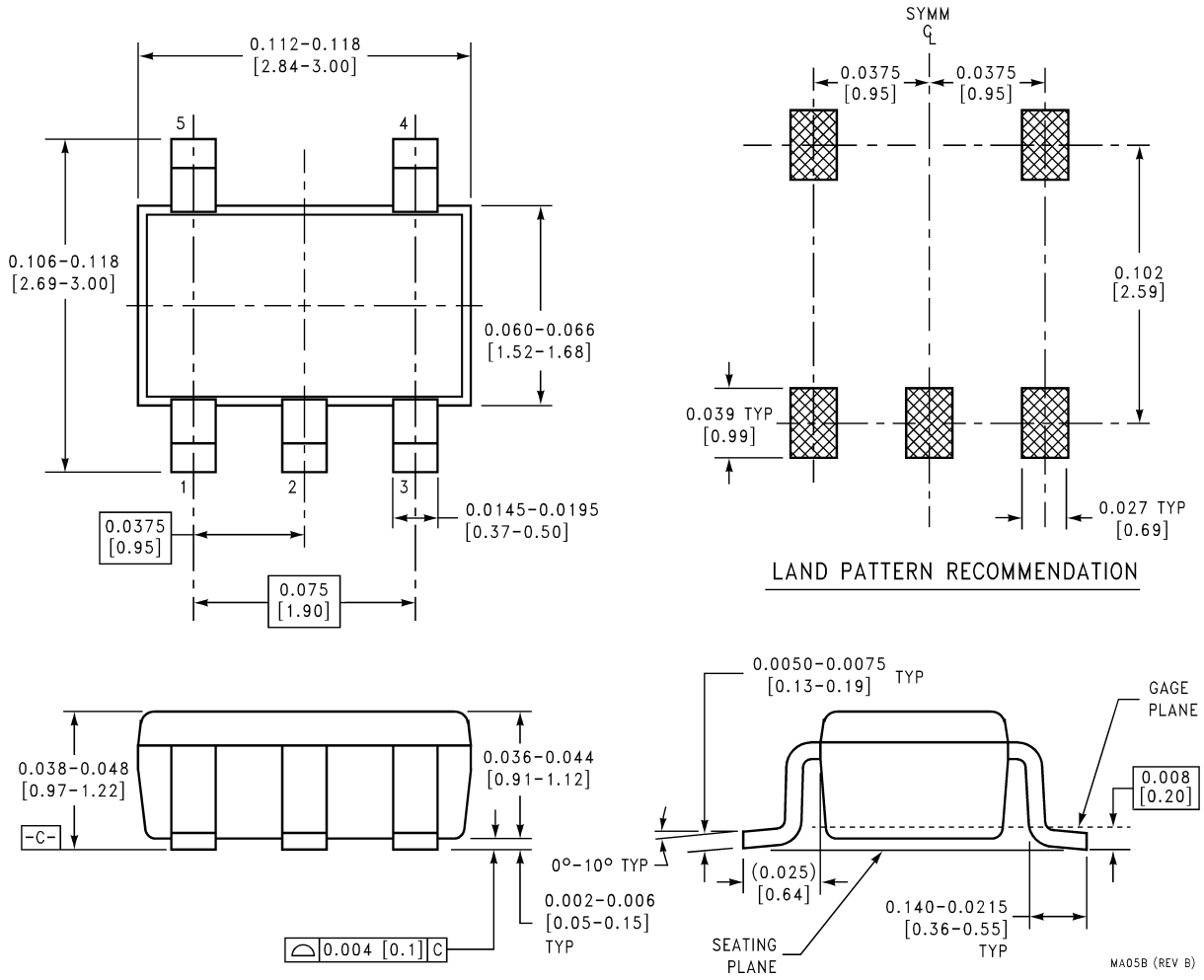


FIGURE 7. 5V to 12V Application

Physical Dimensions inches (millimeters) unless otherwise noted



5-Lead Small Outline Package (M5)
For Ordering, Refer to Ordering Information Table
NS Package Number MA05B

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor
Americas Customer
Support Center
Email: new.feedback@nsc.com
Tel: 1-800-272-9959

www.national.com

National Semiconductor
Europe Customer Support Center
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor
Asia Pacific Customer
Support Center
Fax: +65-6250 4466
Email: ap.support@nsc.com
Tel: +65-6254 4466

National Semiconductor
Japan Customer Support Center
Fax: 81-3-5639-7507
Email: jpn.feedback@nsc.com
Tel: 81-3-5639-7560

Document Title

512M x 8 Bit / 1G x 8 Bit NAND Flash Memory

Revision History

Revision No	History	Draft Date	Remark
0.0	1. Initial issue	Feb. 19. 2003	Advance
0.1	1. Add two-K9K4GXXU0M-YCB0/YIB0 Stacked Package	Mar. 31. 2003	Preliminary
0.2	1. The 3rd Byte ID after 90h ID read command is don't cared. The 5th Byte ID after 90h ID read command is deleted.	Apr. 9. 2003	Preliminary
0.3	1. The K9W8G16U1M-YCB0,YIB0,PCB0,PIB0 is deleted in line up. 2. Note is added. (VIL can undershoot to -0.4V and VIH can overshoot to VCC +0.4V for durations of 20 ns or less.) 3. Pb-free Package is added. K9K4G08Q0M-PCB0,PIB0 K9K4G08U0M-PCB0,PIB0 K9K4G16U0M-PCB0,PIB0 K9K4G16Q0M-PCB0,PIB0 K9W8G08U1M-PCB0,PIB0	Apr. 30. 2003	Preliminary
0.4	1. Added Addressing method for program operation.	Jan. 27. 2004	Preliminary
0.5	1. The tADL(Address to Data Loading Time) is added. - tADL Minimum 100ns - tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle at program operation. 2. Added addressing method for program operation 3. PKG(TSOP1) Dimension Change	May.31. 2004	Preliminary
0.6	1. Technical note is changed 2. Notes of AC timing characteristics are added 3. The description of Copy-back program is changed 4. 1.8V part is deleted	Feb. 01. 2005	Preliminary
0.7	1. $\overline{CE}$ access time : 23ns->35ns (p.11)	Feb. 14. 2005	Preliminary
0.8	1. The value of tREA is changed.(18ns->20ns) 2. The value of output load capacitance is changed. 3. EDO mode is added.	May 4. 2005	
0.9	1. The flow chart to creat the initial invalid block table is changed.	May 6. 2005	

512M x 8 Bit / 1G x 8 Bit NAND Flash Memory

PRODUCT LIST

Part Number	Vcc Range	Organization	PKG Type
K9K4G08U0M-Y,P	2.7 ~ 3.6V	X8	TSOP1
K9W8G08U1M-Y,P			

FEATURES

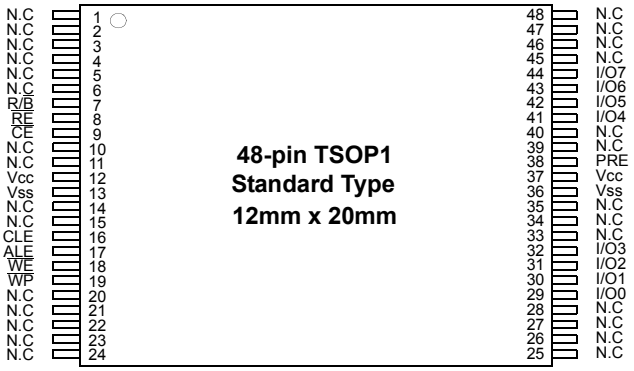
- Voltage Supply
  - 2.7 V ~3.6 V
- Organization
  - Memory Cell Array
    - (512M + 16,384K)bit x 8bit
  - Data Register
    - (2K + 64)bit x8bit
  - Cache Register
    - (2K + 64)bit x8bit
- Automatic Program and Erase
  - Page Program
    - (2K + 64)Byte
  - Block Erase
    - (128K + 4K)Byte
- Page Read Operation
  - Page Size
    - 2K-Byte
  - Random Read : 25μs(Max.)
  - Serial Access : 30ns(Min.)
- Fast Write Cycle Time
  - Program time : 200μs(Typ.)
  - Block Erase Time : 2ms(Typ.)
- Command/Address/Data Multiplexed I/O Port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
  - Endurance : 100K Program/Erase Cycles
  - Data Retention : 10 Years
- Command Register Operation
- Cache Program Operation for High Performance Program
- Power-On Auto-Read Operation
- Intelligent Copy-Back Operation
- Unique ID for Copyright Protection
- Package :
  - K9K4G08U0M-YCB0/YIB0
    48 - Pin TSOP I (12 x 20 / 0.5 mm pitch)
  - K9W8G08U1M-YCB0/YIB0 : Two K9K4G08U0M stacked.
    48 - Pin TSOP I (12 x 20 / 0.5 mm pitch)
  - K9K4G08U0M-PCB0/PIB0 : Pb-FREE PACKAGE
    48 - Pin TSOP I (12 x 20 / 0.5 mm pitch)
  - K9W8G08U1M-PCB0/PIB0 : Two K9K4G08U0M stacked.
    48 - Pin TSOP I (12 x 20 / 0.5 mm pitch)

GENERAL DESCRIPTION

Offered in 512Mx8bit, the K9K4G08U0M is 4G bit with spare 128M bit capacity. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. A program operation can be performed in typical 200μs on the 2112-byte page and an erase operation can be performed in typical 2ms on a 128K-byte block. Data in the data page can be read out at 30ns cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command input. The on-chip write controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. Even the write-intensive systems can take advantage of the K9K4G08U0M′s extended reliability of 100K program/erase cycles by providing ECC(Error Correcting Code) with real time mapping-out algorithm. The K9K4G08U0M is an optimum solution for large non-volatile storage applications such as solid state file storage and other portable applications requiring non-volatility. An ultra high density solution having two 4Gb stacked with two chip selects is also available in standard TSOPI package.

PIN CONFIGURATION (TSOP1)

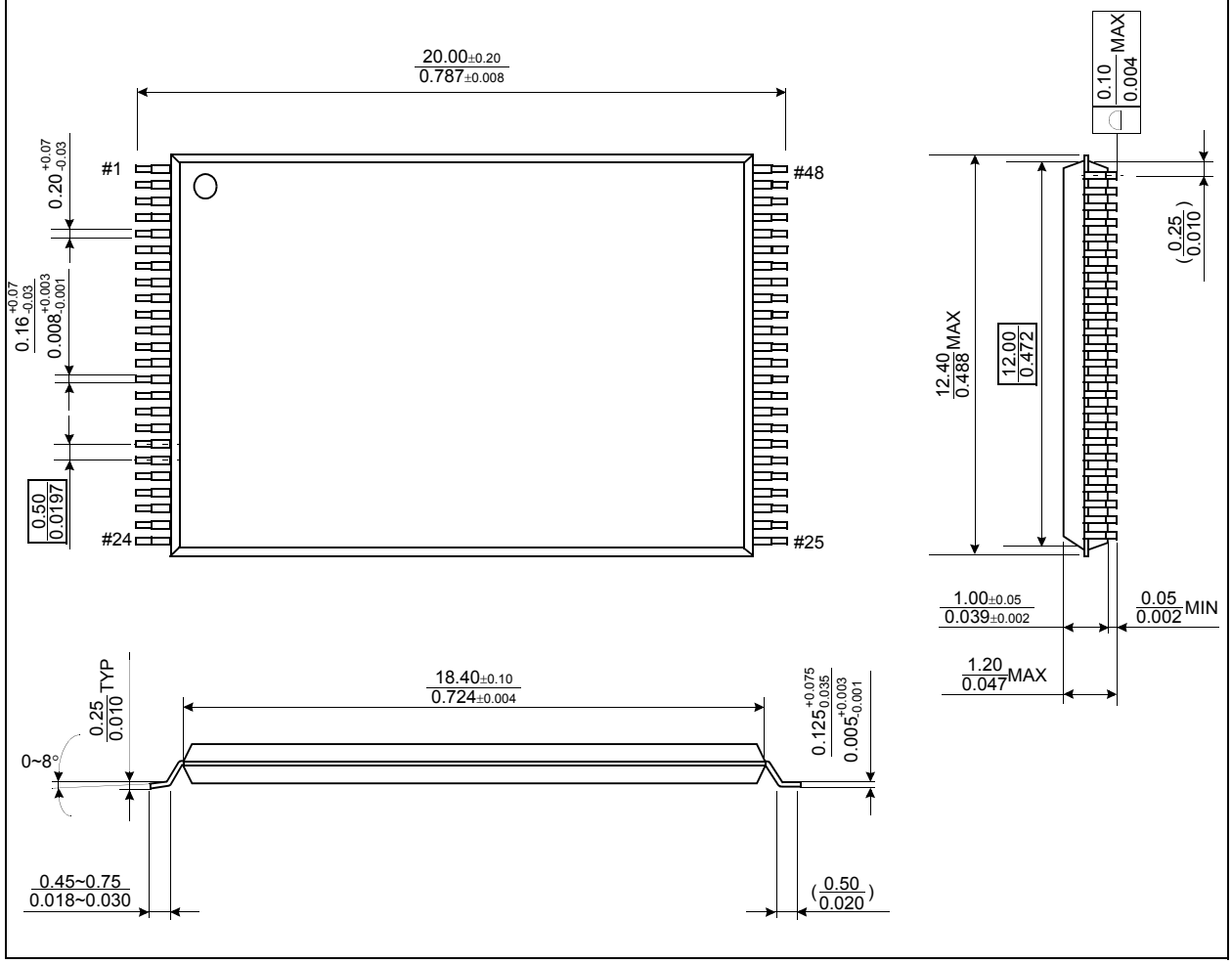
K9K4G08U0M-YCB0,PCB0/YIB0,PIB0



PACKAGE DIMENSIONS

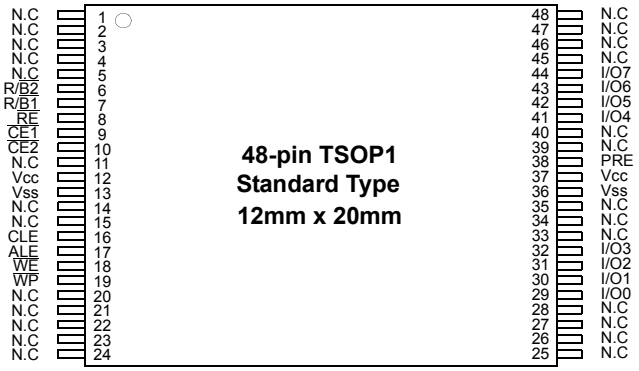
48-PIN LEAD/LEAD FREE PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(I)

48 - TSOP1 - 1220AF Unit :mm/Inch



PIN CONFIGURATION (TSOP1)

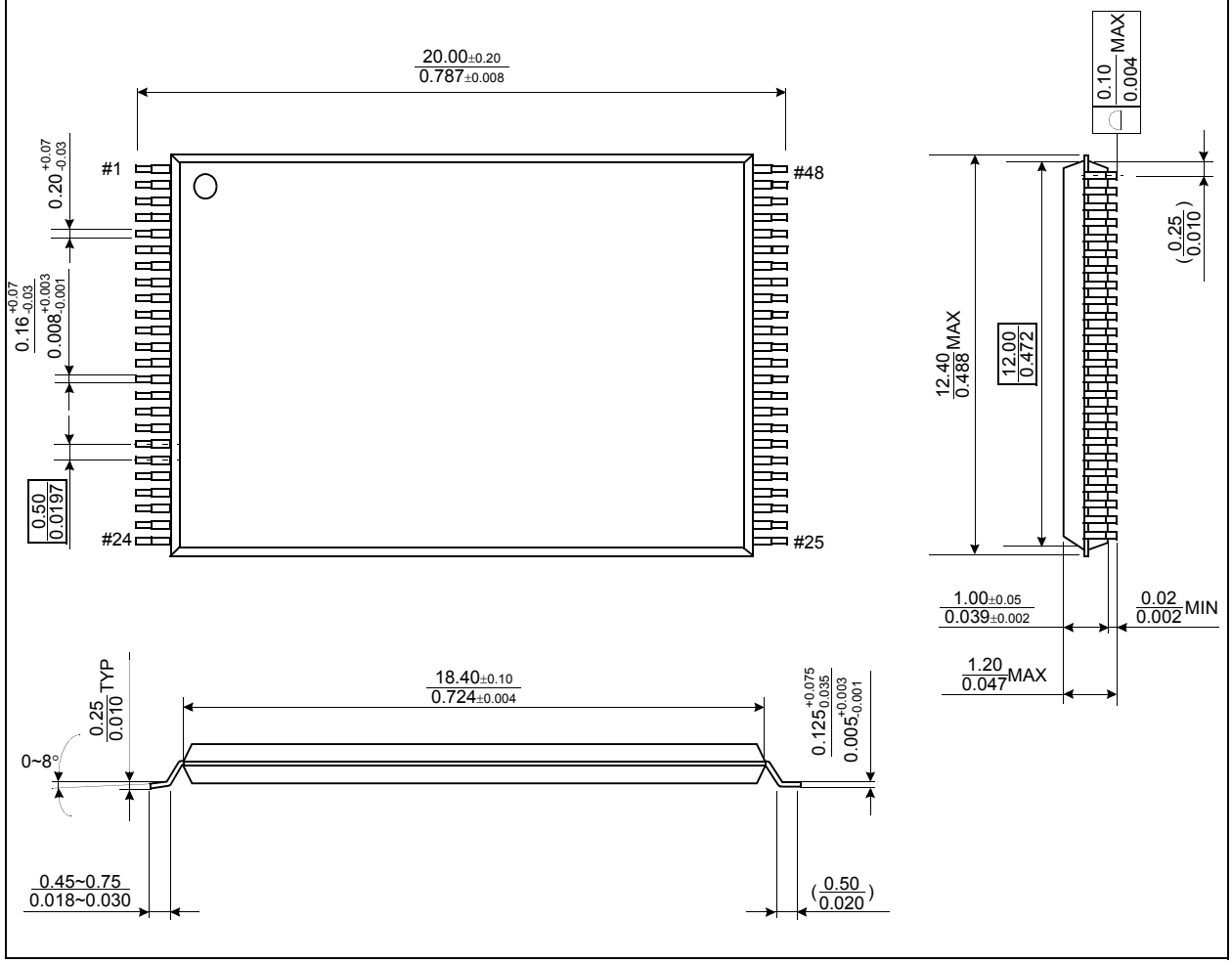
K9W8G08U1M-YCB0,PCB0/YIB0,PIB0



PACKAGE DIMENSIONS

48-PIN LEAD/LEAD FREE PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(I)

48 - TSOP1 - 1220AF Unit :mm/Inch



PIN DESCRIPTION

Pin Name	Pin Function
$I/O_0 \sim I/O_7$	**DATA INPUTS/OUTPUTS** The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the $\overline{WE}$ signal.
ALE	**ADDRESS LATCH ENABLE** The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of $\overline{WE}$ with ALE high.
$\overline{CE}$ / $\overline{CE}$1	**CHIP ENABLE** The $\overline{CE}$ / $\overline{CE}$1 input is the device selection control. When the device is in the Busy state, $\overline{CE}$ / $\overline{CE}$1 high is ignored, and the device does not return to standby mode in program or erase operation. Regarding $\overline{CE}$ / $\overline{CE}$1 control during read operation, refer to 'Page read' section of Device operation .
$\overline{CE}$2	**CHIP ENABLE** The $\overline{CE}$2 input enables the second K9K4G08U0M
$\overline{RE}$	**READ ENABLE** The $\overline{RE}$ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of $\overline{RE}$ which also increments the internal column address counter by one.
$\overline{WE}$	**WRITE ENABLE** The $\overline{WE}$ input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the $\overline{WE}$ pulse.
$\overline{WP}$	**WRITE PROTECT** The $\overline{WP}$ pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the $\overline{WP}$ pin is active low.
R/$\overline{B}$1/ R/$\overline{B}$2	**READY/BUSY OUTPUT** The R/$\overline{B}$ / R/$\overline{B}$1 output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
PRE	**POWER-ON READ ENABLE** The PRE controls auto read operation executed during power-on. The power-on auto-read is enabled when PRE pin is tied to Vcc.
Vcc	**POWER** Vcc is the power supply for device.
Vss	**GROUND**
N.C	**NO CONNECTION** Lead is not internally connected.

NOTE: Connect all Vcc and Vss pins of each device to common power supply outputs.

Do not leave Vcc or Vss disconnected.

Figure 1-1. K9K4G08U0M Functional Block Diagram

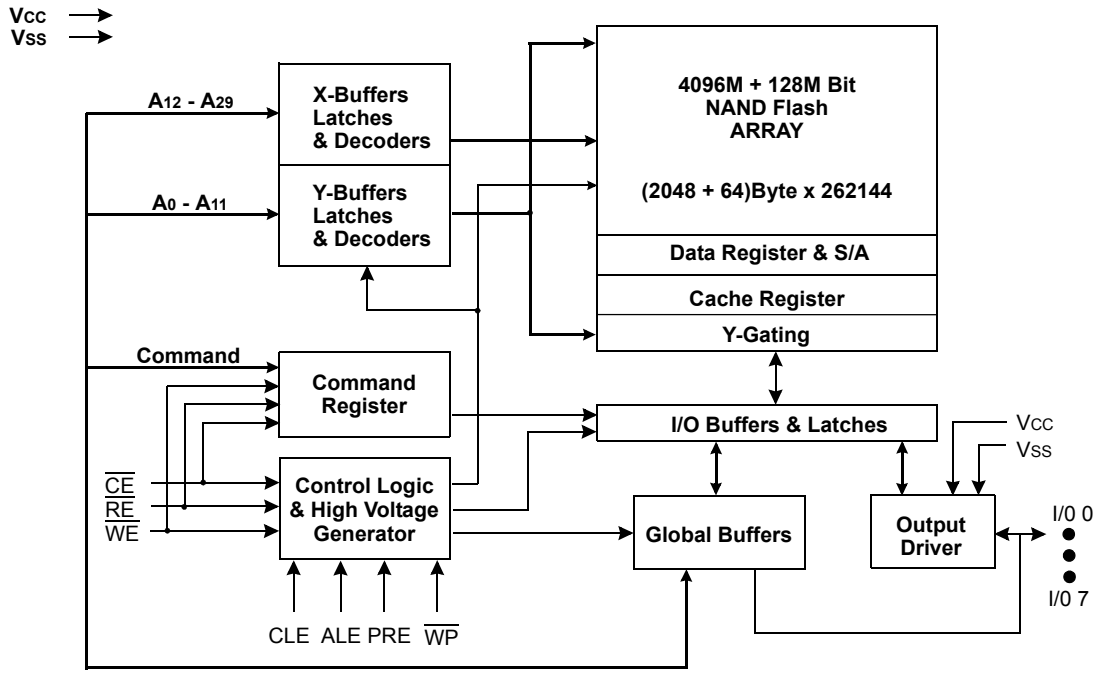
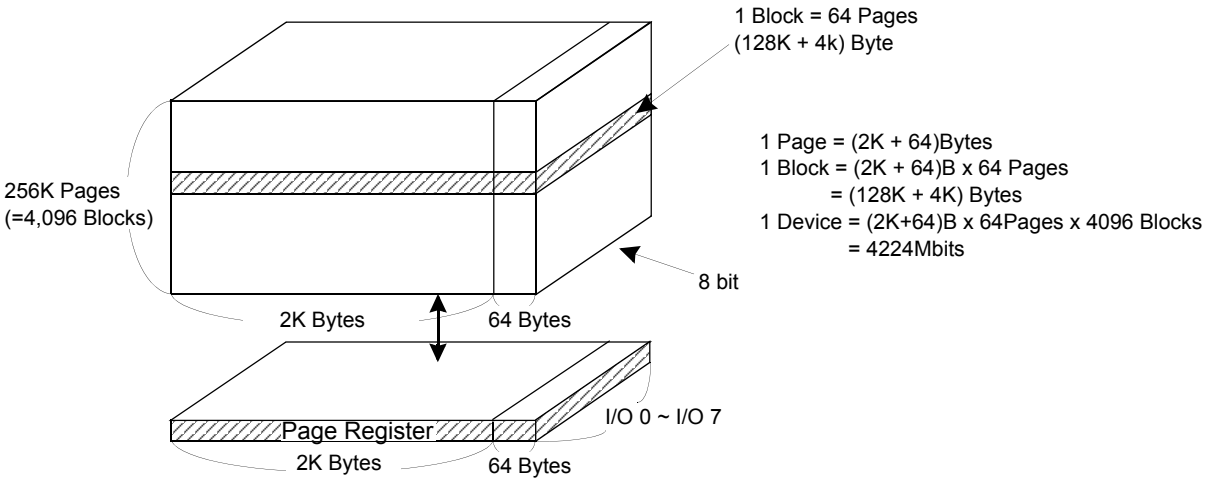


Figure 2-1. K9K4G08U0M Array Organization



	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7	**Column Address**
2nd Cycle	A8	A9	A10	A11	*L	*L	*L	*L	**Column Address**
3rd Cycle	A12	A13	A14	A15	A16	A17	A18	A19	**Row Address**
4th Cycle	A20	A21	A22	A23	A24	A25	A26	A27	**Row Address**
5th Cycle	A28	A29	*L	*L	*L	*L	*L	*L	**Row Address**

NOTE : Column Address : Starting Address of the Register.

* L must be set to "Low".

* The device ignores any additional input of address cycles than reguired.

Product Introduction

The K9K4G08U0M is a 4224Mbit (4,429,185,024 bit) memory organized as 262,144 rows(pages) by 2112x8 columns. Spare 64 columns are located from column address of 2048~2111. A 2112-byte data register and a 2112-byte cache register are serially connected to each other. Those serially connected registers are connected to memory cell arrays for accommodating data transfer between the I/O buffers and memory cells during page read and page program operations. The memory array is made up of 32 cells that are serially connected to form a NAND structure. Each of the 32 cells resides in a different page. A block consists of two NAND structured strings. A NAND structure consists of 32 cells. Total 1081344 NAND cells reside in a block. The program and read operations are executed on a page basis, while the erase operation is executed on a block basis. The memory array consists of 4096 separately erasable 128K-byte blocks. It indicates that the bit by bit erase operation is prohibited on the K9K4G08U0M.

The K9K4G08U0M has addresses multiplexed into 8 I/Os. This scheme dramatically reduces pin counts and allows system upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O's by bringing $\overline{WE}$ to low while $\overline{CE}$ is low. Those are latched on the rising edge of $\overline{WE}$. Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the I/O pins. Some commands require one bus cycle. For example, Reset Command, Status Read Command, etc require just one cycle bus. Some other commands, like page read and block erase and page program, require two cycles: one cycle for setup and the other cycle for execution. The 512M byte physical space requires 30 addresses, thereby requiring five cycles for addressing: 2 cycles of column address, 3 cycles of row address, in that order. Page Read and Page Program need the same five address cycles following the required command input. In Block Erase operation, however, only the three row address cycles are used. Device operations are selected by writing specific commands into the command register. Table 1 defines the specific commands of the K9K4G08U0M.

The device provides cache program in a block. It is possible to write data into the cache registers while data stored in data registers are being programmed into memory cells in cache program mode. The program performace may be dramatically improved by cache program when there are lots of pages of data to be programmed.

The device embodies power-on auto-read feature which enables serial access of data of the 1st page without command and address input after power-on.

In addition to the enhanced architecture and interface, the device incorporates copy-back program feature from one page to another page without need for transporting the data to and from the external buffer memory. Since the time-consuming serial access and data-input cycles are removed, system performance for solid-state disk application is significantly increased.

Table 1. Command Sets

Function	1st. Cycle	2nd. Cycle	Acceptable Command during Busy
Read	00h	30h	
Read for Copy Back	00h	35h	
Read ID	90h	-	
Reset	FFh	-	O
Page Program	80h	10h	
Cache Program	80h	15h	
Copy-Back Program	85h	10h	
Block Erase	60h	D0h	
Random Data Input*1	85h	-	
Random Data Output*1	05h	E0h	
Read Status	70h		O

NOTE : 1. Random Data Input/Output can be executed in a page.

Caution : Any undefined command inputs are prohibited except for above command set of Table 1.

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}		$V_{IN/OUT}$	-0.6 to + 4.6	V
		V_{CC}	-0.6 to + 4.6	
Temperature Under Bias	K9K4G08U0M-XCB0	T_{BIAS}	-10 to +125	°C
	K9K4G08U0M-XIB0		-40 to +125	
Storage Temperature	K9K4G08U0M-XCB0	T_{STG}	-65 to +150	°C
	K9K4G08U0M-XIB0			
Short Circuit Current		Ios	5	mA

NOTE :
1. Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns.
   Maximum DC voltage on input/output pins is V_{CC},+0.3V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.
2. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltage reference to GND, K9K4G08U0M-XCB0 :T_A=0 to 70°C, K9K4G08U0M-XIB0:T_A=-40 to 85°C)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{CC}	2.7	3.3	3.6	V
Supply Voltage	V_{SS}	0	0	0	V

DC AND OPERATING CHARACTERISTICS(Recommended operating conditions otherwise noted.)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Current	Page Read with Serial Access	$I_{CC}1$	tRC=30ns, $\overline{CE}$=V_{IL} I_{OUT}=0mA	-	15	30	mA
	Program	$I_{CC}2$	-	-	15	30	
	Erase	$I_{CC}3$	-	-	15	30	
Stand-by Current(TTL)		$I_{SB}1$	$\overline{CE}$=V_{IH}, $\overline{WP}$=$\overline{PRE}$=0V/V_{CC}	-	-	1	
Stand-by Current(CMOS)		$I_{SB}2$	$\overline{CE}$=V_{CC}-0.2, $\overline{WP}$=$\overline{PRE}$=0V/V_{CC}	-	20	100	µA
Input Leakage Current		I_{LI}	V_{IN}=0 to Vcc(max)	-	-	±20	
Output Leakage Current		I_{LO}	V_{OUT}=0 to Vcc(max)	-	-	±20	
Input High Voltage		V_{IH}*	-	0.8xVcc	-	V_{CC}+0.3	V
Input Low Voltage, All inputs		V_{IL}*	-	-0.3	-	0.2xVcc	
Output High Voltage Level		V_{OH}	K9K4G08U0M :I_{OH}=-400µA	2.4	-	-	
Output Low Voltage Level		V_{OL}	K9K4G08U0M :I_{OL}=2.1mA	-	-	0.4	
Output Low Current(R/$\overline{B}$)		I_{OL}(R/$\overline{B}$)	K9K4G08U0M :V_{OL}=0.4V	8	10	-	mA

NOTE :
1. V_{IL} can undershoot to -0.4V and V_{IH} can overshoot to V_{CC} +0.4V for durations of 20 ns or less.
3. The typical value of the K9W8G08U1M's $I_{SB}2$ is 40µA and the maximum value is 200µA.
4. The maximum value of K9W8G08U1M's I_{LI} and I_{LO} is ±40µA.

VALID BLOCK

	Parameter	Symbol	Min	Max	Unit
K9K4G08U0M	Valid Block Number	N_{VB}	4016	4096	Blocks
K9W8G08U1M	Valid Block Number	N_{VB}	8032*	8192*	Blocks

NOTE :
1. The device may include invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for appropriate management of invalid blocks.
2. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block, does not require Error Correction up to 1K program/erase cycles.

* : Each K9K4G08U0M chip in the K9W8G08U1M has Maximum 80 invalid blocks.

AC TEST CONDITION

(K9K4G08U0M-XCB0 :TA=0 to 70°C, K9K4G08U0M-XIB0:TA=-40 to 85°C
K9K4G08U0M : Vcc=2.7V~3.6V unless otherwise noted)

Parameter	K9K4G08U0M
Input Pulse Levels	0V to Vcc
Input Rise and Fall Times	5ns
Input and Output Timing Levels	Vcc/2
Output Load	1 TTL GATE and CL=50pF (K9K4G08U0M-Y,P)
	1 TTL GATE and CL=30pF (K9W8G08U1M-Y,P)

CAPACITANCE(T_A=25°C, V_{CC}=3.3V, f=1.0MHz)

Item	Symbol	Test Condition	Max		Unit
			K9K4G08U0M	K9W8G08U1M	
Input/Output Capacitance	$C_{I/O}$	V_{IL}=0V	20	40	pF
Input Capacitance	C_{IN}	V_{IN}=0V	20	40	pF

NOTE : Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	PRE	Mode	
H	L	L	↑	H	X	X	Read Mode	Command Input
L	H	L	↑	H	X	X		Address Input(5clock)
H	L	L	↑	H	H	X	Write Mode	Command Input
L	H	L	↑	H	H	X		Address Input(5clock)
L	L	L	↑	H	H	X	Data Input	
L	L	L	H	↓	X	X	Data Output	
X	X	X	X	H	X	X	During Read(Busy)	
X	X	X	X	X	H	X	During Program(Busy)	
X	X	X	X	X	H	X	During Erase(Busy)	
X	X(1)	X	X	X	L	X	Write Protect	
X	X	H	X	X	0V/V_{CC}*2	0V/V_{CC}*2	Stand-by	

NOTE : 1. X can be V_{IL} or V_{IH}.
2. $\overline{WP}$ and $\overline{PRE}$ should be biased to CMOS high or CMOS low for standby.

Program / Erase Characteristics

Parameter		Symbol	Min	Typ	Max	Unit
Program Time		t_{PROG}*1	-	200	700	μs
Dummy Busy Time for Cache Program		t_{CBSY}*2		3	700	μs
Number of Partial Program Cycles in the Same Page	Main Array	Nop	-	-	4	cycles
	Spare Array		-	-	4	cycles
Block Erase Time		t_{BERS}	-	2	3	ms

NOTE : 1.Typical program time is defined as the time within which more than 50% of the whole pages are programmed at Vcc of 3.3V and 25'C
2.Max. time of t_{CBSY} depends on timing between internal program completion and data in

AC Timing Characteristics for Command / Address / Data Input

Parameter	Symbol	Min		Max		Unit
		K9K4G08U0M*	K9K4G08U0M	K9K4G08U0M*	K9K4G08U0M	
CLE setup Time	t_{CLS}*1	25	15	-	-	ns
CLE Hold Time	t_{CLH}	10	5	-	-	ns
$\overline{CE}$ setup Time	t_{CS}*1	35	20	-	-	ns
$\overline{CE}$ Hold Time	t_{CH}	10	5	-	-	ns
$\overline{WE}$ Pulse Width	t_{WP}	25	15	-	-	ns
ALE setup Time	t_{ALS}*1	25	15	-	-	ns
ALE Hold Time	t_{ALH}	10	5	-	-	ns
Data setup Time	t_{DS}*1	20	15	-	-	ns
Data Hold Time	t_{DH}	10	5	-	-	ns
Write Cycle Time	t_{WC}	45	30	-	-	ns
$\overline{WE}$ High Hold Time	t_{WH}	15	10	-	-	ns
ALE to Data Loading Time	t_{ADL}*2	100	100	-	-	ns

NOTES : 1. The transition of the corresponding control pins must occur only once while $\overline{WE}$ is held low.
2. tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle.
3. **For cache program operation, the whole AC Charcateristics must be same as that of K9K4G08U0M*.**

AC Characteristics for Operation

Parameter	Symbol	Min		Max		Unit
		K9K4G08U0M*	K9K4G08U0M	K9K4G08U0M*	K9K4G08U0M	
Data Transfer from Cell to Register	t_R	-	-	25	25	μs
ALE to $\overline{RE}$ Delay	t_{AR}	10	10	10	-	ns
CLE to $\overline{RE}$ Delay	t_{CLR}	10	10	-	-	ns
Ready to $\overline{RE}$ Low	t_{RR}	20	20	-	-	ns
$\overline{RE}$ Pulse Width	t_{RP}	25	15	-	-	ns
$\overline{WE}$ High to Busy	t_{WB}	-	-	100	100	ns
Read Cycle Time	t_{RC}	50	30	-	-	ns
$\overline{RE}$ Access Time	t_{REA}	-	-	30	20	ns
$\overline{CE}$ Access Time	t_{CEA}	-	-	45	35	ns
$\overline{RE}$ High to Output Hi-Z	t_{RHZ}	-	-	30	30	ns
$\overline{CE}$ High to Output Hi-Z	t_{CHZ}	-	-	20	20	ns
$\overline{RE}$ or $\overline{CE}$ High to Output hold	t_{OH}	15	15	-	-	ns
$\overline{RE}$ High Hold Time	t_{REH}	15	10	-	-	ns
Output Hi-Z to $\overline{RE}$ Low	t_{IR}	0	0	-	-	ns
$\overline{RE}$ High to $\overline{WE}$ Low	t_{RHW}	100	100	-	-	ns
$\overline{WE}$ High to $\overline{RE}$ Low	t_{WHR}	60	60	-	-	ns
Device Resetting Time (Read/Program/Erase)	t_{RST}	-	-	5/10/500*1	5/10/500*1	μs

NOTE: 1. If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 5us.
2. **For cache program operation, the whole AC Charcateristics must be same as that of K9K4G08U0M*.**

NAND Flash Technical Notes

Initial Invalid Block(s)

Initial invalid blocks are defined as blocks that contain one or more initial invalid bits whose reliability is not guaranteed by Samsung. The information regarding the initial invalid block(s) is so called as the initial invalid block information. Devices with initial invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An initial invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the initial invalid block(s) via address mapping. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block, does not require Error Correction up to 1K program/erase cycles.

Identifying Initial Invalid Block(s)

All device locations are erased(FFh) except locations where the initial invalid block(s) information is written prior to shipping. The initial invalid block(s) status is defined by the 1st byte in the spare area. Samsung makes sure that either the 1st or 2nd page of every initial invalid block has non-FFh data at the column address of 2048. Since the initial invalid block information is also erasable in most cases, it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the initial invalid block(s) based on the initial invalid block information and create the initial invalid block table via the following suggested flow chart(Figure 3). Any intentional erasure of the initial invalid block information is prohibited.

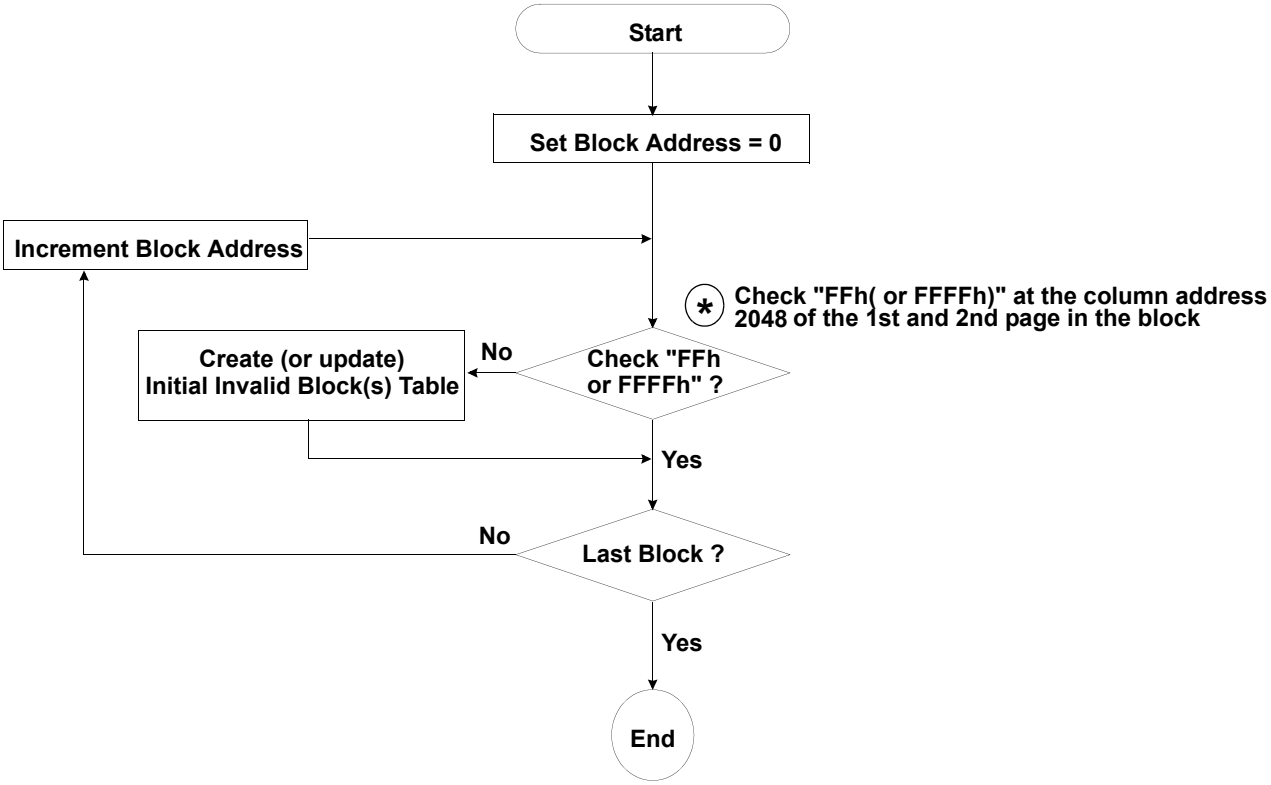


Figure 3. Flow chart to create initial invalid block table.

NAND Flash Technical Notes *(Continued)*

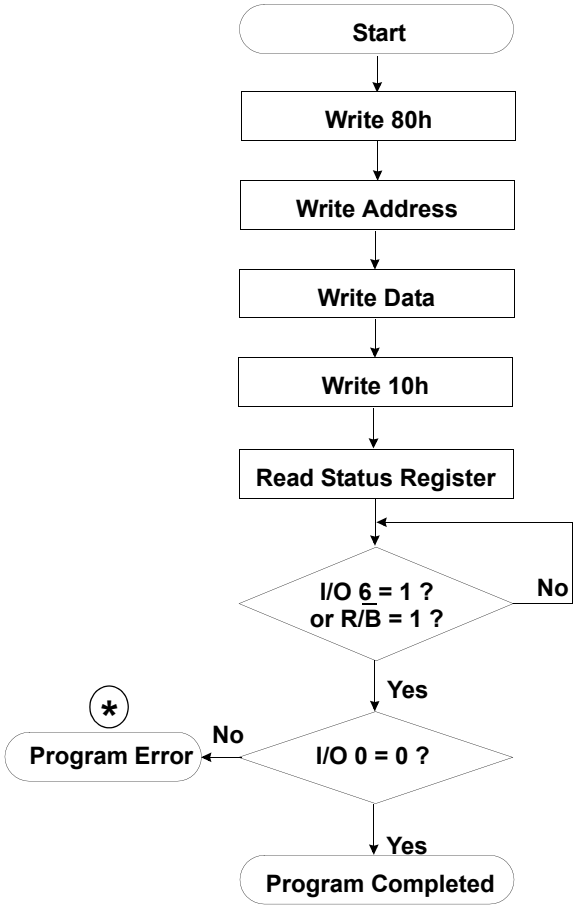
Error in write or read operation

Within its life time, additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the block failure rate.The following possible failure modes should be considered to implement a highly reliable system. In the case of status read failure after erase or program, block replacement should be done. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block. In case of Read, ECC must be employed. To improve the efficiency of memory space, it is recommended that the read failure due to single bit error should be reclaimed by ECC without any block replacement. The block failure rate in the qualification report does not include those reclaimed blocks.

Failure Mode		Detection and Countermeasure sequence
Write	Erase Failure	Status Read after Erase --> Block Replacement
	Program Failure	Status Read after Program --> Block Replacement
Read	Single Bit Failure	Verify ECC -> ECC Correction

ECC : Error Correcting Code --> Hamming Code etc.
Example) 1bit correction & 2bit detection

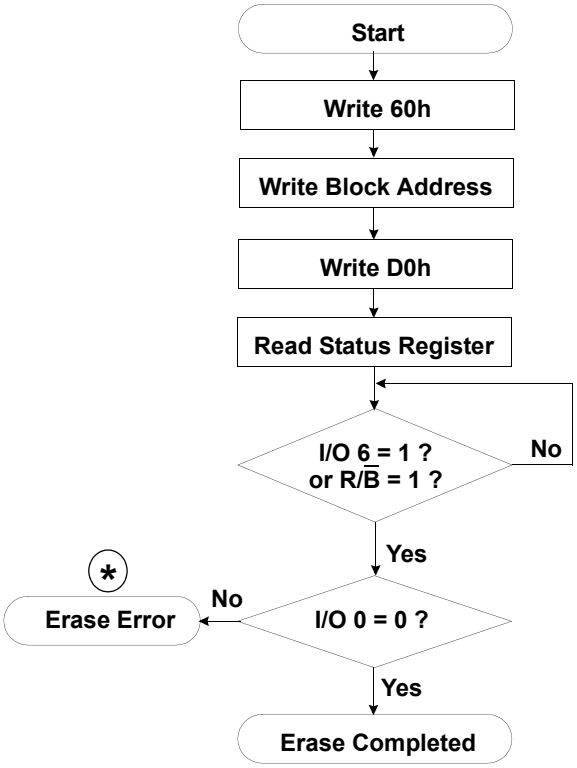
Program Flow Chart



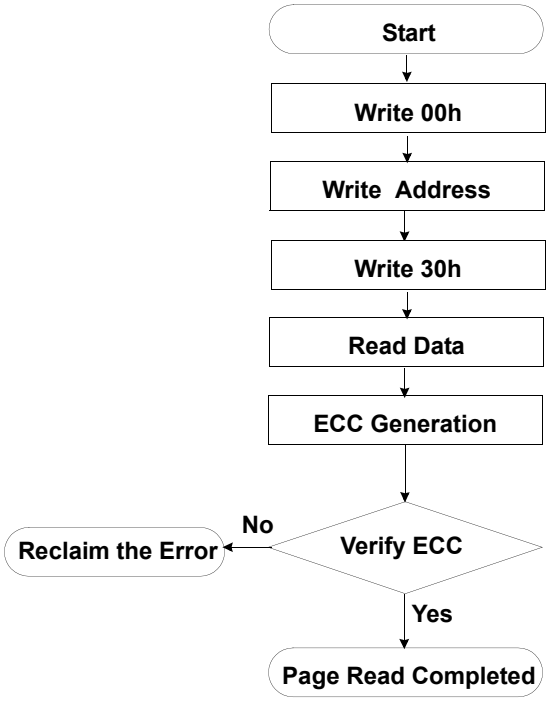
(*) : If program operation results in an error, map out the block including the page in error and copy the target data to another block.

NAND Flash Technical Notes *(Continued)*

Erase Flow Chart

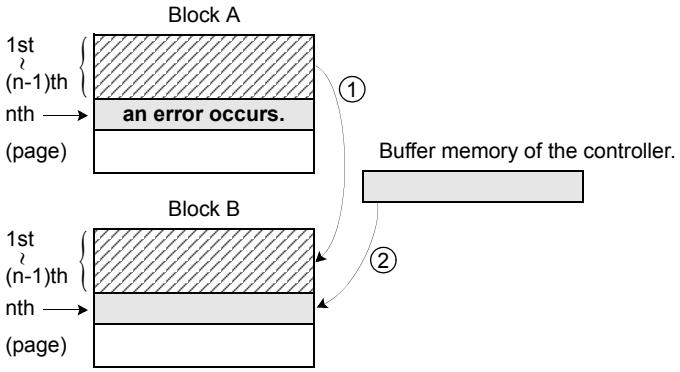


Read Flow Chart



(*) : If erase operation results in an error, map out the failing block and replace it with another block.

Block Replacement

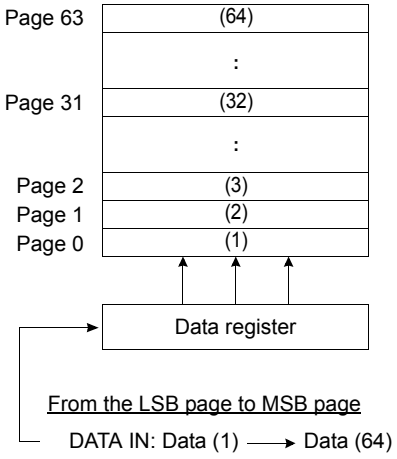


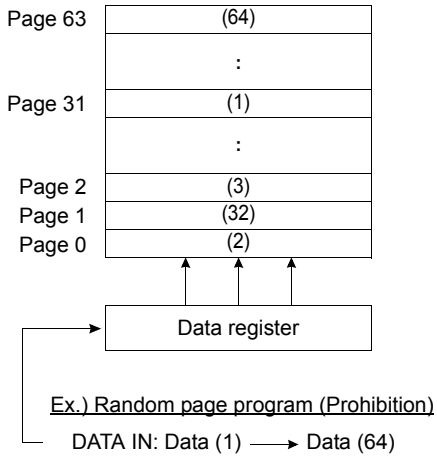
* Step1
When an error happens in the nth page of the Block 'A' during erase or program operation.
* Step2
Copy the data in the 1st ~ (n-1)th page to the same location of another free block. (Block 'B')
* Step3
Then, copy the nth page data of the Block 'A' in the buffer memory to the nth page of the Block 'B'.
* Step4
Do not erase or program to Block 'A' by creating an 'invalid Block' table or other appropriate scheme.

NAND Flash Technical Notes *(Continued)*

Addressing for program operation

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) pages of the block. Random page address programming is prohibited.





System Interface Using $\overline{CE}$ don't-care.

For an easier system interface, $\overline{CE}$ may be inactive during the data-loading or serial access as shown below. The internal 2112byte data registers are utilized as separate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications which use slow cycle time on the order of u-seconds, de-activating $\overline{CE}$ during the data-loading and serial access would provide significant savings in power consumption.

Figure 4. Program Operation with $\overline{CE}$ don't-care.

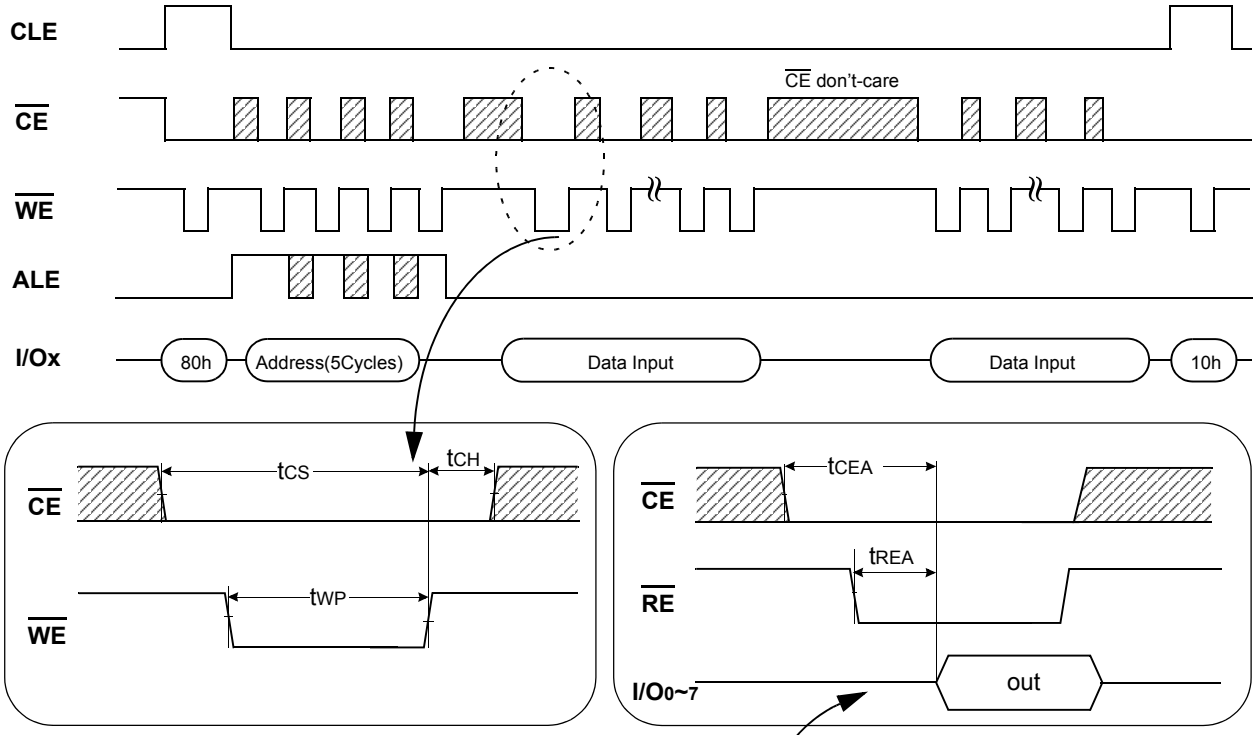
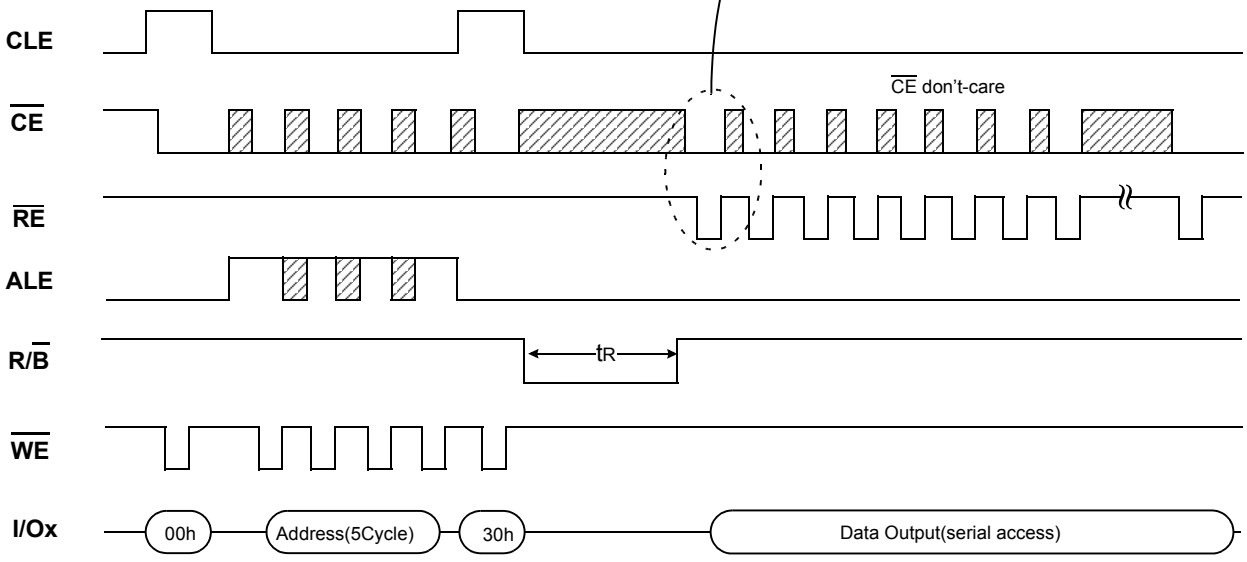


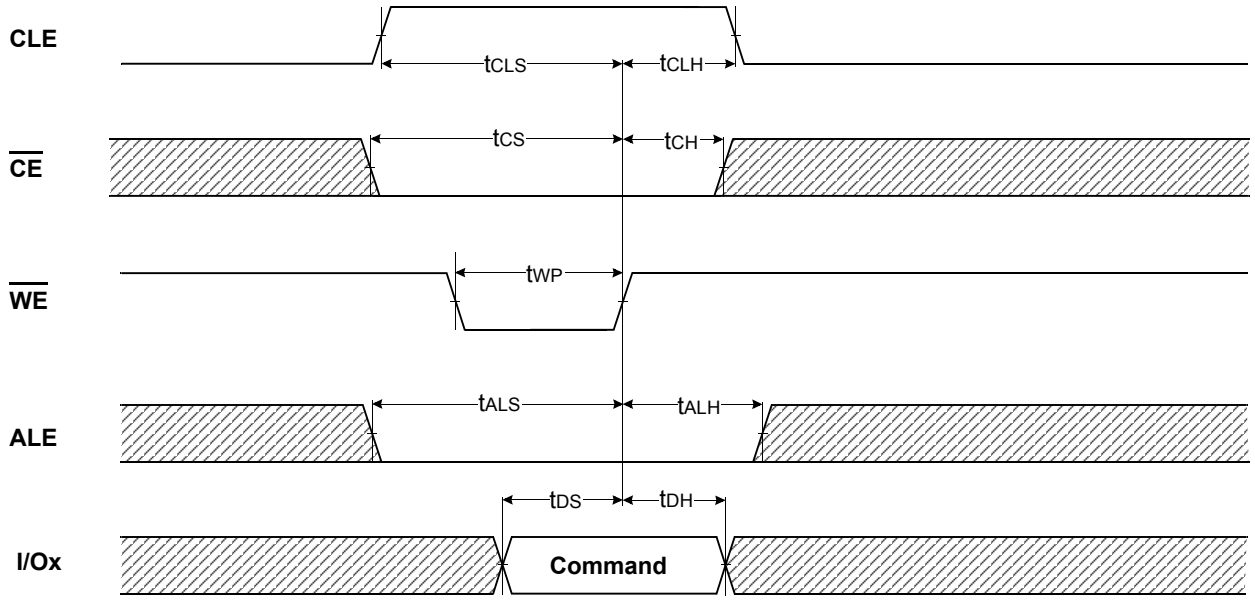
Figure 5. Read Operation with $\overline{CE}$ don't-care.



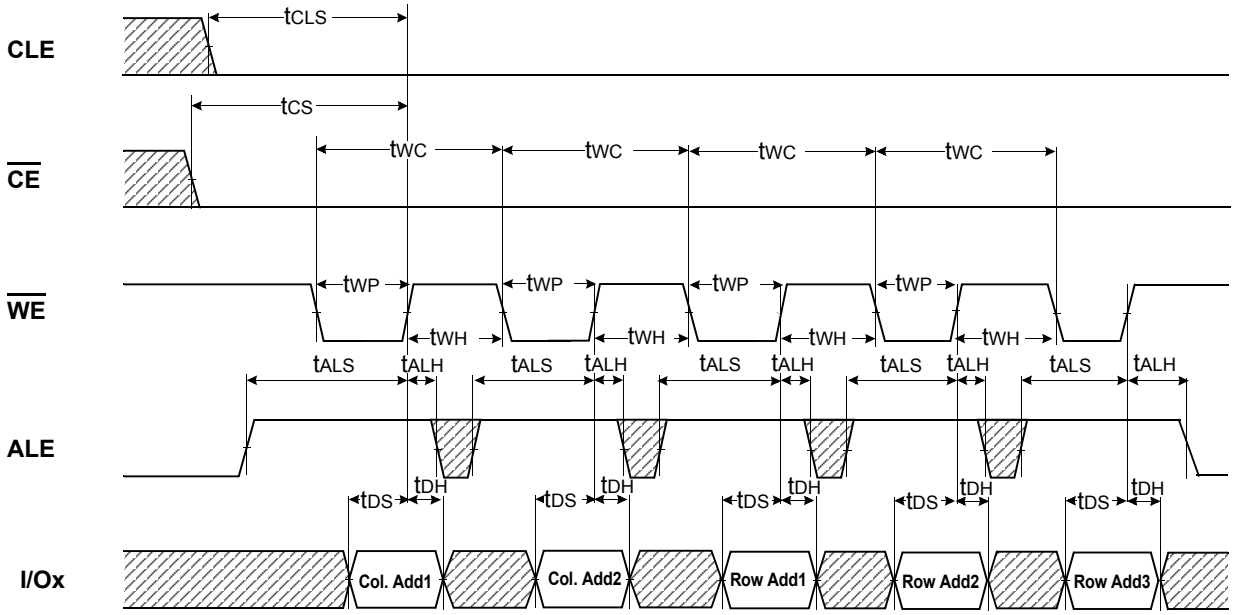
NOTE

Device	I/O	DATA	ADDRESS				
	I/Ox	Data In/Out	Col. Add1	Col. Add2	Row Add1	Row Add2	Row Add3
K9K4G08U0M	I/O 0 ~ I/O 7	~2112byte	A0~A7	A8~A11	A12~A19	A20~A27	A28~A29

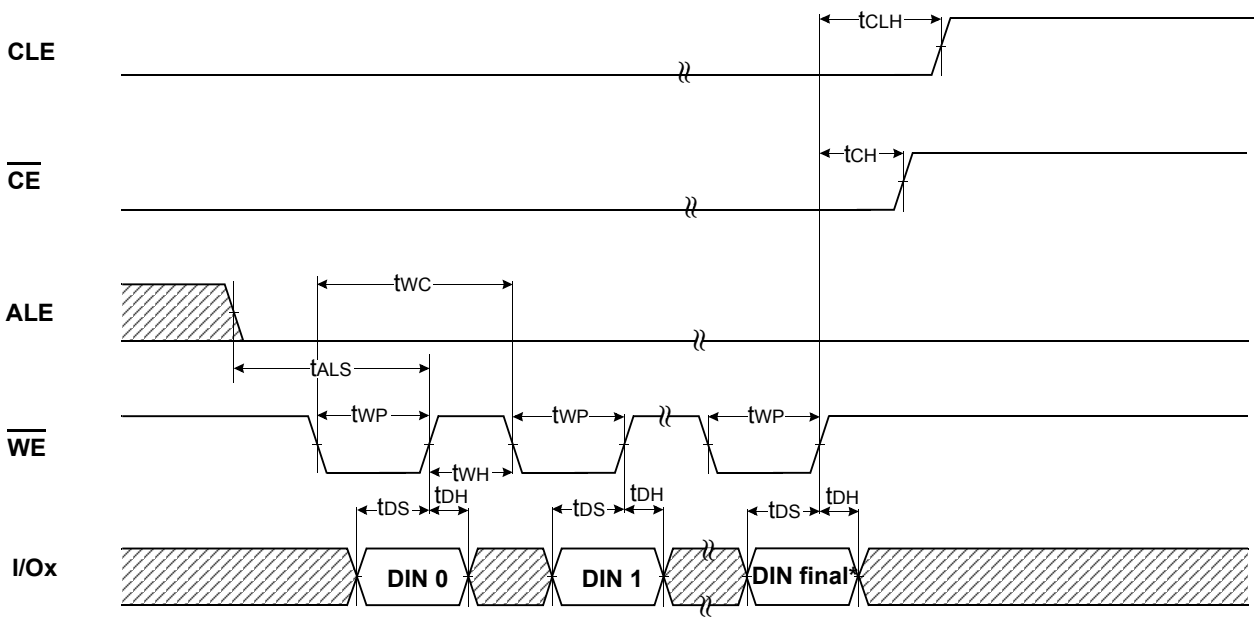
Command Latch Cycle



Address Latch Cycle

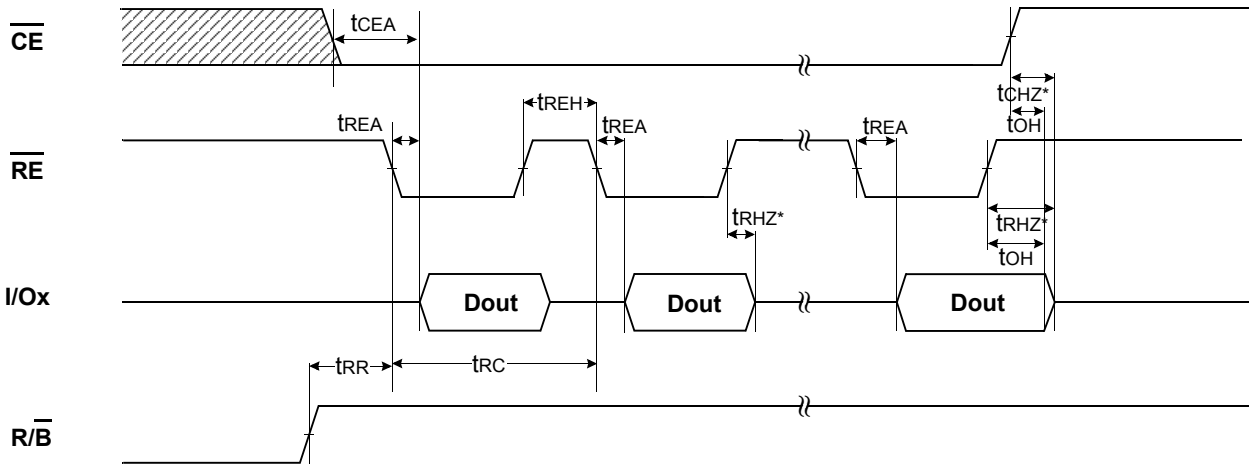


Input Data Latch Cycle



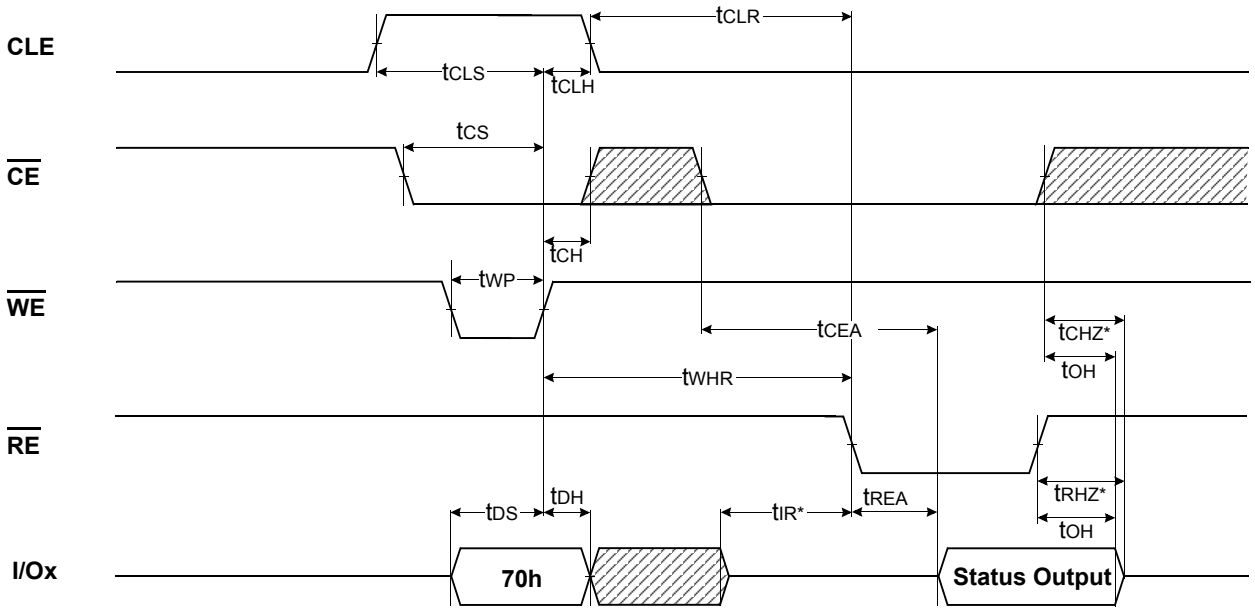
NOTES : DIN final means 2112

Serial Access Cycle after Read(CLE=L, $\overline{WE}$=H, ALE=L)

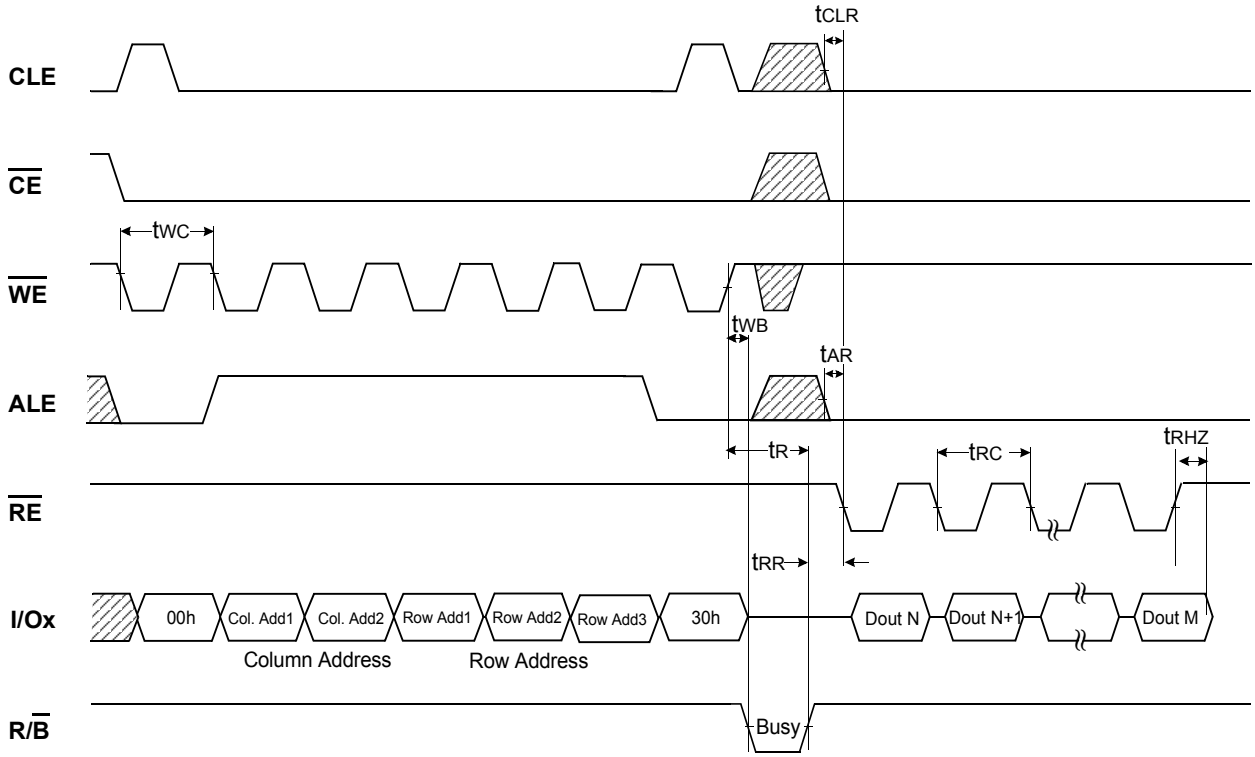


NOTES : Transition is measured ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.

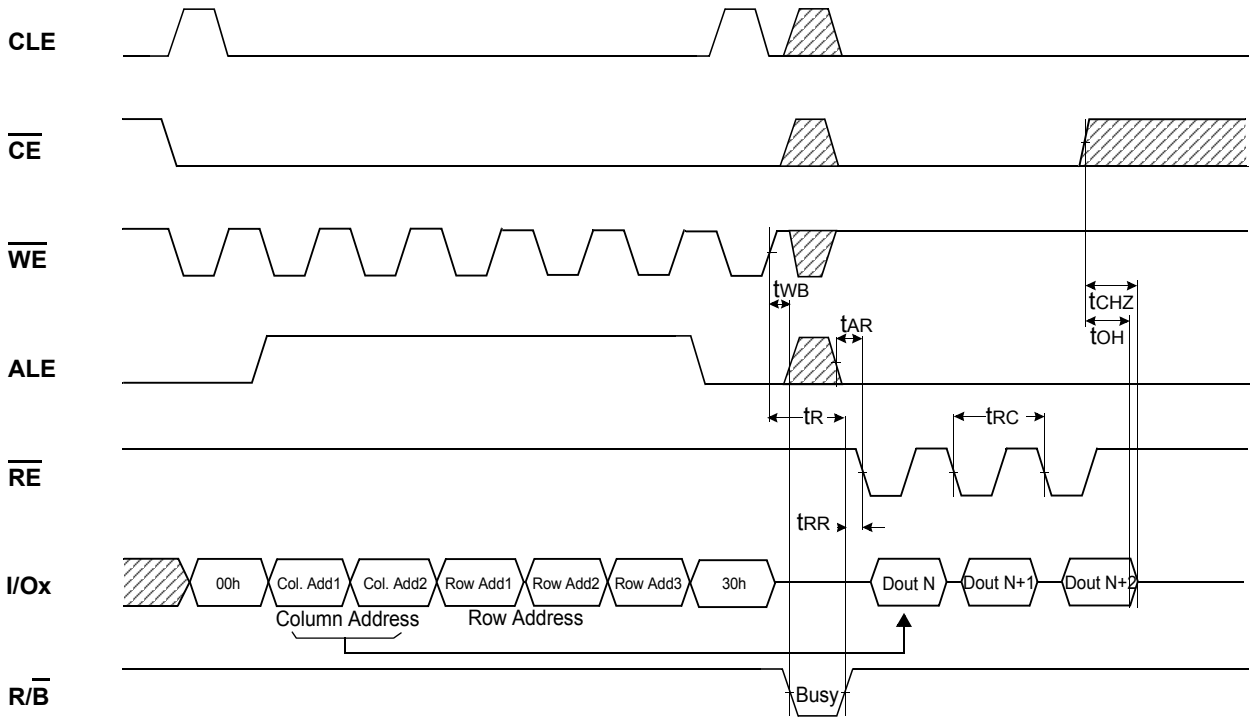
Status Read Cycle



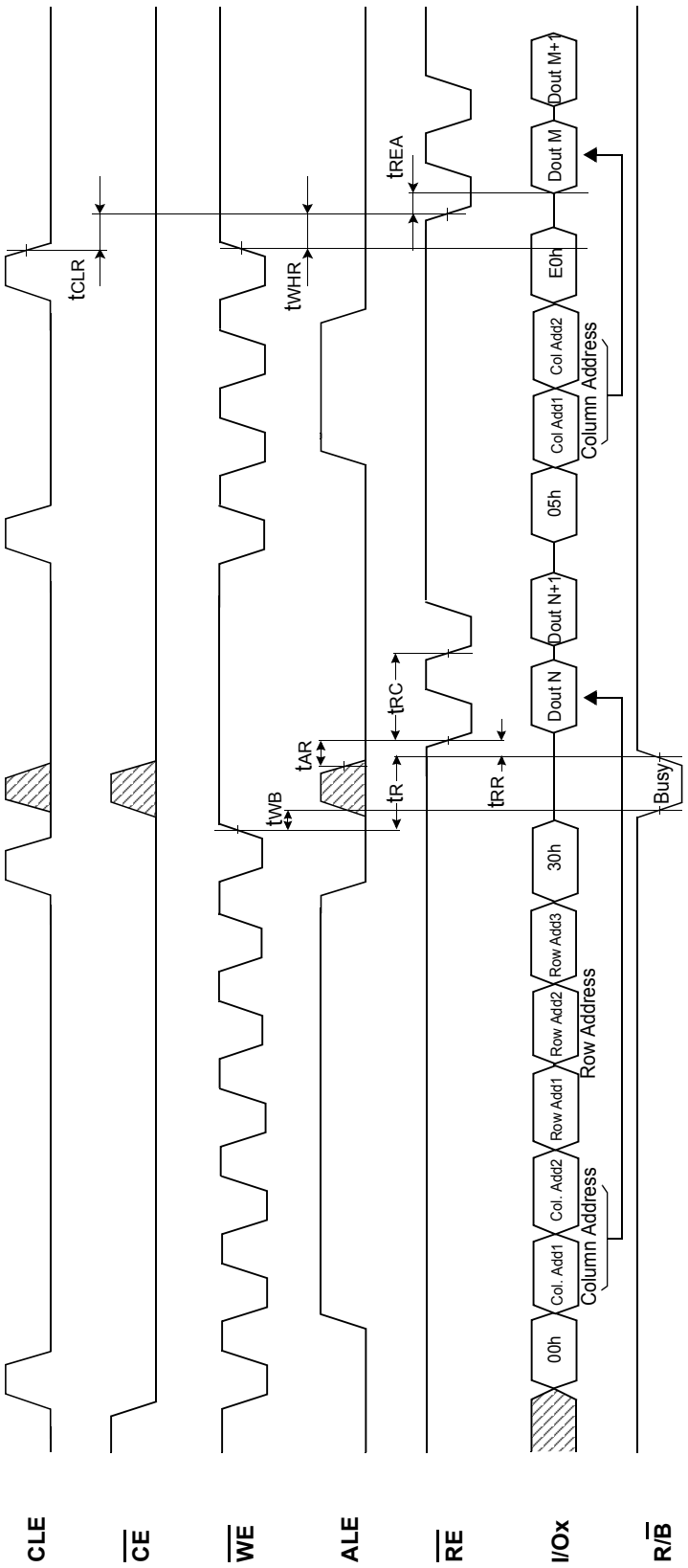
Read Operation



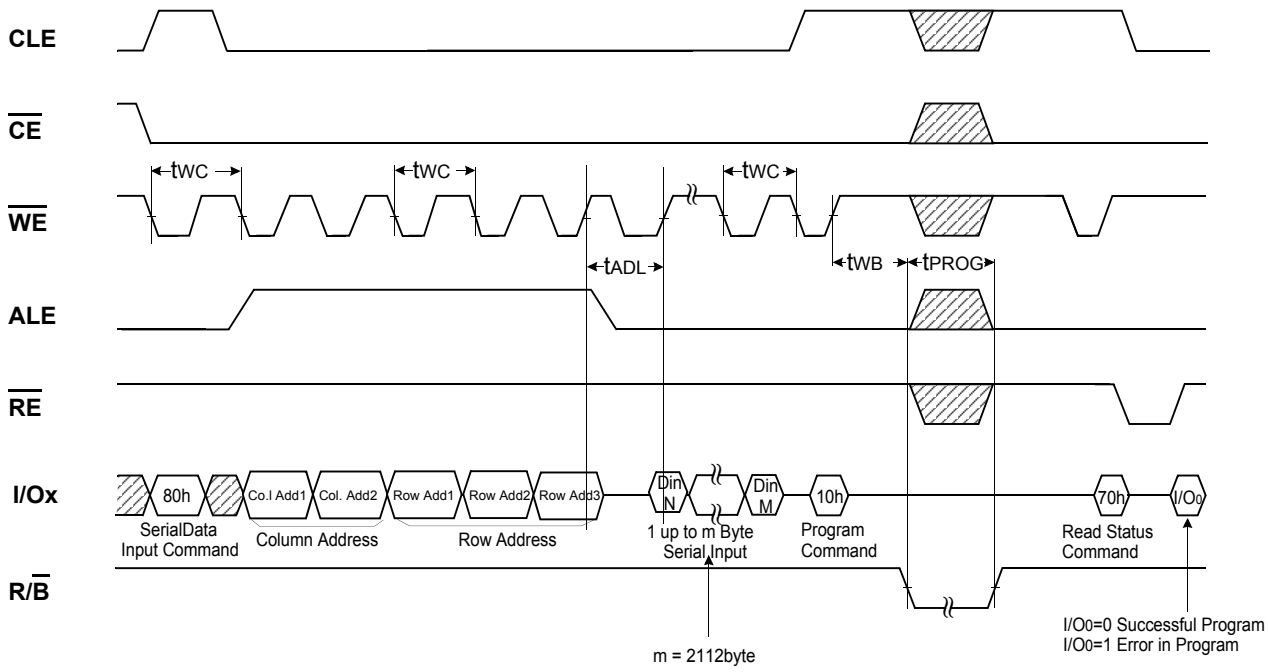
Read Operation(Intercepted by $\overline{CE}$)



Random Data Output In a Page

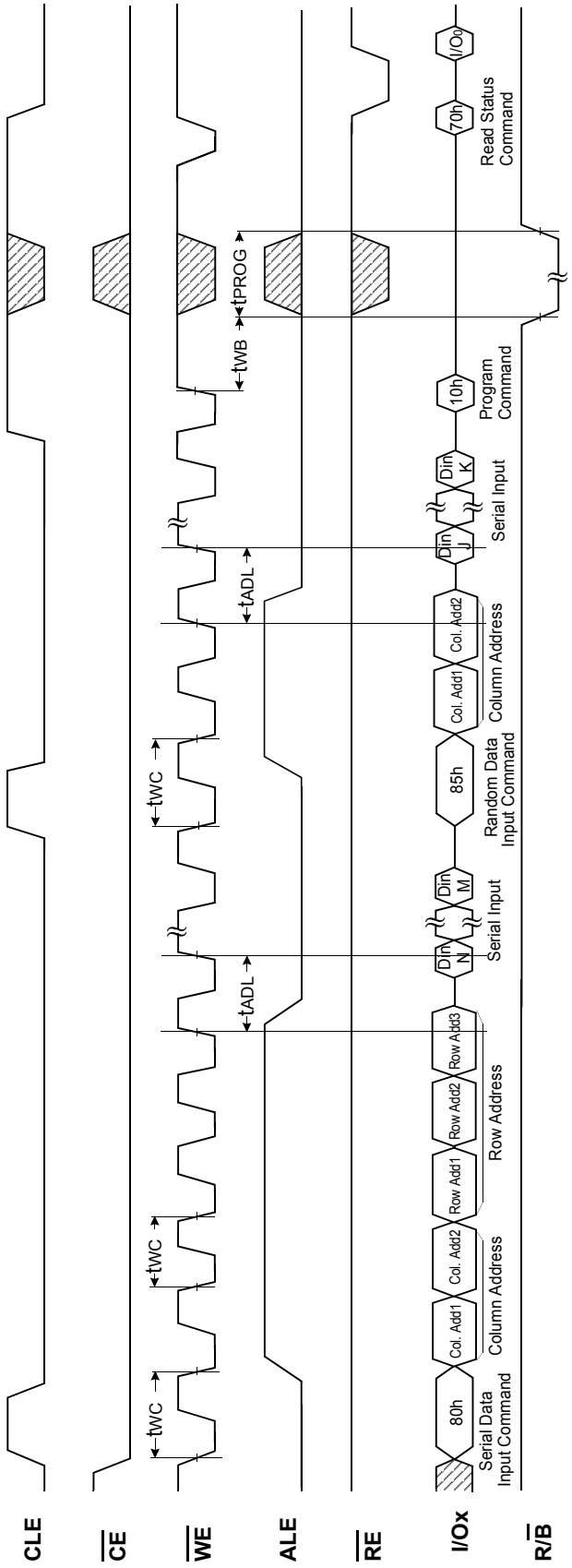


Page Program Operation



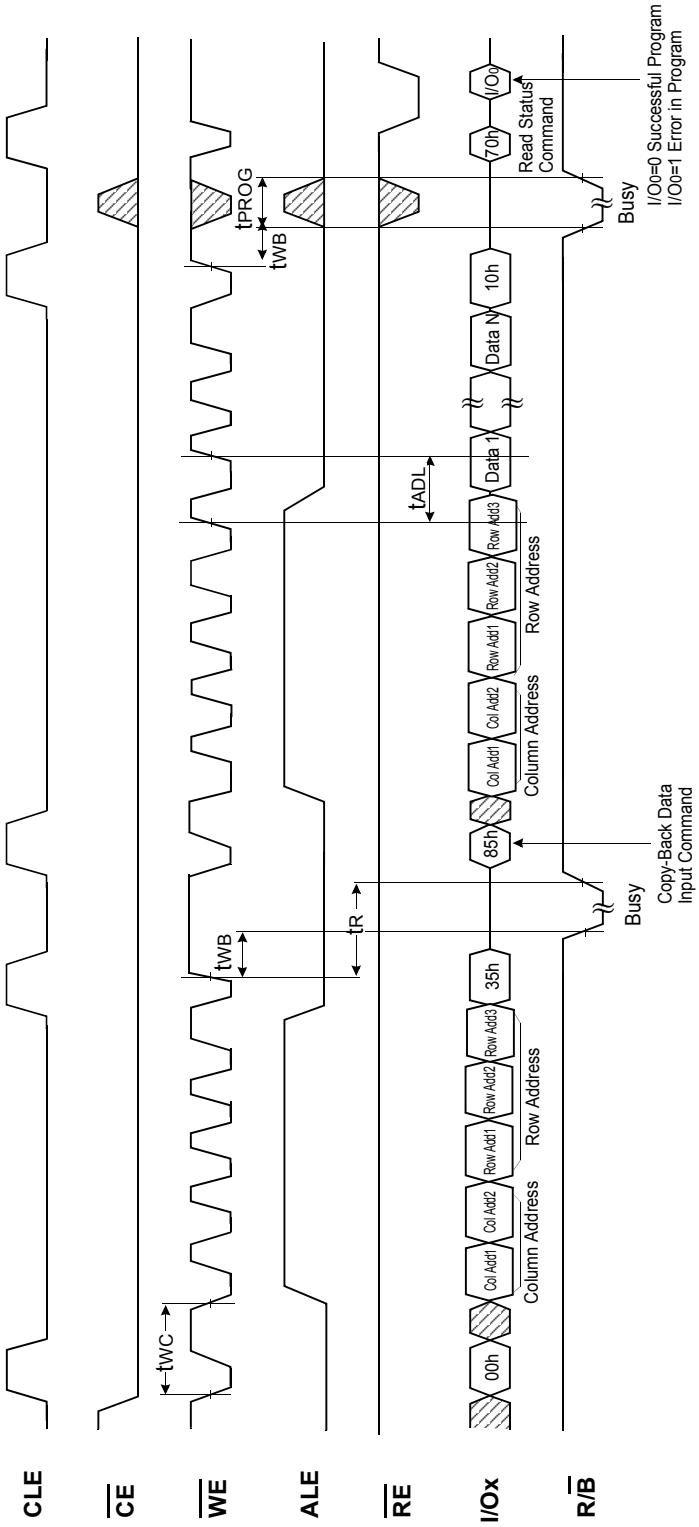
NOTES : tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle.

Page Program Operation with Random Data Input



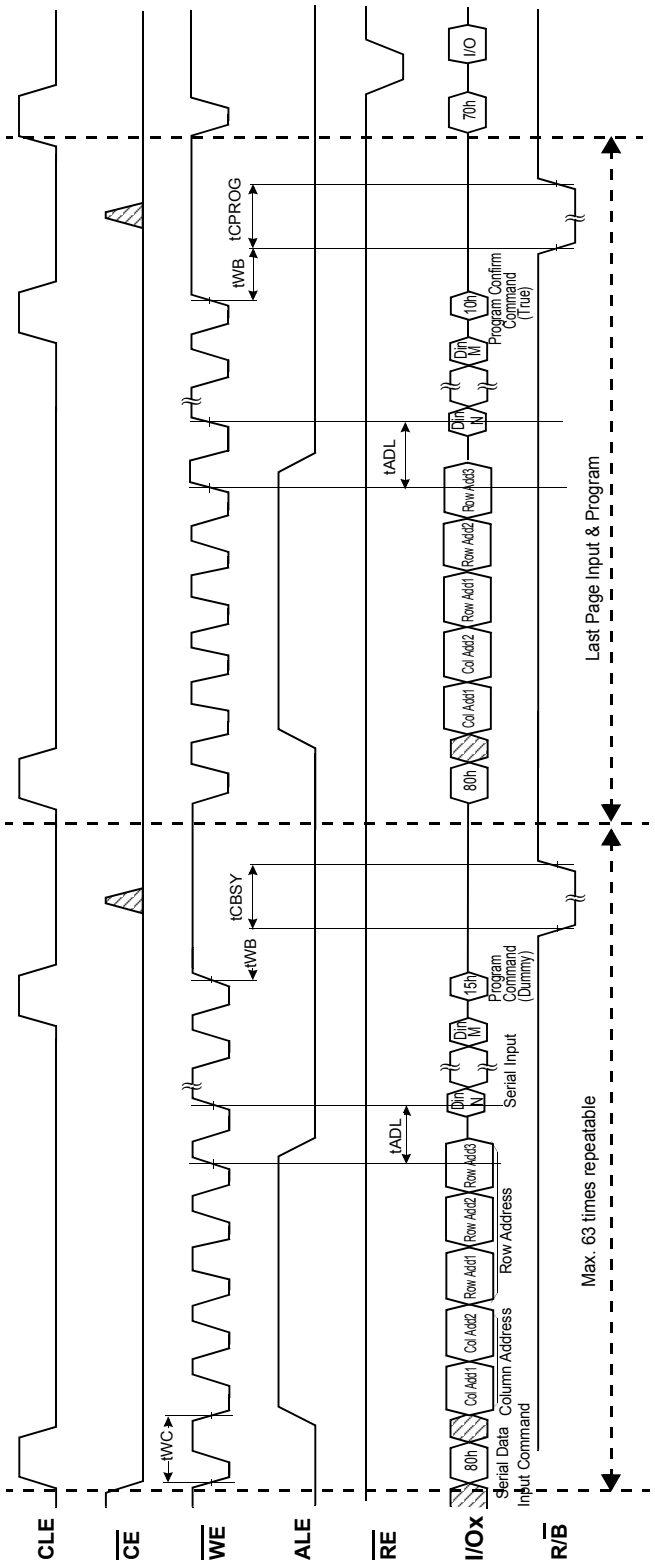
NOTES : tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle.

Copy-Back Program Operation With Random Data Input



NOTES : tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle.

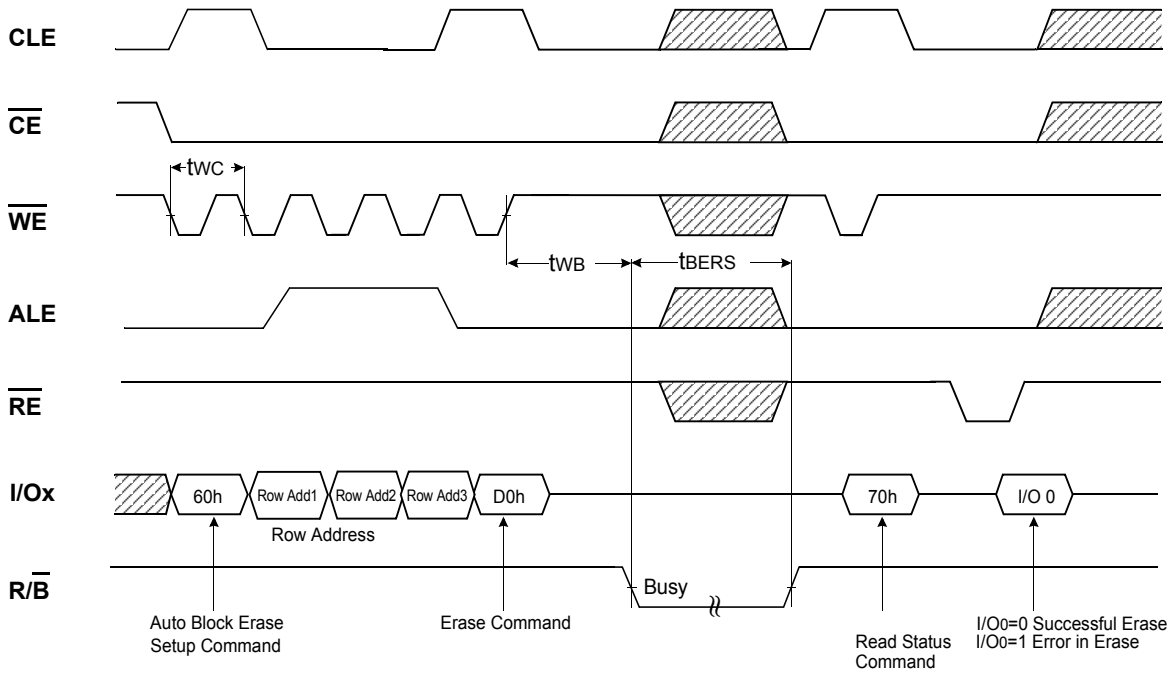
Cache Program Operation(available only within a block)



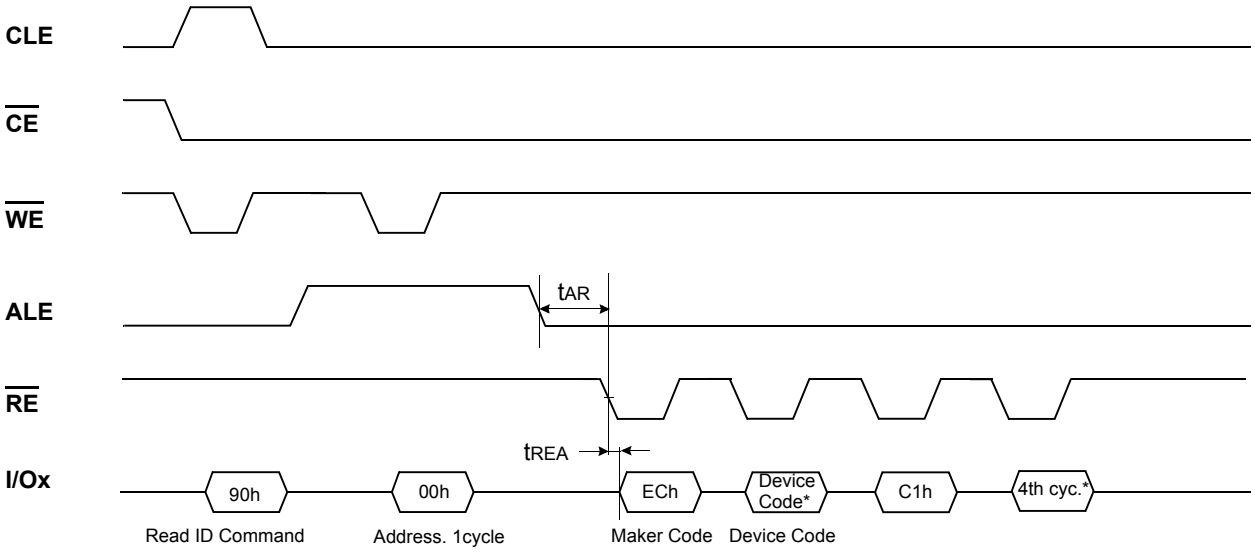
NOTES : tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle.

Ex.) Cache Program

BLOCK ERASE OPERATION



Read ID Operation



Device	Device Code*(2nd Cycle)	4th Cycle*
K9K4G08U0M	DCh	15h
K9W8G08U1M	Same as each K9K4G08U0M in it	

ID Defintition Table
90 ID : Access command = 90H

	Description
1st Byte	Maker Code
2nd Byte	Device Code
3rd Byte	Don't care
4th Byte	Page Size, Block Size, Spare Size, Organization

4th ID Data

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Page Size (w/o redundant area)	1KB 2KB Reserved Reserved							0 0 1 1	0 1 0 1
Blcok Size (w/o redundant area)	64KB 128KB 256KB Reserved			0 0 1 1	0 1 0 1				
Redundant Area Size (byte/512byte)	8 16						0 1		
Organization	x8 x16		0 1						
Serial AccessMinimum	50ns/30ns 25ns Reserved Reserved	0 1 0 1				0 0 1 1			

Device Operation

PAGE READ

Page read is initiated by writing 00h-30h to the command register along with five address cycles. After initial power up, 00h command is latched. Therefore only five address cycles and 30h command initiates that operation after initial power up. The 2,112 bytes of data within the selected page are transferred to the data registers in less than 25μs(tR). The system controller can detect the completion of this data transfer(tR) by analyzing the output of R/$\overline{B}$ pin. Once the data in a page is loaded into the data registers, they may be read out in 30ns cycle time by sequentially pulsing $\overline{RE}$. The repetitive high to low transitions of the $\overline{RE}$ clock make the device output the data starting from the selected column address up to the last column address.

The device may output random data in a page instead of the consecutive sequential data by writing random data output command. The column address of next data, which is going to be out, may be changed to the address which follows random data output command. Random data output can be operated multiple times regardless of how many times it is done in a page.

Figure 6. Read Operation

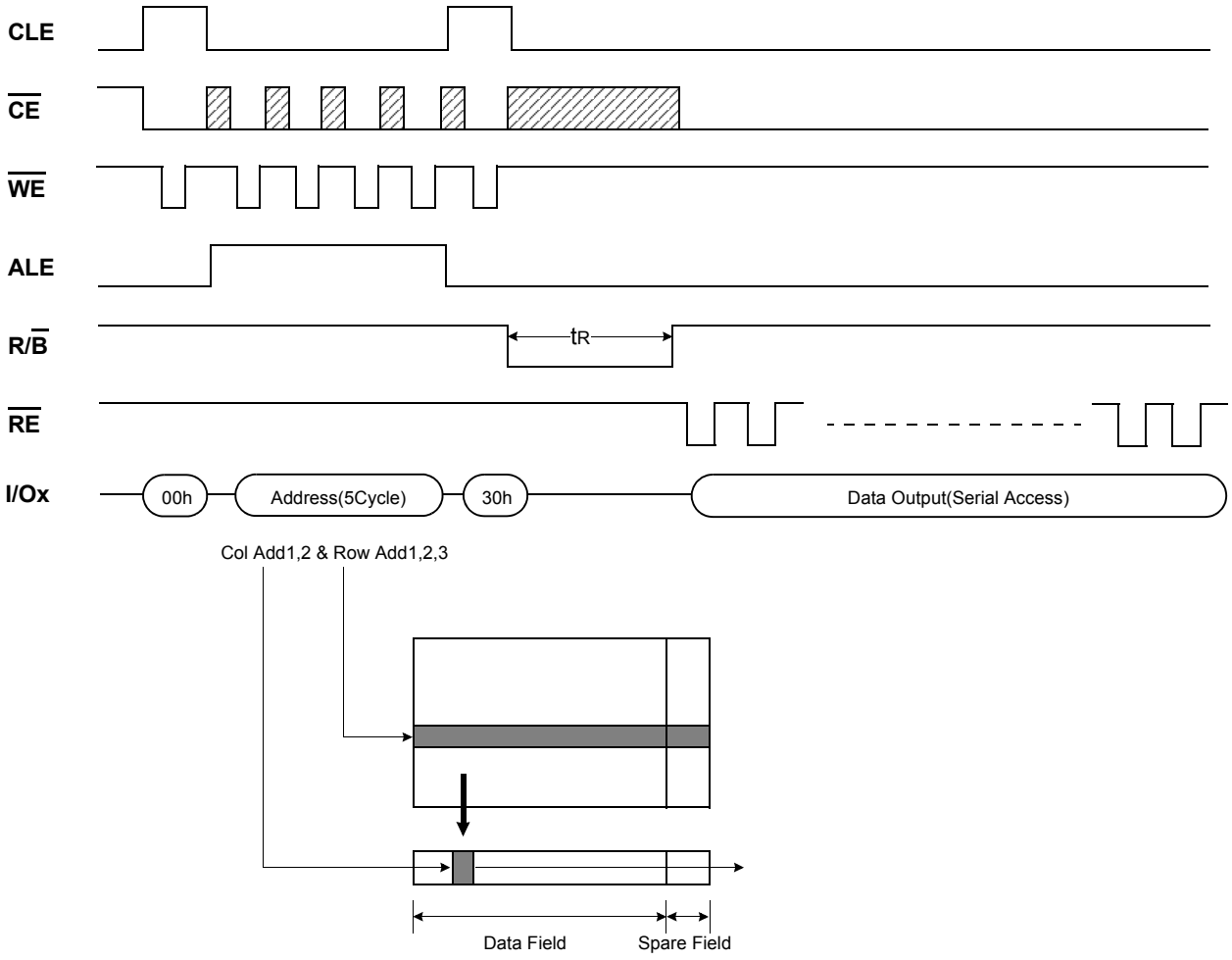
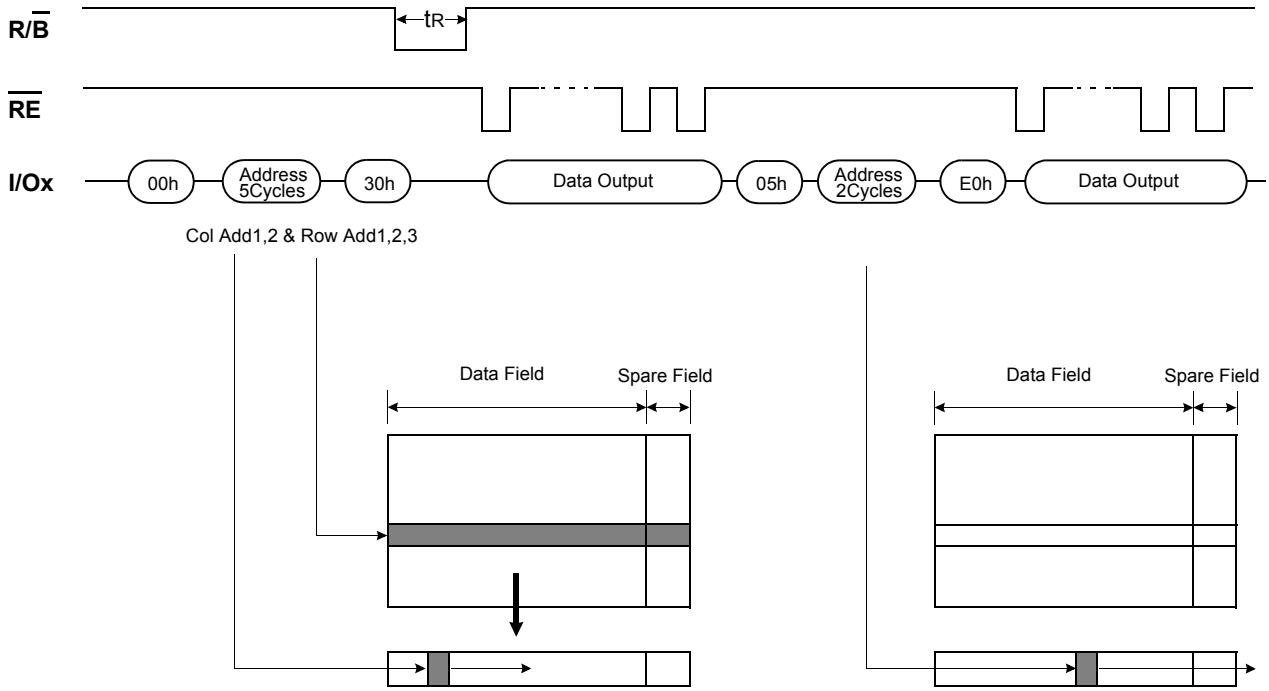


Figure 7. Random Data Output In a Page



PAGE PROGRAM

The device is programmed basically on a page basis, but it does allow multiple partial page programing of a word or consecutive bytes up to 2112, in a single page program cycle. The number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed 4 times for main array(1time/512byte) and 4 times for spare array (1time/16byte). The addressing should be done in sequential order in a block. A page program cycle consists of a serial data loading period in which up to 2112bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell.

The serial data loading period begins by inputting the Serial Data Input command(80h), followed by the five cycle address inputs and then serial data loading. The words other than those to be programmed do not need to be loaded. The device supports random data input in a page. The column address for the next data, which will be entered, may be changed to the address which follows random data input command(85h). Random data input may be operated multiple times regardless of how many times it is done in a page.

The Page Program confirm command(10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write state controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or the Status bit(I/O 6) Page Program is complete, the Write Status Bit(I/O 0) may be checked(Figure 8). The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

Figure 8. Program & Read Status Operation

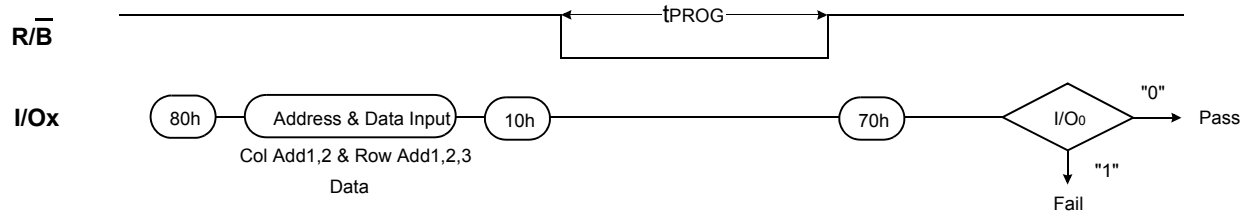
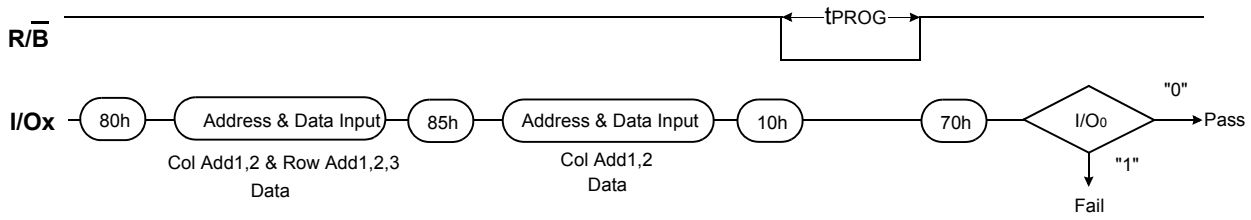


Figure 9. Random Data Input In a Page

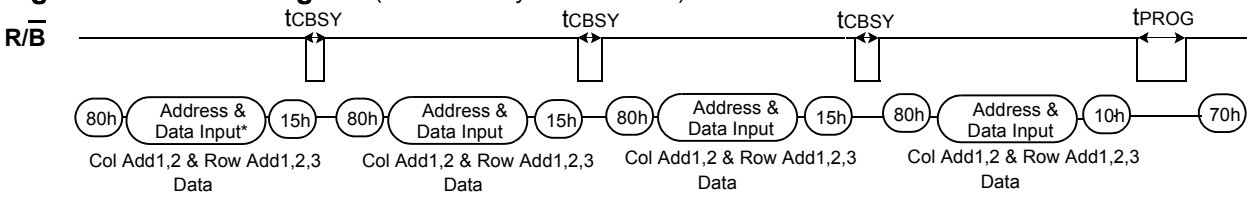


Cache Program

Cache Program is an extension of Page Program, which is executed with 2112byte data registers, and is available only within a block. Since the device has 1 page of cache memory, serial data input may be executed while data stored in data register are programmed into memory cell.

After writing the first set of data up to 2112byte into the selected cache registers, Cache Program command (15h) instead of actual Page Program (10h) is inputted to make cache registers free and to start internal program operation. To transfer data from cache registers to data registers, the device remains in Busy state for a short period of time(tCBSY) and has its cache registers ready for the next data-input while the internal programming gets started with the data loaded into data registers. Read Status command (70h) may be issued to find out when cache registers become ready by polling the Cache-Busy status bit(I/O 6). Pass/fail status of only the previouse page is available upon the return to Ready state. When the next set of data is inputted with the Cache Program command, tCBSY is affected by the progress of pending internal programming. The programming of the cache registers is initiated only when the pending program cycle is finished and the data registers are available for the transfer of data from cache registers. The status bit(I/O5) for internal Ready/Busy may be polled to identify the completion of internal programming. If the system monitors the progress of programming only with R/B, the last page of the target programming sequence must be progammed with actual Page Program command (10h).

Figure 10. Cache Program (available only within a block)



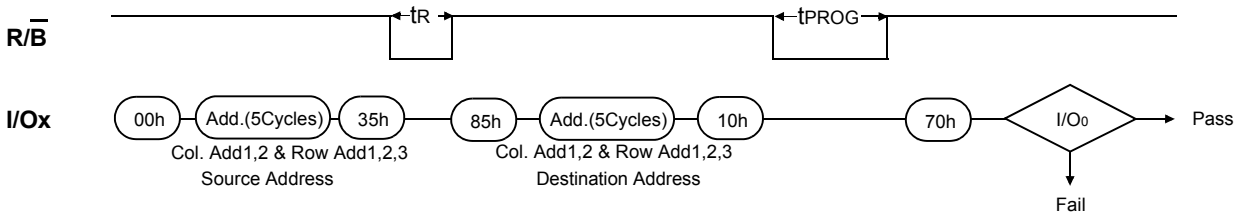
NOTE : Since programming the last page does not employ caching, the program time has to be that of Page Program. However, if the previous program cycle with the cache data has not finished, the actual program cycle of the last page is initiated only after completion of the previous cycle, which can be expressed as the following formula.

tPROG= Program time for the last page+ Program time for the (last -1)th page
- (Program command cycle time + Last page data loading time)

Copy-Back Program

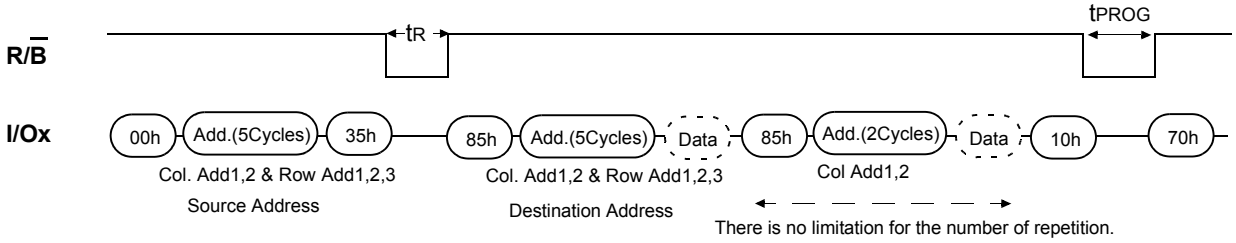
The copy-back program is configured to quickly and efficiently rewrite data stored in one page without utilizing an external memory. Since the time-consuming cycles of serial access and re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block also need to be copied to the newly assigned free block. The operation for performing a copy-back program is a sequential execution of page-read without serial access and copying-program with the address of destination page. A read operation with "35h" command and the address of the source page moves the whole 2112byte data into the internal data buffer. As soon as the device returns to Ready state, Page-Copy Data-input command (85h) with the address cycles of destination page followed may be written. The Program Confirm command (10h) is required to actually begin the programming operation. Copy-Back Program operation is allowed only within the same memory plane. Once the Copy-Back Program is finished, any additional partial page programming into the copied pages is prohibited before erase. The MSB(A29) must be the same between source and target page during copy-back program.Data input cycle for modifying a portion or multiple distant portions of the source page is allowed as shown in Figure 11.**"When there is a program-failure at Copy-Back operation, error is reported by pass/fail status. But if the soure page has an error bit by charge loss, accumulated copy-back operations could also accumulate bit errors. In this case, verifying the source page for a bit error is recommended before Copy-back program"**

Figure 11. Page Copy-Back program Operation



NOTE: It's prohibited to operate Copy-Back program from an odd address page(source page) to an even address page(target page) or from an even address page(source page) to an odd address page(target page). Therefore, the Copy-Back program is permitted just between odd address pages or even address pages.

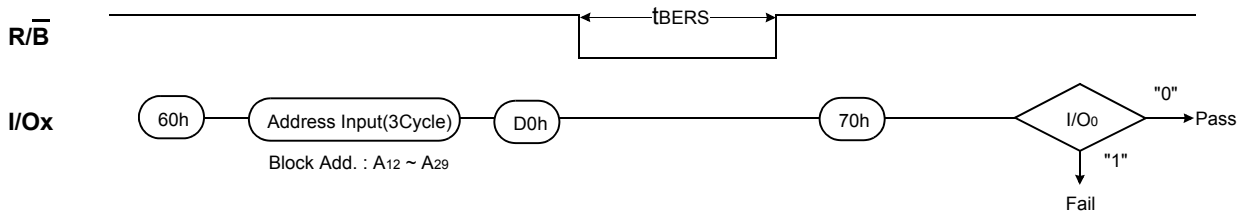
Figure 12. Page Copy-Back program Operation with Random Data Input



BLOCK ERASE

The Erase operation is done on a block basis. Block address loading is accomplished in three cycles initiated by an Erase Setup command(60h). Only address A_{18} to A_{29} is valid while A_{12} to A_{17} is ignored. The Erase Confirm command(D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.
At the rising edge of $\overline{WE}$ after the erase confirm command input, the internal write controller handles erase and erase-verify. When the erase operation is completed, the Write Status Bit(I/O 0) may be checked. Figure 13 details the sequence.

Figure 13. Block Erase Operation



READ STATUS

The device contains a Status Register which may be read to find out whether program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of $\overline{CE}$ or $\overline{RE}$, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/$\overline{B}$ pins are common-wired. $\overline{RE}$ or $\overline{CE}$ does not need to be toggled for updated status. Refer to table 2 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command(00h) should be given before starting read cycles.

Table2. Read Staus Register Definition

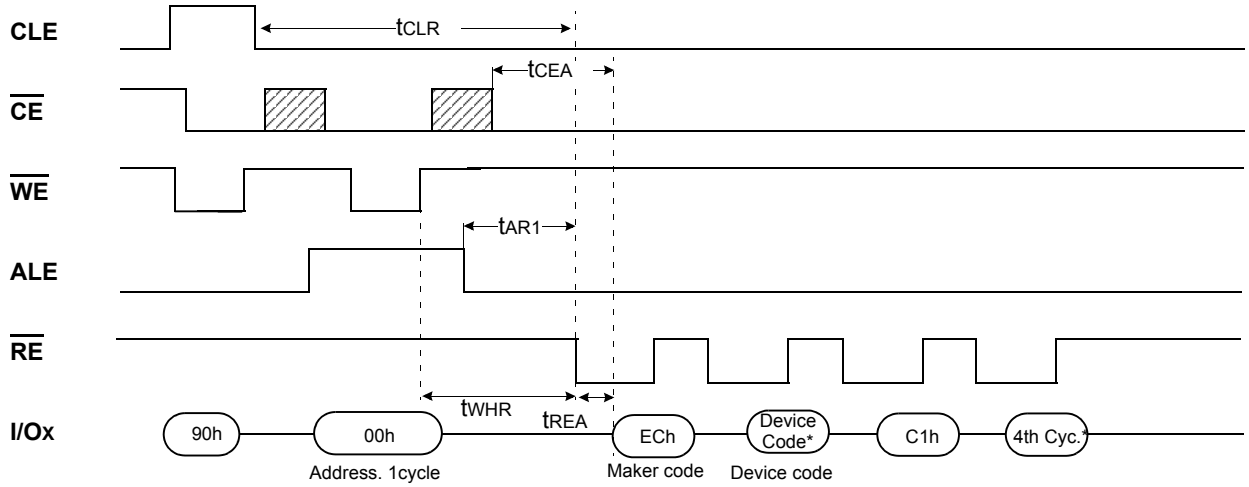
I/O No.	Page Program	Block Erase	Cache Prorgam	Read	Definition	
I/O 0	Pass/Fail	Pass/Fail	Pass/Fail(N)	Not use	Pass : "0"	Fail : "1"
I/O 1	Not use	Not use	Pass/Fail(N-1)	Not use	Pass : "0"	Fail : "1"
I/O 2	Not use	Not use	Not use	Not use	Don't -cared	
I/O 3	Not Use	Not Use	Not Use	Not Use	Don't -cared	
I/O 4	Not Use	Not Use	Not Use	Not Use	Don't -cared	
I/O 5	Ready/Busy	Ready/Busy	True Ready/Busy	Ready/Busy	Busy : "0"	Ready : "1"
I/O 6	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Busy : "0"	Ready : "1"
I/O 7	Write Protect	Write Protect	Write Protect	Write Protect	Protected : "0"	Not Protected

NOTE : 1. True Ready/Busy represents internal program operation status which is being executed in cache program mode.
2. I/Os defined 'Not use' are recommended to be masked out when Read Status is being executed.

Read ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Five read cycles sequentially output the manufacturer code(ECh), and the device code and XXh, 4th cycle ID respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 14 shows the operation sequence.

Figure 14. Read ID Operation



Device	Device Code*(2nd Cycle)	3rd Cycle	4th Cycle*
K9K4G08U0M	DCh	C1h	15h
K9W8G08U1M	Same as each K9K4G08U0M in it		

RESET

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when $\overline{WP}$ is high. Refer to table 3 for device status after reset operation. If the device is already in reset state a new reset command will be accepted by the command register. The R/$\overline{B}$ pin transitions to low for tRST after the Reset command is written. Refer to Figure 15 below.

Figure 15. RESET Operation

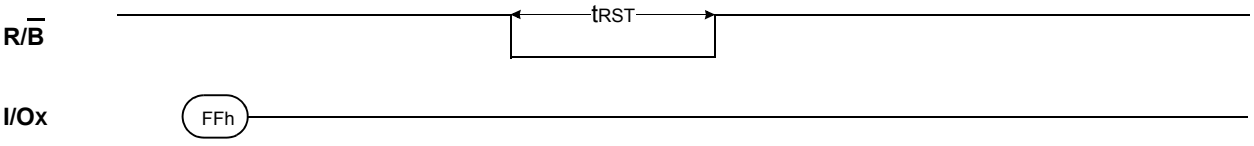


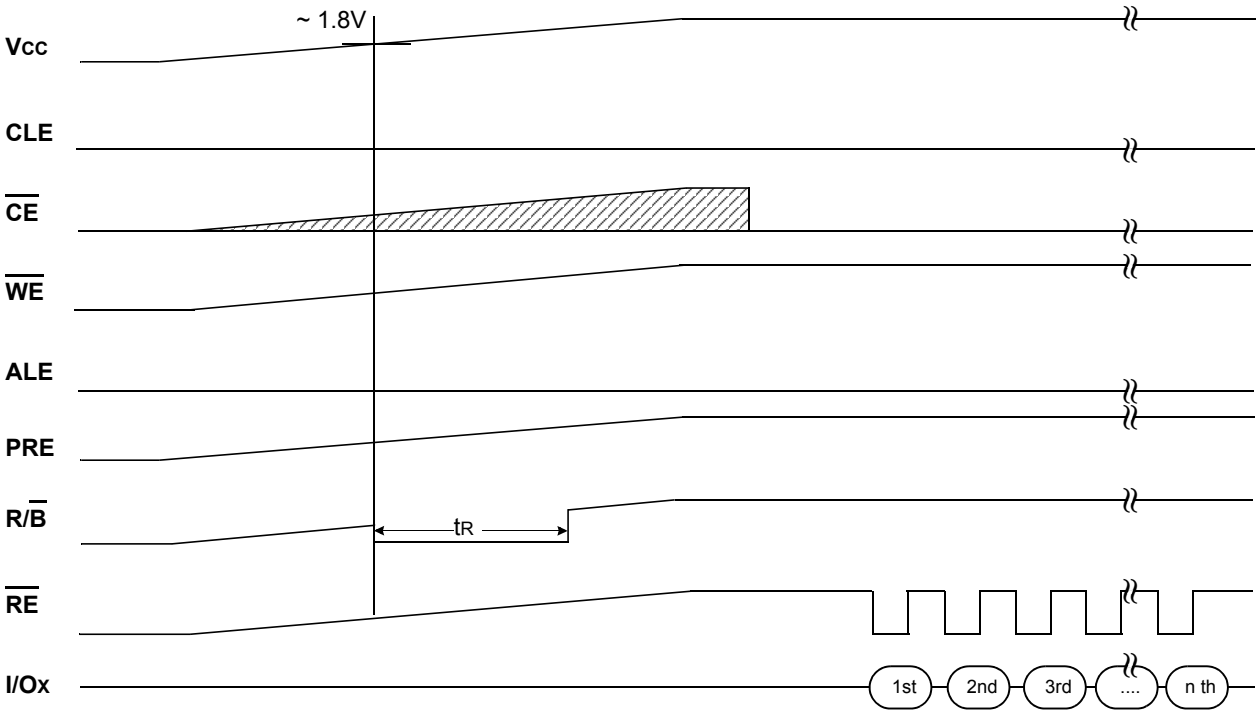
Table3. Device Status

	After Power-up		After Reset
PRE status	High	Low	Waiting for next command
Operation Mode	First page data access is ready	00h command is latched	

Power-On Auto-Read

The device is designed to offer automatic reading of the first page without command and address input sequence during power-on. An internal voltage detector enables auto-page read functions when Vcc reaches about 1.8V. PRE pin controls activation of auto-page read function. Auto-page read function is enabled only when PRE pin is tied to V_{CC}. Serial access may be done after power-on without latency.

Figure 16. Power-On Auto-Read



READY/$\overline{BUSY}$

The device has a R/$\overline{B}$ output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/$\overline{B}$ pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/$\overline{B}$ outputs to be Or-tied. Because pull-up resistor value is related to tr(R/$\overline{B}$) and current drain during busy(ibusy) , an appropriate value can be obtained with the following reference chart(Fig 17). Its value can be determined by the following guidance.

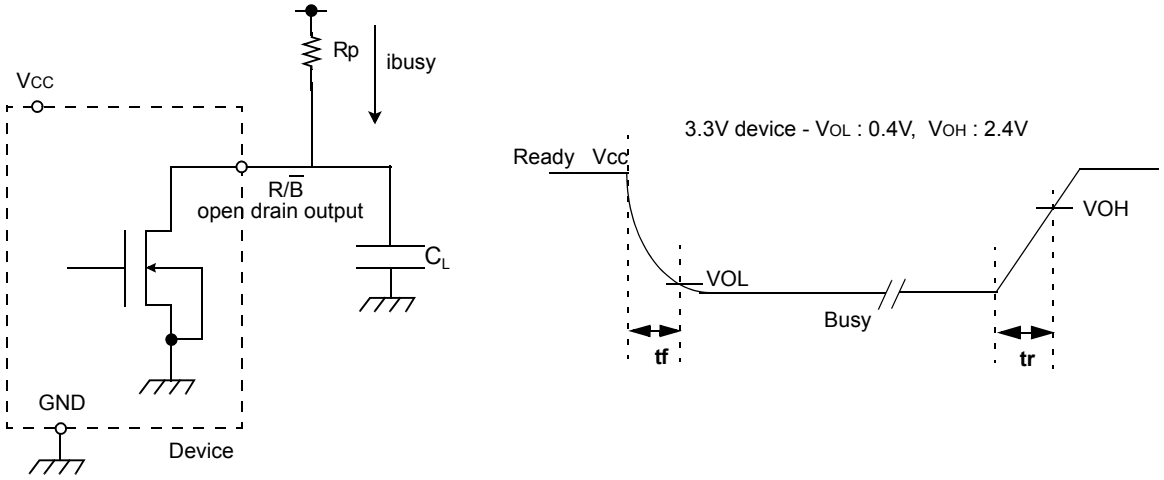
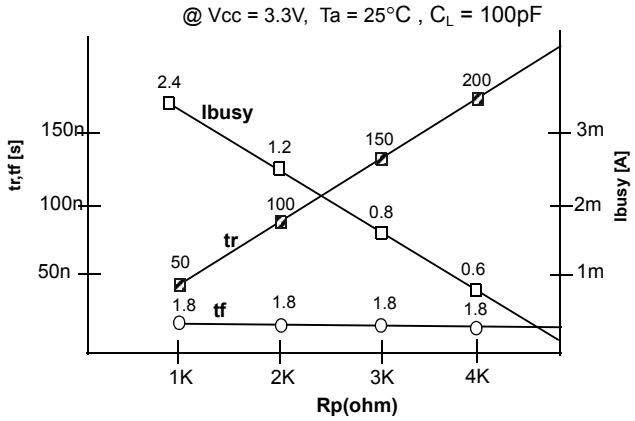


Figure 17. Rp vs tr ,tf & Rp vs ibusy



Rp value guidance

$$Rp(min, 3.3V\ part) = \frac{V_{CC}(Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{3.2V}{8mA + \Sigma I_L}$$

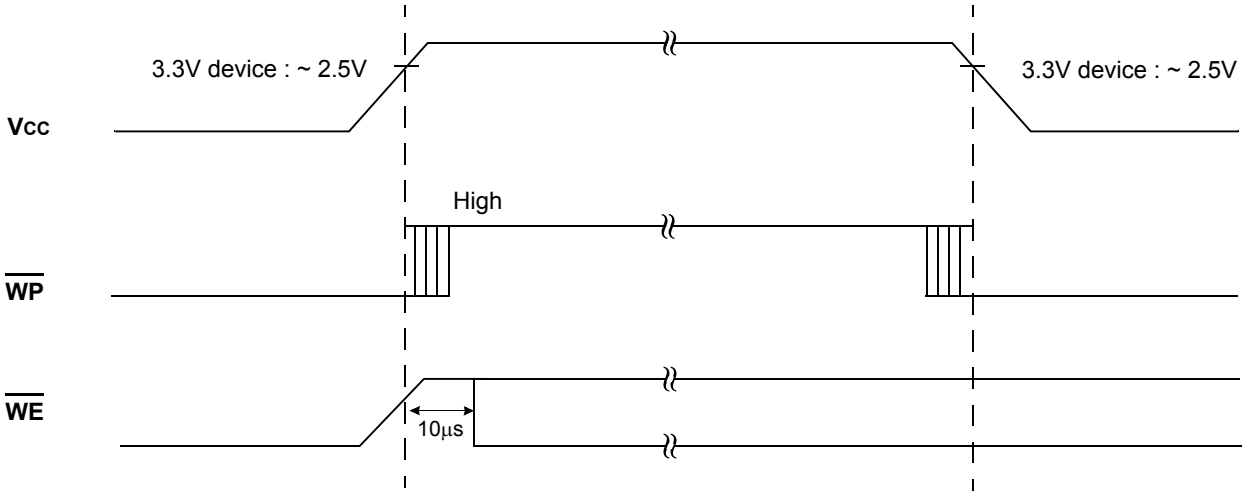
where I_L is the sum of the input currents of all devices tied to the R/$\overline{B}$ pin.

Rp(max) is determined by maximum permissible limit of tr

Data Protection & Power up sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 2V. $\overline{WP}$ pin provides hardware protection and is recommended to be kept at V_{IL} during power-up and power-down. A recovery time of minimum 10μs is required before internal circuit gets ready for any command sequences as shown in Figure 18. The two step command sequence for program/erase provides additional software protection.

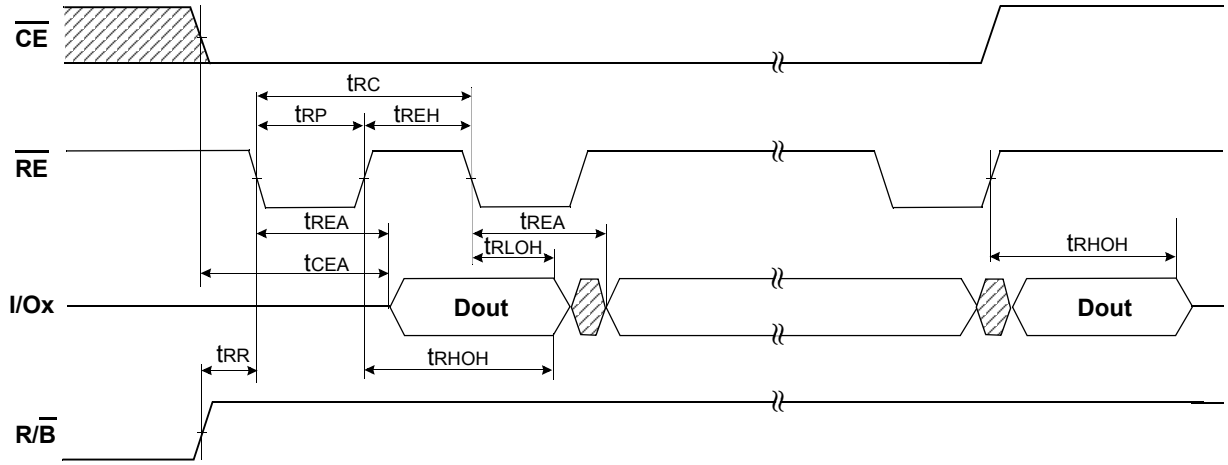
Figure 18. AC Waveforms for Power Transition



Extended Data Out Mode

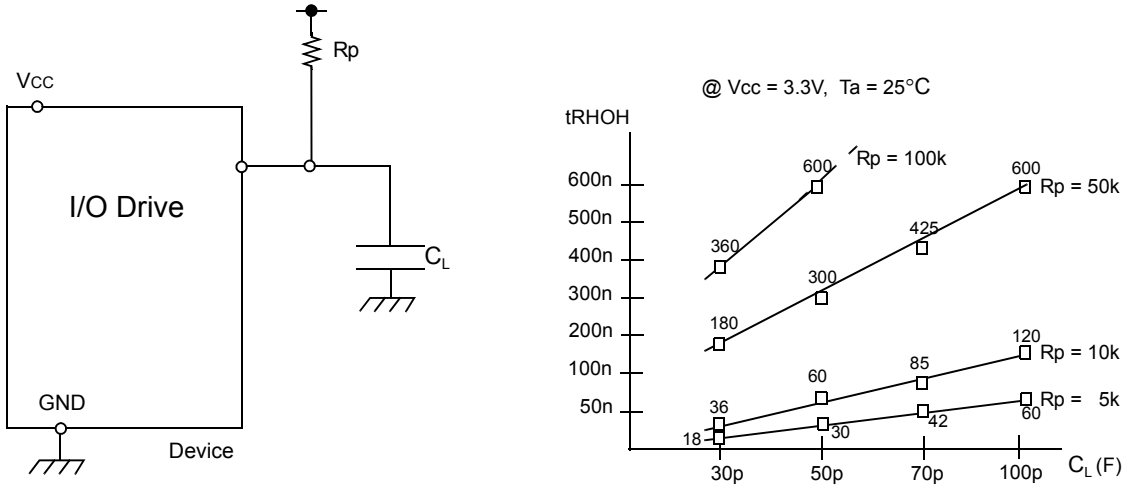
For the EDO mode, the device should hold the data on the system memory bus until the beginning of the next cycle, so that controller could fetch the data at the falling edge. However NAND flash dosen't support the EDO mode exactly.
The device stops the data input into the I/O bus after $\overline{RE}$ rising edge. But since the previous data remains in the I/O bus, the flow of I/O data seems like Figure 18 and the system can access serially the data with EDO mode. tRLOH which is the parameter for fetching data at RE falling time is necessary. Its appropriate value can be obtained with the reference chart as shown in Figure 19. The tRHOH value depands on output load(C_L) and I/O bus Pull-up resistor (Rp).

Figure 19. Serial Access Cycle after Read(EDO Type, CLE=L, $\overline{WE}$=H, ALE=L)



NOTES : Transition is measured at ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.

Figure 20. Rp vs tRHOH vs C_L



tRLOH / tRHOH value guidance

$tRHOH = C_L * V_{OL} * Rp / Vcc$

tRLOH(min, 3.3V part) = tRHOH - tREH

Data Sheet | February 18, 2005 | FN9174.0

High Input Voltage Charger

The ISL6294 is a cost-effective, fully integrated high input voltage single-cell Li-ion battery charger. The charger uses a CC/CV charge profile required by Li-ion batteries. The charger accepts an input voltage up to 28V but is disabled when the input voltage exceeds the OVP threshold, typically 6.8V, to prevent excessive power dissipation. The 28V rating eliminates the overvoltage protection circuit required in a low input voltage charger.

The charge current and the end-of-charge (EOC) current are programmable with external resistors. When the battery voltage is lower than typically 2.55V, the charger preconditions the battery with typically 20% of the programmed charge current. When the charge current reduces to the programmable EOC current level during the CV charge phase, an EOC indication is provided by the CHG pin, which is an open-drain output. An internal thermal foldback function protects the charger from any thermal failure.

Two indication pins (PPR and CHG) allow simple interface to a microprocessor or LEDs. When no adapter is attached or when disabled, the charger draws less than 1µA leakage current from the battery.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6294IRZ (Note)	-40 to 85	8 Ld 2x3 DFN (Pb-free)	L8.2x3
ISL6294IRZ-T (Note)	-40 to 85	8 Ld 2x3 DFN (Pb-free)	L8.2x3

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

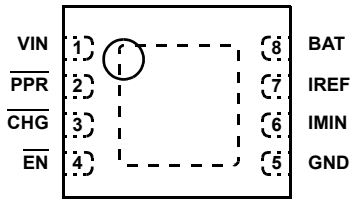
- Complete Charger for Single-Cell Li-ion/Polymer Batteries
- Integrated Pass Element and Current Sensor
- No External Blocking Diode Required
- Low Component Count and Cost
- 1% Voltage Accuracy
- Programmable Charge Current
- **Programmable End-of-Charge Current**
- **Charge Current Thermal Foldback for Thermal Protection**
- Trickle Charge for Fully Discharged Batteries
- **28V Maximum Voltage for the Power Input**
- Power Presence and Charge Indications
- Less Than 1µA Leakage Current off the Battery When No Input Power Attached or Charger Disabled
- Ambient Temperature Range: -40°C to 85°C
- **2x3 DFN-8 Packages**
- Pb-Free Available (RoHS Compliant)

Applications

- Mobile Phones
- Blue-Tooth Devices
- PDAs
- MP3 Players
- Stand-Alone Chargers
- Other Handheld Devices

Pinout

DFN 8 LEAD
TOP VIEW



Absolute Maximum Ratings (Reference to GND)

VIN . . . . . -0.3V to 30V
IMIN, IREF, BAT, CHG, EN, PPR . . . . . -0.3V to 7V
ESD Rating
Human Body Model (Per EIA JESD22 Method A114-B) 3kV
Machine Model (Per EIA JED-4701 Method C-111) 200V

Recommended Operating Conditions

Ambient Temperature Range . . . . . -40°C to 85°C
Maximum Supply Voltage (VIN Pin) 28V
Operating Supply Voltage (VIN Pin) . . . . . 4.5V to 6.5V
Programmed Charge Current . . . . . 100mA to 700mA

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
DFN Package (Notes 1, 2)	78	11

Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
2. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Typical Values Are Tested at VIN = 5V and the Ambient Temperature at 25°C. All Maximum and Minimum Values Are Guaranteed Under the Recommended Operating Supply Voltage Range and Ambient Temperature Range, Unless Otherwise Noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER-ON RESET						
Rising POR Threshold	V_{POR}	VBAT = 3.0V, use PPR to indicate the comparator output.	3.3	3.9	4.3	V
Falling POR Threshold	V_{POR}		3.1	3.6	4.15	V
VIN-BAT OFFSET VOLTAGE						
Rising Edge	V_{OS}	V_{BAT} = 4.0V, use CHG pin to indicate the comparator output (Note 3)	-	90	150	mV
Falling Edge	V_{OS}		10	50	-	mV
OVER VOLTAGE PROTECTION						
Over Voltage Protection Threshold	V_{OVP}	(Note 4) Use PPR to indicate the comparator output	6.5	6.8	7.1	V
OVP Threshold Hysteresis			100	240	400	mV
STANDBY CURRENT						
BAT Pin Sink Current	$I_{STANDBY}$	Charger disabled or the input is floating	-	-	1.0	µA
VIN Pin Supply Current	I_{VIN}	Charger disabled	-	300	400	µA
VIN Pin Supply Current	I_{VIN}	Charger enabled	-	400	600	µA
VOLTAGE REGULATION						
Output Voltage	V_{CH}	4.3V < V_{IN} < 6.5V, charge current = 20mA	4.158	4.20	4.242	V
PMOS On Resistance	$r_{DS(ON)}$	V_{BAT} = 3.8V, charge current = 0.5A	-	0.6	-	Ω
CHARGE CURRENT (Note 5)						
IREF Pin Output Voltage	I_{IREF}	V_{BAT} = 3.8V	1.18	1.22	1.26	V
Constant Charge Current	I_{CHG}	R_{IREF} = 24.3kΩ, V_{BAT} = 2.8V - 4.0V	450	500	550	mA
Trickle Charge Current	I_{TRK}	R_{IREF} = 24.3kΩ, V_{BAT} = 2.4V	70	95	130	mA
End-of-Charge Current	I_{MIN}	R_{IMIN} = 243kΩ	33	45	57	mA
EOC Rising Threshold		R_{IMIN} = 243kΩ	325	380	415	mA
PRECONDITIONING CHARGE THRESHOLD						
Preconditioning Charge Threshold Voltage	V_{MIN}		2.45	2.55	2.65	V
Preconditioning Voltage Hysteresis	V_{MINHYS}		40	100	150	mV

Electrical Specifications Typical Values Are Tested at VIN = 5V and the Ambient Temperature at 25°C. All Maximum and Minimum Values Are Guaranteed Under the Recommended Operating Supply Voltage Range and Ambient Temperature Range, Unless Otherwise Noted. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INTERNAL TEMPERATURE MONITORING						
Charge Current Foldback Threshold (Note 6)	T_{FOLD}		100	115	130	°C
LOGIC INPUT AND OUTPUTS						
EN Pin Logic Input High			1.3	-	-	V
EN Pin Logic Input Low			-	-	0.5	V
EN Pin Internal Pull Down Resistance			100	200	400	kΩ
CHG Sink Current when LOW		Pin Voltage = 1V	10	20	-	mA
CHG Leakage Current When HIGH		V_{CHG} = 6.5V	-	-	1	µA
PPR Sink Current when LOW		Pin Voltage = 1V	10	20	-	mA
PPR Leakage Current When HIGH		V_{PPR} 6= 6.5V	-	-	1	µA

NOTES:

3. The 4.0V V_{BAT} is selected so that the CHG output can be used as the indication for the offset comparator output indication. If the V_{BAT} is lower than the POR threshold, no output pin can be used for indication.
4. For junction temperature below 100 °C.
5. The charge current can be affected by the thermal foldback function if the IC under the test setup cannot dissipate the heat.
6. This parameter is guaranteed by design, not tested.

Pin Descriptions

VIN - Power input. The absolute maximum input voltage is 28V. A 0.47µF or larger value X5R ceramic capacitor is recommended to be placed very close to the input pin for decoupling purpose. Additional capacitance may be required to provide a stable input voltage.

PPR - Open-drain power presence indication. The open-drain MOSFET turns on when the input voltage is above the POR threshold but below the OVP threshold and off otherwise. This pin is capable to sink 10mA (minimum) current to drive an LED. The maximum voltage rating for this pin is 7V. This pin is independent on the EN-pin input.

CHG - Open-drain charge indication pin. This pin outputs a logic LOW when a charge cycle starts and turns to HIGH when the end-of-charge (EOC) condition is qualified. This pin is capable to sink 10mA min. current to drive an LED. When the charger is disabled, the CHG outputs high impedance.

EN - Enable input. This is a logic input pin to disable or enable the charger. Drive to HIGH to disable the charger. When this pin is driven to LOW or left floating, the charger is enabled. This pin has an internal 200kΩ pull-down resistor.

GND - System ground.

IMIN - End-of-charge (EOC) current program pin. Connect a resistor between this pin and the GND pin to set the EOC current. The EOC current IMIN can be programmed by the following equation:

$$I_{MIN} = \frac{11000}{R_{IMIN}} \quad (mA)$$

Where R_{IMIN} is in kΩ. The programmable range covers 5% (or 10mA, whichever is higher) to 50% of IREF. When programmed to less than 5% or 10mA, the stability is not guaranteed.

IREF - Charge-current program and monitoring pin. Connect a resistor between this pin and the GND pin to set the charge current limit determined by the following equation:

$$I_{REF} = \frac{12089}{R_{IREF}} \quad (mA)$$

Where R_{IREF} is in kΩ. The IREF pin voltage also monitors the actual charge current during the entire charge cycle, including the trickle, constant-current, and constant-voltage phases. When disabled, VIREF = 0V.

BAT - Charger output pin. Connect this pin to the battery. A 1µF or larger X5R ceramic capacitor is recommended for decoupling and stability purposes. When the EN pin is pulled to logic HIGH, the BAT output is disabled.

EPAD - Exposed pad. Connect as much as possible copper to this pad either on the component layer or other layers through thermal vias to enhance the thermal performance.

Typical Applications

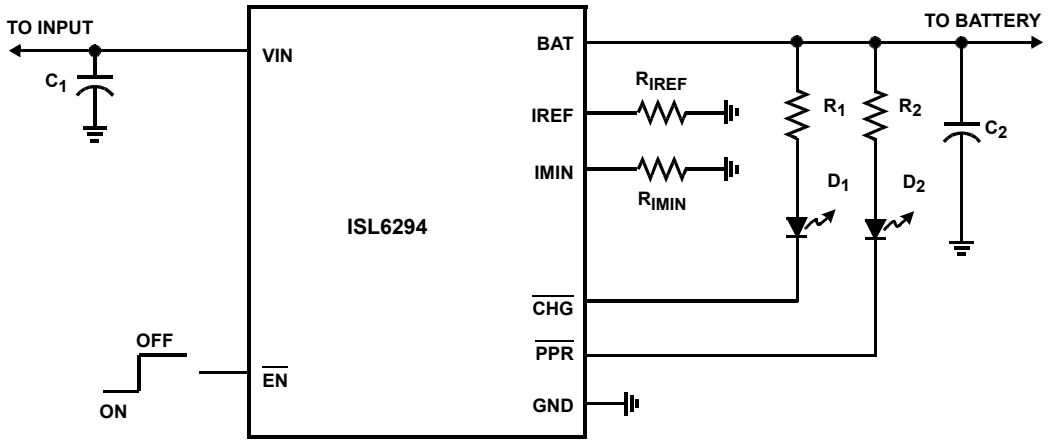


FIGURE 1. TYPICAL APPLICATION CIRCUIT INTERFACING TO INDICATION LEDs

COMPONENT DESCRIPTION FOR FIGURE 1

PART	DESCRIPTION
C_1	1µF X5R ceramic cap
C_2	1µF X5R ceramic cap
R_{IREF}	24.3kΩ, 1%, for 500mA charge current
R_{IMIN}	243kΩ, 1%, for 45mA EOC current
R_1, R_2	300Ω, 5%
D_1, D_2	LEDs for indication

COMPONENT DESCRIPTION FOR FIGURE 2

PART	DESCRIPTION
C_1	1µF X5R ceramic cap
C_2	1µF X5R ceramic cap
R_{IREF}	24.3kΩ, 1%, for 500mA charge current
R_{IMIN}	243kΩ, 1%, for 45mA EOC current
R_1, R_2	100kΩ, 5%

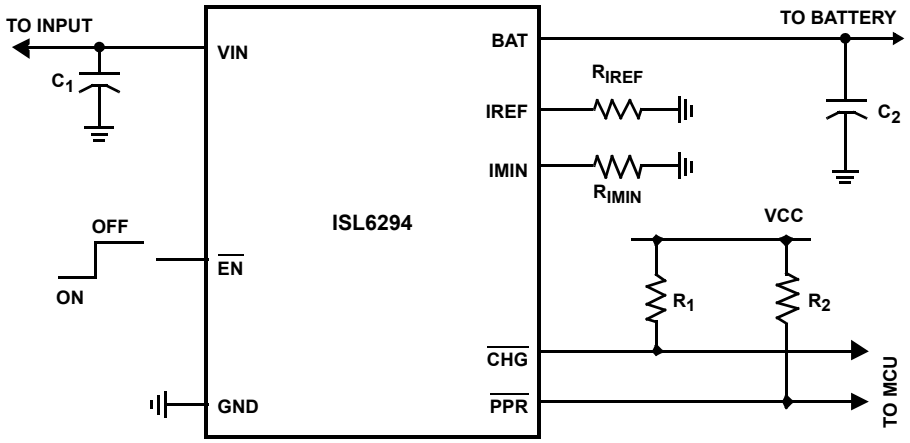


FIGURE 2. TYPICAL APPLICATION CIRCUIT WITH THE INDICATION SIGNALS INTERFACING TO A MCU

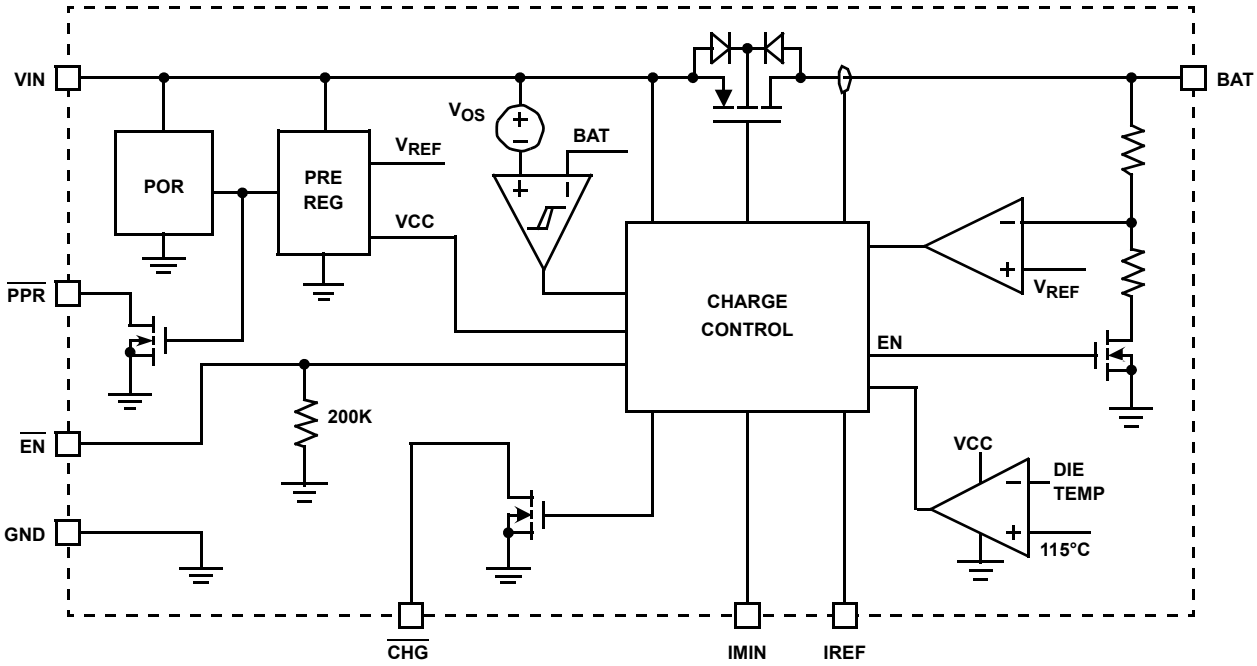


FIGURE 3. BLOCK DIAGRAM

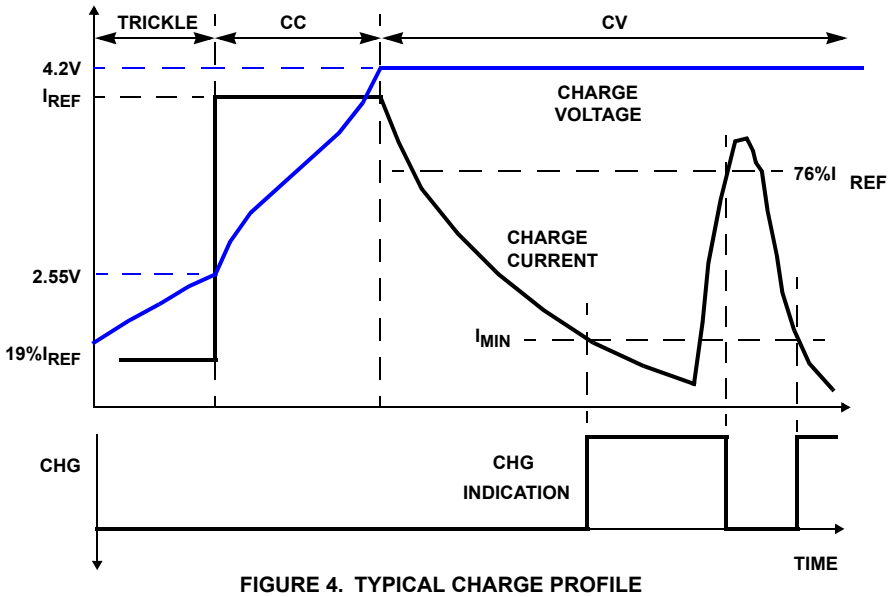


FIGURE 4. TYPICAL CHARGE PROFILE

Description

The ISL6294 charges a Li-ion battery using a CC/CV profile. The constant current I_{REF} is set with the external resistor R_{IREF} (See Figure 1) and the constant voltage is fixed at 4.2V. If the battery voltage is below a typical 2.55V trickle-charge threshold, the ISL6294 charges the battery with a trickle current of 19% of I_{REF} until the battery voltage rises above the trickle charge threshold. Fast charge CC mode is maintained at the rate determined by programming I_{REF} until the cell voltage rises to 4.2V. When the battery voltage reaches 4.2V, the charger enters a CV mode and regulates the battery voltage at 4.2V to fully charge the battery without the risk of over charge. Upon reaching an end-of-charge (EOC) current, the charger indicates the charge completion with the CHG pin, but the charger continues to output the 4.2V voltage. Figure 4 shows the typical charge waveforms after the power is on.

The EOC current level IMIN is programmable with the external resistor R_{IMIN} (See Figure 1). The CHG signal turns

to LOW when the trickle charge starts and rises to HIGH at the EOC. After the EOC is reached, the charge current has to rise to typically 76% I_{REF} for the CHG signal to turn on again, as shown in Figure 4. The current surge after EOC can be caused by a load connected to the battery.

A thermal foldback function reduces the charge current anytime when the die temperature reaches typically 115°C. This function guarantees safe operation when the printed-circuit board (PCB) is not capable of dissipating the heat generated by the linear charger. The ISL6294 accepts an input voltage up to 28V but disables charging when the input voltage exceeds the OVP threshold, typically 6.8V, to protect against unqualified or faulty ac adapters.

PPR Indication

The PPR pin is an open-drain output to indicate the presence of the ac adapter. Whenever the input voltage is higher than the POR threshold, the PPR pin turns on the internal open-drain MOSFET to indicate a logic LOW signal, independent on the EN-pin input. When the internal open-drain FET is turned off, the PPR pin should leak less than 1µA current. When turned on, the PPR pin should be able to sink at least 10mA current under all operating conditions.

The PPR pin can be used to drive an LED (see Figure 1) or to interface with a microprocessor.

Power-Good Range

The power-good range is defined by the following three conditions:

1. VIN > VPOR
2. VIN - VBAT > VOS
3. VIN < VOVP

where the VOS is the offset voltage for the input and output voltage comparator, discussed shortly, and the VOVP is the overvoltage protection threshold given in the Electrical Specification. All V_{POR}, V_{OS}, and V_{OVP} have hysteresis, as given in the Electrical Specification table. The charger will not charge the battery if the input voltage is not in the power-good range.

Input and Output Comparator

The charger will not be enabled unless the input voltage is higher than the battery voltage by an offset voltage VOS. The purpose of this comparator is to ensure that the charger is turned off when the input power is removed from the charger. Without this comparator, it is possible that the charger will fail to power down when the input is removed and the current can leak through the PFET pass element to continue biasing the POR and the Pre-Regulator blocks shown in the Block Diagram.

CHG Indication

The CHG is an open-drain output capable to at least 10mA current when the charger starts to charge and turns off when the EOC current is reached. The CHG signal is interfaced either with a micro-processor GPIO or an LED for indication.

EN Input

EN is an active-low logic input to enable the charger. Drive the EN pin to LOW or leave it floating to enable the charger. This pin has a 200kΩ internal pulldown resistor so when left floating, the input is equivalent to logic LOW. Drive this pin to HIGH to disable the charger. The threshold for HIGH is given in the ES (Electrical Specification) table.

IREF Pin

The IREF pin has the two functions as described in the Pin Description section. When setting the fast charge current, the charge current is guaranteed to have 10% accuracy with the charge current set at 500mA. When monitoring the charge current, the accuracy of the IREF pin voltage vs. the actual charge current has the same accuracy as the gain from the IREF pin current to the actual charge current. The accuracy is 10% at 500mA and is expected to drop to 30% of the actual current (not the set constant charge current) when the current drops to 50mA.

Operation Without the Battery

The ISL6294 relies on a battery for stability and is not guaranteed to be stable if the battery is not connected. With a battery, the charger will be stable with an output ceramic decoupling capacitor in the range of 1µF to 200µF. The maximum load current is limited by the dropout voltage or the thermal foldback.

Dropout Voltage

The constant current may not be maintained due to the $r_{DS(ON)}$ limit at a low input voltage. The worst case on resistance of the pass FET is 1.2Ω the maximum operating temperature, thus if tested with 0.5A current and 3.8V battery voltage, constant current could not be maintained when the input voltage is below 4.4V.

Thermal Foldback

The thermal foldback function starts to reduce the charge current when the internal temperature reaches a typical value of 115°C.

Applications Information

Input Capacitor Selection

The input capacitor is required to suppress the power supply transient response during transitions. Mainly this capacitor is selected to avoid oscillation during the start up when the input supply is passing the POR threshold and the VIN-BAT comparator offset voltage. When the battery voltage is above the POR threshold, the VIN-VBAT offset voltage dominates the hysteresis value. Typically, a 1µF X5R ceramic capacitor should be sufficient to suppress the power supply noise.

Output Capacitor Selection

The criteria for selecting the output capacitor is to maintain the stability of the charger as well as to bypass any transient load current. The minimum capacitance is a 1µF X5R ceramic capacitor. The actual capacitance connected to the output is dependent on the actual application requirement.

Charge Current Limit

The actual charge current in the CC mode is limited by several factors in addition to the set I_{REF}. Figure 5 shows three limits for the charge current in the CC mode. The charge current is limited by the on resistance of the pass element (power P-channel MOSFET) if the input and the output voltage are too close to each other. The solid curve shows a typical case when the battery voltage is 4.0V and the charge current is set to 700mA. The non-linearity on the R_{ON}-limited region is due to the increased resistance at higher die temperature. If the battery voltage increases to higher than 4.0V, the entire curve moves towards right side. As the input voltage increases, the charge current may be reduced due to the thermal foldback function. The limit caused by the thermal limit is dependent on the thermal impedance. As the thermal impedance increases, the thermal-limited curve moves towards left, as shown in Figure 5.

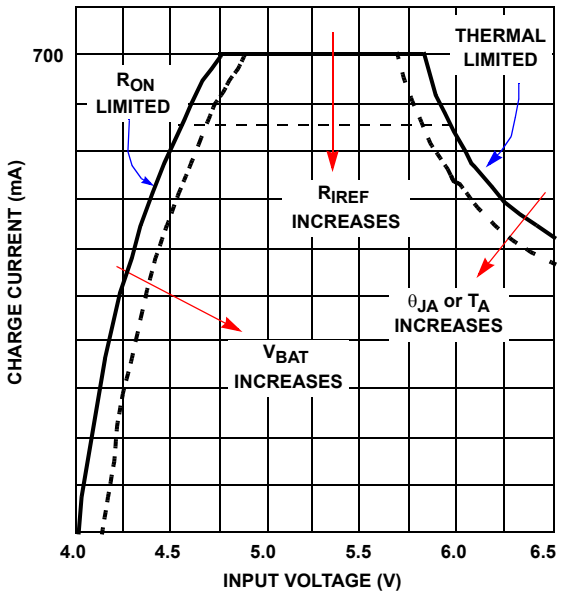


FIGURE 5. CHARGE CURRENT LIMITS IN THE CC MODE

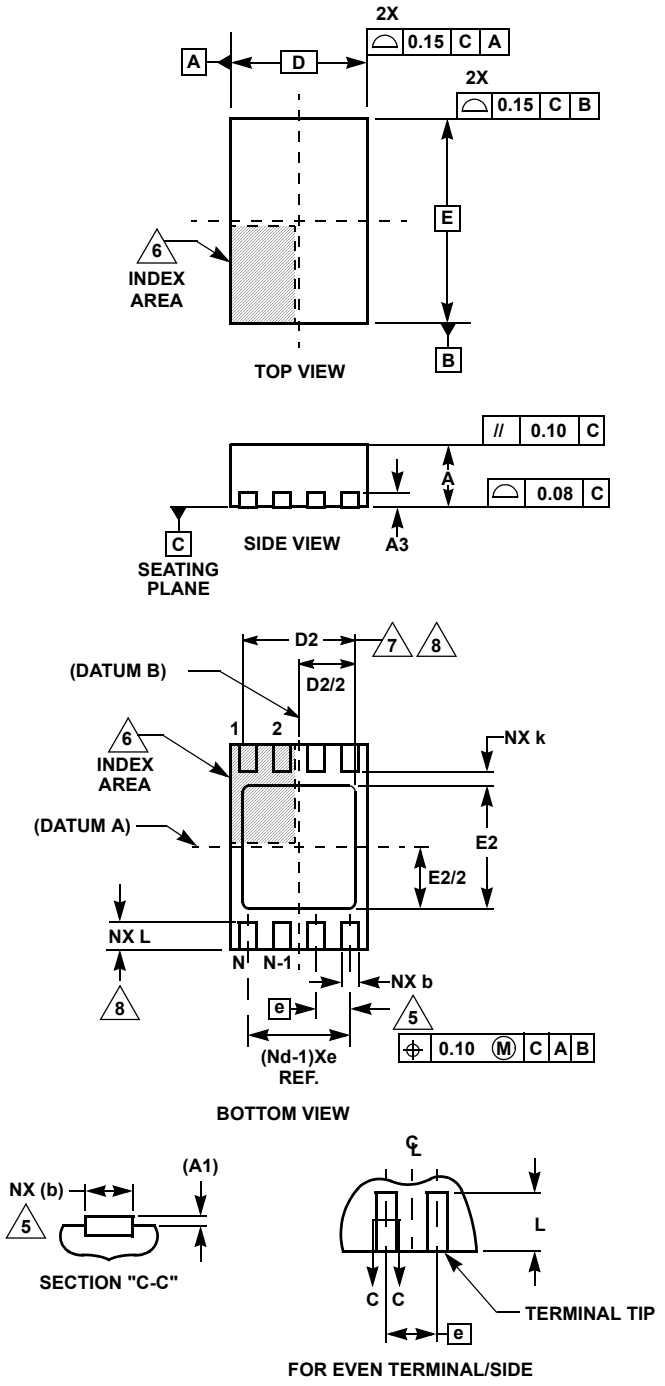
Layout Guidance

The ISL6294 uses a thermally-enhanced DFN package that has an exposed thermal pad at the bottom side of the package. The layout should connect as much as possible to copper on the exposed pad. Typically the component layer is more effective in dissipating heat. The thermal impedance can be further reduced by using other layers of copper connecting to the exposed pad through a thermal via array. Each thermal via is recommended to have 0.3mm diameter and 1mm distance from other thermal vias.

Input Power Sources

The input power source is typically a well-regulated wall cube with 1-meter length wire or a USB port. The input voltage ranges from 4.25V to 6.5V under full-load and unloaded conditions. The ISL6294 can withstand up to 28V on the input without damaging the IC. If the input voltage is higher than typically 6.8V, the charger stops charging.

Dual Flat No-Lead Plastic Package (DFN)



L8.2x3

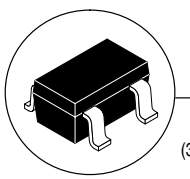
8 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

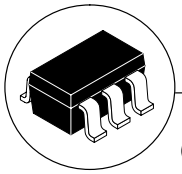
SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.20	0.25	0.32	5,8
D		2.00 BSC		-
D2	1.50	1.65	1.75	7,8
E		3.00 BSC		-
E2	1.65	1.80	1.90	7,8
e		0.50 BSC		-
k	0.20	-	-	-
L	0.30	0.40	0.50	8
N		8		2
Nd		4		3

Rev. 0 6/04

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.25mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.





SLVS348C – JULY 2001 – REVISED APRIL 2002

ULTRALOW-NOISE, HIGH PSRR, FAST RF 200-mA LOW-DROPOUT LINEAR REGULATORS

FEATURES

- **200-mA Low-Dropout Regulator With EN**
- **Available in 1.8-V, 2.5-V, 2.8-V, 2.85-V, 3-V, 3.3-V, 4.75-V, and Adjustable**
- **High PSRR (70 dB at 10 kHz)**
- **Ultralow Noise (32 μV)**
- **Fast Start-Up Time (50 μs)**
- **Stable With a 2.2-μF Ceramic Capacitor**
- **Excellent Load/Line Transient**
- **Very Low Dropout Voltage (112 mV at Full Load, TPS79330)**
- **5-Pin SOT23 (DBV) Package**

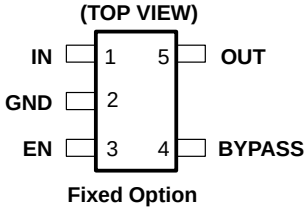
APPLICATIONS

- **Cellular and Cordless Telephones**
- **VCOs**
- **RF**
- **Bluetooth™, Wireless LAN**
- **Handheld Organizers, PDA**

DESCRIPTION

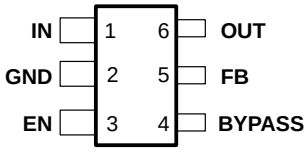
The TPS793xx family of low-dropout (LDO) low-power linear voltage regulators features high power supply rejection ratio (PSRR), ultralow noise, fast start-up, and excellent line and load transient responses in a small outline, SOT23, package. Each device in the family is stable, with a small 2.2-μF ceramic capacitor on the output. The TPS793xx family uses an advanced, proprietary BiCMOS fabrication process to yield extremely low dropout voltages (e.g., 112 mV at 200 mA, TPS79330). Each device achieves fast start-up times (approximately 50 μs with a 0.001-μF bypass capacitor) while consuming very low quiescent current (170 μA typical). Moreover, when the device is placed in standby mode, the supply current is reduced to less than 1 μA. The TPS79328 exhibits approximately 32 μV_{RMS} of output voltage noise with a 0.1-μF bypass capacitor. Applications with analog components that are noise sensitive, such as portable RF electronics, benefit from the high PSRR and low-noise features as well as the fast response time.

DBV PACKAGE
(TOP VIEW)



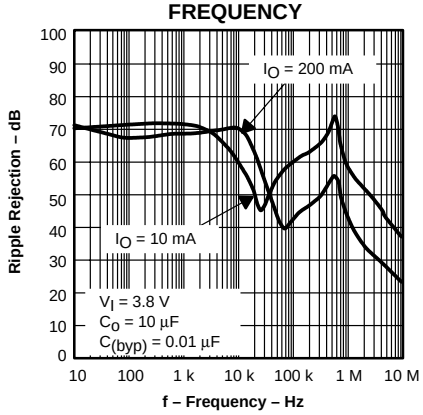
Fixed Option

DBV PACKAGE
(TOP VIEW)

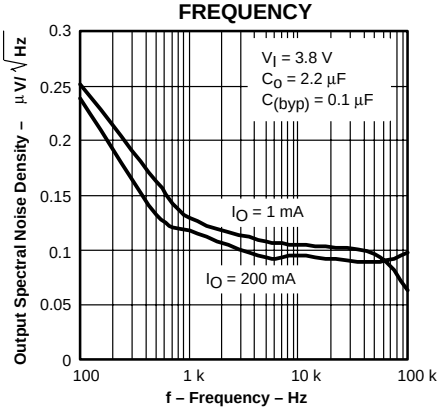


Adjustable Option

TPS79328
RIPPLE REJECTION
vs
FREQUENCY



TPS79328
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Bluetooth is a trademark owned by Bluetooth SIG, Inc.

AVAILABLE OPTIONS

T_J	VOLTAGE	PACKAGE	PART NUMBER	SYMBOL
–40°C to 125°C	1.2 to 5.5 V	SOT23 (DBV)	TPS79301DBVR†	PGVI
	1.8 V		TPS79318DBVR†	PHHI
	2.5 V		TPS79325DBVR†	PGWI
	2.8 V		TPS79328DBVR†	PGXI
	2.85 V		TPS793285DBVR†	PHII
	3 V		TPS79330DBVR†	PGYI
	3.3 V		TPS793333DBVR†	PHUI
	4.75 V		TPS793475DBVR†	PHJI

† The DBVR indicates tape and reel of 3000 parts.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Input voltage range (see Note 1) . . . . . –0.3 V to 6 V
Voltage range at EN . . . . . –0.3 V to V_I + 0.3 V
Voltage on OUT . . . . . –0.3 V to 6 V
Peak output current . . . . . internally limited
ESD rating, HBM . . . . . 2 kV
ESD rating, CDM . . . . . 500 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating virtual junction temperature range, T_J . . . . . –40°C to 150°C
Operating ambient temperature range, T_A . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

BOARD	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = 25°C	$T_A \le 25°C$ POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
Low K§	DBV	63.75 °C/W	256 °C/W	3.906 mW/°C	391 mW	215 mW	156 mW
High K¶	DBV	63.75 °C/W	178.3 °C/W	5.609 mW/°C	561 mW	308 mW	224 mW

§ The JEDEC low K (1s) board design used to derive this data was a 3-inch x 3-inch, two layer board with 2 ounce copper traces on top of the board.
¶ The JEDEC high K (2s2p) board design used to derive this data was a 3-inch x 3-inch, multilayer board with 1 ounce internal power and ground planes and 2 ounce copper traces on top and bottom of the board.

electrical characteristics over recommended operating free-air temperature range EN = V_I, T_J = –40 to 125 °C, V_I = $V_{O(typ)}$ + 1 V, I_O = 1 mA, C_o = 10 µF, $C_{(byp)}$ = 0.01 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_I Input voltage (see Note 2)				2.7		5.5	V
I_O Continuous output current (see Note 3)				0		200	mA
T_J Operating junction temperature				–40		125	°C
Output voltage	TPS79301	0 µA< I_O < 200 mA, (see Note 4)	1.22 V ≤ V_O ≤ 5.2 V,	0.98 V_O		1.02 V_O	V
	TPS79318	T_J = 25°C			1.8		V
		0 µA< I_O < 200 mA,	2.8 V < V_I < 5.5 V	1.764		1.836	
	TPS79325	T_J = 25°C			2.5		V
		0 µA< I_O < 200 mA,	3.5 V < V_I < 5.5 V	2.45		2.55	
	TPS79328	T_J = 25°C			2.8		V
		0 µA< I_O < 200 mA,	3.8 V < V_I < 5.5 V	2.744		2.856	
	TPS793285	T_J = 25°C			2.85		V
		0 µA< I_O < 200 mA,	3.85 V < V_I < 5.5 V	2.793		2.907	
	TPS79330	T_J = 25°C			3		V
		0 µA< I_O < 200 mA,	4 V < V_I < 5.5 V	2.94		3.06	
	TPS79333	T_J = 25°C			3.3		V
		0 µA ≤ I_O < 200 mA,	4.3 V < V_I < 5.5 V	3.234		3.366	
	TPS793475	T_J = 25°C			4.75		V
		0 µA< I_O < 200 mA,	5.25 V < V_I < 5.5 V	4.655		4.845	
Quiescent current (GND current)		0 µA< I_O < 200 mA,	T_J = 25°C		170		µA
		0 µA< I_O < 200 mA				220	µA
Load regulation		0 µA< I_O < 200 mA,	T_J = 25°C		5		mV
Output voltage line regulation ($\Delta V_O/V_O$) (see Note 5)		V_O + 1 V < V_I ≤ 5.5 V,	T_J = 25°C		0.05		%/V
		V_O + 1 V < V_I ≤ 5.5 V				0.12	
Output noise voltage (TPS79328)		BW = 200 Hz to 100 kHz, I_O = 200 mA, T_J = 25°C	$C_{(byp)}$ = 0.001 µF		55		μV_{RMS}
			$C_{(byp)}$ = 0.0047 µF		36		
			$C_{(byp)}$ = 0.01 µF		33		
			$C_{(byp)}$ = 0.1 µF		32		
Time, start-up (TPS79328)		R_L = 14 Ω, C_o = 1 µF, T_J = 25°C	$C_{(byp)}$ = 0.001 µF		50		µs
			$C_{(byp)}$ = 0.0047 µF		70		
			$C_{(byp)}$ = 0.01 µF		100		
Output current limit		V_O = 0 V,	See Note 4	285		600	mA
Standby current		EN = 0 V,	2.7 V < V_I < 5.5 V		0.07	1	µA
High level enable input voltage		2.7 V < V_I < 5.5 V		2			V
Low level enable input voltage		2.7 V < V_I < 5.5 V				0.7	V
Input current (EN)		EN = 0		–1		1	µA
Input current (FB) (TPS79301)		FB = 1.8 V				1	µA

NOTES: 2. To calculate the minimum input voltage for your maximum output current, use the following formula:
$V_I(min) = V_O(max) + V_{DO}$ (max load)

3. Continuous output current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

4. The minimum IN operating voltage is 2.7 V or $V_{O(typ)}$ + 1 V, whichever is greater. The maximum IN voltage is 5.5 V. The maximum output current is 200 mA.

5. If V_O ≤ 2.5 V then V_{Imin} = 2.7 V, V_{Imax} = 5.5 V:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O\left(V_{Imax} - 2.7\ V\right)}{100} \times 1000$$

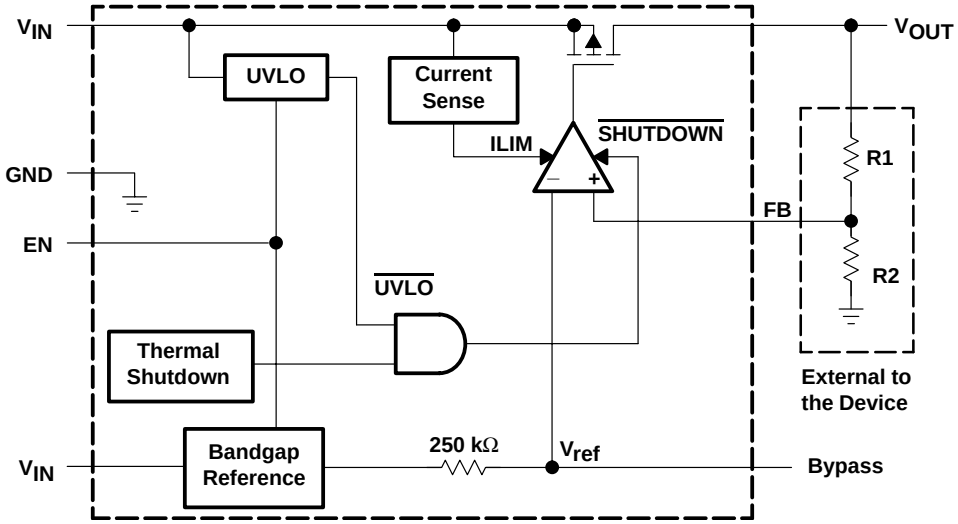
If V_O ≥ 2.5 V then $V_{Imin} = V_O$ + 1 V, V_{Imax} = 5.5 V.

electrical characteristics over recommended operating free-air temperature range EN = V_I, T_J = –40 to 125 °C, V_I = $V_{O(typ)}$ + 1 V, I_O = 1 mA, C_o = 10 μF, $C_{(byp)}$ = 0.01 μF (unless otherwise noted) (continued)

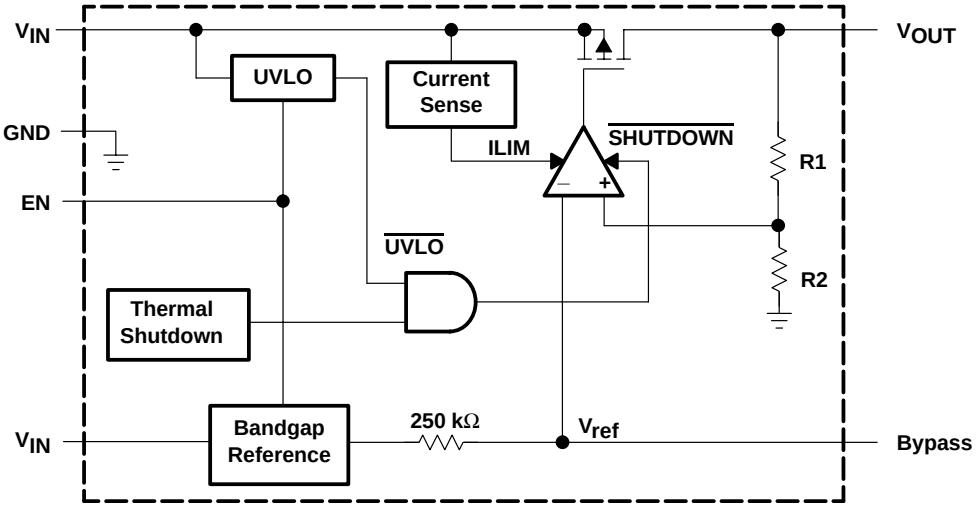
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Power supply ripple rejection	TPS79328	f = 100 Hz, T_J = 25°C,	I_O = 10 mA		70		dB
		f = 100 Hz, T_J = 25°C,	I_O = 200 mA		68		
		f = 10 kHz, T_J = 25°C,	I_O = 200 mA		70		
		f = 100 kHz, T_J = 25°C,	I_O = 200 mA		43		
Dropout voltage (see Note 6)	TPS79328	I_O = 200 mA,	T_J = 25°C		120		mV
		I_O = 200 mA				200	
	TPS793285	I_O = 200 mA,	T_J = 25°C		120		
		I_O = 200 mA				200	
	TPS79330	I_O = 200 mA,	T_J = 25°C		112		
		I_O = 200 mA				200	
	TPS79333	I_O = 200 mA,	T_J = 25°C		102		mV
		I_O = 200 mA				180	
	TPS793475	I_O = 200 mA,	T_J = 25°C		77		mV
		I_O = 200 mA				125	
UVLO threshold		V_{CC} rising		2.25		2.65	V
UVLO hysteresis		T_J = 25°C	V_{CC} rising		100		mV

NOTE 6: IN voltage equals V_O(typ) – 100 mV; The TPS79325 dropout voltage is limited by the input voltage range limitations.

functional block diagram—adjustable version



functional block diagram—fixed version



Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	ADJ	FIXED		
BYPASS	4	4		An external bypass capacitor, connected to this terminal, in conjunction with an internal resistor, creates a low-pass filter to further reduce regulator noise.
EN	3	3	I	The EN terminal is an input which enables or shuts down the device. When EN goes to a logic high, the device will be enabled. When the device goes to a logic low, the device is in shutdown mode.
FB	5	N/A	I	This terminal is the feedback input voltage for the adjustable device.
GND	2	2		Regulator ground
IN	1	1	I	The IN terminal is the input to the device.
OUT	6	5	O	The OUT terminal is the regulated output of the device.

TYPICAL CHARACTERISTICS

TPS79328
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

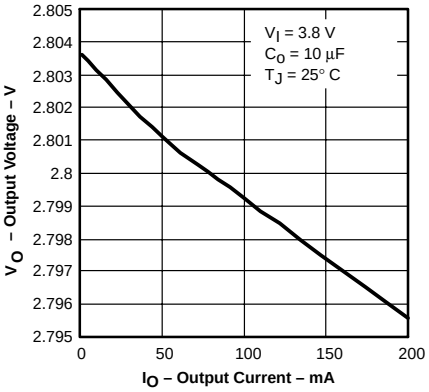


Figure 1

TPS79328
OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

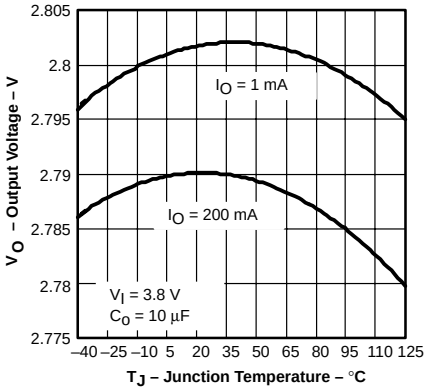


Figure 2

TPS79328
GROUND CURRENT
vs
JUNCTION TEMPERATURE

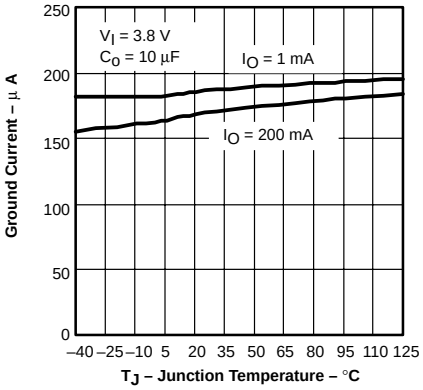


Figure 3

TPS79328
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

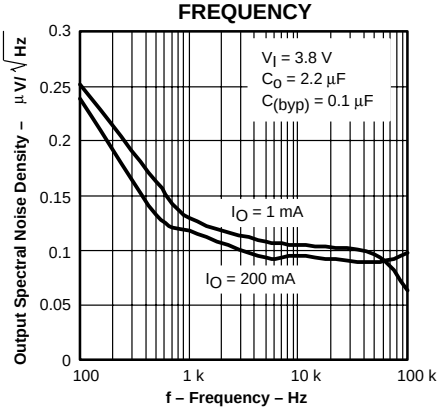


Figure 4

TPS79328
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

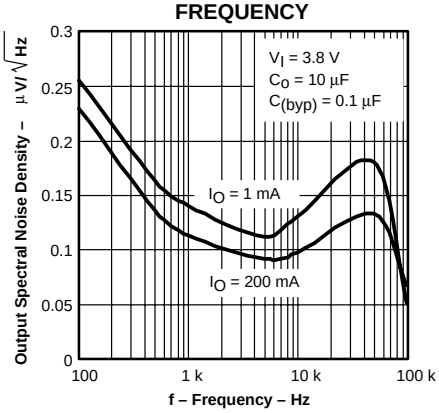


Figure 5

TPS79328
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

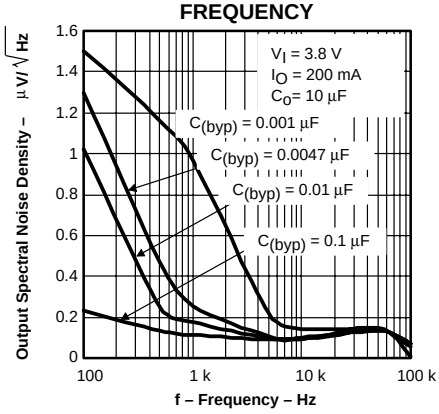


Figure 6

ROOT MEAN SQUARED OUTPUT NOISE
vs
BYPASS CAPACITANCE

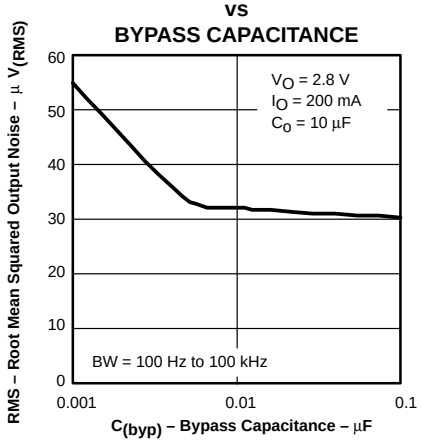


Figure 7

OUTPUT IMPEDANCE
vs
FREQUENCY

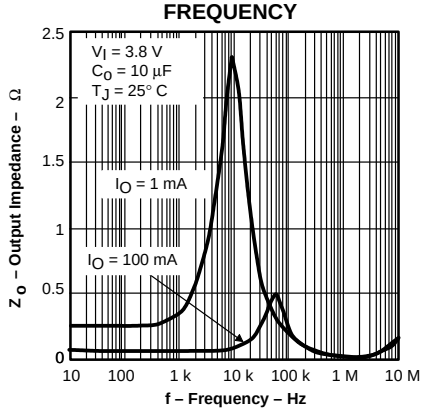


Figure 8

TPS79328
DROPOUT VOLTAGE
vs
JUNCTION TEMPERATURE

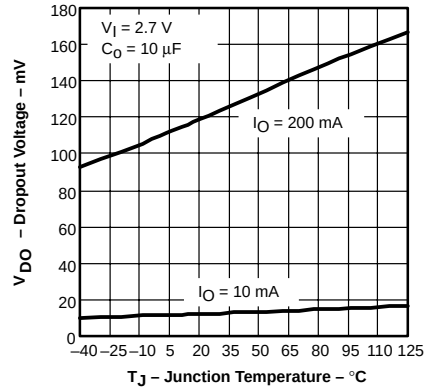


Figure 9

TYPICAL CHARACTERISTICS

TPS79328
RIPPLE REJECTION vs FREQUENCY

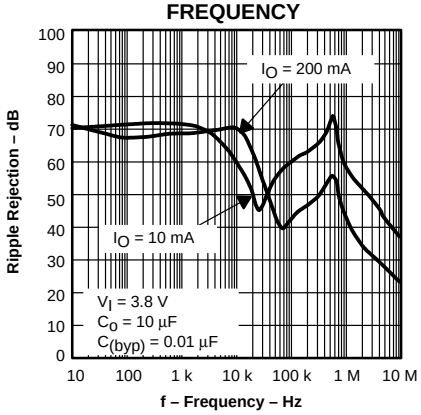


Figure 10

TPS79328
RIPPLE REJECTION vs FREQUENCY

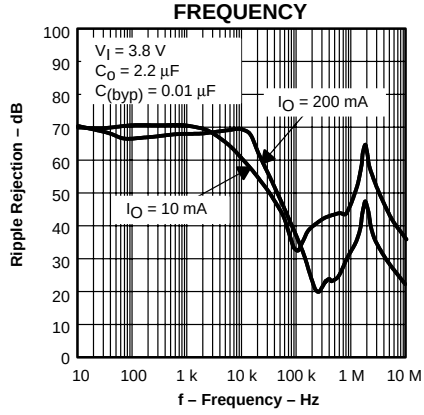


Figure 11

TPS79328
RIPPLE REJECTION vs FREQUENCY

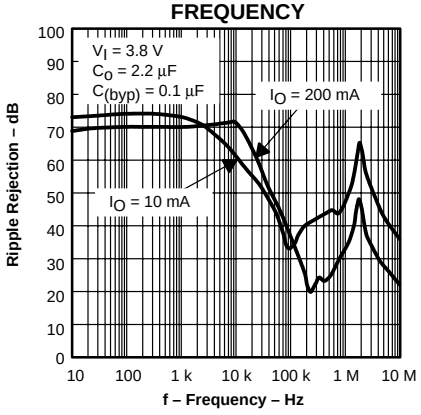


Figure 12

TPS79328
OUTPUT VOLTAGE, ENABLE VOLTAGE vs TIME (START-UP)

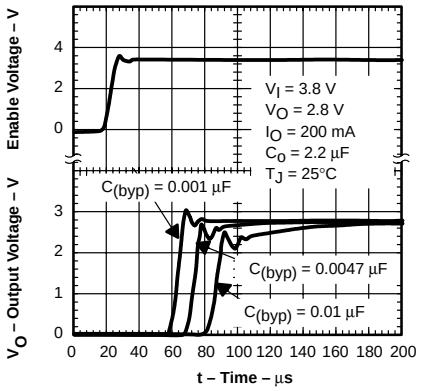


Figure 13

TPS79328
LINE TRANSIENT RESPONSE

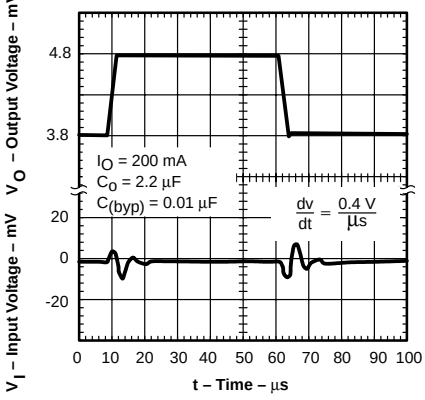


Figure 14

TPS79328
LOAD TRANSIENT RESPONSE

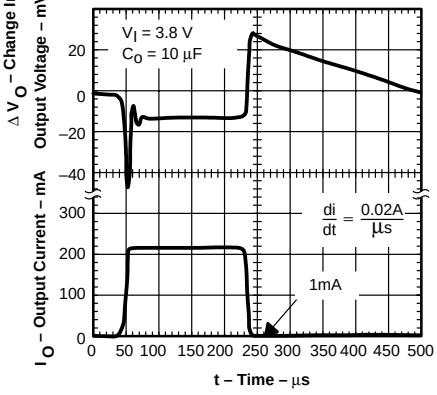


Figure 15

POWER UP / POWER DOWN

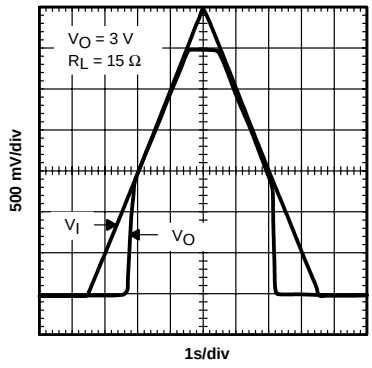


Figure 16

DC DROPOUT VOLTAGE vs OUTPUT CURRENT

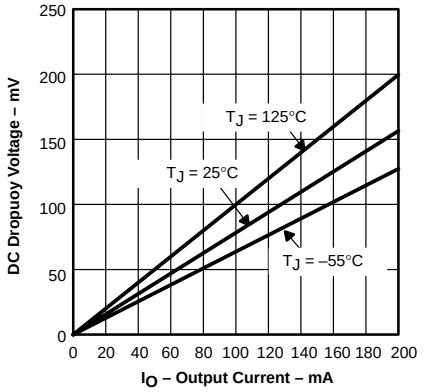


Figure 17

TPS79301
DROPOUT VOLTAGE vs INPUT VOLTAGE

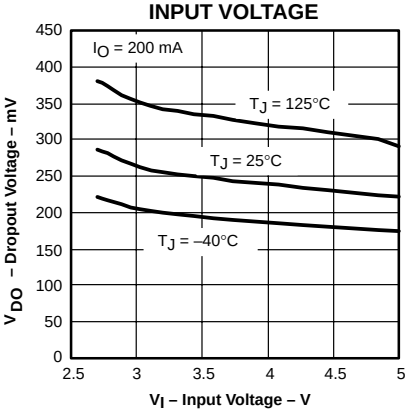


Figure 18

TYPICAL CHARACTERISTICS

MINIMUM REQUIRED INPUT VOLTAGE vs OUTPUT VOLTAGE

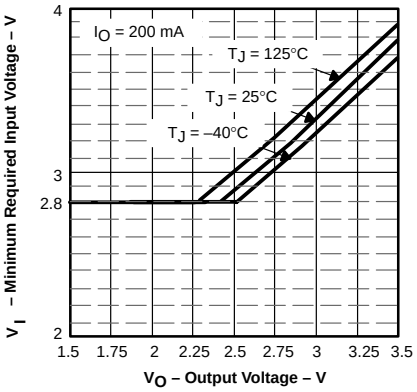


Figure 19

TYPICAL REGIONS OF STABILITY EQUIVALENT SERIES RESISTANCE (ESR) vs OUTPUT CURRENT

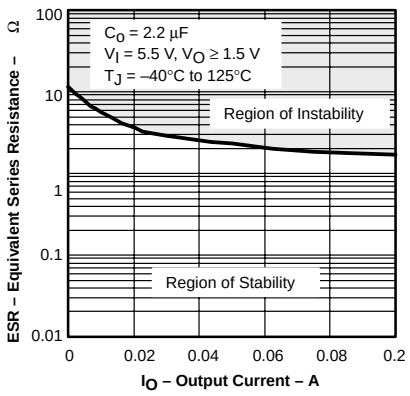


Figure 20

TYPICAL REGIONS OF STABILITY EQUIVALENT SERIES RESISTANCE (ESR) vs OUTPUT CURRENT

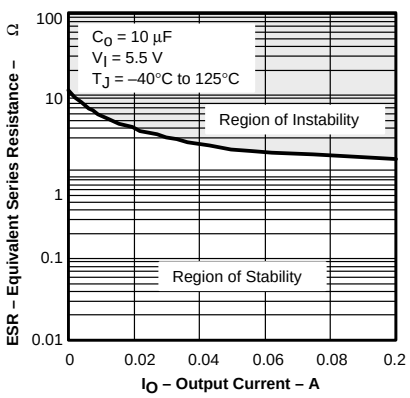


Figure 21

APPLICATION INFORMATION

The TPS793xx family of low-dropout (LDO) regulators has been optimized for use in noise-sensitive battery-operated equipment. The device features extremely low dropout voltages, high PSRR, ultralow output noise, low quiescent current (170 μA typically), and enable-input to reduce supply currents to less than 1 μA when the regulator is turned off.

A typical application circuit is shown in Figure 22.

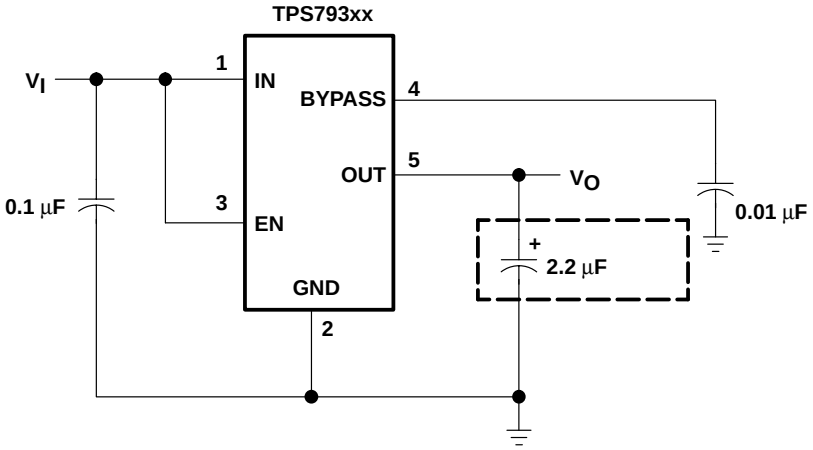


Figure 22. Typical Application Circuit

external capacitor requirements

A 0.1-μF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS793xx, is required for stability and will improve transient response, noise rejection, and ripple rejection. A higher-value electrolytic input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like all low dropout regulators, the TPS793xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 2.2 μF. Any 2.2 μF or larger ceramic capacitor is suitable, provided the capacitance does not vary significantly over temperature.

The internal voltage reference is a key source of noise in an LDO regulator. The TPS793xx has a BYPASS pin which is connected to the voltage reference through a 250-kΩ internal resistor. The 250-kΩ internal resistor, in conjunction with an external bypass capacitor connected to the BYPASS pin, creates a low pass filter to reduce the voltage reference noise and, therefore, the noise at the regulator output. In order for the regulator to operate properly, the current flow out of the BYPASS pin must be at a minimum, because any leakage current will create an IR drop across the internal resistor thus creating an output error. Therefore, the bypass capacitor must have minimal leakage current.

For example, the TPS79328 exhibits only 32 μV_{RMS} of output voltage noise using a 0.1-μF ceramic bypass capacitor and a 2.2-μF ceramic output capacitor. Note that the output starts up slower as the bypass capacitance increases due to the RC time constant at the BYPASS pin that is created by the internal 250-kΩ resistor and external capacitor.

APPLICATION INFORMATION

board layout recommendation to improve PSRR and noise performance

To improve ac measurements like PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}} \quad (1)$$

Where:

$T_J max$ is the maximum allowable junction temperature.

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, see the dissipation rating table.

T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = \left(V_I - V_O\right) \times I_O \quad (2)$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

programming the TPS79301 adjustable LDO regulator

The output voltage of the TPS79301 adjustable regulator is programmed using an external resistor divider as shown in Figure 23. The output voltage is calculated using:

$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \quad (3)$$

Where:

V_{ref} = 1.2246 V typ (the internal reference voltage)

APPLICATION INFORMATION

programming the TPS79301 adjustable LDO regulator (continued)

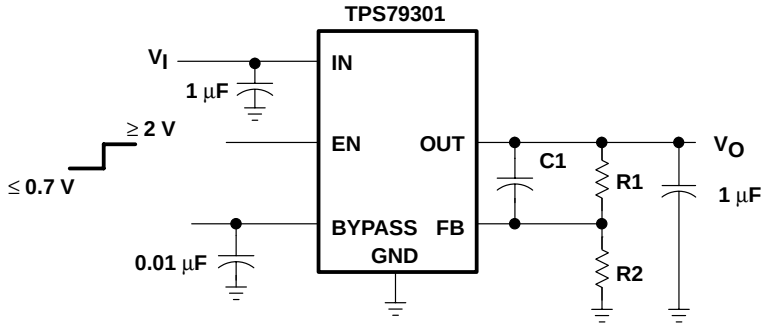
Resistors R1 and R2 should be chosen for approximately 50-μA divider current. Lower value resistors can be used for improved noise performance, but the solution consumes more power. Higher resistor values should be avoided as leakage current into/out of FB across R1/R2 creates an offset voltage that artificially increases/decreases the feedback voltage and thus erroneously decreases/increases V_O. The recommended design procedure is to choose R2 = 30.1 kΩ to set the divider current at 50 μA, C1 = 15 pF for stability, and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \quad (4)$$

In order to improve the stability of the adjustable version, it is suggested that a small compensation capacitor be placed between OUT and FB. For voltages <1.8 V, the value of this capacitor should be 100 pF. For voltages >1.8 V, the approximate value of this capacitor can be calculated as:

$$C1 = \frac{(3 \times 10^{-7}) \times (R1 + R2)}{(R1 \times R2)} \quad (5)$$

The suggested value of this capacitor for several resistor ratios is shown in the table below. If this capacitor is not used (such as in a unity-gain configuration) or if an output voltage <1.8 V is chosen, then the minimum recommended output capacitor is 4.7 μF instead of 2.2 μF.



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	C1
2.5 V	33.4 kΩ	30.1 kΩ	22 pF
3.3 V	53.6 kΩ	30.1 kΩ	15 pF
3.6 V	59 kΩ	30.1 kΩ	15 pF

Figure 23. TPS79301 Adjustable LDO Regulator Programming

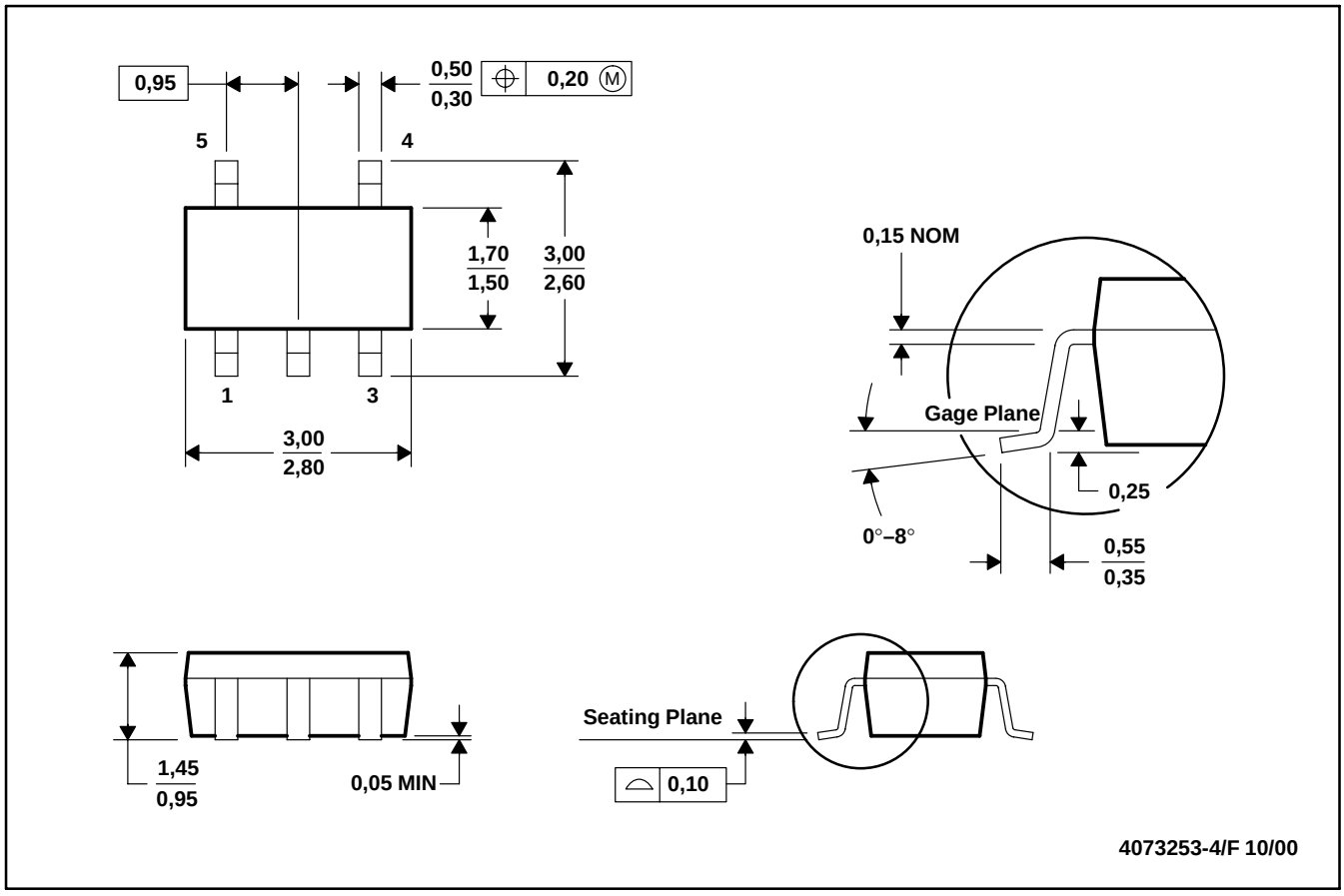
regulator protection

The TPS793xx PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS793xx features internal current limiting and thermal protection. During normal operation, the TPS793xx limits output current to approximately 400 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package or the absolute maximum voltage ratings of the device. If the temperature of the device exceeds approximately 165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below approximately 140°C, regulator operation resumes.

MECHANICAL DATA

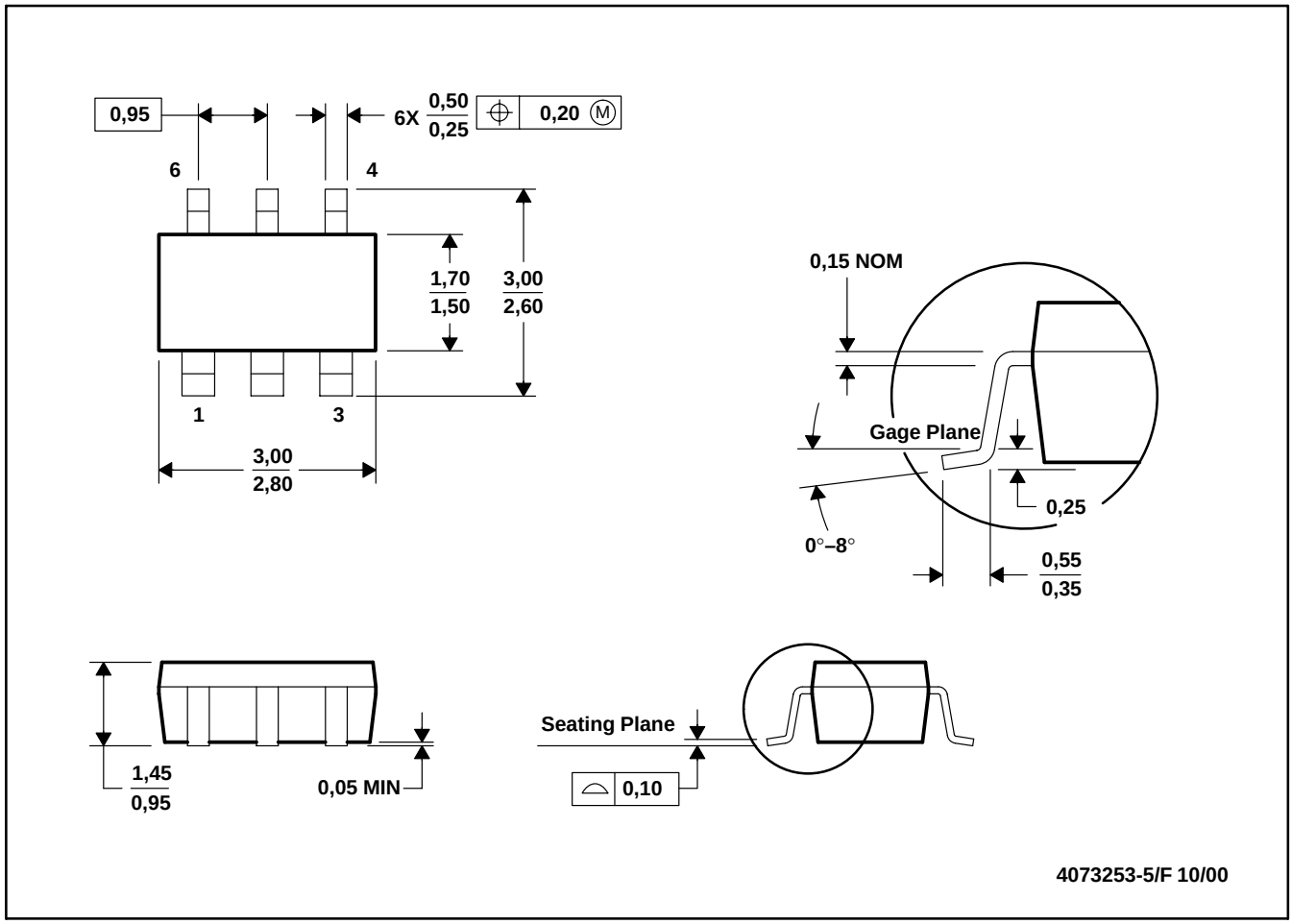
DBV (R-PDSO-G5) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-178

MECHANICAL DATA

DBV (R-PDSO-G6) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Leads 1, 2, 3 are wider than leads 4, 5, 6 for package orientation.
E. Pin 1 is located below the first letter of the top side symbolization.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

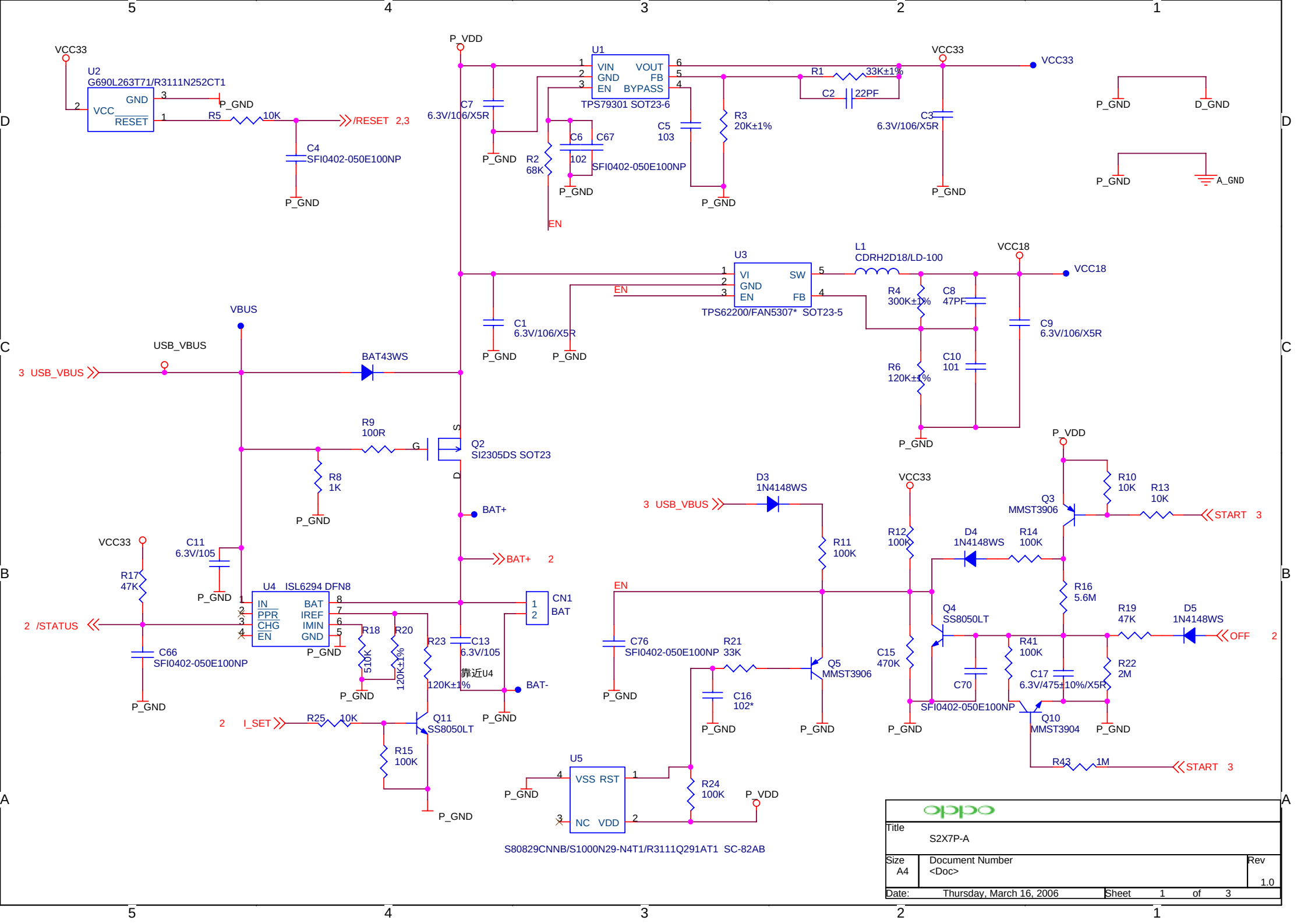
TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third–party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

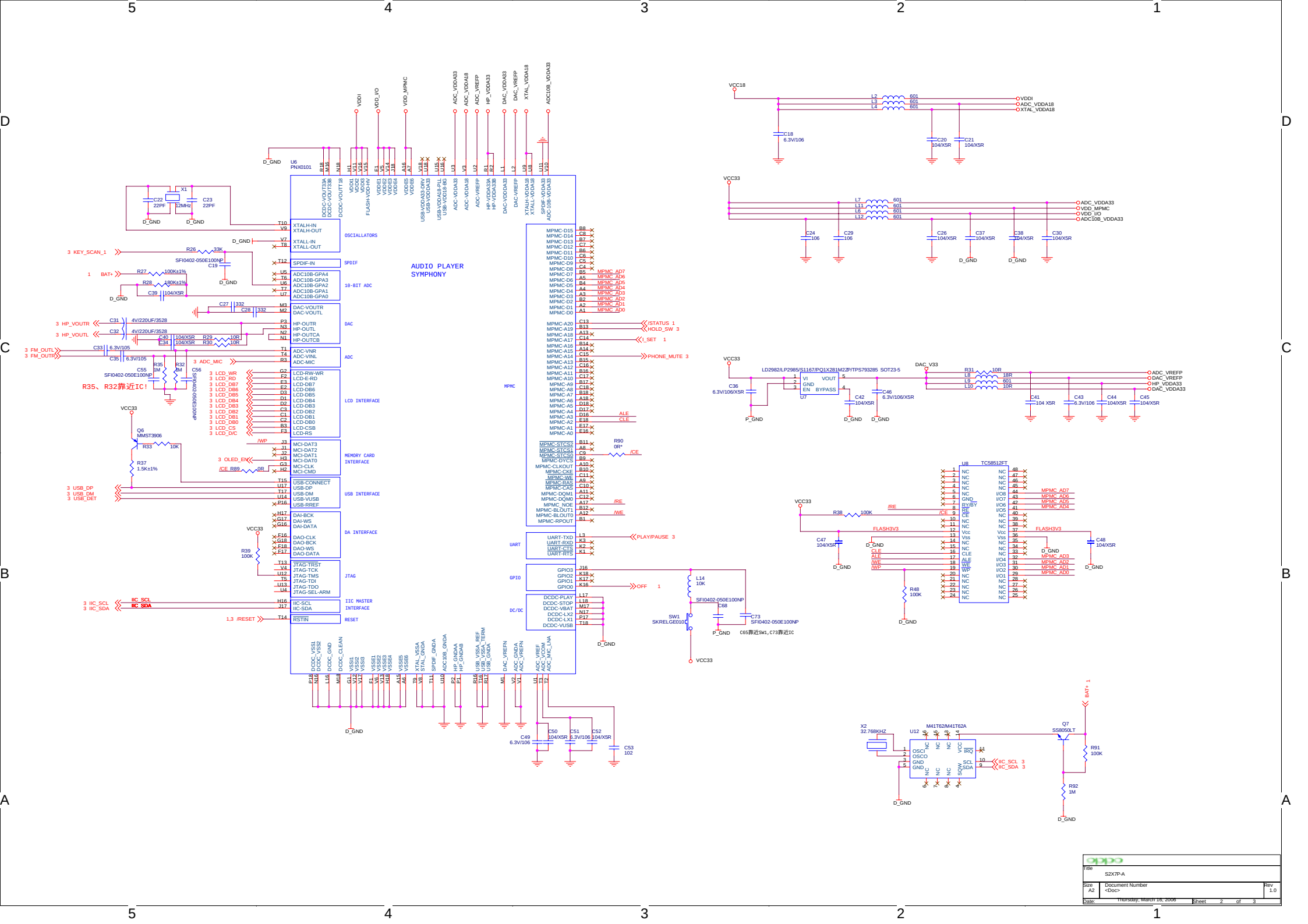
Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

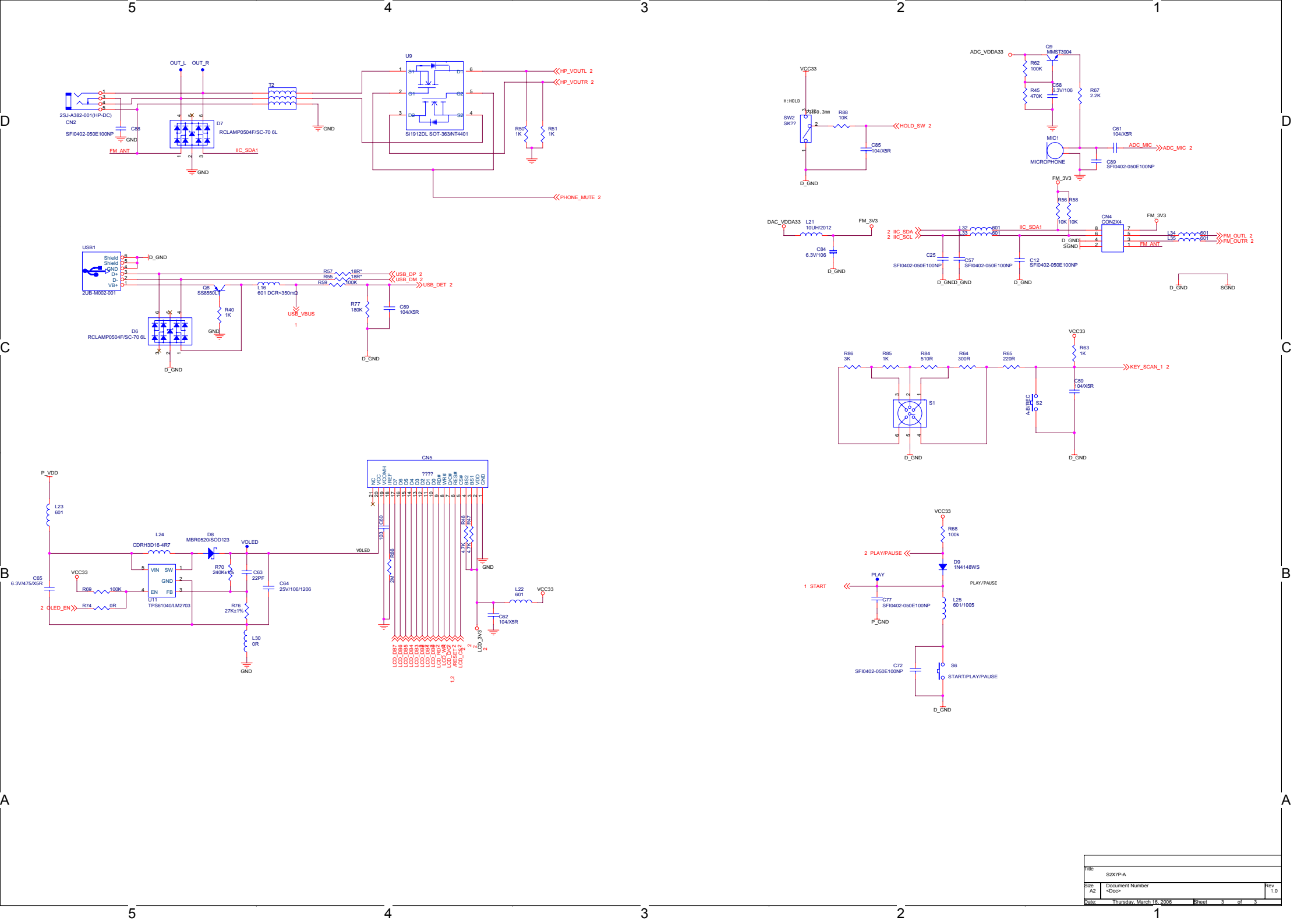
Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

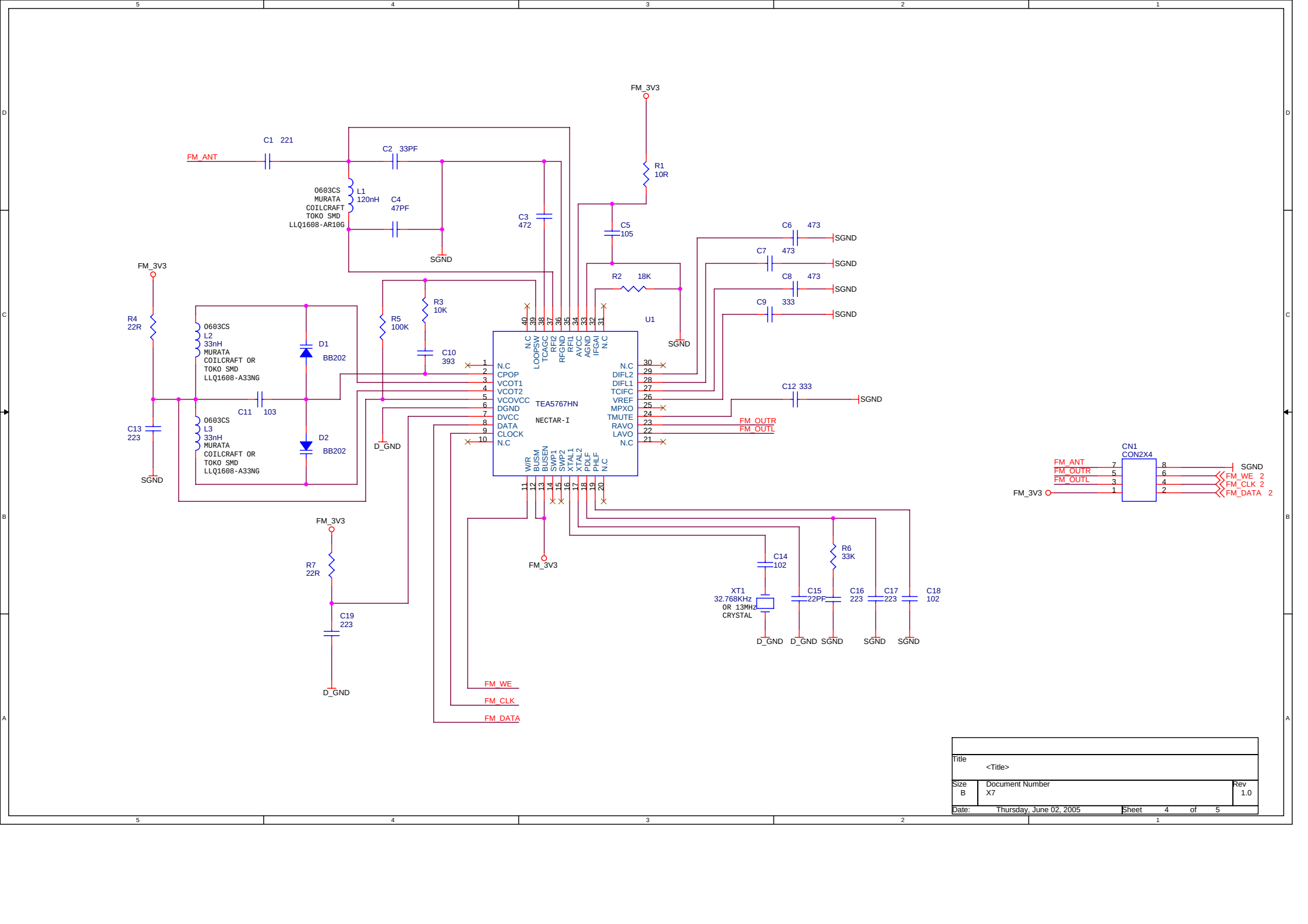
Texas Instruments
Post Office Box 655303
Dallas, Texas 75265


VCC33
U2
G690L263T71/R3111N252CT1
GND
VCC
RESET
P_GND
R5
10K
/RESET 2,3
C4
SFI0402-050E100NP
P_VDD
U1
VIN
GND
EN
VOUT
FB
BYPASS
TPS79301 SOT23-6
C7
6.3V/106/X5R
C5
103
C6
C67
102
SFI0402-050E100NP
R2
68K
R3
20K±1%
R1
33K±1%
C2
22PF
C3
6.3V/106/X5R
VCC33
P_GND
D_GND
A_GND
EN
U3
VI
GND
EN
SW
FB
TPS62200/FAN5307* SOT23-5
L1
CDRH2D18/LD-100
VCC18
R4
300K±1%
C8
47PF
C9
6.3V/106/X5R
C10
101
R6
120K±1%
C1
6.3V/106/X5R
VBUS
USB_VBUS
3 USB_VBUS
BAT43WS
R9
100R
Q2
SI2305DS SOT23
R8
1K
BAT+
BAT+ 2
D3
1N4148WS
R11
100K
R12
100K
Q3
MMST3906
R10
10K
R13
10K
START 3
D4
1N4148WS
R14
100K
R16
5.6M
Q4
SS8050LT
R19
47K
D5
1N4148WS
OFF 2
R41
100K
C17
6.3V/475±10%/X5R
R22
2M
C70
SFI0402-050E100NP
Q10
MMST3904
R43
1M
START 3
C11
6.3V/105
R17
47K
2 /STATUS
C66
SFI0402-050E100NP
U4 ISL6294 DFN8
IN
PPR
CHG
EN
BAT
IREF
IMIN
GND
CN1
BAT
R18
510K
R20
120K±1%
R23
120K±1%
C13
6.3V/105
靠近U4
BAT-
2 I_SET
R25
10K
Q11
SS8050LT
R15
100K
C76
SFI0402-050E100NP
R21
33K
Q5
MMST3906
C16
102*
C15
470K
U5
VSS
RST
NC
VDD
R24
100K
S80829CNNB/S1000N29-N4T1/R3111Q291AT1 SC-82AB
oppo
Title
S2X7P-A
Size
A4
Document Number
<Doc>
Rev
1.0
Date:
Thursday, March 16, 2006
Sheet
1
of
3

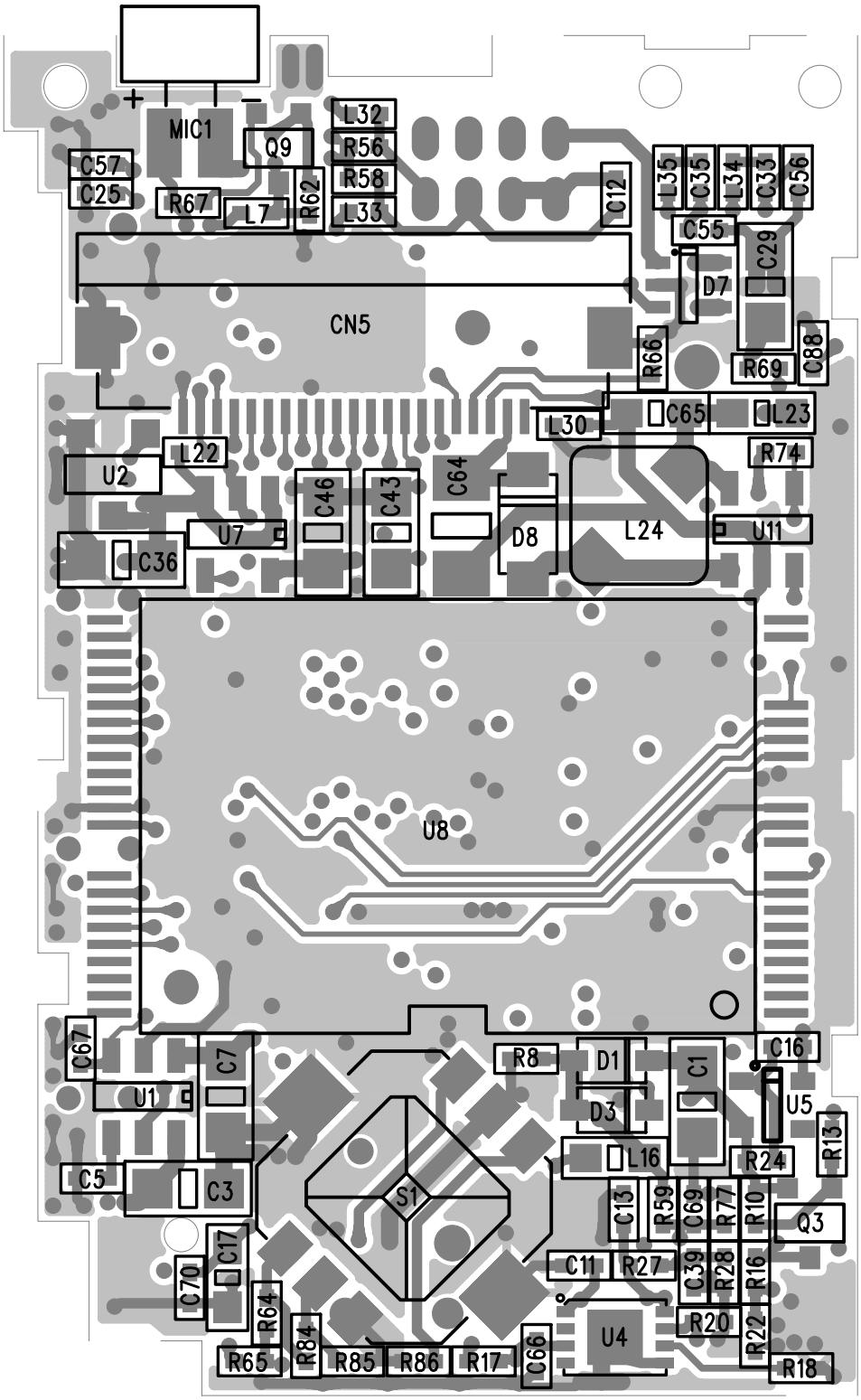

AUDIO PLAYER
SYMPHONY
R35、R32靠近IC！
C65靠近SW1,C73靠近IC
U6
PNX0101
OSCILLATORS
SPDIF
10-BIT ADC
DAC
ADC
LCD INTERFACE
MEMORY CARD
INTERFACE
USB INTERFACE
DA INTERFACE
JTAG
IIC MASTER
INTERFACE
RESET
MPMC
UART
GPIO
DC/DC
U8
TC58512FT
M41T62/M41T62A
Q6
MMST3906
Q7
SS8050LT
SW1
SKRELGED010
Title
S2X7P-A
Size
A2
Document Number
<Doc>
Rev
1.0
Date:
Thursday, March 16, 2006
Sheet
2
of
3

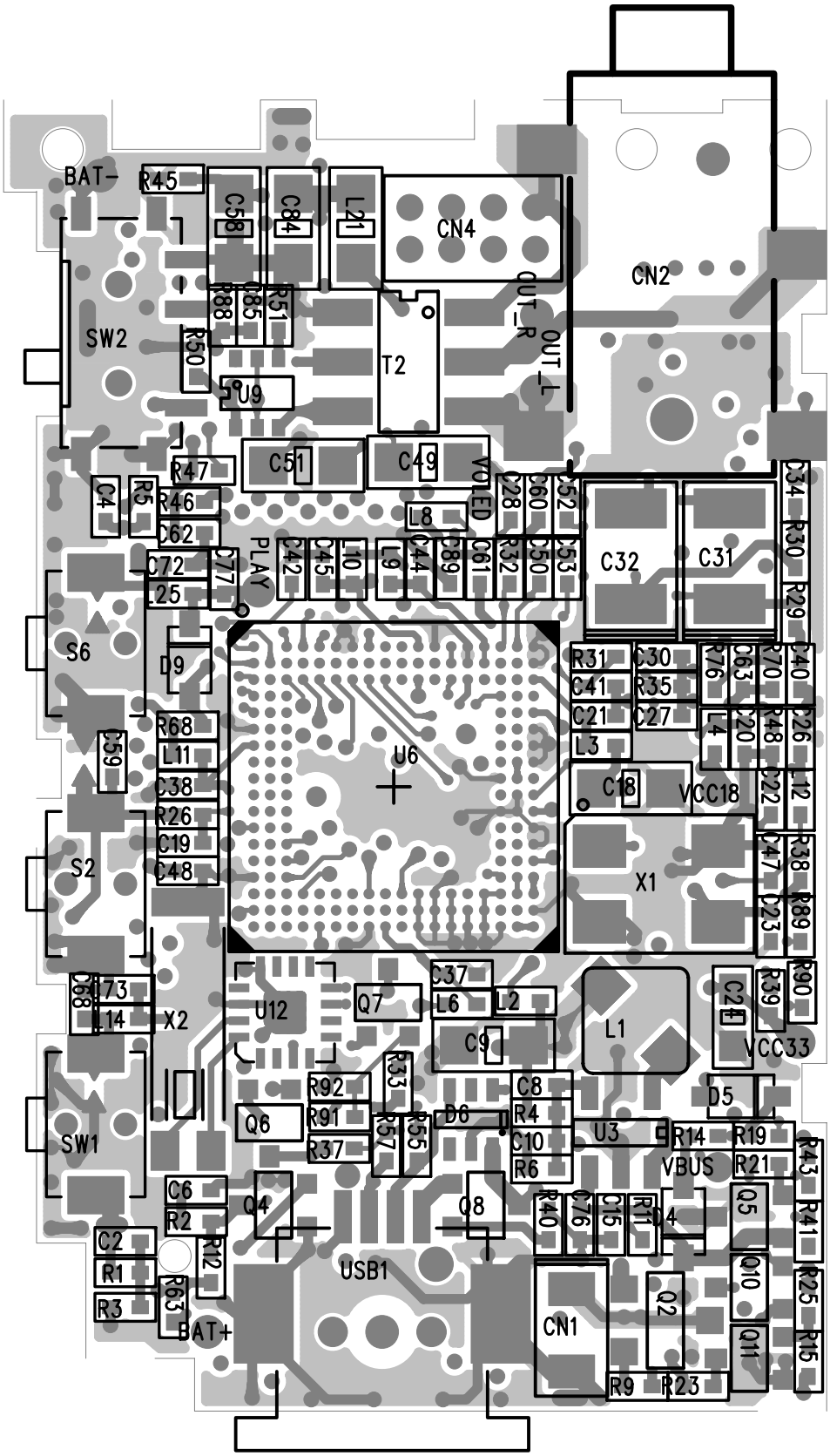


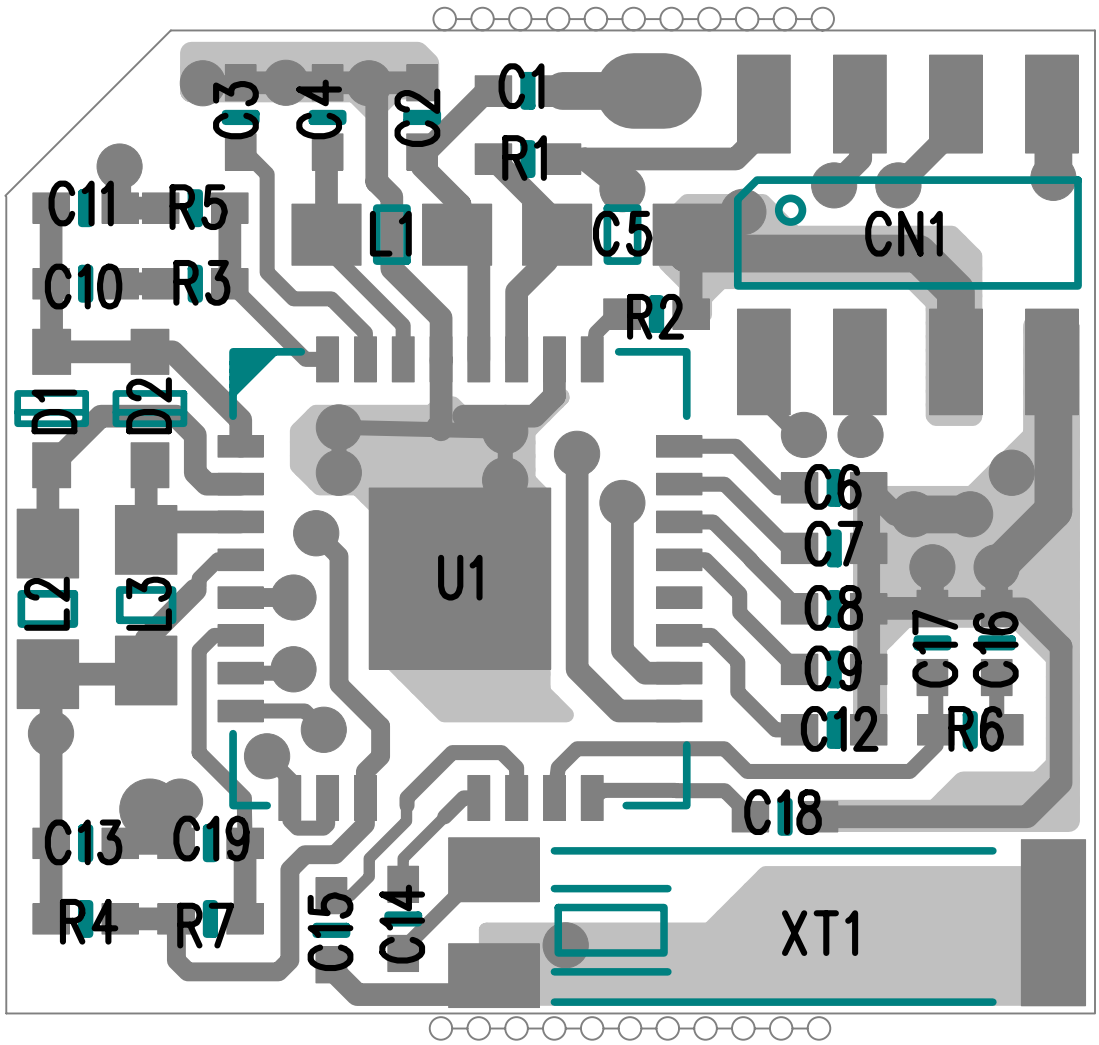
Title	S2X7P-A
Size	A2
Document Number	<Doc>
Rev	1.0
Date:	Thursday, March 16, 2006
Sheet	3 of 3

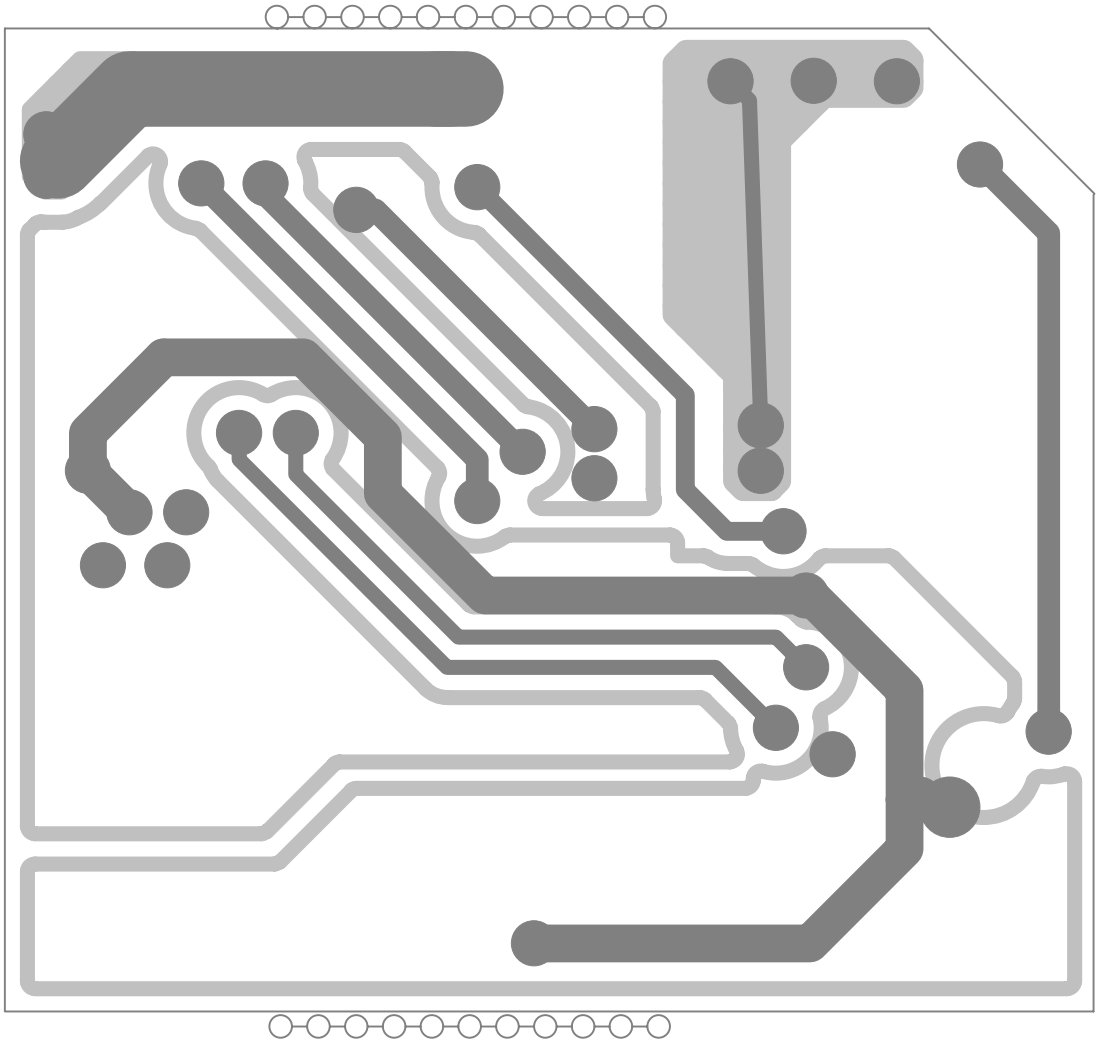


Title	<Title>	
Size B	Document Number X7	Rev 1.0
Date: Thursday, June 02, 2005	Sheet 4 of 5	


MIC1
Q9
L32
R56
R58
L33
C57
C25
R67
L7
R62
C12
L35
C35
L34
C33
C56
C55
C29
D7
CN5
R66
R69
C88
L30
C65
L23
R74
L22
U2
C46
C43
C64
D8
L24
U11
U7
C36
U8
C67
C7
U1
R8
D1
C1
C16
U5
R13
D3
L16
R24
C5
C3
S1
C13
R59
C69
R77
R10
Q3
C17
C70
C11
R27
C39
R28
R16
R64
R84
R20
R22
R65
R85
R86
R17
C66
U4
R18


BAT-
R45
C58
C84
L21
CN4
CN2
OUT_R
OUT_L
SW2
R88
C85
R51
R50
T2
U9
C51
C49
VOLED
C4
R5
R47
R46
C62
C72
C25
C77
PLAY
C42
C45
L10
L9
C44
C89
C61
R32
C50
C53
C52
C28
C60
C32
C31
C34
R30
R29
S6
D9
R31
C41
C21
L3
C30
R35
C27
R76
C63
R70
R48
L4
C20
C40
C26
L12
C18
VCC18
R22
C47
C23
R38
R89
R90
S2
C59
R68
L11
C38
R26
C19
C48
U6
X1
C68
C73
L14
X2
U12
Q7
C37
L6
L2
C9
L1
C24
R39
VCC33
D5
SW1
R92
R91
R37
R33
R57
R55
Q6
D6
C8
R4
C10
R6
U3
R14
R19
VBUS
R21
R43
R41
C6
R2
Q4
Q8
R40
C76
C15
R11
D4
Q5
C2
R1
R3
R12
R63
USB1
CN1
Q2
Q10
Q11
R25
R15
BAT+
R9
R23


C1
R1
C2
C3
C4
C11
R5
C10
R3
L1
C5
R2
CN1
D1
D2
U1
C6
C7
C8
C9
C12
C17
C16
R6
L2
L3
C18
C13
C19
R4
R7
C15
C14
XT1



FX7P-1.pcb - Thu Mar 16 17:55:58 2006

BOM List

MATERIAL CODE	MATERIAL NAME	SPECIFICATIONS	LOCATION
MAINBOARD			
0090324	SMD RESISTOR	1/16W 0O± 5% 0402	L30,R74,R90
0090326	SMD RESISTOR	1/16W 10O± 5% 0402	L10,R29,R30,R31
0090644	SMD RESISTOR	1/16W 18O± 5% 0402	L8,R55,R57
0090339	SMD RESISTOR	1/16W 100O± 5% 0402	R9
0090346	SMD RESISTOR	1/16W 220O± 5% 0402	R65
0090349	SMD RESISTOR	1/16W 300O ± 5% 0402	R64
0090355	SMD RESISTOR	1/16W 510O± 5% 0402	R84
0090362	SMD RESISTOR	1/16W 1K± 5% 0402	R8,R40,R50,R51,R63,R85
0090369	SMD RESISTOR	1/16W 2.2K± 5% 0402	R67
0090372	SMD RESISTOR	1/16W 3K ± 5% 0402	R86
0090377	SMD RESISTOR	1/16W 4.7K± 5% 0402	R46,R47
0090385	SMD RESISTOR	1/16W 10K± 5% 0402	R10,R13,R25,R33,R56,R58,L14,R88,R5
0090396	SMD RESISTOR	1/16W 33K± 5% 0402	R21,R26
0090400	SMD RESISTOR	1/16W 47K± 5% 0402	R19,R17
0090404	SMD RESISTOR	1/16W 68K± 5% 0402	R2
0090408	SMD RESISTOR	1/16W 100K± 5% 0402	R11,R12,R14,R15,R24,R38,R39,R41,R48 ,R59,R62,R68,R69
0090425	SMD RESISTOR	1/16W 470K± 5% 0402	C15,R45
0090433	SMD RESISTOR	1/16W 1MO± 5% 0402	R35,R32,R43
0090436	SMD RESISTOR	1/16W 2MO± 5% 0402	R22,R66
0090443	SMD RESISTOR	1/16W 5.6MO± 5% 0402	R16
0090639	PRECISION SMD RESISTOR	1/16W 1.5K± 1% 0402	R37
0090672	PRECISION SMD RESISTOR	1/16W 20K ± 1% 0402	R3
0090485	PRECISION SMD RESISTOR	1/16W 27K± 1% 0402	R76
0090671	PRECISION SMD RESISTOR	1/16W 33K ± 1% 0402	R1
0090509	PRECISION SMD RESISTOR	1/16W 100K± 1% 0402	R27
0090681	PRECISION SMD RESISTOR	1/16W 120K± 1% 0402	R6,R20,R23
0090645	PRECISION SMD RESISTOR	1/16W 180K± 1% 0402	R28,R77
0090687	PRECISION SMD RESISTOR	1/16W 240K± 1% 0402	R70
0090682	PRECISION SMD RESISTOR	1/16W 300K± 1% 0402	R4
0090667	PRECISION SMD RESISTOR	1/16W 510K ± 1% 0402	R18
1030029	SMD PRESS SENSITIVITY RESISTOR	SFI0402-050E100NP	C4,C19,C54,C55,C56,C66,C67,C68,C70, C72,C73,C76,C77,C88,C89

MATERIAL CODE	MATERIAL NAME	SPECIFICATIONS	LOCATION
1030033	SMD PRESS SENSITIVITY RESISTOR	SDV1005H180C100GPT 0402	C4,C19,C54,C55,C56,C66,C67,C68,C70,C72,C73,C76,C77,C88,C89
0310416	SMD CAPACITOR	50V 22P± 5% NPO 0402	C2,C22,C23,C63
0310424	SMD CAPACITOR	50V 47P± 5% NPO 0402	C8
0310432	SMD CAPACITOR	50V 101± 5% NPO 0402	C10
0310704	SMD CAPACITOR	25V 102± 10% X7R 0402	C6,C53
0310705	SMD CAPACITOR	25V 332± 10% X7R 0402	C27,C28
0310453	SMD CAPACITOR	25V 103± 10% X7R 0402	C5,C60
0310480	SMD CAPACITOR	10V 104± 10% X5R 0402	C20,C21,C26,C30,C34,C37,C38,C39,C40,C41,C42,C44,C45,C47,C48,C50,C52,C59,C61,C62,C69,C85
0310776	SMD CAPACITOR	6.3V 105± 20% X5R 0402	C11,C13,C33,C35
0310662	SMD CAPACITOR	6.3V 105± 10% X5R 0402	C11,C13,C33,C35
0310757	SMD CAPACITOR	10V 105± 10% X7R 0402	C11,C13,C33,C35
0310674	SMD CAPACITOR	6.3V 475± 10% X5R 0603	C17
0310717	SMD CAPACITOR	6.3V 475± 20% X5R 0603	C65,C24
0310486	SMD CAPACITOR	6.3V 106± 20% X5R 0805	C1,C3,C7,C9,C36,C46
0310701	SMD CAPACITOR	10V 106± 20% Y5V 0805	C18,C29,C43,C49,C51,C58,C84
0310389	SMD CAPACITOR	10V 106 +80%-20% Y5V 0805	C18,C29,C43,C49,C51,C58,C84
0310752	SMD CAPACITOR	25V 106± 10% X5R 1206	C64
0310736	SMD TANTALUM CAPACITOR	4V 220uF± 20% 3528(B)	C31,C32
0390142	SMD MAGNETIC BEADS	FCM1608-601T02	L16,L23
0390388	SMD MAGNETIC BEADS	600O/100MHZ± 25% 1005	L2,L3,L4,L6,L7,L9,L11,L12,L22,L25,L32,L33,L34,L35
0390044	SMD INDUCTOR	10UH ± 10% 2012	L21
0390397	SMD CORES INDUCTOR	10uH ± 20% CDRH2D11/HP	L1
0390384	SMD CORES INDUCTOR	4.7uH ± 20% CDRH3D16-4R7	L24
0390387	SMD CORES INDUCTOR	4.7uH ± 30% CDRH3D16/HP	L24
1090080	ESD ELEMENT	RCLAMP0504F SC70-6L	D6,D7
1090084	ESD ELEMENT	PLR0504F-P SC70-6L	D6,D7
0700154	SMD TRIODE	1N4148WS SOD-323	D3,D4,D5,D9
0680074	SMD SCHOTTKY DIODE	BAT43WS SOD-323	D1
0680077	SMD SCHOTTKY DIODE	MBR0520 SOD123	D8
0780298	SMD TRIODE	MMST3904 SOD-323	Q9,Q10
0780299	SMD TRIODE	SS8050LT SOD-323	Q4,Q11
0780293	SMD TRIODE	MMST3906 SOD-323	Q3,Q5,Q6
0780300	SMD TRIODE	SS8550LT SOD-323	Q8

MATERIAL CODE	MATERIAL NAME	SPECIFICATIONS	LOCATION
0790041	SMD FIELD EFFECT TRANSISTOR	SI2305DS SOT-23	Q2
1000044	COMMON MODE FILTER	500O/100MHz 5×5.3×2.7	T2
0790068	SMD FIELD EFFECT TRANSISTOR	SI1912 SOT363	U9
0790070	SMD FIELD EFFECT TRANSISTOR	NTJD4401N SOT363	U9
0882475	IC	TPS79301 SOT23-6	U1
0882668	IC	TPS79333DBVR SOT23-5	U1
0882481	IC	G690L263T71 SOT23-3	U2
0882476	IC	TPS62200 SOT23-5	U3
0882851	IC	ISL6294IRZ DFN	U4
0882524	IC	S80829CNNB SC-82	U5
0882403	IC	PNX0101ET/N302 TFBGA	U6
0882480	IC	PQ1X281M2ZP SOT23-5	U7
0882629	IC	TPS793285DBVR SOT23-5	U7
0882324	IC	K9F2G08U0M-YCBO TSOP	U8
0882576	IC	K9F2G08U0M-PIB0 TSOP	U8
0882565	IC	LM2703 SOT-23-5	U11
1340099	SMD LIGHT TOUCH SWITCH	SKRELGE010	SW1,S2,S6
1310057	SMD STIR SWITCH	SSSS811101	SW2
1340119	SMD LIGHT TOUCH SWITCH	SKRHABE010	S1
1140070	MICROPHONE	44dB ± 3dB 4×1.5 WITH NEEDLE	MIC1
1980050	EARPHONE SOCKET	2SJ-A382-001	CN2
1860085	USB SOCKET	2UB-M002-001	USB1
1940282	CABLE SOCKET	21P 0.5mm SMD,SUBMIT MEET WITH CLASP	CN5
1970081	DUAL FLAT NEEDLE	2×4 4.5mm 1.27mm STRAIGHT INSERT,MOLD HIGH:1mm	CN4
0960284	SMD CRYSTAL OSCILLATOR	12MHz± 30ppm 5032/4 20P	X1
1632959	PCB	2X7P-1	
BATTERY PROTECT BOARD			
0090223	SMD RESISTOR	1/16W 2K ± 5%	R2
0090011	SMD RESISTOR	1/16W 470O ± 5% 0603	R1
0310207	SMD CAPACITOR	50V104 ± 20% 0603	C1,C2,C3
0310543	SMD CAPACITOR	50V 104 ± 10% X7R 0603	C1,C2,C3
0882570	IC	S-8261AANMD-G2N-T2 SOT23-6	U1
0790065	SMD FIELD EFFECT TRANSISTOR	ECH8601 TSSOP	U2
0790090	SMDFIELD EFFECT TRANSISTOR	ECH8601R TSSOP	U2

MATERIAL CODE	MATERIAL NAME	SPECIFICATIONS	LOCATION
1632263	PCB	EX9-0	
FM MODULE			
0310432	SMD CAPACITOR	50V 101± 5% NPO 0402	C1
0310418	SMD CAPACITOR	50V 27P± 5% NPO 0402	C2
0310706	SMD CAPACITOR	25V 472± 10% X7R 0402	C3
0310424	SMD CAPACITOR	50V 47P± 5% NPO 0402	C4
0310717	SMD CAPACITOR	6.3V 475± 20% X5R 0603	C5
0310712	SMD CAPACITOR	10V 473± 10% X5R 0402	C6,C7,C8
0310710	SMD CAPACITOR	16V 333± 10% X5R 0402	C12,C9
0310711	SMD CAPACITOR	10V 393± 10% X5R 0402	C10
0310453	SMD CAPACITOR	25V 103± 10% X7R 0402	C11
0310480	SMD CAPACITOR	10V 104± 10% X5R 0402	C13,C19
0310704	SMD CAPACITOR	25V 102± 10% X7R 0402	C14,C18
0310416	SMD CAPACITOR	50V 22P± 5% NPO 0402	C15
0310455	SMD CAPACITOR	16V 223± 10% X7R 0402	C16,C17
0090326	SMD RESISTOR	1/16W 10O± 5% 0402	R1
0090390	SMD RESISTOR	1/16W 18K± 5% 0402	R2
0090385	SMD RESISTOR	1/16W 10K± 5% 0402	R3
0090447	SMD RESISTOR	1/16W 22O± 5% 0402	R7,R4
0090408	SMD RESISTOR	1/16W 100K± 5% 0402	R5
0090396	SMD RESISTOR	1/16W 33K± 5% 0402	R6
0700115	SMD TRANSFIGURATION DIODE	BB202	D1,D2
0390112	SMD COIL THREAD INDUCTOR	33nH± 5% 1608	L2,L3
0390326	SMD COIL THREAD INDUCTOR	120nH± 5% 1608	L1
0882388	IC	TEA5767HN HVQFN	U1
0960279	SMD CRYSTAL OSCILLATOR	32.768KHz ± 20ppm SSPT6 12.5P	XT1
1860088	FLAT FEMALE	4p 1.27mm DUAL RANK,SMD,MOLD HIGH 2.1mm	CN1
1632960	PCB	FX7P-1	

MATERIAL CODE	MATERIAL NAME	SPECIFICATIONS
LITHIUM BATTERY CORD UNIT		
1510156	RECHARGEABLE BATTERY	260mAH 3.7V LITHIUM 38×23×3.4
5446654	PCB SEMI-FINISHED PRODUCT	SEX9-0 X9
2110167	LEAD	28# 30mm BLACK
2110507	LEAD	28# 25mm RED
ASSEMBLY		
3110589	ALUMINIUM ALLOY OUTER CASING	X7-2(RU)(256M) GREEN
3071924	UPPER BRACKET	X7-2(RU)
3070991	LOWER BRACKET	X7 2#
3070846	COVER BOARD OF PRESS BUTTON	X7 PLATING
3070214	5-DIRECTION BUTTON	X7 PLATING
3070215	LOCK BUTTON	X7 PLATING
3070216	COMBINATION BUTTON	X7 PLATING
3071925	LOWER COVER BOARD	X7-2(RU) PLATING
3070218	OVERHEAD DOOR	X7 PLATING
3071811	UPPER COVER BOARD	X7 PLATING 3#
3071926	GLASS	X7-2(RU) BLACK
3810061	PRESSING SPRING	F1.5×6 F0.2
3820088	WRING SPRING	X7 F0.35 2#
3871391	GATE SPIN AXIS	F0.8×12.5
3150028	FLYING RINGS	X7 PLATING 2#
4450047	“E” RINGS	F2×F4×0.4
5234798	PORON SOFT SPACER	F3.8×0.6 SINGLE-FACED WITH GLUE IN REAR SIDE
4040081	SELF-TAPPING SCREW	FB1.2×3.5H WHITE NICKEL
4040090	SELF-TAPPING SCREW	FB 1.2×4 WHITE NICKEL
4040082	SELF-TAPPING SCREW	FB1.2×5.5H WHITE NICKEL
5233662	SOFT SPONGE SPACER	7×5×2 DOUBLE-FACED,SOFT
5233764	SOFT SPONGE SPACER	8×5×1 DOUBLE-FACED,SOFT
1210248	OLED MODULE	RGS080960390W006
5461874	LITHIUM BATTEMETAL OXIDE FILM RESISTOR CORE UNIT	260mAH 3.7V 38×23×3.4
1632909	FPC SOCKET	4X7P-0
5447789	PCB SEMI-FINISHED PRODUCT	2X7P-0 X7-2(RU)
5447790	PCB SEMI-FINISHED PRODUCT	FX7P-0 X7-2(RU)

MATERIAL CODE	MATERIAL NAME	SPECIFICATIONS
PACKAGE MATERIAL		
2180086	USB CORD	1.2m DOUBLE HEAD(USB MALE/MINI 4P MALE) USB2.0
5233737	PROTECT FILM	X7
5070981	GLUE BAG FOR ENVIRONMENTAL PROTECTION (WITH HOLE)	145× 65× 0.05 PE
5071010	DISC PACKING BAG	86× 86× 0.01 PE WITH HEAL GLUE 2#
5070982	DISC PACKING BAG	86× 86× 0.01 PE WITH HEAL GLUE
5013016	INNER PAPER CSE	154× 61× 125 X7
5210465	WARRANTY CARD	MP3 120× 80 RUSSIA
5456529	MP3 PLAYER	X7-2(RU)(256M) GREEN
5194438	USER MANUAL	X7-2(RU) ENGLISH/RUSSIA
2400253	SUITABLE SOFTWARE DISC (8cm)	MP3(RU) philips
5070954	GLUE BAG FOR ENVIRONMENTAL PROTECTION (WITH HOLE)	95× 65× 0.05 PE
5070953	RUBBER SET	X7
5142663	SN LABELL	MP3(RUSSIA BBK) WITH BAR CODE NUMBER
5013589	GIFT BOX	X7-2(RU)
5002899	CARTON BOX	33× 32.5× 15.5cm3 X7-2(RU)
5180014	SEALING STICKER OF CARTON BOX	0
5002900	CARTON BOX	63× 33.5× 34.5cm3 X7-2(RU)
5180014	SEALING STICKER OF CARTON BOX	0
5156132	MODEL LABELL FOR GIFE BOX	X7-2(RU) GREEN
5156135	PAPER BOX WITH MODEL STICKER	X7-2(RU) GREEN 65× 38
5180752	COLOR LABELL	APPLE GREEN (COLOR) F12
5071067	LIFTING ROPE	MP3(OPPO)GIRTH:80cm GREY BLACK ALTERNATE WITH
5180806	SEALING LABELL OF GIFT BOX	X17(RU) F25
5471438	CHARGER	@5V 300mA WITH miniUSB HEAD,RUSSIA CE
1150063	EARPHONE	OPPO/Sennheiser MX400 WITH EARPHONE SET
SN LASEL		
5142067	SN LABELL	RUSSIA WITHOUT BAR CODE NUMBER
SUPPLEMENT MODULE		
5233646	RESIST HIGH TEMPERATURE INSULATING TAPE	LENGTH:33m WIDTH:6mm
5120754	GLUEWATER	LOCTITE 3517
5120592	3M GLUEWATER	DP460(37ML)
5120761	AID WELDING GREASE	MC40