LG

Service Manual

Model : U8110

LG

Service Manual

U8110

P/N : MMBD0032201

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1. INTRODUCTION

1.1 Purpose

This manual provides the information necessary to repair, calibration, description and download the features of this model.

1.2 Regulatory Information

A. Security

Toll fraud, the unauthorized use of telecommunications system by an unauthorized part (for example, persons other than your company's employees, agents, subcontractors, or person working on your company's behalf) can result in substantial additional charges for your telecommunications services. System users are responsible for the security of own system. There are may be risks of toll fraud associated with your telecommunications system. System users are responsible for programming and configuring the equipment to prevent unauthorized use. The manufacturer does not warrant that this product is immune from the above case but will prevent unauthorized use of common-carrier telecommunication service of facilities accessed through or connected to it. The manufacturer will not be responsible for any charges that result from such unauthorized use.

B. Incidence of Harm

If a telephone company determines that the equipment provided to customer is faulty and possibly causing harm or interruption in service to the telephone network, it should disconnect telephone service until repair can be done. A telephone company may temporarily disconnect service as long as repair is not done.

C. Changes in Service

A local telephone company may make changes in its communications facilities or procedure. If these changes could reasonably be expected to affect the use of the phones or compatibility with the network, the telephone company is required to give advanced written notice to the user, allowing the user to take appropriate steps to maintain telephone service.

D. Maintenance Limitations

Maintenance limitations on the phones must be performed only by the manufacturer or its authorized agent. The user may not make any changes and/or repairs expect as specifically noted in this manual. Therefore, note that unauthorized alternations or repair may affect the regulatory status of the system and may void any remaining warranty.

E. Notice of Radiated Emissions

This model complies with rules regarding radiation and radio frequency emission as defined by local regulatory agencies. In accordance with these agencies, you may be required to provide information such as the following to the end user.

F. Pictures

The pictures in this manual are for illustrative purposes only; your actual hardware may look slightly different.

G. Interference and Attenuation

A phone may interfere with sensitive laboratory equipment, medical equipment, etc.
Interference from unsuppressed engines or electric motors may cause problems.

H. Electrostatic Sensitive Devices

ATTENTION

Boards, which contain Electrostatic Sensitive Device (ESD), are indicated by the sign.
Following information is ESD handling:

- Service personnel should ground themselves by using a wrist strap when exchange system boards.
- When repairs are made to a system board, they should spread the floor with anti-static mat which is also grounded.
- Use a suitable, grounded soldering iron.
- Keep sensitive parts in these protective packages until these are used.
- When returning system boards or parts like EEPROM to the factory, use the protective package as described.

1.3 Abbreviations

For the purposes of this manual, following abbreviations apply:

APC	Automatic Power Control
BB	Baseband
BER	Bit Error Ratio
CC-CV	Constant Current – Constant Voltage
CLA	Cigar Lighter Adapter
DAC	Digital to Analog Converter
DCS	Digital Communication System
dBm	dB relative to 1 milliwatt
DSP	Digital Signal Processing
DTC	DeskTop Charger
EEPROM	Electrical Erasable Programmable Read-Only Memory
EL	Electroluminescence
ESD	Electrostatic Discharge
FPCB	Flexible Printed Circuit Board
GMSK	Gaussian Minimum Shift Keying
GPIB	General Purpose Interface Bus
GPRS	General Packet Radio Service
GSM	Global System for Mobile Communications
IPUI	International Portable User Identity
IF	Intermediate Frequency
LCD	Liquid Crystal Display
LDO	Low Drop Output
LED	Light Emitting Diode
OPLL	Offset Phase Locked Loop
PAM	Power Amplifier Module
PCB	Printed Circuit Board
PGA	Programmable Gain Amplifier
PLL	Phase Locked Loop

PSTN	Public Switched Telephone Network
RF	Radio Frequency
RLR	Receiving Loudness Rating
RMS	Root Mean Square
RTC	Real Time Clock
SAW	Surface Acoustic Wave
SIM	Subscriber Identity Module
SLR	Sending Loudness Rating
SRAM	Static Random Access Memory
UMTS	Universal Mobile Telephony System

2. PERFORMANCE

2.1 System Overview

Item	Specification
Shape	GSM900/1 800 & WCDMA Folder- Dual Mode Handset
Size	49.5 x 95.7 x 22.5 mm
Weight	120g (with Battery)
Power	4.0V > 1200mAh Li-Ion
Talk Time	Over 140 Min (WCDMA, Tx=12 dBm, Voice) Over 180 Min (GSM, Tx=Max, Voice)
Standby Time	Over 120 hrs (WCDMA, DRX=1.28) Over 1 50 hrs (GSM, Paging period=9)
Antenna	Fixed Type (Fixed Screw)
LCD	176 x 220 Pixel
Main LCD BL	White LED Back Light
Sub LCD BL	7-color LED
Vibrator	Yes (Coin Type)
LED Indicator	7-color(Sub LCD BL)
C-MIC	Yes
Receiver	Yes
Earphone Jack	Yes
SIM Socket	Yes (3.0V/1.8V)
Volume Key	Push Type(+,-)
Voice Key	Push Type (Memo)
I/O Connect	24 Pin

2.2 Usable environment

1) Environment

Item	Spec.	Unit
Voltage	4.0 (Typ), 3.4 (Min), (Shut Down: 3.2)	V
Size	-20 ~ + 60	°C
Storage	-30 ~ + 85	°C
Humidity	max. 85	%

2) Environment(Accessory)

Item	Spec.	Min	Typ.	Max	Unit
Power	Available power	100	220	240	Vac

* CLA: 12~24V(DC)

2.3 Radio Performance

1) Transmitter -GSM Mode

<table>
<tr><th>No</th><th colspan="2">Item</th><th colspan="2">GSM</th><th colspan="2">DCS</th></tr>
<tr><td rowspan="10">1</td><td rowspan="10">Conducted Spurious Emission</td><td rowspan="4">MS allocated Channel</td><td rowspan="2">100k ~ 1GHz</td><td rowspan="2">-39dBm</td><td>9k ~ 1GHz</td><td>-39dBm</td></tr>
<tr><td>1G ~ 1710MHz</td><td>-33dBm</td></tr>
<tr><td rowspan="2">1G ~ 12.75GHz</td><td rowspan="2">-33dBm</td><td>1710M ~ 1785MHz</td><td>-39dBm</td></tr>
<tr><td>1785M ~ 12.75GHz</td><td>-33dBm</td></tr>
<tr><td rowspan="6">Idle Mode</td><td>100k ~ 880MHz</td><td>-60dBm</td><td>100k ~ 880MHz</td><td>-60dBm</td></tr>
<tr><td>880M ~ 915MHz</td><td>-62dBm</td><td>880M ~ 915MHz</td><td>-62dBm</td></tr>
<tr><td>915M ~ 1000Mz</td><td>-60dBm</td><td>915M ~ 1000MHz</td><td>-60dBm</td></tr>
<tr><td>1G ~ 1.71GHz</td><td>-50dBm</td><td>1G ~ 1.71GHz</td><td>-50dBm</td></tr>
<tr><td>1.71G ~ 1.785GHz</td><td>-56dBm</td><td>1.71G ~ 1.785GHz</td><td>-56dBm</td></tr>
<tr><td>1.785G ~ 12.75GHz</td><td>-50dBm</td><td>1.785G ~ 12.75GHz</td><td>-50dBm</td></tr>
</table>

2. PERFORMANCE

No	Item		GSM		DCS	
1	Radiated Spurious Emission	MS allocated Channel	30M ~ 1GHz	-36dBm	30M ~ 1GHz	-36dBm
					1G ~ 1710MHz	-30dBm
			1G ~ 4GHz	-30dBm	1710M ~ 1785MHz	-36dBm
					1785M ~ 4GHz	-30dBm
		Idle Mode	30M ~ 880MHz	-57dBm	30M ~ 880MHz	-57dBm
			880M ~ 915MHz	-59dBm	880M ~ 915MHz	-59dBm
			915M ~ 1000Mz	-57dBm	915M ~ 1000MHz	-57dBm
			1G ~ 1.71GHz	-47dBm	1G ~ 1.71GHz	-47dBm
			1.71G ~ 1.785GHz	-53dBm	1.71G ~ 1.785GHz	-53dBm
			1.785G ~ 4GHz	-47dBm	1.785G ~ 4GHz	-47dBm
2	Frequency Error		±0.1ppm		±0.1ppm	
3	Phase Error		±5(RMS)		±5(RMS)	
			±20(PEAK)		±20(PEAK)	
4	Frequency Error Under Multipath and Interference Condition		3dB below reference sensitivity		3dB below reference sensitivity	
			RA250: ±200Hz		RA250: ±250Hz	
			HT100: ±100Hz		HT100: ±250Hz	
			TU50: ±100Hz		TU50: ±150Hz	
			TU3: ±150Hz		TU1.5: ±200Hz	
5	Output RF Spectrum	Due to modulation	0 ~ 100kHz	+0.5dB	0 ~ 100kHz	+0.5dB
			200kHz	-30dB	200kHz	-30dB
			250kHz	-33dB	250kHz	-31dB
			400kHz	-60dB	400kHz	-33dB
			600 ~ 1800kHz	-66dB	600 ~ 1800kHz	-60dB
			1800 ~ 3000kHz	-69dB	1800 ~ 6000kHz	-60dB
			3000 ~ 6000kHz	-71dB	≥6000kHz	-73dB
			≥6000kHz	-77dB		
		Due to Switching transient	400kHz	-19dB	400kHz	-22dB
			600kHz	-21dB	600kHz	-24dB
			1200kHz	-21dB	1200kHz	-24dB
			1800kHz	-24dB	1800kHz	-27dB

No	Item	GSM			DCS		
7	Intermodulation attenuation		–		Frequency offset		800kHz
					Intermodulation product should be Less than 55dB below the level of Wanted signal		
8	Transmitter Output Power	Power control Level	Power (dBm)	Tolerance (dB)	Power control Level	Power (dBm)	Tolerance (dB)
		5	33	±3	0	30	±3
		6	31	±3	1	28	±3
		7	29	±3	2	26	±3
		8	27	±3	3	24	±3
		9	25	±3	4	22	±3
		10	23	±3	5	20	±3
		11	21	±3	6	18	±3
		12	19	±3	7	16	±3
		13	17	±3	8	14	±3
		14	15	±3	9	12	±4
		15	13	±3	10	10	±4
		16	11	±5	11	8	±4
		17	9	±5	12	6	±4
		18	7	±5	13	4	±4
		19	5	±5	14	2	±5
					15	0	±5
9	Burst timing	Mask IN			Mask IN		

2. PERFORMANCE

2) Transmitter-WCDMA Mode

No	Item	Specification
1	Maximum Output Power	Class3: +24dBm(+1/-3dB) Class4: +21dBm(±2dB)
2	Frequency Error	±0.1ppm
3	Open Loop Power control in uplink	±9dB@normal, ±12dB@extreme
4	Inner Loop Power control in uplink	Adjust output(TPC command) cmd 1dB 2dB 3dB +1 +0.5/1.5 +1/3 +1.5/4.5 0 -0.5/+0.5 -0.5/+0.5 -0.5/+0.5 -1 -0.5/-1.5 -1/-3 -1.5/-4.5 group(10equal command group) +1 +8/+12 +16/+24
5	Minimum Output Power	-50dBm(3.84MHz)
6	Out-of-synchronization handling of output power	Qin/Qout:DPCCH quality levels Toff@DPCCH/lor:-22->-28dB Ton@DPCCH/lor:-24->-18dB
7	Transmit OFF Power	-56dBm(3.84M)
8	Transmit ON/OFF Time Mask	±25us PRACH, CPCH, uplink compressed mode
9	Change of TFC	±25us power varies according to the data rate DTX: DPCH off (minimize interference between UE)
10	Power setting in uplink compressed	±3dB(after 14slots transmission gap)
11	Occupied Bandwidth(OBW)	5MHz(99%)
12	Spectrum emission Mask	-35-15*(Δf-2.5)dBc@Δf=2.5~3.5MHz, 30k -35-1*(Δf-3.5)dBc@Δf=3.5~7.5MHz, 1M -39-10*(Δf-7.5)dBc@Δf=7.5~8.5MHz, 1M -49 dBc@Δf=8.5~12.5MHz, 1M

No	Item	Specification
13	Adjacent Channel Leakage Ratio(ACLR)	33dB@5MHz, ACP>-50dBm 43dB@10MHz, ACP>-50dBm
14	Spurious Emissions *: additional requirement	-36dBm@f=9~150KHz, 1k BW -36dBm@f=150KHz~30MHz, 10k -36dBm@f=30~1000MHz, 100k -30dBm@f=1~12.75GHz, 1M -41dBm*@1893.5~1919.6MHz, 300k -67dBm*@925~935MHz, 100k -79dBm*@935~960MHz, 100k -71dBm*@1805~1880MHz, 100k
15	Transmit Intermodulation	-31dBc@5MHz, Interferer -40dBc -41dBc@10MHz, Interferer -40dBc
16	Error Vector Magnitude(EVM)	17.5% (>-20dBm) (@12.2k, 1DPDCH+1DPCCH)
17	Transmit OFF Power	-15dB@SF=4, 768kbps, multi-code transmission

3)Receiver - GSM Mode

No	Item		GSM	DCS
1	Sensitivity (TCH/FS Class II)		-105dBm	-105dBm
2	Co-Channel Rejection (TCH/FS Class II, RBER, TUhigh/FH)		C/Ic=7dB	C/Ic=7dB
3	Adjacent Channel Rejection	200kHz	C/Ia1=-12dB	C/Ia1=-12dB
		400kHz	C/Ia2=-44dB	C/Ia2=-44dB
4	Intermodulation Rejection		Wanted Signal: -98dBm 1'st interferer: -44dBm 2'st interferer: -45dBm	Wanted Signal: -96dBm 1'st interferer: -44dBm 2'st interferer: -44dBm
5	Blocking Response (TCH/FS Class II, RBER)		Wanted Signal: -101dBm Unwanted Signal: Depend on freq.	Wanted Signal: -101dBm Unwanted Signal: Depend on freq.

4) Receiver - WCDMA Mode

No	Item	Specification
18	Reference Sensivitivity Level	-106.7dBm(3.84M)
19	Maximum Input Level	-25dBm(3.84MHz) -44dBm/3.84MHz(DPCH_Ec) UE@+20dBm output power(class3)
20	Adjacent Channel Selectivity(ACS)	33dB UE@+20dBm output power(class3)
21	In-band Blocking	-56dBm/3.84MHz@10MHz UE@+20dBm output power(class3)
		-44dBm/3.84MHz@15MHz UE@+20dBm output power(class3)
22	Out-band Blocking	-44dBm/3.84MHz@f=2050~2095 & 2185~2230MHz, band a) UE@+20dBm output power(class3)
		-30dBm/3.84MHz@f=2025~2050 & 2230~2255MHz, band a) UE@+20dBm output power(class3)
		-15dBm/3.84MHz@f=1~2025 & 2255~12500MHz, band a) UE@+20dBm output power(class3)
23	Spurious Response	-44dBm CW UE@+20dBm output power(class3)
24	Intermodulation Characteristic	-46dBm CW@10MHz & -46dBm/3.84MHz@20MHz UE@+20dBm output power(class3)
25	Spurious Emissions	-57dBm@f=9KHz~1GHz, 100k BW
		-47dBm@f=1~12.75GHz, 1M
		-60dBm@f=1920~1980MHz, 3.84MHz
		-60dBm@f=2110~2170MHz, 3.84MHz

2.4 Current Consumption

(VT test : Speaker off, LCD backlight On)

	Stand by	Voice Call	VT
WCDMA	120Hours=10mA (DRX=1.28)	140Min=514mA (Tx=12dBm)	100Min=720mA (Tx=12dBm)
GSM	150Hours=8mA (paging=9period)	180Min=400mA (Tx=Max)	

2.5 RSSI

TBD

	GSM	WCDMA(TBD)
BAR 4 → 3	-91 ±2dBm	
BAR 3 → 2	-96 ±2dBm	
BAR 2 → 1	-101 ±2dBm	
BAR 1 → 0	-106 ±2dBm	

2.6 Battery Bar

Indication	Voltage
BAR 4 → 3 (68%)	3.87 ±0.03V
BAR 3 → 2 (47%)	3.77 ±0.03V
BAR 2 → 1 (26%)	3.72 ±0.03V
BAR 1 → Icon Blinking (5%)	3.50 ±0.03V
Low voltage, warning message	3.50 ±0.03V(Talk: 1min. interval) -5% 3.46 ±0.03V(Standby: 3min. Inverval) -3%
Power OFF	3.10 ±0.03V ↓ (WCDMA Talk) 3.20 ±0.03V ↓ (else)

2.7 Sound Pressure Level

<table>
<tr><th></th><th>No</th><th colspan="4">Test Item</th><th colspan="2">Specification</th></tr>
<tr><td rowspan="36">A
C
O
U
S
T
I
C</td><td rowspan="2">1</td><td colspan="3" rowspan="2">Sending Loudness Rating (SLR)</td><td rowspan="14">MS</td><td>NOM</td><td rowspan="2">8±3dB</td></tr>
<tr><td>MAX</td></tr>
<tr><td rowspan="2">2</td><td colspan="3" rowspan="2">Receiving Loudness Rating (RLR)</td><td>NOM</td><td>-1±3dB</td></tr>
<tr><td>MAX</td><td>-13±1dB</td></tr>
<tr><td rowspan="2">3</td><td colspan="3" rowspan="2">Side Tone Masking Rating (STMR)</td><td>NOM</td><td rowspan="2">17dB over</td></tr>
<tr><td>MAX</td></tr>
<tr><td rowspan="2">4</td><td colspan="3" rowspan="2">Echo Loss (EL)</td><td>NOM</td><td rowspan="2">40dB over</td></tr>
<tr><td>MAX</td></tr>
<tr><td>5</td><td colspan="3">Sending Distortion (SD)</td><td colspan="2">refer to TABLE 30.3</td></tr>
<tr><td>6</td><td colspan="3">Receiving Distortion (RD)</td><td colspan="2">refer to TABLE 30.4</td></tr>
<tr><td rowspan="2">7</td><td colspan="3" rowspan="2">Idle Noise-Sending (INS)</td><td>NOM</td><td rowspan="2">-64dBm0p under</td></tr>
<tr><td>MAX</td></tr>
<tr><td rowspan="2">8</td><td colspan="3" rowspan="2">Idle Noise-Receiving (INR)</td><td>NOM</td><td>-47dBPA under</td></tr>
<tr><td>MAX</td><td>-36dBPA under</td></tr>
<tr><td rowspan="2">9</td><td colspan="3" rowspan="2">Sending Loudness Rating (SLR)</td><td rowspan="14">HEAD
SET</td><td>NOM</td><td rowspan="2">8±3dB</td></tr>
<tr><td>MAX</td></tr>
<tr><td rowspan="2">10</td><td colspan="3" rowspan="2">Receiving Loudness Rating (RLR)</td><td>NOM</td><td>-1±3dB</td></tr>
<tr><td>MAX</td><td>-12±3dB</td></tr>
<tr><td rowspan="2">11</td><td colspan="3" rowspan="2">Side Tone Masking Rating (STMR)</td><td>NOM</td><td rowspan="2">25dB over</td></tr>
<tr><td>MAX</td></tr>
<tr><td rowspan="2">12</td><td colspan="3" rowspan="2">Echo Loss (EL)</td><td>NOM</td><td rowspan="2">40dB over</td></tr>
<tr><td>MAX</td></tr>
<tr><td>13</td><td colspan="3">Sending Distortion (SD)</td><td colspan="2">refer to TABLE 30.3</td></tr>
<tr><td>14</td><td colspan="3">Receiving Distortion (RD)</td><td colspan="2">refer to TABLE 30.4</td></tr>
<tr><td rowspan="2">15</td><td colspan="3" rowspan="2">Idle Noise-Sending (INS)</td><td>NOM</td><td rowspan="2">-55dBm0p under</td></tr>
<tr><td>MAX</td></tr>
<tr><td rowspan="2">16</td><td colspan="3" rowspan="2">Idle Noise-Receiving (INR)</td><td>NOM</td><td>-45dBPA under</td></tr>
<tr><td>MAX</td><td>-40dBPA under</td></tr>
<tr><td rowspan="8">17</td><td rowspan="8">TDMA NOISE
–.GSM: Power Level: 5
DCS: Power Level: 0
(Cell Power: -90 ~ -105dBm)
–.Acoustic(Max Vol.)
MS/HEADSET SLR: 8±3dB
MS/HEADSET RLR: -13±1dB/-15dB
(SLR/RLR: mid-Value Setting)</td><td rowspan="4">MS</td><td rowspan="2">GSM</td><td>SEND</td><td colspan="2" rowspan="8">-62dBm under</td></tr>
<tr><td>REV.</td></tr>
<tr><td rowspan="2">DCS</td><td>SEND</td></tr>
<tr><td>REV.</td></tr>
<tr><td rowspan="4">Headset</td><td rowspan="2">GSM</td><td>SEND</td></tr>
<tr><td>REV.</td></tr>
<tr><td rowspan="2">DCS</td><td>SEND</td></tr>
<tr><td>REV.</td></tr>
</table>

2.8 Charging

• **Normal mode:** Complete Voltage: 4.2V
Charging Current: 600mA

• **Await mode:** In case of During a Call, should be kept 3.9V
(GSM: It should be kept 3.9V in all power level
WCDMA: It will not be kept 3.9V in some power level)

Extend await mode: At Charging prohibited temperature(-20C under or 60C over)
(GSM: It should be kept 3.7V in all power level
WCDMA: It will not be kept 3.7V in some power level)

3. Technical Brief

3.1 Digital Baseband(DBB) & Multimedia Processor

3.1.1 General Description

A. Features

• CPU ARM946 running at 104 MHz
  - 32 kB Instruction Cache, 16 kB Data Cache, 128 kB Instruction TCM and 128 kB Data TCM
  - 8 channel DMAC

• DSP C55x (LEAD3) Megastar (MGS3_2.0B) running at 170 MHz
  - 144 kWord ROM, 32 kWord DARAM, 32 kWord SARAM
  - 7 channel DMAC
  - Dedicated API channel to DSP memory (not locked up to other DMA channels)

• UMTS Access
  - Support for WCDMA/GSM Dual Mode
  - GSM/GPRS network signaling (from Layer 1 to 3)
  - WCDMA Ciphering and Integrity
  - High Speed Serial Link (HSSL) to the WCDMA Modem (at Layer 1)
  - GSM AMR
  - Multislot Class 8
  - HSCSD 14.4 kb/s

• MMI
  - Keypad Interface
  - Tone Generator Interface
  - Camera Data and Programmable Display Interfaces
  - Enhanced graphics support for QCIF display

• Operation and Services
- I²C™ Interface
- SIM Interfaces
- General Purpose I/O (GPIO) Interface
- External Memory Interface that supports FLASH, SRAM and PSRAM
- JTAG
- RTC
- ETM (in Prototype Package)

• Data Communication
- IrDA ® (SIR)
- UARTs (ACB, EDB (RS232))
- Slave USB

• Package
- 12 by 12 mm 289 pin FPBGA Production Package

3.1.2 Hardware Architecture

The hardware structure is delivered as five separate hardware macros to the top-level design, also depicted in Figure.

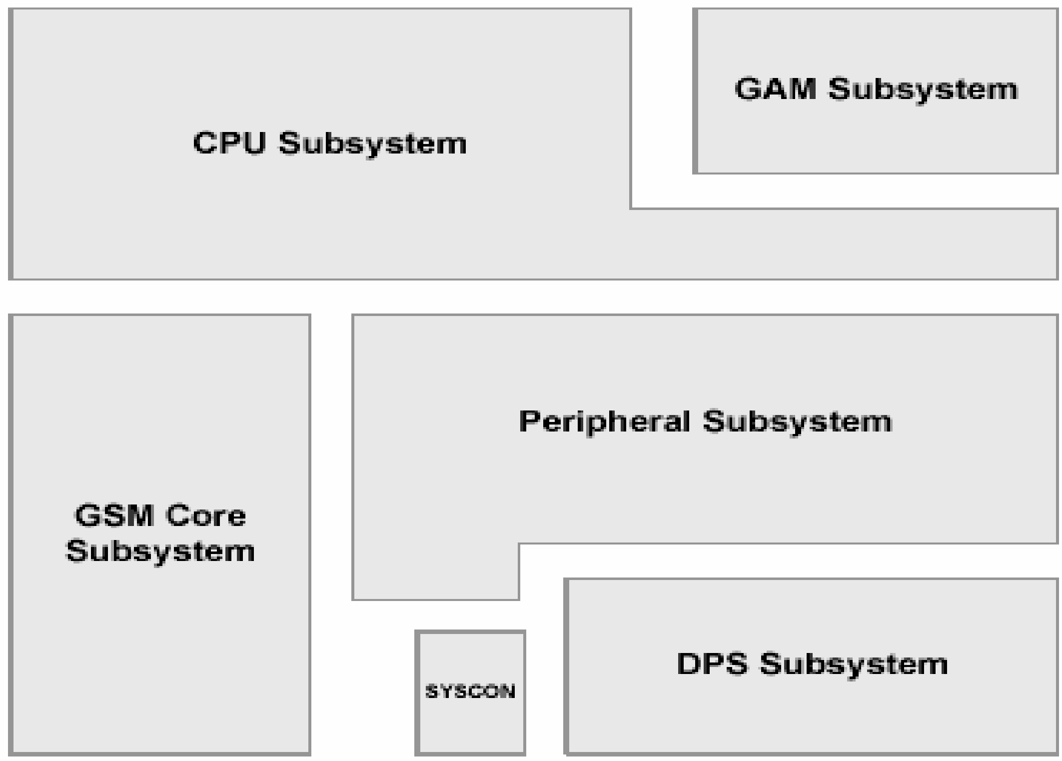


Figure. Simplified Block Diagram

A. Block Diagram

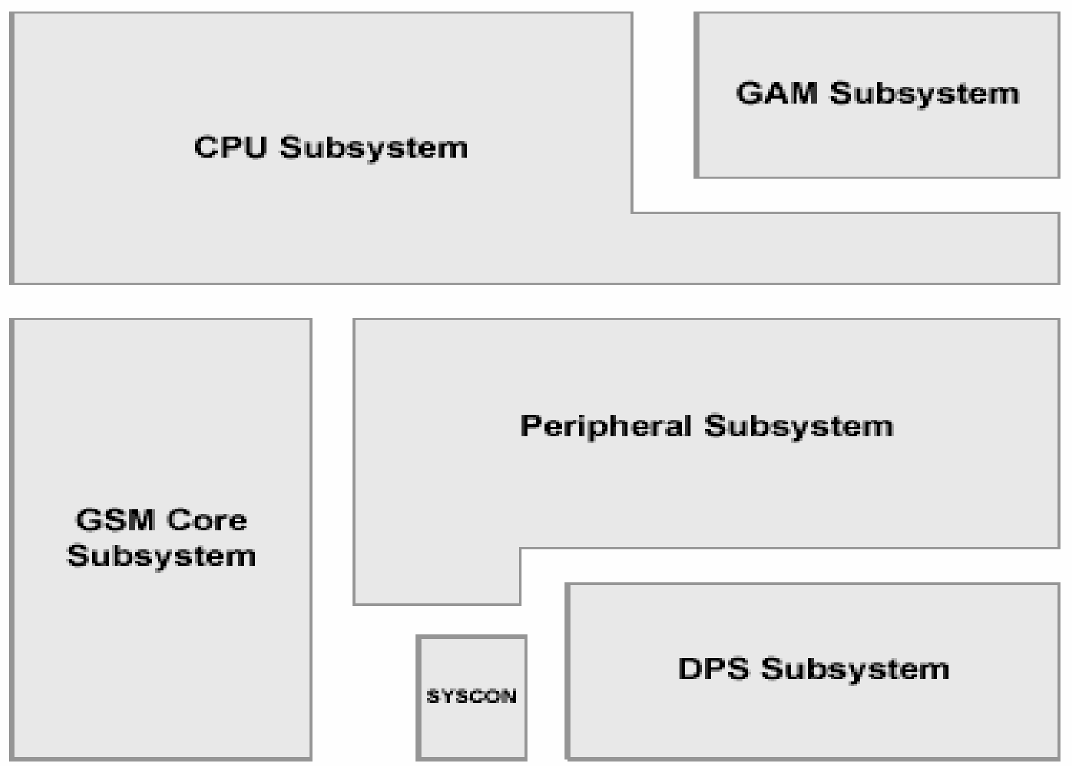


Figure. Simplified Block Diagram

B. CPU Hardware Subsystem

The CPU subsystem incorporates:
- CPU Sub chip
- Backplane
- JTAG
- DMA Controller
- System Buffer RAM
- Boot ROM
- External Memory Interface (EMIF) for connection to external SRAM and Flash memories.

The bus architecture is built on the ARM AMBA standard with multi-layer AHB (Advanced High-speed Bus) and APB (Advanced Peripheral Bus) for the peripheral buses.

There are two AHB busses, the CPU AHB and the DMA AHB.

Clocks to the CPU subsystem are distributed from the system control (SYSCON) backplane clocking.

The reset lines are all asynchronously asserted low and synchronously negated high.

The CPU subsystem has separate clocking and reset for the ARM946, AHB system, EMIF and DMAC.

C. Peripheral Hardware Subsystem

There are 29 peripherals within the peripheral hardware subsystem. With the exception of the USB, all hardware peripheral blocks are APB slave peripherals. From an architecture-hierarchy perspective, the SYSCON block is an APB slave on the slow APB bridge, but resides at the top level of the ASIC. The APB provides a simple interface to support low-performance peripherals.
Within the peripheral subsystem, there are four separate APB busses with AHB to APB (AHB2APB) bridges to the multi-layer AHB.

D. DSP Hardware Subsystem

The DSP subsystem provides support for processor intensive activity, such as voice coding and multimedia application support. The DSP subsystem includes the standard C55xTM Core (LEAD3) from Texas Instruments with associated memory system and peripherals.

E. GAM Hardware Subsystem

The Graphics Accelerator Module (GAM) subsystem provides hardware support in the creation of visual imagery and the transfer of this data to the display. GAM also provides support for the camera module. The visual data could be graphics, still images or video.
The GAM subsystem consists of five modules:

- GRAM - graphics memory (160 kB).
- GAMCON . GAM controller.
- GRAPHCON . graphics controller.
- PDI/SSI - programmable display interface for parallel/serial displays.
- CDI - camera data interface.

F. GSM Hardware Subsystem

The GSM subsystem is a stand-alone sub-chip incorporating GSM modem and interface to GSM radio together with memory control (MEMSYS) and internal RAM (IRAM).
The hardware peripheral blocks are RXIF, FCHDET, CRYPTO, EQU, NODI, 4 x CHD, GPRS CRYPTO, GPRS CRC24, CHE, DIRMOD, CLKCON, SERCON, TIMGEN, MEMSYS and IRAM.
The peripherals are accessible to the AHB (CPU-only) by an asynchronous I/O bridge.
The dual port IRAM is accessible to the AHB (CPU and DMA) by a synchronous AHB slave interface.

G. System Control Subsystem

The system controller subsystem (SYSCON) is primarily responsible for generating clock signals and distributing the clock and reset signals within the ASIC and certain external devices. The GSM core, GAM and DSP subsystems include their own system controllers that are sourced from SYSCON. SYSCON consists of analog and digital PLL clocks and a clock squarer. The block is a slave peripheral on the slow APB bus under control of the CPU.

The programming of SYSCON controls the fundamental modes of operation within the ASIC.

Individual blocks can also be reset and their clocks held inactive by accessing the appropriate control registers. SYSCON also controls the requesting protocol through which different sub-blocks in Ericsson DB 20000 can request clocks derived from the system clock.

The system controller also stores the chip-ID number in a read only register.

3.1.3 External memory interface

There are four independent chip selects (CS0, CS1, CS2, CS3) provided for external memories and each has an address range of 256 Mb.
RF calibration data, Audio parameters and battery calibration data etc are stored in flash memory area.

A. U8100 & U8110

- 384Mb flash memory + 64Mb PSRAM
- 4-CS(Chip Select) are used

Interface Spec.						
Device	Part Name	Maker	Read Access Time			Write Access Time
			Async	Page	Burst	
MCP	S71WS256HC0BAW00	AMD	56 ns	–	13.5 ns at 54MHz	56 ns
FLASH	Am29BDS128HD9VKI	AMD	56 ns	–	13.5 ns at 54MHz	70 ns
PSRAM	S71WS256HC0BAW00	AMD	70 ns	20 ns	–	70 ns

Table External memory interface for U8100 & U8110

B. U8120

- 512Mb flash memory + 64Mb PSRAM
- 3-CS(Chip Select) are used

Interface Spec.						
Device	Part Name	Maker	Read Access Time			Write Access Time
			Async	Page	Burst	
MCP	RD38F4050L0YTQ0	Intel	85 ns	25 ns	14 ns at 54MHz	85 ns
FLASH	NZ48F4000L0YBQ0	Intel	85 ns	25 ns	14 ns at 54MHz	85 ns
PSRAM	RD38F4050L0YTQ0	Intel	85 ns	25 ns	10 ns at 66MHz	85 ns

Table External memory interface for U8120

3.1.4 RF Interface

A. MARITA Interface

Marita controls GSM RF part using these signals through GSM RF chip-Ingela.

- RFCLK, RFDAT, RFSTR : Control signals for Ingela
- TXON, RXON : Control signals for TX and RX part of Ingela
- PCTL : Control signal for GSM TX PAM
- BANDSEL0 : Band selection signal for GSM or DCS
- ANTSW[0:3] : Control signals for antenna switch
- DCLK, IDATA, QDATA : GSM/DCS RX Data
- DIRMOD[A:D] : GSM/DCS TX Data

RF I/F

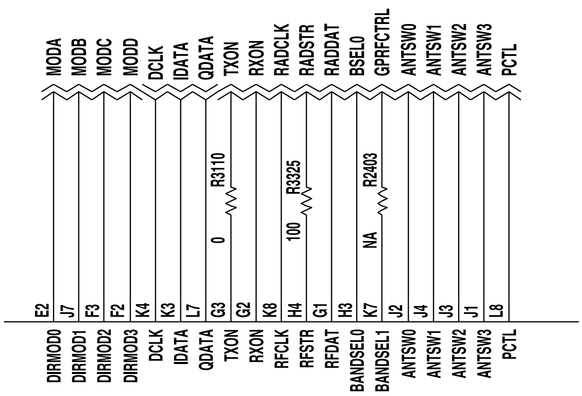


Figure. Schematic of MARITA RF Interface

B. WANDA Interface

Wanda controls WCDMA RF part using these signals through W-CDMA RF chip-Wopy & Wivi.

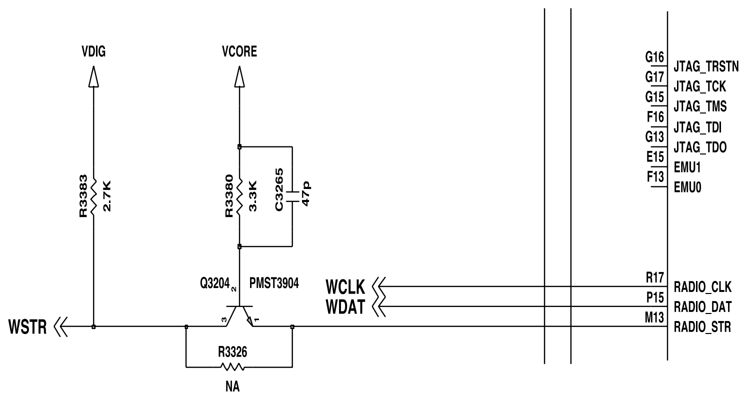


Figure. Schematic of WANDA RF Interface

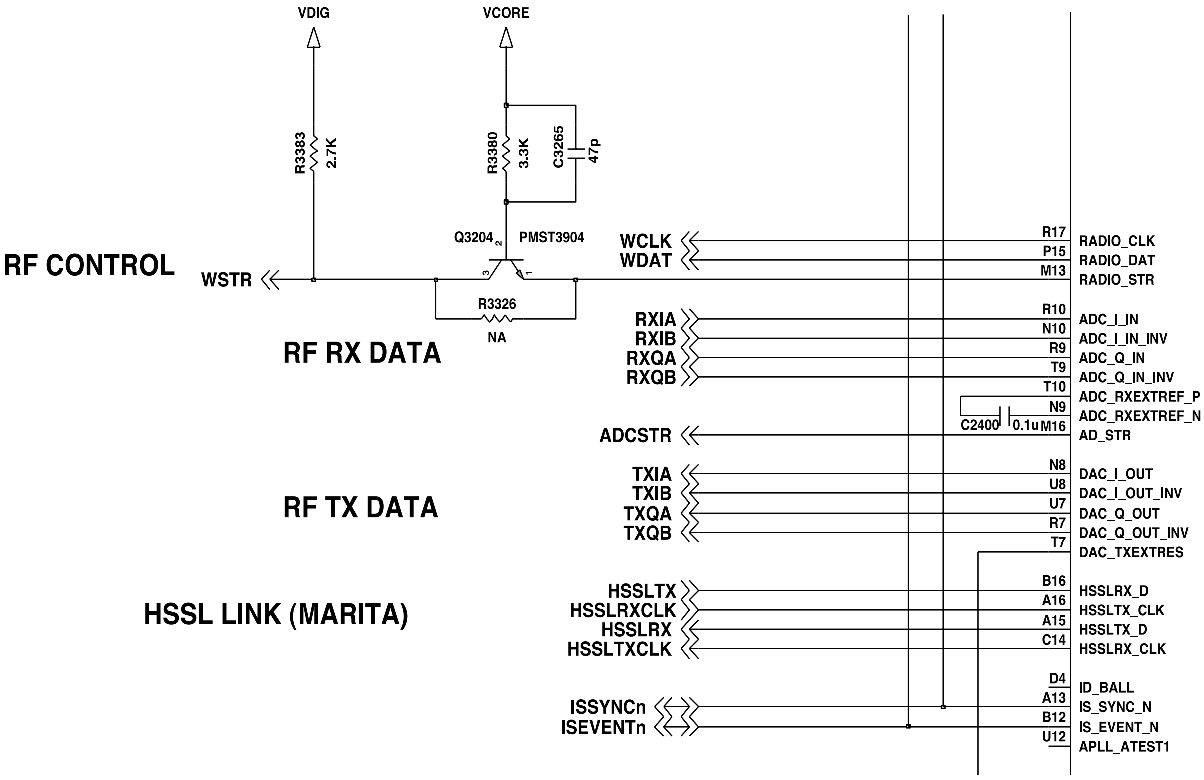


Figure. Schematic of WANDA RF Interface

- RADIO_CLK, RADIO_DAT, RADIO_STR : Control signals for Wivi & Wopy
- RXIA, RXIB, RXQA, RXQB : WCDMA RX Data
- TXIA, TXIB, TXQA, TXQB : WCDMA TX Data
- HSSLRX_D, HSSLRX_CLK : Marita & Wanda Communication Signal
- HSSLTX_D, HSSLTX_CLK : Marita & Wanda Communication Signal

3.1.5 SIM Interface

SIMDAT0, SIMCLK0, SIMRST0 ports are used to communicate DBB(MARITA) with ABB(VINCENNE) and filter.

SIM (Interface between DBB and ABB)	
SIMDAT0	SIM card bidirectional data line
SIMCLK0	SIM card reference clock
SIMRST0	SIM card async/sync reset

Table. SIM Interface

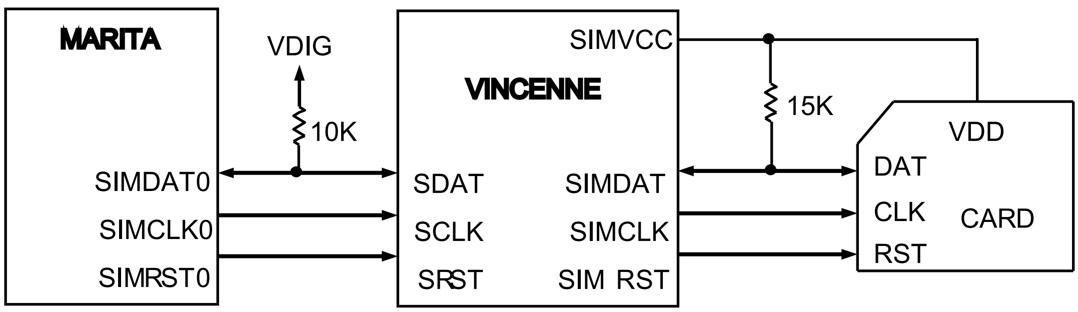


Figure. SIM Interface

3.1.6 UART Interface

UART signals are connected to MARITA GPIO through IO connector

UART0		
Resource	**Name**	**Note**
GPIO10	UARTRX0	Transmit Data
GPIO11	UARTTX0	Receive Data
UART1		
GPIO14	UARTRX1	Transmit Data (UART1)
GPIO15	UARTTX1	Receive Data (UART1)
GPIO16	UARTRTS1	Request To Send
GPIO17	UARTCTS1	Clear To Send

Table. UART Interface

3.1.7 GPIO (General Purpose Input/Output) map

In total 40 allowable resources. This model is using 25 resources.
GPIO Map, describing application, I/O state, and enable level are shown in below table.

IO #	Application	IO	Resource	Inactive State	Active State
GPIO00	Not used	–	–	–	–
GPIO01	BL_PWL	O	GPIO	Low	High
GPIO02	7C_LED_VDD_EN	O	GPIO	Low	High
GPIO03	PULSESKIP (Not used)	I	GPIO	–	–
GPIO04	CAMERA_DET	I	GPIO	High	Low
GPIO05	GPIO05 (Not used)	O	–	–	–
GPIO06	AMPCTR	O	GPIO	Low	High
GPIO07	TGBUZZ (Not used)	O	GPIO	Low	High
GPIO10	UARTRX0	I	UART0	High	Low
GPIO11	UARTTX0	O	UART0	High	Low
GPIO12	Not used	–	–	–	–
GPIO13	Not used	–	–	–	–
GPIO14	UARTRX1	I	UART1	High	Low
GPIO15	UARTTX1	O	UART1	High	Low
GPIO16	UARTRTS1	I	UART1	High	Low
GPIO17	UARTCTS1	O	UART1	–	–
GPIO20	CAM_REG_EN	O	GPIO	Low	High
GPIO21	CAM_FLASH_ON	O	GPIO	Low	High
GPIO22	TP2125 (Not used)	–	–	–	–
GPIO23	CAM_FLASH_SHOT	O	GPIO	Low	High
GPIO24	Not used	–	–	–	–
GPIO25	Not used	–	–	–	–
GPIO26	Not used	–	–	–	–
GPIO27	Not used	–	–	–	–
GPIO30	Not used	–	–	–	–
GPIO31	Not used	–	–	–	–

IO #	Application	IO	Resource	Inactive State	Active State
GPIO32	KEY_LED_ONOFF	O	GPIO	Low	High
GPIO33	Not used	–	–	–	–
GPIO34	Not used	–	–	–	–
GPIO35	LCDVSYNCI (Not used)	I	GPIO	Low	High
GPIO36	SPKMUTE	O	GPIO	LOW (Ear piece)	HIGH (Speaker)
GPIO37	Not used	–	–	–	–
GPIO40	USBSENSE	I	GPIO	Low	High
GPIO41	Not used	–	–	–	–
GPIO42	BL_EN	O	GPIO	Low	High
GPIO43	FOLDER_DET	I	GPIO	High	Low
GPIO44	EN_LED_R	O	GPIO	Low	High
GPIO45	EN_LED_G	O	GPIO	Low	High
GPIO46	EN_LED_B	O	GPIO	Low	High
GPIO47	IRDA_REG_CTRL	O	GPIO	Low	High

Table. MARITA GPIO Map Table

3.1.8 USB

The USB block supports the implementation of a "full-speed" device fully compliant to USB 2.0 standard. It provides an interface between the CPU (embedded local host) and the USB wire, and handles USB transactions with minimal CPU intervention.
The USB specification allows up to 15 pairs of endpoints. Data for each endpoint is buffered in RAM within the USB block and is read/written from the endpoint FIFO using DMA transfers or FIFO register access. High-speed (high throughput) endpoints can use DMA while slower endpoints can use FIFO register access.
The USB block can request up to six DMA channels, three for IN endpoints and three for OUT endpoints.

USB Function	Note
USBDP	USB differential (+) line
USBDM	USB differential (-) line
USBSENSE (GPIO40)	USB detection (input)
USBPUEN	USB pull-up control
VDDUSB	Power supply for MARITA USB block

Table. USB Signal Interface of MARITA

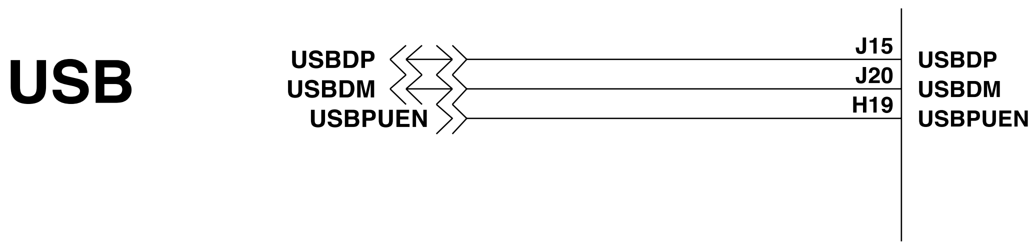


Figure. Schematic of MARITA USB block

USB regulator input voltage is 5V and uses external USB device power through IO Connector.
Output voltage is 3.3V and supply to MARITA USB block.
USB is detected by MARITA GPIO40(USBSENES).

• VUSB / (10K + 51K) = VUSBSENSE / 51K

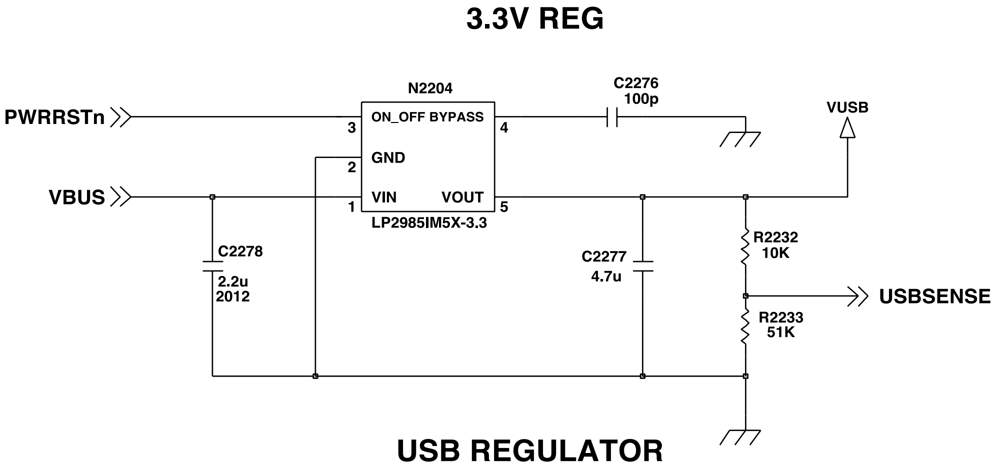


Figure. Schematic of USB Regulator

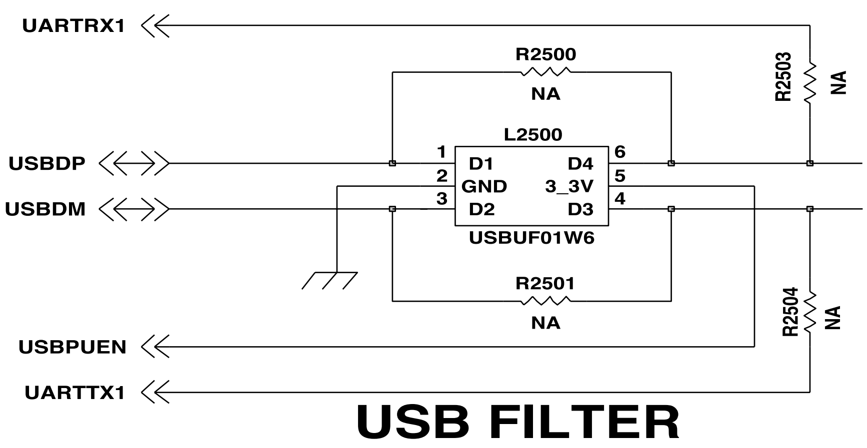


Figure. Schematic of USB filter

3.1.9 IrDA Interface

MARITA supports FIR, MIR and SIR mode.
In this model, the IrDA block supports SIR (Standard IrDA) mode.
SIR supports data rates up to 115,200 bps, including 9,600/19,200/38,400/57,600 bps.
In this mode, IrDA uses eight data bits per character and one stop bit.
IrDA supports a protocol defined by the IrDA Association.

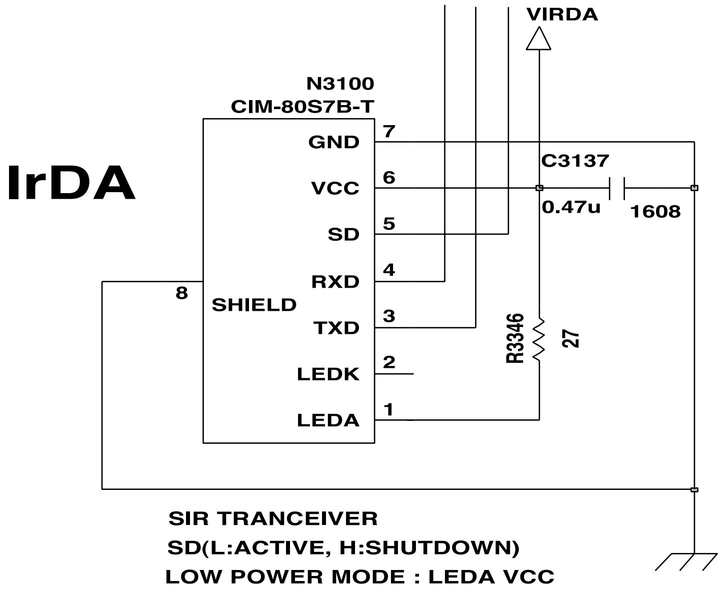


Figure. Schematic of MARITA IrDA Interface

3.1.10 Folder ON/OFF Operation

There is a magnet to detect the folder status, opened or closed.
If a magnet is close to the hall-effect switch (U1 on keypad), the voltage at pin2 of U1 goes to 0V. Otherwise, 2.8V.
This folder signal is delivered to MARITA GPIO43.

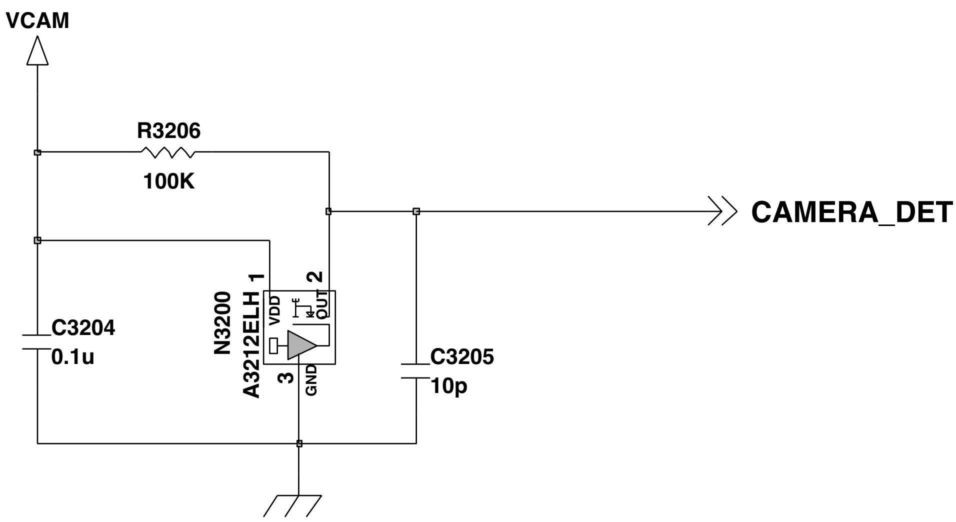


Figure. Schematic of MARITA IrDA Interface

3.1.11 Power On Sequence

① User press END key and ONSWAn signal is changed to Low.
② VINCENNE initiate the internal oscillator and power up the regulators.
③ VINCENNE generate a power for MARITA.
④ VINCENNE release the power reset signal(PWRRSTn) and generate an interrupt(IRQ0n) to MARITA.

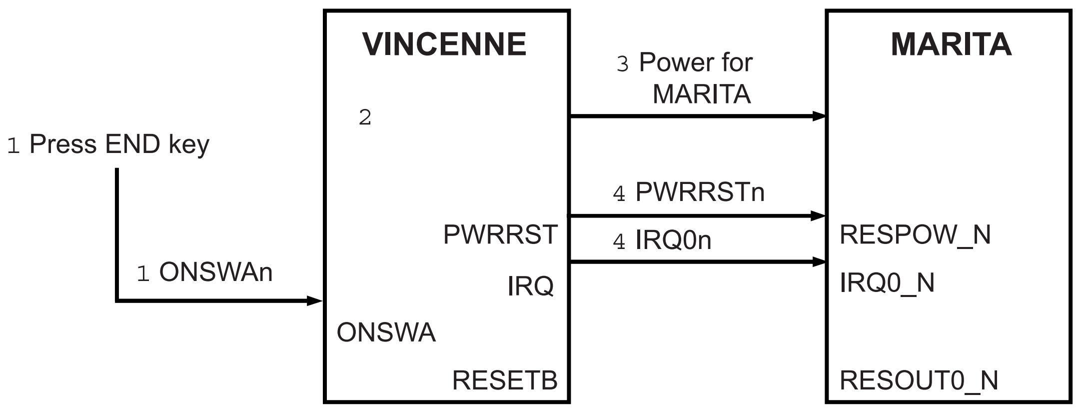


Figure. Power On Sequence

3.1.12 Key Pad

There are 26 buttons and 3 side keys in Figure 3-xx.Shows the Keypad circuit.‘END’ Key is connected ONSWAn from Vincenne.

	KEYIN0	KEYIN1	KEYIN2	KEYIN3	KEYIN4
KEYOUT0		SIDE1	SIDE2	SIDE3	
KEYOUT1	1	4	7	*	UP
KEYOUT2	2	5	8	0	DOWN
KEYOUT3	3	6	9	#	RIGHT
KEYOUT4	SEND	CLEARER	BACK	GAME	LEFT
KEYOUT5	MENU	SEARCH	MULTI	CAM	OK

Table Key Matrix Mapping Table

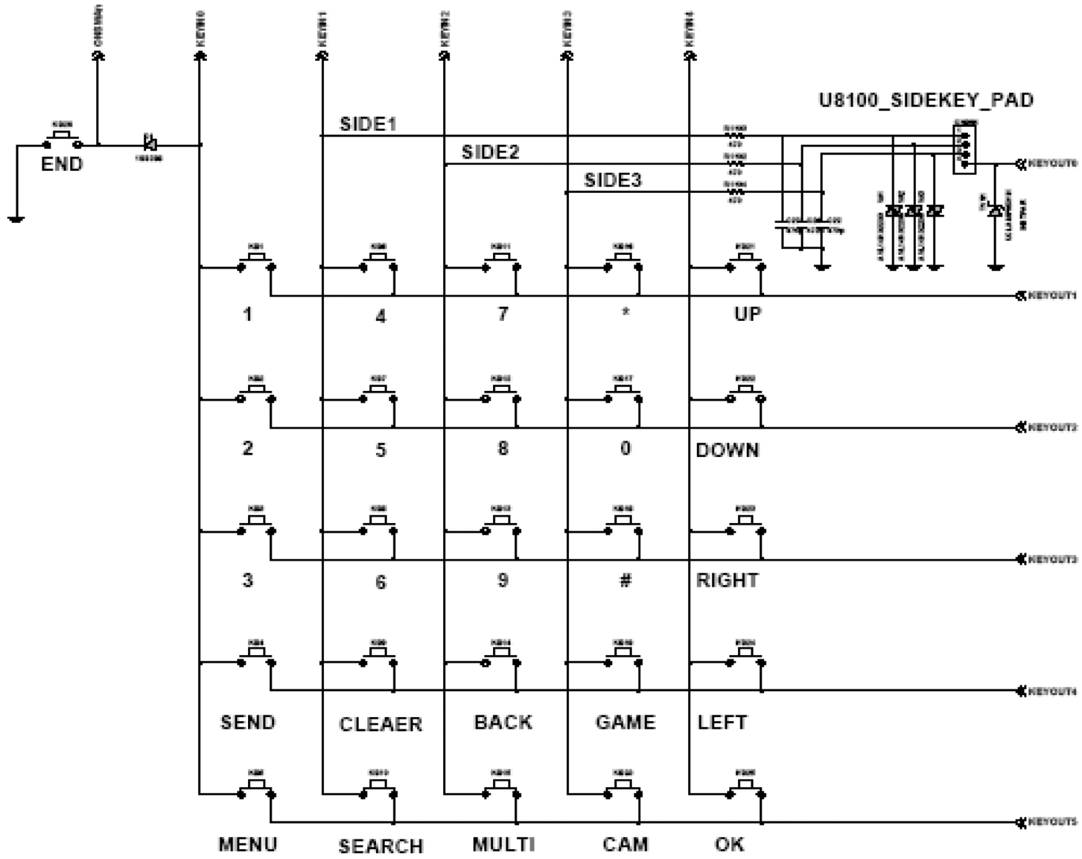


Figure. Power On Sequence

3.2 GAM Hardware Subsystem

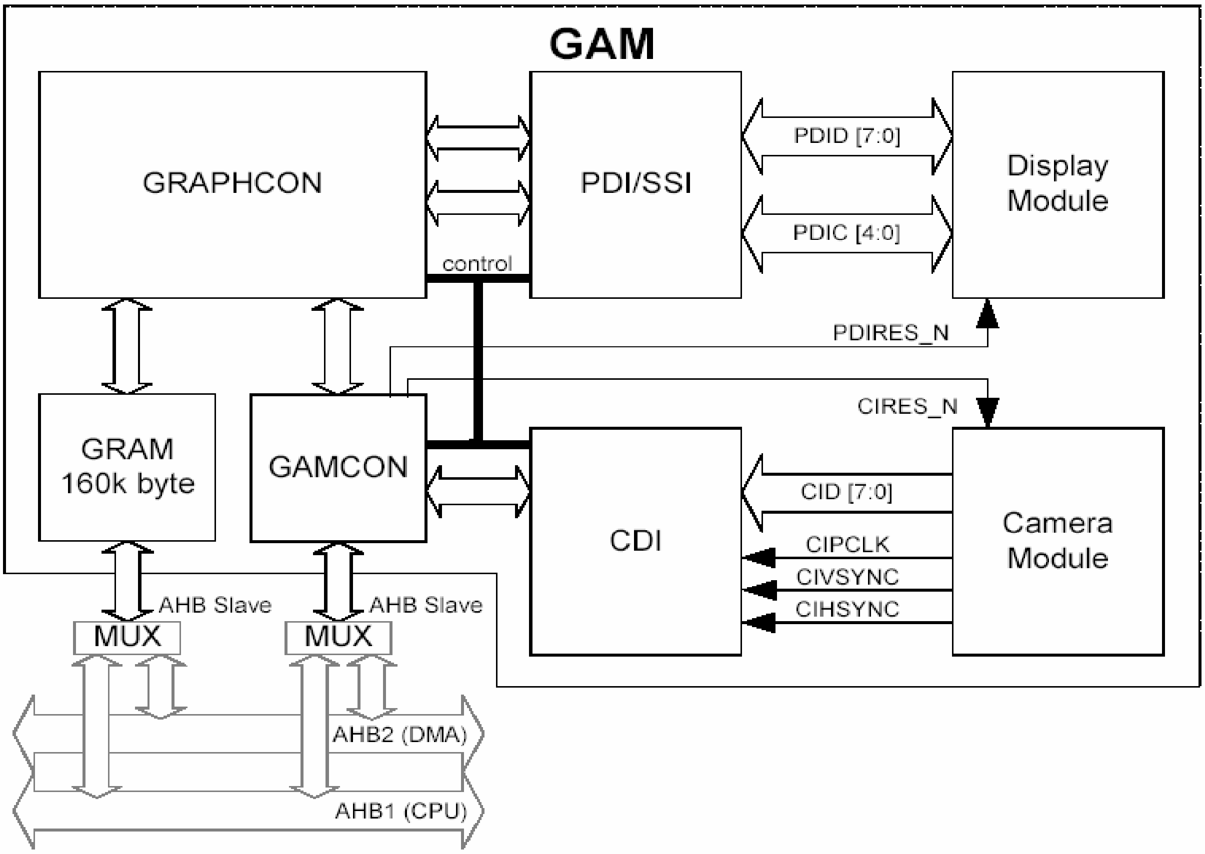


Figure. GAM Subsystem Functional Block Diagram

3.2.1 General Description

The Graphics Accelerator Module (GAM) subsystem provides hardware support in the creation of visual imagery and the transfer of this data to the display. GAM also provides support for the camera module. The visual data could be graphics, still images or video. The GAM subsystem consists of five modules:

- GRAM - graphics memory (160 kB).
- GAMCON . GAM controller.
- GRAPHCON . graphics controller.
- PDI/SSI - programmable display interface for parallel/serial displays.
- CDI - camera data interface.

3.2.2 Block Description

GAM Controller(GAMCON)

The GAM Controller (GAMCON) is responsible for clock gating and distribution within the GAM module. GAMCON receives the HCLK from SYSCON and distributes to GRAPHCON, GRAM, PDI and CDI. GAMCON also distributes the GAM reset signal to GRAPHCON, GRAM, PDI and CDI. The reset signals CIRES_N and PDIRES_N are distributed from GAMCON to the camera and display module respectively, see Figure. The CIPCLK is used to clock the received data into the camera data interface. The CIPCLK can be in the range of 100 kHz to 16 MHz.

Graphics RAM (GRAM) Block

GAM includes 160 kB of graphics memory (GRAM) in order to support display screen sizes of QCIF + alfa display size and three frame buffers when decoding QCIF video.
The GRAM can be accessed in 8, 16 or 32-bit mode. Write access takes a single AHB clock cycle. Non-sequential read and the first access of a sequential read access takes two AHB clock cycles. Subsequent sequential read access take a single AHB clock cycle.
The GRAM contains both frame buffer and temporary data. There are three image areas with one used for normal MMI graphics and the other two areas used for still images, video frames or camera frames. The three image areas can be combined into one frame buffer.
GRAM is required to transfer a VGA (640 by 480 pixels) image from the camera data interface (CDI) over DMA at 100 MBit/s, within a 50 ms timeframe. The GRAM is used as a buffer, but the average transfer bandwidth required is approximately 3 Mword/s (32-bit word), that is 12 MByte/s.

Graphics Controller (GRAPHCON) Block

GRAPHCON is controlled by the application CPU and can perform operations on pixels and image areas. Images can be moved and merged with other images and text.
The GRAPHCON block receives graphical objects from GRAM and performers the appropriate graphical manipulation. The resulting data is transfers to the display interface (PDI). GRAPHCON can receive images from the camera data interface (CDI) and send them to the PDI automatically.
GRAPHCON performs conversion from YUV to RGB and can scale (zoom) still or video images.

Programmable Display Interface (PDI) Block

The programmable display interface (PDI) is designed to interface both parallel and serial display modules. The display data is transferred from the 32 word FIFO on GAMCON to the display module via the PDI block. The PDI block is built around a micro controller and executes 16-bit instruction words to individually control the I/O ports. It has a 128 byte program memory, programmable by the CPU, which can store up to 64 instructions.
The CPU transfers all set-up and control data to the display. Data is transferred to PDI as 32-bit words, which in turn writes 8-bit data to the display. The programmable PDI block is configured at the software build stage, to support either parallel interface such as PPI or serial interface such as SSI or I2C.

Camera Data Interface (CDI) Block

The camera data interface (CDI) block is designed to support a range of still image camera modules. An 8-bit parallel bus supports data transfer from the camera module to the CDI.

The pixel clock is an output clock from the camera module to the CDI and qualifies the data on the parallel bus. One byte of data is captured on each rising edge of the pixel clock. CDI allows the pixel clock to be in the range of 100 kHz to 16 MHz.

The horizontal synchronization line is an input from the camera module and defines one scan-line of image data. The horizontal synchronization line can be programmed to be active high or low. The vertical synchronization line is an input from the camera module and defines one image frame (image height) of data. The vertical synchronization line can be programmed to be active high or low.

The frame rate can be adjusted by skipping frames and various interrupts are used to inform the application CPU regarding the progress of incoming images and potential errors. The normal data format on the data bus is YUV 4:2:2 (raw binary image data) according to the CCIR-656 standard. A function within the CDI can be programmed to reorder the YUV parameters as they pass through the CDI. In addition, the CDI is able to detect the end of an image and perform some truncation as well as overflow conditions. There is nothing preventing the use of other data types such as JPEG or RGB (as long as the timing is followed), but only YUV data can be sent to the display.

Camera images can also be sent to a DMA channel to store the image in external memory.The I2C interface and GPIO are part of the interface to the camera module, but they are not part of the CDI block. The I2C is used to set-up and control the camera module.

The camera module I2C lines must go high impedance when the supply is removed from the camera. The I2C commands needed to control the camera, as well as the functional behavior of the module, are also different for each implementation.

The ON-signal (GPIO) is used to power-on the camera from Standby or Off mode (implementation dependent). This signal must be held low when the mobile equipment is powered down and during the mobile equipment reset period. The GPIO pin can also be an input or high impedance during mobile equipment reset and start. In this case, it must have pull-down to ground.

The camera module reset signal is an output to the camera module.

3.2.3 Camera & Camera FPC Interface

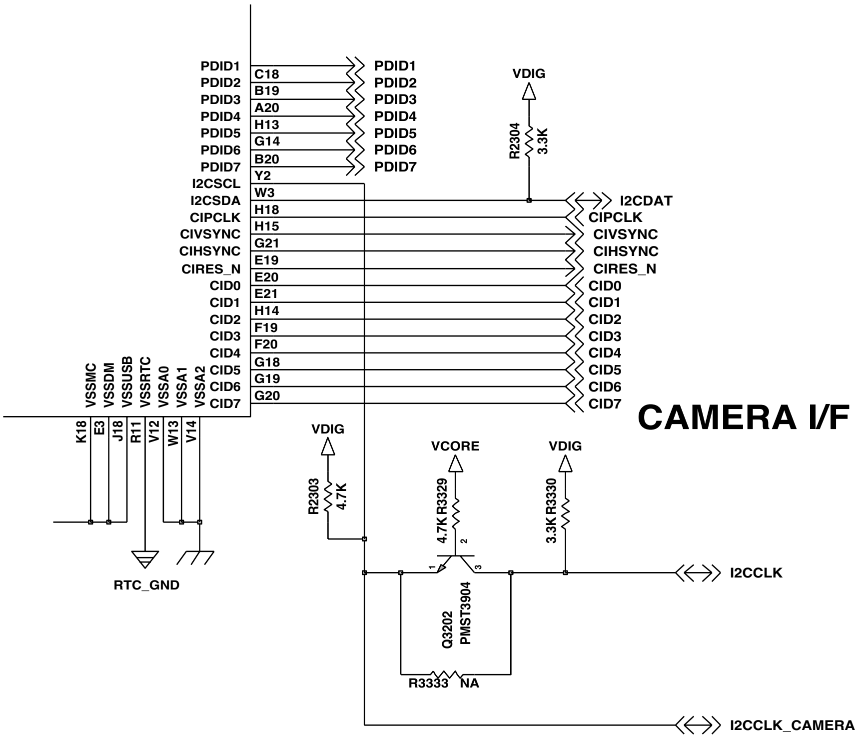
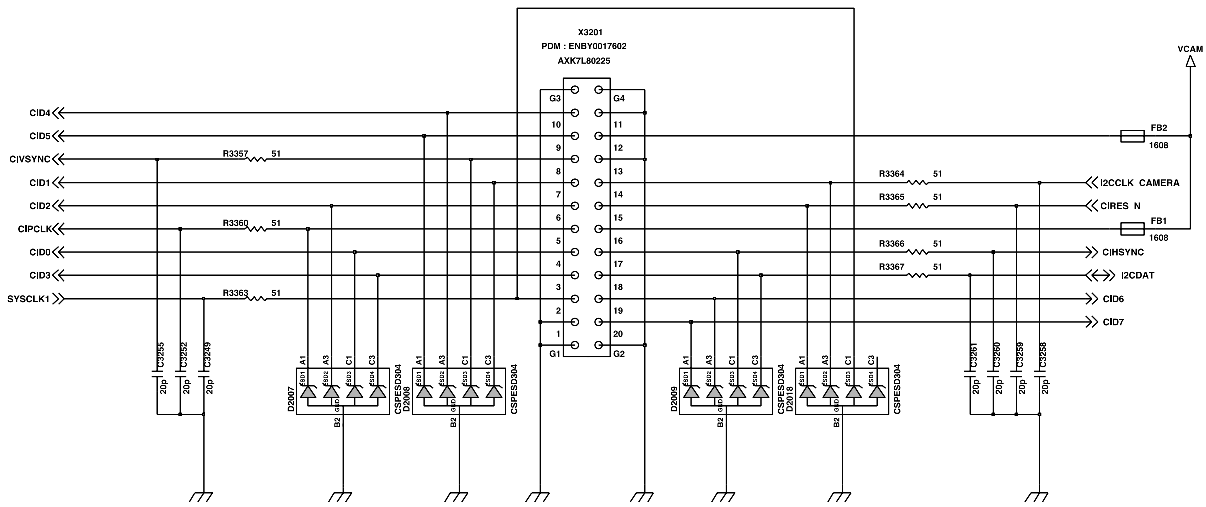


Figure. Camera Interface (in Marita)



CAMERA I/F

Figure. Camera Board to Board Connector

The Camera module is connected to main board with 20pin Board to Board connector (AXK7L80225). Its interface is dedicated camera interface port in Marita. The camera port supply 24MHz master clock to camera module and receive 12MHz pixel clock (30fps), vertical sync signal, horizontal sync signal, reset signal and 8bits YUV data from camera module. The camera module is controlled by I2C port.

NO	Pin Name	Pin Type	Description
1	DOUT4	DO	Image data output
2	DOUT5	DO	Image data output
3	VD	DO	Vertical Synchronization Pulse Output
4	DOUT1	DO	Image data output
5	DOUT2	DO	Image data output
6	DCLK	DO	Clock for Output Data
7	DOUT0	DO	Image data output
8	DOUT3	DO	Image data output
9	EXTCLK	DI	External Clock Input
10	GND		Ground
11	FSSTB	DO	Strobe Pulse for Flash
12	DVDD		VDD for the Digital Circuit
13	GND		Ground
14	SCL		Clock for IIC bus Command
15	RESET	DI	Reset Terminal
16	AVDD		VDD for the Sensor and PLL
17	HD	DO	Horizontal Synchronization Pulse Output
18	SDA		Clock for IIC bus Command
19	DOUT6	DO	Image data output
20	DOUT7	DO	Image data output

Table. Interface between Camera Module and Main Board (in camera module)

3.2.4 Camera Position Detection

GPIO_04 detects the Camera Position (front or back)

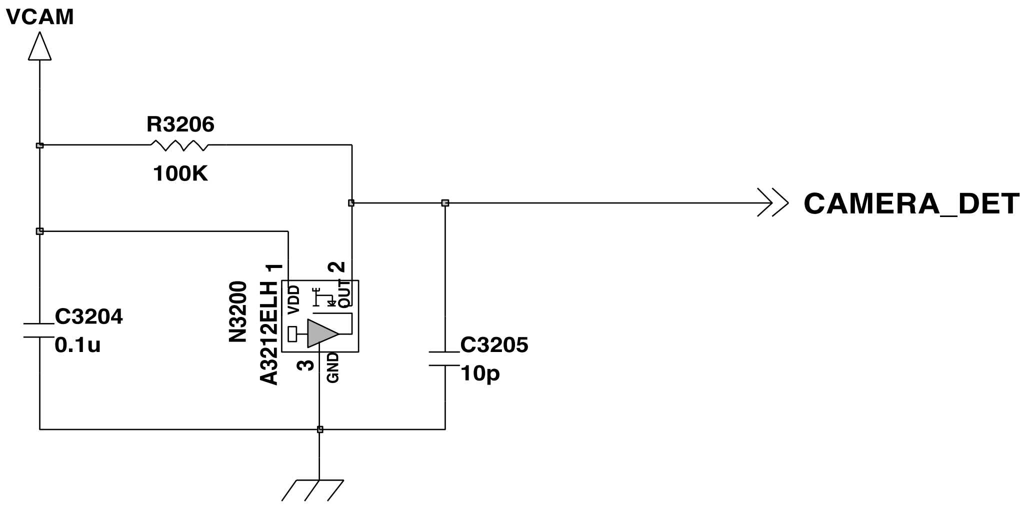


Figure. Camera Position Detection

3.2.5 Camera Regulator

GPIO_20 enables Camera Regulator Operation

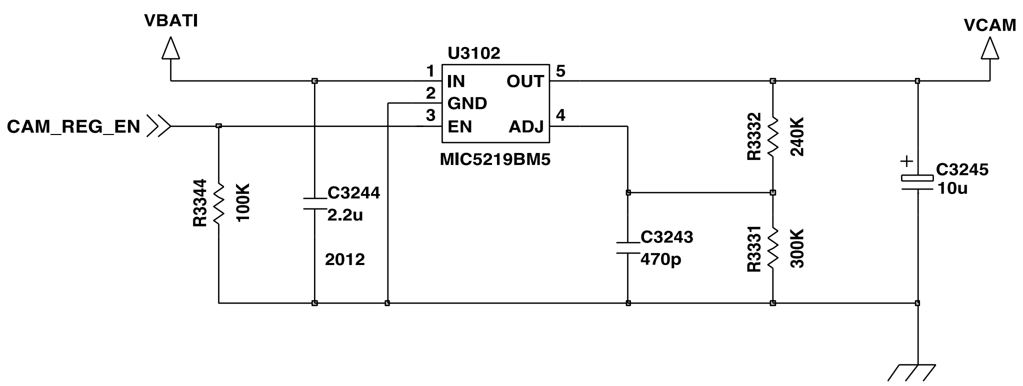


Figure. Camera Regulator

3.2.6 Display & LCD FPC Interface

LCD module include device in table 3-2

Device	Type
Main LCD	176 x RGB x 220 65K Color TFT LCD
Sub LCD	96 x 64 Mono FSTN LCD
Main LCD Backlight	White LED
Sub LCD Backlight	7 color LED

Table. Devices in LCD Module

LCD module is connected to key board with 40-pin BtoB connector (CONN_40_AXK840145J) and Speaker, Receiver, Vibrator, Camera Flash is connected by soldering the leads to 9 pads in LCD module.
The Main LCD is controlled by 8-bit PDI(Parallel Data Interface) in Marita and Sub LCD is controlled by 8-bit PDI in Marita.

PIN	SYMBOL	FUNCTION	I/O	REMARKS
SPK TERMINAL				
1	EARP	Ear Piece Plus	O	
2	EARM	Ear Piece Minus	O	
3	SPKP	Loud Speaker Plus	O	
4	SPKM	Loud Speaker Minus	O	
MOTOR TERMINAL				
1	MOTOR_BATT	MOTOR Power	O	
2	MOTOR_GND	MOTOR Ground	O	
CAMERA FLASH TERMINAL				
1	VOUT_F1	FLASH Power	O	
2	VSIG_F2	FLASH Signal	O	
3	F3	Dummy Ground	O	

Table. Interface between LCD module and Speaker, Receiver, Vibrator, Flash

PIN	SYMBOL	FUNCTION	I/O	REMARKS
1	GND	Ground		
2	CAM_FLASH_SHOT	Turn ON the Camera Flash Shot		
3	MOTOR_BATT	MOTOR Power		
4	SPKP	Loud Speaker Plus		
5	SPKM	Loud Speaker Minus		
6	EN_LED_G	Enable Signal for Sub LCD Backlight LED(Green)		
7	7C_LED_VDD	Power Supply for Sub LCD Backlight		
8	BL_EN	Enable Signal for Main LCD Backlight		
9	PDID0	Parallel Data 0 bit for Main/Sub LCD		
10	PDID2	Parallel Data 2 bit for Main/Sub LCD		
11	PDID4	Parallel Data 4 bit for Main/Sub LCD		
12	PDID6	Parallel Data 6 bit for Main/Sub LCD		
13	LCDRDX	Read Signal for Main/Sub LCD status		
14	LCDRS	Register Select Pin		
15	LCDCSX_SUB	Chip Select Signal for Sub LCD		
16	LCDVSYNCI	Main LCD Vertical Synch. Signal		
17	GND	Ground		
18	GND	Ground		
19	GND	Ground		
20	GND	Ground		
21	GND	Ground		
22	GND	Ground		
23	VDIG_2.8V	Power Supply for system and I/O Logic(2.8V)		
24				
25	LCDERESX	Reset Signal for Main/Sub LCD		
26	LCDCSX_MAIN	Chip Select Signal for Main LCD		
27	LCDWRX	Write Signal for Main/Sub LCD		
28	PDID7	Parallel Data 7 bit for Main/Sub LCD		
29	PDID5	Parallel Data 5 bit for Main/Sub LCD		

PIN	SYMBOL	FUNCTION	I/O	REMARKS
30	PDID3	Parallel Data 3 bit for Main/Sub LCD		
31	PDID1	Parallel Data 1 bit for Main/Sub LCD		
32	BL_PWL	Main LCD PWL signal		
33	VBATI_4.2V	Battery Power(4.2V)		
34	EN_LED_B	Enable Signal for Sub LCD Backlight LED(Blue)		
35	EN_LED_R	Enable Signal for Sub LCD Backlight LED(Red)		
36	EARP	Ear Piece Plus		
37	ERAM	Ear Piece Minus		
38	GND	Ground		
39	CAM_FLASH_ON	Turn ON the Camera Flash Continuous ON		
40	GND	Ground		

Table. Interface between LCD module and main board(in LCD Module)

3.2.7 Main LCD Backlight Illumination

There are 4 white LEDs in Main LCD Backlight circuit which are driven by 4.5V Regulated Output Charge Pump(SC604). GPIO_01(BL_PWL) is used for Backlightbrightness control.

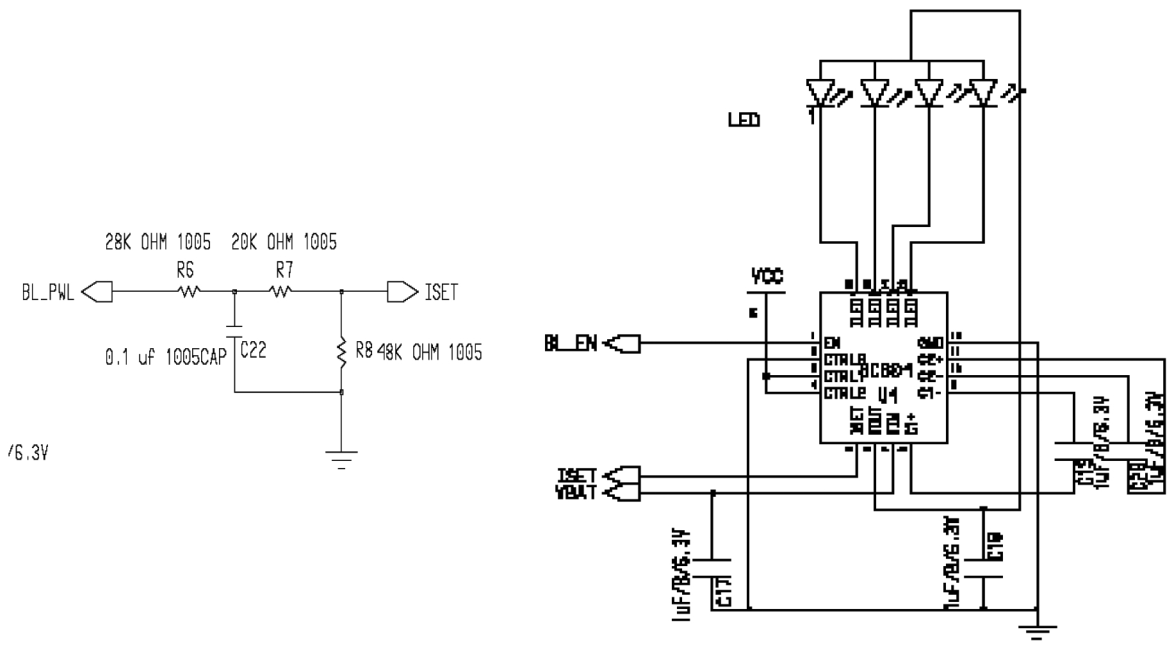


Figure. Charge Pump Circuit for Main LCD Backlight

* LED : SSC-HWTS902(Seoul Semiconductor)

3.2.8 Sub LCD Backlight Illumination

GPIO_02(7C_LED_VDD_EN) in Marita enables 7 color LED. 7 color LED consists of Red LED, Green LED and Blue LED. GPIO_44(EN_LED_R), GPIO_45(EN_LED_G) and GPIO_46(EN_LED_B) in Marita does ON or OFF its own LEDs.

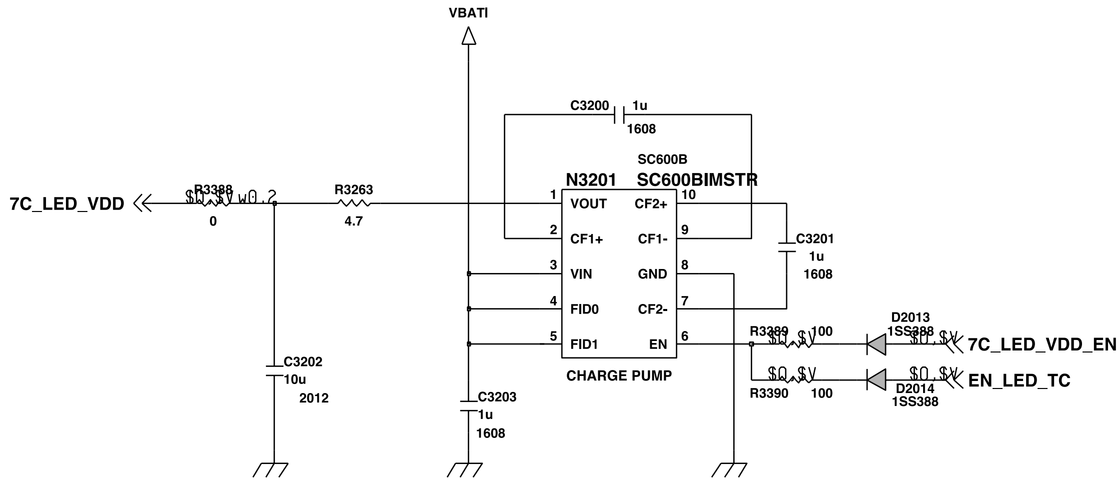


Figure. Sub LCD Backlight 4.5V

In case of power off mode, if TA is inserted, Red LED is turned-on.

3.2.9 Keypad Illumination

There are 19 blue LEDs in key board backlight circuit, which aredriven by GPIO_32 (KEY_LED_ONOFF) line form Marita.

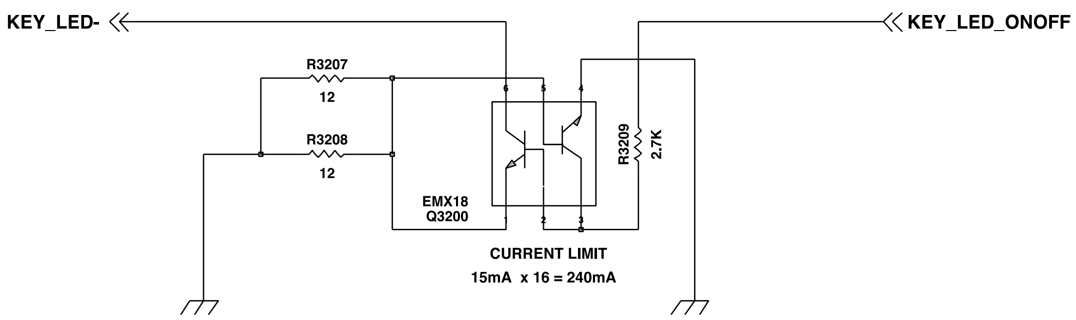


Figure. Keypad Backlight Blue LED Interface

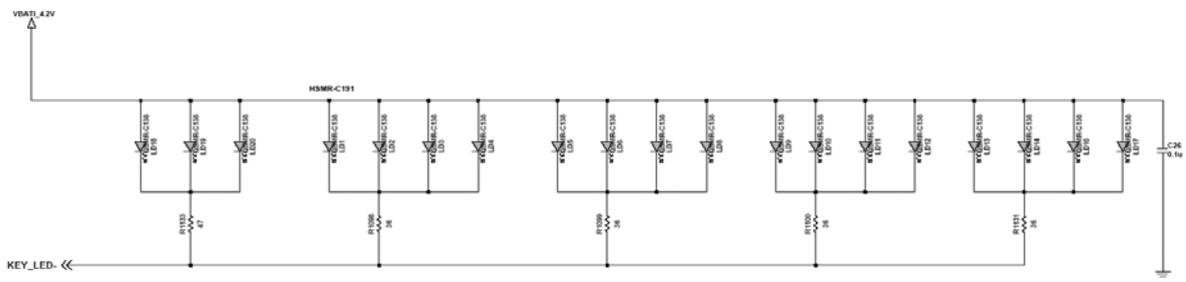


Figure. Keypad Backlight Circuit

3.2.10 Camera Flash Illumination

Camera Flash illumination circuit make 3 modes using white LED. Mode 1. Is Continuous ON mode using GPIO_21(CAM_FLASH_ON), Mode 2. Is Flash Shot using GPIO_23(CAM_FLASH_SHOT) and Mode 3. combines Mode 1. and Mode 2.

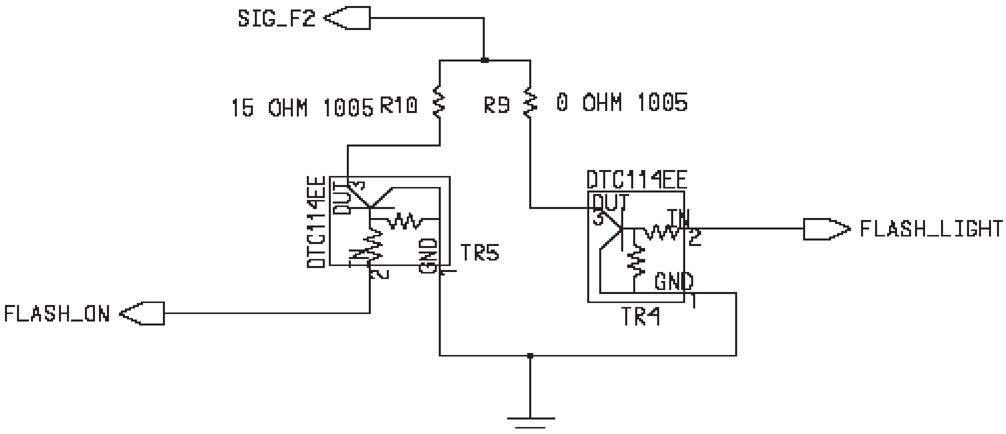


Figure. Camera Flash Circuit

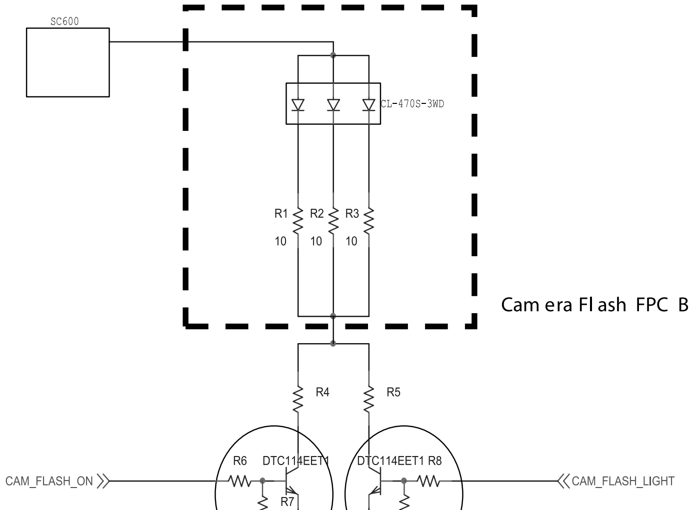


Figure. Camera Flash FPCB & Circuit

3.3 LCD Module

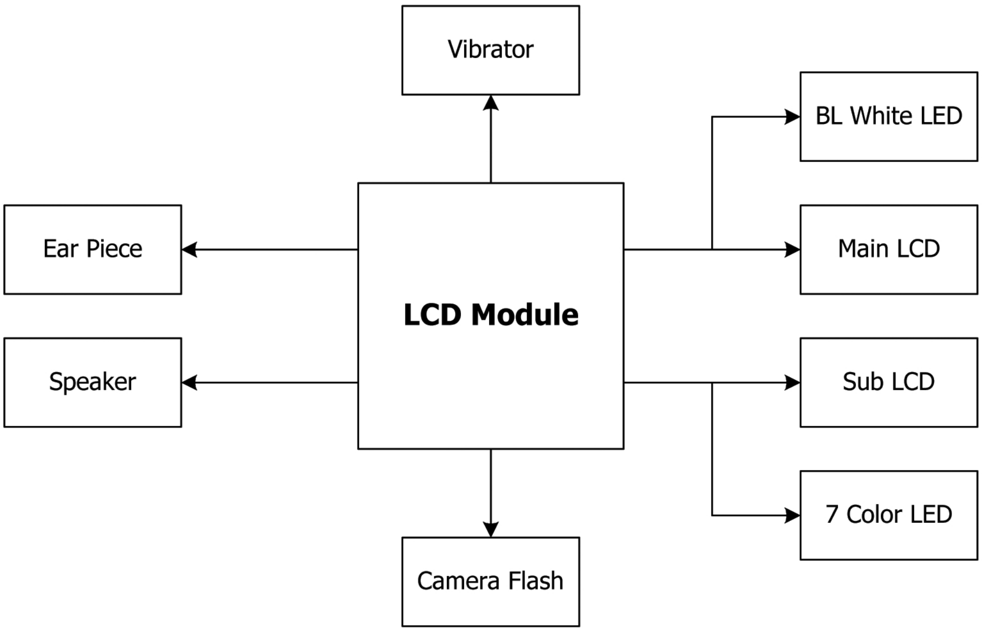


Figure. LCD Module Block Diagram

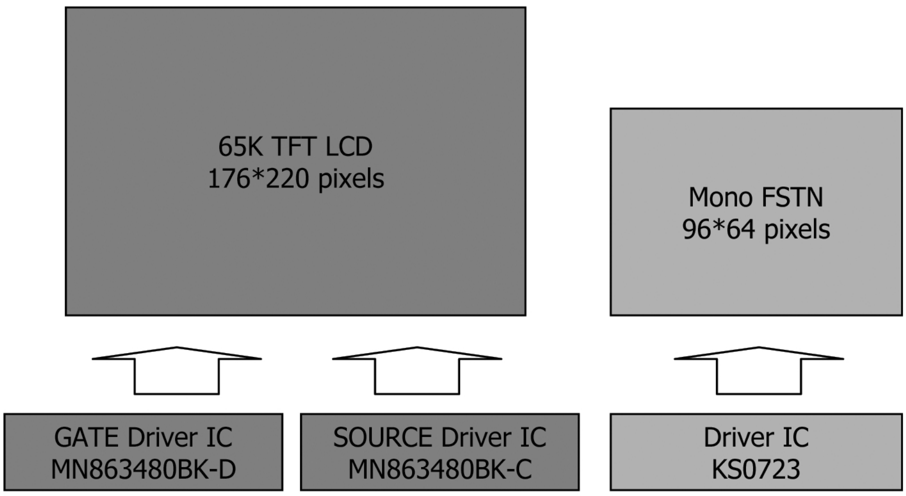


Figure. LCD Module(Main & Sub LCD)

3.4 Analog Baseband (ABB) Processor

3.4.1 Overview of Audio path

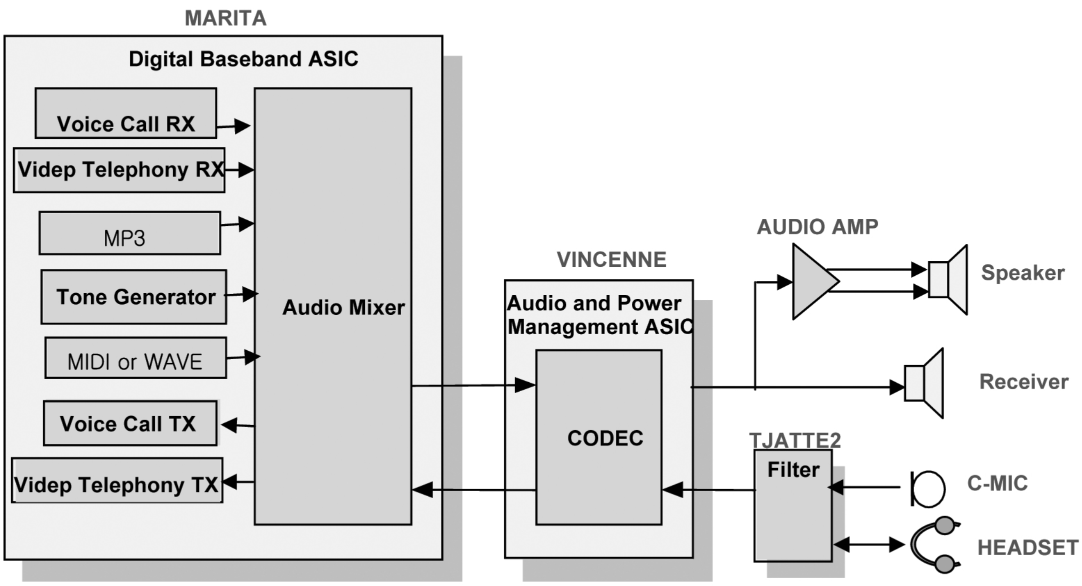


Figure. Audio Path Block Diagram

3.4.2 Audio Signal Processing & Interface

Audio signal processing is divided Uplink path and downlink path.
The uplink path amplifies the audio signal from MIC and converts this analog signal to digital signal and then transmit it to DBB Chip (Marita).
This transmitted signal is reformed to fit in GSM & WCDMA Frame format and delivered to RF Chip.
The downlink path amplifies the signal from DBB chip (Marita) and outputs it to Receiver (or Speaker).
The audio interface consists of PCM encoding and decoding circuitry, microphone amplifiers and earphone drivers.
The PCM encoder and decoder blocks are two-channel, 16-bit circuits with programmable gain amplifiers (PGA).
The decoder has a receive volume control. The audio inputs and outputs can be switched to normal or auxiliary ports.

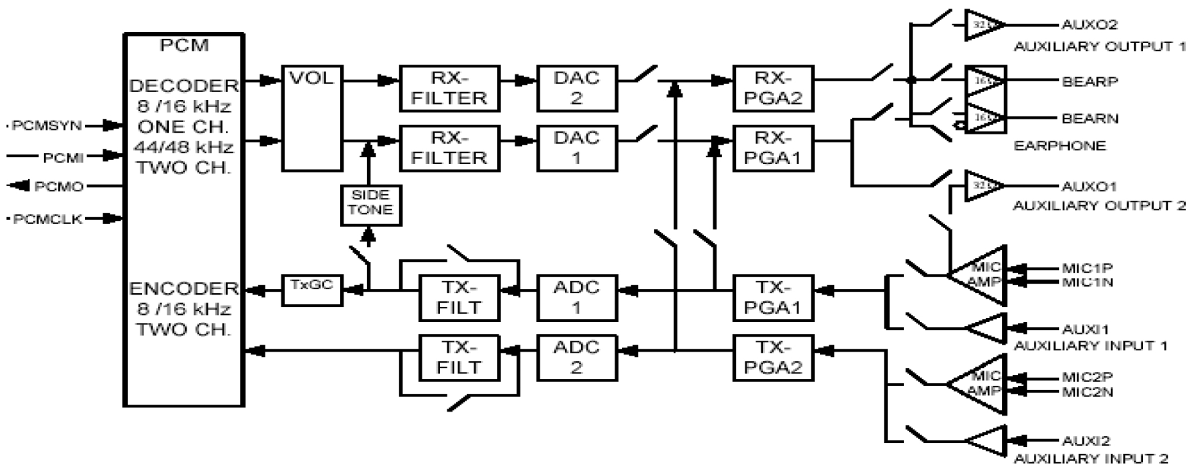


Figure. Audio Interface Detailed Diagram (VICENNE)

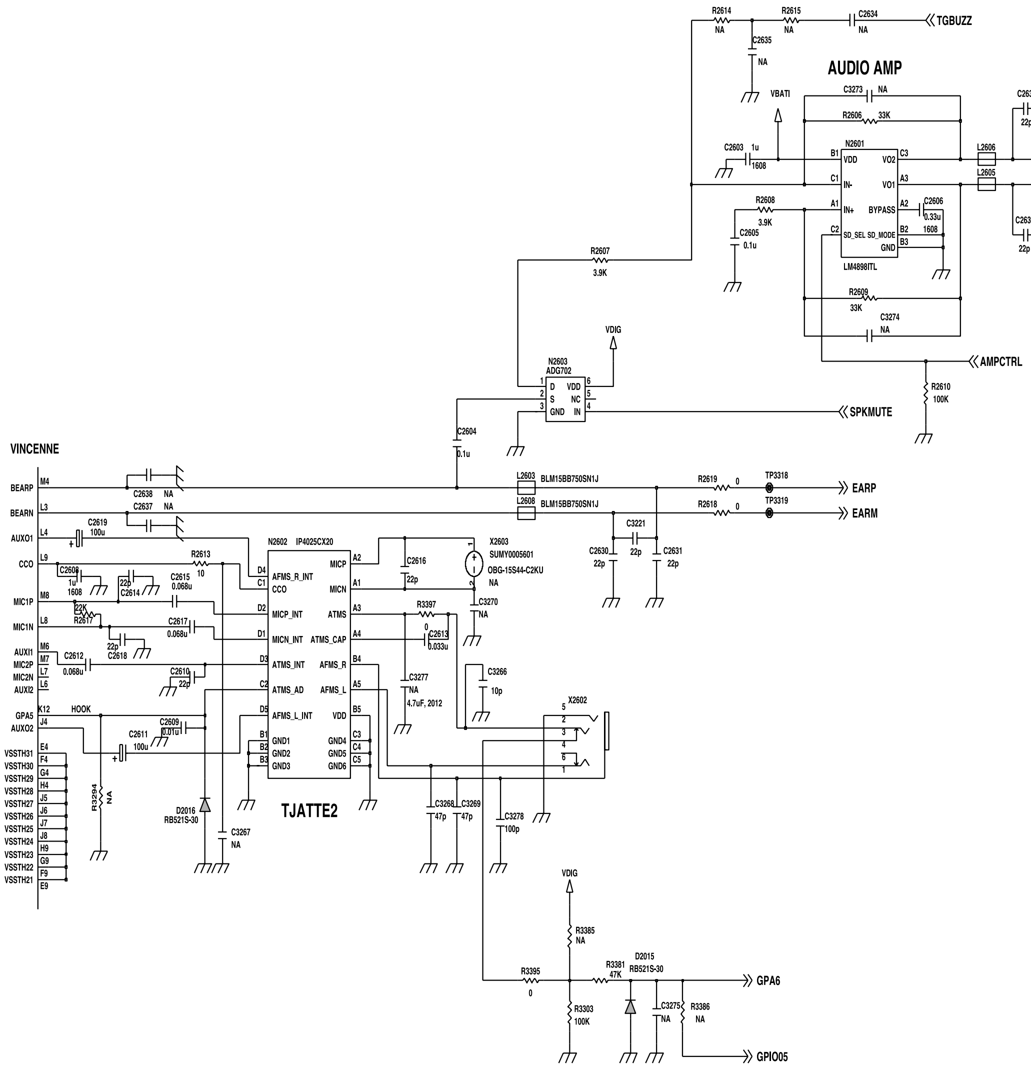


Figure. Audio Section scheme

3.4.3 Audio Mode

Audio Mode includes three states. (Voice call, Midi.MP3).
Each states is sorted by the total 7 Modes according to external Devices
(Receiver, Loud Speaker, Headset).
Video Telephony Mode Operate on state of the WCDMA CALL.

Mode		VINCENNE In/Out Port	
		IN	OUT
Voice call	Receiver Mode	MIC1P/MIC1N	BEARP/BEARN
	Loud Speaker Mode	MIC1P/MIC1N	BEARP
	Headset Mode	AUXI1	AUXO1/AUXO2
	Video Telephony Mode	MIC1P/MIC1N	BEARP
MIDI	Only Loud Speaker		BEARP
MP3	Loud Speaker Mode		BEARP
	Headset Mode		AUXO1/AUXO2

Table Audio Mode

3.4.4 Voice Call

3.4.4.1 Voice call Downlink Mode(Receiver, Speaker, Headset)

This section provides a detailed description of the Voice Call RX functions.

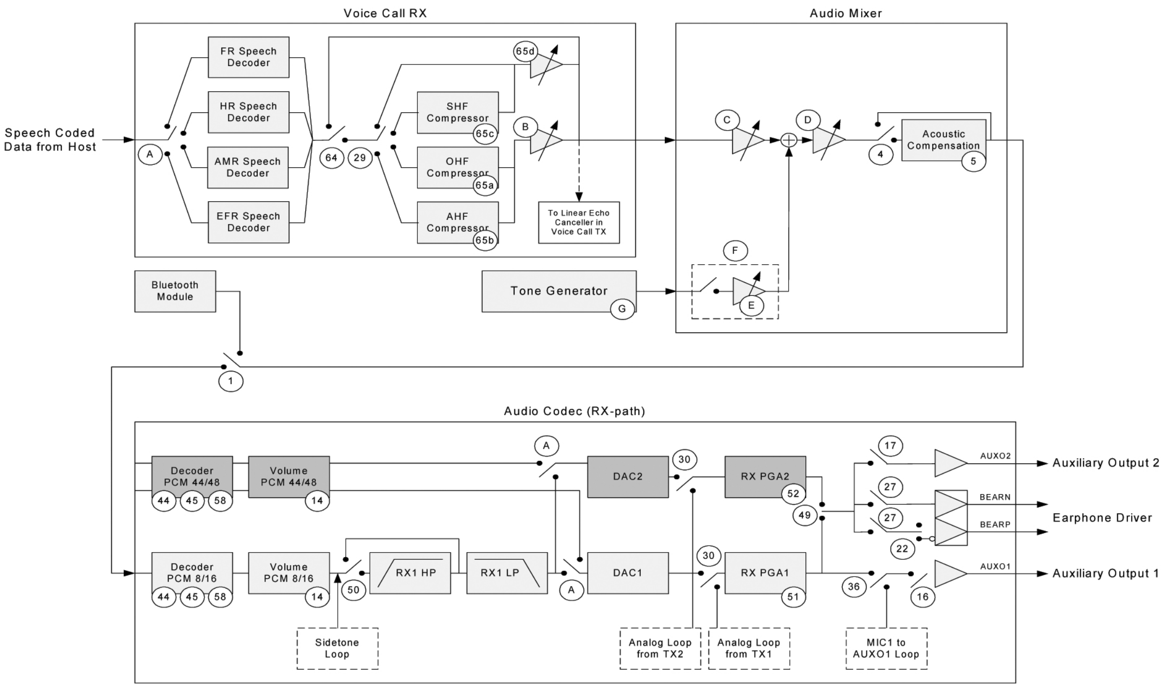


Figure. Voice call Downlink Scheme

The voice decoder accepts a serial input stream of linear PCM coded speech. The receive band-pass filter is the next step in the CODEC receive path. Following the filter is the DAC, followed by a PGA enabling to adjust or trim the circuit in the product for different sensitivity of the earphone and spread in the RX path. **The final step in the receive path is the earphone amplifier and the auxiliary output. The auxiliary audio amplifier is intended to drive low impedance headphones.** The earphone amplifier and the auxiliary audio outputs can be powered down (muted) via I2C. Both the earphone driver and one of the auxiliary drivers can simultaneously provide an output signal during voice decoding.

- **Receiver Mode :** Earphone amplifier → BEARP/N Port → Receiver(32Ω)
- **Loud Speaker Mode :** Earphone amplifier → BEARP Port → Analog S/W(ADG702) →
  AUDIO AMP(LM4894IBP) → Speaker(8Ω)
- **Video Telephony Mode :** Earphone amplifier → BEARP Port → Analog S/W(N2603) →
  AUDIO AMP (LM4894IBP) → Speaker(8Ω)
- **Headset Mode :** Auxiliary audio amplifier → AUXO1/2 →
  TJATTE2 IN (AFMS_R_INT/AFMS_L_INT) →
  TJATTE2 OUT(AFMS_R/AFMS_L) → Head Phone

Speaker Phone Mode has two GPIO switching control ports. One is **SPKMUTE** and the other is **AMPCTRL**. SPKMUTE controls analog switch(ADG702) and AMPCTRL controls shutdown of AUDIOAMP(LM4894IBP). **Video Telephony Mode** has same paths with Loud Speaker Mode.

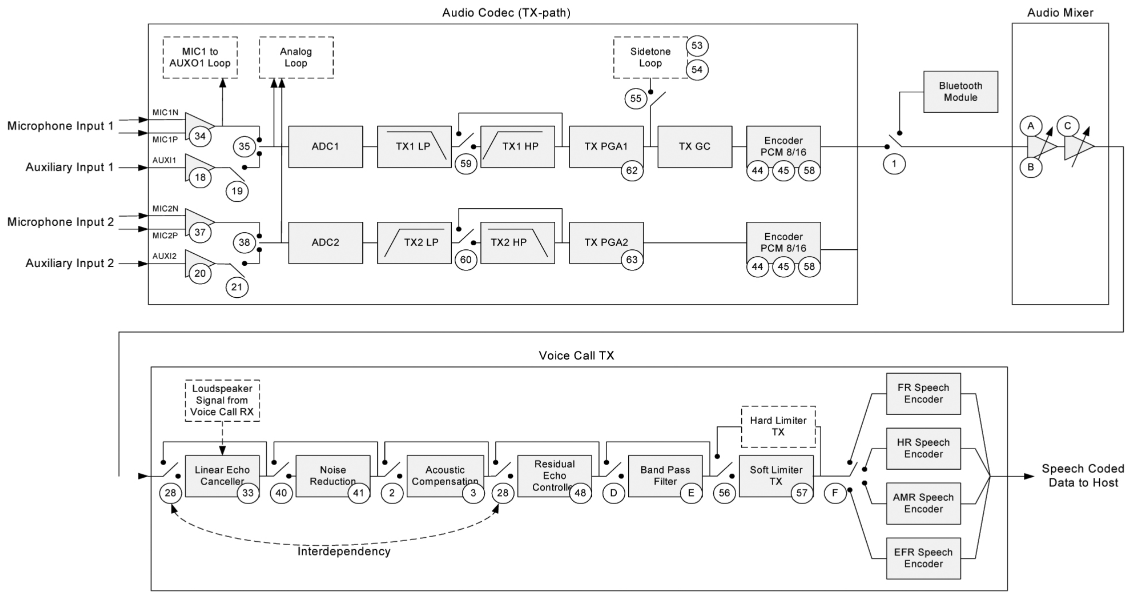
Mode	SPKMUTE	AMPCTRL
Receiver	High	Low
Headset	High	Low
Loud Speaker	Low	High
Video Telephony	Low	High

Table Speaker Phone Mode GPIO control state

* SPKMUTE; MARITA GPIO36
* AMPCTRL; MARITA GPIO06

3.4.4.2 Voice Call Uplink Mode (Receiver, Speaker, Headset)

This section provides a detailed description of the Voice Call TX functions.



<u>**Figure. Voice call Uplink Scheme**</u>

The Uplink supports two microphones and two auxiliary inputs to the speech encoder blocks. Both microphone inputs are compatible with an electric microphone.

The VINCENNE internal voltage source (CCO) provides the necessary drive current for the electric microphone. The voltage source is via I2C programmable to supply 2.2V or 2.4V. But the voltage source of our Model is to supply 2.4V.

The auxiliary audio inputs can be used as an alternative source of speech, a source from an external microphone or as an analog loop connection. Figure shows that the audio inputs are fed to the transmit PGAs, which enables to adjust the total gain in the product for different sensitivities of the microphones and spread in the transmit paths. The ADCs are followed by the transmit band pass filters, which accept the maximum output swing that the microphone preamplifiers can deliver without clipping, and maintain a good signal-to-noise ratio. The high pass filter in the TX-paths can be disabled via I2C; still removing the DC offset from the signal. For one of the two transmit paths, a transmit gain control amplifier precedes the final encoding of the PCM output.

Each Voice Uplink Mode paths shown below.

Receiver Mode : C-MIC(OBG-15S44) → TJATTE2 IN (MICP/N) → TJATTE2 OUT (MICP_INT/MICN_INT) → VICENNE Input(MIC1N/1P)
Loud Speaker Mode : C-MIC(OBG-15S44) → TJATTE2 IN (MICP/N) → TJATTE2 OUT(MICP_INT/MICN_INT) → VICENNE Input(MIC1N/1P)
Video Telephony Mode : C-MIC(OBG-15S44) → TJATTE2 IN (MICP/N) → TJATTE2 OUT (MICP_INT/MICN_INT) → VICENNE Input(MIC1N/1P)
Headset Mode : Headset MIC → EARJACK S/W(X2602, Pin Num 2) → TJATTE2 IN(ATMS_CAP) TJATTE2 OUT (ATMS_INT) VICENNE Input(AUXI1)

When **the headset** is inserted, **GPA6**(Circuit Diagram net Name) converted into low state.
So, the headset icon is displayed on Main LCD.

3.4.5 MIDI (Ring Tone Play)

This section provides a detailed description of the MIDI and WAV-file functions.

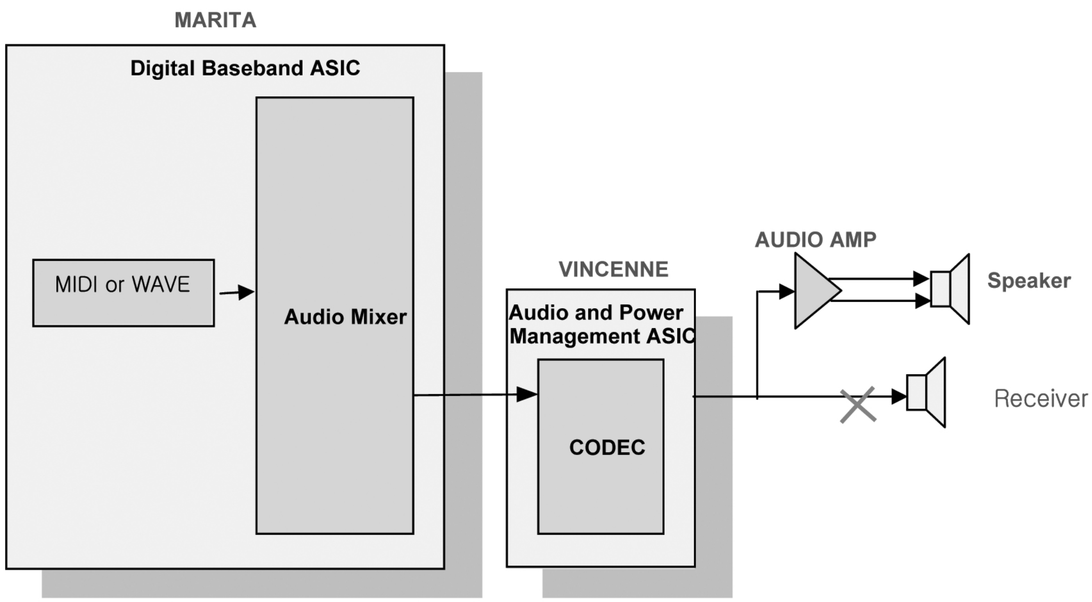


Figure. MIDI Scheme

External MIDI path is the same as Voice Loudspeaker downlink Mode, except source in MARITA (DSP and Audio Mixer).

• MIDI : MARITA → PCM Decoder → Earphone amplifier → BEARP Port → Analog S/W(ADG702) → AUDIO AMP(LM4894IBP) → Speaker(8Ω)

MIDI being played through external Device Speaker only. MIDI Mode control port shown below

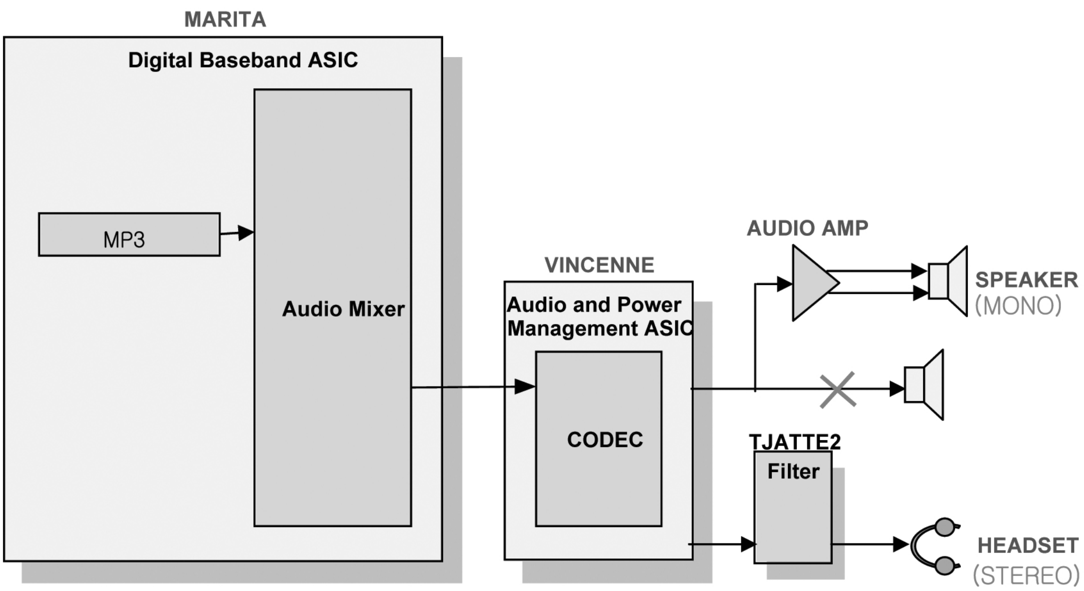
STATE(SPK ONLY)	SPKMUTE	AMPCTRL
MIDI ON	LOW	High
MIDI OFF	High	Low

Tabel MIDI GPIO Control STATE

* SPKMUTE; MARITA GPIO36
* AMPCTRL; MARITA GPIO06

3.4.6 MP3 (Audio Player)

This section provides a detailed description of the MP3 file functions.



<u>**Figure. MP3 Scheme**</u>

MP3 function supports PCM 44/48KHz sampling rate.The PCM44/48 RX-path is intended to be used as a stereo music headphones. It is also possible to connect a differential load or to use the RX-path with only one channel running (mono).
In stereo mode, auxiliary outputs (AUXO1 and AUXO2) can be used to drive **the headset**.

In single channel mode (mono), BEARP can be used to drive a load (**Speaker**).

3.4.7 Video Telephony

This section provides a description of the Video Telephony functions.

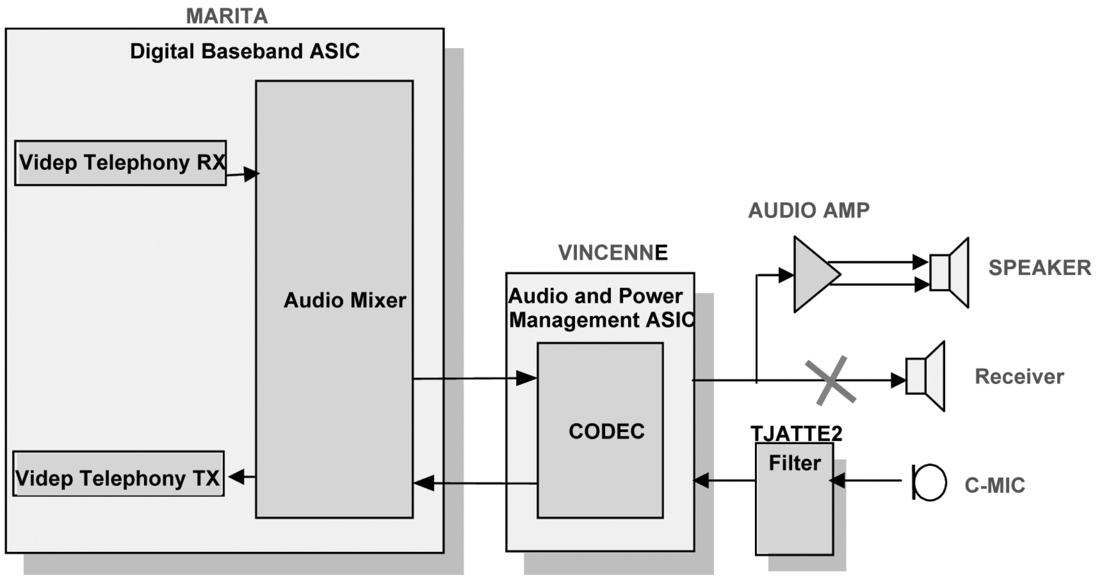


Figure. Video Telephony Scheme

Video Telephony Mode has same paths with Loud Speaker Mode.

STATE(SPK ONLY)	SPKMUTE	AMPCTRL
Video Telephony ON	LOW	High
Video Telephony OFF	High	Low

Tabel Video Telephony GPIO Control STATE

* SPKMUTE; MARITA GPIO36
* AMPCTRL; MARITA GPIO36

3.4.8 Audio Main Component

There are 6 components in U8100 schematic Diagram. Part Number marked on U8100 Schematic Diagram.

N0	ITEM	Part Name	Part Number
1	Dual Speaker	**EMD1940A**	
1	C-MIC	**OBG-15S44**	X2603
3	Audio AMP	**LM4894IBP**	N2601
4	TJATTE2	**IP4025CS20**	N2602
5	Ear-JACK	**HSJ1730**	X2602
6	Analog Switch	**ADG702**	N2603

Tabel Audio Component List

TJATTE2 Description

The TJATTE2 is a 6-channel RC low pass filter array that is designed to provide filtering of undesired RF signals in the 800-2700 MHz frequency band.
In addition, the TJATTE2 incorporates diodes to provide protection to downstream components from Electrostatic Discharge (ESD) voltages as high as 8 kV.

PIN	DESCRIPTION	PIN	DESCRIPTION	PIN	DESCRIPTION	PIN	DESCRIPTION
A1	MICN	B1	GND	C1	CCO	D1	MICN-int
A2	MICP	B2	GND	C2	ATMS_AD	D2	MICP-int
A3	ATMS	B3	GND	C3	GND	D3	ATMS-int
A4	ATMS-cap	B4	AFMS_R	C4	GND	D4	AFMS_R-int
A5	AFMS_L	B5	VDD	C5	GND	D5	AFMS_L-int

Tabel TJATTE Pin Description

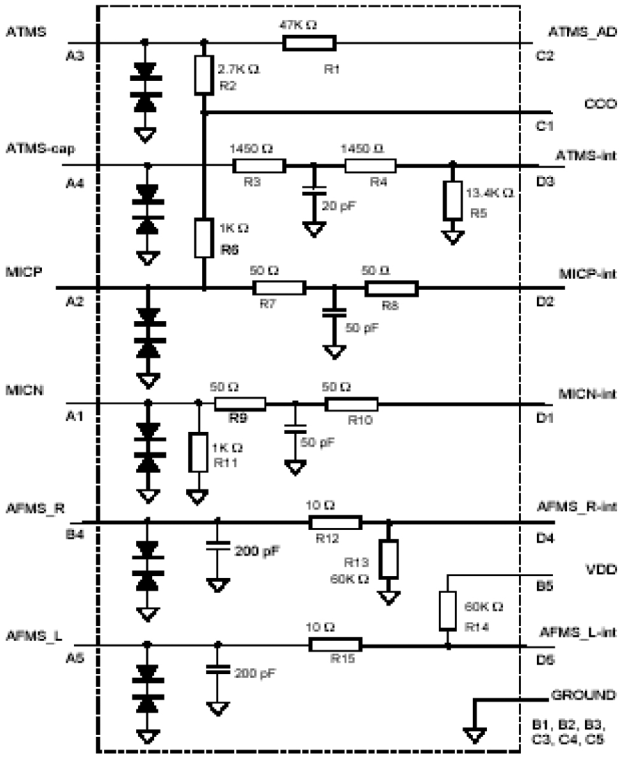


Figure. TJATTE2 Block Diagram

3.4.9 GPADC(General Purpose ADC) and AUTOADC2

The GPADC consists of a 14 input MUX and an 8-bit ADC. The analog input signal is selected with the MUX and converted in the ADC.
The GPADC has a built in controller, AUTOADC2, which is able to operate in the background without software intervention. The AUTOADC2 periodically measures the battery voltage or current. Figure shows the schematic of GPADC part. The GPADC channel spec is as following Table.

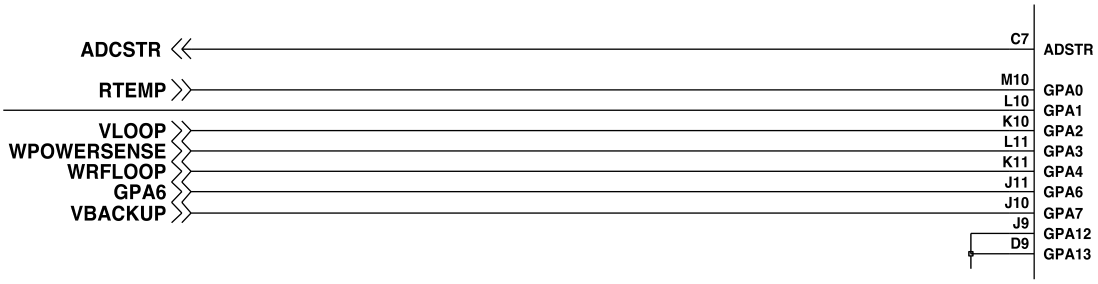


Figure. Schematic of GPADC and AUTOADC2

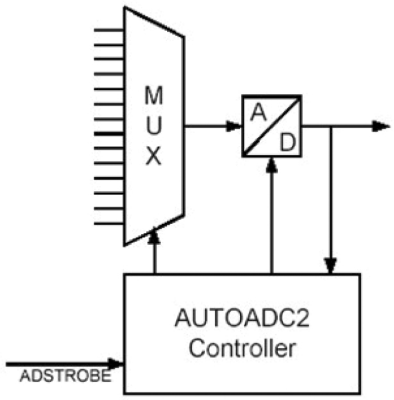


Figure. GPADC and AUTOADC2 Block diagram

ADC 6 channels		
Resource	Name	Description
GPA0	RTEMP	Radio temperature sense
GPA2	VLOOP	Loop voltage sense
GPA3	WPOWERSENSE	Reference voltage for PAM
GPA4	WRFLOOP	Lock inform
GPA6	GPA6	Headset detect
GPA7	VBACKUP	Backup battery

Table. GPADC channel spec

3.4.10 Charger control

A programmable charger in AB2000 is used for battery charging. It is possible to set limits for the output voltage at CHSENSE- and the output current from DCIO via the sense resistor to CHSENSE-. The voltage at CHSENSE- and the current feed to CHSENSE- cannot be measured directly by the GPADC. Instead, the two measuring amplifiers translate these inputs to a voltage proportional to the input and within the range of the GPADC. Figure shows the schematic of charging control part.

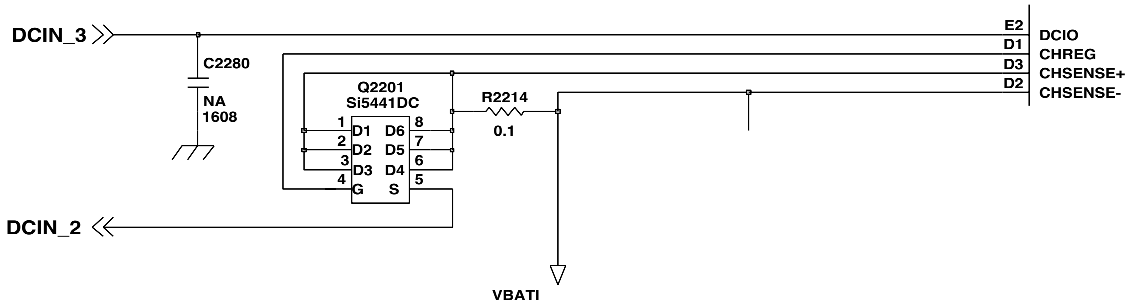


Figure. Schematic of charging control part

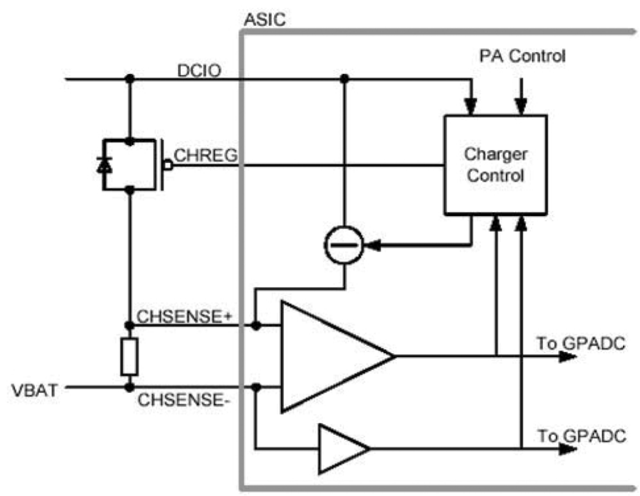


Figure. Battery charging block diagram

3.4.11 Fuel Gauge

AB2000 supports the measurement of the current consumption/charging current in the U8100 with a fuel gauge block. By constantly integrating the current flowing into and out of the battery, the fuel gauge block is used to determine the remaining battery capacity.
The function of the fuel gauge block is schematically described in Figure. A sense resistor R_FGSENSE is connected in series with the battery. The voltage across the resistor, equivalent to the current entering/leaving the battery, is integrated using an ADC block.

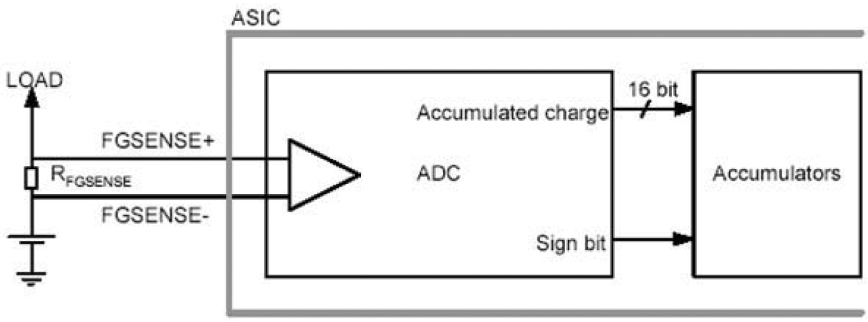


Figure. The analog front-end of the fuel gauge block

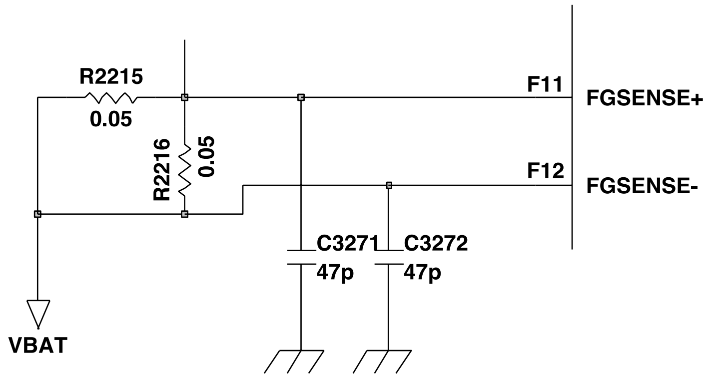


Figure. The Schematic of the fuel gauge block

Name	Type	Unused	Description
FGSENSE+	Analog	VBAT	Fuel gauge current sensing input positive
FGSENSE-	Analog	VBAT	Fuel gauge current sensing input negative

Table. Fuel Gauge channel spec

3.4.12 Battery Temperature Measurement

The BDATA node, the constant current source, feed the battery data output while monitoring the voltage at the battery data node with GPADC. This battery data is converted to the battery temperature. Figure shows the schematic of battery temperature measurement part.

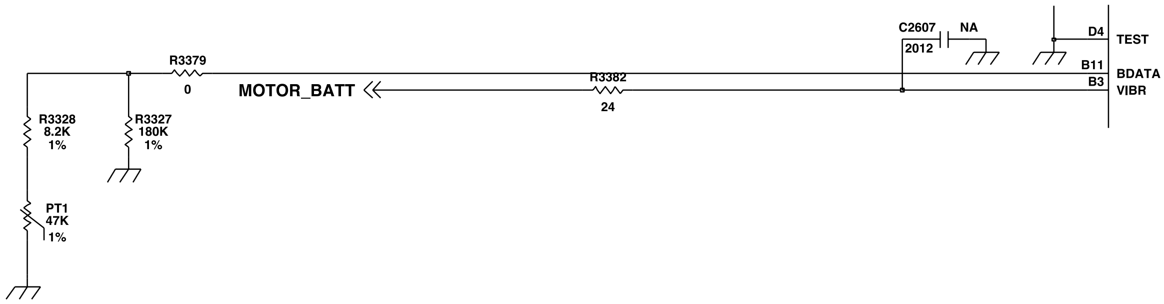


Figure. Battery Temperature Measurement

Name	Type	Unused	Description
BDATA	Digital Input/Output	Unconnected	Current output

Table BDATA channel spec

3.4.13 Charging Part

The charging block in AB2000 processes the charging operation by using VBAT voltage. It is enabled or disabled by the assertion/negation of the external signal DCIO. Part of the charging block are activated and deactivated depending on the level of VBAT. Figure shows the schematic of charging part.

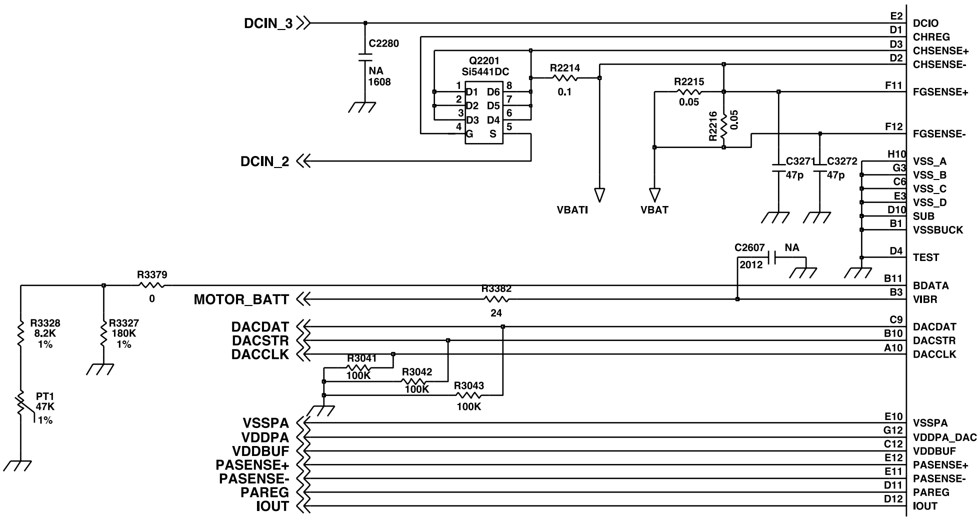


Figure. Charging Part

When VBAT is below a certain value, 3.2V, a current generator take care of initial charging of the CHSENSE+ node and internal trickle charge signal is active. This part of the charging block is powered on and active when DCIO is asserted. The DCIO signal is asserted when its voltage is above the voltage at VBAT. As soon as generator is turned off and all parts of the charging block are functional and active.
Battery block indication as shown in Fig

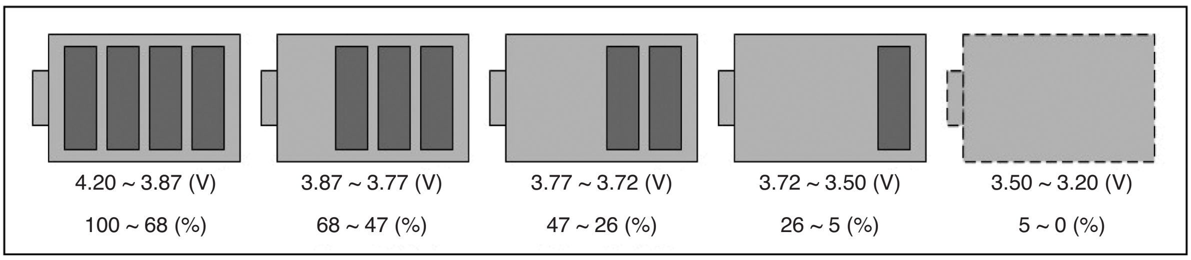


Figure. Battery Block Indication

Trickle charging

When the VBAT is below a certain value, 3.2V, a current generator take care of internal trickle charge signal is active. The charging current is set to 50mA.

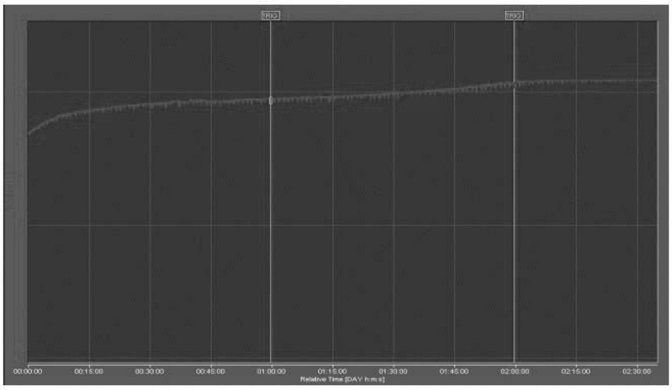
Parameter	Min	Typ	Max	Unit
Trickle current	30	50	60	mA

Table BDATA channel spec

Normal charging

When the VBAT voltage is within limits or the internal regulators are turned on, the current source for trickle charging is turned off and all parts of the charging block are active. The charging method is ‘CCCV’. (Constant Current Constant Voltage)
This charging method is used for Lithium chemistry battery packs. The CCCV method regulates the charge current and the VBAT voltage. This charging method prevents the battery voltage to go above the charge set in the CCCV algorithm. This picture shows the charging voltage(a) and charging current change(b).

(a) Charging voltage



(b) Charging current

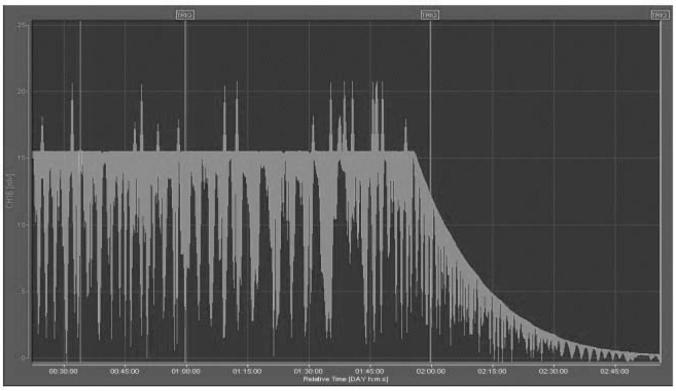


Figure. CCCV charging method

- Charging Method : CCCV (Constant Current Constant Voltage)
- Maximum Charging Voltage : 4.2V
- Maximum Charging Current : 600mA
- Nominal Battery Capacity : 1200 mAh
- Charger Voltage : 4.6V
- Charging time : Max 3.5h
- Full charge indication current (icon stop current) : 80mA
- Low battery POP UP : Idle - 3.46V, Dedicated – 3.50V
- Low battery alarm interval : Idle - 3 min, Dedicated - 1 min
- Cut-off voltage : WCDMA call - 3.1V, ELSE – 3.2V

Charging of Extended Temperature

When the battery temperature is outside the normal charging specification, the battery voltage, VBAT, is maintained at 3.7V.

- Under 0 °C : Extended temperature
- From 0 °C to 55 °C : Normal charging temperature
- Over 55 °C : Extended temperature

3.5 Voltage Regulation

3.5.1 Internal Regulation

There are LDO (Low Drop Output) regulators and BUCK converter in AB2000 (Vincenne) chip. LDO regulators and BUCK converter generate the following voltages : 1.5V, 1.8V and 2.75V. The output of these LDOs supply VDD-A, VDD-B and VDIG with 2.75V. BUCK converter steps down the VBAT to 1.5V for VCORE and VRTC, and to 1.8V for VMEM voltage. The output of these LDOs and BUCK converter are as following Table. Figure shows the power supply of each module in U8100.

3.5.2 External Regulation

1.5V LDO - supply 1.5V for wanda core
2.8V LDO - supply 2.8V for IrDA
2.8V LDO - supply 2.8V for Camera
3.3V LDO - supply 3.3V for USB
4.5V DC-DC converter – supply 4.5V for LCD back light

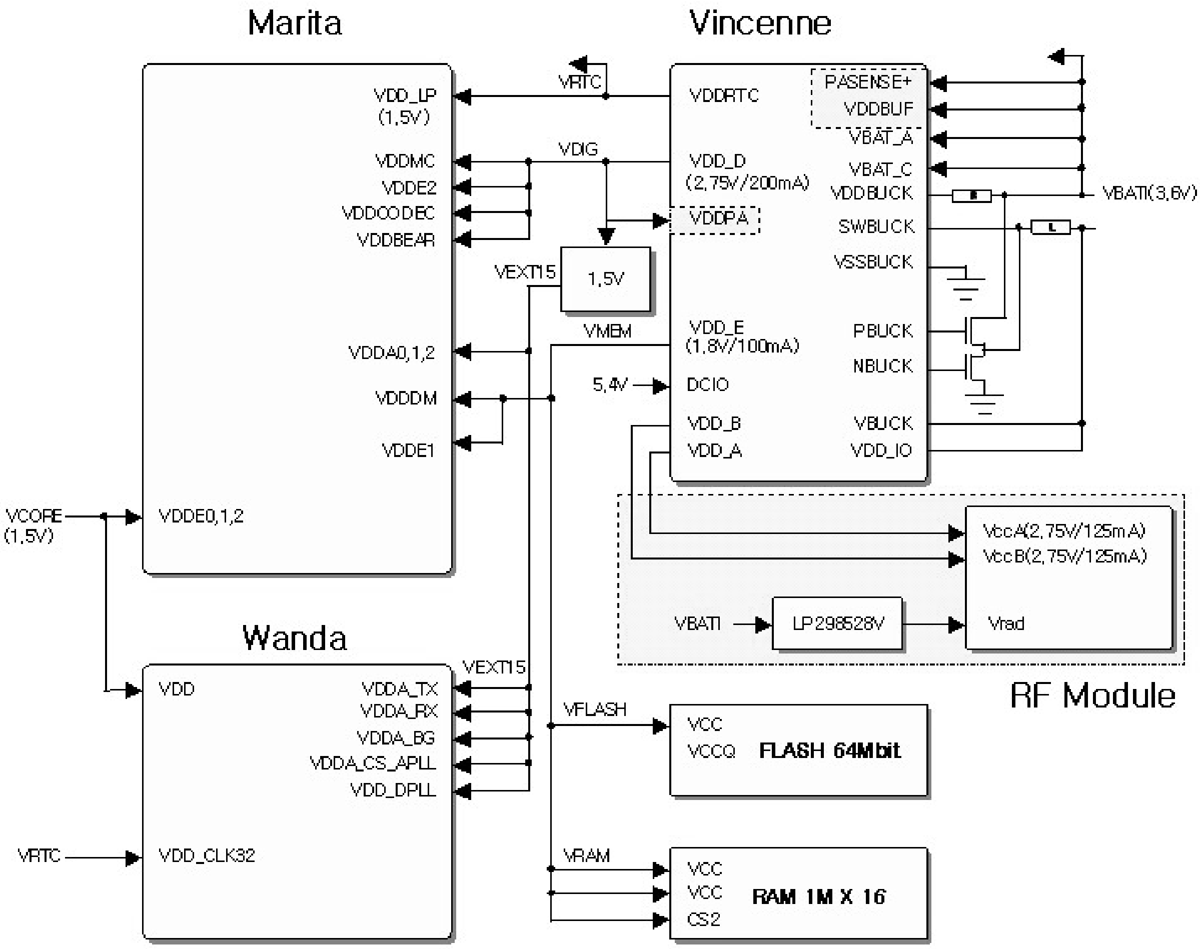


Figure. Power Supply Scheme

Pin	Name	Type	Output voltage	Description
B12	VDD_A	Power Supply	2.75V	Supply output
A11	VDD_B	Power Supply	2.75V	Supply output
M11	VDD_D	Power Supply	2.75V	Supply output
L12	VDD_E	Power Supply	1.8V	Supply output
L2	VDDLP	Power Supply	1.5V	Low Power supply output
A2	VDDBUCK	Power Supply	Unused: VBAT	Buck converter switch supply
B1	VSSBUCK	Power Supply	GND	Buck converter switch ground

Table BDATA channel spec

3.6 General Description

The RF part includes a dual-band GSM/DCS part (900 and 1800MHz) and W-CDMA part for IMT-2000 (UL 1900MHz, DL 2100MHz). It also contains Antenna Switch, WCDMA duplexer, WCDMA Power Amplifier and GSM Power Amplifier.

The whole structure of Radio part is shown in Figure 3-1.

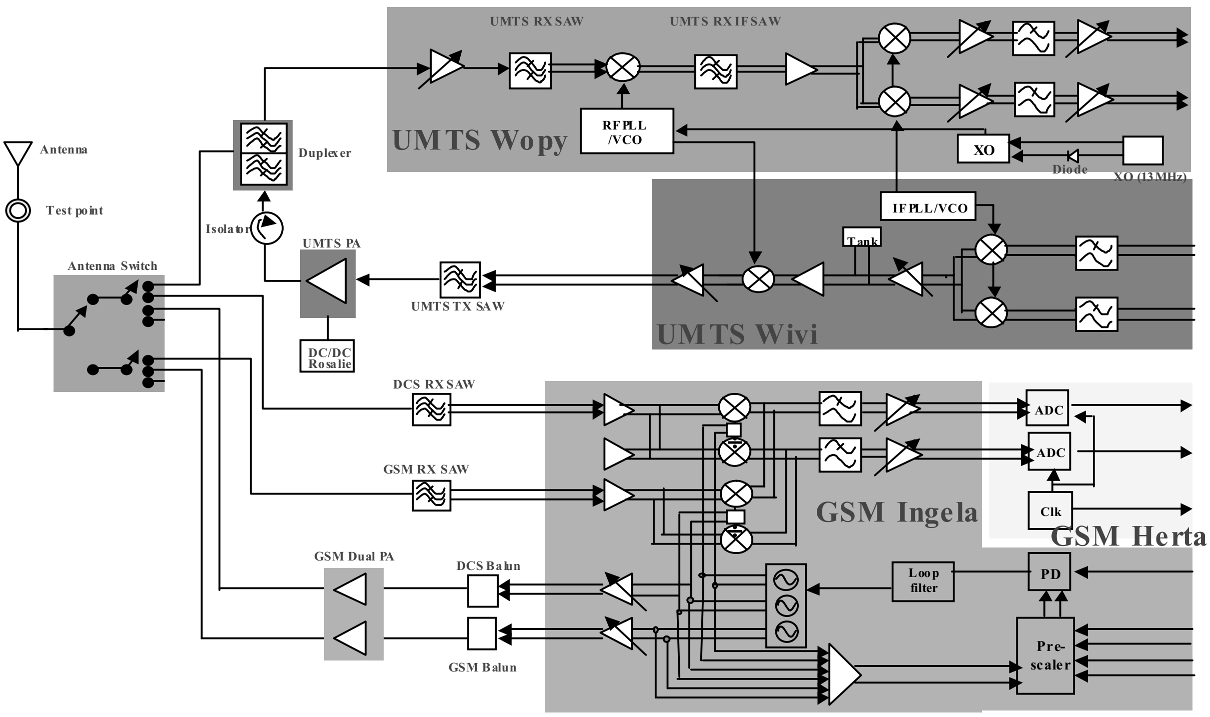


Figure 3-1. Block diagram of RF part

Starting at the antenna end, an antenna switch provides switching capability needed for three frequency bands (900, 1800 and 2100MHz). For the W-CDMA part, duplexer is included to facilitate the simultaneous transmission and reception required for the FDD mode.
The main components in the radio are Wopy (W-CDMA receiver ASIC), Wivi(W-CDMA transmitter ASIC), Ingela(GSM/GPRS transceiver) and two power amplifiers.
The mixed-signal circuit ASIC, Vincenne provides power supply for the main RF components.

The control flow for the Radio is shown in Figure 3-2.

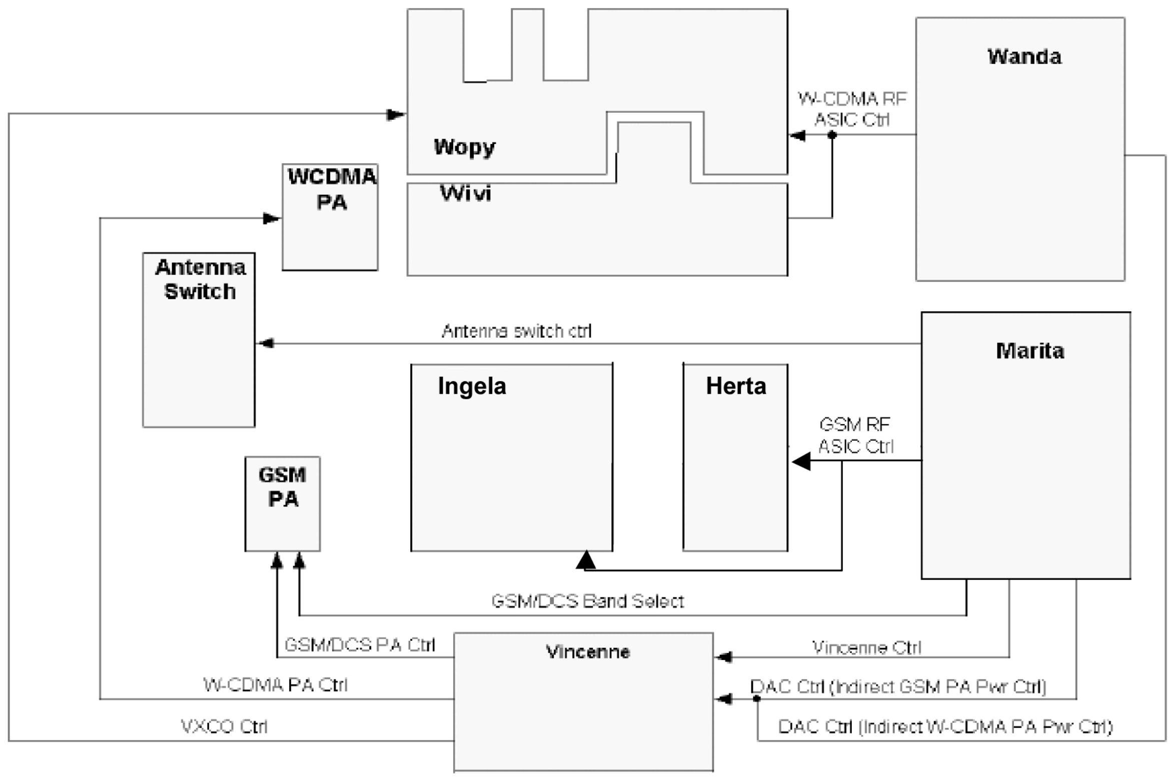


Figure 3-2. RF control signal flow diagram

The Marita(the main processor) controls the overall radio system. In the GSM/GPRS air interface mode, this control is handled via direct interfaces to individual RF components. The Marita(the main processor) also handles the antenna switch mechanism for selection of mode.

In the W-CDMA mode, the RF system is managed via the Wanda (WCDMA digital base-band coprocessor ASIC) and its DSP processor.

3.7 GSM Mode

3.7.1 Receiver

The received RF signal on the antenna connector arrives via antenna switch at external band pass filters for band selectivity. One filter is required per supported GSM band. The corresponding LNA amplifies the signal for optimum noise suppression.
The LNA output signal is mixed with the on-channel LO generated by the proper VCO and transformed into a Q and an I signal. The I and Q signals are low pass filtered with two parallel high dynamic range filters.
Finally, the filtered I and Q signals are converted by a sigma-delta converter into two 13 Mbps digital bit streams by Herta(A/D converter), then fed to the Marita baseband ASIC.

A. Front end.

RF Front end consists of antenna, antenna switch(N1000), two RF SAWs(Z1100, Z1110) and dual band LNAs integrated in transceiver(N1100). The Received RF signals(GSM 925MHz ~ 960MHz, DCS 1805MHz ~ 1880MHz) are fed into the antenna or coaxial connector. An antenna matching circuit is between the antenna and the coaxial connector.
The Antenna Switch(N1000) is used to select the signal path, which is one of WCDMA, GSM RX, GSM TX, DCS RX, and DCS TX. The control signals VC1, VC2 and VCG of antenna switch (N1000) are connected to Marita baseband ASIC(D2000) to control the signal path. For example, when the GSM RX path is turned on, the received RF signal, which has passed through the antenna switch, is filtered by GSM RF SAW filter to suppress any unwanted signal except GSM RX band. The filtered RF signal is amplified by an LNA integrated in the transceiver IC(N1100) and is passed to a direct conversion demodulator. The process for DCS RX is also the same as GSM RX case.

The logic for antenna switch is given below Table 3-1.

	VC1	VC2	VCG
GSM TX	0V	0V	2.8V ~ 3.0V
GSM RX	0V	0V	0V
DCS TX	2.8V ~ 3.0V	2.8V ~ 3.0V	0V
DCS RX	0V	2.8V ~ 3.0V	0V
WCDMA	0V	0V	0V

Table 3-1. Antenna Switch logic

B. Receiver Block.

The circuit contains one frequency down-conversion section for each receive band and a common base band amplifier and filter section. The GSM900 RF part consists of a low noise amplifier followed by high dynamic range mixers.
The DCS 1800 RF part also has low noise amplifier connected to the other mixers.
The amplified RF signal is mixed with the quadrature local oscillator signal to create in-phase (I) and quadrature phase (Q) baseband signals. The I and Q signals are then buffered and low pass filtered. The same baseband circuitry is used for all bands.
Balanced signals are used for minimizing cross talk due to package parasitics. An impedance level at RF of 150 ohms for the GSM 900 input and 50 ohms for the DCS 1800 input is chosen to minimmize current consumption at best noise performance.
The low gain mode in GSM 900 is used in high input signal mode. There is no gain switch in DCS 1800.

Figure 3-3 shows a block diagram of the receiver block.

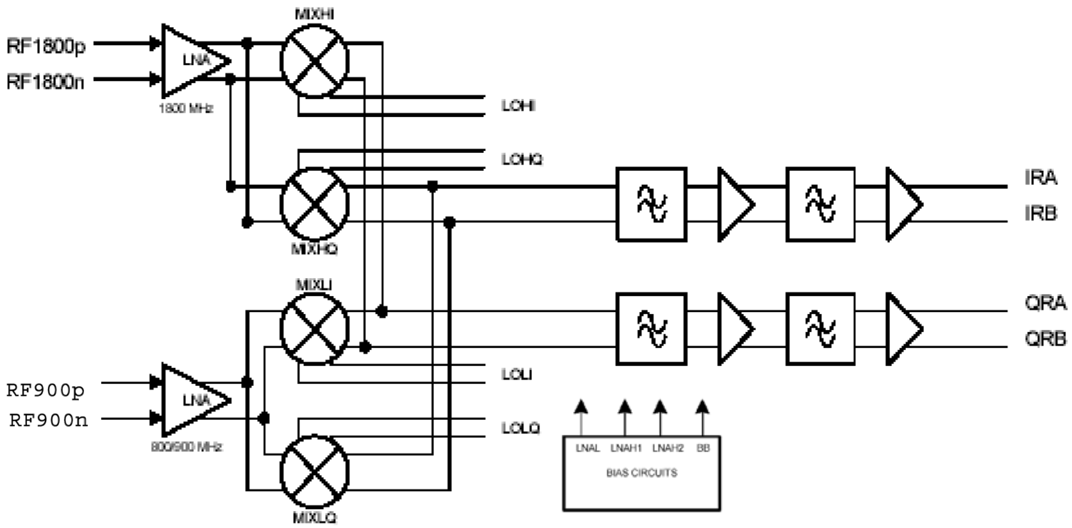


Figure 3-3. Block diagram of receiver part.

C. LO Block

The LO signals from the receive VCO section drive the dividers for GSM 900 and DCS 1800 respectively to provide quadrature LO signals to the receive mixers. The LO signal is also supplied to the prescaler and transmit output buffer.

Figure 3-4 shows a block diagram of the LO block.

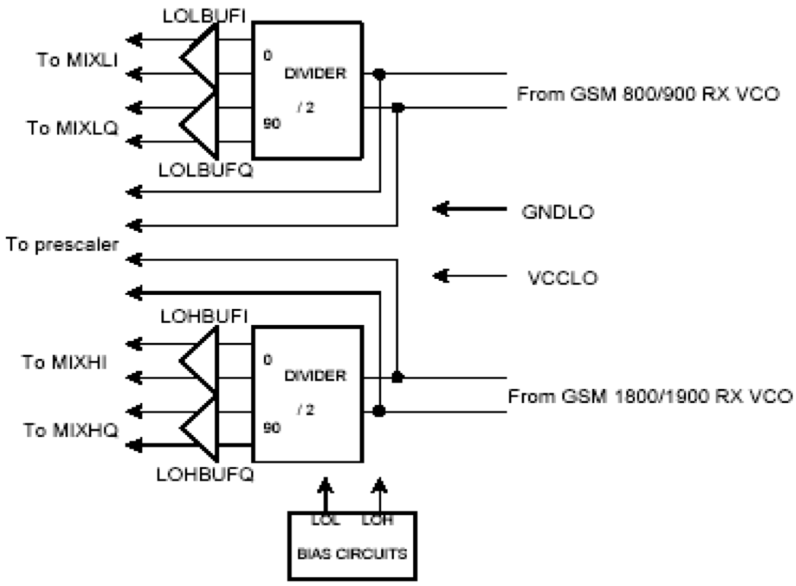


Figure 3-4. Block diagram of the LO part.

D. VCO Block

The VCOs are fully integrated balanced LC oscillators with on-chip resonators. The receive VCOs run on double frequency.
Different frequency ranges can be selected in the VCOs for GSM/DCS band operation.
The VCOs are supplied from a separated external voltage regulator to avoid frequency pushing and up conversion of low frequency noise. A separate ground pin is also used as varactor ground reference to prevent DC voltage drop changes from affecting the VCO frequency.

Figure 3-5 shows a block diagram of the VCO block.

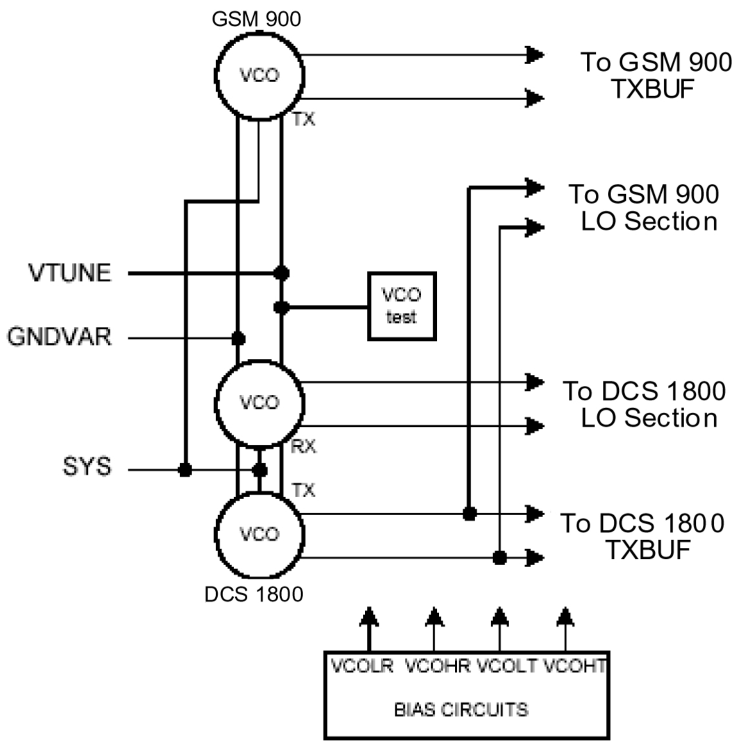


Figure 3-5. Block diagram of the VCO part.

E. PLL Block

The PLL consists of a programmable prescaler with multiple division ratios and a phase and frequency detector with a charge pump with programmable output current. Channel frequency selection and transmitter modulation is controlled via the prescaler modulus inputs MODA ~ MODD and the prescaler offset value N offset. The MODA ~ MODD signals could be delayed 0, 5, 10 or 15 ns with MD bits to be synchronized with the XO signal.

Figure 3-6 shows a block diagram of the PLL block.

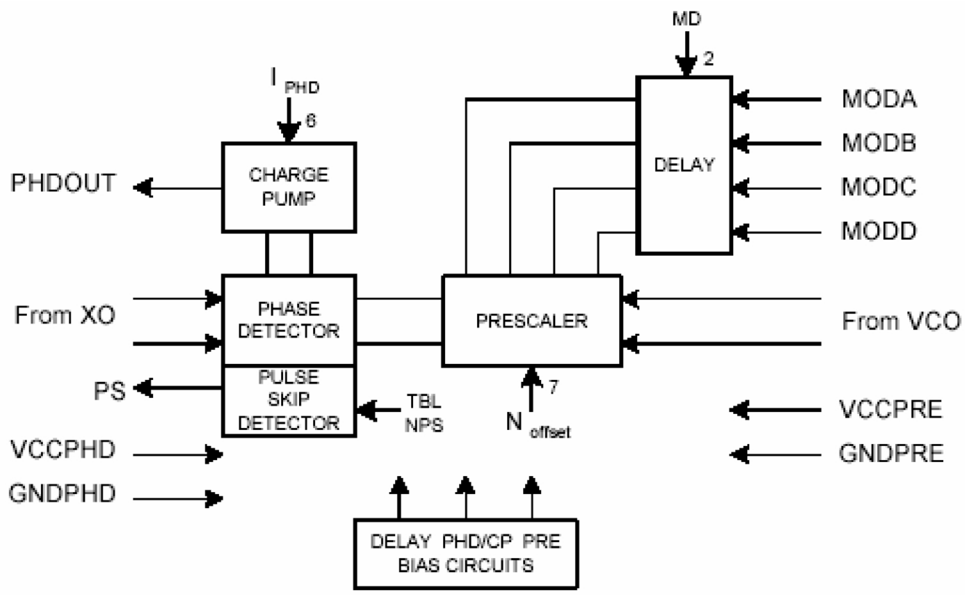


Figure 3-6. Block diagram of the PLL part.

3.7.2 Transmitter

A 4-bit sigma-delta bit stream comes from the Marita ASIC including both channel information and the GMSK phase information. Via the 3-wire control bus also driven from Marita, the selection of transmitter band is made. The 4bits from the bit stream provides the fine-tuning of the division ratio before going to the divider of the used VCO (low band, 900MHz or high band, 1800MHz).
The modulated VCO signal is fed to the output buffer. One buffer is available for each of the low and high bands. Trimming capability is included for best match versus the PA used.
The GSM/GPRS transceiver, Ingela, output is passed to the dual-band PA that after amplification feeds the signal via a low pass filter to the antenna switch and further to the antenna.
The transmit block consists of two differential high power transmit output buffers with controllable output power. The modulated transmit signal from the VCO buffer is amplified to a level suitable to drive the external power amplifier. The buffer outputs are of open collector type and must be terminated into a suitable load.

Figure 3-7 shows a block diagram of the transmitter block.

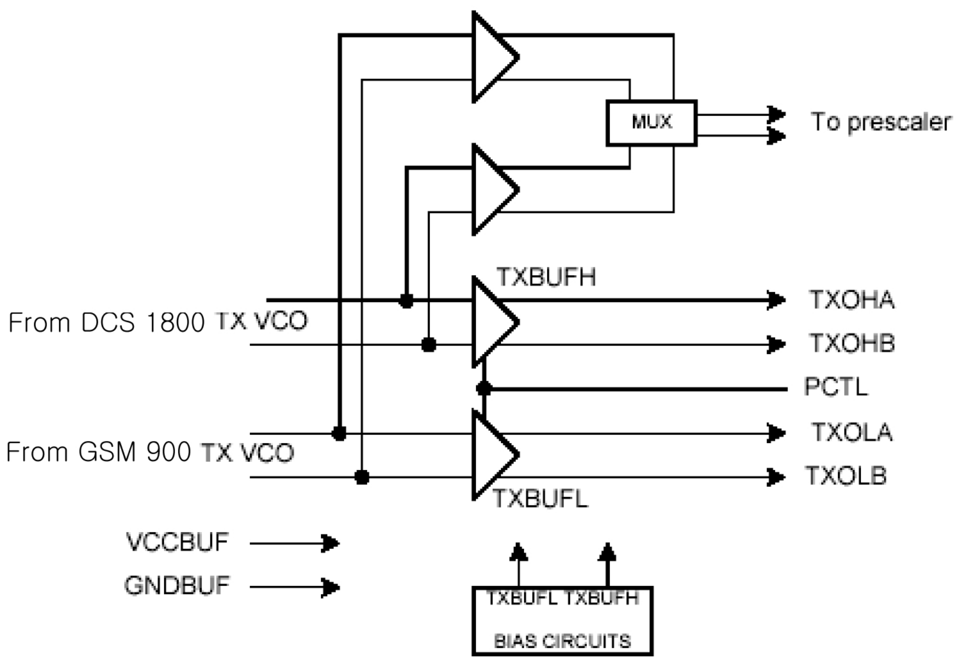


Figure 3-7. Block diagram for the transmitter.

B. Power Amplifier

The Power Amplifier (N1300) is intended for use in EGSM and DCS/PCS mobile equipment. It is a module with two parallel amplifier chains, with one chain for the EGSM transmitter section and one for the DCS/PCS transmitter section. Each chain amplifies the RF signal from the respective transmitter to the antenna. The power amplifier supports class 10.
Band selection and the output power level of the RF amplifier are controlled by discrete signals Vband and Vapc respectively from the digital baseband controller ASIC.

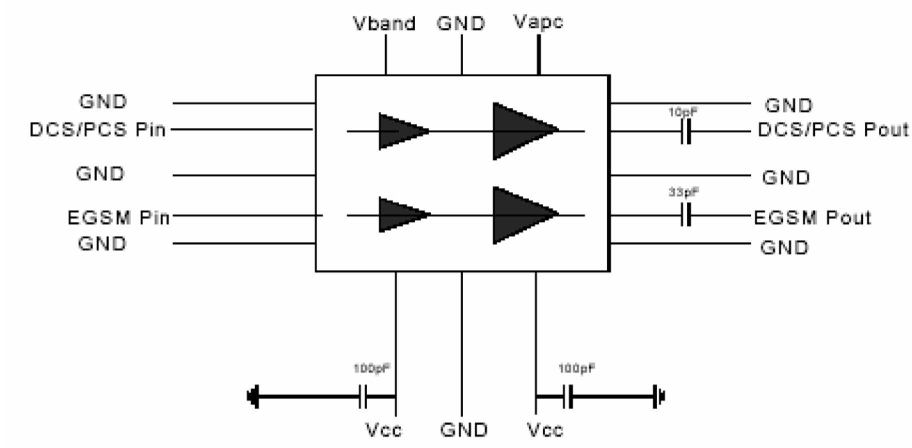


Figure 3-8. Block diagram of the Power Amplifier with Two Parallel chains.

3.8 WCDMA Mode

3.8.1 Receiver

The received RF signal on the antenna connector arrives via the antenna switch to the duplexer. The duplexer directs the signal to the LNA, which resides in Wopy (W-CDMA Receive ASIC) as every other active part of the radio receiver. The LNA has two different gain settings. From the output of the LNA, the signal is fed to the input of a RF SAW filter, and then appears at the differential output of the filter. The differential output of the RF SAW filter is connected to the differential mixer input, and the received signal is down-converted to a 190MHz IF frequency (with the RFLO signal) by the mixer.
At 190MHz, the signal is filtered in a differential (input and output) IF SAW filter, with the approximate bandwidth of 4MHz, and then again the signal is fed to Wopy (W-CDMA Receive ASIC), this time to the differential IF input, which also has a LNA.
From the 190MHz, the signal is mixed down to base-band I and Q which represented signals (using the IFLO signal). Finally the signals are filtered in low pass filters and amplified in base-band VGAs.
The I and Q represented signals appear at the output of Wopy (W-CDMA Receive ASIC) as differential voltages.
The large signal gain provided by the processing steps from the antenna down to base-band gives a DC offset at the outputs of Wopy (W-CDMA Receive ASIC). To eliminate this, there are DC-offset compensation loops included, one in the VGA of each of the I and the Q signals.

A. IFLO Section

The balanced IFLO signal from an external IFVCO drives the divider to provide qaudrature LO signals to the RxIF mixers. The LO buffers amplifies the signal to a suitable amplitude and DC level to drive the RxIF mixers.

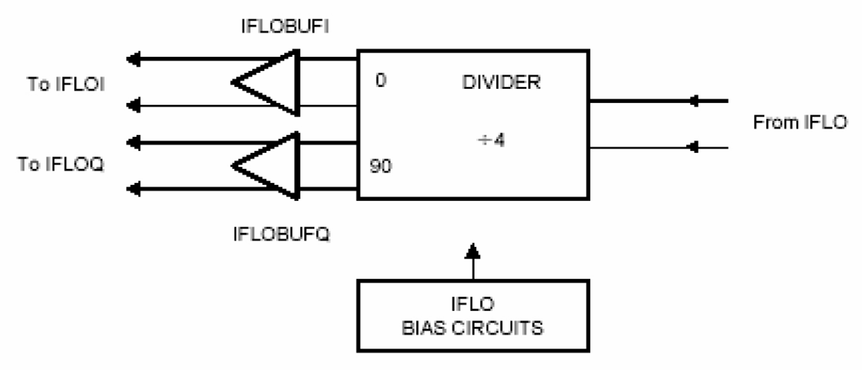


Figure 3-9. Block diagram of the IFLO section.

B. RFLO Section

The VCO is a fully integrated balanced LC oscillator with on-chip resonator. An on-chip varactor is used to control the frequency over the desired tuning range.

A separate external voltage regulator supplies the VCO with power to avoid frequency pushing and up conversion of low frequency noise. A separate ground pin is also used as varactor ground reference to prevent DC voltage drop changes from affecting the VCO frequency. Via the serial interface, the VTUNE voltage can be set to VCC/2 to check the center frequency of the VCO. The PLL consists of a programmable prescaler with multiple division ratios and a phase and frequency detector with a charge pump with programmable output current. Channel frequency selection is set via the serial interface.

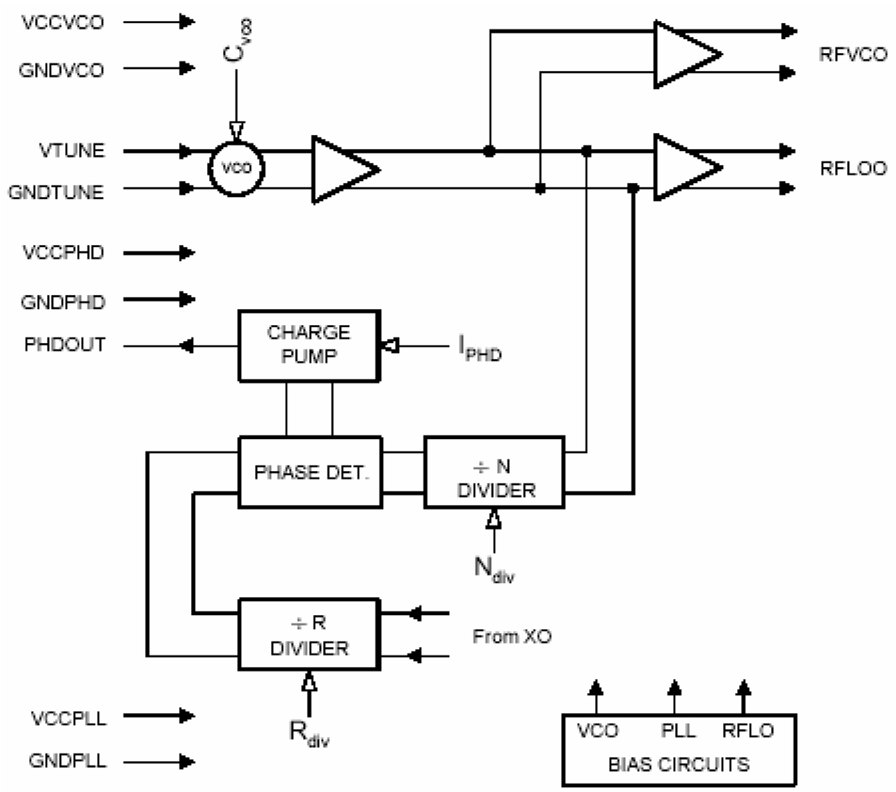


Figure 3-10. Block diagram of the RFLO section

C. Reference Section

The reference block consists of a balanced oscillator and a buffer amplifier. The crystal unit and the feedback capacitors are external. The current consumption when only the reference oscillator and the output buffer are activated must be kept to an absolute minimum.

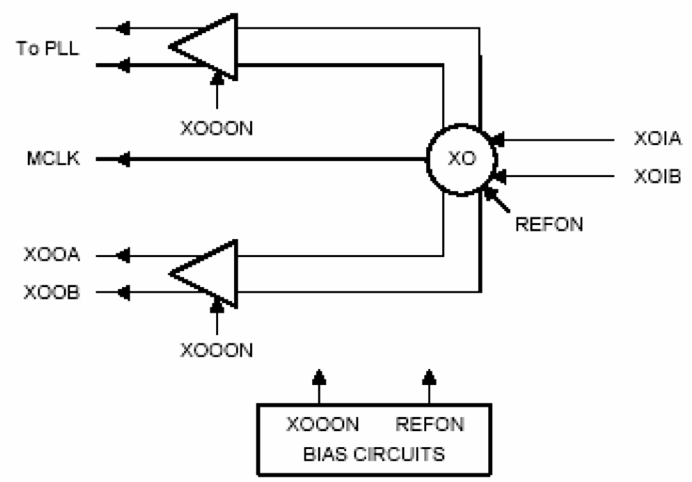


Figure 3-11. Block diagram of the Reference section.

3.8.2 Transmitter

Analogue differential signals (currents), representing I and Q, are sent to the radio ASCI Wivi (W-CDMA Transmitter ASIC) from the D/A converter in Wanda (W-CDMA digital base-band coprocessor ASIC). The signals are filtered in a reconstruction filter and then modulated up to 380MHz (using the IFLO signal). The signal is then amplified in a VGA and filtered in an external filter (an LC filter). After filtering, the signal is mixed to its final frequency (using the RFLO) and amplified in a differential output RF buffer with two different gain settings (high gain or low gain).
The differential RF signal is fed into a SAW filter with a single ended output, and is then amplified in a stand-alone RF buffer. After the RF buffer, the signal is filtered again in a SAW filter before it is fed to the PA (Power Amplifier).
In the PA the signal is amplified for the last time before leaving the radio. After the PA, the signal is sent through an isolator and through the duplexer, which directs the transmit signal to the antenna connector via the antenna switch.
The PA has variable supply voltage, which adapts itself by means of a control loop so that the linearity of the PA is kept constant. The variable supply voltage is provided from the battery through a DC/DC converter and a signal linearity detector sits at the PA output. The detected signal at the PA output is compared with a reference (supplied by the Vincenne, the mixed-signal circuit ASIC), and the error signal is used in a loop filter, which provides the control signal to the DC/DC converter.

A. Reconstruction Filters

The reconstruction filters consist of input buffers that provide the correct DC biasing for the preceding DAC in the digital baseband controller, and a low-pass filter for removing the unwanted high frequency components from the baseband input waveform.
The filter inputs are adapted for use with a current-source type of input signal.

B. IQ-modulator

The IQ-modulator receives the incoming I and Q analog baseband signals at baseband frequency and converts them to an intermediate frequency of 380MHz.

C. Variable Gain Amplifier (VGA)

Comprising two cascaded variable gain amplifiers, the VGA-together with the RF mixer- controls the power of the transmitter.
The first of these two amplifiers, the so-called QVGA, enables fine-tuning of the transmitter by varying the gain in 0.25dB steps, that is 0/0.25/0.5/0.75dB. The second amplifier provides a 54dB gain range in 1 dB steps (54steps = 55 levels).

D. IF Band Bass Filter (IFBP)

The IF filter suppresses spurious signals and eliminates unwanted frequency components generated in the IQ modulator and subsequently amplified in the VGA. The filter is tuned using an external RLC load as shown in Figure 3-12.

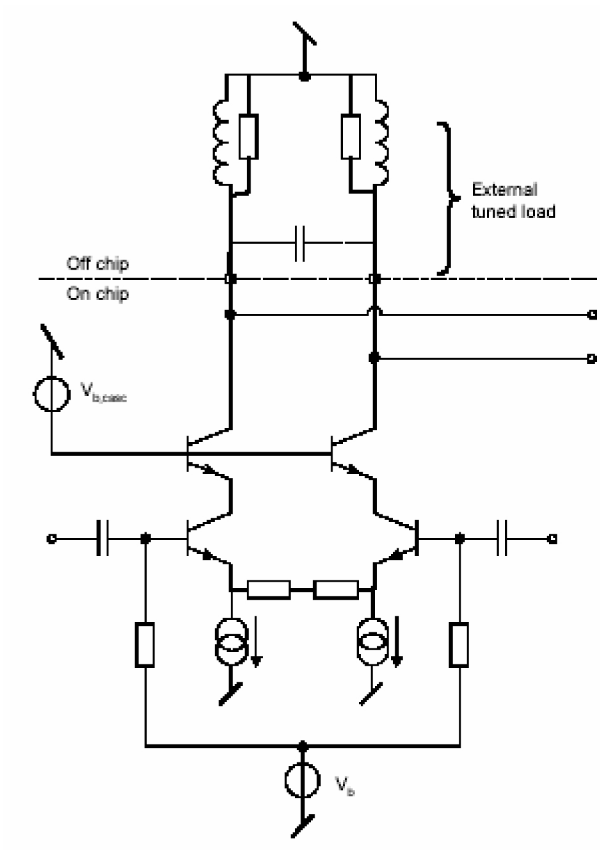


Figure 3-12. Principle Schematic of the IFBP.

E. RF Mixer and Buffer

The RF mixer converts the signal output from the IF BP filter from an intermediate frequency (IF) to the final radio frequency (RF). The mixer can be switched between three different gain levels: high gain (HG), medium gain (MG), and low gain (LG).
The LO buffer provides the buffering for either an internal LO signal generated within the internal RFPLL, or an external LO signal applied to the RFLO/RFLOBAR pins. External DC blocking is necessary for the external LO signal.
The RF buffer is used to drive an external PA stage. The buffer is of an open-collector design. The gain switching together with the VGA amplifier at IF will enable an output power control in 0.25 dB steps over no less than 80dB.
The programmable bias in the high and mid-gain settings is specified as a reduction of bias current from the maximum bias condition. It should achieve a reduction of bias current from the nominal value of 17mA to 3mA (signal ended) in 7 steps.

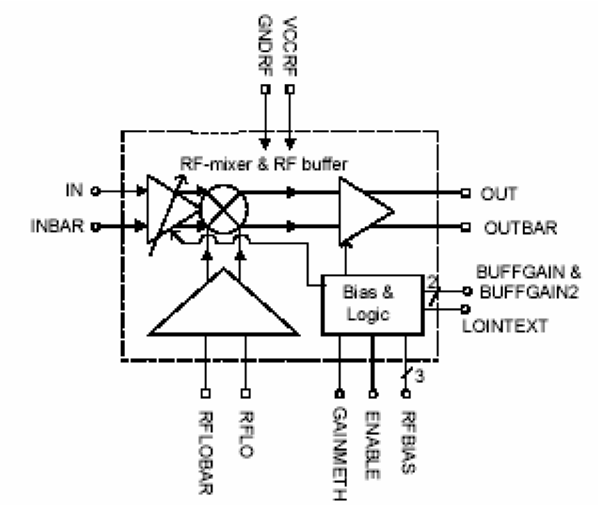


Figure 3-13. Block Diagram of RF Mixer and Buffer.

F. Power Amplifier

The N1630(RF9266) is a high-power, high-efficiency linear amplifier module targeting W-CDMA transmitter ASIC. The module is fully matched to 50(for easy system integration and utilizes advanced GaAs HBT process technology. The PA features an integrated RF power output detection network and is compatible with DC-DC converter operation in DC power management applications. Additionally, a variable bias-current allows the idle current to be adjusted for optimum performance at a given RF output power.

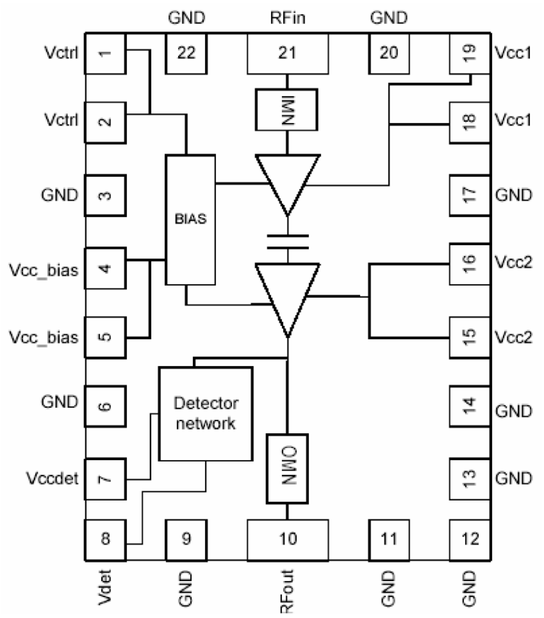


Figure 3-14. Block Diagram of W-CDMA power amplifier.

3.8.3 Frequency Generation

The Wopy (W-CDMA Receive ASIC) contains the active elements for a 13MHz VCXO, which is designed to be the reference frequency of the UE.

There are two synthesizers in the W-CDMA part of the radio, an intermediate frequency (IF) synthesizer and a radio frequency (RF) synthesizer. They generate the Intermediate Frequency Local Oscillator (IFLO) and Radio Frequency Local Oscillator (RFLO) signals. Both synthesizers are used in both the transmitter and the receiver, which gives the radio a fixed duplex distance of 190MHz.

The RF synthesizer is in the Wopy (W-CDMA Receive ASIC), except for the loop filter, which is external. The 13MHz clock is used as the reference, and the phase detector frequency is 200kHz. The programmable divider makes the RF synthesizer cover the 2300~2360MHz band.

The IF synthesizer is in the Wivi (W-CDMA Transmitter ASIC), except for the loop filter. The 13MHz is used as the reference, and the phase detector frequency is 1MHz. The IF VCO runs at 1520MHz given that the (programmable) reference divider is set to 13.

The synthesizers are controlled by Wanda (W-CDMA digital base-band coprocessor ASIC) via the serial bus to Wivi (W-CDMA Transmitter ASIC) and Wopy (W-CDMA Receive ASIC).

A. IF PLL

The IF LO frequency synthesis comprises the four following parts:

- Input buffer: A 13MHz input buffer with DC-biasing provided at source.
- VCO: Operating on 1.52GHz which is 4times the TX-IF frequency (380MHz) and 8 times the RX-IF (190MHz), this is a fully integrated balanced LC oscillator with on-chip resonator. On-chip varactor are used to tune the VCO frequency.
- Prescaler
- Phase-detector with charge pump

For maintaining check on the VCO center frequency, the tuning voltage is set to Vcc/2. External DC blocking capacitors must be used on the IFLO/IFLOBAR signals.

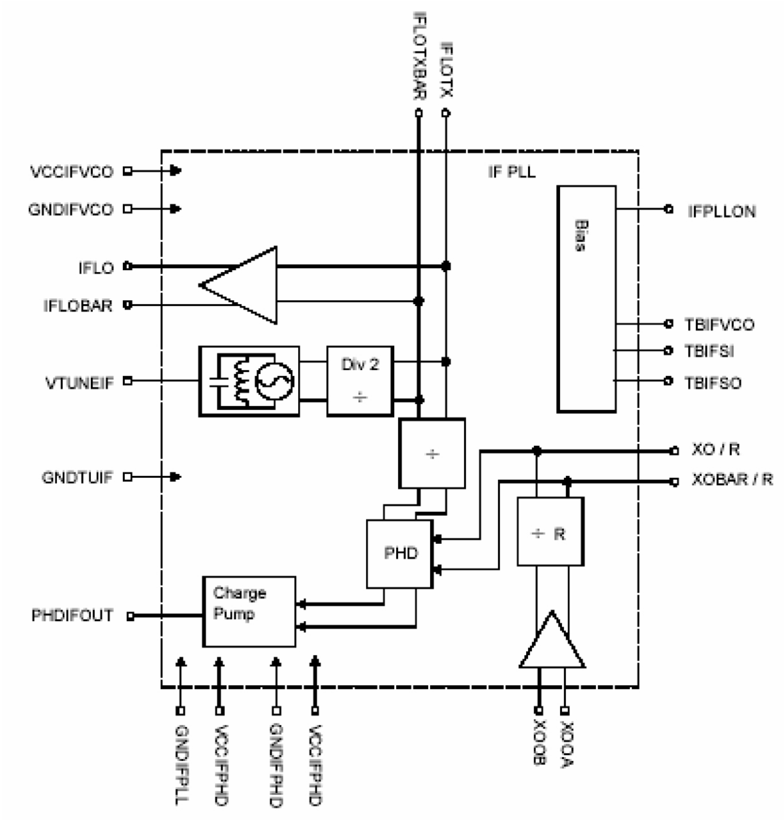
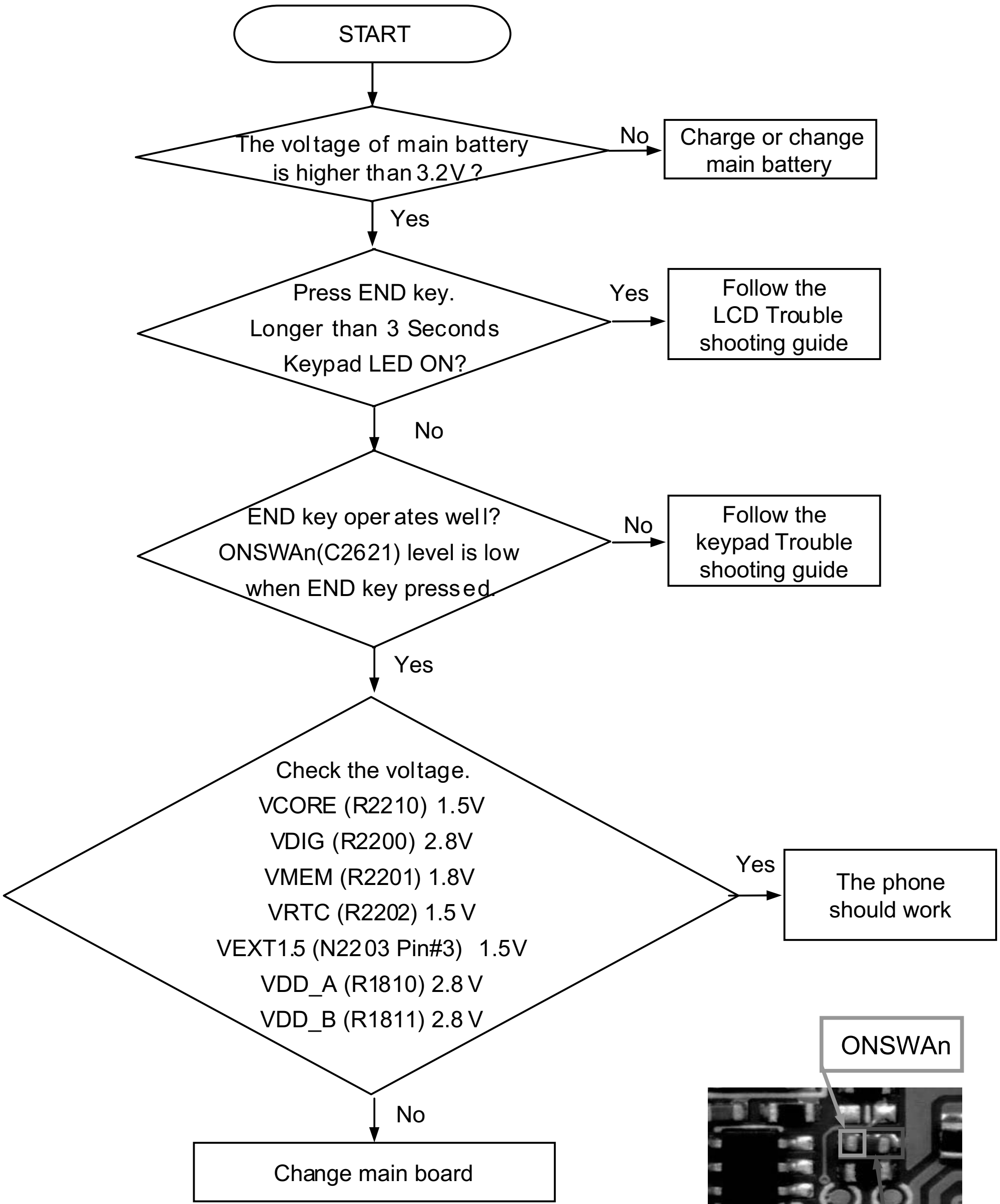
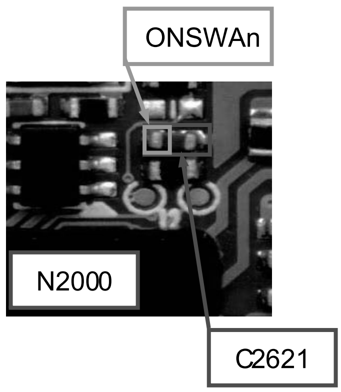


Figure 3-15. Block Diagram of Frequency Synthesizer Part(IF PLL).

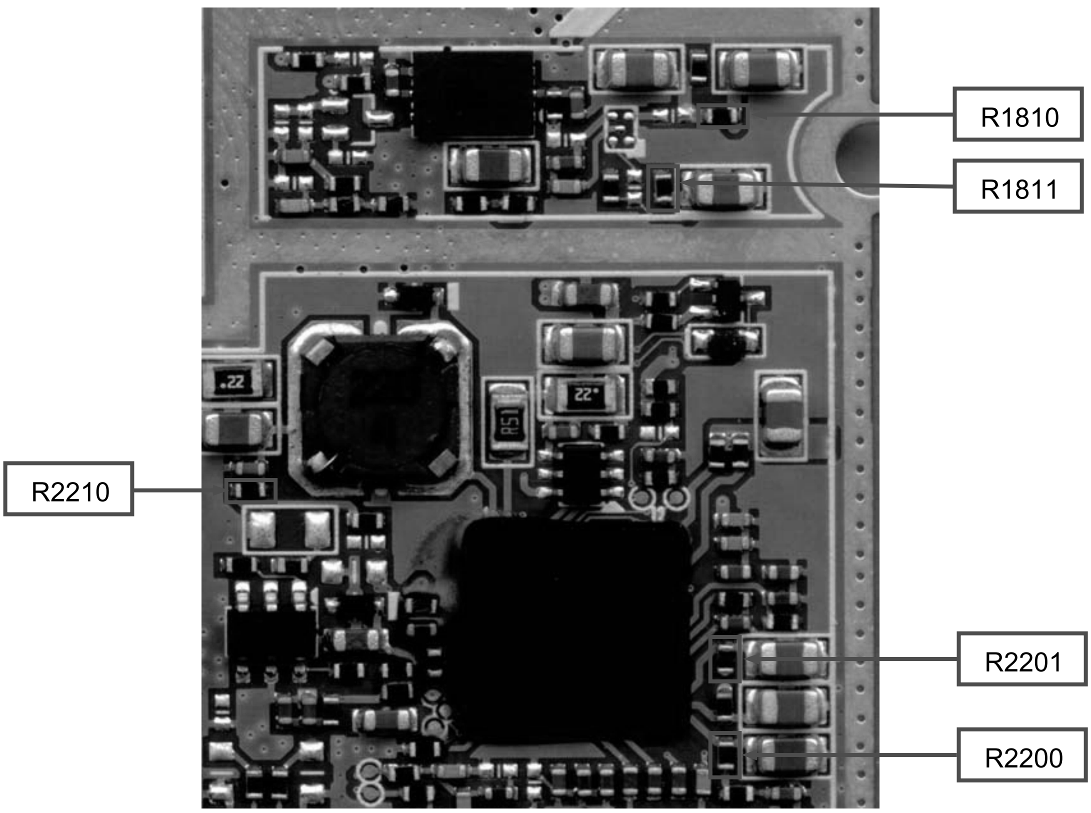
4. TROUBLE SHOOTING

4.1 Power ON Trouble



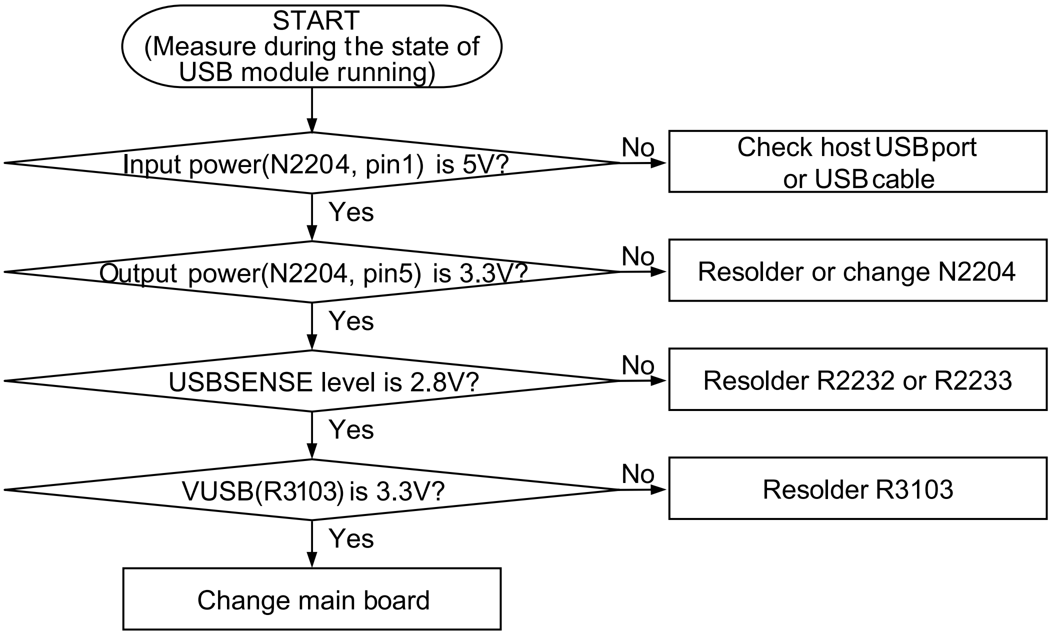


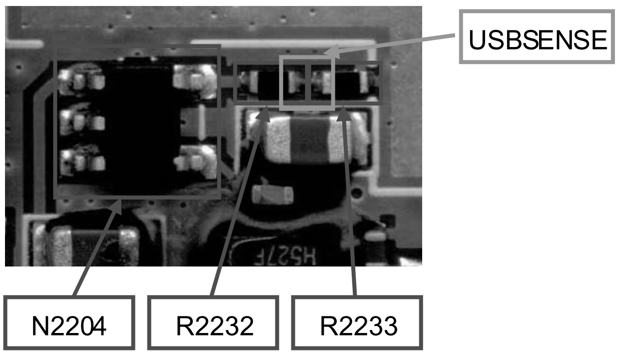
< Main Board - Top side >

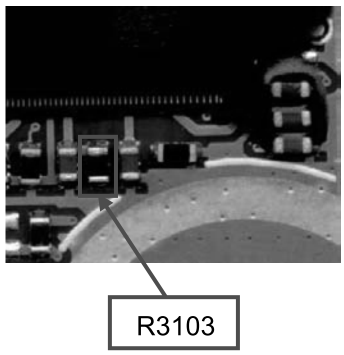


< Main Board - Bottom side >

4.2 USB Trouble



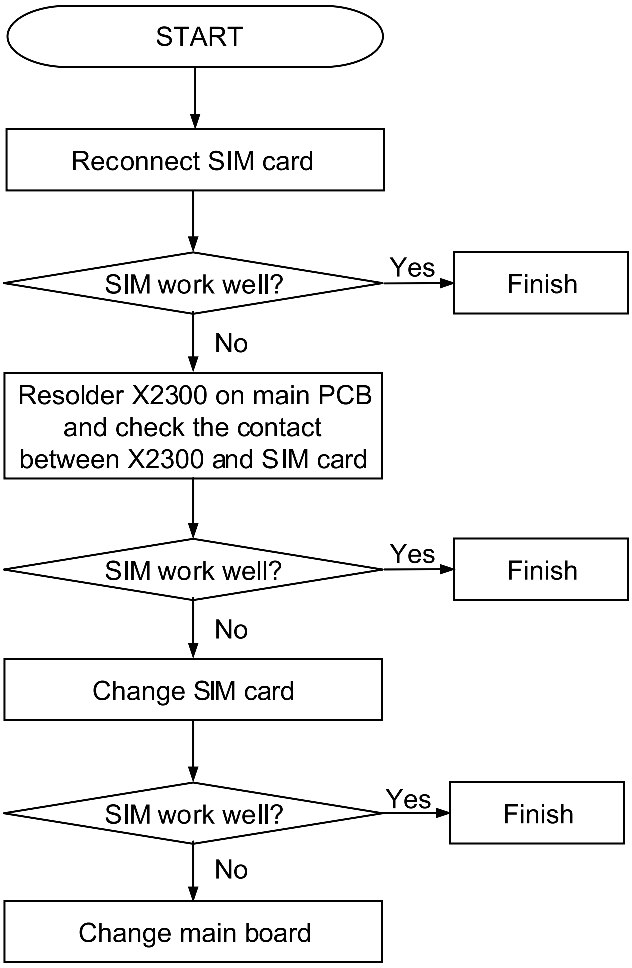


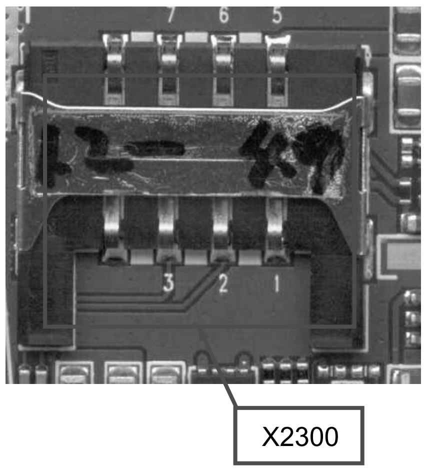


4.3 SIM Detect Trouble

・SIM control path

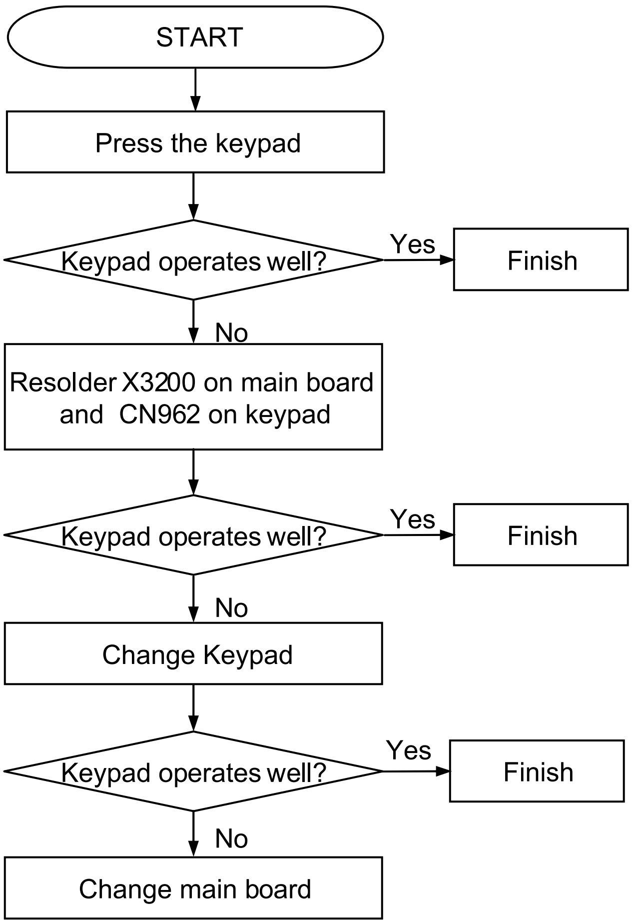
- MARITA generates SIM interface signals(2.75V level) to VINCENNE.
- Vincenne converts SIM interface signals to 1.8V/3V.

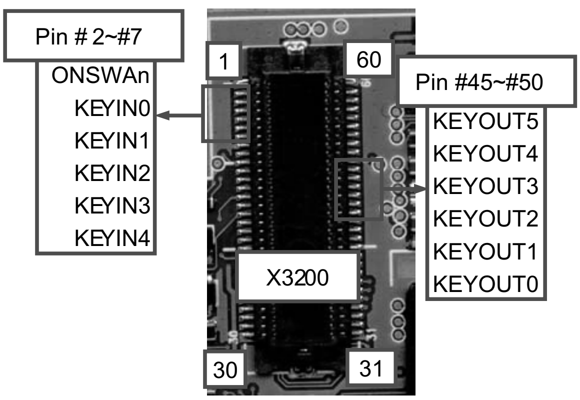


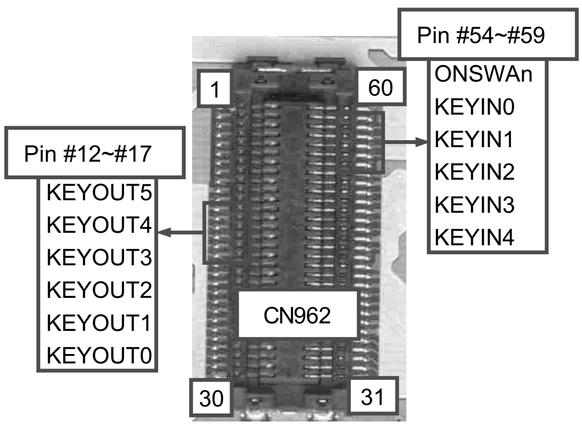


4.4 Keypad Trouble

• Keypad signals go to MARITA and VINCENNE through board-to-board connector.

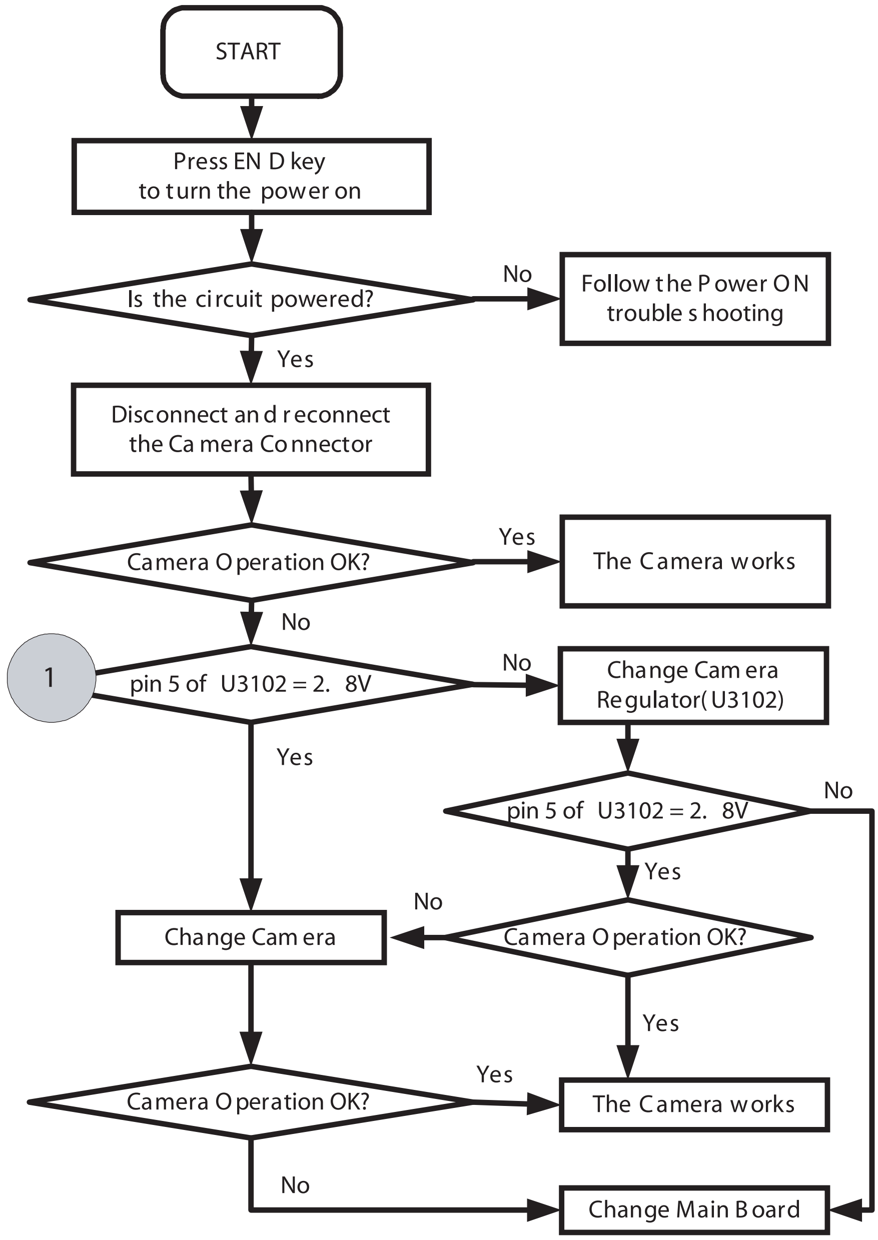




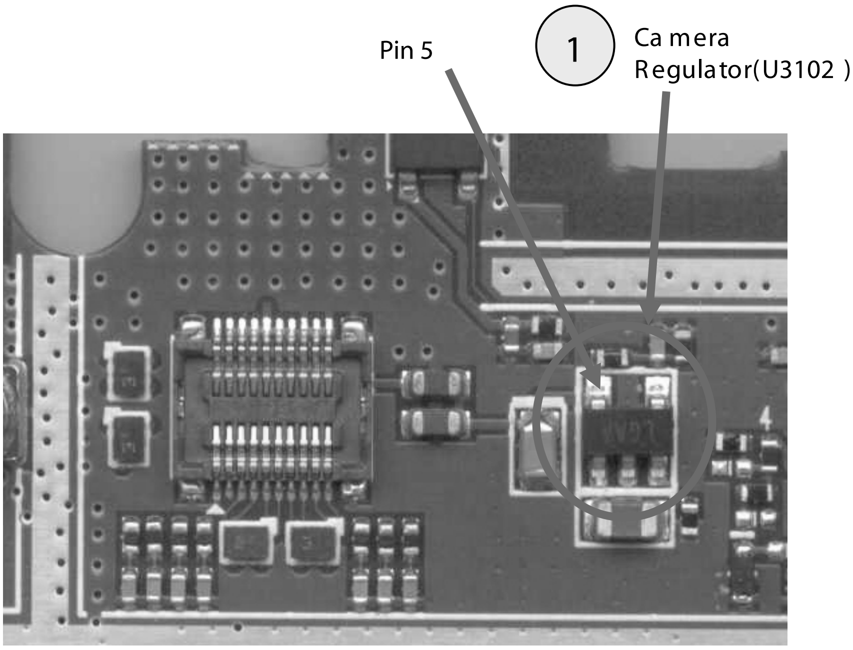


4.5 Camera Trouble

Camera control signals are generated by Marita

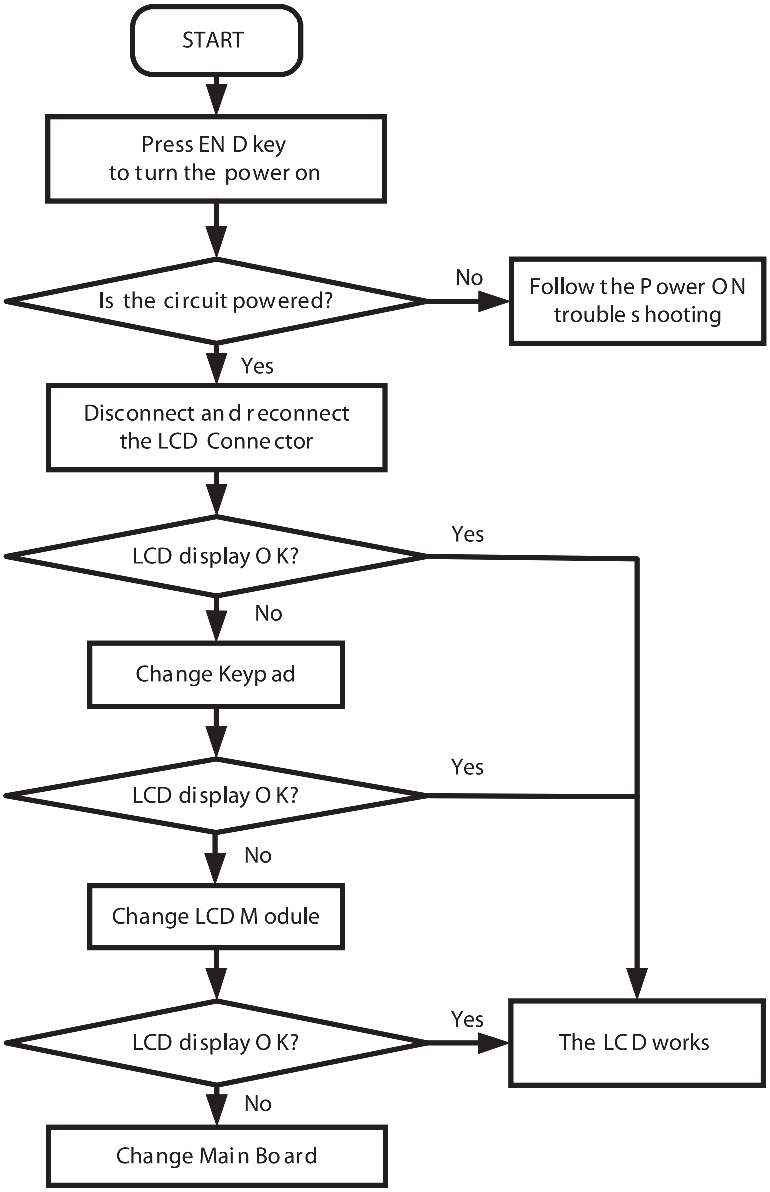


Camera control signals are generated by Marita



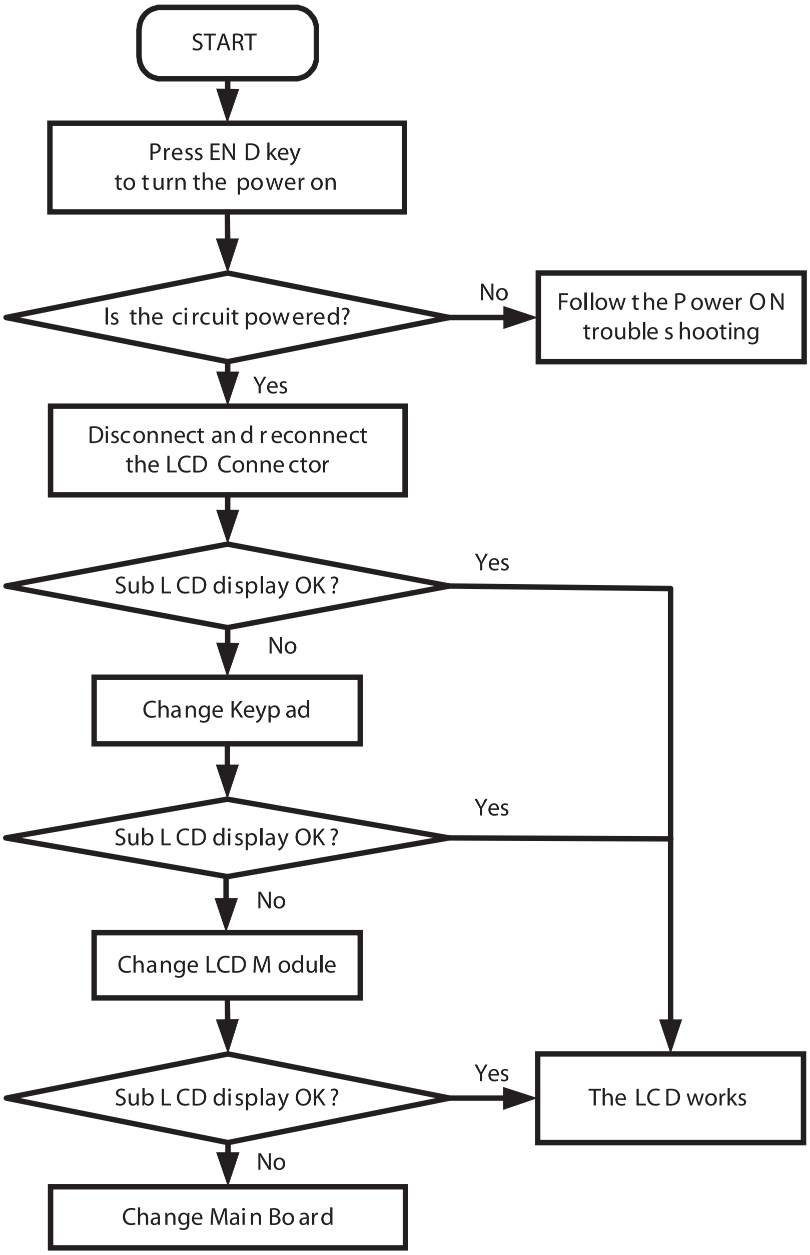
4.6 Main LCD Trouble

LCD control signals are generated by Marita.

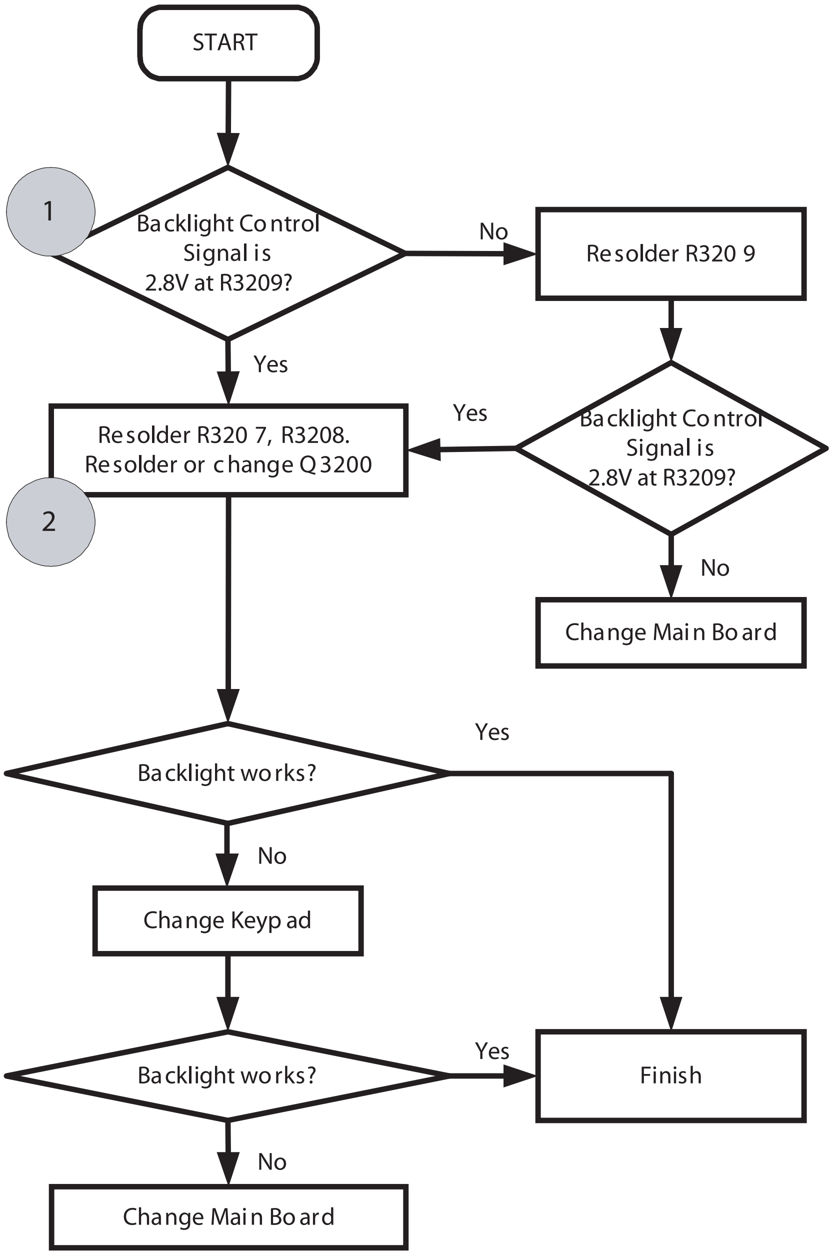


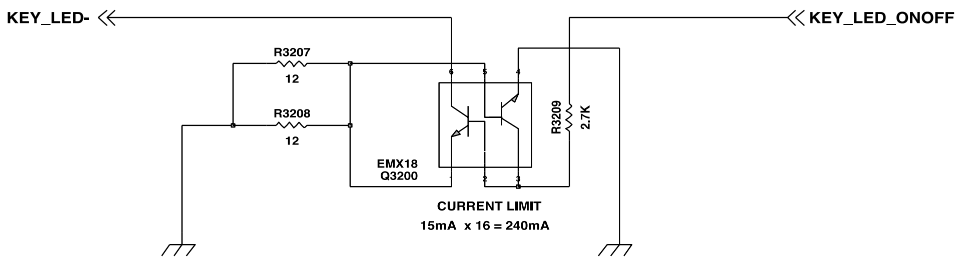
LCD control signa ls a re g enerated by M arita.

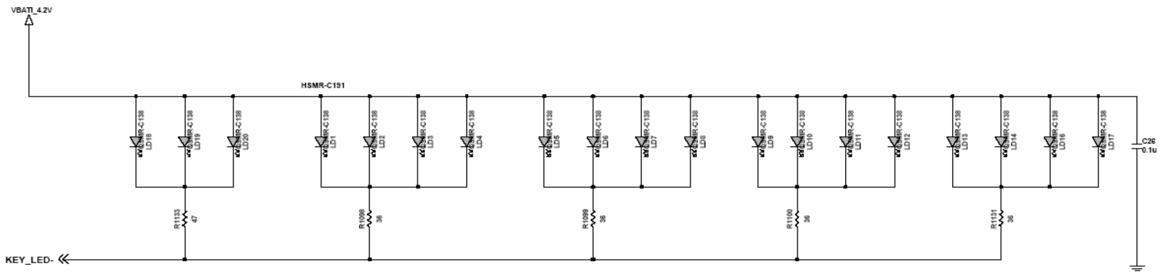
4.7 Sub LCD Trouble

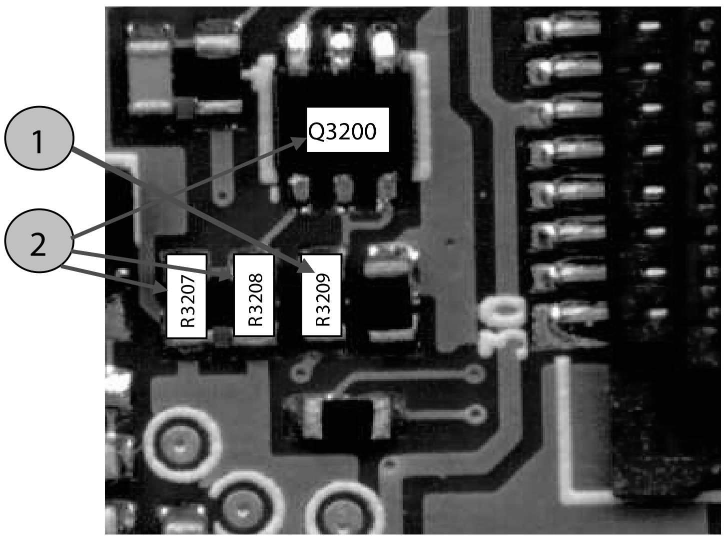


4.8 Keypad Backlight Trouble

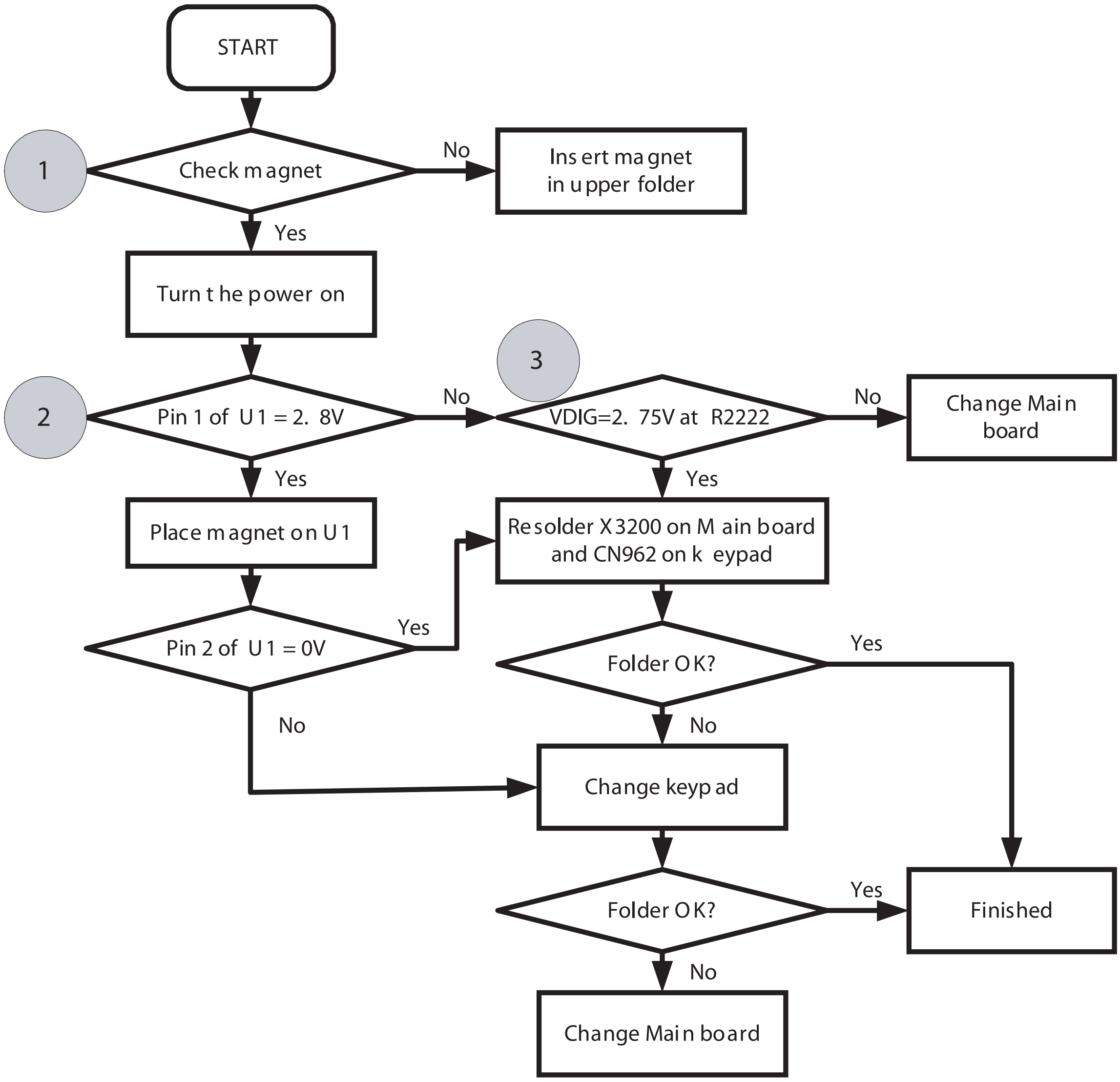


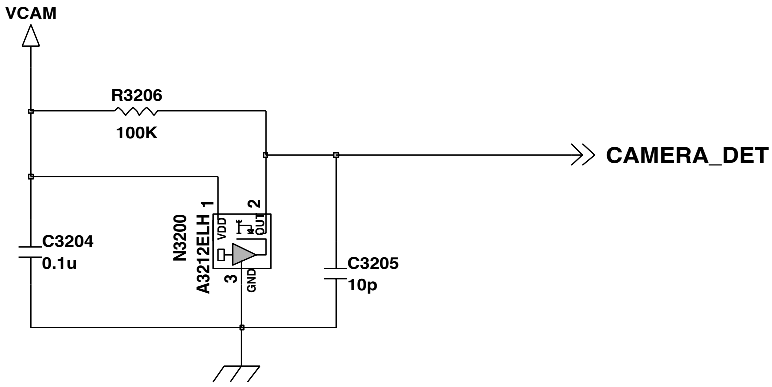

KEY_LED-
KEY_LED_ONOFF
R3207
12
R3208
12
R3209
2.7K
EMX18
Q3200
CURRENT LIMIT
15mA x 16 = 240mA

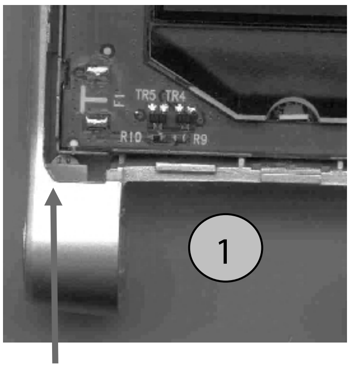

VBATI_4.2V
HSMR-C191
KEY_LED-


1
2
Q3200
R3207
R3208
R3209

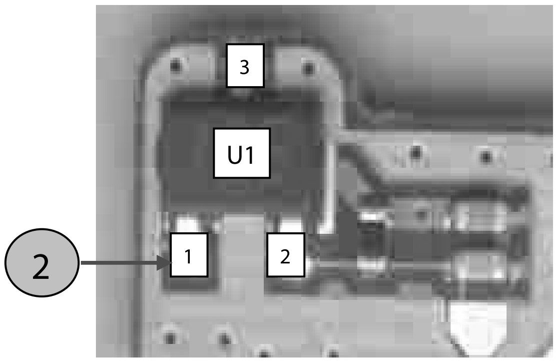
4.9 Folder ON/OFF Trouble

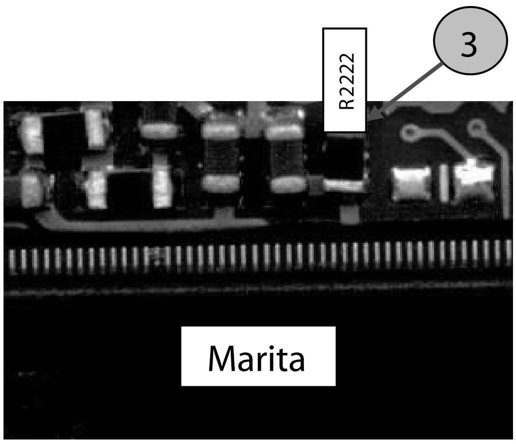




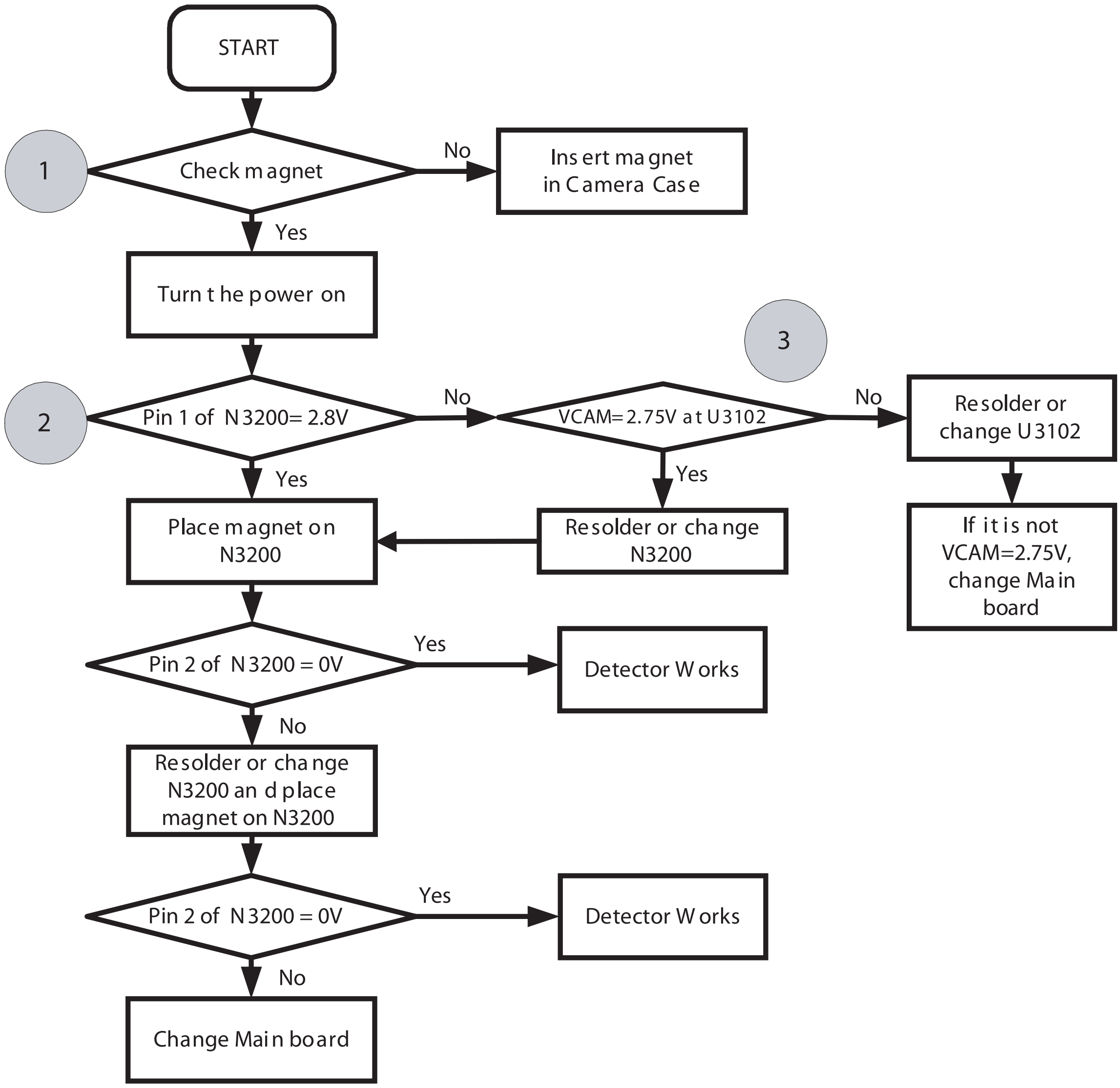


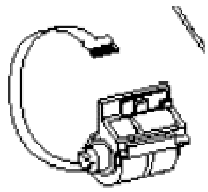
Be sure that magnet is here





4.10 Camera Detection Trouble





1

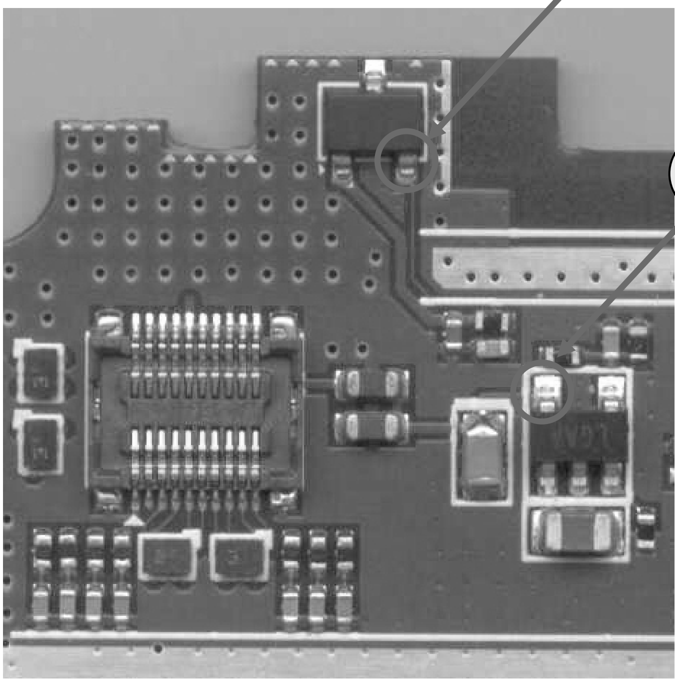
Be sure that magnet is in camera module

2

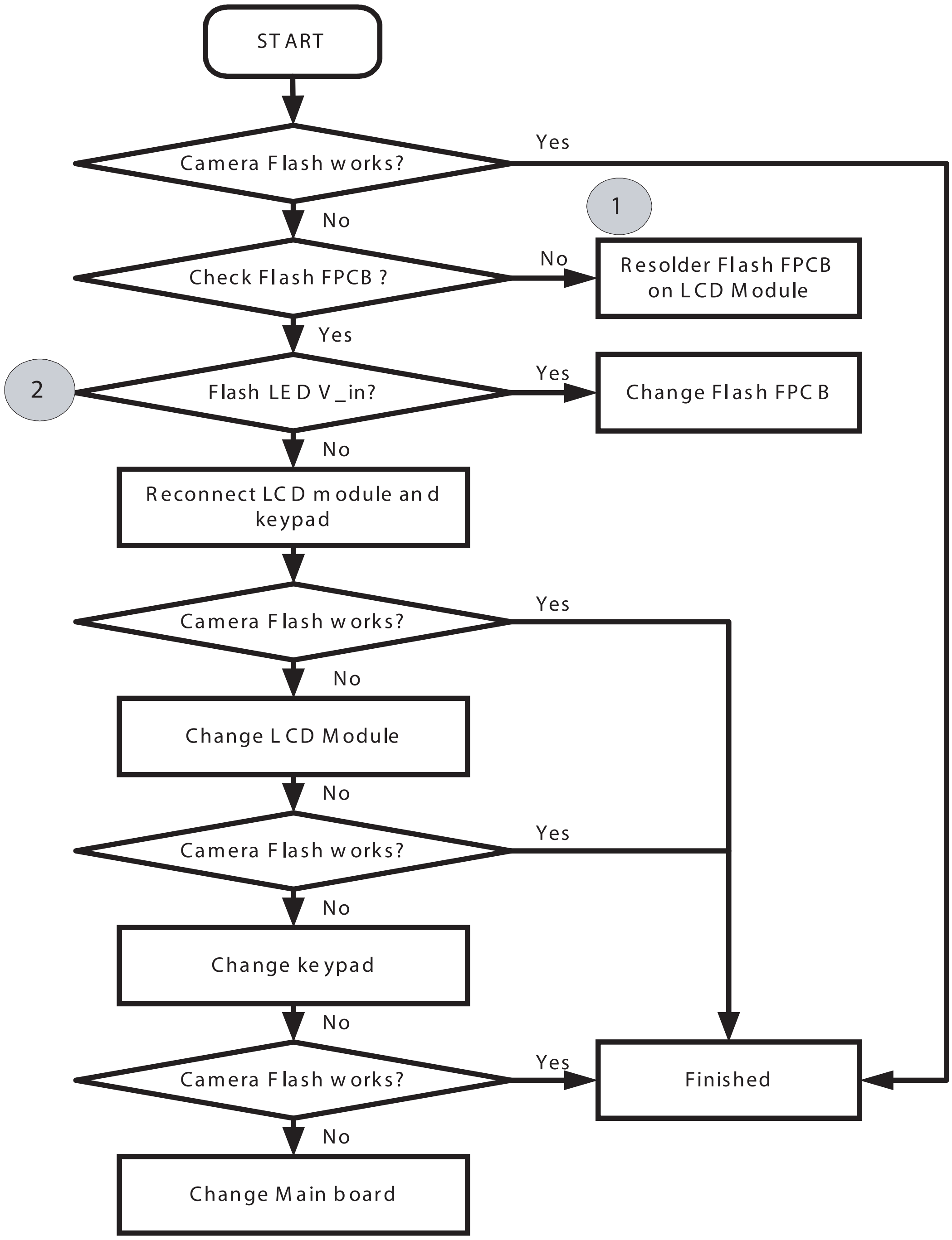
Pin 2 of N3200

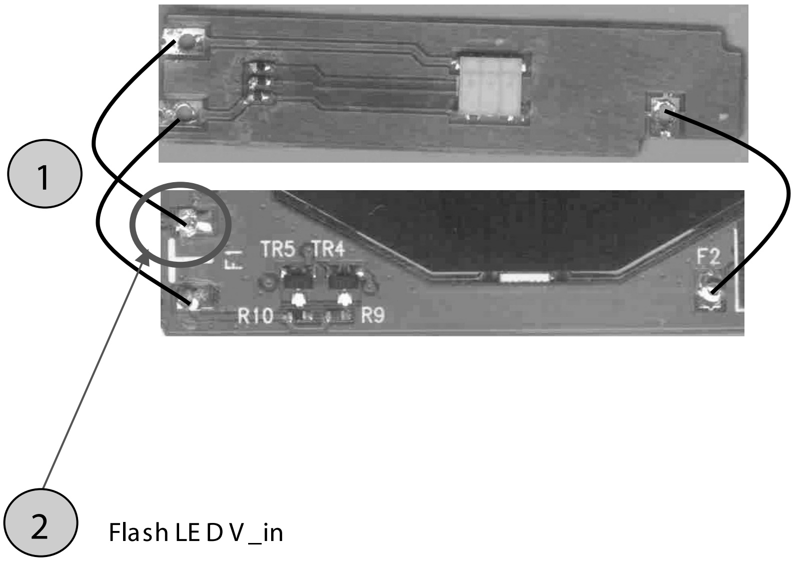
3

VCAM=2.75V at U3102



4.11 Camera Flash Trouble



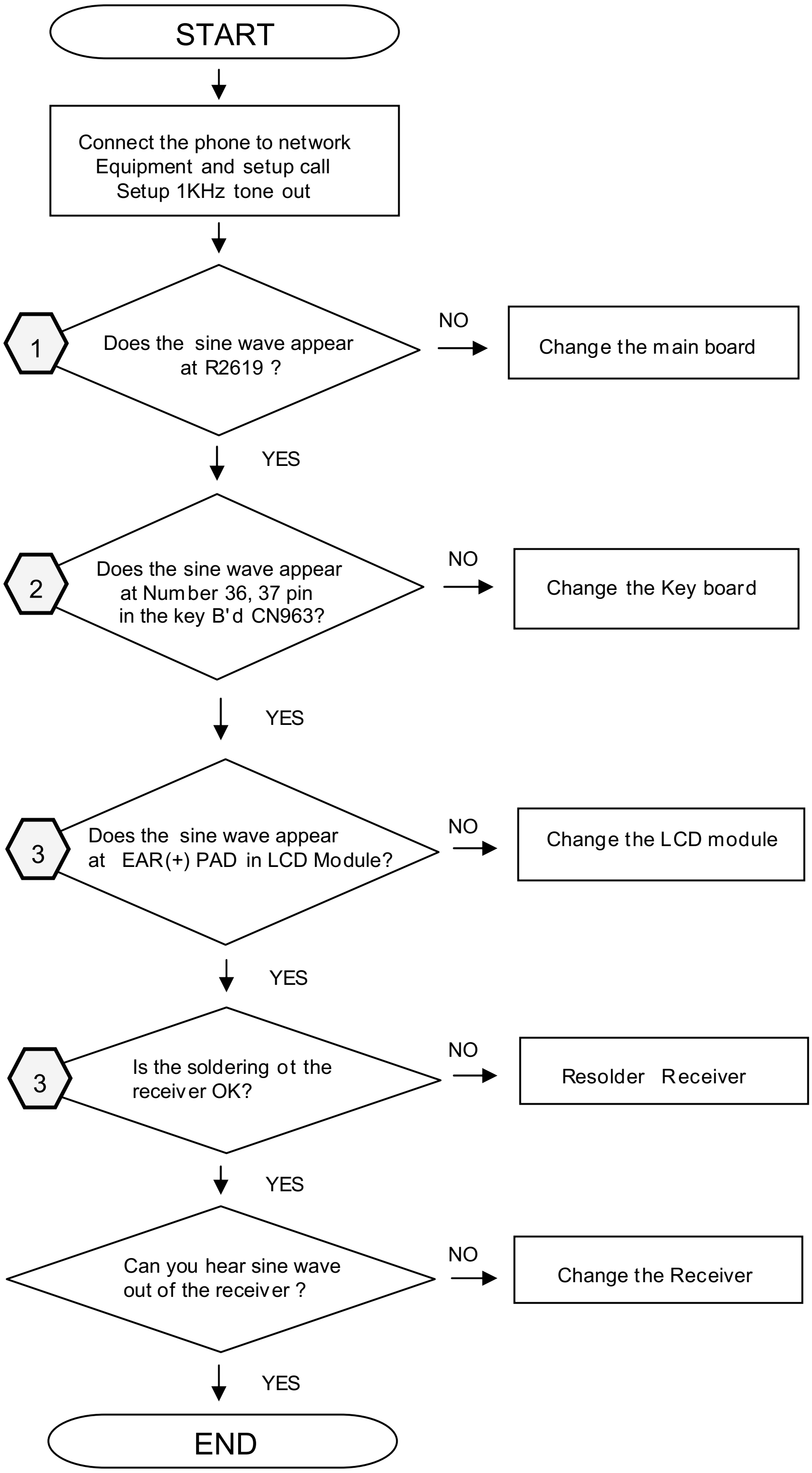


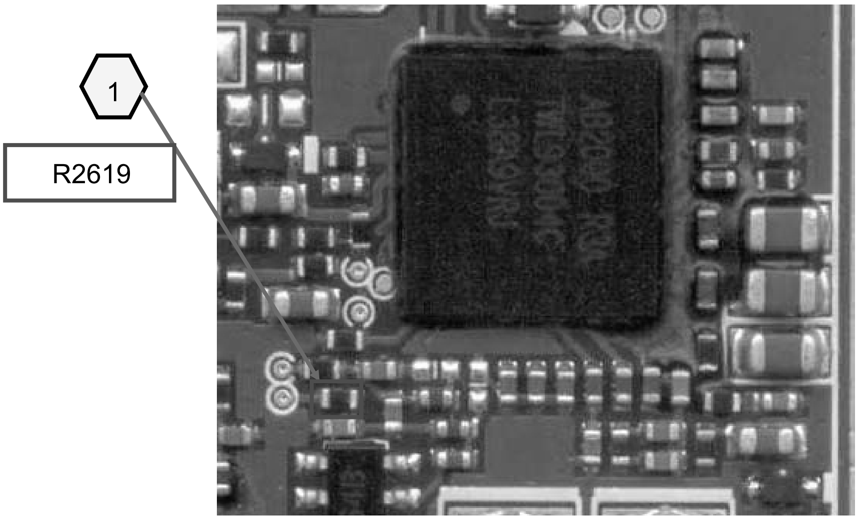
Flash LE D V _in

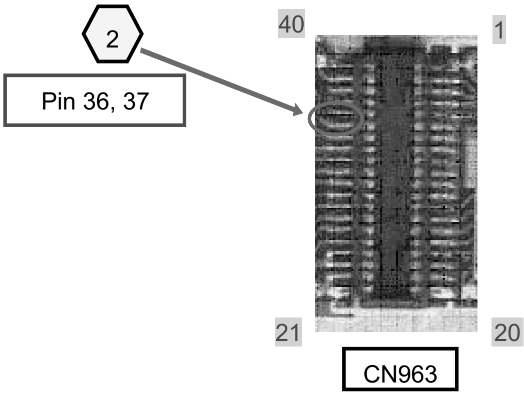
4.12 Audio Trouble Shooting

A. Receiver

- **Signals to the receiver**
  - – Receiver signals are generated at Vincenne
    - BEARP, BEARM
  - – Receiver path :
    - 1. Vincenne (BEARP, BEARM) ->
    - 2. X3200 on main board ->
    - 3. CN962 on key PCB ->
    - 4. CN963 on key PCB ->
    - 5. LCD Module ->
    - 6. Receiver
- Note : It is recommanded that engineer should check the soldering of R, L, C along the corresponding path before every step.


START
Connect the phone to network Equipment and setup call Setup 1KHz tone out
1
Does the sine wave appear at R2619 ?
NO
Change the main board
YES
2
Does the sine wave appear at Number 36, 37 pin in the key B'd CN963?
NO
Change the Key board
YES
3
Does the sine wave appear at EAR(+) PAD in LCD Module?
NO
Change the LCD module
YES
3
Is the soldering ot the receiver OK?
NO
Resolder Receiver
YES
Can you hear sine wave out of the receiver ?
NO
Change the Receiver
YES
END

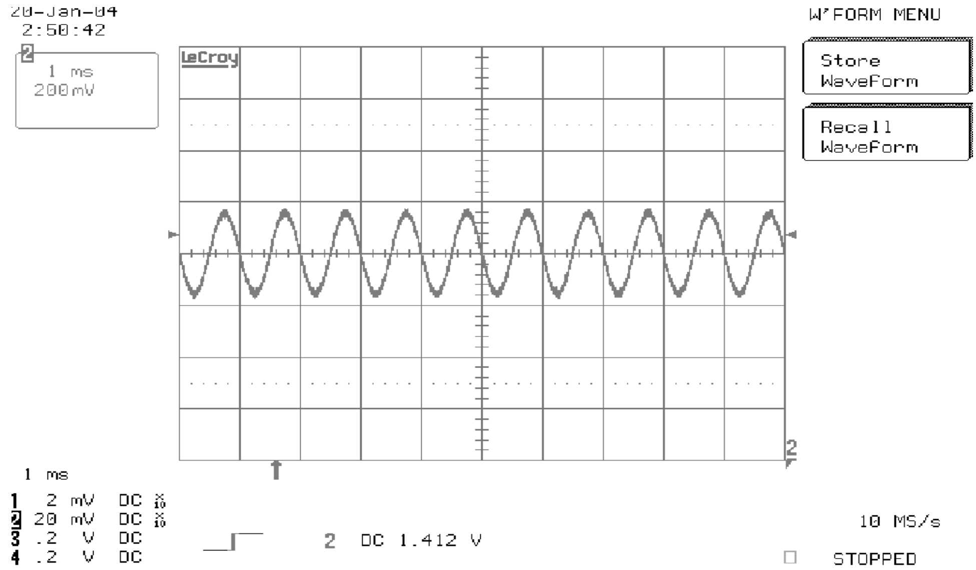

1
R2619


2
Pin 36, 37
40
1
21
20
CN963


3
+
SPK
EAR

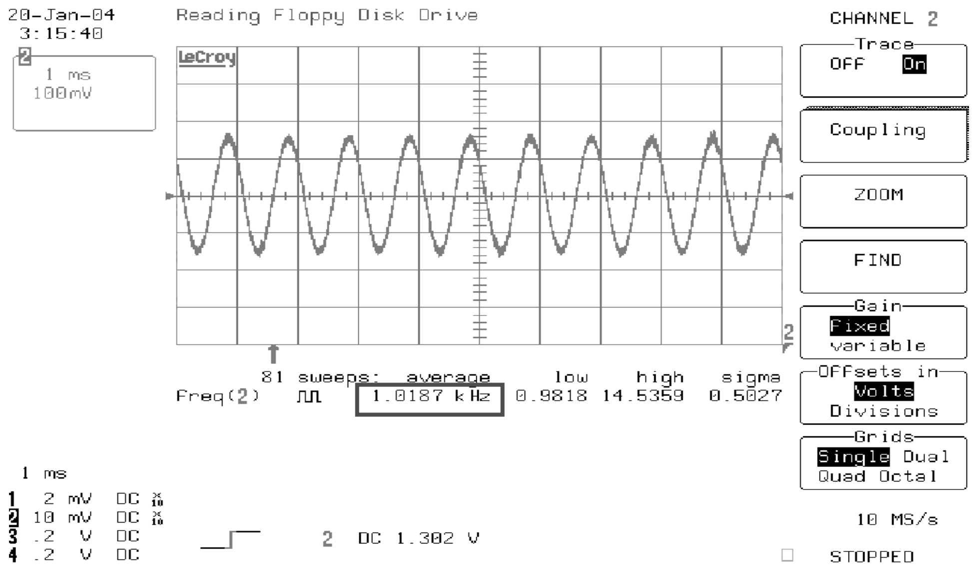
1

2



Measured 1khz Sine Wave Signal

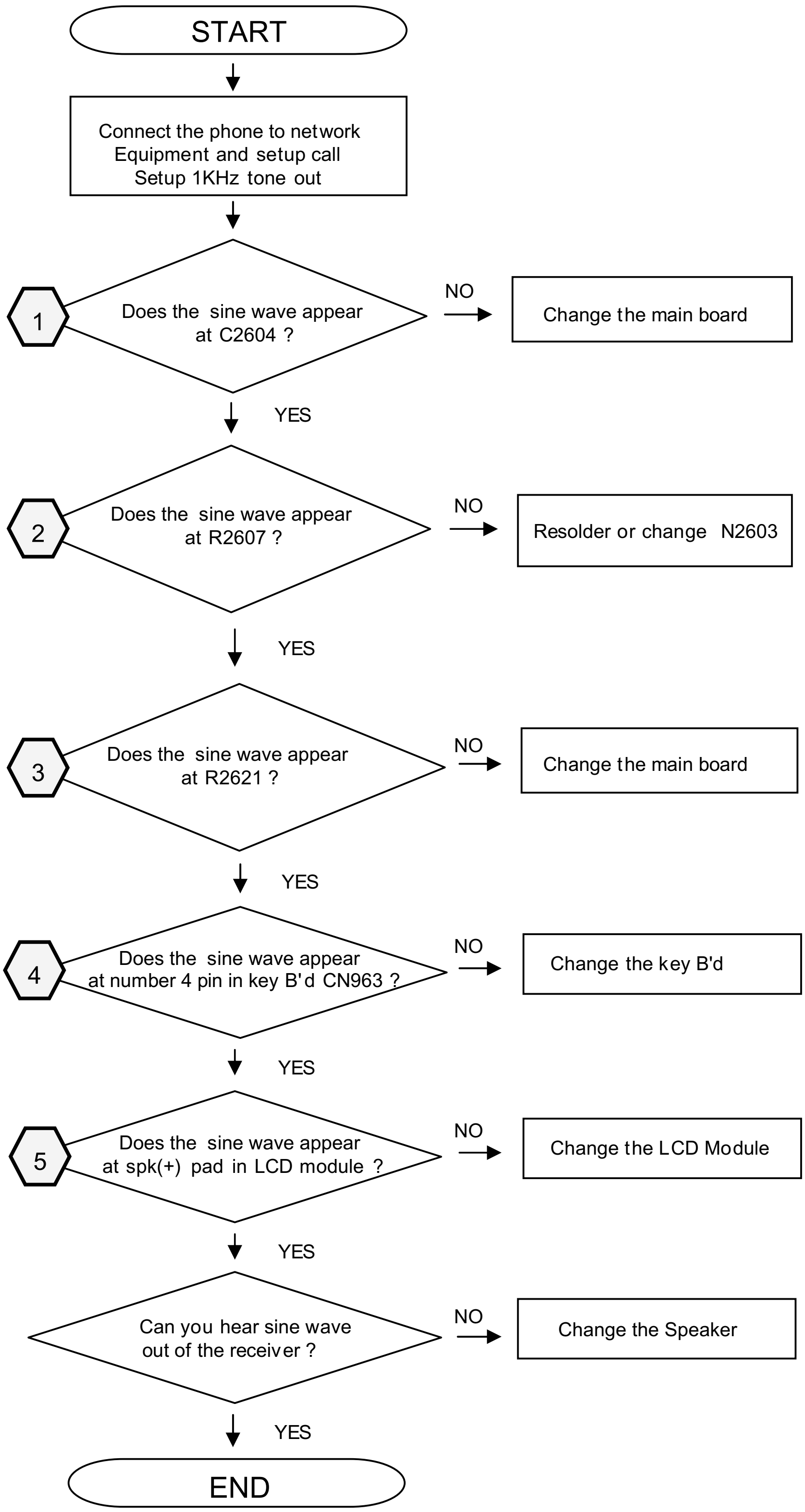
3

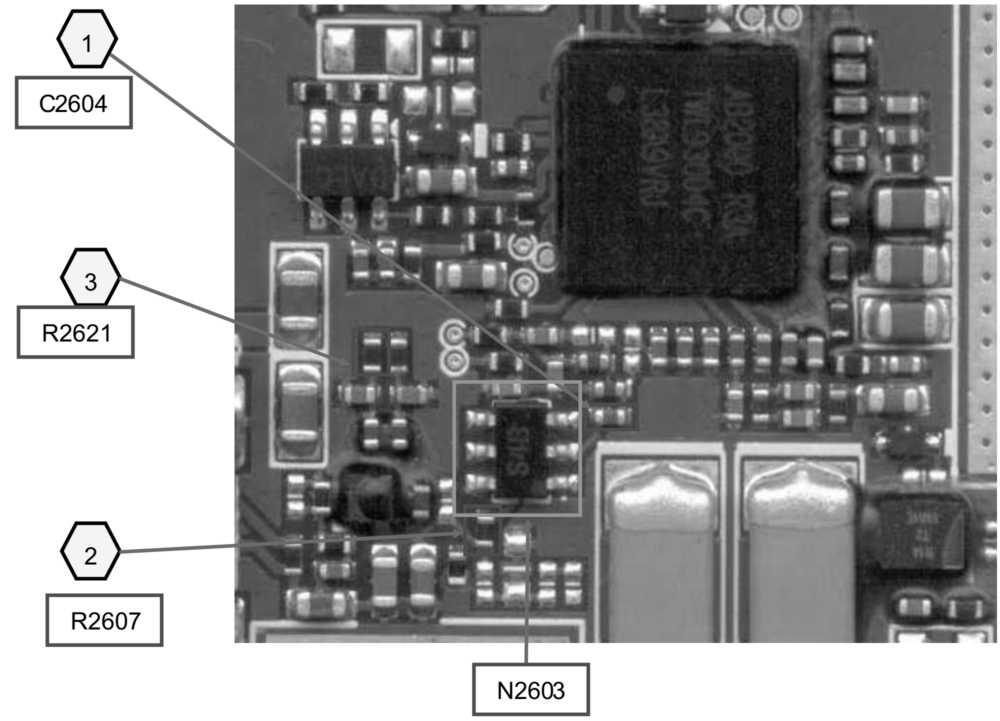


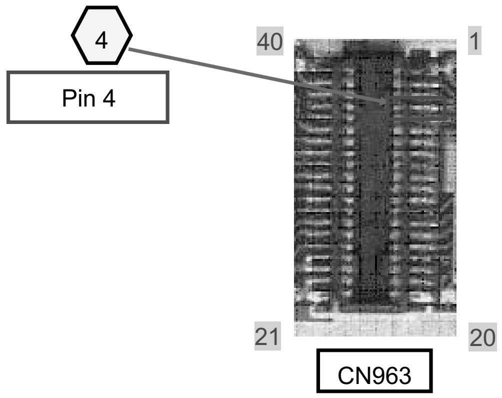
Measured 1khz Sine Wave Signal

B. Speaker (Voice Loud Speaker, Midi, MP3, Key Tone)

- Signals to the speaker
  – Speaker signals are generated at Vincenne
    - BEARP
  – Speaker path :
    - 1. Vincenne (BEARP) ->
    - 2. C2604 on main board ->
    - 3. N2603(ADG) on main board ->
    - 4. N2601(Audio Amp) on main board ->
    - 5. CN963 on key PCB ->
    - 6. LCD Module ->
    - 7. Speaker
- Note : It is recommanded that engineer should check the soldering of R, L, C along the corresponding path before every step.

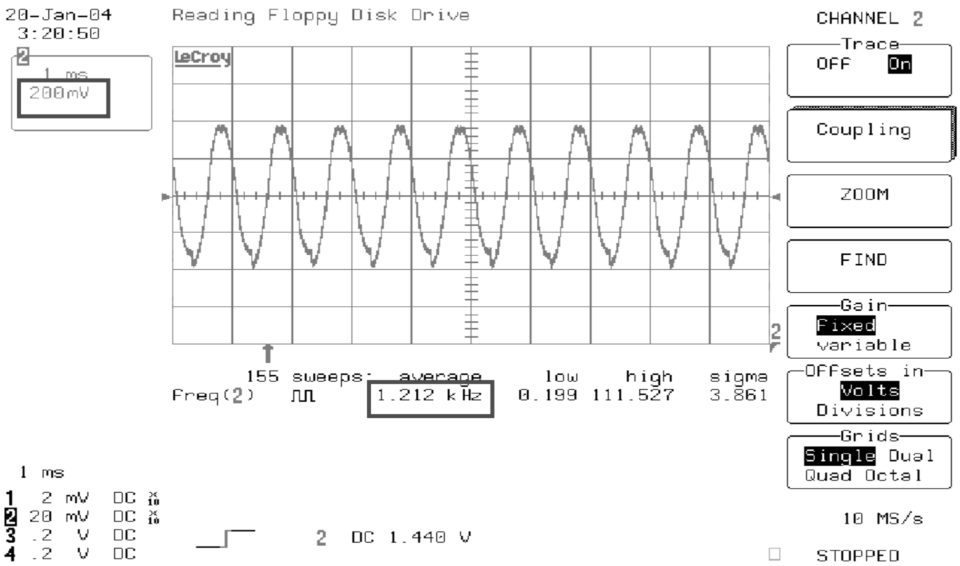

START
Connect the phone to network
Equipment and setup call
Setup 1KHz tone out
1
Does the sine wave appear
at C2604 ?
NO
Change the main board
YES
2
Does the sine wave appear
at R2607 ?
NO
Resolder or change N2603
YES
3
Does the sine wave appear
at R2621 ?
NO
Change the main board
YES
4
Does the sine wave appear
at number 4 pin in key B'd CN963 ?
NO
Change the key B'd
YES
5
Does the sine wave appear
at spk(+) pad in LCD module ?
NO
Change the LCD Module
YES
Can you hear sine wave
out of the receiver ?
NO
Change the Speaker
YES
END


1
C2604
3
R2621
2
R2607
N2603


4
Pin 4
40
1
21
20
CN963


5
+
SPK
EAR

5



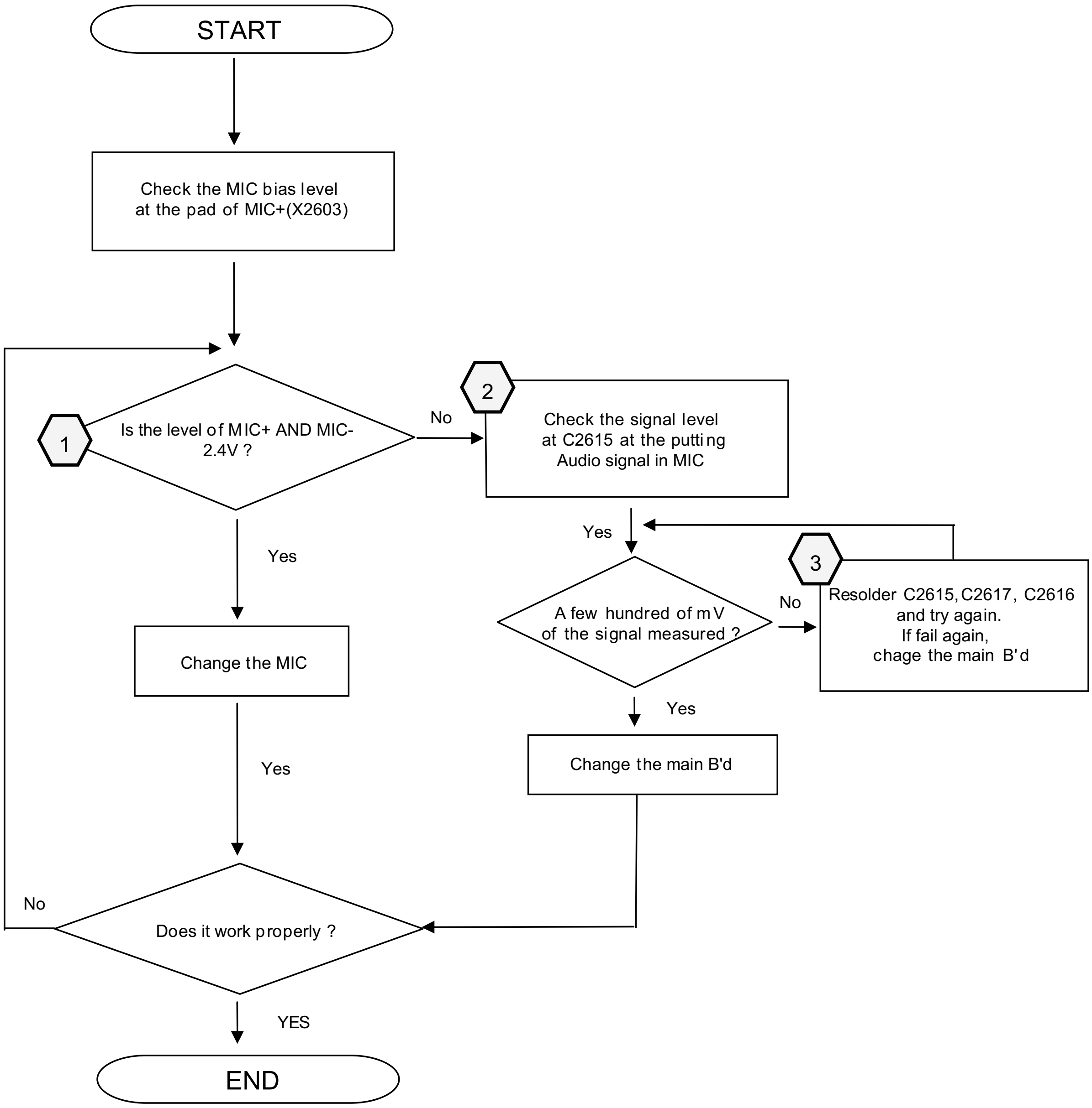
Measured 1khz Sine Wave Signal

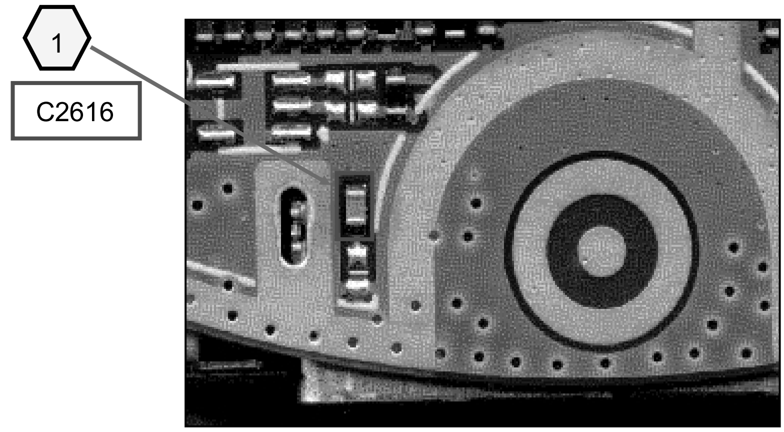
C. Microphone (Voice call, Voice Recorder, Video Recorder)

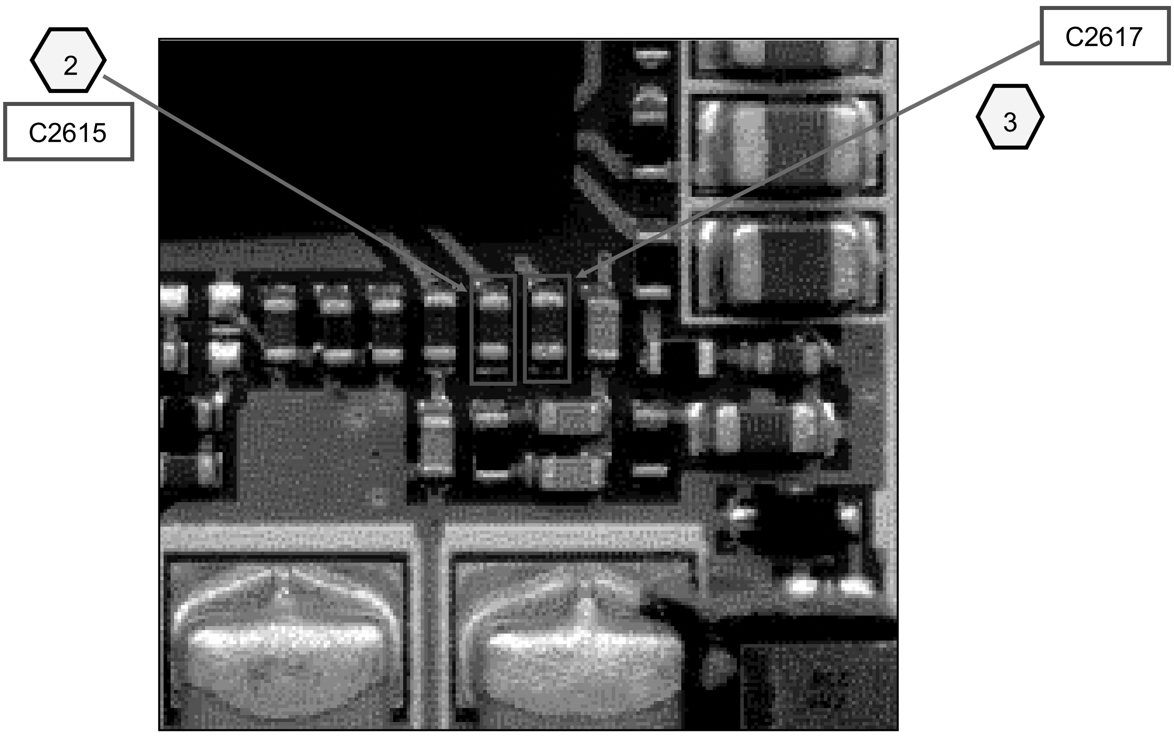
• Microphone Signal Flow
  – MIC is enable by MIC Bias
  – MICBAS, MICIP, MICIN signals to ABB (Vincenne)

• Check Points
  – Microphone bias
  – Audio signal level of the microphone
  – Soldering of components

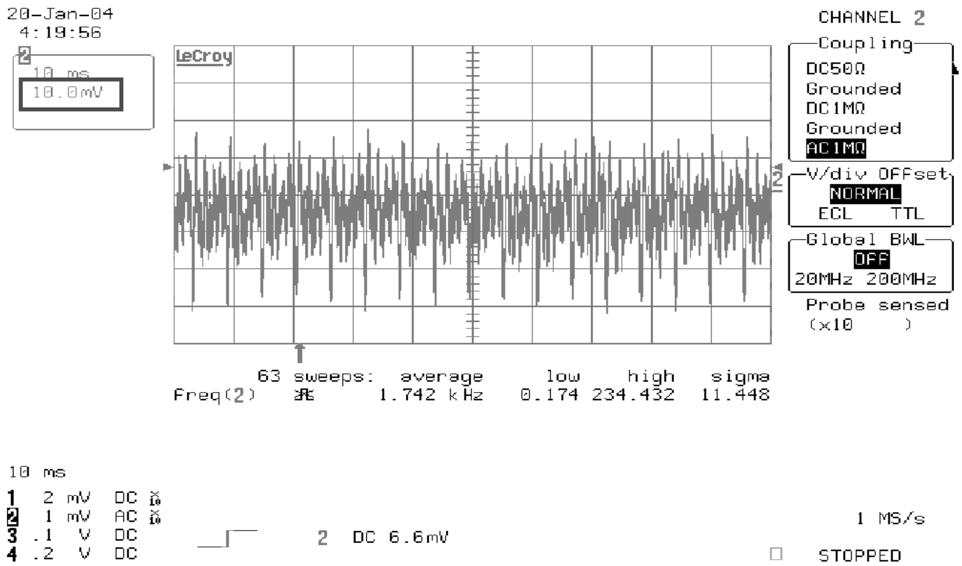
• Signal from the mic
  – MIC ->
  – N2602(TJATTE2) on main board ->
  – C2615 on main board ->
  – Vincenne


START
Check the MIC bias level at the pad of MIC+(X2603)
1
Is the level of MIC+ AND MIC- 2.4V ?
No
2
Check the signal level at C2615 at the putting Audio signal in MIC
Yes
Yes
3
A few hundred of mV of the signal measured ?
No
Resolder C2615, C2617, C2616 and try again. If fail again, chage the main B'd
Change the MIC
Yes
Change the main B'd
Yes
No
Does it work properly ?
YES
END


1
C2616

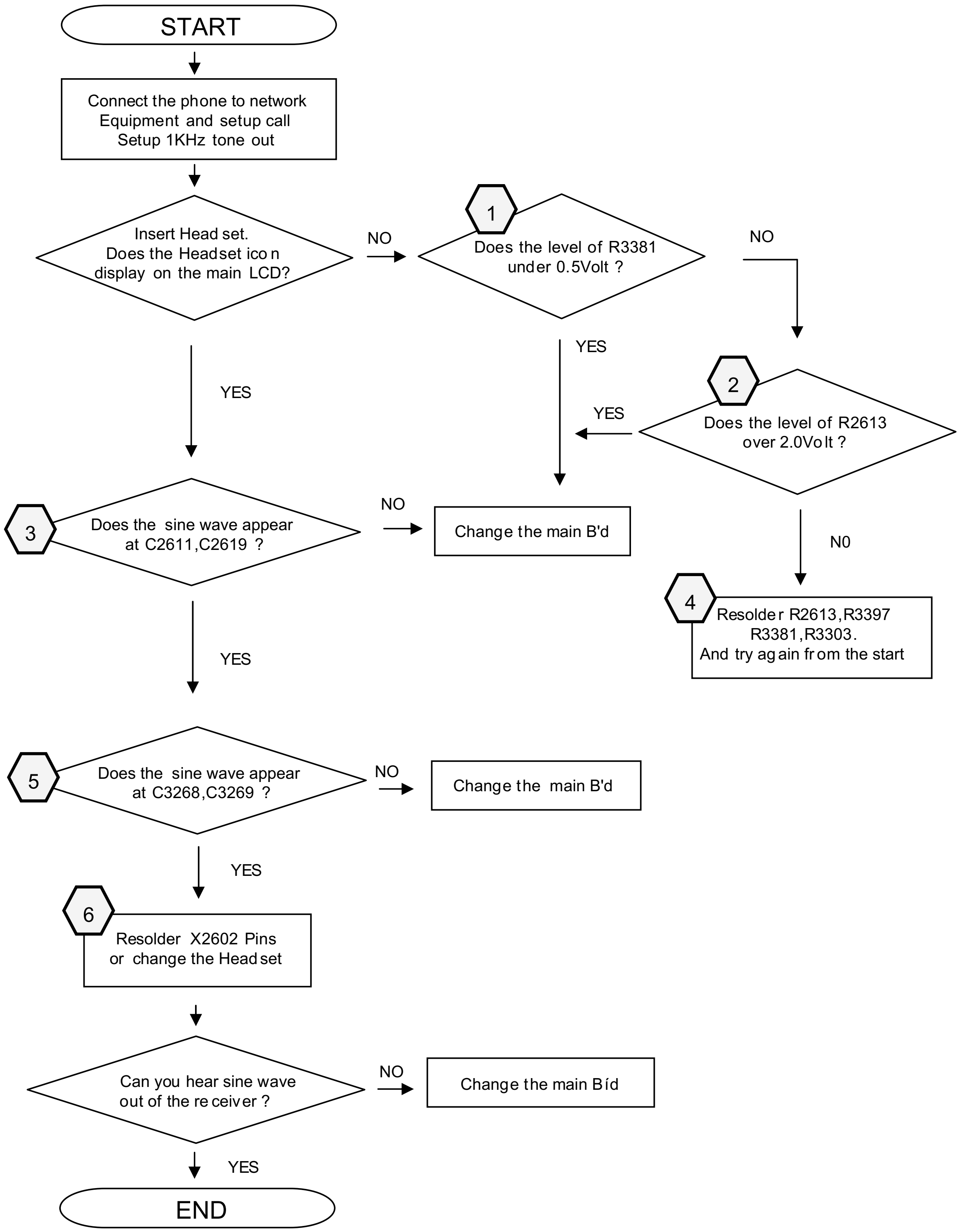

2
C2615
C2617
3

2

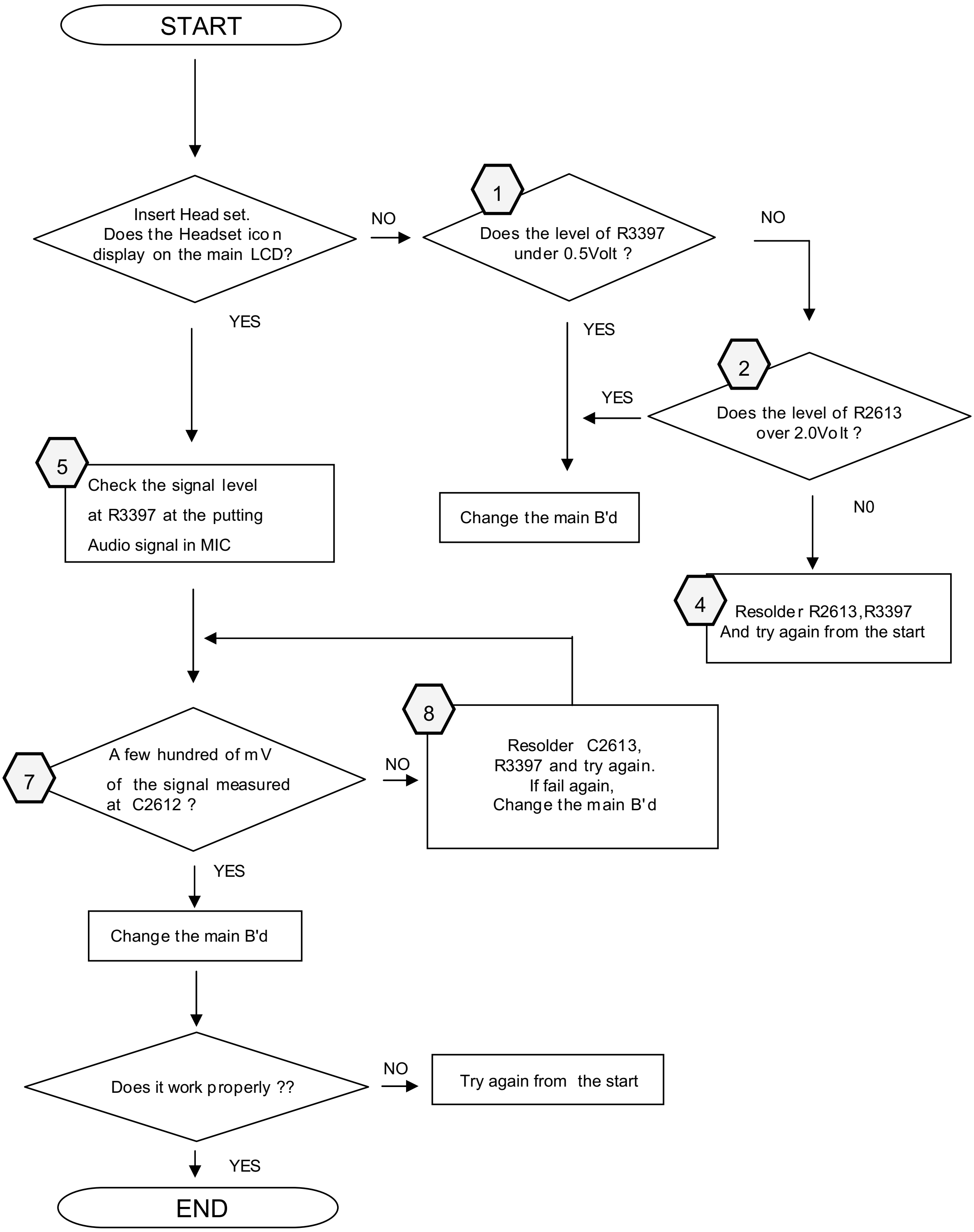


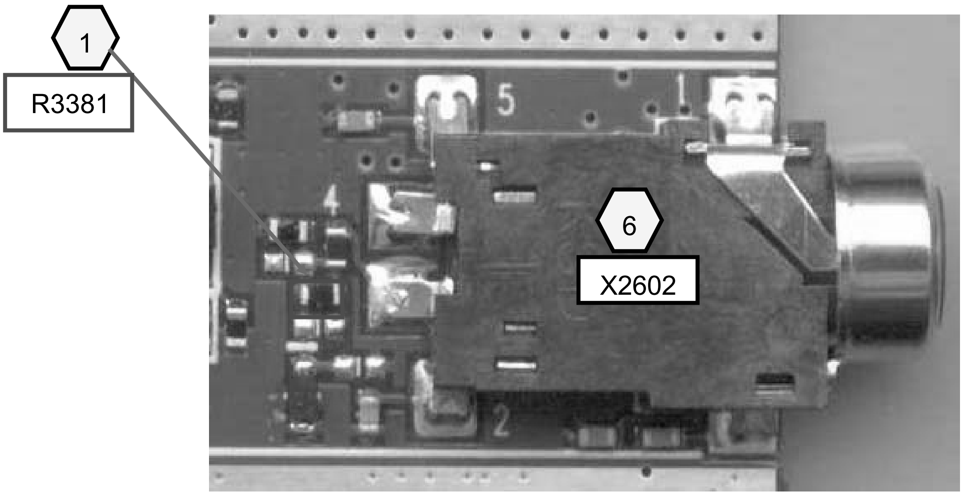
Measured Some Noise Signal

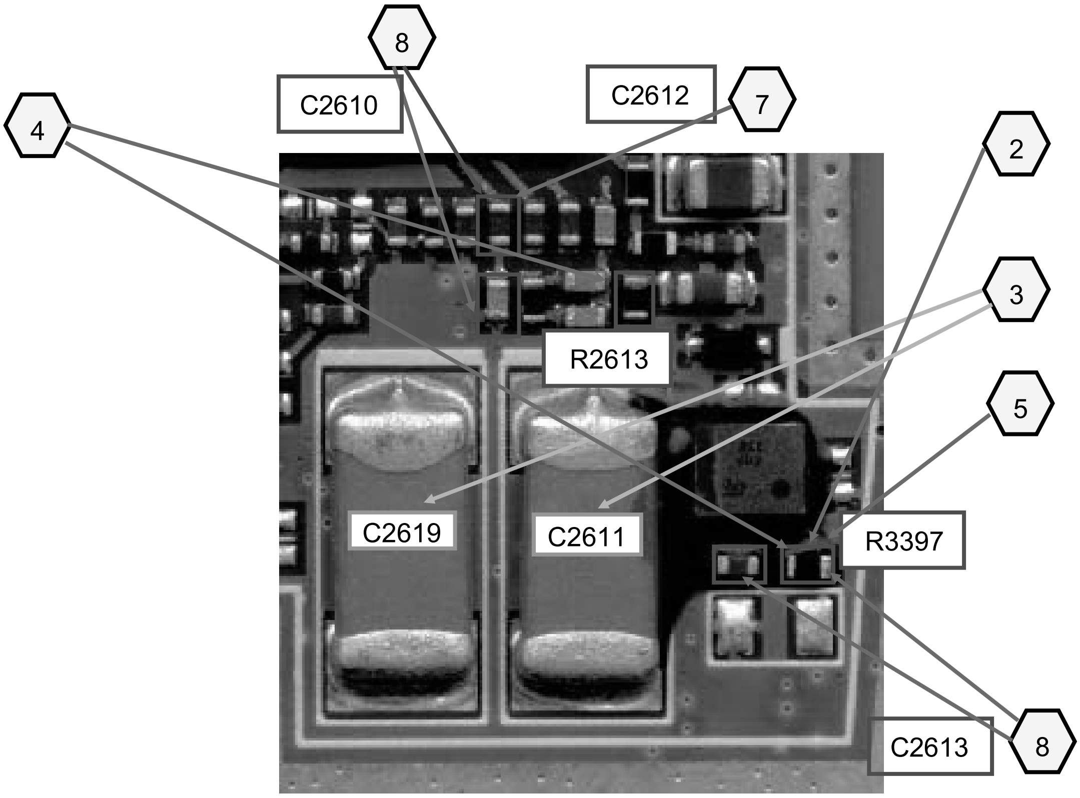
D. Headset Receiver (Voice call, Video Telephony, MP3)



E. Headset MIC(Voice call, Video Telephony)




1
R3381
6
X2602


8
C2610
C2612
7
4
2
3
R2613
5
C2619
C2611
R3397
C2613
8

4.13 Charger Trouble Shooting

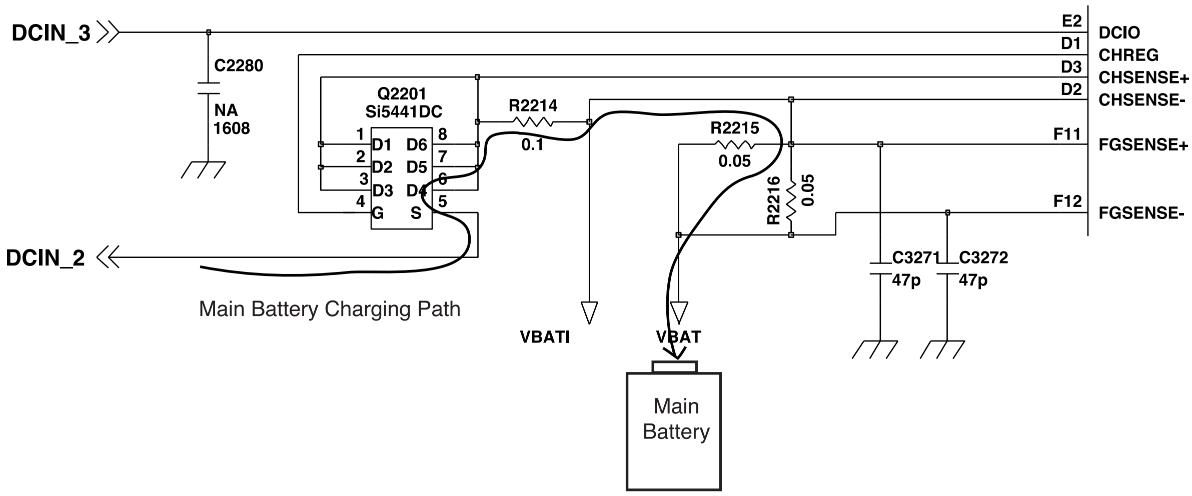


Figure. 13. Main Battery Charging Path

• Charging Procedure

- Connecting TA and Charger Detection
- Control the charging current by AB2000(Vincenne)
- Charging current flows into the battery

• Check Point

- Connection of TA
- Charging current path
- Battery

• Trouble shooting setup

- Connect TA and battery to the phone

• Trouble Shooting Procedure

- Check the charger connecter
- Check the Charging current Path
- Check the battery

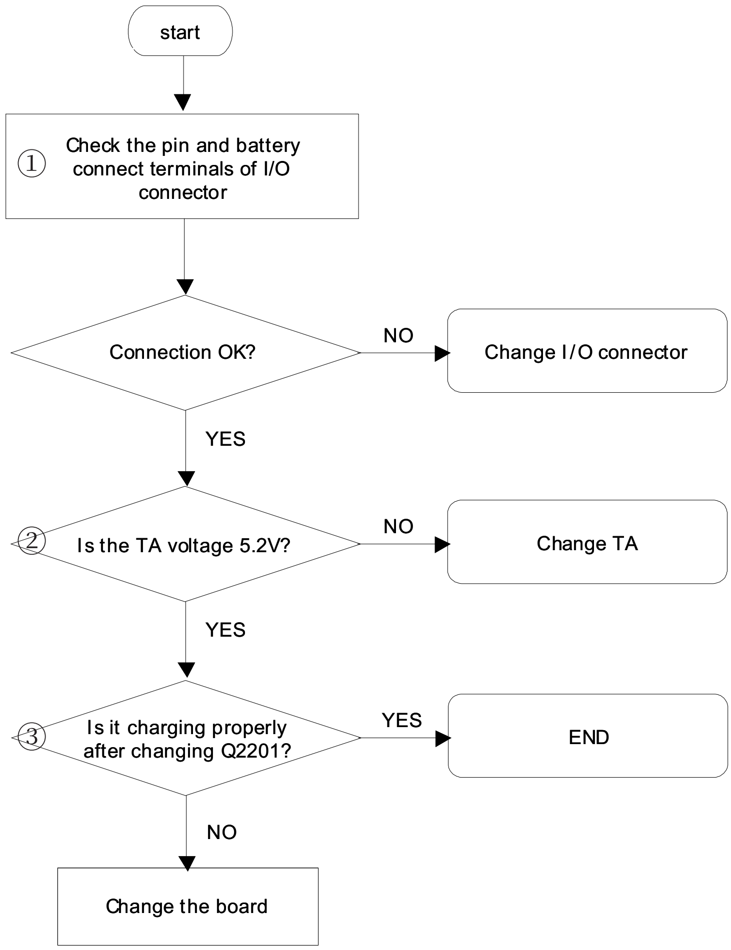


Figure. 14. Trouble Shooting - Charging

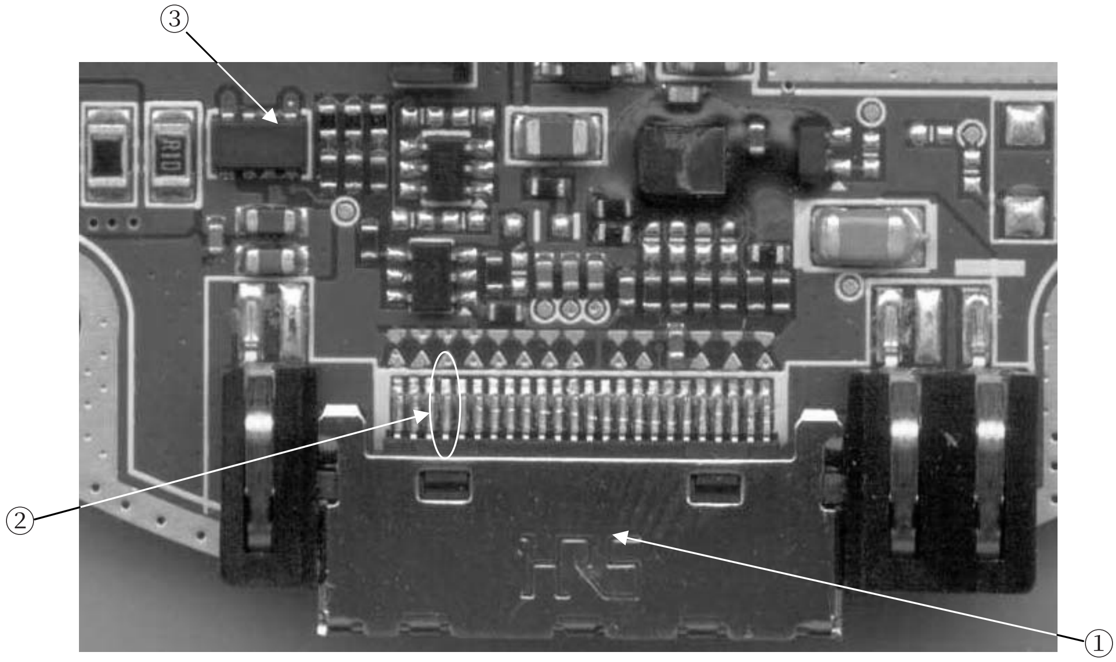


Figure. 15. Main Board - I/O connector and FET

4.14 RF Component

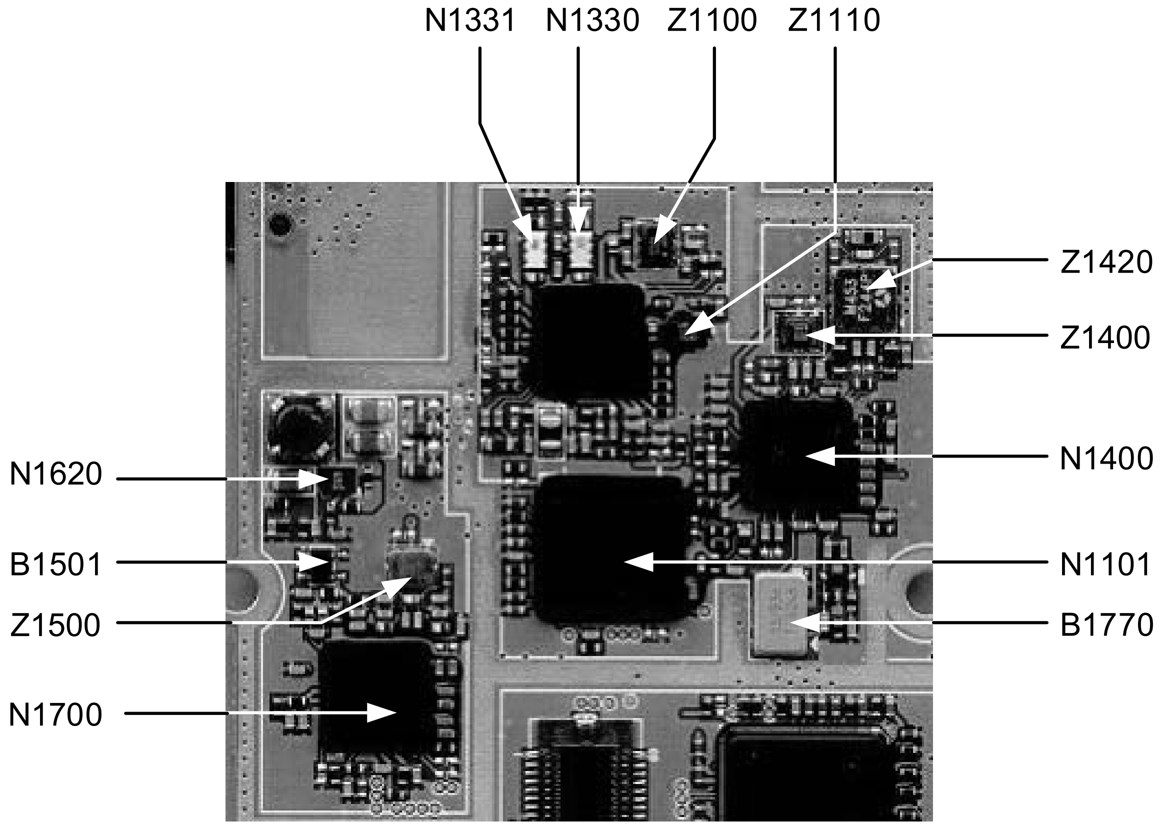


Figure 4-1. RF component (Top)

Reference	Description	Reference	Description
B1501	Temperature Sensor	N1700	WCDMA TX IC
B1770	Crystal	Z1100	DCS RX SAW
N1101	GSM ADC	Z1110	GSM RX SAW
N1330	GSM TX Balun	Z1400	WCDMA RX RF SAW
N1331	DCS TX Balun	Z1420	WCDMA RX IF SAW
N1400	WCDMA RX IC	Z1500	WCDMA TX RF SAW
N1620	DC/DC Convertor		

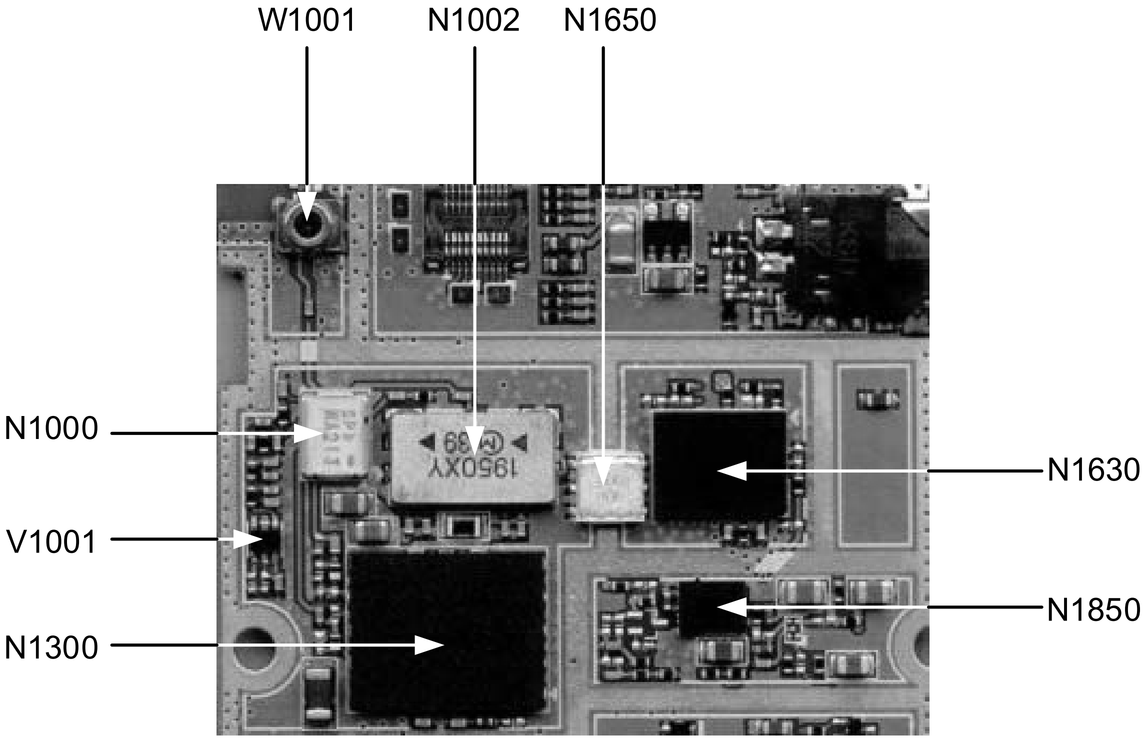
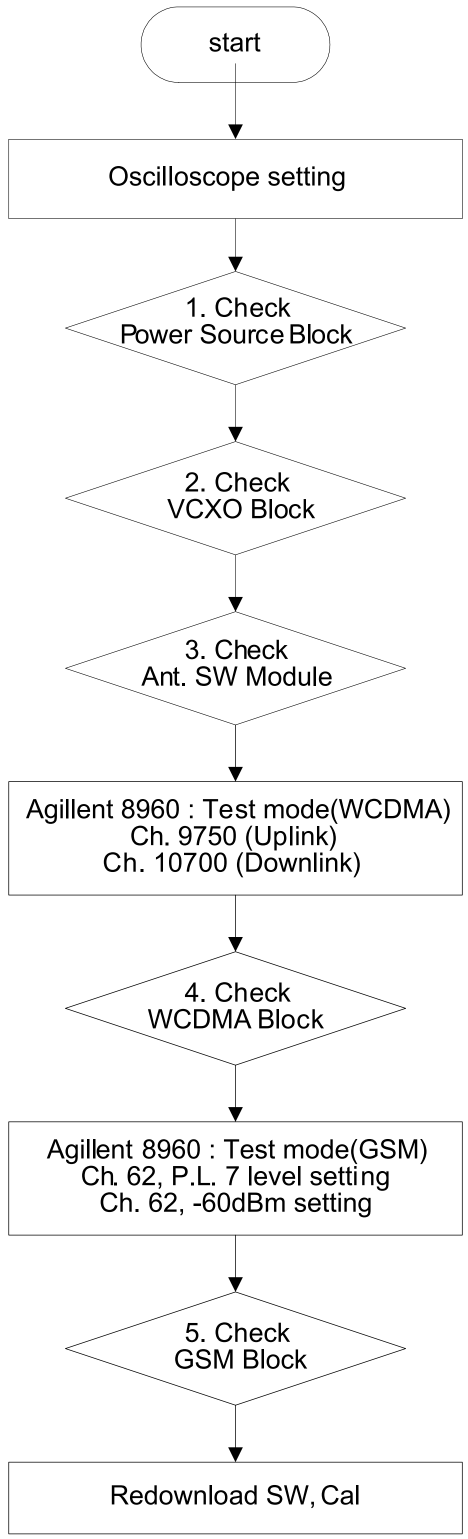


Figure 4-2. RF component (Bottom)

Reference	Description	Reference	Description
N1000	Ant. SW Module	N1650	Isolator
N1002	Duplexer	N1850	Regulator
N1300	GSM PAM	V1001	Transistor
N1630	WCDMA PAM	W1001	Test Connector

4.15 Procedure to check



4.16 Checking Common Power Source Block

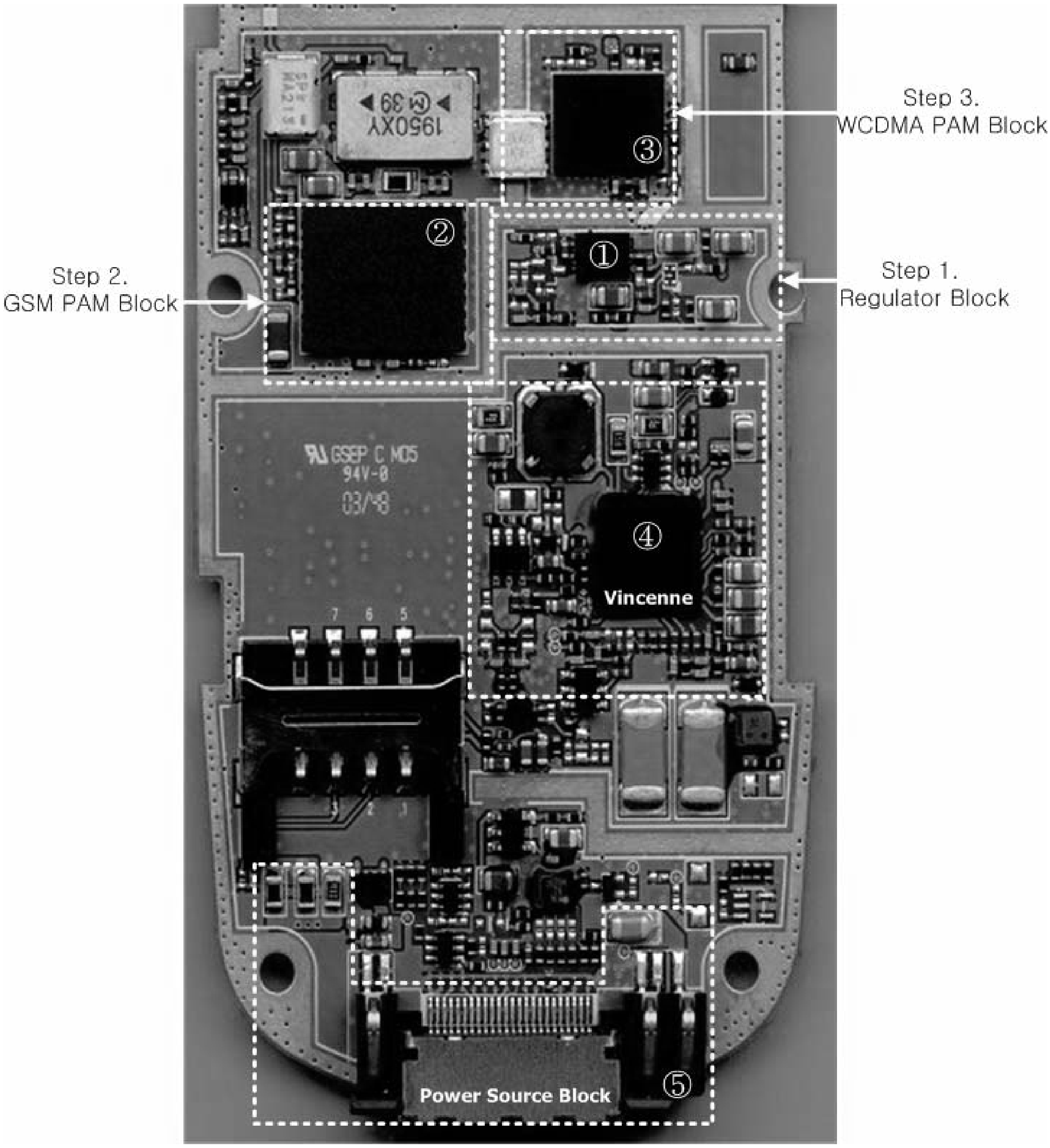


Figure 4-3. Common Source Block(Bottom)

4.16.1 Step 1

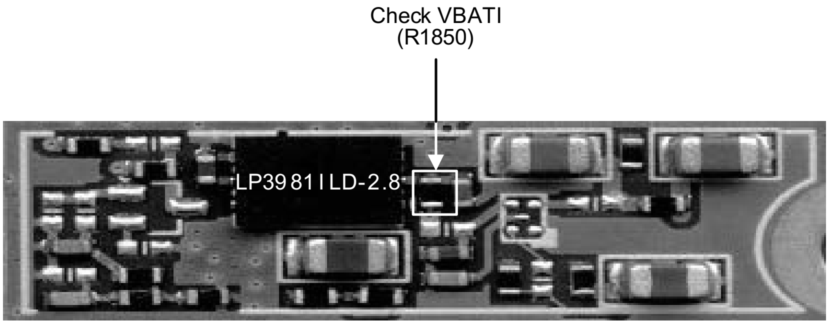


Figure 4-4. Regulator Block ①

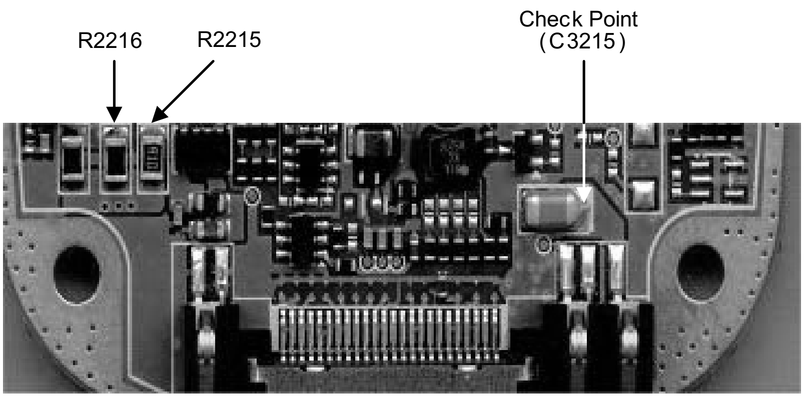
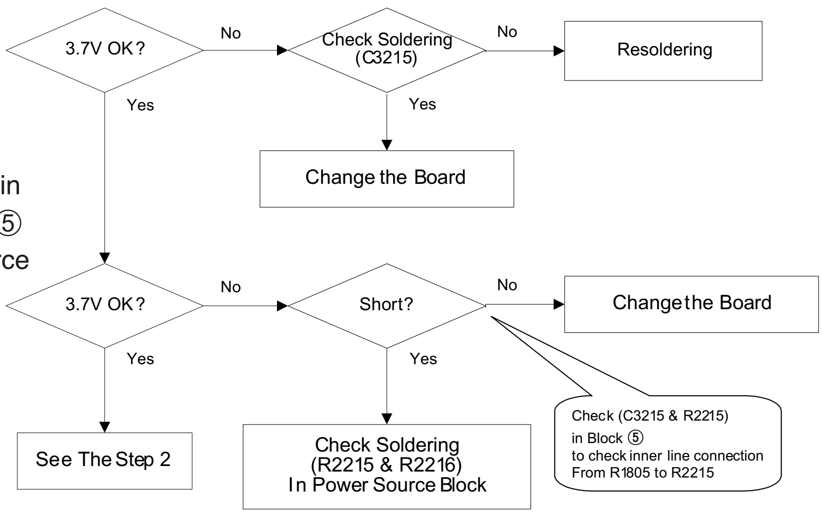


Figure 4-5. Power Source Block ⑤

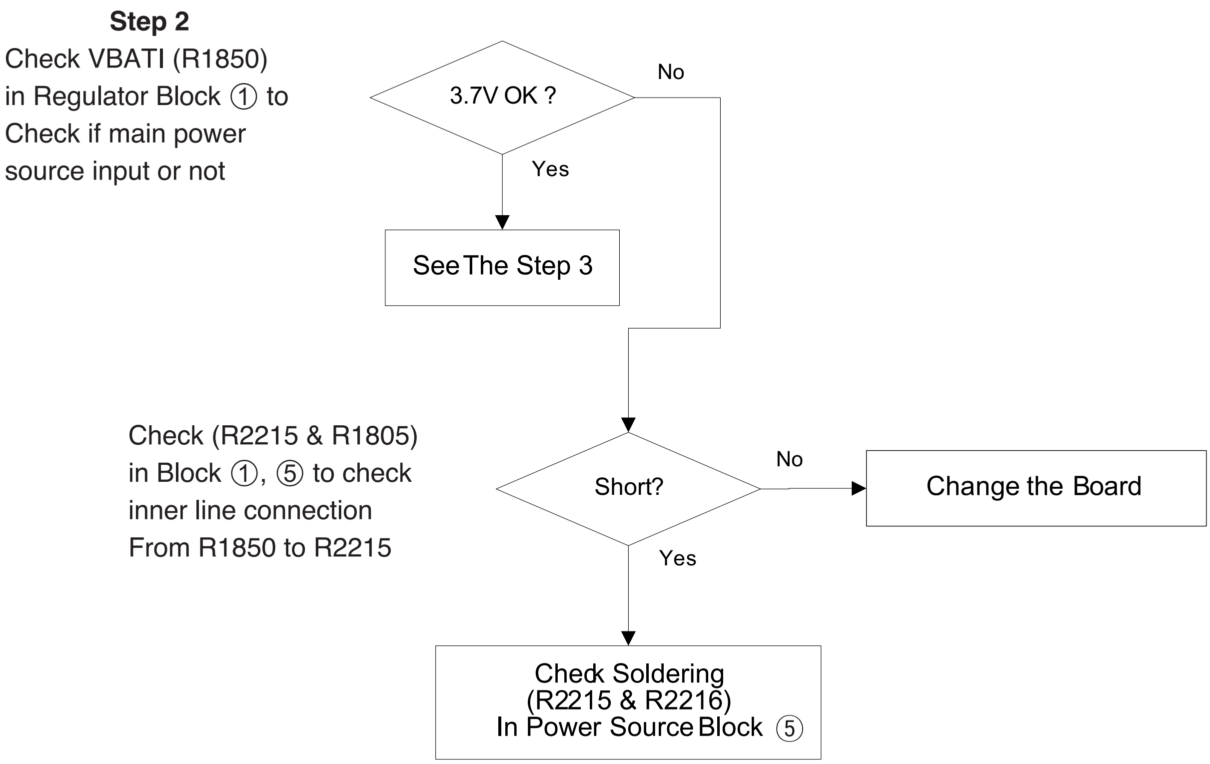
Step 1

Check Point (C3215) in Power Source Block ⑤ To Check Power source to Check if main power source input or not

Check Point (R2215) in Power Source Block ⑤ To Check Power source



4.16.2 Step 2


Step 2
Check VBATI (R1850)
in Regulator Block ① to
Check if main power
source input or not
3.7V OK ?
No
Yes
See The Step 3
Check (R2215 & R1805)
in Block ①, ⑤ to check
inner line connection
From R1850 to R2215
Short?
No
Change the Board
Yes
Check Soldering
(R2215 & R2216)
In Power Source Block ⑤

4.16.3 Step 3

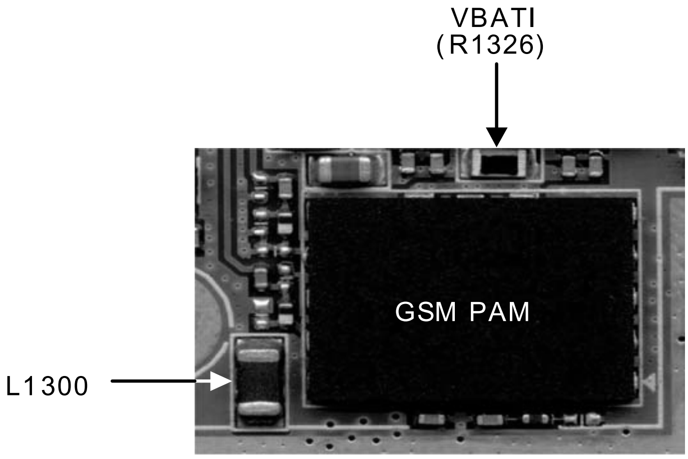


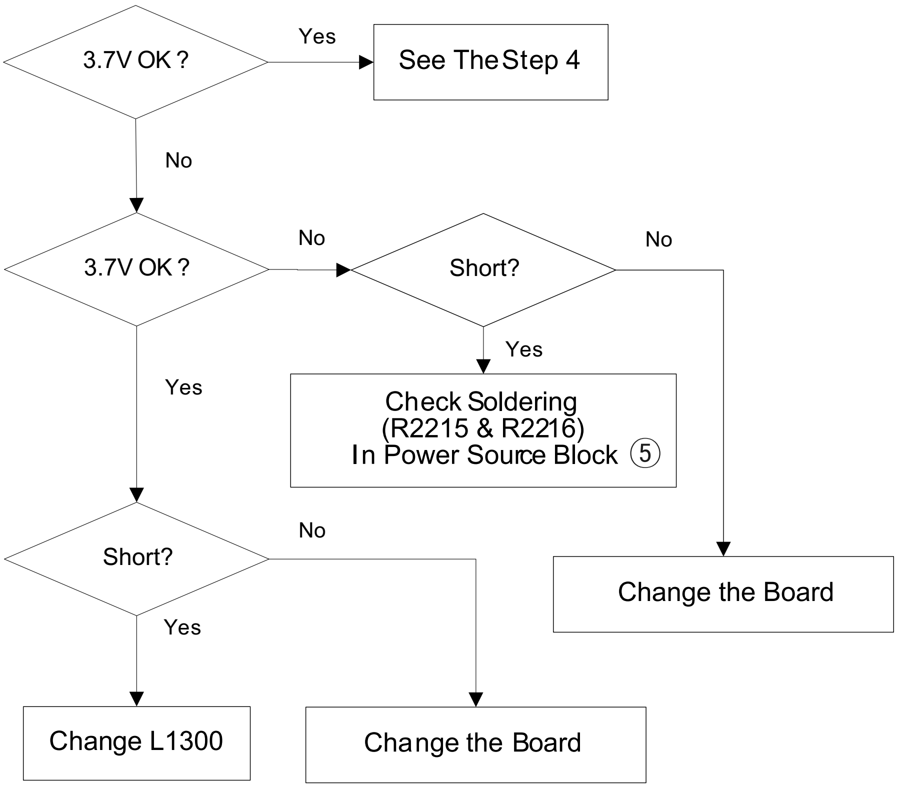
Figure 4-6. GSM PAM Block ②

Step 3
Check VBATI (R1326) in GSM PAM Block ② to Check if main power source input or not

Check L1300 to check if power source input or not

Check L1300 & R1326 inner Line connection

Check (L1300 & R2215) in Block ②, ⑤ to check inner line connection From L1300 to R2215



4.16.4 Step 4

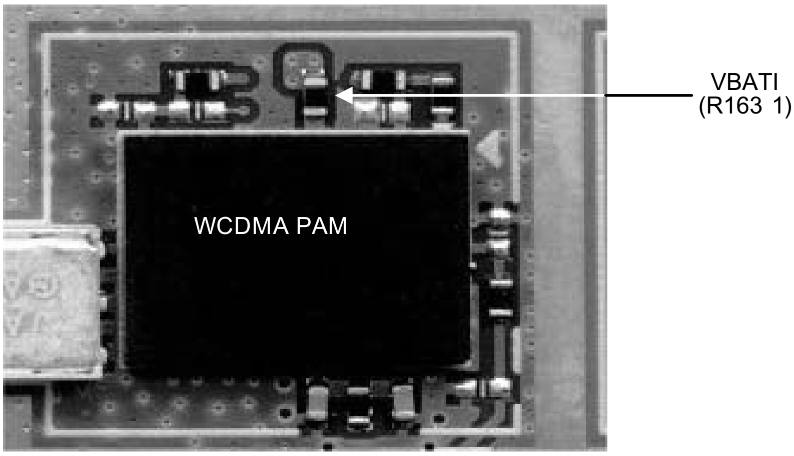


Figure 4-7. WCDMA PAM Block ③

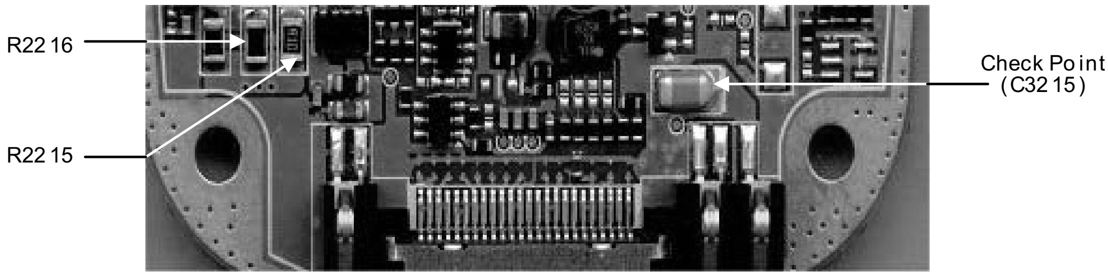
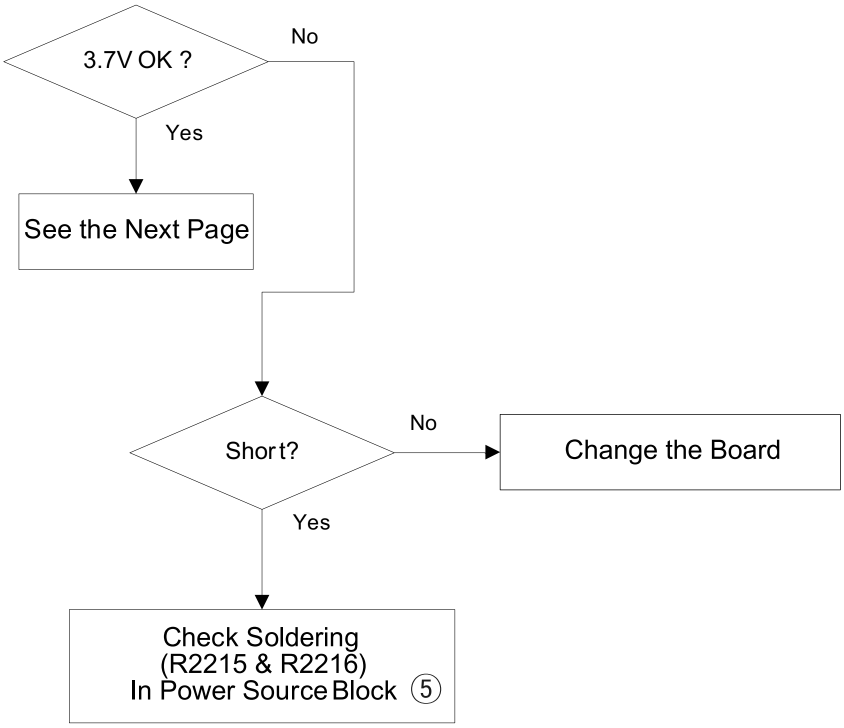


Figure 4-7-1. PAM-Power Source

Step 4
Check R1631 in WCDMA PAM block



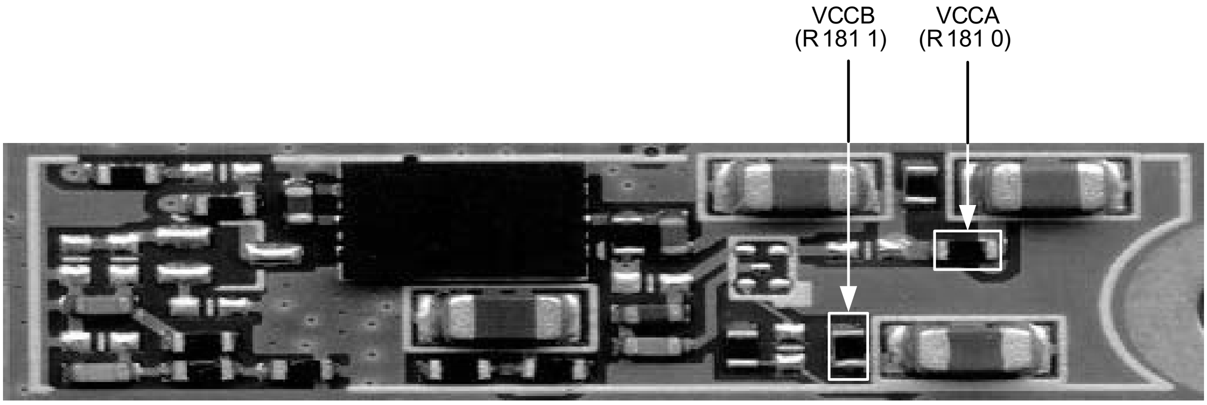
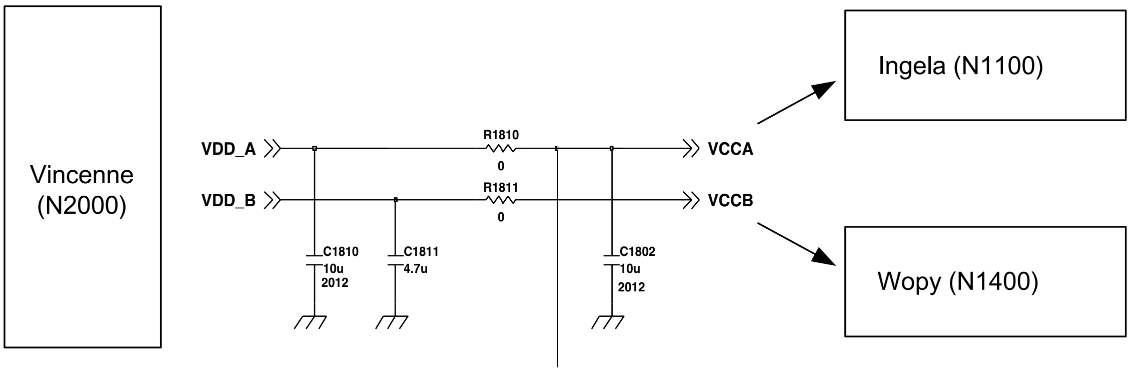
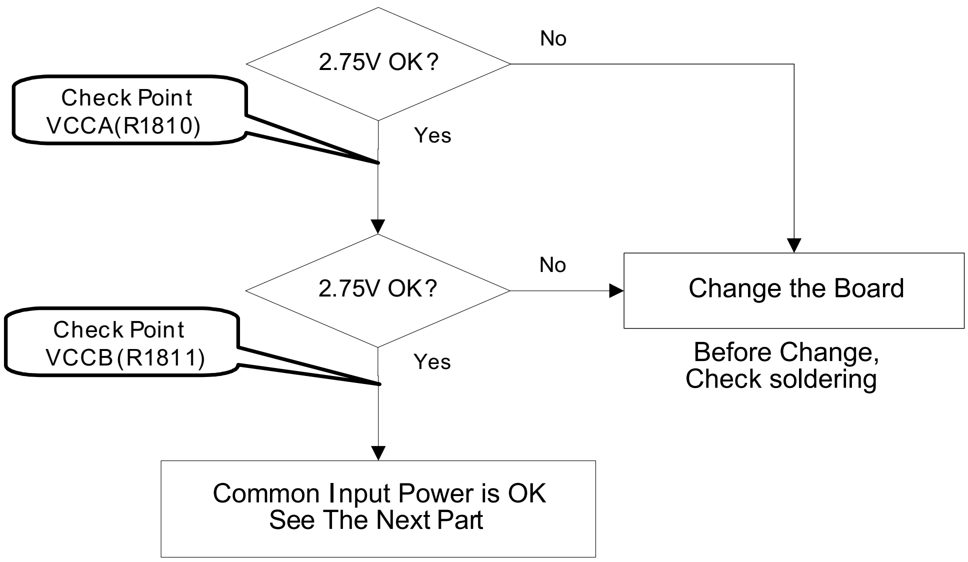


Figure 4-8. Power for Radio ASIC





4.16.5 Checking Regular Part

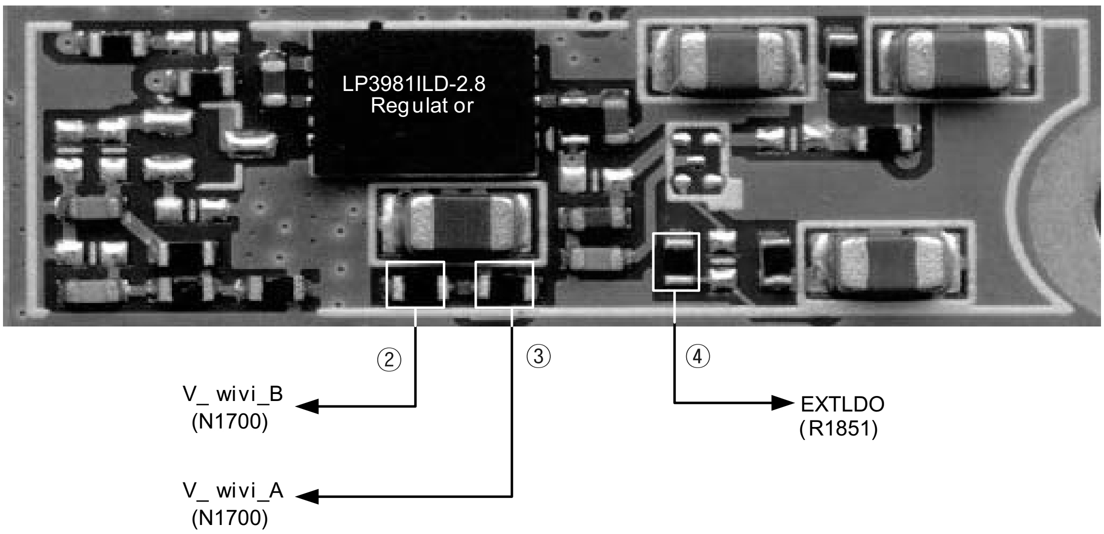


Figure 4-9. Regulator Block

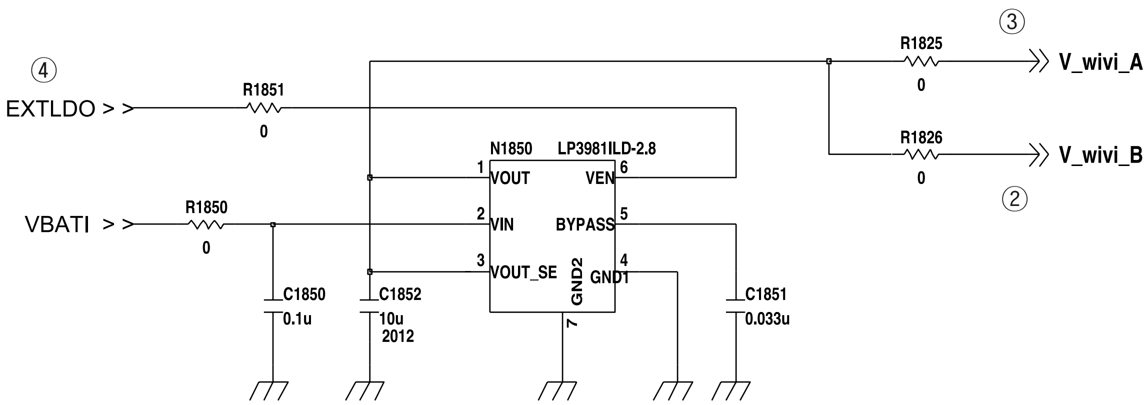
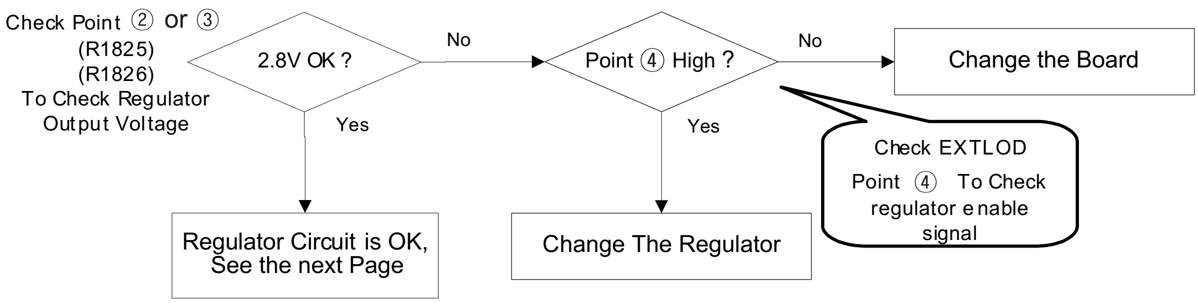


Figure 4-10. Regular Circuit Diagram



4.17 Checking VCXO Block

The reference frequency (13MHz) from B1770 (Crystal) is used WCDMA TX part, GSM part and BB part. Therefore you have to check below 4 point.

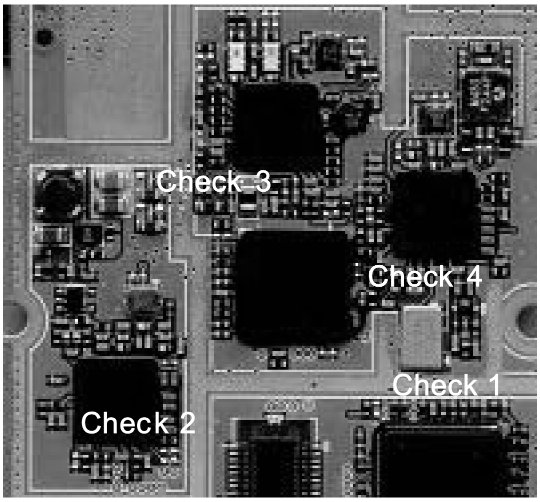


Figure 4-12. Top Place

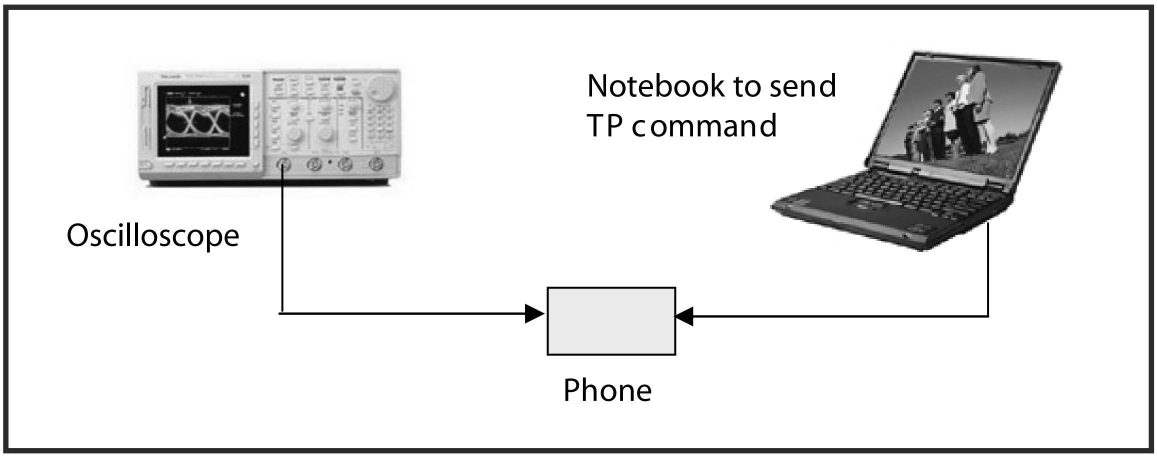


Figure 4-13. Connection for Checking VCXO Block

Check 1. Crystal part
If you already check this crystal part, you can skip check 1.

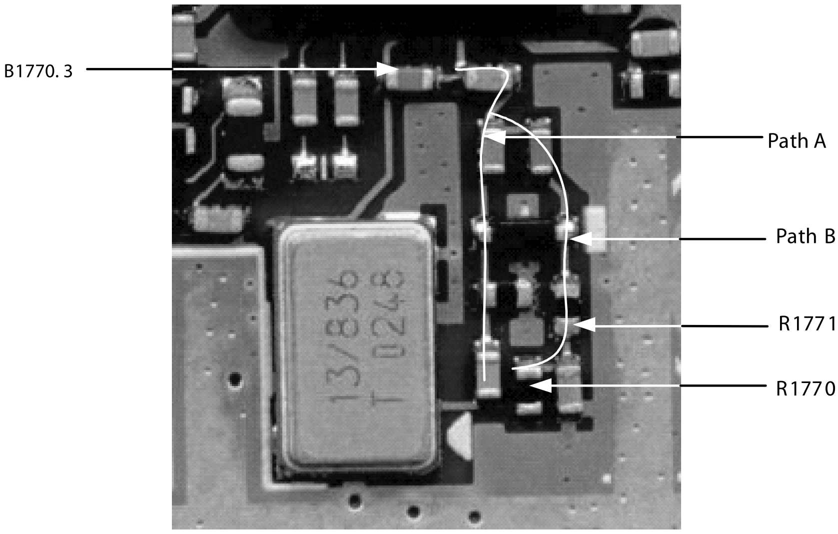


Figure 4-14. Test Point (Crystal Part)

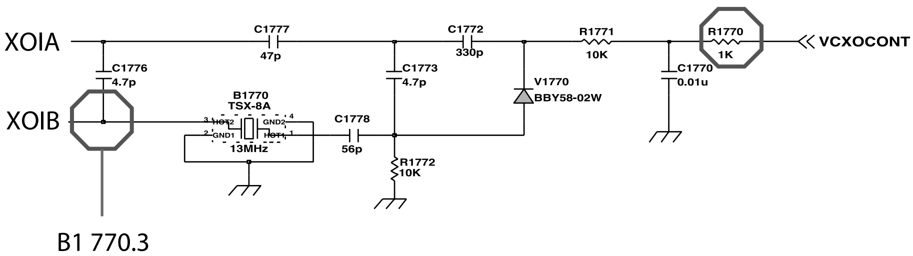


Figure 4-15. Schematic of the Crystal Part

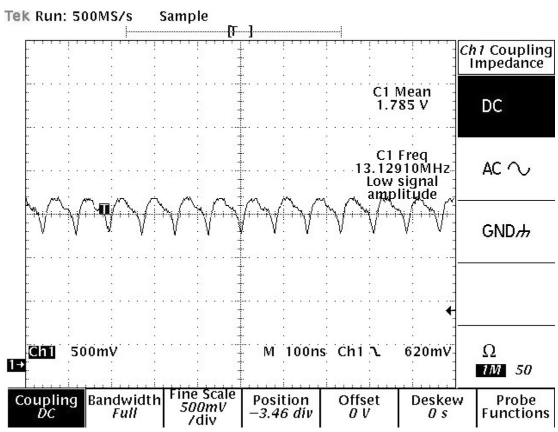
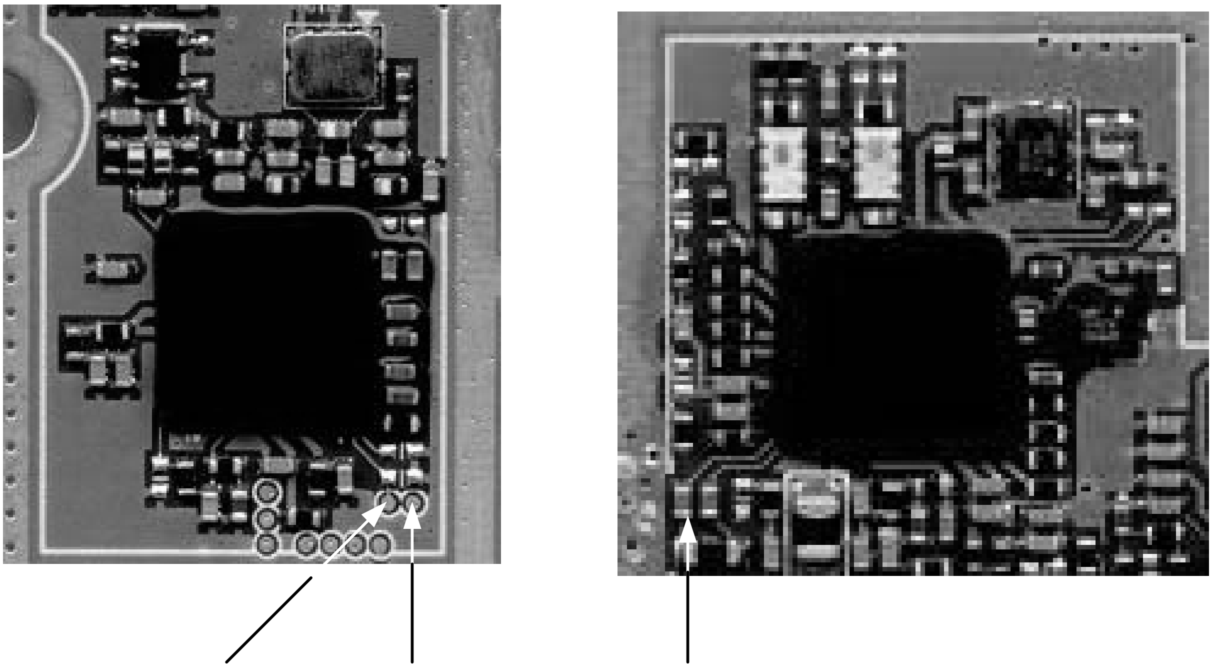


Figure 4-16. 13MHz at B1770.3

Check 2,3 13MHz at WCDMA TX part and GSM part



N1770.B1 N1770.C1 N1100.K9

Figure 4-17. Test point (13MHz at TX Part)

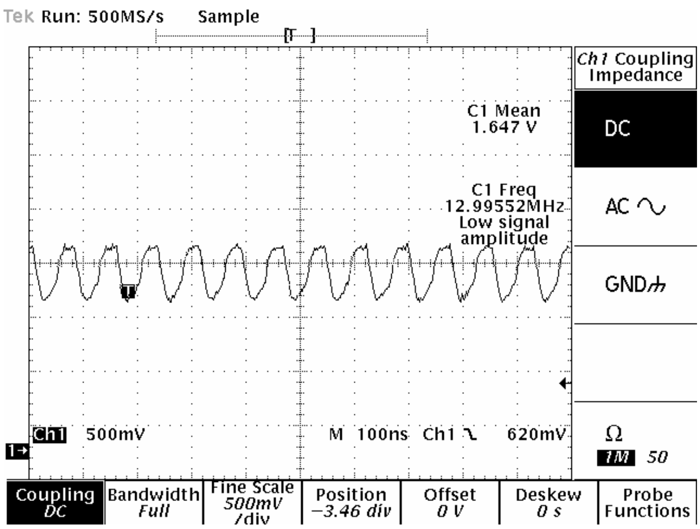


Figure 4-18. 13MHz at N1770.B1 and N1100.K9

Check 4. 13MHz at BB part

N1400.C1

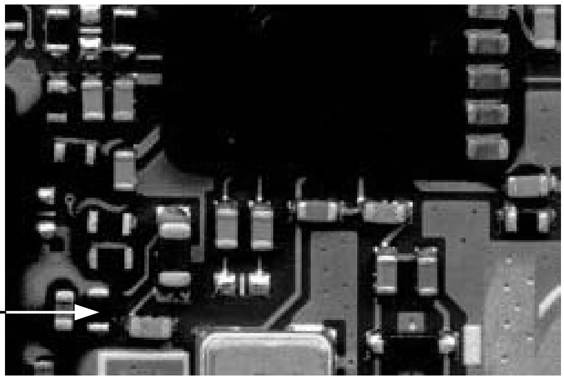


Figure 4-19. Test Point (13MHz at BB Part)

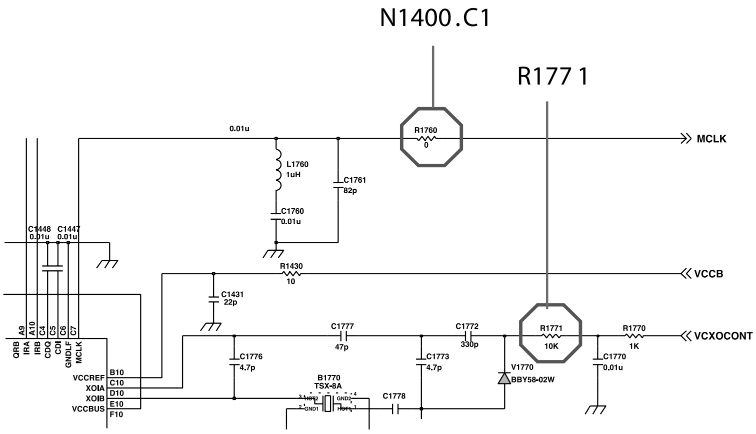


Figure 4-20. Schematic (13MHz at BB Part)

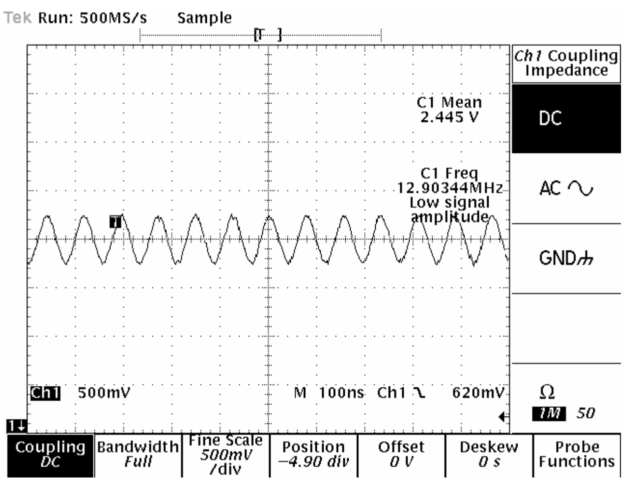
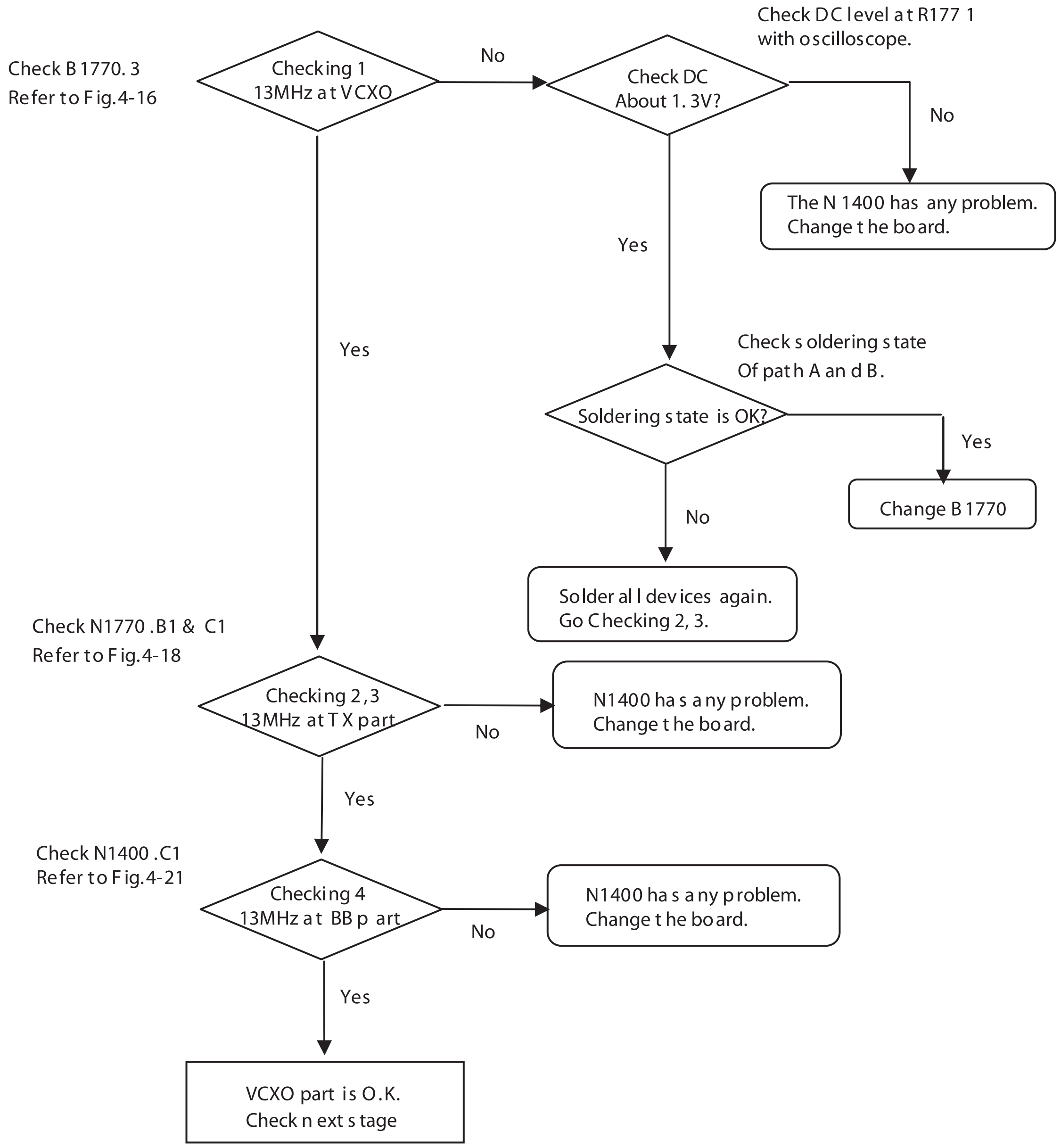


Figure 4-21. 13MHz at N1400.C1


Check B1770. 3
Refer to Fig.4-16
Checking 1
13MHz at VCXO
No
Check DC level at R1771
with oscilloscope.
Check DC
About 1. 3V?
No
The N1400 has any problem.
Change the board.
Yes
Yes
Check soldering state
Of path A and B.
Soldering state is OK?
Yes
Change B1770
No
Solder all devices again.
Go Checking 2, 3.
Check N1770 .B1 & C1
Refer to Fig.4-18
Checking 2,3
13MHz at TX part
No
N1400 has any problem.
Change the board.
Yes
Check N1400 .C1
Refer to Fig.4-21
Checking 4
13MHz at BB part
No
N1400 has any problem.
Change the board.
Yes
VCXO part is O.K.
Check next stage

4.18 Checking Ant. SW Module Block

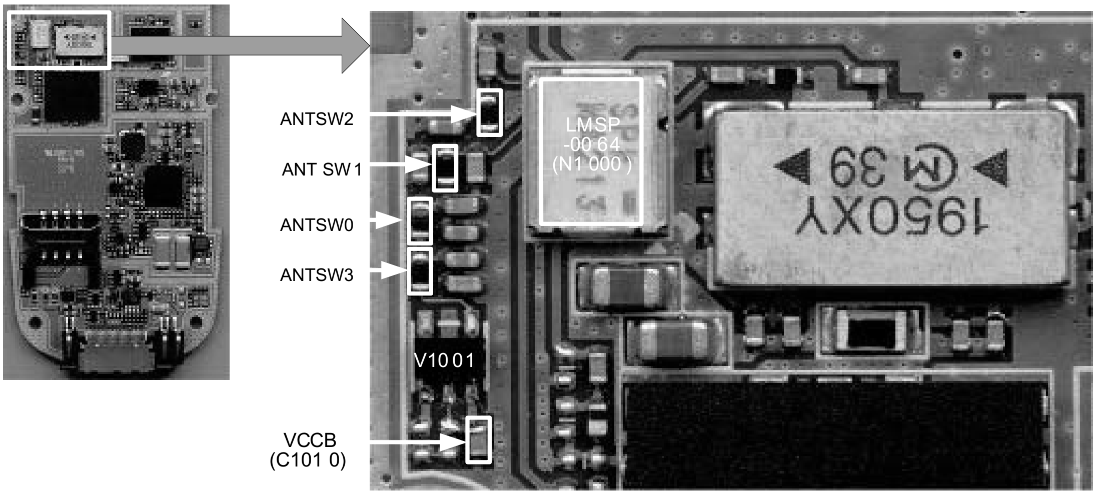
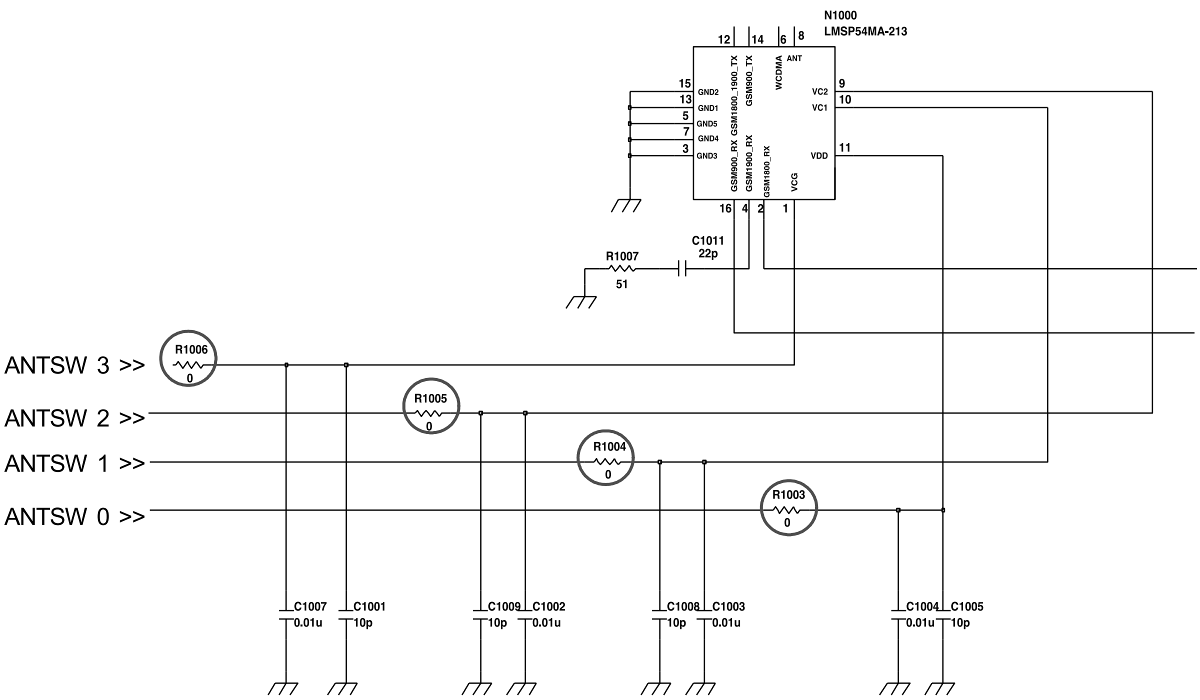
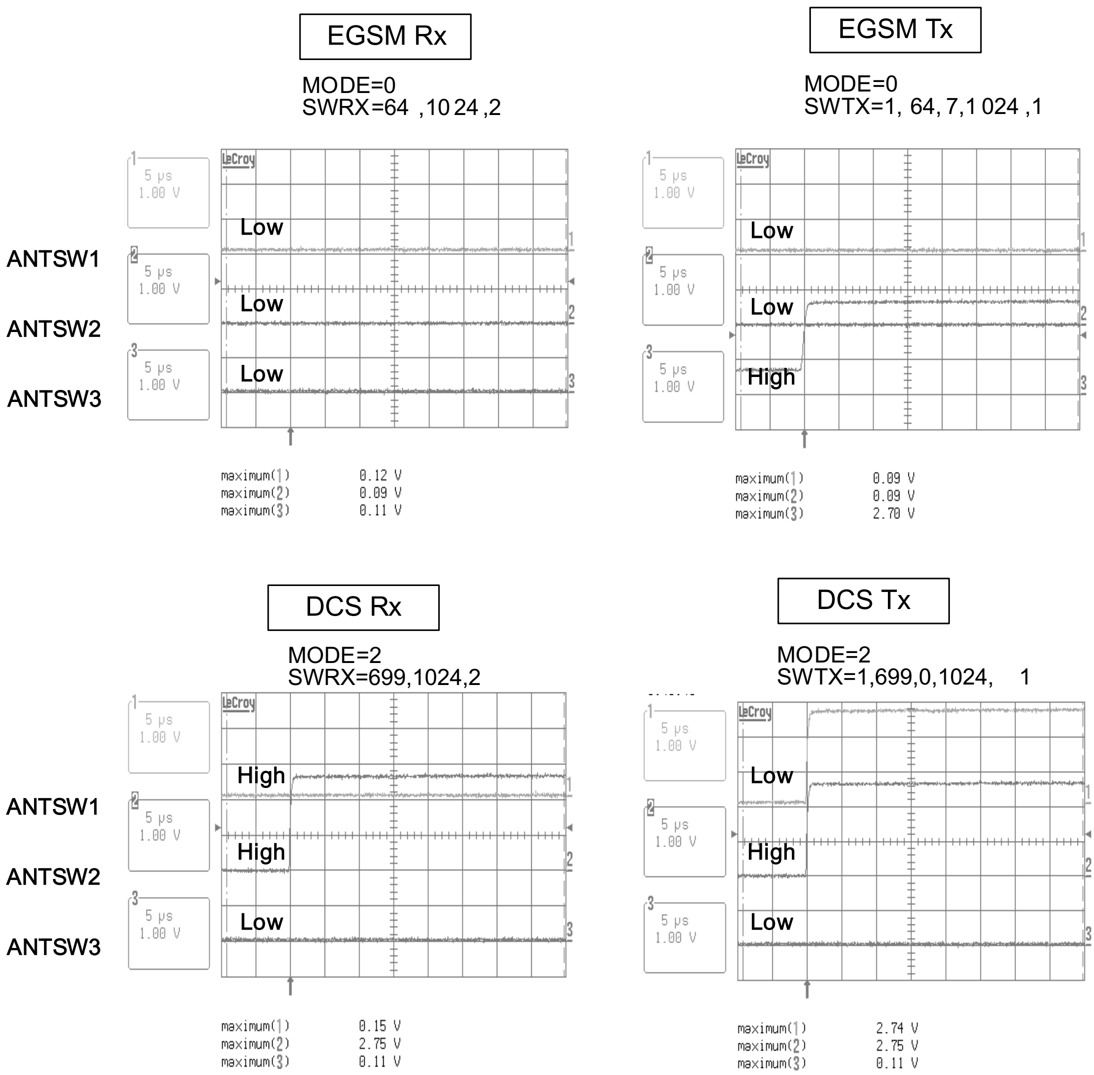


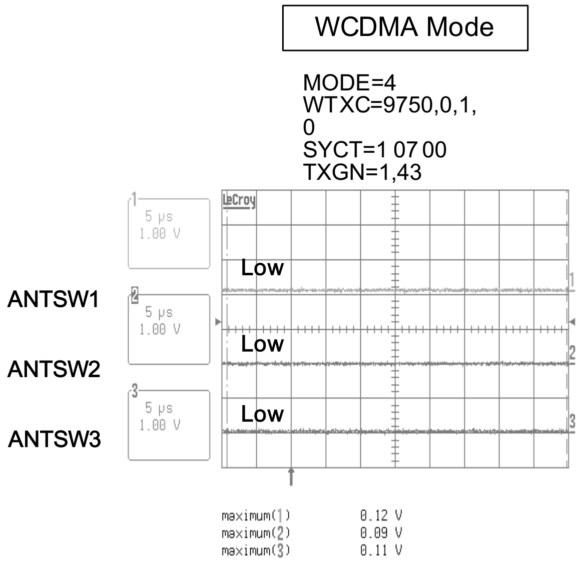
Figure 4-20. Antenna Switch Block(Bottom)



4.19 Checking Antenna Switch Block input logic

4.19.1 Mode Logic by TP Command



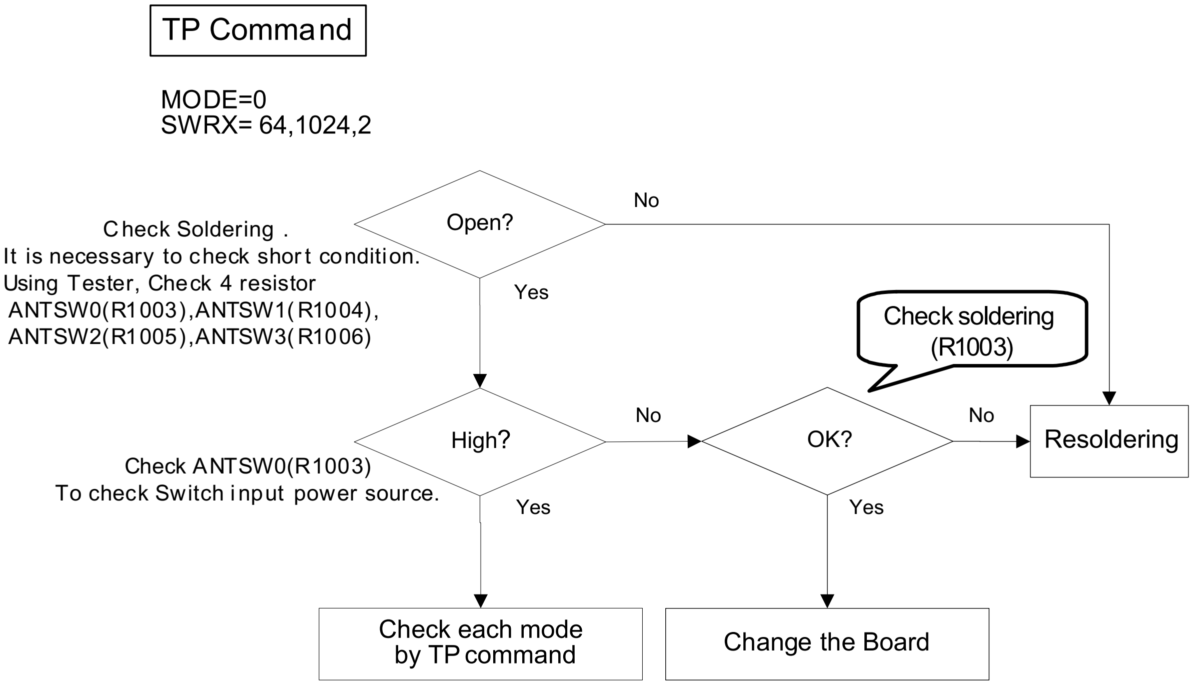


Band	ANTSW0	ANTSW1	ANTSW2	ANTSW3
EGSM Tx	H	L	L	H
EGSM Rx	H	L	L	L
DCS Tx	H	H	H	L
DCS Rx	H	L	H	L
WCDMA	H	L	L	L

Table 4-1. Antenna Switch Module Logic

4.19.2 Checking Switch Block power source

❊ Before Checking this part, must check common power source (through Vincenne) part



A. EGSM Rx Mode

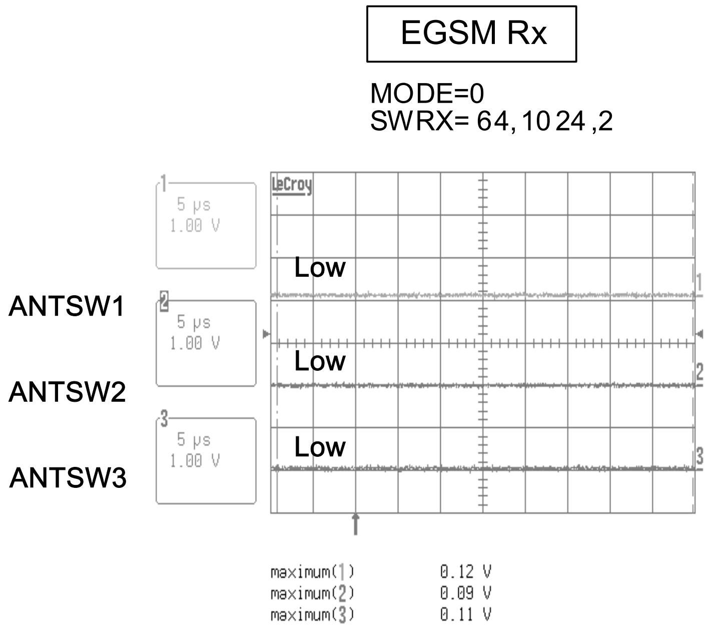
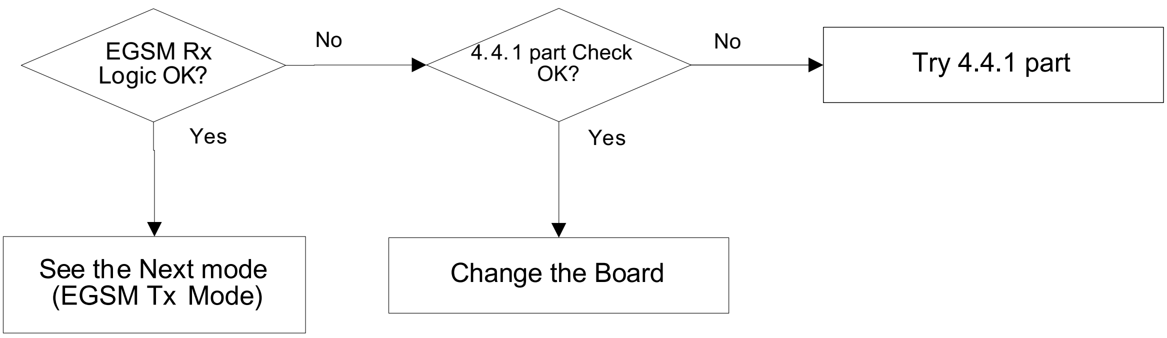


Figure 4-21. EGSM Rx Mode



B. EGSM Tx Mode

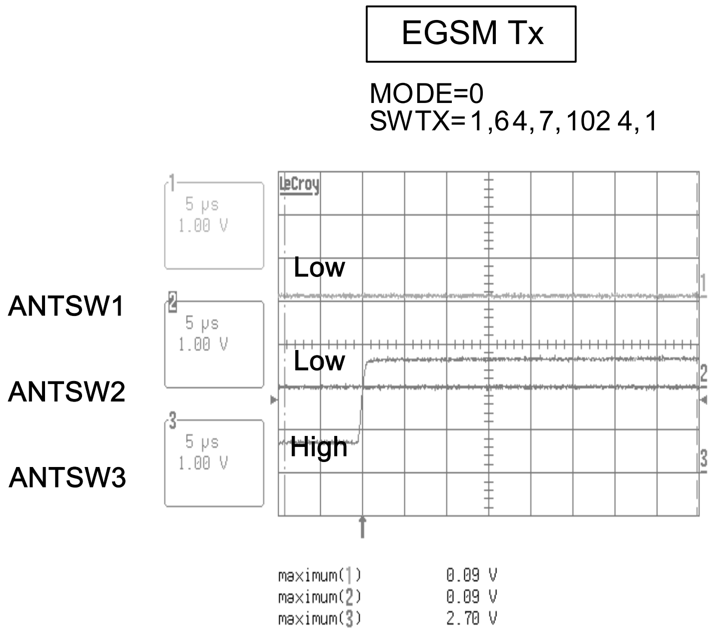
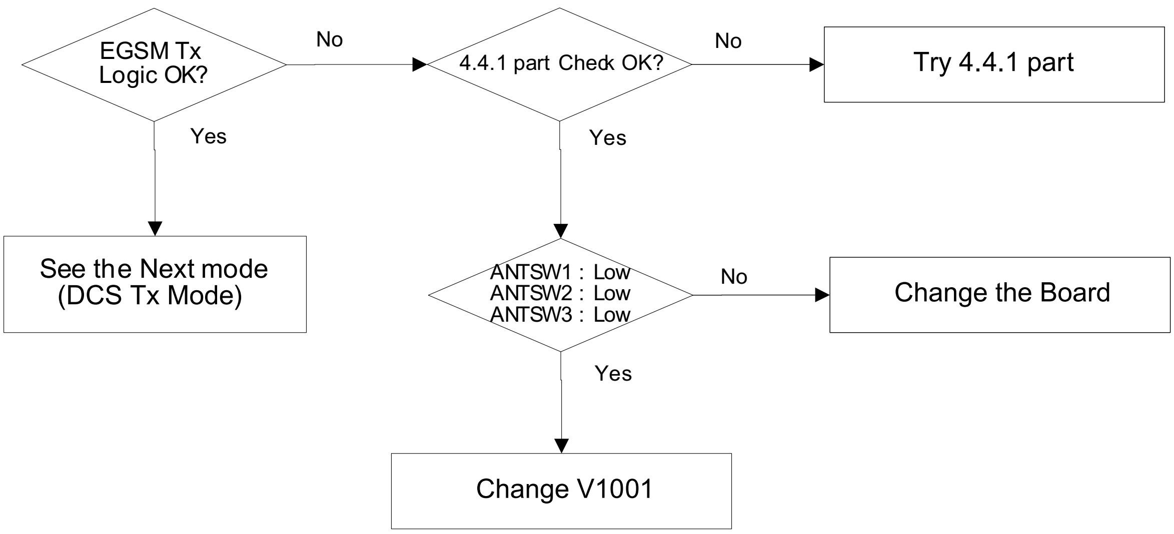


Figure 4-22. EGSM Tx Mode



C. DCS Rx Mode

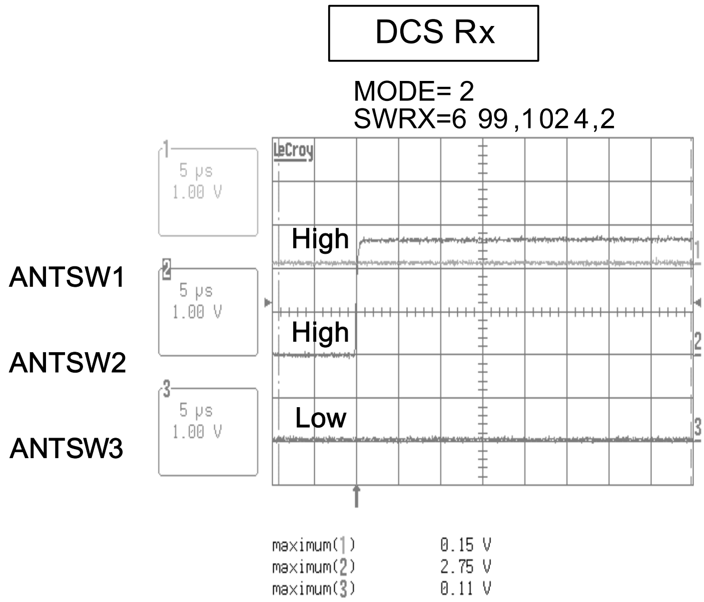
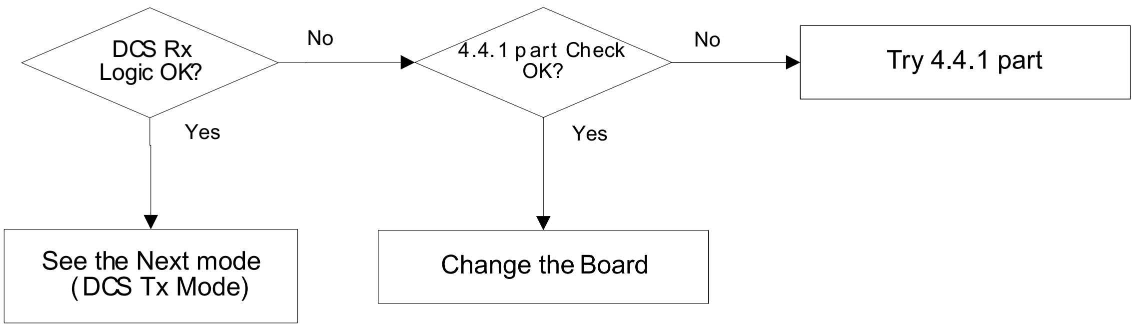


Figure 4-23. DCS Rx Mode



D. DCS Tx Mode

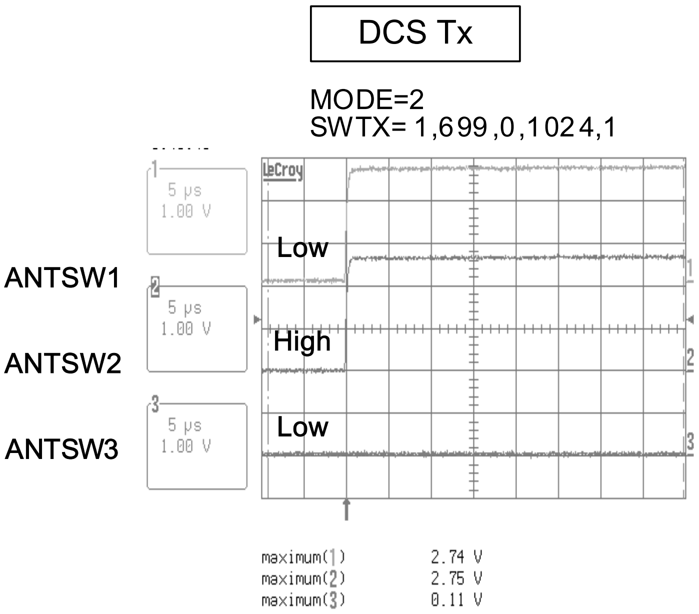
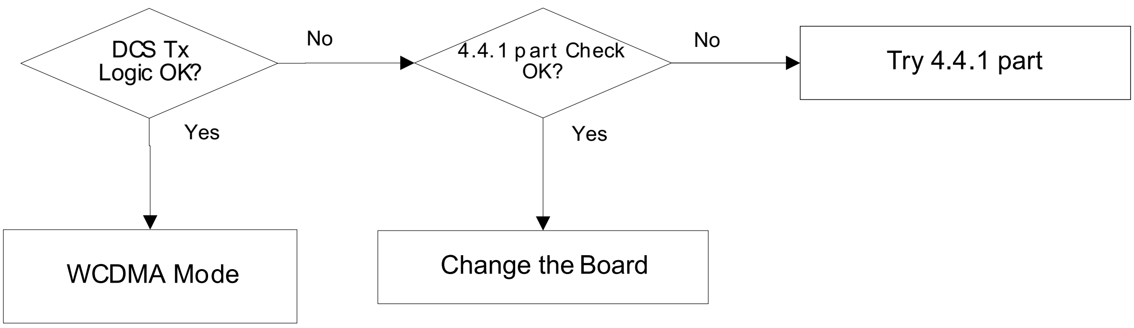


Figure 4-24. DCS Tx Mode



E. WCDMA Mode

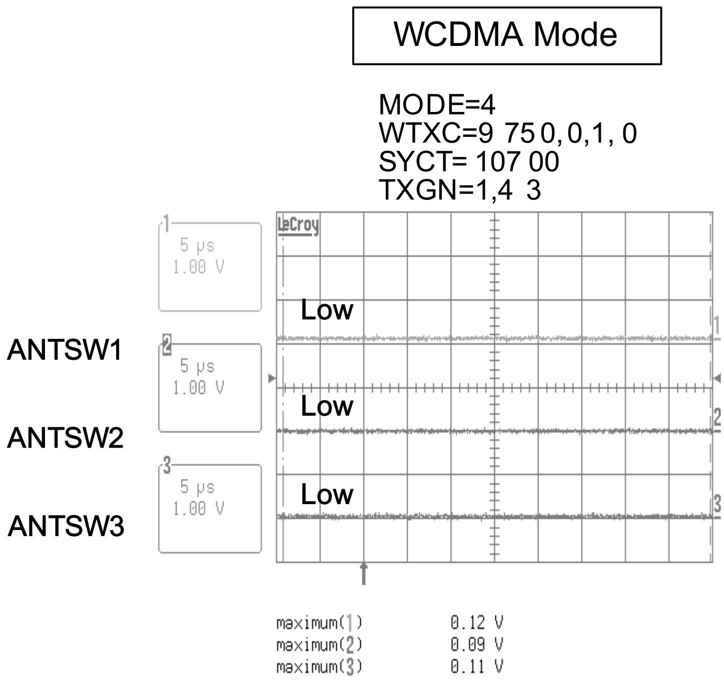
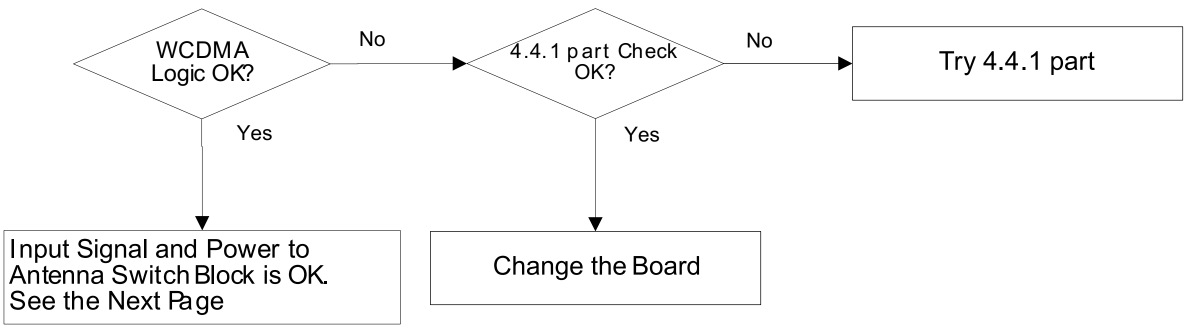


Figure 4-25. WCDMA Mode



4.20 Checking WCDMA Block

start

↓

1. Check VCXO Block

↓

2. Check Ant. SW Module

↓

3. Check Control Signal

↓

4. Check RF Tx Level

↓

5. Check PAM Block

↓

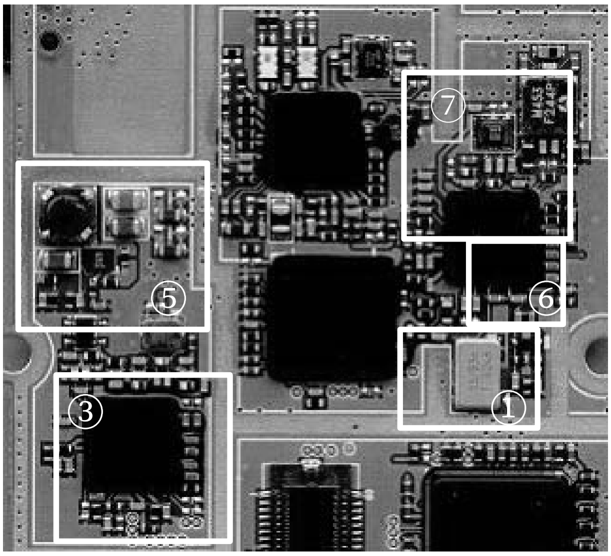
6. Check Rx IQ

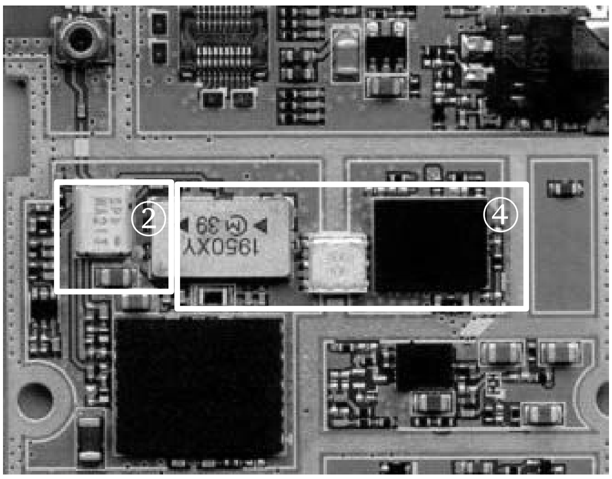
↓

7. Check RF Rx Level

↓

Redownload SW, Cal





4.20.1 Checking

Refer to 4.4

4.20.2 Checking Ant. SW module

Refer to 4.5

4.20.3 Checking Control Signal

First of all, you have to check control signal. (data, clk, strobe)

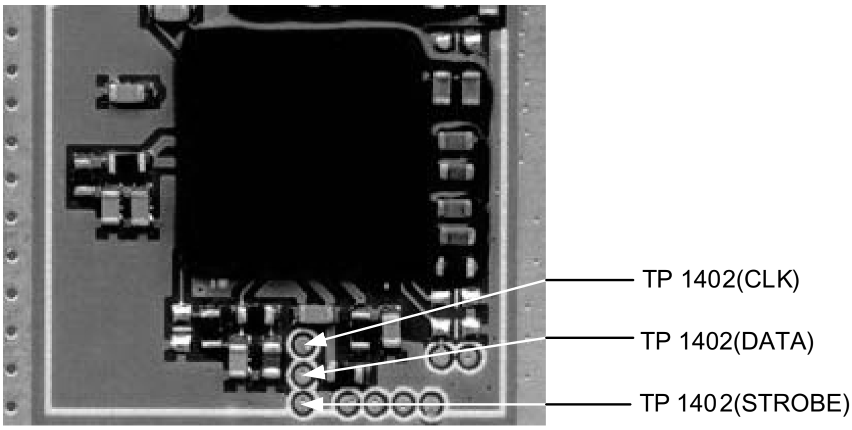


Figure 4-28. Test Point (Control Signal)

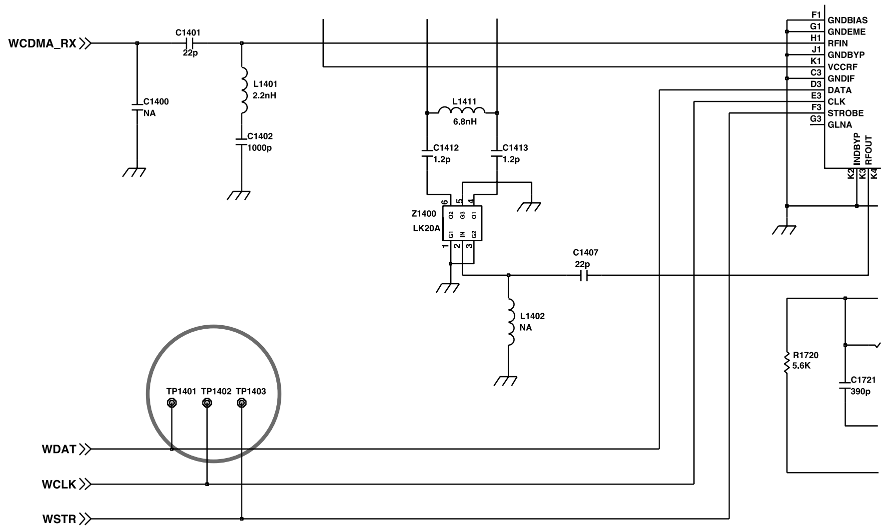


Figure 4-29. Schematic (Control Signal)

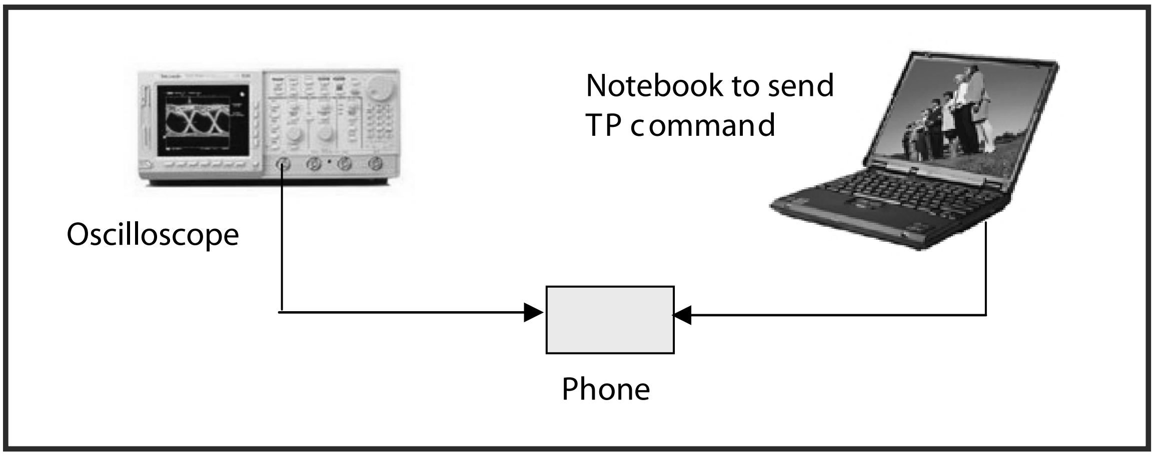


Figure 4-30. Connection for Checking Control Signal

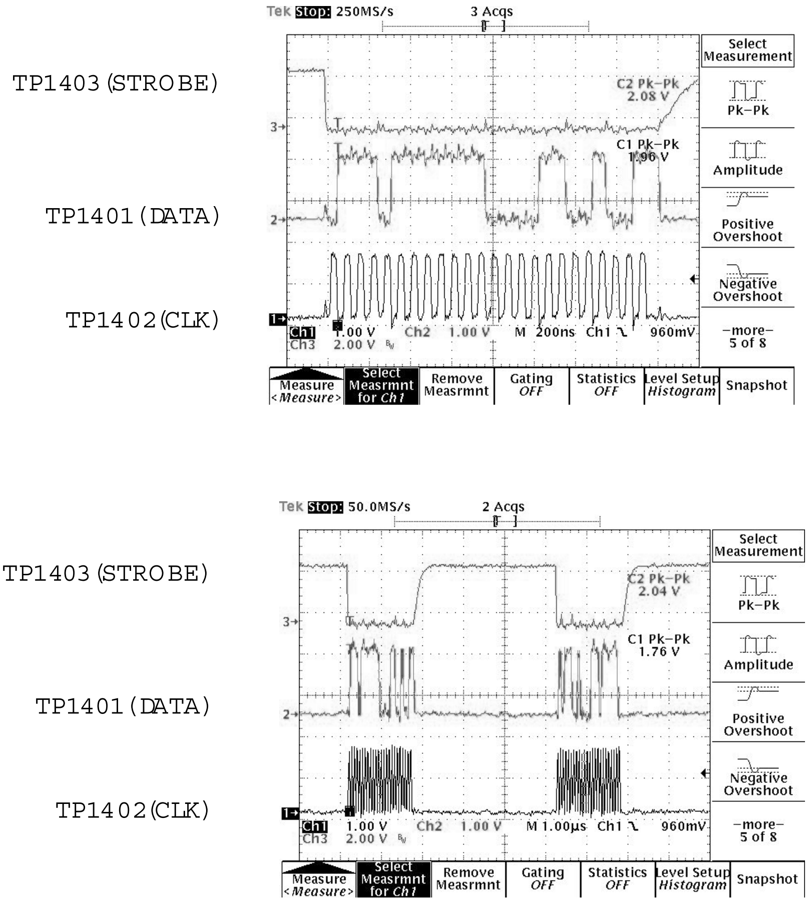
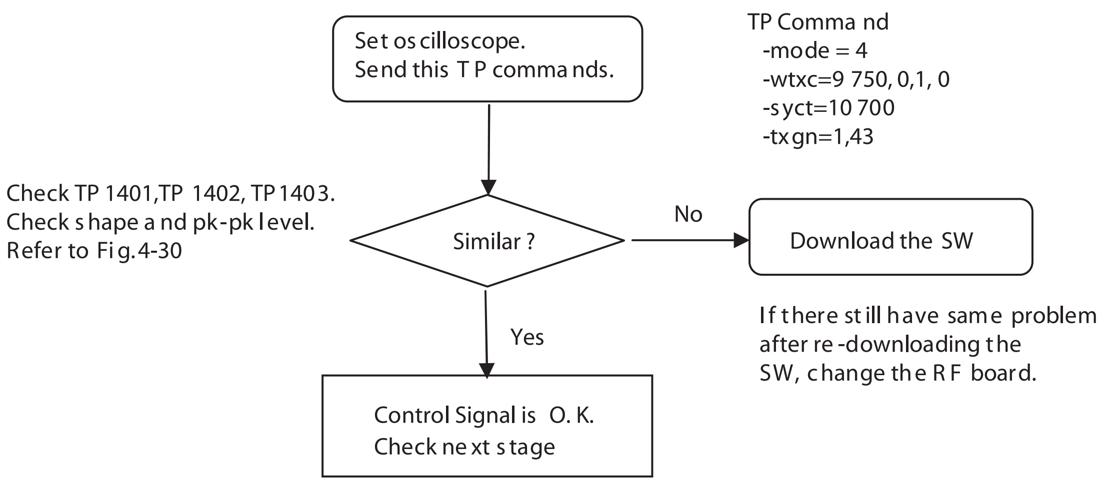


Figure 4-30. Control signal



4.20.4 Checking RF TX Level

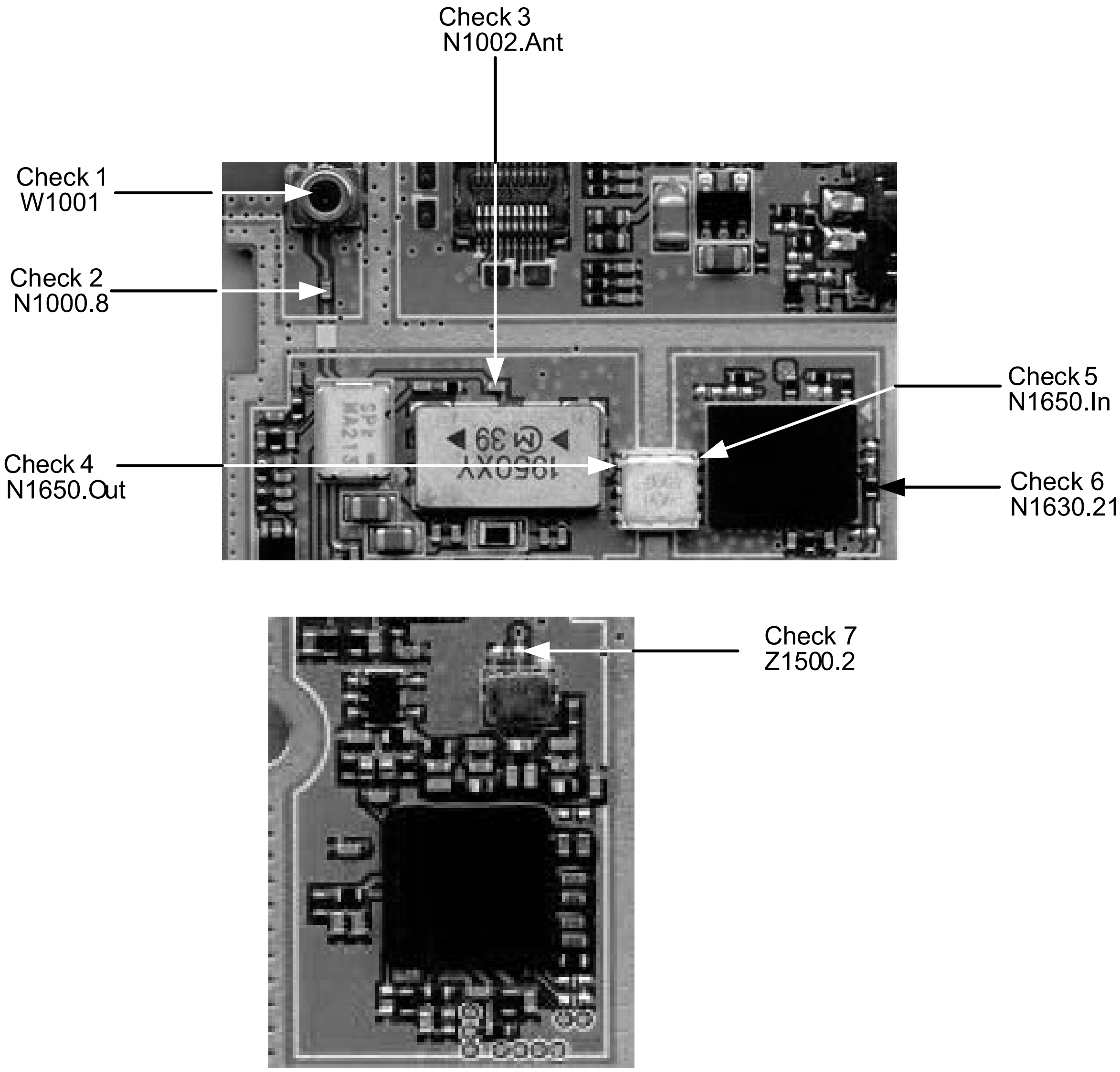


Figure 4-31. Test Point (RF TX Level)

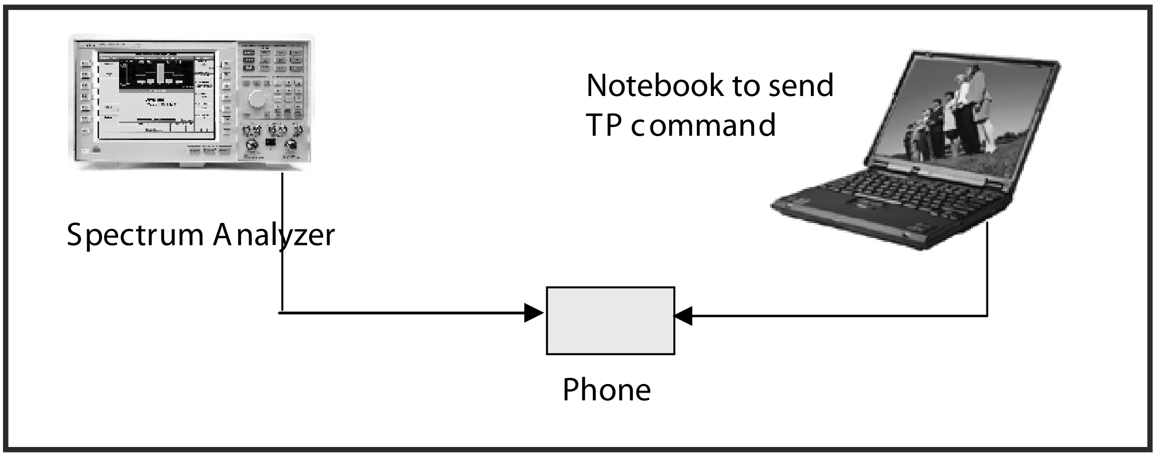
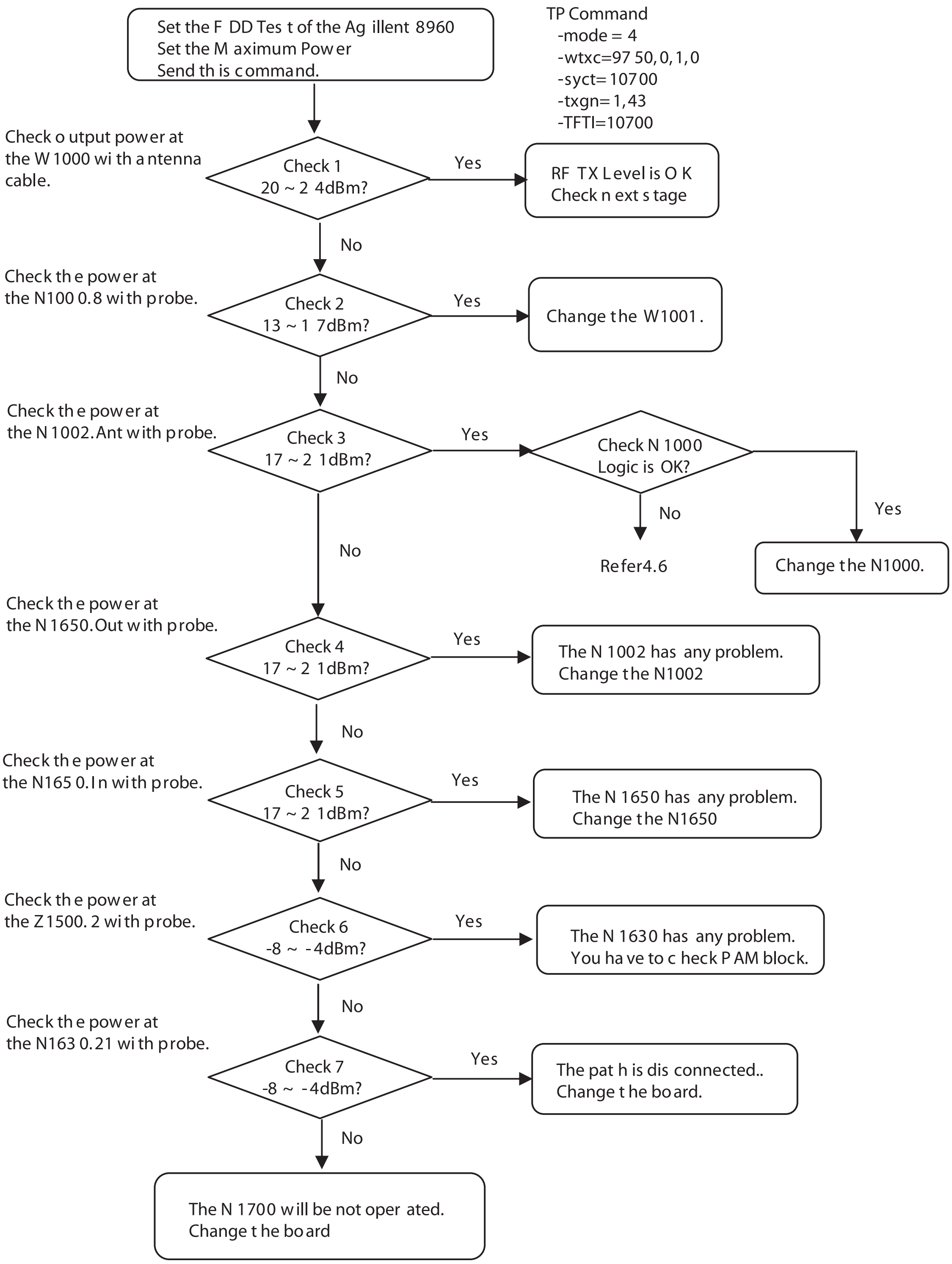
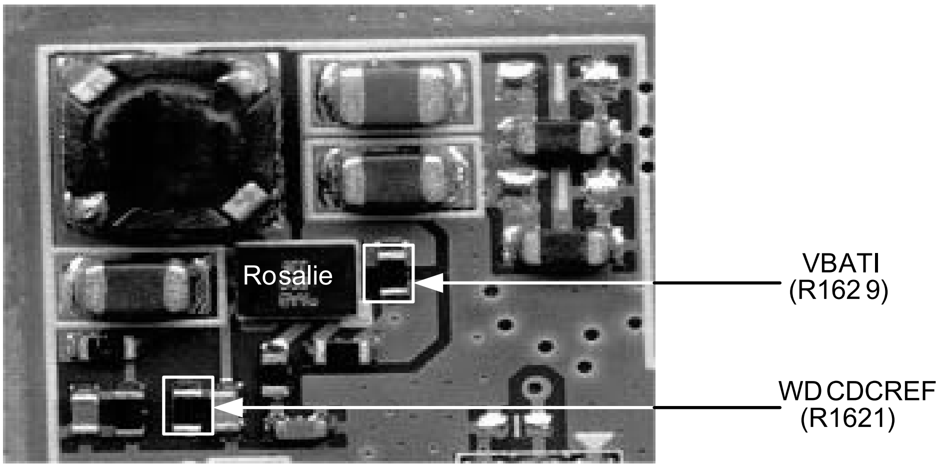


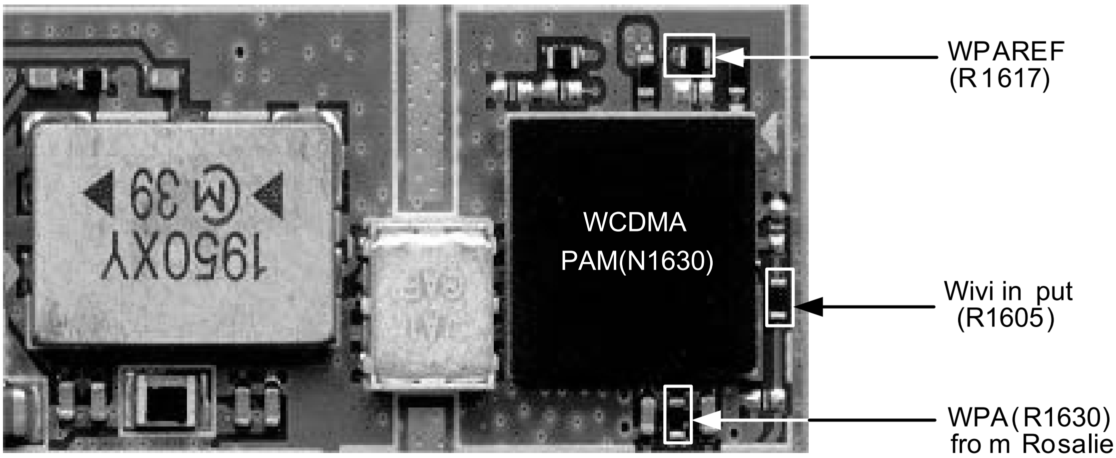
Figure 4-32. Connection for Checking RF TX Level

To verify that the phone fulfils requirements on maximum output power.



4.20.5 Checking PAM Block



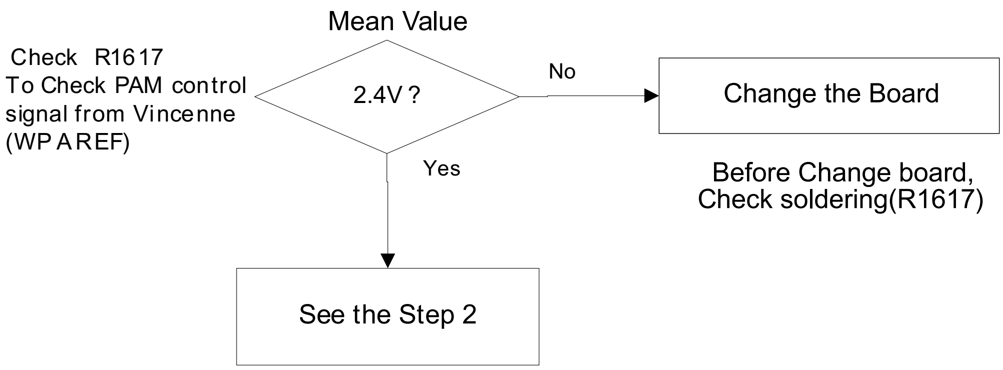


Step1: Check PAM(N1630) control signal from N2000
Step2: Check PAM(N1630) control signal from N1620

❈ Before Checking this part , must check 4.2 Common power source(Battery Direct) part

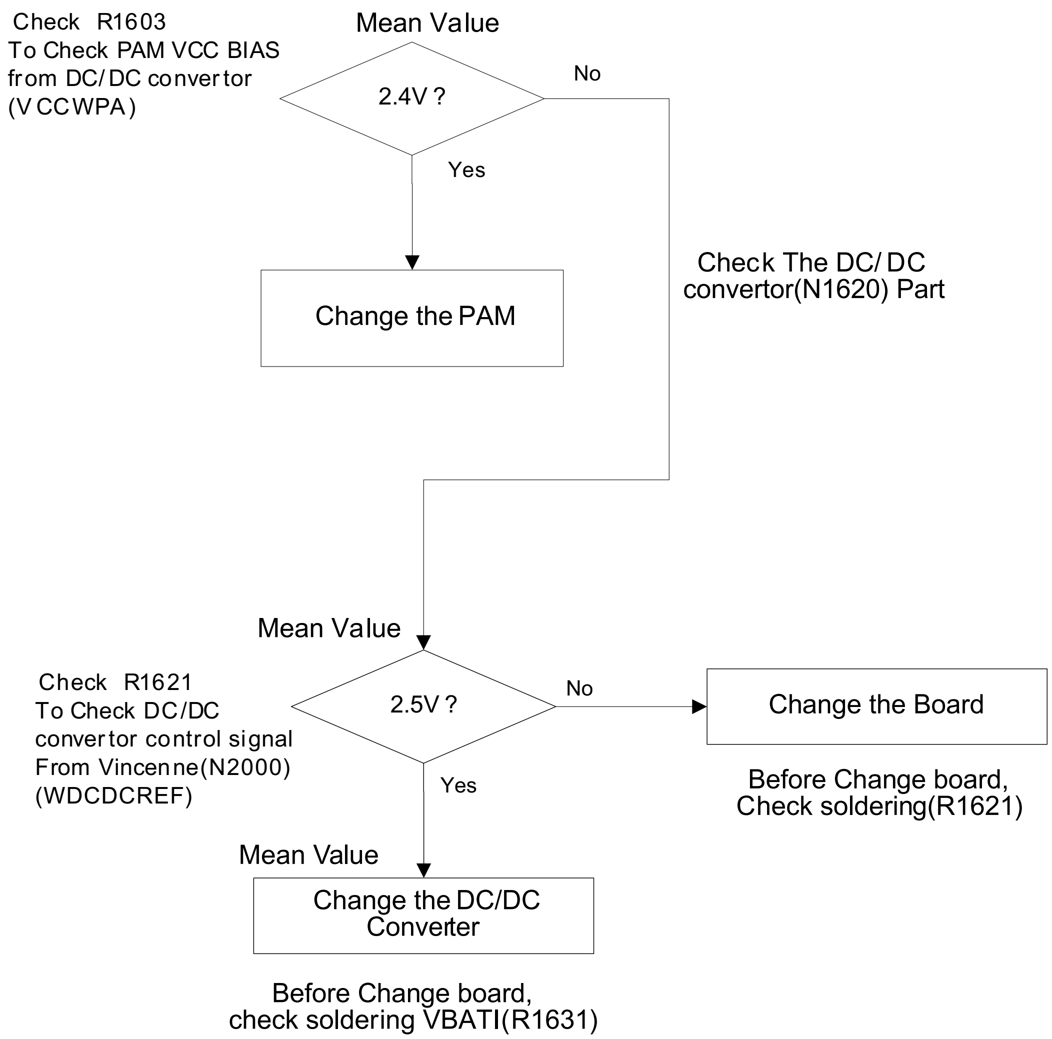
TP Command
-mode =4
-Wtxc=9750,0,1,0
-Syct=10700
-Txgn=1,43
-TFTI=10700

Step1: Check PAM control signal from N2000

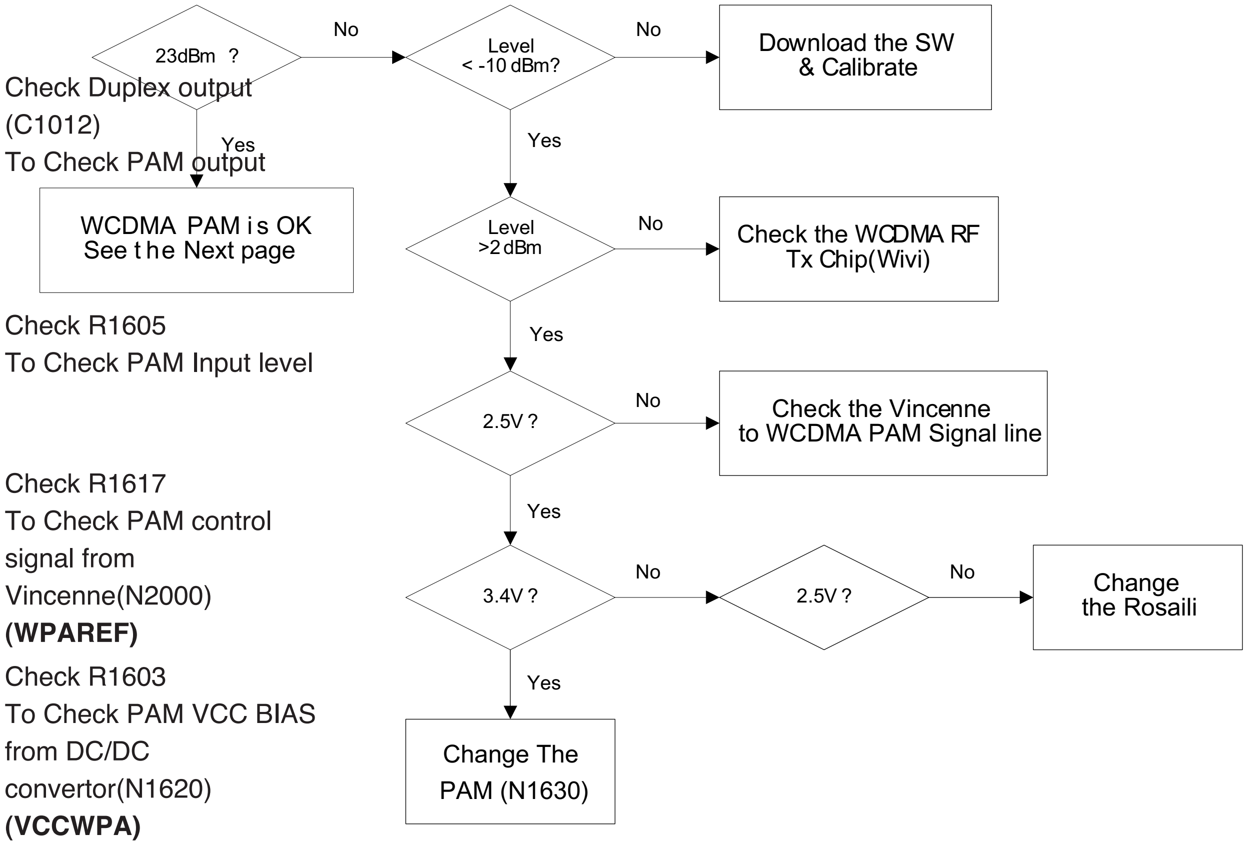


TP Command
-mode =4
-Wtxc=9750,0,1,0
-Syct=10700
-Txgn=1,43
-TFTI=10700

Step2: Check PAM control signal from DC/DC converter(N1620)



TP Command
-mode =4
-Wtxc=9750,0,1,0
-Syct=10700
-Txgn=1,43
-TFTI=10700



4.20.6 Checking RX I,Q

To verify the RX path you have to check the pk-pk level and the shape of the RX I,Q.

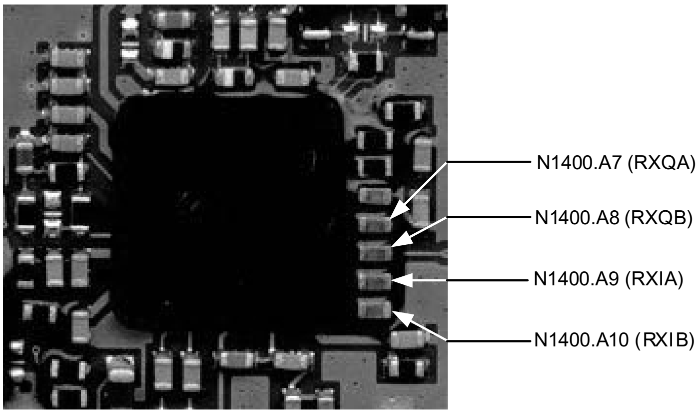
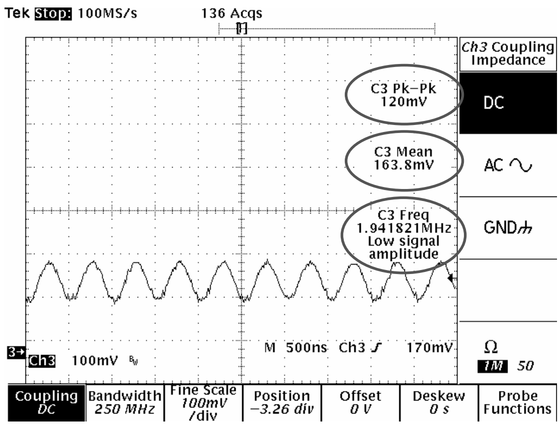
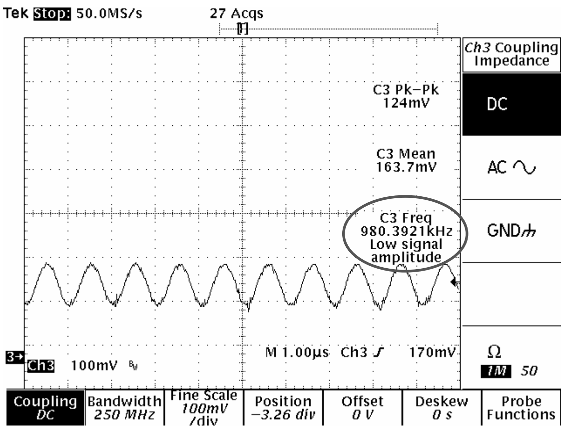


Figure 4-33. WCDMA RF RX IC (Top)



Feed a C W signal at 2142 MHz with a power level of –60dBm.

Figure 4-34. RX I,Q signal (CW:2142MHz)



Feed a C W signal at 2141 MHz with a power level of –60dBm.

Figure 4-35. RX I,Q signal (CW:2141MHz)

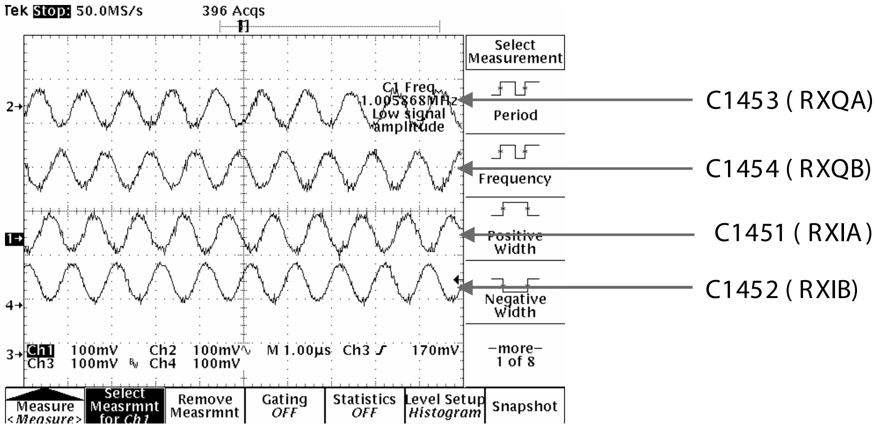
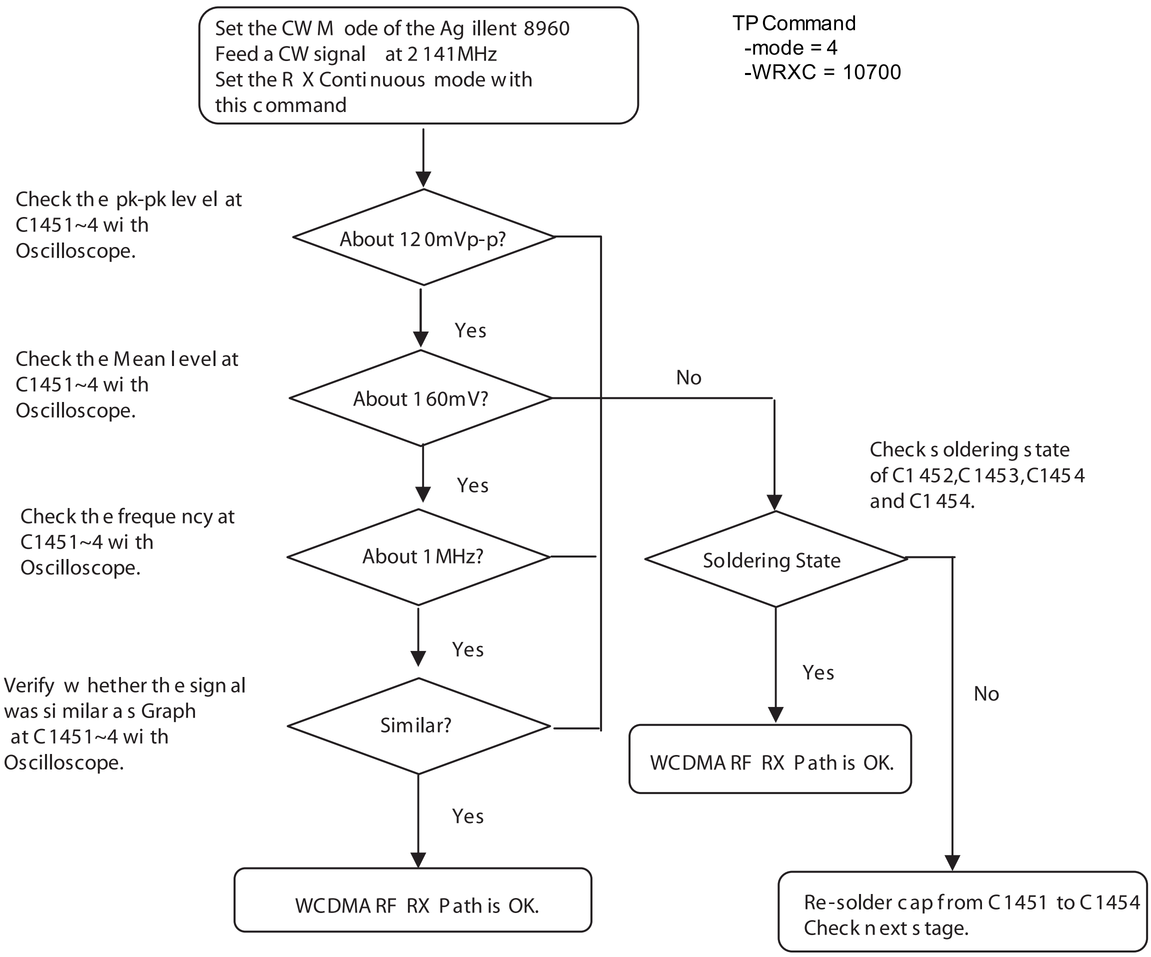


Figure 4-36. RX I, Q signal



4.20.7 Checking RX Level

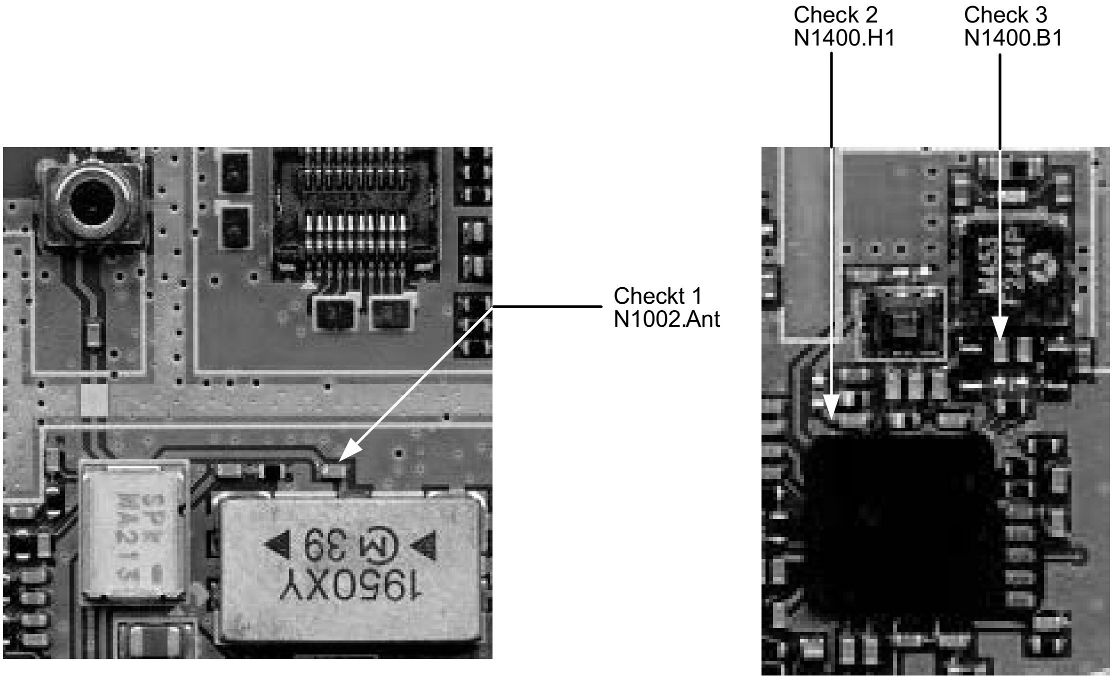


Figure 4-37. Peak level at N1400.B1

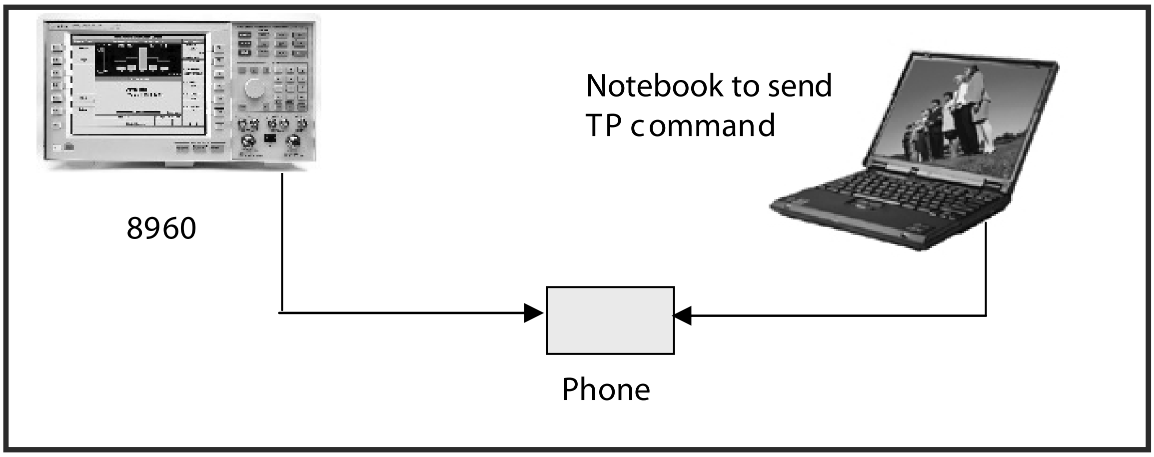
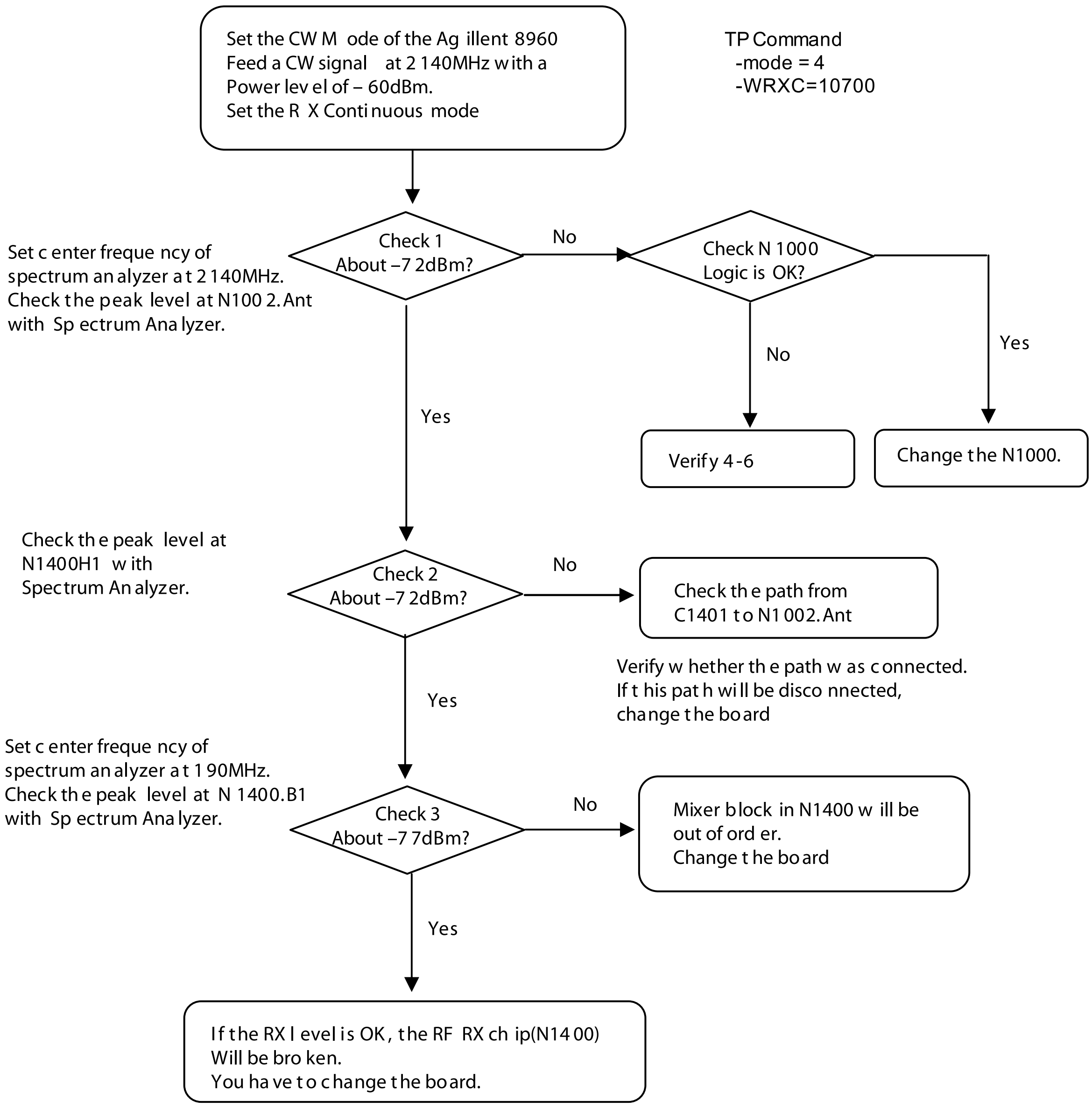
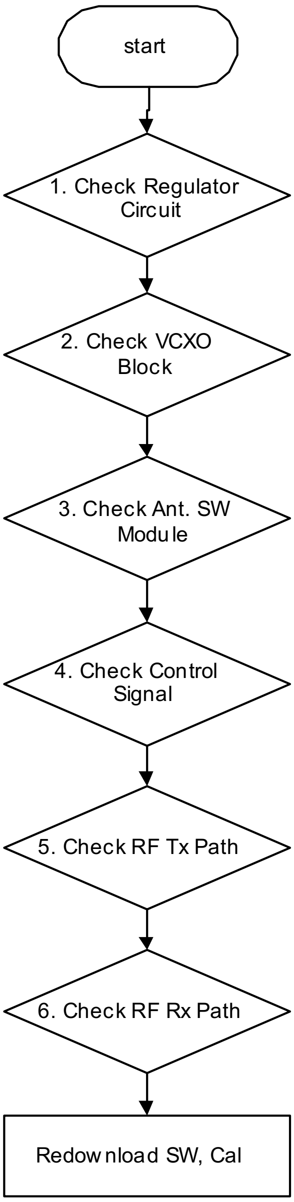
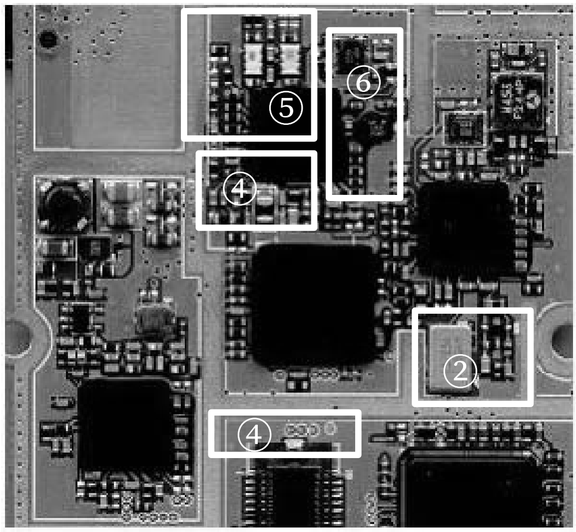


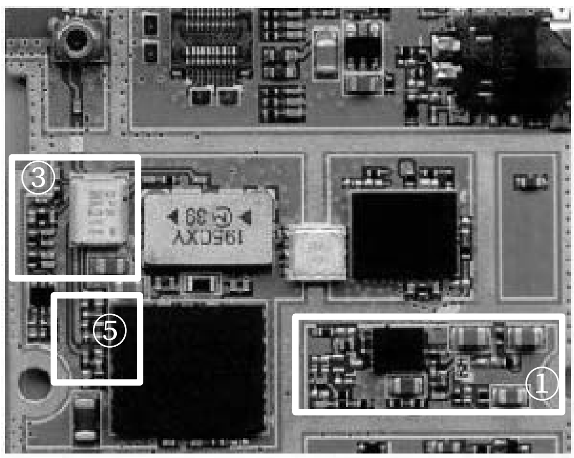
Figure 4-38. Connection for Checking RX Level


Set the CW Mode of the Agillent 8960
Feed a CW signal at 2140MHz with a
Power level of – 60dBm.
Set the RX Continuous mode
TP Command
-mode = 4
-WRXC=10700
Set center frequency of
spectrum analyzer at 2140MHz.
Check the peak level at N1002.Ant
with Spectrum Analyzer.
Check 1
About –72dBm?
No
Check N1000
Logic is OK?
No
Yes
Verify 4-6
Change the N1000.
Yes
Check the peak level at
N1400H1 with
Spectrum Analyzer.
Check 2
About –72dBm?
No
Check the path from
C1401 to N1002.Ant
Verify whether the path was connected.
If this path will be disconnected,
change the board
Yes
Set center frequency of
spectrum analyzer at 190MHz.
Check the peak level at N1400.B1
with Spectrum Analyzer.
Check 3
About –77dBm?
No
Mixer block in N1400 will be
out of order.
Change the board
Yes
If the RX level is OK, the RF RX chip(N1400)
Will be broken.
You have to change the board.

4.21 Checking GSM Block







4.21.1 Checking Regulator Circuit

Refer to chapter 4.3 Checking Common Power Source Block.
IF you already check this point while Checking Common Power Source Block, You can skip this test.

4.21.2 Checking VCXO Block

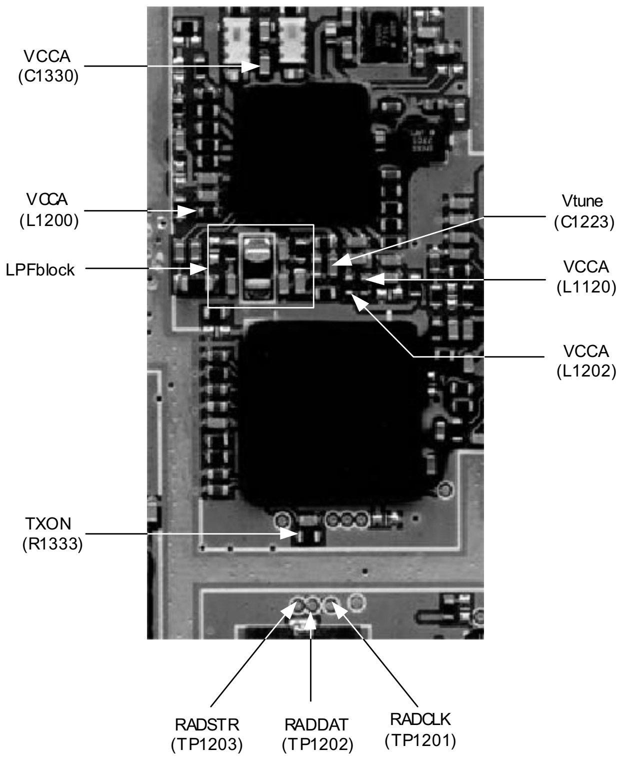
Refer to chapter 4.4 Checking VCXO Block.
IF you already check this point while Checking VCXO Block, You can skip this test.

4.21.3 Checking Ant. SW Module

Refer to chapter 4.6 Checking Antenna Switch Block input logic.
IF you already check this point while Checking Antenna Switch Block input logic, You can skip this test.

4.21.4 Checking Control Signal

Test Program Script
MODE=0
SWTX=1,64,7,1024,1



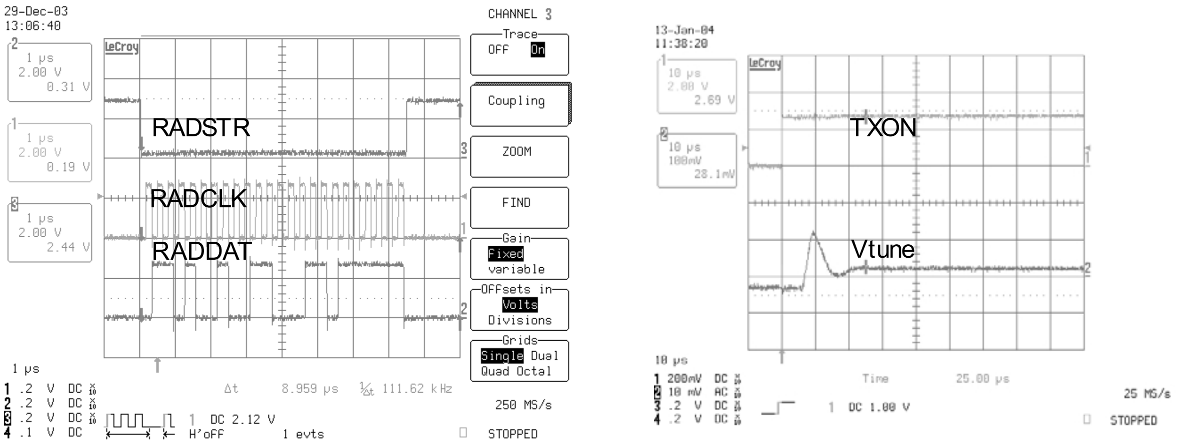
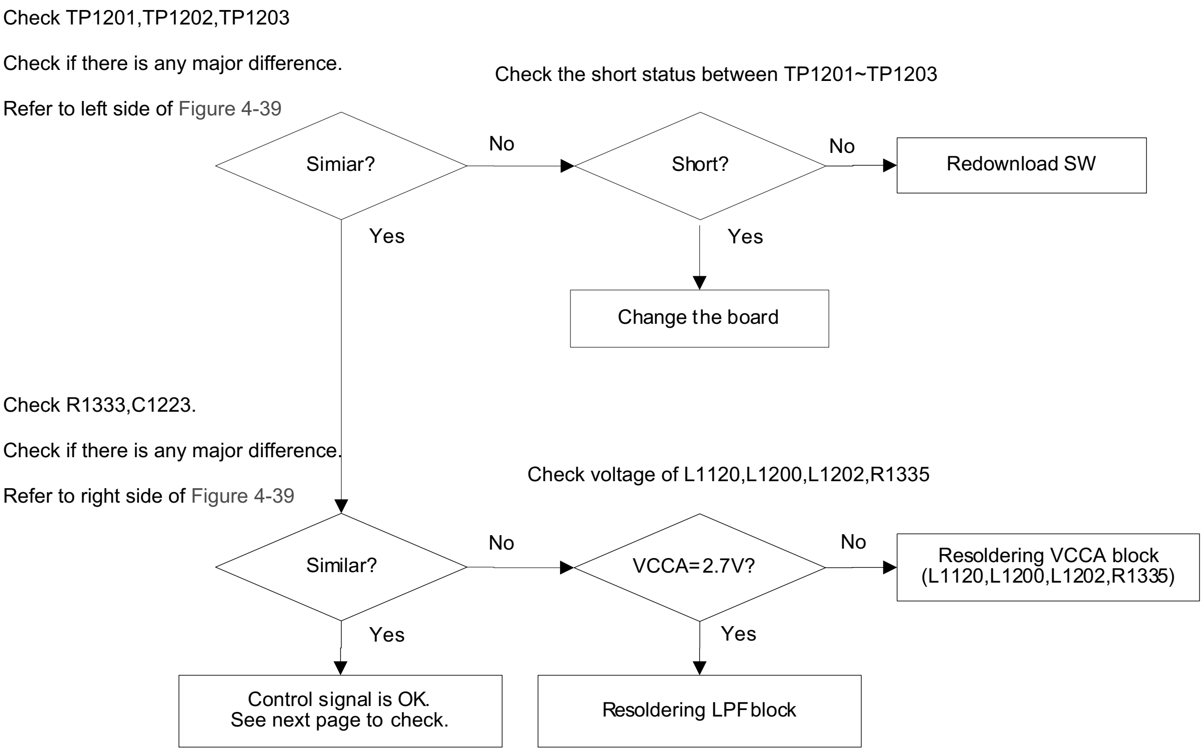


Figure 4-39. GSM RF Control signal


Check TP1201,TP1202,TP1203
Check if there is any major difference.
Refer to left side of Figure 4-39
Check the short status between TP1201~TP1203
Simiar?
No
Short?
No
Redownload SW
Yes
Yes
Change the board
Check R1333,C1223.
Check if there is any major difference.
Refer to right side of Figure 4-39
Check voltage of L1120,L1200,L1202,R1335
Similar?
No
VCCA=2.7V?
No
Resoldering VCCA block
(L1120,L1200,L1202,R1335)
Yes
Yes
Control signal is OK.
See next page to check.
Resoldering LPF block

4.21.5 Checking RF Tx Path

A. GSM Tx path Level

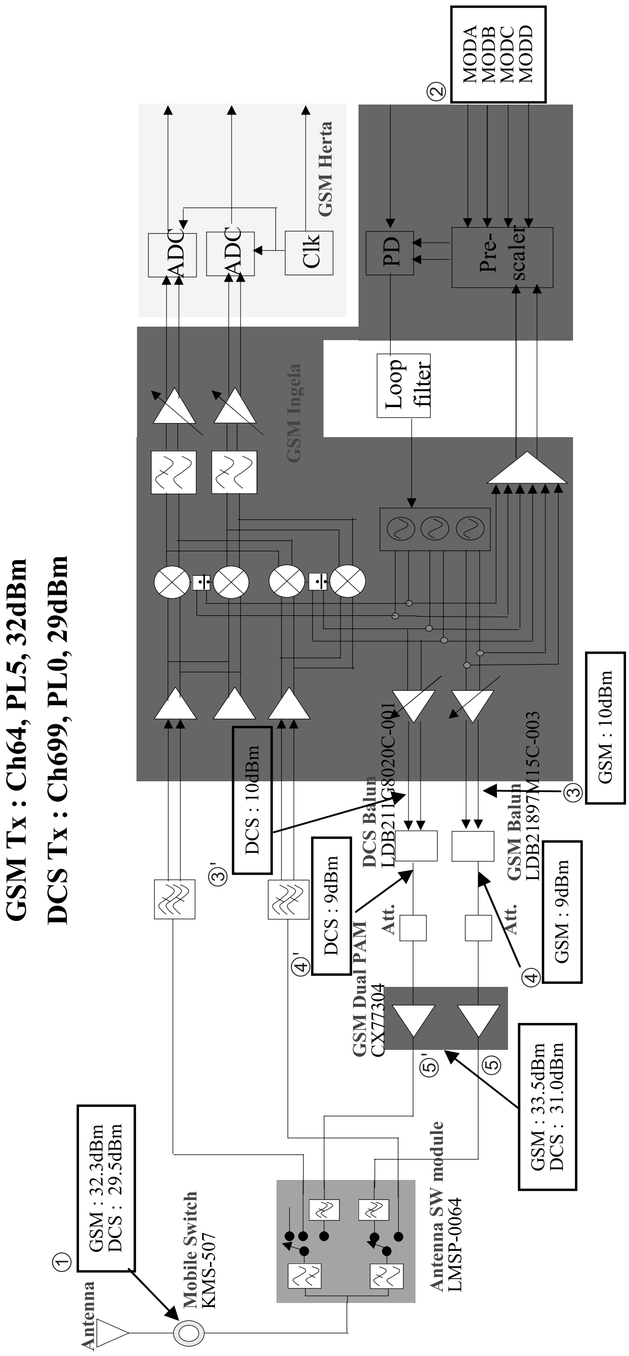


Figure 4-40. GSM/DCS Tx Path Level

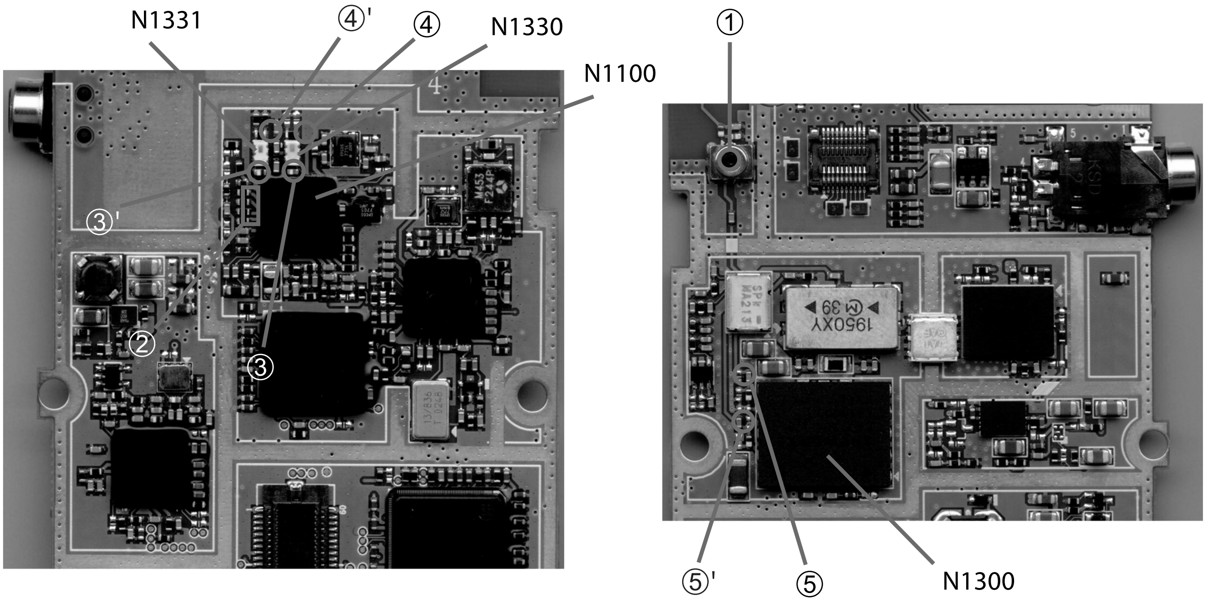


Figure 4-41. Test Point of GSM/DCS Tx path

B. GSM Tx Output Level Check

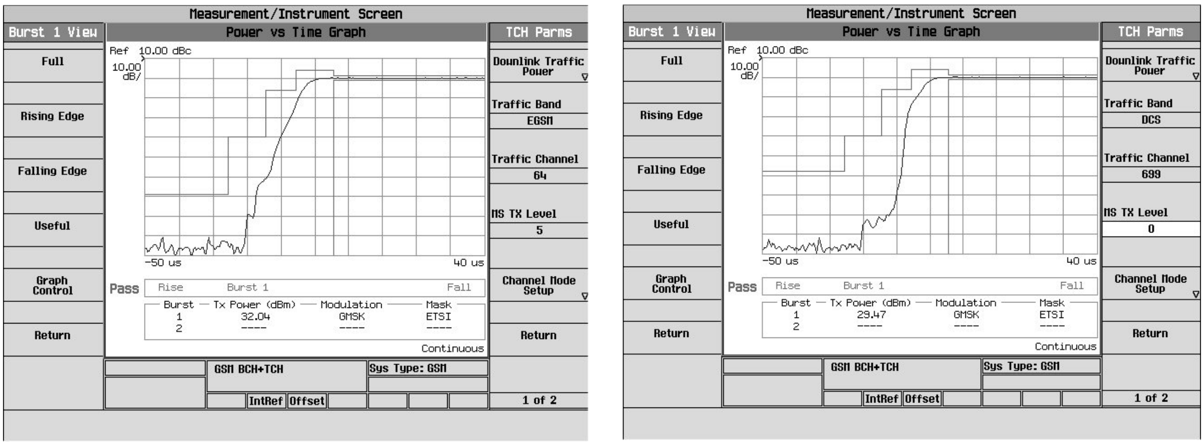


Figure 4-42. GSM Tx Level at ①

Test Program Script

1. GSM Tx

MODE=0
SWTX=1,64,5,1024,1

2. DCS Tx

MODE=2
SWTX=1,699,0,1024,1

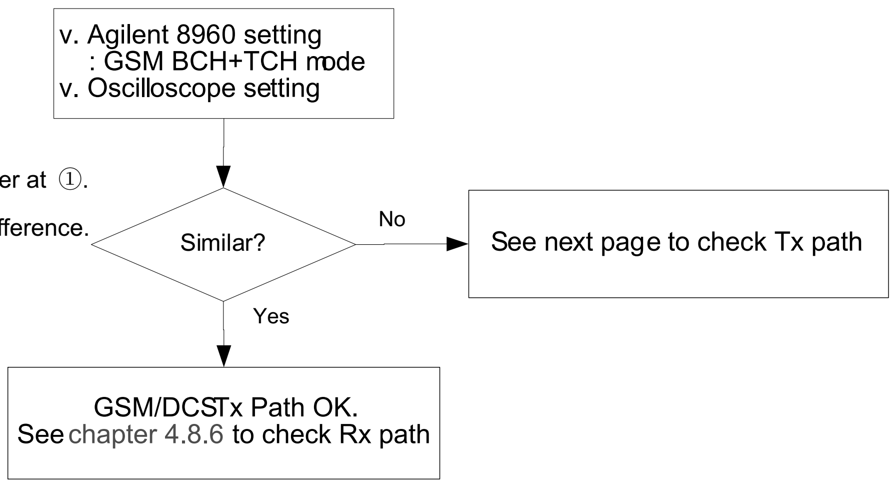
Check GSM/DCS output power at ①.

Check if there is any Major difference.

Refer to Figure 4-42.

GSM > 32dBm

DCS > 29dBm



C. GSM RF Transceiver IN/OUT Signal Check

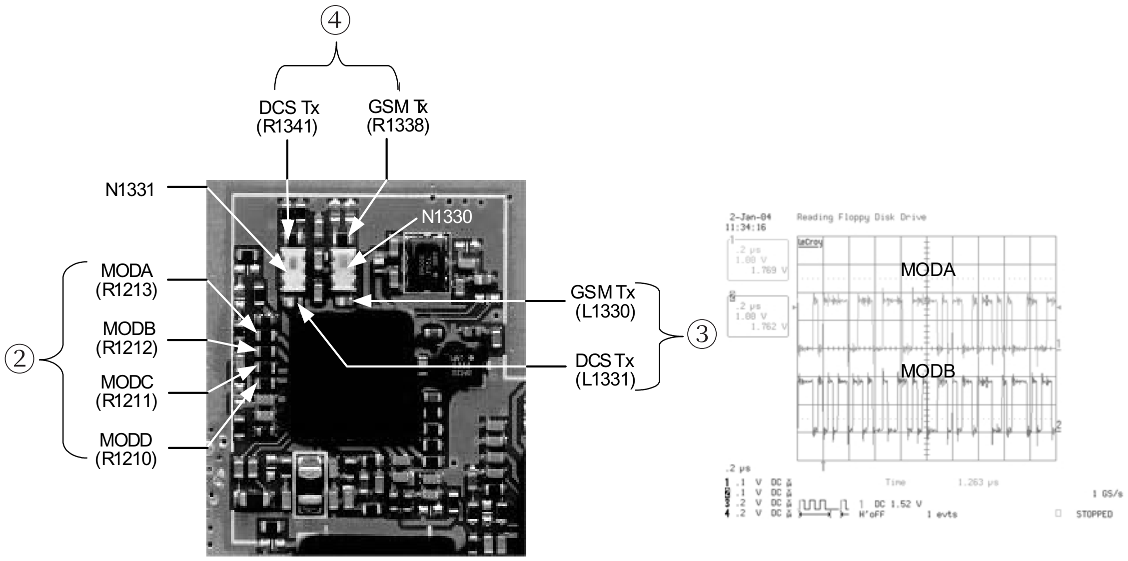


Figure 4-43. GSM Tx MODE signal

Check Mode(A/B/C/D)signal at ②.

Check if there is any Major difference.

Refer to right side of Figure 4-43.

Simiar?

No → Resoldering MODE block (R1210,R1211,R1212,R1213)

Yes

Check GSM RF Transceiver Output power at ③ .

GSM/DCS >- 5dBm

No → Redownload SW

Yes

Check GSM/DCS Tx Balun output power at ④ .

GSM/DCS >- 7dBm

No → Resoldering Tx Balun GSM : N1330 DCS : N1331

Yes

See next page to check Tx path

D. GSM PAM Check

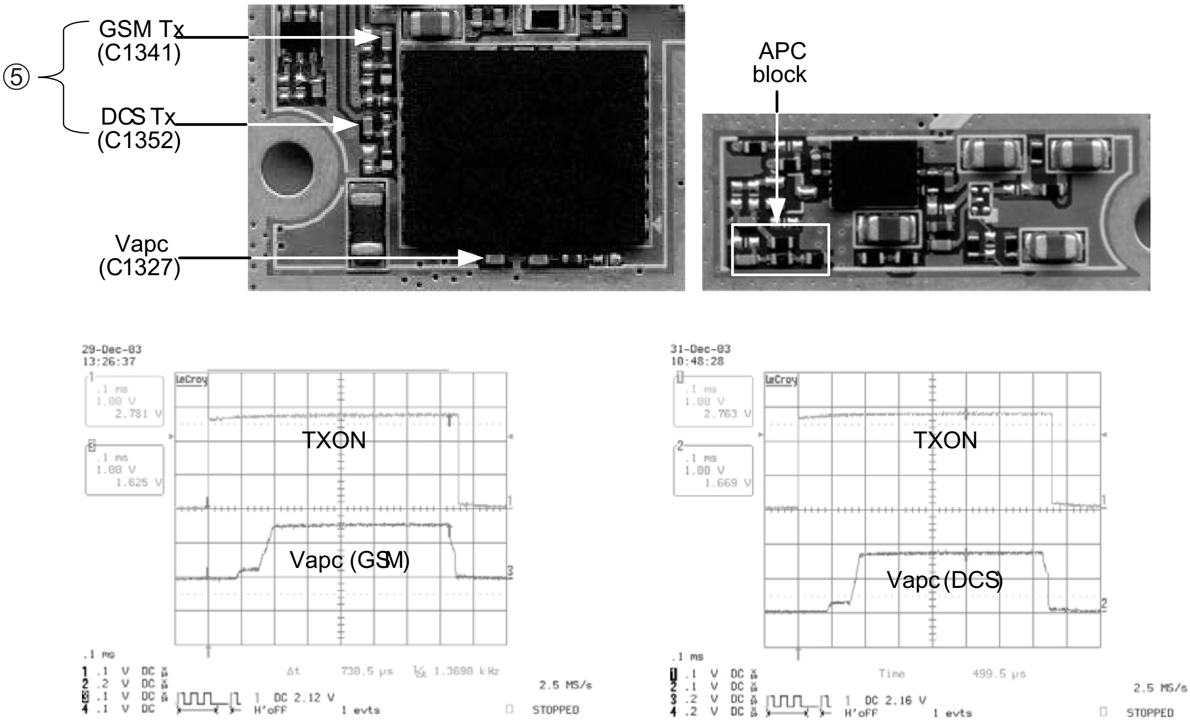


Figure 4-44. GSM/DCS Tx control signal

Check Vapc level.
Check if there is any Major difference.
Refer to Figure 4-44.

Vapc > 1.5V ?

- No → Resoldering APC block
- Yes ↓

Check GSM/DCS PAM output power at ⑤ .

GSM:>23dBm
DCS:>20dBm

- No → Changing GSM PAM (N1300)
- Yes ↓

GSM Tx Path OK. See Next page to check

4.21.6 Checking RF Rx Path

A. GSM Rx path Level

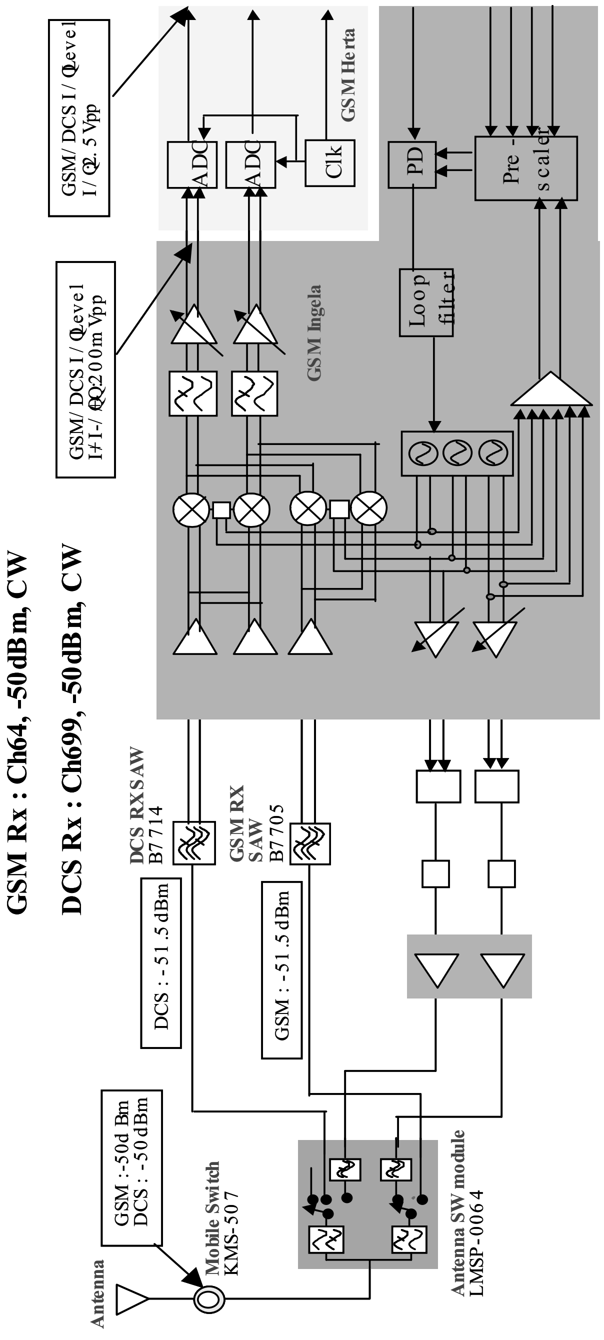
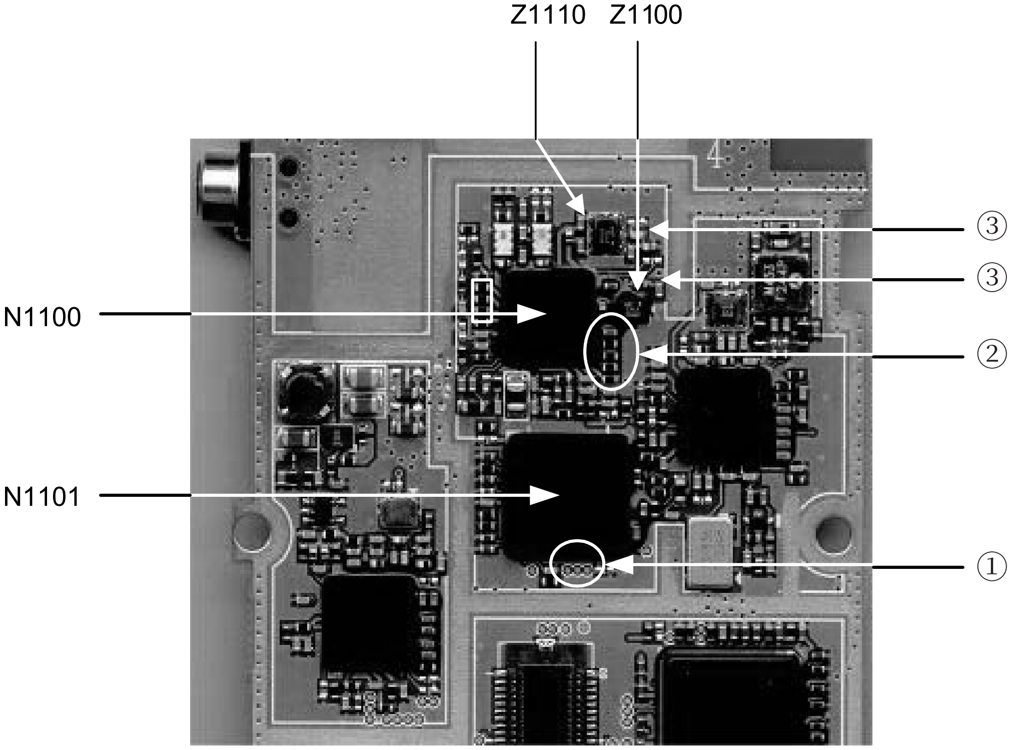


Figure 4-45. GSM/DCS Rx Path Level



Test Program Script

1. GSM Rx

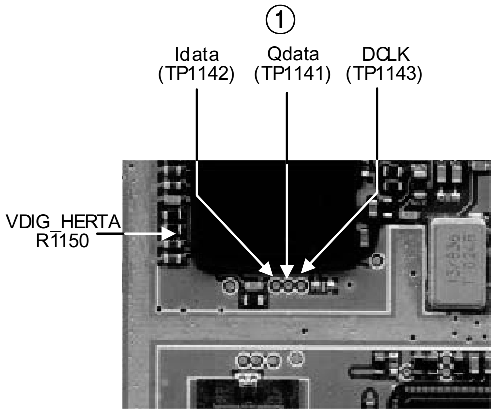
MODE=0
SWRX=64,1024,2

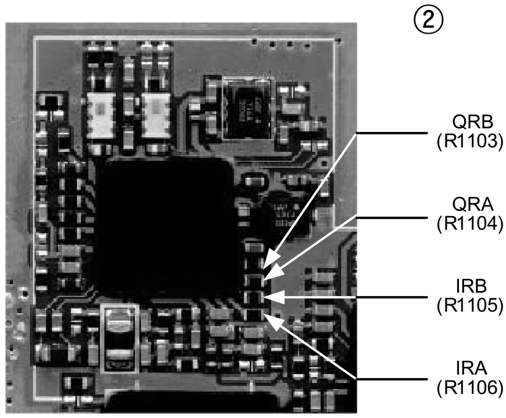
2. DCS Rx

MODE=2
SWRX=699,1024,2

v Agilent 8960 Setting
CW Mode
GSM : -50dBm@Ch65(948MHz)
DCS : -50dBm@Ch700(1842.8MHz)
v Oscilloscope Setting

B. GSM I/Q Signal Check





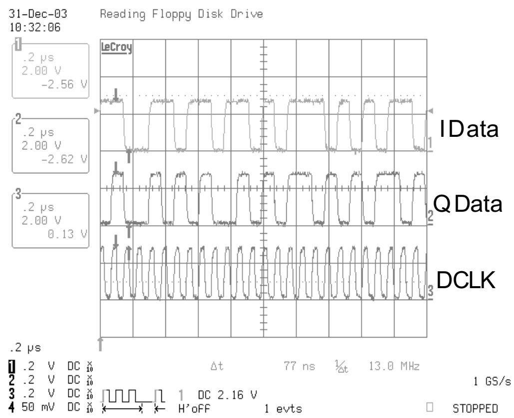


Figure 4-46. Herta IQ data and DCLK

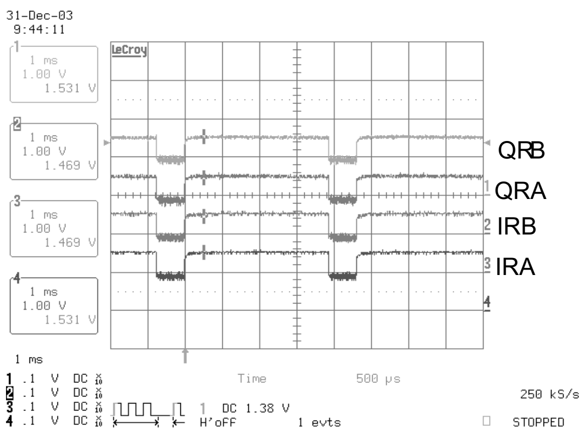


Figure 4-47. Ingela IQ signal

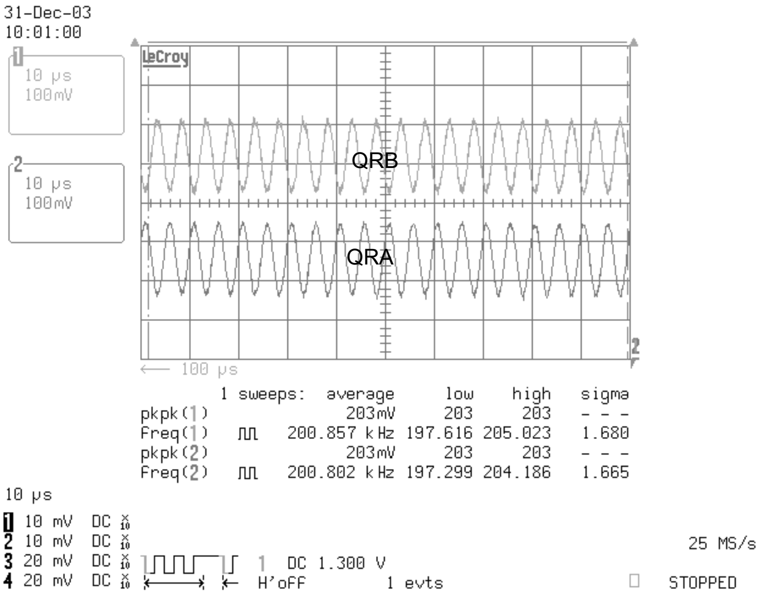


Figure 4-48. Ingela IQ signal

Check GSM/DCS Rx IQ data at ①.

Check if there is any Major difference.

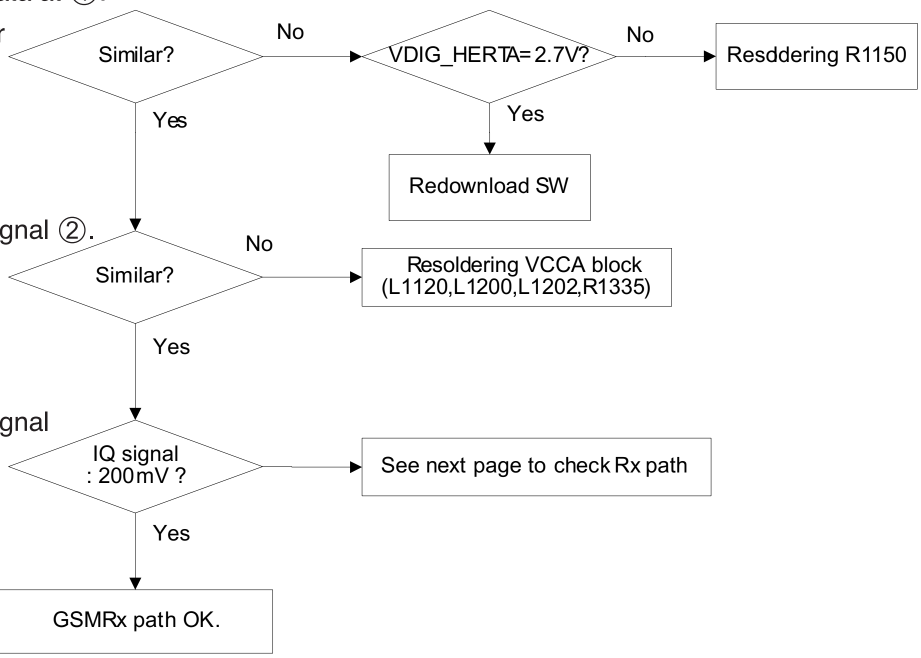
Refer to Figure 4-46.

Check GSM/DCS Rx IQ signal ②.

Refer to Figure 4-47.

Check GSM/DCS Rx IQ signal level at ②.

Refer to Figure 4-48.



C. GSM RF Level Check

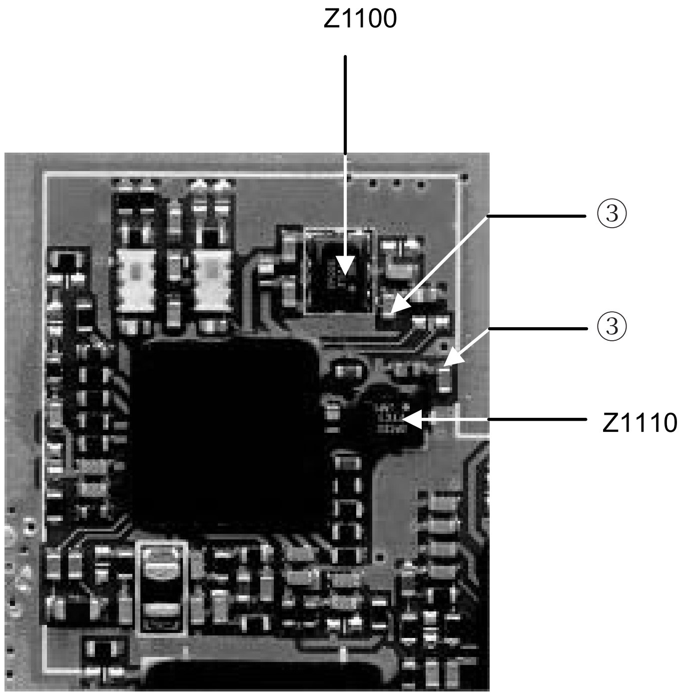


Figure 4-49. GSM/DCS Rx Path

v Agilent 8960 Setting
CW Mode
GSM : -50dBm@Ch65(948MHz)
DCS : -50dBm@Ch700(1842.8MHz)

Check GSM/DCS Rx signal level at ③.

GSM:-51.5dBm
DCS:-51.5dBm

No → Change Ant. SW module (N1000)

Yes → GSM Rx path OK.

5. BLOCK DIAGRAM

5.1 GSM & WCDMA RF Block

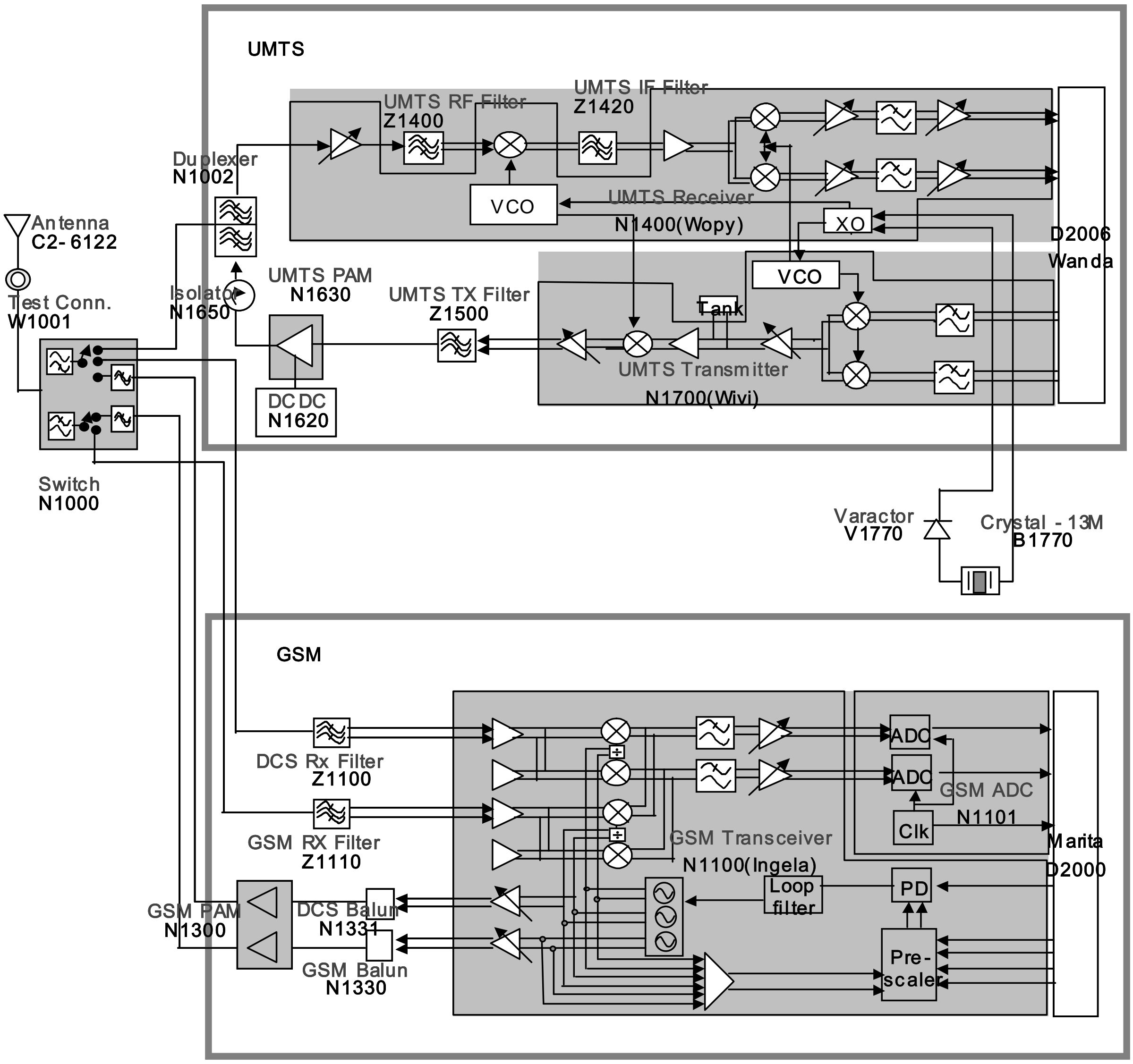


Figure 5-1. RF Block Diagram

Block	Ref. Name	Part Name	Function	Comment
Common	N1000	LMSP-0064	Switch	Band select
	W1001	KMS-507	Test Connector	Calibration, etc
	B1770	TSX-8A	Crystal	Reference –13M
WCDMA	N1002	DFYK61G95LBNCB	Duplexer	TRX
	N1400	LZT-108-5323(WOPY)	Receiver	RX
	Z1400	LK20A	RX RF Filter	RX
	Z1420	TMX-M453	RX IF Filter	RX
	N1620	MAX1820ZEBC	DC/DC	TX
	N1630	RF9266	PAM	TX
	N1650	CEO0401G95DCB	Isolator	TX
	N1700	LZT-108-5322(WIVI)	Transmitter	TX
	Z1500	SX-S205B	TX RF Filter	TX
	D2006	ROP-101-3033 (WANDA)	Analog Baseband	TRX
GSM	Z1100	B7714	DCS RX Filter	Direct Conversion
	Z1110	B7705	GSM RX Filter	Direct Conversion
	N1100	LZT-108-5325 (INGELA)	Transceiver	TRX
	N1300	CX77304	PAM	GSM/DCS Dual
	N1330	LDB21897M15C	GSM Balun	TX
	N1331	LDB211G8020C	DCS Balun	TX
	D2000	POP-101-3035 (MARITA)	Modem	

Table 5-1. RF Block Component

5.2 Interface Diagram

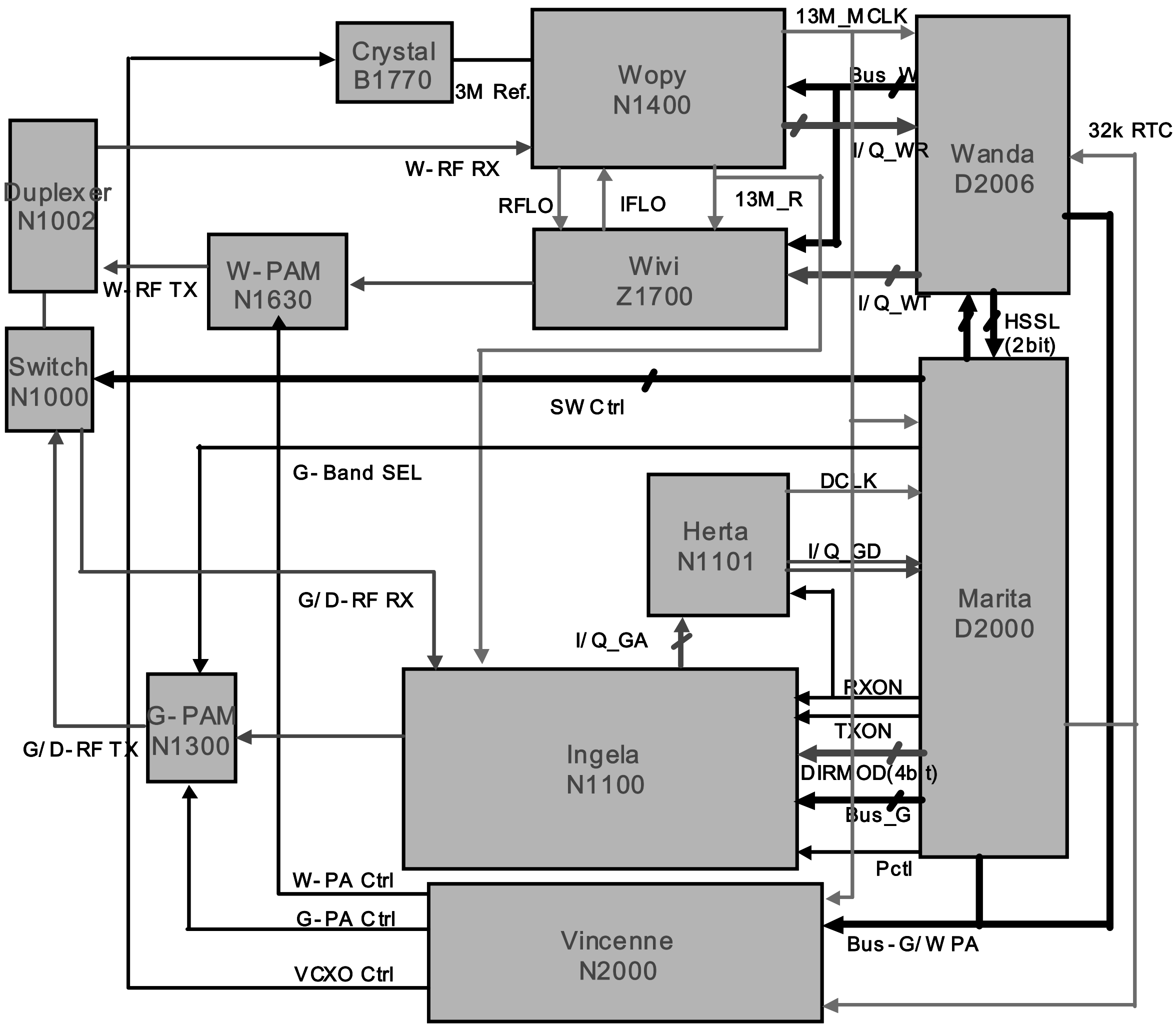


Figure 5-2. Interface Diagram 1

Function Block	Name	Schematic_Signal Name	Function
13M	13M_MCLK	MCLK	Main clock to BB
	13M_R	XOOA/XOOB	Ref for PLL
LO	RFLO	RFLO/RFLOBAR	RF LO Generation
	IFLO	IFLO/IFLOBAR	IF LO Generation
32K	32K	RTCCLK	Real Time
Signal	W-RF RX	WCDMA_RX	RX RF signal
	W-RF TX	WCDMA_TX	TX RF signal
	G/D-RF RX	GSM_RX/DCS_RX	RX RF signal
	G/D-RF TX	GSM_TXDCS_TX	RX RF signal
	I/Q_WR	RXIA/RXIB/RXQA/RXQB	WCDMA RXIQ
	I/Q_WT	TXIA/TXIB/TXQA/TXQB	WCDMA TXIQ
	I/Q_GA	IRA/IRB/QRA/QRB	GSM RX analog
	I/Q_GD	IDATA/QDATA	GSM RX digital
Control	SW Ctrl	ANTSW0/1/2/3	Band/System switch
	G-Band SEL	BSEL0	GSM/DCS switch
	W-PA Ctrl	WPAREF	PAM Ref. Bias
	G-PA Ctrl	PAREG	Power control
	Pctl	PCTL	TX power control
	VCXO Ctrl	VCXOCONT	AFC
	RXON	RXON	RX block ON
	TXON	TXON	TX block ON
Bus	Bus_W	WDAT/WCLK/WSTR	PLL program
	Bus_G	RADDAT/RADCLK/RADSTR	PLL program
	Bus-G/WPA	DACDAT/DACCLK/DACSTR	TX Gain program

Table 5-2. Interface Signal Block

5.3 Detailed Interface Signal

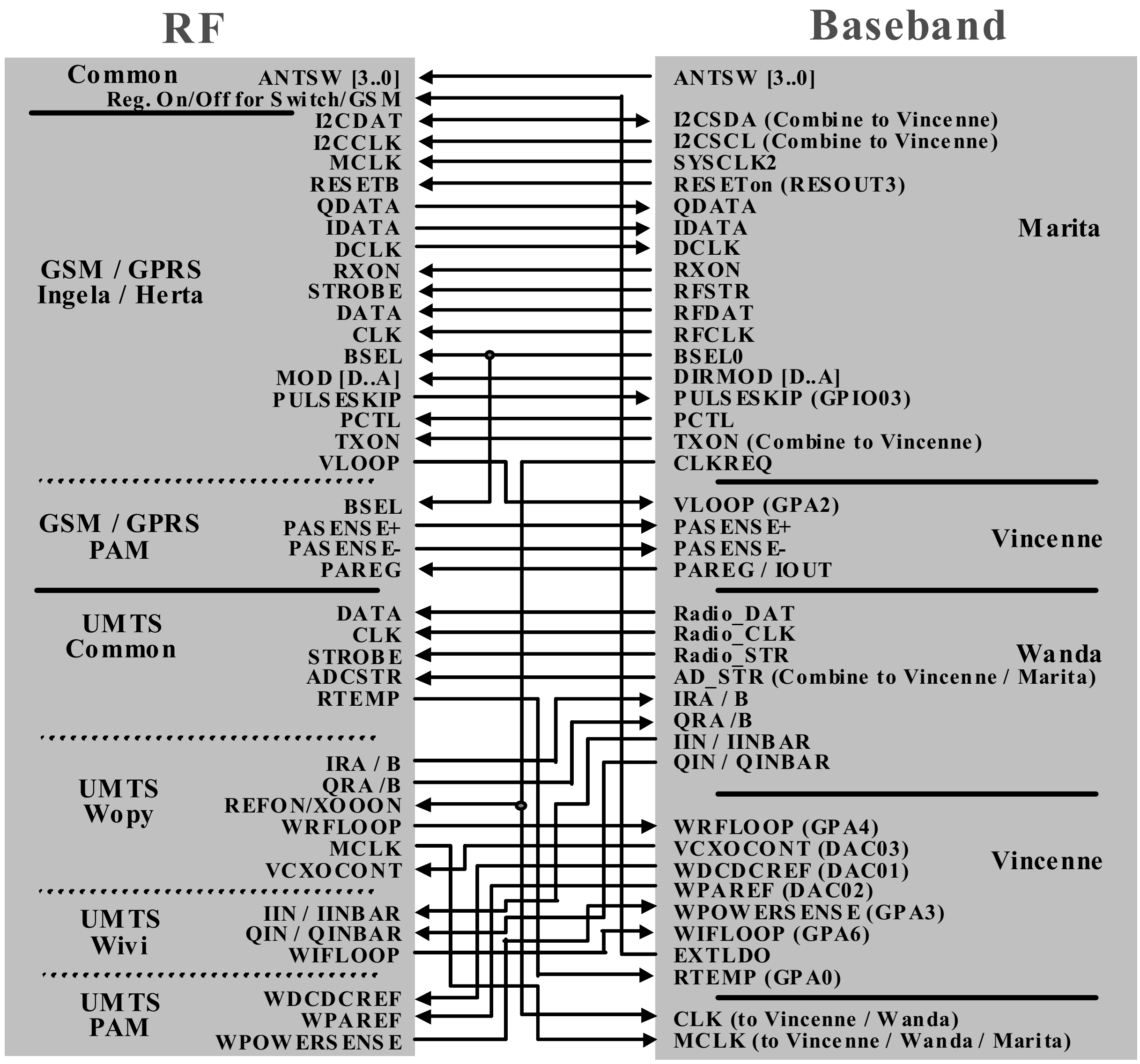


Figure 5-3. Interface Diagram 2

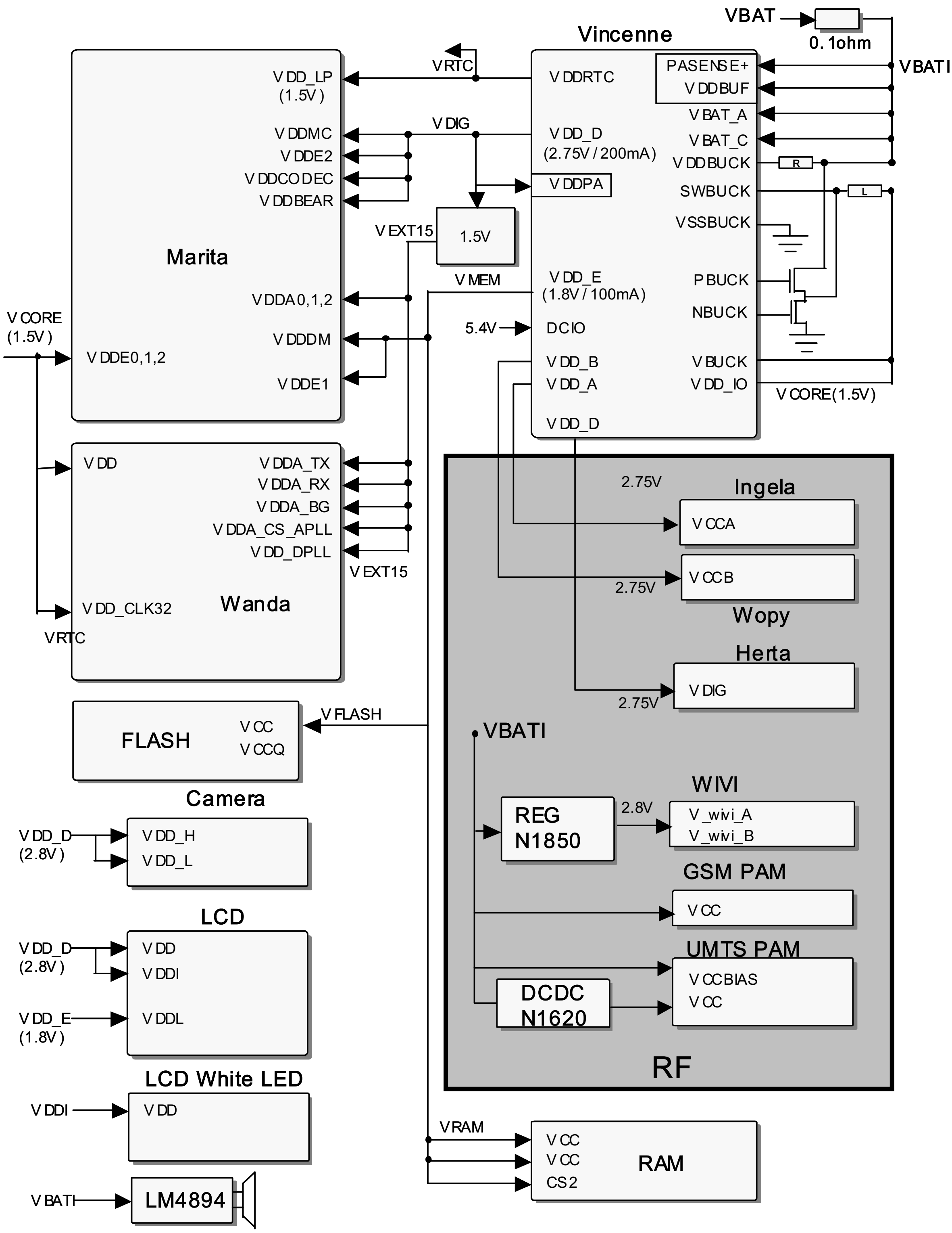
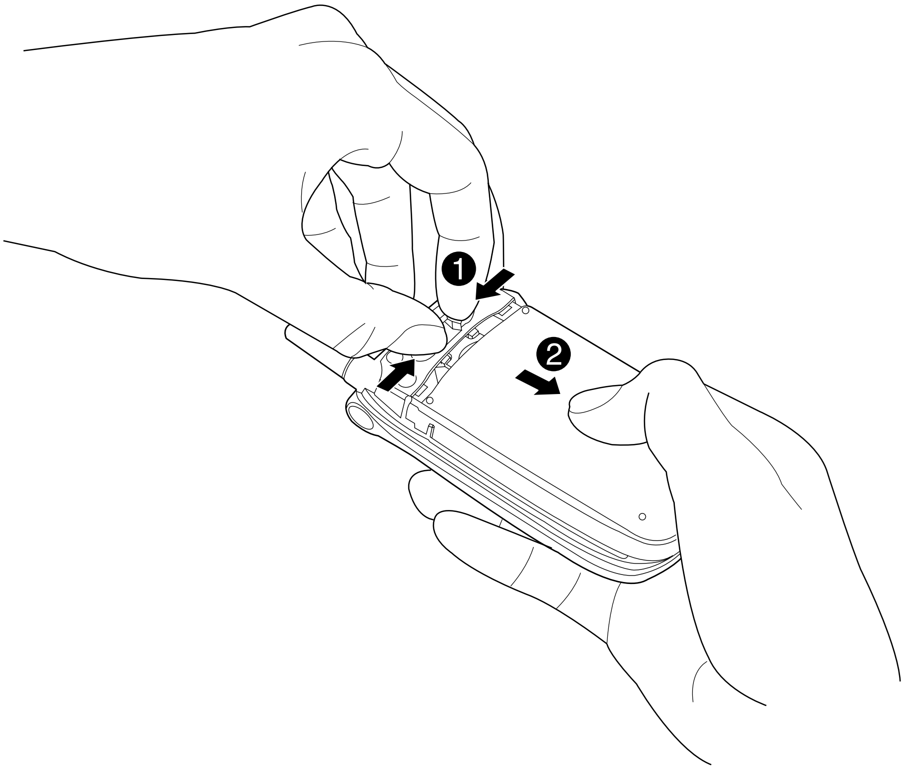
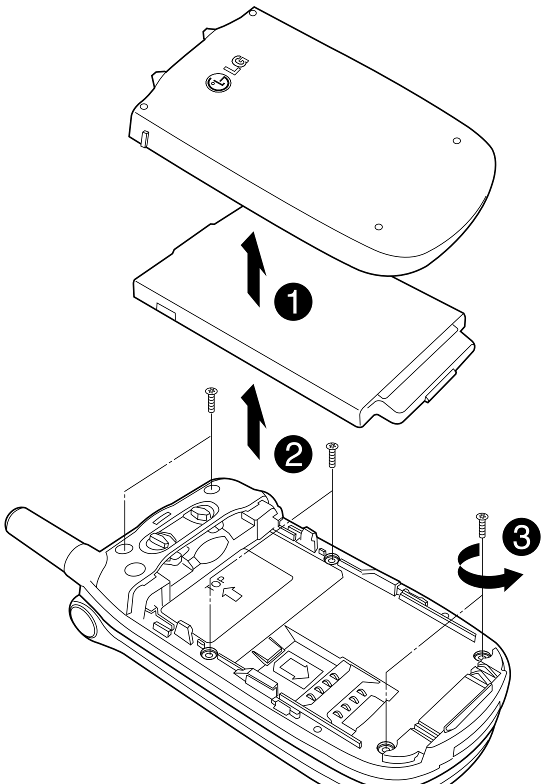
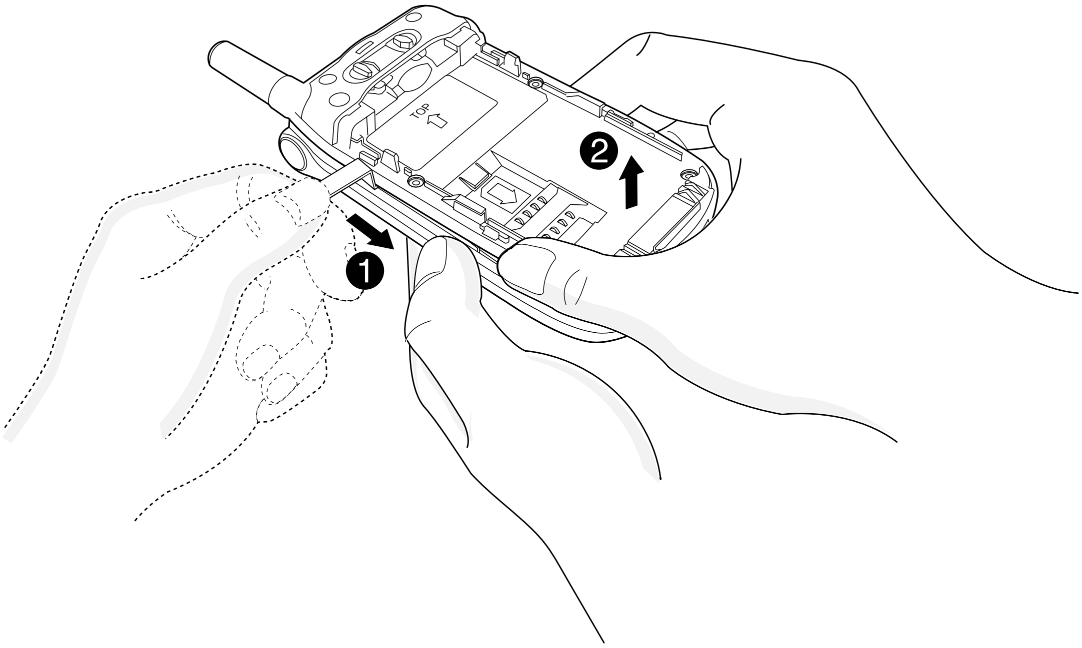


Figure 5-4. Power Diagram

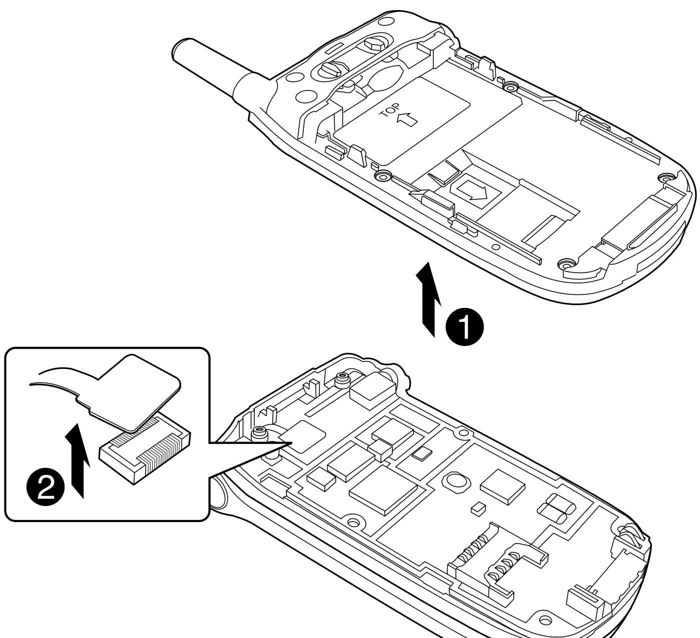
6. DISASSEMBLY INSTRUCTION







2
1
TOP



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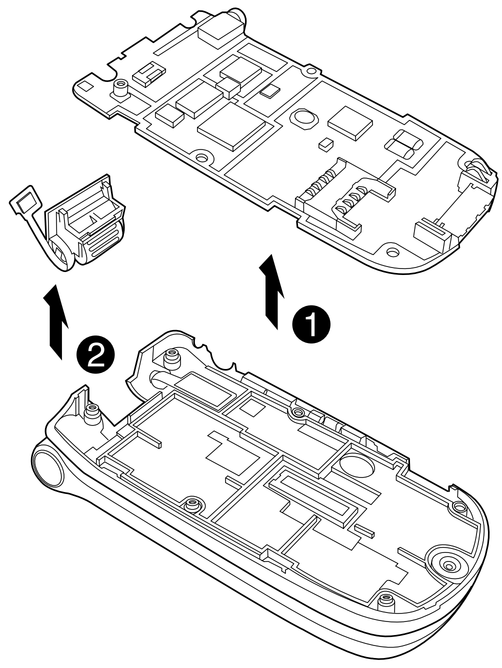
2
TOP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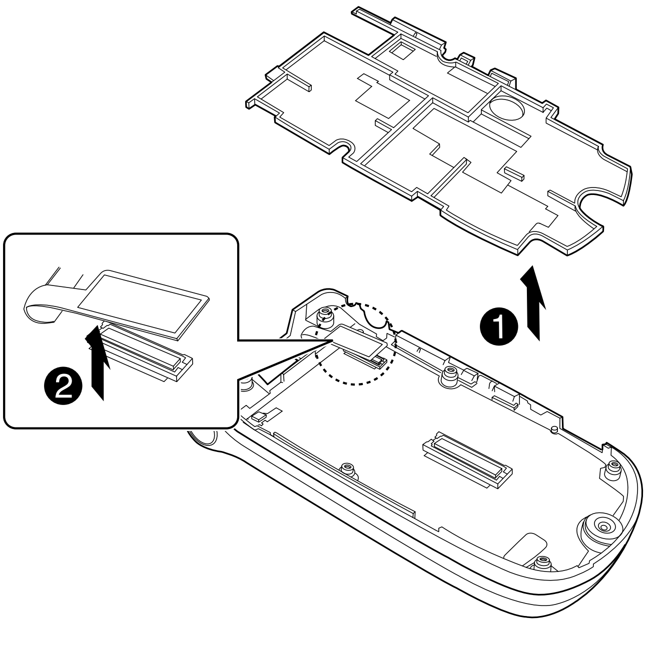
❷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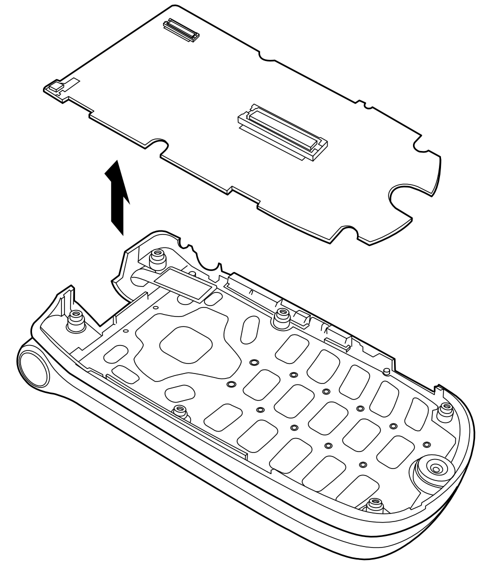
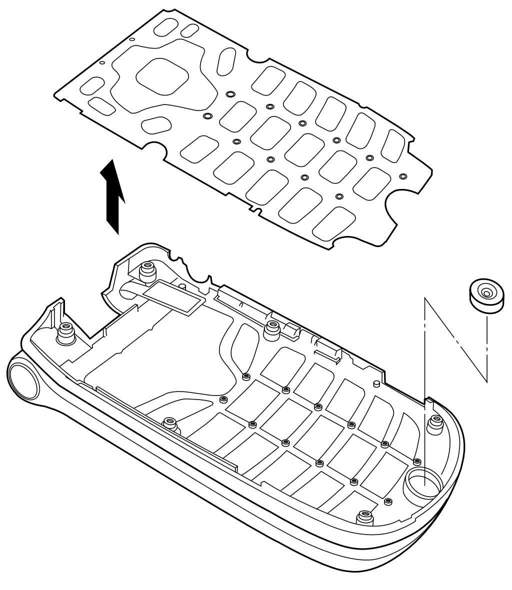
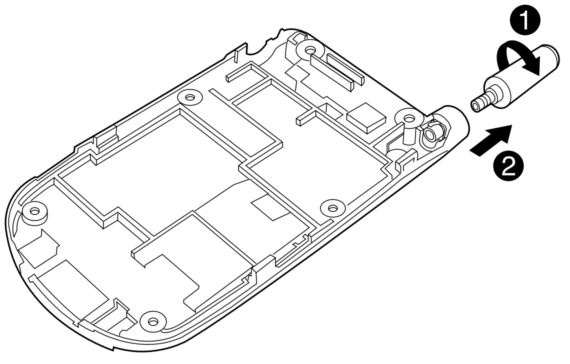
❷



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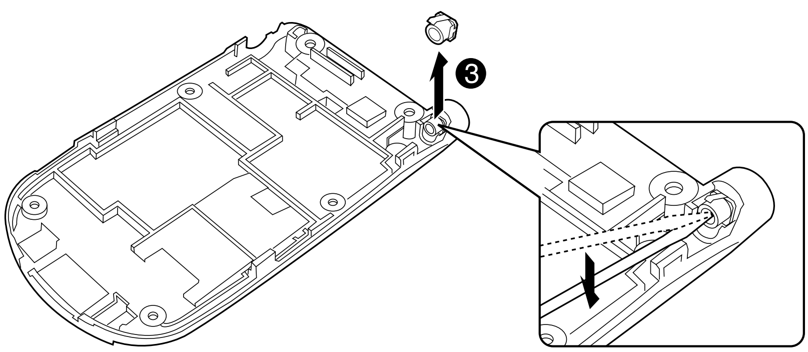
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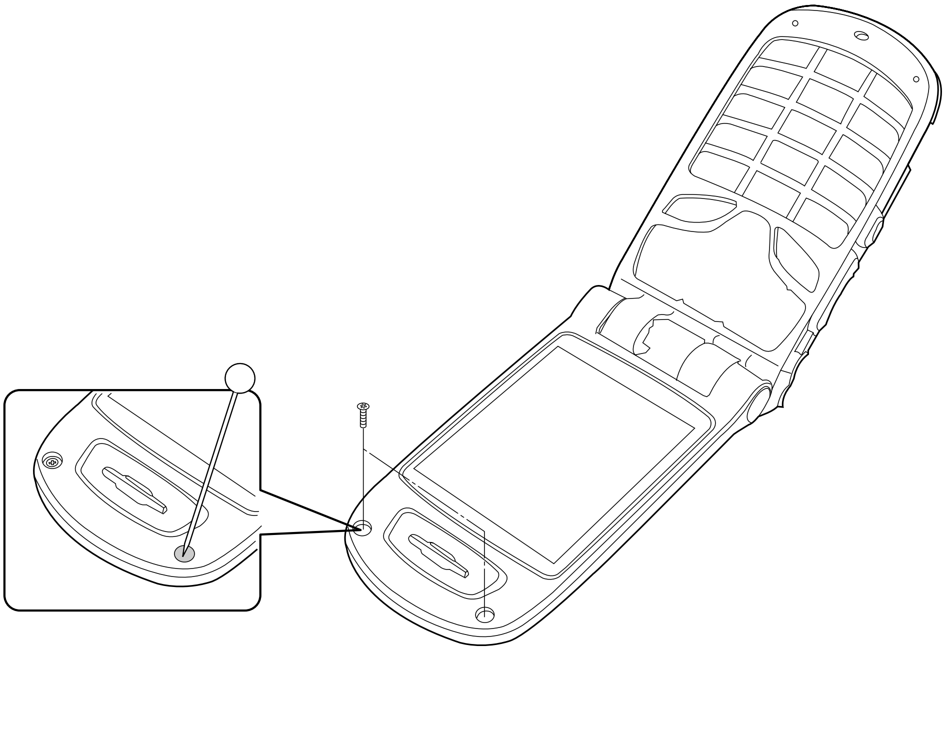

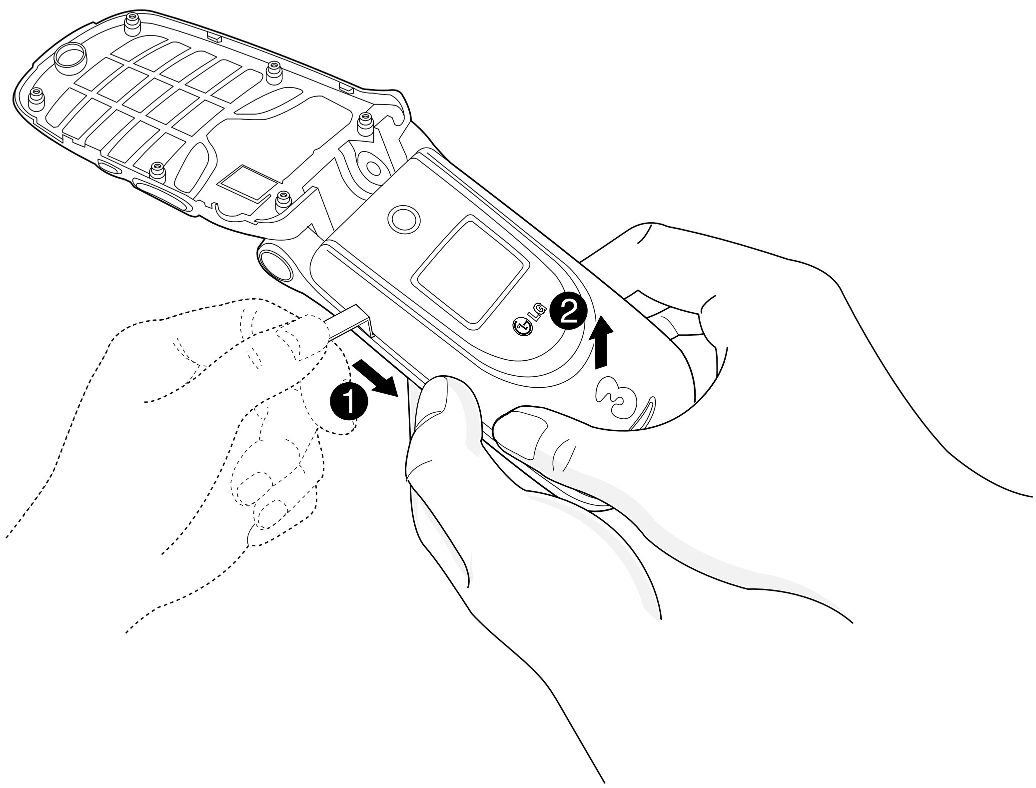
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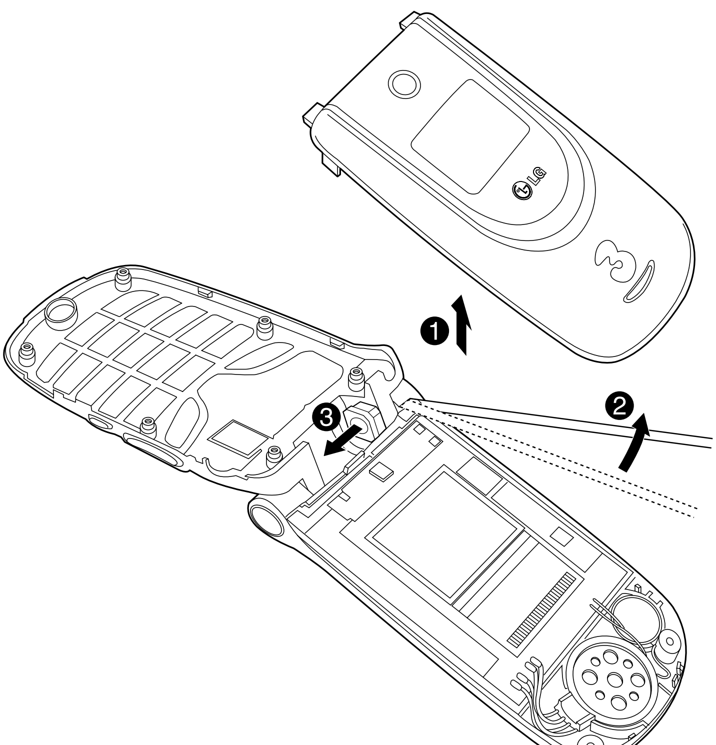
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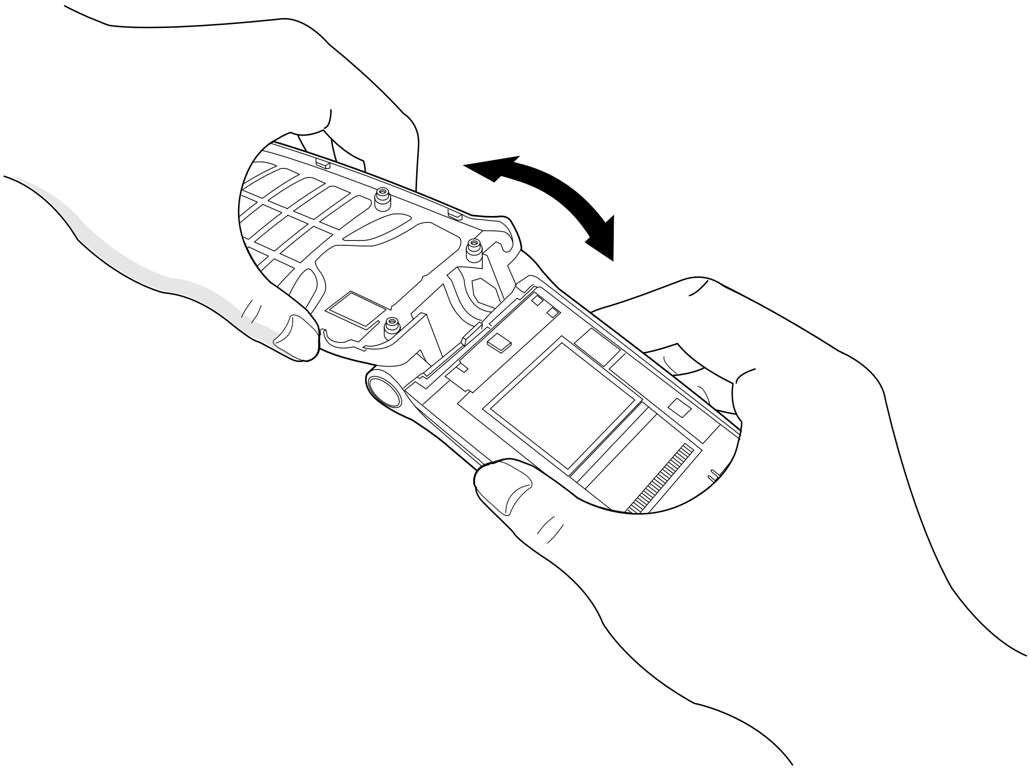
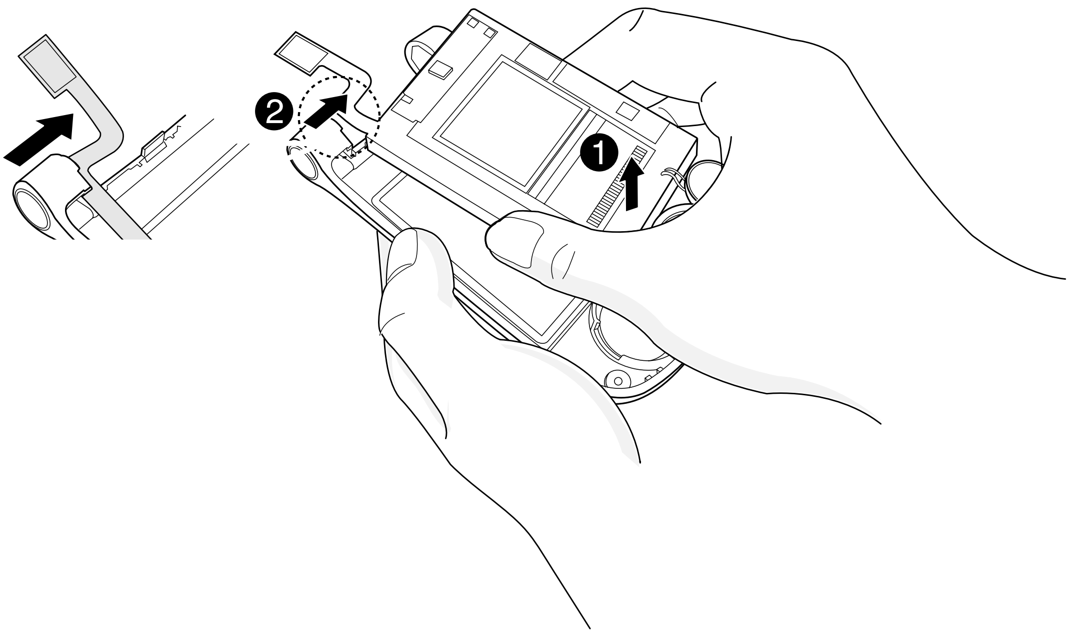
2
3





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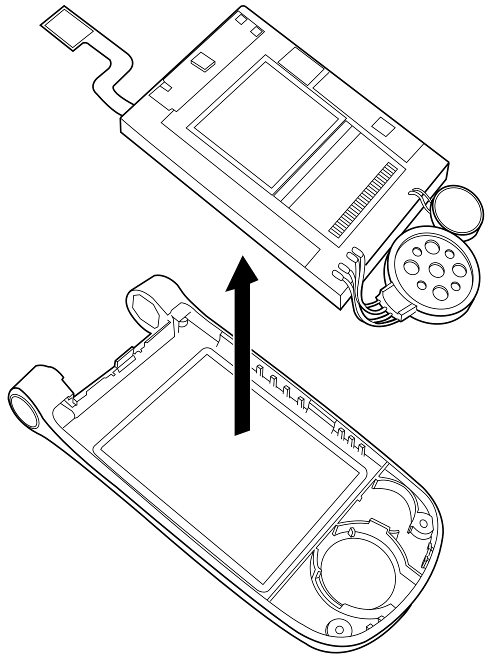
1

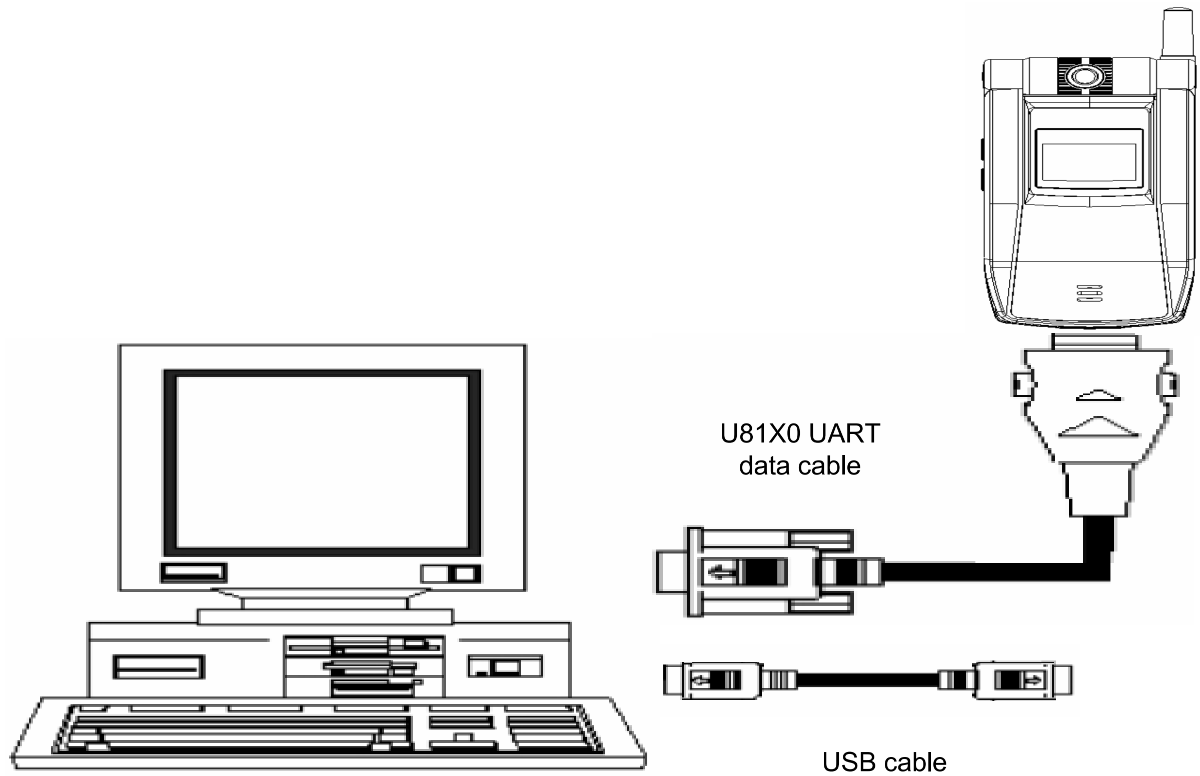


7. DOWNLOAD

The Purpose of Downloading Software

- To make a phone operate at the first manufacturing
  – A phone = Hardware + Software
  – A phone cannot operate with hardware alone.
  – The hardware with the suitable software can operate properly.
- To upgrade the software of the phone
  – The software of the phone may be changed to enhance the performance of the phone.
  – The older version software of the phone can be replaced to the newer version.
- Download Tools
  FlashRW : Download tool for U81X0 software

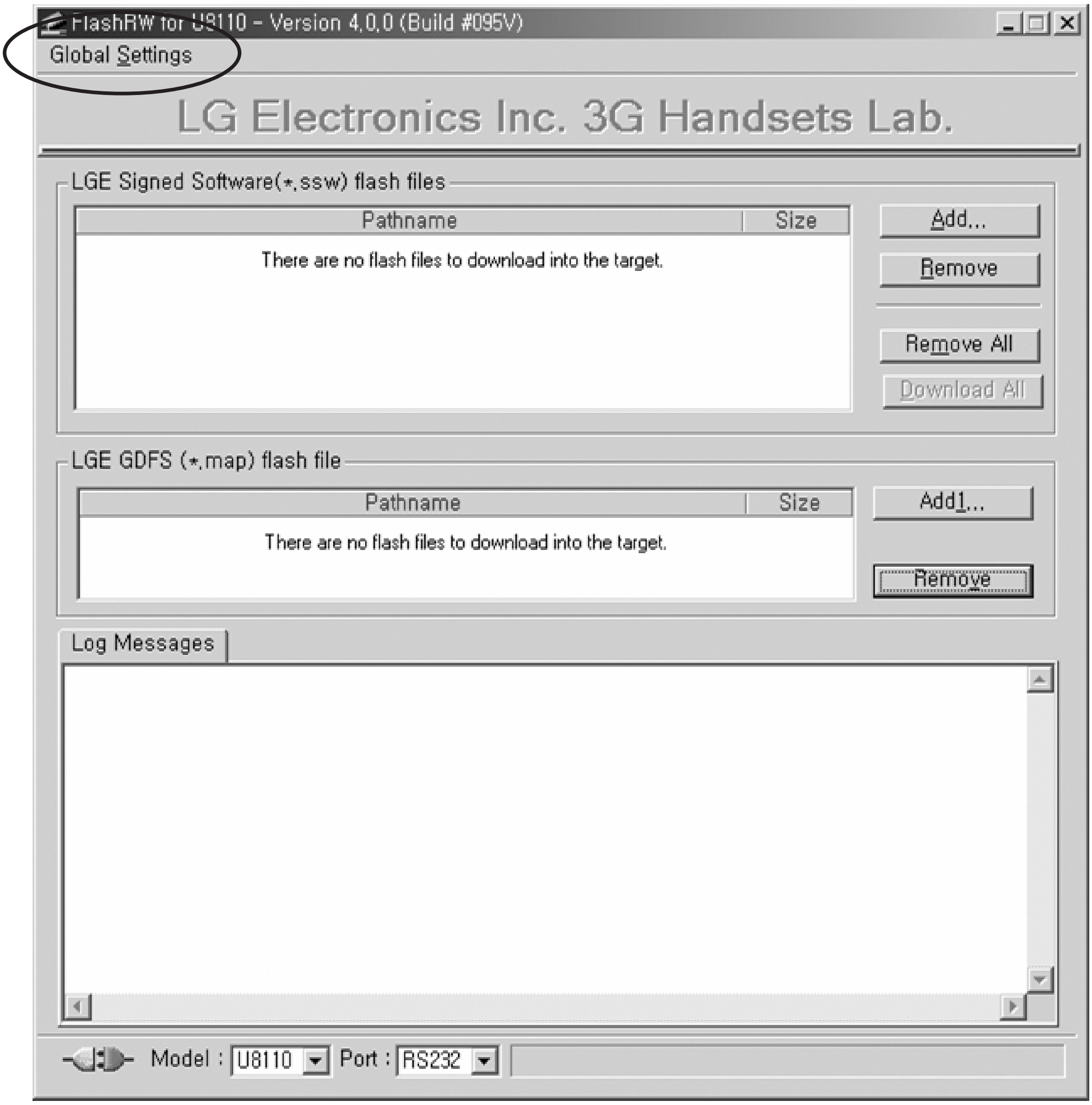
Download Environment Setup



U81X0 Download can be done via UART & USB

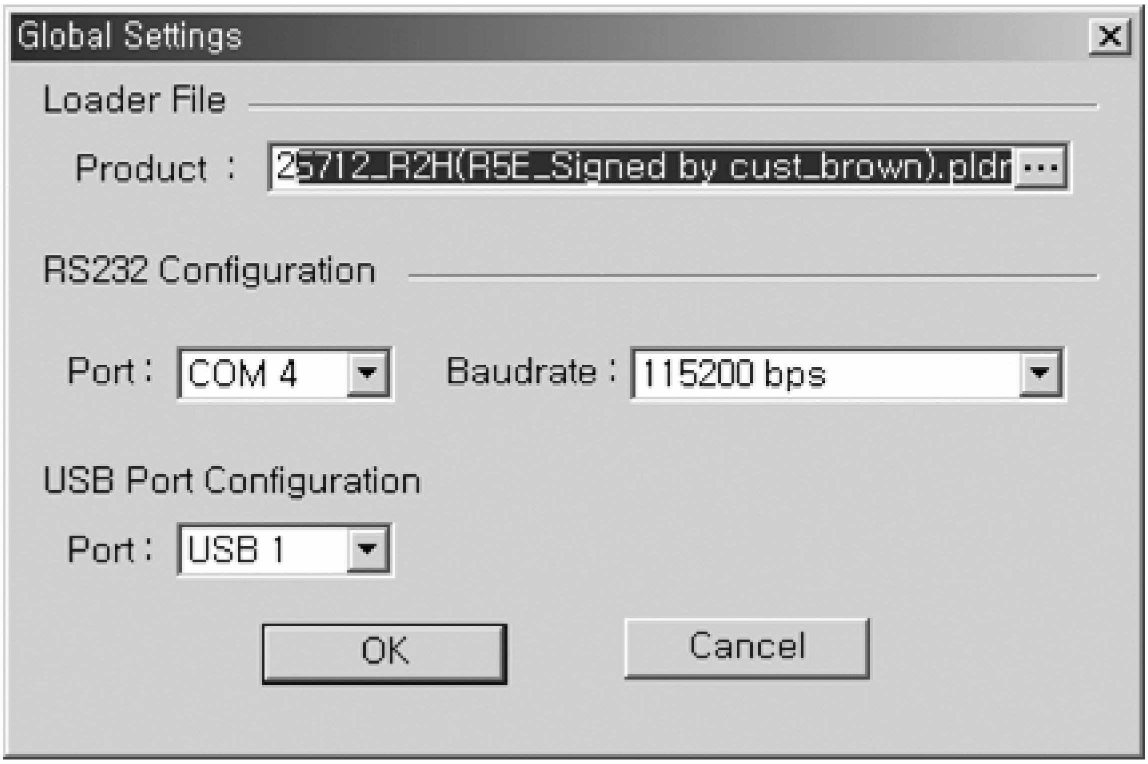
U81X0 Download (1) – FlashRW configuaration

1. Execute FLASHRW.exe.
2. Press the “Global Settings” on the top menu to configure FlashRW environment



U8110 Download (2) – FlashRW configuaration

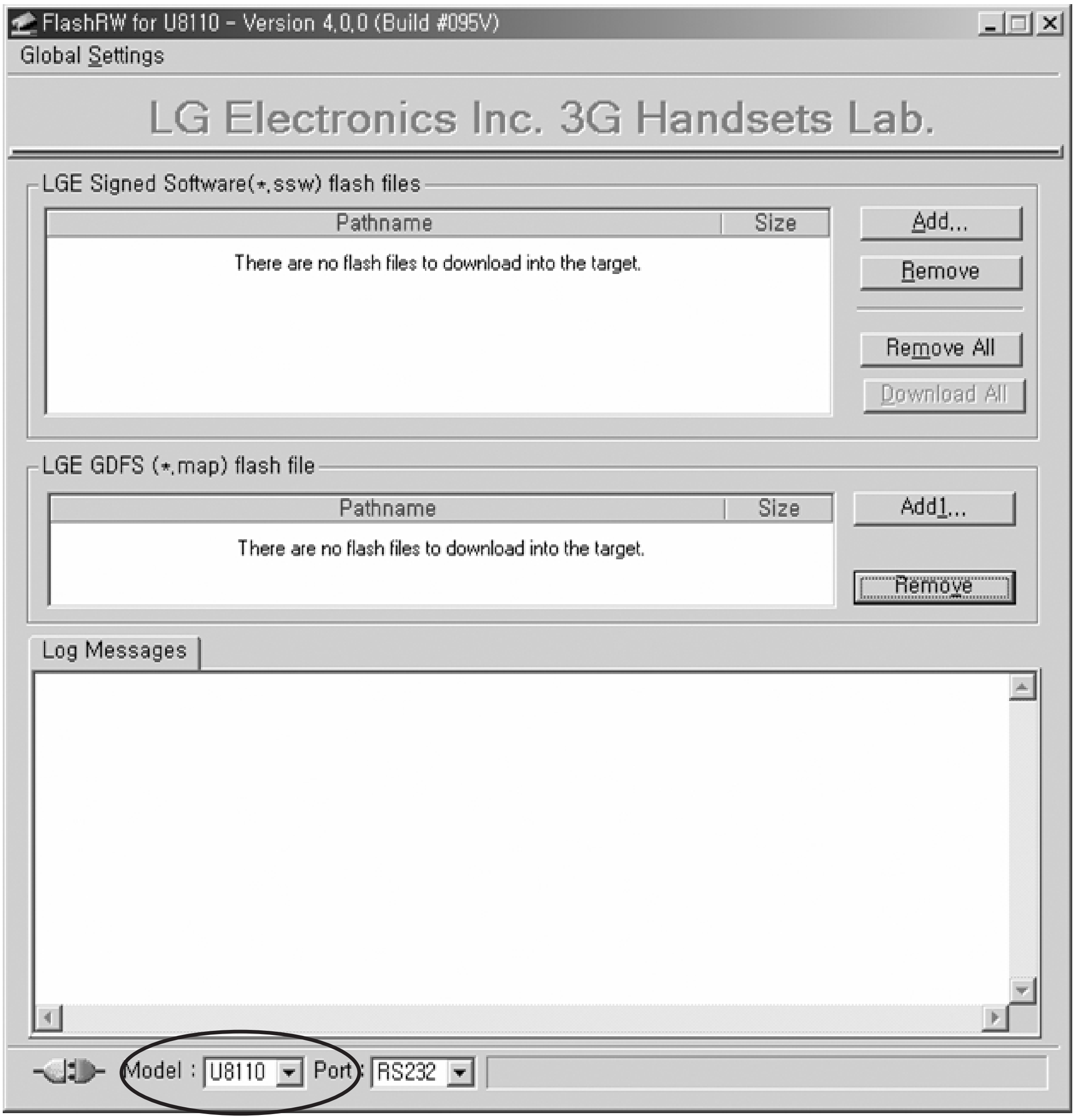
3. Select Loader File for Product.
   You can use browse button to select Loader File.
   You must select only U8120_CXC1325712_R2H(R5E_Signed by cust_brown).pldr for U8120.
   You may select any loader of 3 loaders in loader folder for U8110.
   Loader File is provided with FlashRW.
4. Select Port configurations for both RS232 Port and USB Port.
   Baudrate should be 115200bps.



You have to do FlashRW configuration only at the first time of installation

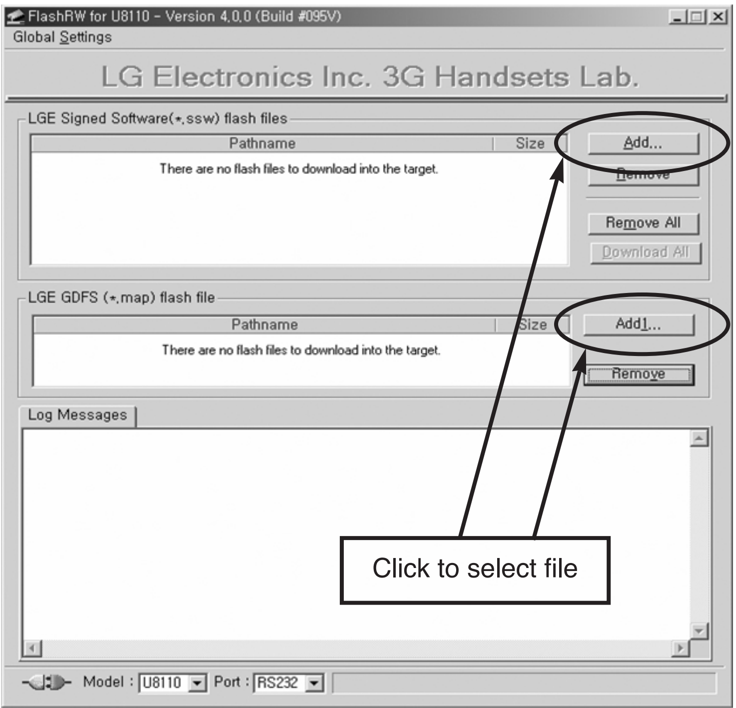
U81X0 Download (3) – Phone Model Selection

1. Press Button for Model.
2. Select Model to download images

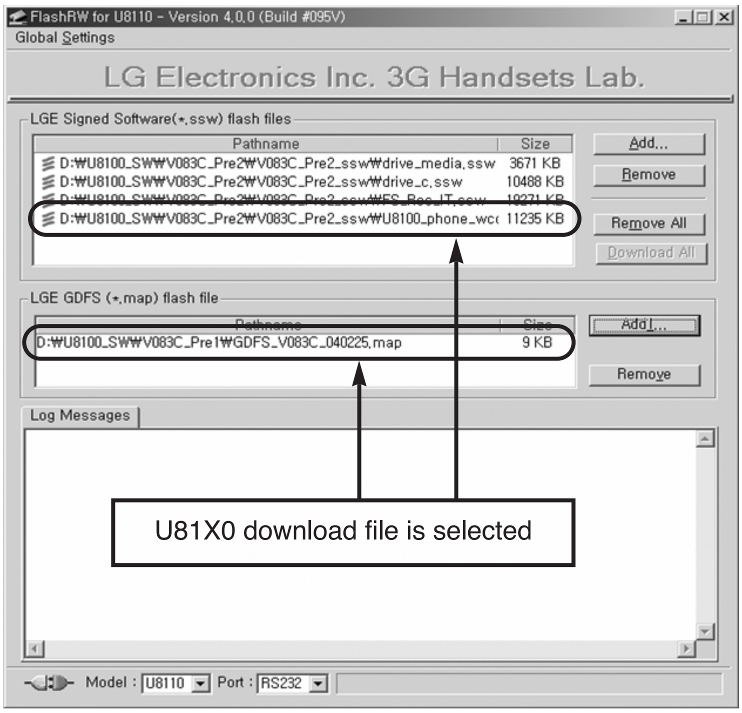


U81X0 Download (4) – Download file selection

1. Press “Add” button to select LGE SSW files to download.
2. Press “Add1” button to select LGE GDFS file to download.



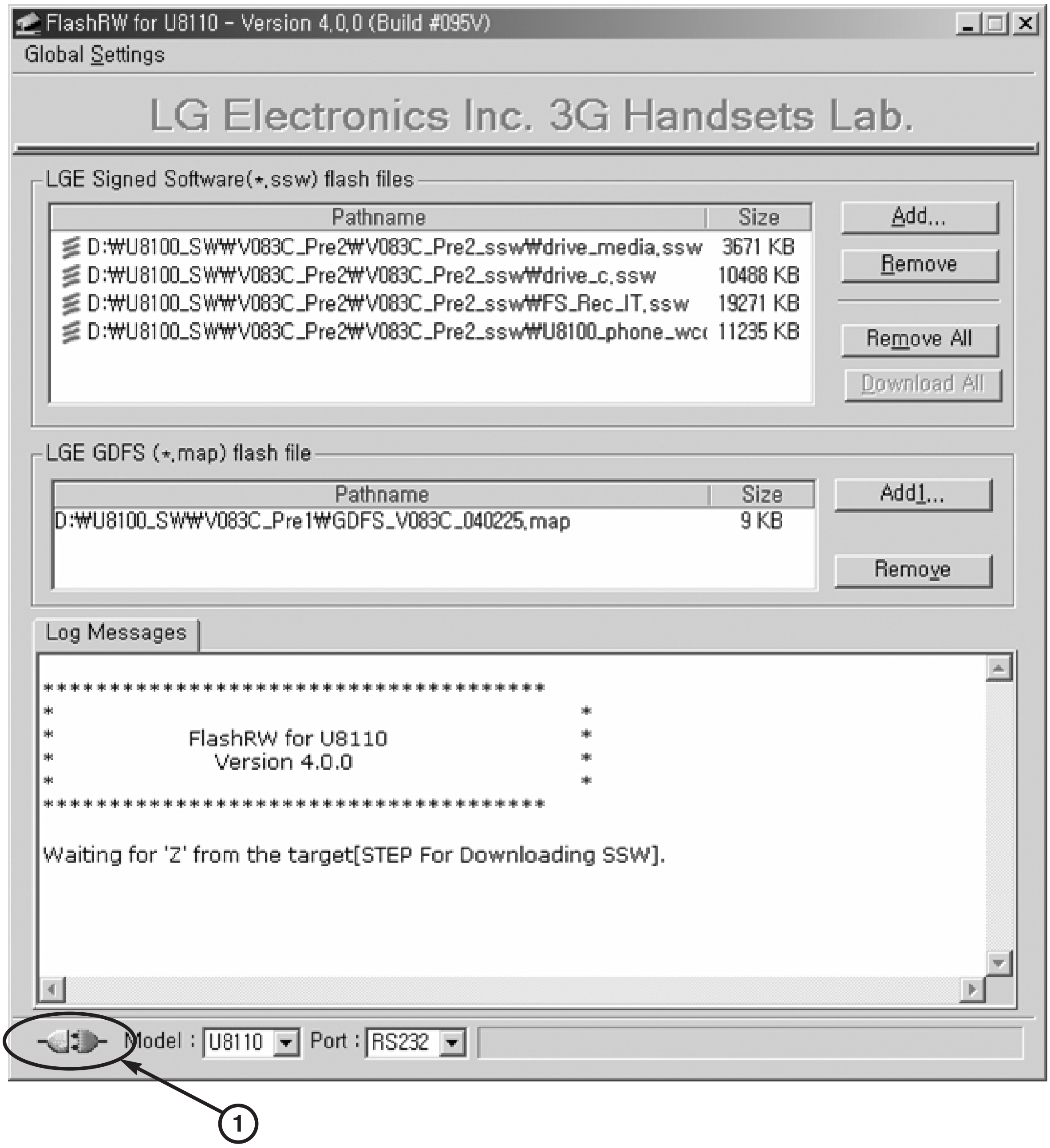
<Before Select>



<After Select>

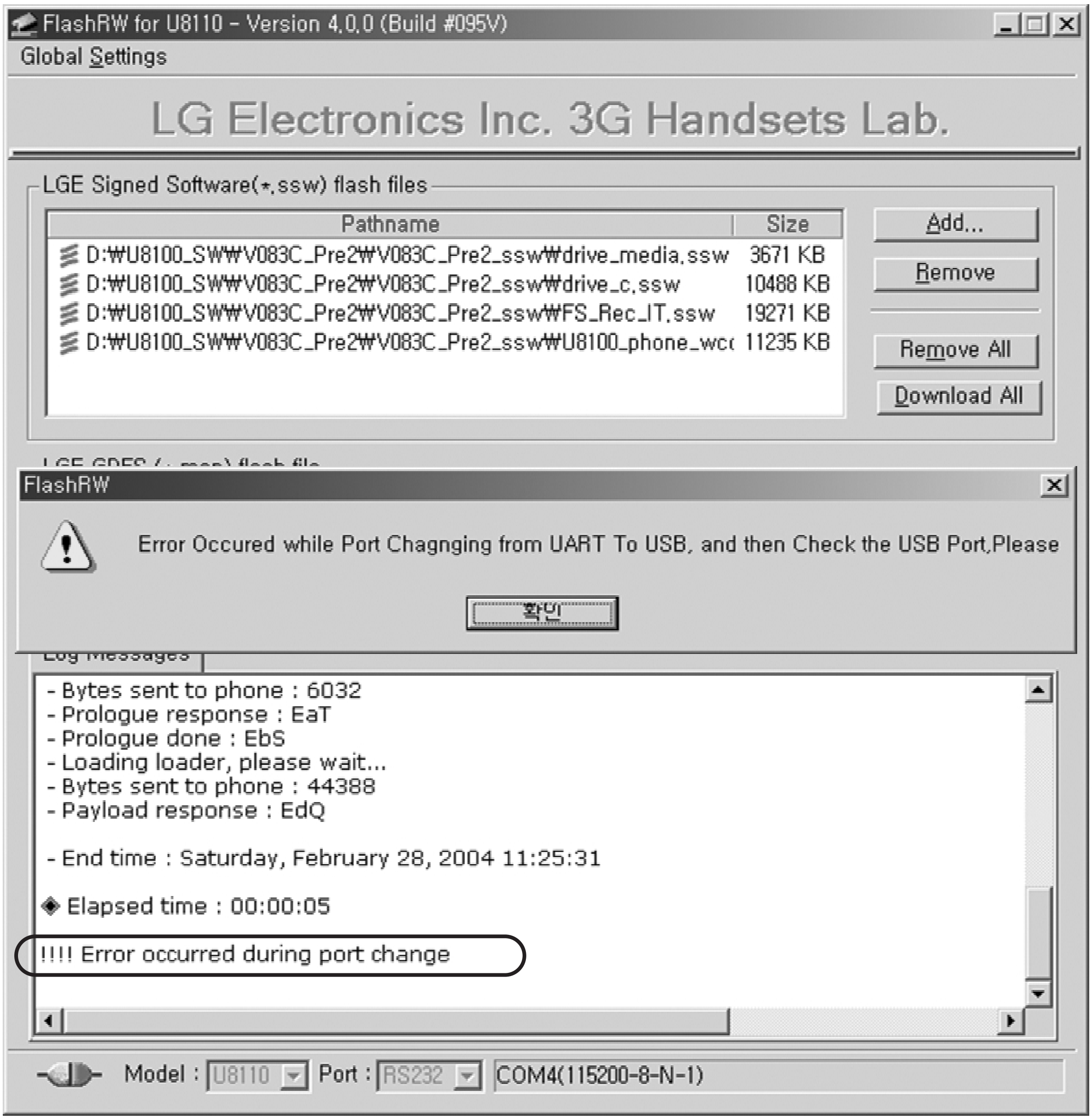
U81X0 Download (5) – Connect & Download

1. Click on connector icon ( ) to connect to the phone
   Check the Dialog Box that say “Please,switch on the target”.
2. Connect the phone to PC via Cable for Downloading.
   Phone should be turned off.
3. Turn the phone on to connect to PC.



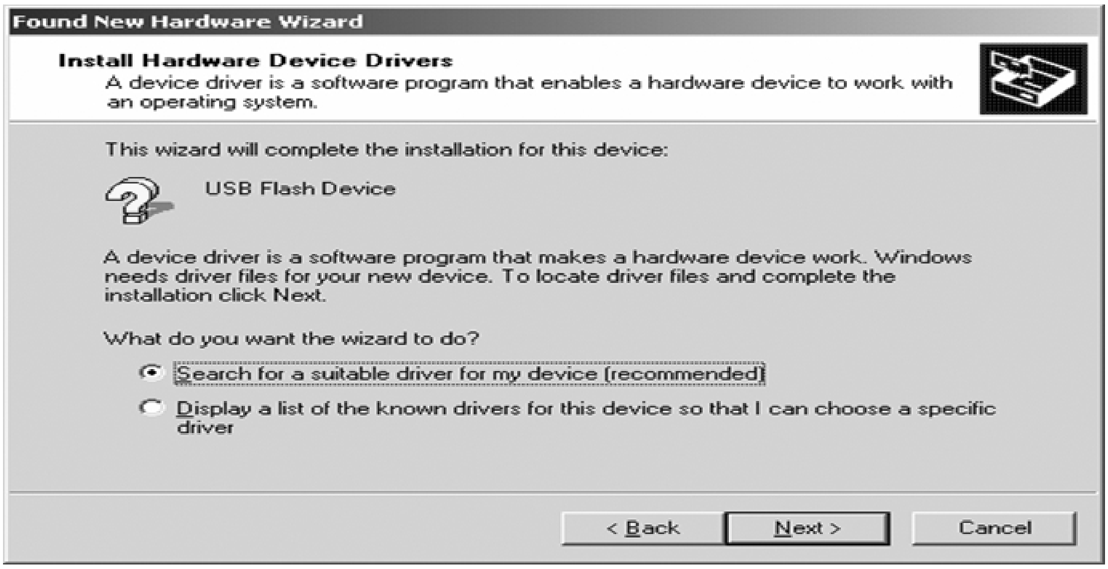
U81X0 Download (6) – USB Driver Install

1. If you use FlashRW Tool firstly, Error will happen because of USB Driver uninstalled.
   You have to do FlashRW USB Driver Installation only at the first time of installation



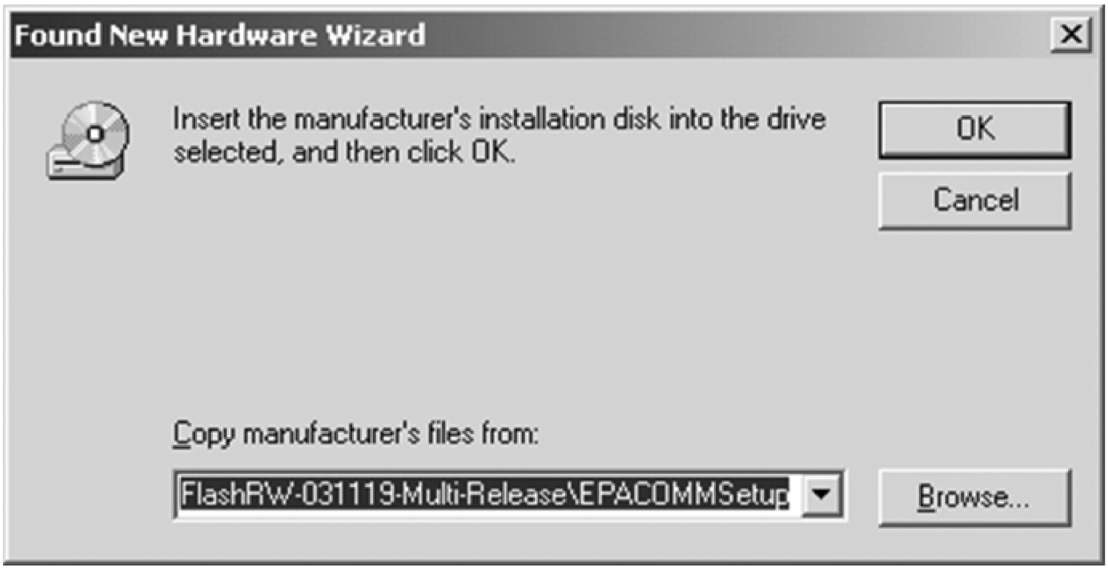
U81X0 Download (7) – USB Driver Install

2. Push “the Next Button” in Found New Hardware Wizard
3. Select “Search for a suitable driver for my device” in Found New Hardware Wizard



U81X0 Download (8) – USB Driver Install

4. Select “Specify a location” in Found New Hardware Wizard
5. Push “the Browse Button” , and then select “USB driver Information file”
   This File is provided with FlashRW.

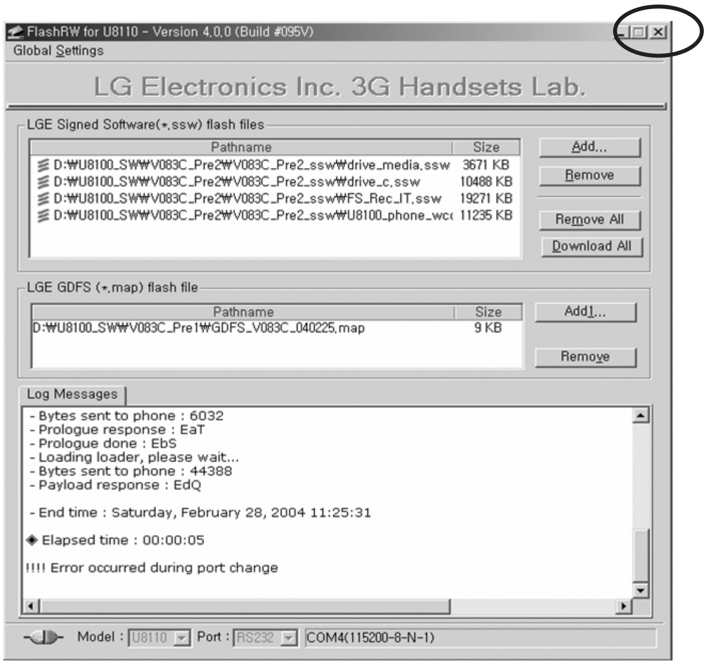


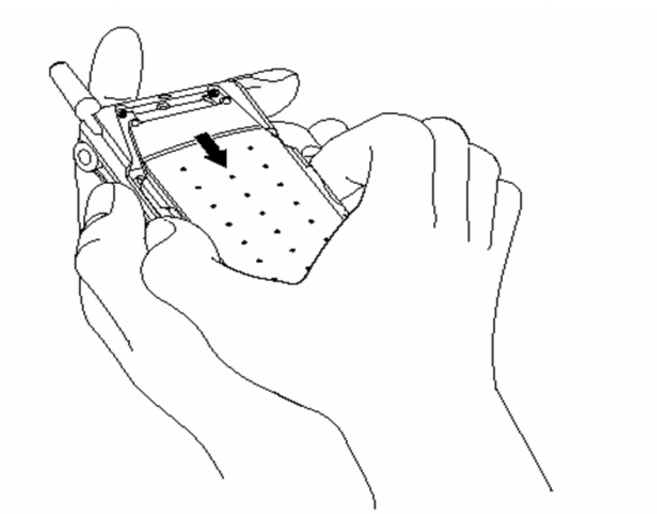
U81X0 Download (9) – USB Driver Install

6. Push “the Next Button” in Found New Hardware Wizard
7. Push “the Finish Button” in Found New Hardware Wizard

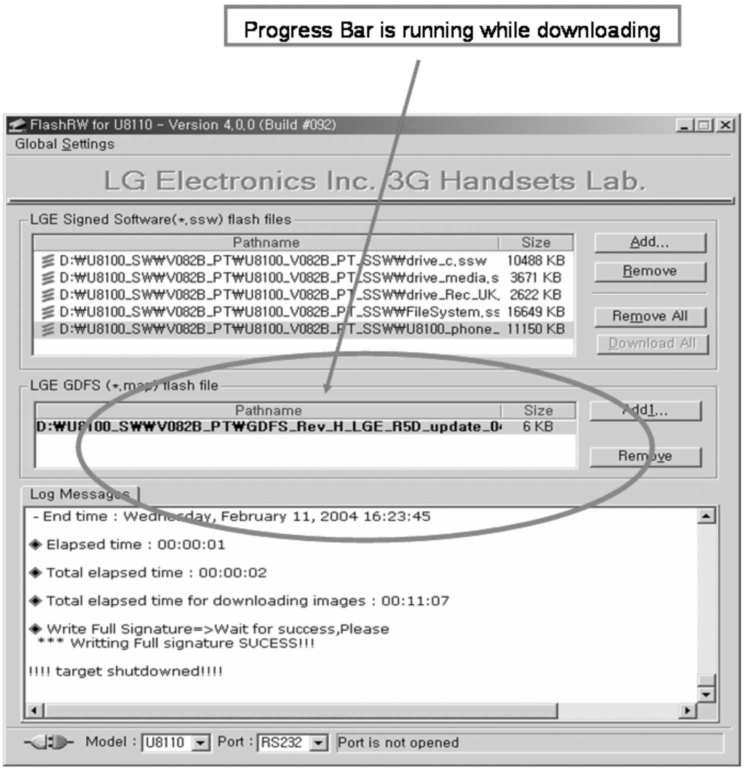
U81X0 Download (10) – USB Driver Install

8. Close FlashRW.exe
9. Remove & Insert Main battery to reset the phone
   % This action for USB Driver Install is done only at the first time of installation
   If you want to download Software, just do as same as U81X0 Download (5) – Connect & Download says

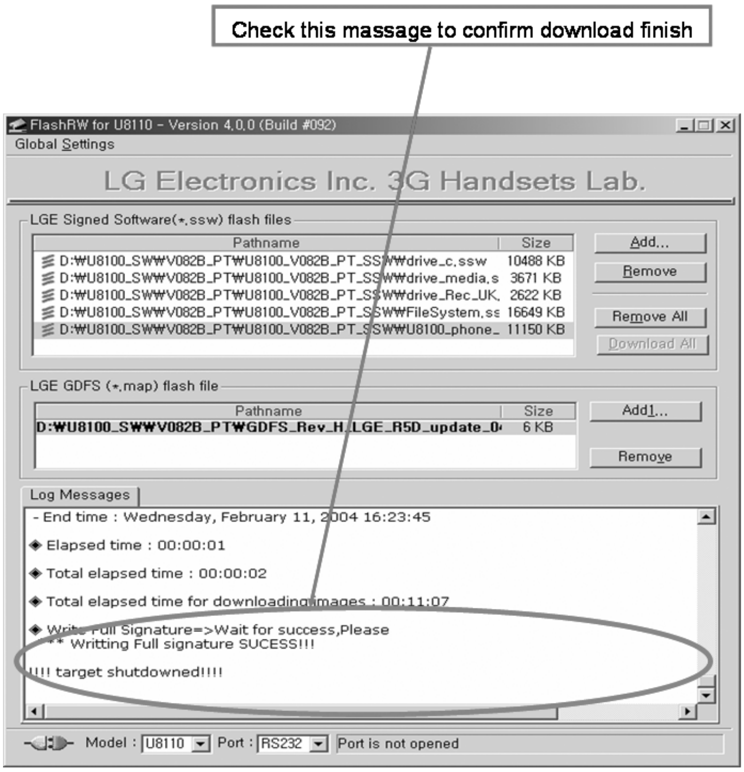




U81X0 Download (11) – Connect & Download



< While Downloading >



< After Downloading finished >

U81X0 Download (12) - Trouble shooting

• Check these questions when trouble happens.

1. Check if UART & USB Port configuration is right.
2. Do not change RS-232 baud rate(115200BPS). It is fixed and never changed.
3. Check if UART & USB Cable is connected.

8. CALIBRATION

8.1 General Description

This document describes the construction and the usage of the software used for the calibration of LG's GSM/GPRS/WCDMA Multimedia Mobile Phone (U8110). The calibration menu and their results are displayed in PC terminal by Mobile phone.
This calibration software includes GSM, DCS, WCDMA Band RF partscalibration and Battery calibration. This calibration software was called "XCALMON(eXtended CALibration and MONitor program)". From now on, the calibration software will be called XCALMON in this document.

8.2 XCALMON Environment

8.2.1 H/W Environment

- PC with RS-232 Interface & GPIB card installed
- GSM/GPRS/WCDMA Multimedia Mobile Set (U8110)
- Agilent 8960 Series 10 E5515C Instrument (E1985B ver04.08)
- Tektronix PS2521G Power Supply
- ETC (GPIB cable, Serial cable, RF cable, Power cable, Dummy battery)

8.2.2 S/W Environment

- National Instrument GPIB &VISA (ver 2.60 full)driver install
- Agilent 8960 VXI driver(E1960)install
- XCALMON EXE files
- OS :Window98,Window2000,WindowXP
- Serial port configuration :
  Baud rate:115200 /Char length:8bit /No Parity/No Flow control
  Stop bits:1 bit

8.2.3 Configuration Diagram of Calibration Environment

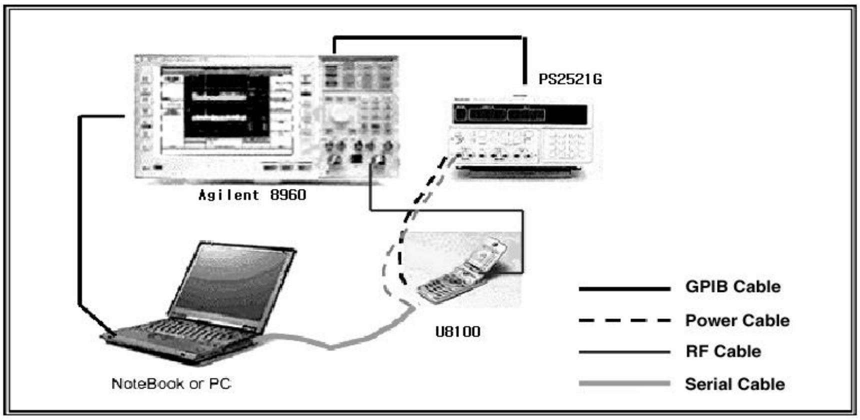


Figure 8-1. Calibration Configuration Figure

8.3 Calibration Explanation

8.3.1 Overview

In this section,it is explained each calibration item in the XCALMON.Also the explanation includes technical information such as basic formula of calibration and settings for key parameters in each calibration procedure.
At first,when any of calibration is done,the results are displayed in the XCALMON result window and the result of calibration will be stored in GDFS(Global Data Flash Storage).

8.3.2 Calibration Items

A. EGSM 900 Band

- MODA-D(MD bit)Delay Calibration
- RXVCO Varactor Operating Point Calibration
- TXVCO Varactor Operating Point Calibration
- TX Loop Bandwidth Calibration
- VCXO Calibration
- TX Power Calibration
- RSSI and AGC Calibration

B. DCS 1800 Band

- RXVCO Varactor Operating Point Calibration
- TXVCO Varactor Operating Point Calibration
- TX Loop Bandwidth Calibration
- TX Power Calibration
- RSSI Cal i br at i on

C. WCDMA Band

- RF VCO Center Frequency Calibration
- TX Carrier Suppression Calibration
- TX LPF Bandwidth Calibration
- TX Maximum Output Power Calibration
- TX Power Table Calibration
- TX Open Loop Power Control Calibration
- RX LPF Bandwidth Calibration
- RX LNA Gain Switch and AGC Hysteresis Calibration
- RX AGC Gain Max and Rx RSSI Calibration

8.3.3 EGSM 900 Calibration Items

A. MOD-A(MD bit) Delay Calibration

- Pur pose

The procedure is designed to calibrate the timing alignment between the MODA-D signals and the reference signal (13 MHz).It also ensures that the MOD signals have stable values when they are clocked into the divider of the Phase-Locked Loop (PLL).

- Procedure Proposal

1. Set the ME to mid channel in the GSM TX band.
2. Set the delay setting in default mode,that is,no delay.
3. Wait approximately 300 us to 400 us to allow the PLL to lock.
4. Measure the RMS phase error.A threshold value of >20 deg indicates that the PLL is running in the forbidden time region.
5. Save the RMS phase error result locally.
6. Step up the delay setting according to Table 8.1 below.
7. Repeat from step 4.
8. Choose delay setting that gives maximum distance to the consecutive field of corrupted RMS phase error values in the vector.
9. Store delay setting both to the GD_RF_Mod_Delay and to the GD_DirMod_Mod_Delay.
10. Reset the radio.

Index	DIMC	MD
[0]	0	00(0)
[1]	0	01(1)
[2]	0	10(2)
[3]	0	11(3)
[4]	1	00(0)
[5]	1	01(1)
[6]	1	10(2)
[7]	1	11(3)

Table 8-1. Delay Settings for the MOD-A

B. RXVCO Varactor Operating Point Calibration

- Pur pose

To adjust the varactor diode to a pre-determined operating point,so that the loop voltage of the RXVCO (measured with an ADC in AB 2000) is within the valid range. This is necessary to secure that all RX channels can be reached.

- Procedure Proposal

1. Put the ME in static RX mode.
2. Measure the loop voltage with the AB 2000 ADC for all CVCO settings, that is, 0 ~7.
   Find a CVCO value that fulfills the requirements on loop voltage for low and high channel.
3. If there are several CVCO values that fulfill the loop voltage requirements,then the optimum CVCO value is the one that centers the loop voltage within the specified limits.
4. Store the selected CVCO in the memory.
   (GD_RX_VCO_Centre_Frequency_Adjustment_Band)
5. Reset the radio.

C. TXVCO Varactor Operating Point Calibration

- Pur pose

To adjust the varactor diode to a pre-determined operating point,so that the loop voltage of the TXVCO (measured with an ADC in AB 2000) is within the valid range. This is necessary to secure that all TX channels can be reached.

- Procedure Proposal

1. Put the phone in static TX mode.
2. Measure the loop voltage with the AB 2000 ADC for all CVCO settings, that is, 0 ~7.
   Find a CVCO value that fulfills the requirements on loop voltage for low and high channel.
3. If there are several CVCO values that fulfill the loop voltage requirements,then the optimum CVCO value is the one that centers the loop voltage within the specified limits.
4. Store the selected CVCO in the memory.
   (GD_TX_VCO_Centre_Frequency_Adjustment_Band)
5. Reset the radio.

D. TX Loop Bandwidth Calibration

- Pur pose

The loop bandwidth is calibrated to match the pre-filtering of the modulation in DB 2000 by adjusting the phase detector current.

Note:This also indirectly adjusts the VCO gain that can otherwise not be calibrated.

This will ensure a correct transfer function for the modulation and keep phase error to a minimum.

- Procedure Proposal
1. Put the ME in switched TX mode on mid channel in frequency interval 11 for EGSM (with random modulation).
2. Measure the RMS phase error at the RF connector.
3. Tune the phase detector current (IPHD)until the phase error is minimized.If two IPHD settings gave the same RMS,choose the lowest value.Measure 10 bursts for each value.
4. Calculate and store the IPHD values in GDFS (GD_IPHD_8Temperature_and_24Channel_Compensation_Band)
5. The offsets in the table are steps in the IPHD Table 8.2 and all offsets refer to the calibrated value (Trim) at mid channel in room temperature.

Frequency Interval																								
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
0	-2	-2	-2	-2	-1	-1	-1	-1	-1	0	0	0	0	0	1	1	1	1	1	1	2	2	2	2
1	-2	-2	-2	-2	-1	-1	-1	-1	-1	0	0	0	0	0	1	1	1	1	1	1	2	2	2	2
2	-2	-2	-2	-2	-1	-1	-1	-1	-1	0	0	0	0	0	1	1	1	1	1	1	2	2	2	2
3	-2	-2	-2	-2	-1	-1	-1	-1	-1	0	0	0	0	0	1	1	1	1	1	1	2	2	2	2
4	-2	-2	-2	-2	-1	-1	-1	-1	-1	0	0	0	0	0	1	1	1	1	1	1	2	2	2	2
5	-2	-2	-2	-2	-1	-1	-1	-1	-1	0	0	0	0	0	1	1	1	1	1	1	2	2	2	2
6	-2	-2	-2	-2	-1	-1	-1	-1	-1	0	0	0	0	0	1	1	1	1	1	1	2	2	2	2
7	-2	-2	-2	-2	-1	-1	-1	-1	-1	0	0	0	0	0	1	1	1	1	1	1	2	2	2	2

Table 8-2. IPHD Compensation for EGSM Band

E. VCXO Calibration

- Pur pose

This procedure aims to calibrate the value of DAC3 to establish a VCXO-frequency that is sufficiently close to 13 MHz at room temperature.It also ensures that the VCXO tuning range is sufficient,and that the temperature compensation table for VCXO is completed accordingly.

Note:The frequencies in this section are related to the 13 MHz VCXO-frequency.

Depending on the calibration procedure,the 13 MHz VCXO frequency can be acquired by first measuring an EGSM,DCS,or W-CDMA RF frequency at the antenna and then translating the measured frequency to the 13 MHz VCXO frequency.

- Procedure Proposal
1. Put the ME in switched low power TX mode with a modulated carrier on a mid channel. Use the calibrated value of the cap array and phase detector current.
2. Tune DAC3 in AB 2000 (VCXOCONT)to end and mid values,and check tuning range.

Acquire the following VCXO (13 MHz)frequencies:

fmin =13 MHz VCXO-frequency @DAC3=1

fmid =13 MHz VCXO-frequency @DAC3=1024

fmax =13 MHz VCXO-frequency @DAC3=2047

Note that it is necessary to translate the measured RF-frequency (EGSM,DCS,or W- CDMA)to the 13 MHz VCXO-frequency.

3. Acquire the ME temperature,TCal,from the temperature sensor in ME.
4. Store fmin,fmid,fmax and TCal for calculation.
5. Calculate the DAC-value,VCXOCONTCal,that gives zero frequency error at the mid channel, using piecewise linear interpolation,and store the value in the memory (GD_RF_SYNT_CONFIG_ID and GD_VCXO)
6. Calculate

K_LO =(fmid –fmin)/1023

K_HI =(fmax –fmid)/1023

Each value is then multiplied by 100 and rounded to nearest integer, with the results stored in the memory (GD_RF_SYNT_CONFIG_ID).

AFC_DAC_STEP_LO =ROUND(100*K_LO)

AFC_DAC_STEP_HI =ROUND(100*K_HI)

where ROUND(x)=x rounded to the nearest integer.

F. TX Power Calibration

- Pur pose

These procedures describe how to tune the different power levels of the power amplifier to output powers corresponding to values in GSM 05.05,and explain how to calculate intermediate power levels that will ensure a good power versus time performance.

- Procedure Proposal

1. Reset the DIRMOD-block, and select a, mid channel using the trimmed value on the capacity array for VCO tuning and a default IPHD value as phase detector current. Turn on dummy burst modulation.
2. Use the Multi-burst method to characterize the relation between output power and the DAC-value.Then store the DAC values that give the closest approximations to the power targets defined in Table 8-3.
3. To avoid yield problems with the power template and switching transients spectrum a margin to the compression point of the PA should be observed.However,the output power must be kept within the tolerances specified in Table 8-3.
4. Store DAC values in memory (GD_FullPower_Band).
5. Initiate the intermediate value calculation,which calculatesand st or e t he val ues in memory (GD_IntermediatePower_Up/Down_1.7_Band).
6. The difference between the transmitter power at two adjacent power control levels, measured at the same frequency,shall not be less than 0.5 dB and not more than 3.5 dB.

Parameter	Target Full Power (dBm)	Tolerances (dB)	
PL 5	33.0	+0.5 – 1.0	Vol
PL 6	31.0	±0.3	Vol
PL 7	29.0	±0.5	Vol
PL 8	27.0	±0.5	Vol
PL 9	25.0	±0.5	Vol
PL 10	23.0	±0.5	Vol
PL 11	21.0	±0.5	Vol
PL 12	19.0	±0.5	Vol
PL 13	17.0	±0.5	Vol
PL 14	15.0	±0.5	Vol
PL 15	13.0	±0.5	Vol
PL 16	11.0	±0.5	Vol
PL 17	9.0	±0.5	Vol
PL 18	7.0	±0.5	Vol
PL 19	5.0	±0.5	Vol

Table 8-3. Target Power Levels for EGSM

G. RSSI and AGC Calibration

- Purpose

This procedure satisfies the two following requirements:

Calibrate an absolute power level on the antenna to a corresponding RSSI value. This value together with a pre-defined slope figure is then used to calculate the RSSI value of an arbitrary received antenna power. The formula y=kx+m is used. (Where k is the slope value, x the RSSI value, y the actual level, and m is an offset value.)

Calculate the attenuation when the Low Noise Amplifier is switched off in the receiver branch. The attenuation value is stored in the flash memory and used when very high input signals are fed into the ME.

- Procedure Proposal

1. Select switched receiver on a mid EGSM Channel.
2. Feed a modulated -68.5dBmsignal, on the same mid EGSM-Channel to the antenna input. Measure the RSSI value, calculate the RSSI table and store the value in GDFS as parameter: GD_RXLEVS_DBM_BURST_M_BAND.
3. On the same channel, now feed a modulated -50dBmsignal and measure the RSSI value.

4. Switch off the LNA, using the command FREC=3,0,1, and measure the RSSI value.
5. Calculate the difference between on and off (converting the result to, real dB attenuation) and store the result in GD_MPH_RX_AGC_Parameters_Band.

8.3.4 DCS 1800 Calibration Items

A. RXVCO Varactor Operating Point Calibration

- Purpose

To adjust thevaractordiode to a pre-determined operating point, so that the loop voltage of the RXVCO (measured with an ADC in AB 2000) is withinthe valid range. This is necessary to secure that all RX channels can be reached.

- Procedure Proposal

1. Put the ME in static RX mode.
2. Measure the loop voltage with the AB 2000 ADC for all CVCO settings, that is, 0 ~ 7. Find a CVCO value that fulfills the requirements on loop voltagefor low and high channel.
3. If there are several CVCO values that fulfill the loop voltage requirements, then the optimum CVCO value is the one that centers the loop voltage within the specified limits.
4. Store the selected CVCO in the memory. (GD_BAND_RX_VCO_Centre_Frequency_Adjustment)
5. Reset the radio.

B. TXVCO Varactor Operating Point Calibration

- Purpose

To adjust thevaractordiode to a pre-determined operating point, so that the loop voltage of the TXVCO (measured with an ADC in AB 2000) is withinthe valid range. This is necessary to secure that all TX channels can be reached.

- Procedure Proposal

1. Put the phone in static TX mode.
2. Measure the loop voltage with the AB 2000 ADC for all CVCO settings, that is, 0 ~ 7. Find a CVCO value that fulfills the requirements on loop voltagefor low and high channel.
3. If there are several CVCO values that fulfill the loop voltage requirements, then the optimum CVCO value is the one that centers the loop voltage within the specified limits.
4. Store the selected CVCO in the memory. (GD_BAND_TX_VCO_Centre_Frequency_Adjustment)
5. Reset the radio.

C. TX Loop Bandwidth Calibration

- Purpose

The loop bandwidth is calibrated to match the pre-filtering of the modulation in DB 2000 by adjusting the phase detector current.

Note: This also indirectly adjusts the VCO gain that can otherwise notbe calibrated.

This will ensure a correct transfer function for the modulation and keep phase error to a minimum.

- Procedure Proposal
1. Put the ME in switched TX mode on mid channel in frequency interval 11 for DCS (with random modulation).
2. Measure the RMS phase error at the RF connector.
3. Tune the phase detector current (IPHD) until the phase error is minimized. If two IPHD settings gave the same RMS, choose the lowest value. Measure 10 bursts for each value.
4. Calculate and store the IPHD values in GDFS (GD_IPHD_8Temperature_and_24Channel_Compensation_Band)
5. The offsets in the table are steps in the IPHD Table 8.4 andall offsets refer to the calibrated value (Trim) at mid channel in room temperature.

Frequency Interval																								
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
0	-6	-6	-5	-4	-4	-3	-3	-2	-2	-1	-1	0	0	1	1	2	2	3	3	4	4	5	5	5
1	-6	-6	-5	-4	-4	-3	-3	-2	-2	-1	-1	0	0	1	1	2	2	3	3	4	4	5	5	5
2	-6	-6	-5	-4	-4	-3	-3	-2	-2	-1	-1	0	0	1	1	2	2	3	3	4	4	5	5	5
3	-6	-6	-5	-4	-4	-3	-3	-2	-2	-1	-1	0	0	1	1	2	2	3	3	4	4	5	5	5
4	-6	-6	-5	-4	-4	-3	-3	-2	-2	-1	-1	0	0	1	1	2	2	3	3	4	4	5	5	5
5	-6	-6	-5	-4	-4	-3	-3	-2	-2	-1	-1	0	0	1	1	2	2	3	3	4	4	5	5	5
6	-6	-6	-5	-4	-4	-3	-3	-2	-2	-1	-1	0	0	1	1	2	2	3	3	4	4	5	5	5
7	-6	-6	-5	-4	-4	-3	-3	-2	-2	-1	-1	0	0	1	1	2	2	3	3	4	4	5	5	5

Table 8-4. IPHD Compensation for DCS Band

D. TX Power Calibration

- Purpose

To tune the different DCS power levels of the power amplifier tooutput powers corresponding to values in GSM 05.05 and calculate the intermediate levels that ensure a good power versus time performance.

- Procedure Proposal
1. Reset the DIRMOD-block, and select a ,mid channel using the trimmed value on the capacity array for VCO tuning and a default IPHD value as phase detector current. Turn on dummy burst modulation.
2. Use the Multi-burst method to characterize the relation between output power and the DAC-value. Then store the DAC values that give the closest approximations to the power targets defined in Table 8-5.

3. To avoid yield problems with the power template and switchingtransients spectrum a margin to the compression point of the PA should be observed. However, the output power must be kept within the tolerances specified in Table 8-5.
4. Store DAC values in memory (GD_FullPower_Band).
5. Initiate the intermediate value calculation, which calculatesand store the values in memory (GD_IntermediatePower_Up/Down_1.7_Band).
6. The difference between the transmitter power at two adjacent power control levels, measured at the same frequency, shall not be less than 0.5 dB and not more than 3.5 dB.

Parameter	Target Full Power (dBm)	Tolerances (dB)	
PL 0	30.0	+0.5 – 1.0	Vol
PL 1	28.0	±0.3	Vol
PL 2	26.0	±0.5	Vol
PL 3	24.0	±0.5	Vol
PL 4	22.0	±0.5	Vol
PL 5	20.0	±0.5	Vol
PL 6	18.0	±0.5	Vol
PL 7	16.0	±0.5	Vol
PL 8	14.0	±0.5	Vol
PL 9	12.0	±0.5	Vol
PL 10	10.0	±0.5	Vol
PL 11	8.0	±0.5	Vol
PL 12	6.0	±0.5	Vol
PL 13	4.0	±0.5	Vol
PL 14	2.0	±0.5	Vol
PL 15	0.0	±1	Vol

Table 8-5.Target Power Levels for DCS

E. RSSI Calibration

- Purpose

This procedure calibrates an absolute power level on the antennaagainst a corresponding RSSI value. This value together with a pre-defined slope figure is then used to calculate the RSSI value of an arbitrary received antenna power. The formula y=kx+m is used. (Where k is the slope value, x the RSSI value, y the actual level, and m is an offset value).

- Procedure Proposal

1. Select switched receiver on a mid DCS-Channel.
2. Feed a modulated -68.5dBmsignal, on the same mid DCS Channel to the antenna input. Measure the RSSI value, calculate the RSSI table, and store it to the memory (GD_BAND_RXLEVS_DBM_BURST_M[2]) –1 byte.

8.3.5 WCDMA Calibration Items

A. RF VCO Center Frequency Calibration

- Purpose

This procedure is designed to calibrate the RFVCO (Radio Frequency Voltage Controlled Oscillator) center frequency of the Ericsson RF 2110 (hereafter referred to as the RF 2100) and ensure that all channels can be reached with sufficient margin.

The objective of the calibration is to determine a CVCO (Center VCO) value that guarantees the functionality of the RFLO (Radio Frequency Local Oscillator).

- Procedure Proposal

1. Start the VCXO and RFVCO. VCXOCONT is set to its calibrated value, Ericsson AB 2000 DAC3.
2. Measure the loop voltage (WRFLOOP), with the AB 2000 ADC (GPA4), for all CVCO settings, that is, 0-7. Find a CVCO value that fulfills the requirements on loop voltage for low and high channel. If there are several CVCO values that fulfill the loop voltage requirements, then the optimum CVCO value is that that centers the loop voltage within the specified limits.
3. Store the calibrated CVCO value in GD_RF_SYNT_CONFIG_ID.

B. TX Carrier Suppression Calibration

- Purpose

DC offset compensation the carrier, to the wanted signal at the IQ-modulator output.

The leakage is caused by imperfections in the basebandIQ-path and inside the IQ-modulator. It impairs the modulation accuracy and results in a high vector magnitude (EVM). The outcome of the calibration is values for RECDCI and RECDCQ that minimize the carrier.

- Procedure Proposal

1. Set the ME in TX mode on mid-channel. Use typical TX settings. Generate 960 kHz square-wave on both I and Q with amplitude = 8 (sine-wave could be used instead).
   Start with the best value from earlier calibrated units on RECDCI on RECDCQ.

2. Measure the relative power between the 1950 MHz carrier and 1949.04 MHz at the antenna output. Jump to step 6 if the requirement is met.
3. Step RECDCI from 0 to 3. Set TXON = 0 and wait 1 ms before changing RECDCI from 3 to 5. Set TXON = 1, wait 1 ms and continue with stepping from 5 to 7.
4. Set RECDCI to the value that minimizes the 1950 MHz carrier. If this involves a change of sign the TXON switching and delay sequence in point 3 must beexecuted. Jump to 6 if the requirement is met.
5. Find and set RECDCQ to the value that minimizes the 1950 MHz carrier. This can be made by stepping RECDCQ from 0 to 7 with the TXON switching and delay sequence in step 3.
6. If the requirements are not met, repeat steps 3, 4 and, if necessary, 5 once with the new RECDCI and RECDCQ (found in 4 and 5) as initial values. Otherwise proceed with step 6.
7. Save the finaldBcvalue (for statistics), RECDCI and RECDCQ. Store the calibrated parameters in GD_RF_TX_CONFIG_ID.

C. TX LPF Bandwidth Calibration

- Purpose

The low pass filters within the Ericsson DB 2100 (hereafter referred to as DB 2100) are designed to prevent spurious emissions output from the TX IQ-D/A (Digital-Analog) converters Œ without adversely affecting the signal or causing a deterioration of the modulation accuracy.

The objective of this calibration is to determine the values forLPQ and LPBW that offer the best trade off against the system-related requirements. These settings determine the cut-off frequency and should always have the same value.

- Procedure Proposal

1. Use typical TX settings. Generate a 960 kHz square-wave at baseband without phase shift between I and Q. The amplitude should be about 50% of fullscale.
2. Measure the relative power between 1952.88 MHz (fc+ 3*960 kHz) and 1949.04 MHz (fc Œ 960 kHz) in dB at the antenna output. Find the setting of LPQ =LPBW between 3 and 15 that obtains the dBcvalue closest to the typical value. Start with the best value from earlier calibrated units. Spectrum analyzer settings (example):
   RBW = 300 kHz, Span = 8 MHz.
3. Set LPQ=LPBW to the found value in 2. Also save thedBcand the decided LPQ = LPBW value for statistics. Store the calibrated parameters in GD_RF_TX_CONFIG_ID.

D. TX Maximum Output Power Calibration

- Purpose

These procedures verify that the ME can meet the requirements onmaximum output power. The calibration aims to establishWPABias, VGA and QVGA settings that fulfill ACLR requirements for maximum output power, both in high, medium, and low gain mode.

These calibrations are designed to conform to the ME maximum output power and ACLR requirements specified in 3GPP Spec TS34.121.

- Procedure Proposal

1. Use typical TX settings, mid channel.
2. Set gain to the best value based upon previous calibrated units.

3. Measure output power as broadband power.
4. If the ACLR requirements, described in Table 11 are not met, calculate the test step necessary to achieve the correct power. Use correlation from earlier calibrated units to calculate the new gain setting (default correlation between VGA and output power is 1 dB and for QVGA 0.25dB).
5. Measure ACLR at this power level.
6. If the ACLR requirement is not met, reduce VGA and QVGA.
7. Measure and store the temperature at this point. This provides the value forTPmax.
8. This power and gain setting is to be used in calibration of TX power table.
9. Set gain to maximum power in medium gain mode and measure ACLR at this power level.RFBiasshould be set to 1 andWPABiasshould be set to the same value as for maximum output power.
10. If the requirements are not met, step the gain down and measure ACLR until the requirements are met. The correlation between ACLR and output power is that 1 dB in power equals typical 3 dB in ACLR. Use correlation from earlier calibrated units to calculate the new gain setting.
11. This power,Pmax measMG, is input to the calibration of TX power table.
12. Set gain to maximum power in low gain mode and measure ACLR at this power level. RFBiasshould be set to 1 andWPABiasshould be set to the same value as for maximum output power.
13. If the requirements are not met, step the gain down and measure ACLR until the requirements are met. Use known correlation from earlier calibrated units to calculate the new gain setting.
14. This power,Pmax measLG, and gain setting provides input to the calibration of TX power table.

E. TX Power Table Calibration

- Purpose

The calibration data contained within the TX Power Table controls the gain for all types of power change; including, the inner-loop power control and maximum output power of the platform.

The purpose of this calibration is to complete the TX Power gain table with values for VGA, QVGA, RFBIAS, WPABias, and WDCDCREF that meet the specified requirements for inner-loop power-control and Maximum output power. The size of hysteresis area must also be found.

These calibrations are designed to conform to the ME maximum output power, inner loop power control, change of TFC and (PRACH preamble tolerances)requirements specified in 3GPP Spec TS34.121.

- Procedure Proposal

This calibration consists of two parts: first measurements and then an off-line calculation. The measurement results are used for characterizing the hardware so that proper settings can be calculated for all tables. Settings and limitations are also used from maximum output calibration.

1. Perform measurements

(1) VGA behavior in LG (Low Gain) mode. PABias should not be offset and RFBIAS should be 1.
(2) VGA behavior in MG (Medium Gain mode). PABias should not be offset and RFBIAS should be 1.
(3) QVGA behavior in LG mode
(4) IQ-Gain behavior in LG mode.
(5) WPABias gain step size. Every eighth setting is measured twice. For better accuracy take the average of each step pair. Interpolate the gain steps in between the averaged measured values.

(6) WDCDCREF gain step size. Every fifth setting is measured twice. For better accuracy take the average of each step pair. Interpolate the gain steps in between the averaged measured values.
(7) Size of step between LG/MG and MG/HG and between each setting of RFBIAS (1-7). The main purpose is to find the relative difference at different frequencies. Distribute with equal frequency offset except if there are known ,worst-case frequencies. Measured at 5 channels, maximum and minimum steps reported. Average value of minimum and maximum should be used in following calculations.
(8) Measure properties: Measure the following properties using a modulated signal:
WPA-gain expansion versus output power on mid channel.
Compensation needed for maximum output power over the band (13 channels).
2. Perform offline calculations
(1) Calculate the compensation values for Table 8-6. Store these values in GD_RF_TXGAIN_TB_SEL_ID.
(2) Extract the range of needed compensation tables (minimum and maximum).
(3) Calculate the expected compensation for each table in dB (use ,table 0 for the table that is ,0 dB or closest to ,0 dB) and spread out the rest to achieve equidistant compensations.
(4) Calculate and store the 24 sets of tables, GD_RF_TX_GAIN_TB0_ID to GD_RF_TX_GAIN_TB23_ID. Each set of tables shall include:
One High-gain table: 44 bytes.
One Low-gain table: 44 bytes.
One RFBias table: 22 bytes.
One WDCDCRef table: 44 bytes.
One WPABias table: 44 bytes.
One value for IQ-Gain: 1 bit (will occupy 1 byte).
One value for TABLE_OVERLAP: 1 byte.
One value for UPPER_LIMIT: 1 byte.
(5) Calculate the actual compensation (for maximum output power) that each of these 24 tables will give. Store this in GD_RF_TX_FREC_INT_ID.
3. Store data in GDFS

Temp.	UARFCN											
	9612	9637	9662	9687	9712	9737	9763	9788	9813	9838	9863	9888
-15												
0												
15												
30												
45												
60												
75												
90												

Table 8-6.The Complete Gain Compensation Table

E. TX Open Loop Power Control Calibration

- Purpose

The purpose of the calibration of open loop power control is to store parameters for the Open Loop Power Control algorithm. This is a pure off-line calculation. Use data (positions and output power, in dBm) from table 0. Curve fitting should be done preferably with minimum square method.

System related requirements:

Open loop power control

Maximum allowed UL TX Power

UE Transmitted power

- Procedure proposal

1. Create a curve fitting for the low-gain region, use positions with a power greater than -50 dBm: Position = B3 * Pout + A3
2. Extract A3 and B3.
3. The power level (output power) at the highest position in the low-gain region sets the parameter P2.
4. Divide the high-gain region into two regions at the split between mid-gain and high-gain. The output power at this position sets the parameter P1.
5. Do a curve fitting for the mid-gain region (where RFBias > 0) of the high-gain region, use power-levels from P2: Position = B2 * Pout + A2
6. Extract A2 and B2
7. Do a curve fitting for the high-gain region (where RFBias = 0) of the high-gain region: Position = B1 * Pout + A1
8. Extract A1 and B1
9. Save A1, A2, A3, B1, B2, B3, P1 and P2 in GD_RF_TX_GAIN_PARAM_ID.

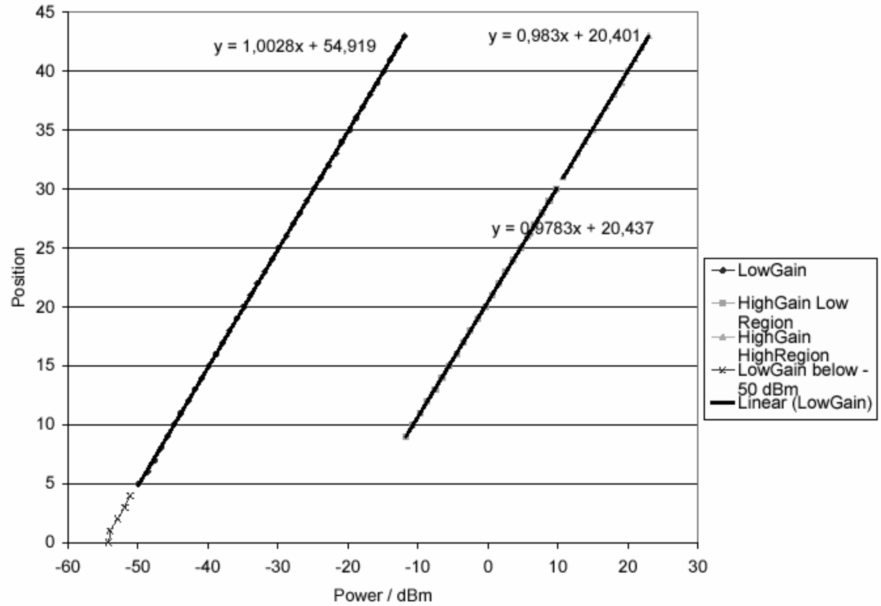


Figure 8-2. Example of Position versus Power and Calculated Equations

F. RX LPF Bandwidth Calibration

- Purpose

This procedure calibrates the LPF bandwidth. The bandwidth of the channel filters will affect system parameters as reception sensitivity and adjacent channel selectivity. The procedure also verifies that the IF-filter is properly matched.

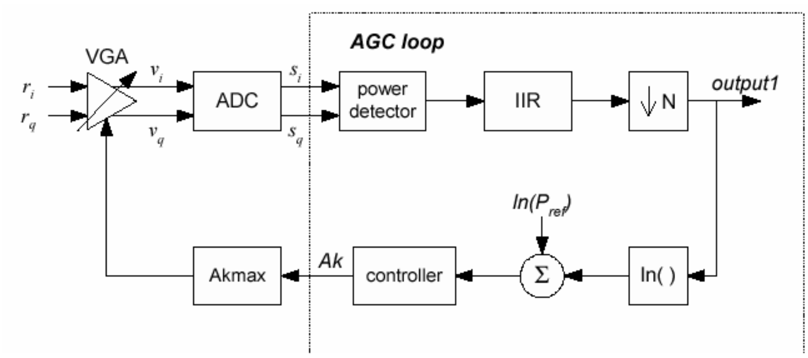


Figure 8-3. AGC Block Diagram (Parameter Ak, Output1, and Pref)

- Procedure Proposal

1. Feed a CW carrier at 2140 MHz with a power of -60dBm into the antenna connector.
2. Set UE in RX-mode on 10695ch.
3. Set the AGC_UL and AGC_LL to minimum. GLNA is forced to high gain mode.
4. Set RF 2110 LPQ and LPBW to 8, that is, LPQ=LPBW=8.
5. Get Ak (output2) from N slots. Calculate Average_Ak (Ak_IB) according to the equation below. N should be as large as possible, with respect to time consumption.

$$Average\_Ak = 10 \cdot \log\left(\frac{1}{N}\sum_{n=1}^{N} 10^{\frac{Ak_n}{10}}\right)$$

Equation 1

6. Set UE on 10705ch and get Ak (output2). Calculate Average_Ak (Ak_LB) according to the Equation 1.
7. Calculate IF-filter symmetry using the following equation.
   IF_SYM = Ak_IB - Ak_LB
8. Set UE on 10685ch and get Ak (output2). Calculate Ak (Ak_OB) according to the Equation 1.
9. Calculate selectivity level using following equation.
   Ak_SE = Ak_OB – Ak_IB
10. If the requirement is not met, decrease LPBW and LPQ one step and repeat from 8.
11. Store the resulting LPBW and LPQ in GD_RF_RX_CONFIG_ID.

F. RX LNA Gain Switch and AGC Hysteresis Calibration

- Purpose

This procedure calibrates the gain correction parameter of Ak in the AGC algorithm between GLNA=0 and GLNA=1; that is, it establishes the gain difference in the LNA between high gain mode and low gain mode. It also calibrates AGC_UL and AGC_LL, the upper and lower Ak values where the AGC should switch between high and low LNA gain (AGC hysteresis).

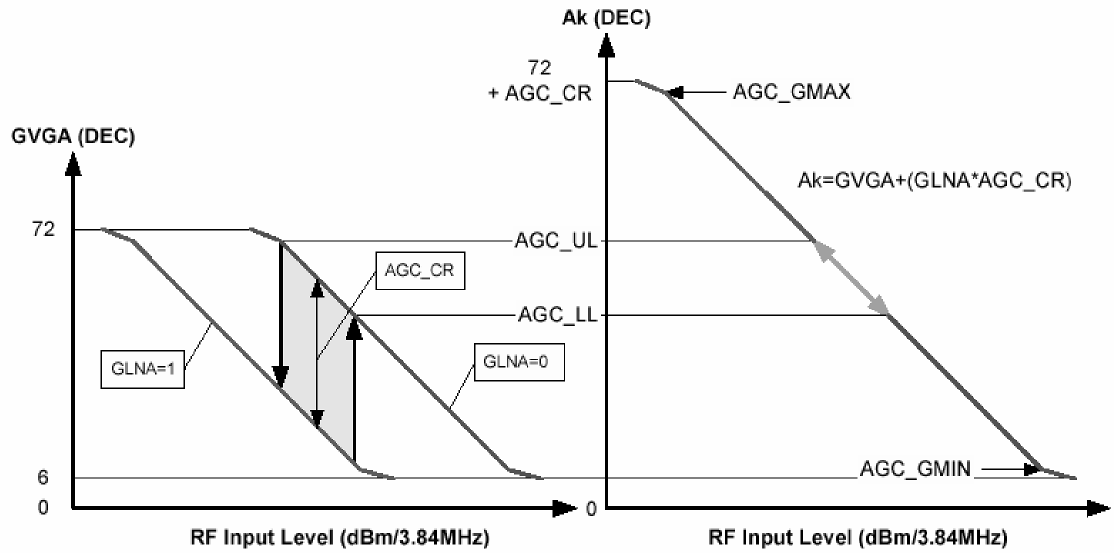


Figure 8-4. LNA Gain Switch and AGC Hysteresis Parameters

- Procedure Proposal

1. Set the UE in RX-mode on 10695ch.
2. Feed a CW carrier at 2140 MHz with a power level of -65dBm.
3. Set the AGC_UL and AGC_LL to maximum. GLNA is forced to low gain mode.
4. Get average Ak from Equation 1 and save it. (Ak_LG)
5. Set the AGC_UL and AGC_LL to minimum. GLNA is forced to high gain mode.
6. Get average Ak. (Ak_HG)
7. (Ak_LG) - (Ak_HG) = (Correction).
8. Round off (Correction) to integer (AGC_CR) and store it in GDFS (GD_RF_RX_CONFIG_ID). AGC_CR is an AGC algorithm parameter and is set to DB 2100 RFIF.
9. Calculate AGC_LL=8+AGC_CR and AGC_UL=18+AGC_CR and store them in GDFS (GD_RF_RX_CONFIG_ID). AGC_LL and AGC_UL are AGC algorithm parameters and are set to DB 2100 RFIF.

G. RX AGC Gain Max and RX RSSI Calibration

- Purpose

To prevent wind up in AGC algorithm, this procedure calibrates the absolute power levels at the antenna connector against RSSI values and the maximum gain setting for AGC. Reference [6] specifies that the reporting range of the RSSI should be between -100 dBm to -25 dBm. The specified accuracy requirement is applied to the received power from -94 through -50 dBm. This is the last RX calibration.

LPBW, LPQ, AGC_CR, AGC_LL and AGC_UL must be calibrated according to above calibrations respectively and applied to this calibration. Initially, the AGC anti-wind up is turned on using AGC_GMAX=127. Use the calibrated value after step 2, otherwise the AGC wind up may occur at the beginning of the RSSI calibration.

- Procedure Proposal

1. Set the ME in RX-mode on channel 10695.
2. Feed a CW carrier at 2140 MHz with a power level of -105 dBm. Get average_Ak (output2), add 6 to the value and store it in GDFS as AGC_GMAX (GD_RF_RX_CONFIG_ID), rounded off to an integer. Set the AGC parameter AGC_GMAX to the calibrated value.
3. Clear Ak ,table 0.
4. Change the CW carrier power level to -95 dBm.
5. Read Ak value (output2) and calculate Average_Ak (Equation 1). Store Pin_Corrected (Equation 2) at Ak=round(Average_Ak). N in Equation 1 should be as large as possible.

   Pin_Corrected = Pin-round(Average_Ak)+Average_Ak   Equation 2
6. Then increase the output level of the signal generator to -80, -60, -40 and -25 dBm and store the corrected RF input level and Ak to the memory respectively.
7. Use the average Ak values and Pin_Corrected from the two lowest power levels (-95 and -80 dBm) to extrapolate Ak and Pin_Corrected for -110 dBm according to:

   Average_Ak_110 = 2*Average_Ak_95 – Average_Ak_80

   Pin_Corrected_110 = Pin_Corrected_95 – Pin_Corrected_80
8. Store Average_Ak_110 and Pin_Corrected_110 according to step 4.
9. Perform the interpolation. AK_BANK_SEL in DB 2100 shall be set to 0.
10. Measure the ME temperature (T) and save for offline calculations.
11. Store the result to GDFS. (GD_RF_RX_AK_TB0_ID). When stored in GDFS, the first position in the table (Ak=0) should be replaced with the table number (0-23) in bcd format and the second position (Ak=1) set to 0xffff to flag that the table is calibrated. Position 2 to 5 should be set to zero.
12. Perform the offline calculations and check the requirements.

8.3.6 Baseband Calibration Item

A. Battery Voltage Calibration

- Purpose

Calibrates the voltage table for the power management functionality. Some voltage measurements in the remaining test will be done with calculated voltage levels from this test.

- Procedure Proposal

1. Send the command LVBA=0 to reset local values in Test Program.
2. Set voltage on VBATT to 3.20 V.
3. Send the command LVBA=5,0x140 to read the low voltage level from ADC.
4. Set voltage on VBATT to 4.10 V.
5. Send the command LVBA=5,0x19A to read the high voltage level from ADC.
6. Send the command LVBA=1 to store local values into global data.
7. Send the command LVBA=3 to view and record values stored in global data.

Voltage Level on VBATT (V)	Min.	Typ.	Max.	Unit
3.2	19	2E	3C	HEX
	25	42	60	DEC
4.1	64	7E	96	HEX
	100	125	150	DEC

Table 8-7. Battery Voltage Calibration Limits

8.4 Program Operation

8.4.1 XCALMON Program Overview

When you try to calibrate the U8110 mobile phone, you should make a configuration of calibration environment like Figure7-1. And if you finish making configuration, please execute the XCALMON program. Running the XCALMON program, you should show XCALMON program window like Figure7-5.

If XCALMON program would be executed, it checks the connection of instruments and initializes them automatically. The result of checking and initializing instruments was shown like Figure7-6.

XCALMON supports three functions.

- Calibration of EGSM 900, DCS 1800, and WCDMA band
- Instrument (Agilent8960, Tektronix PS2521G) control
- UART communication with U8110 mobile phone

XCALMON has three windows and each window support different function.

- ITP(Integrated Test Program) starting window using production loader
- Calibration tree window
- Command window which supports interactive ITP commands like Hyper terminal

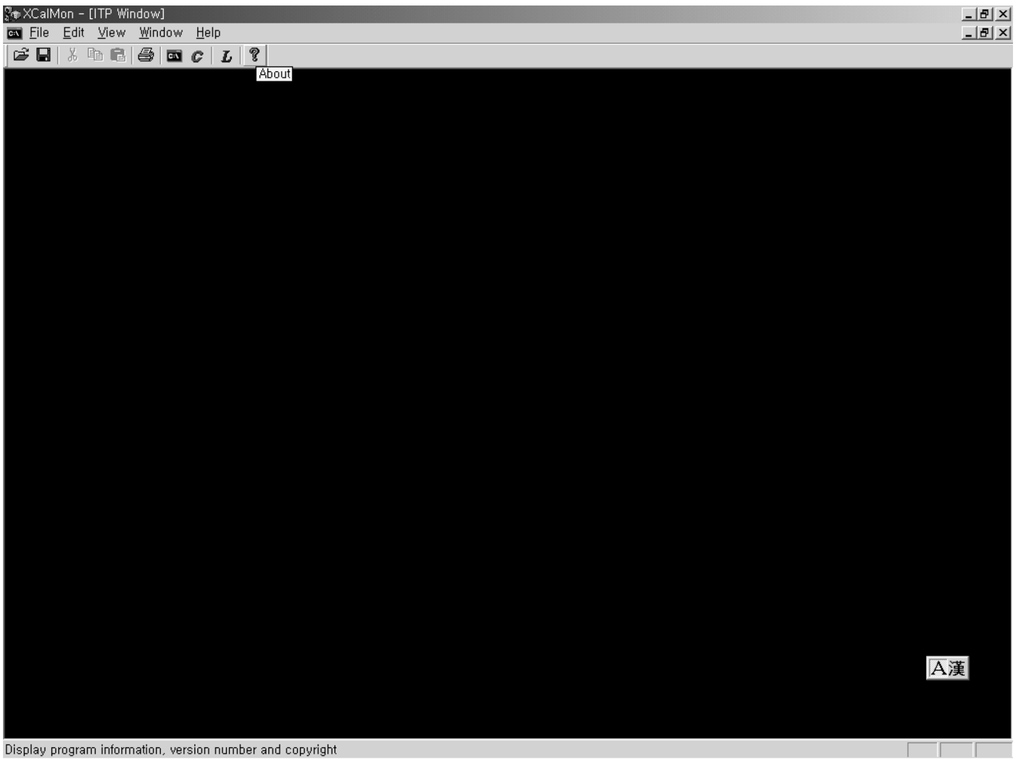


Figure 8-5. XCALMON Window

8.4.2 XCALMON Icon Description

A. DOS Window Icon

When you click the DOS window icon, then you should see the ITP command window like DOS window of DOS-operating system. In ITP command window, you should communicate with U8110 mobile phone which is running in ITP mode.
For example, if you will enter command “VERS” and enter the return key, you should get the response of the present running ITP version information from U8110 mobile phone.

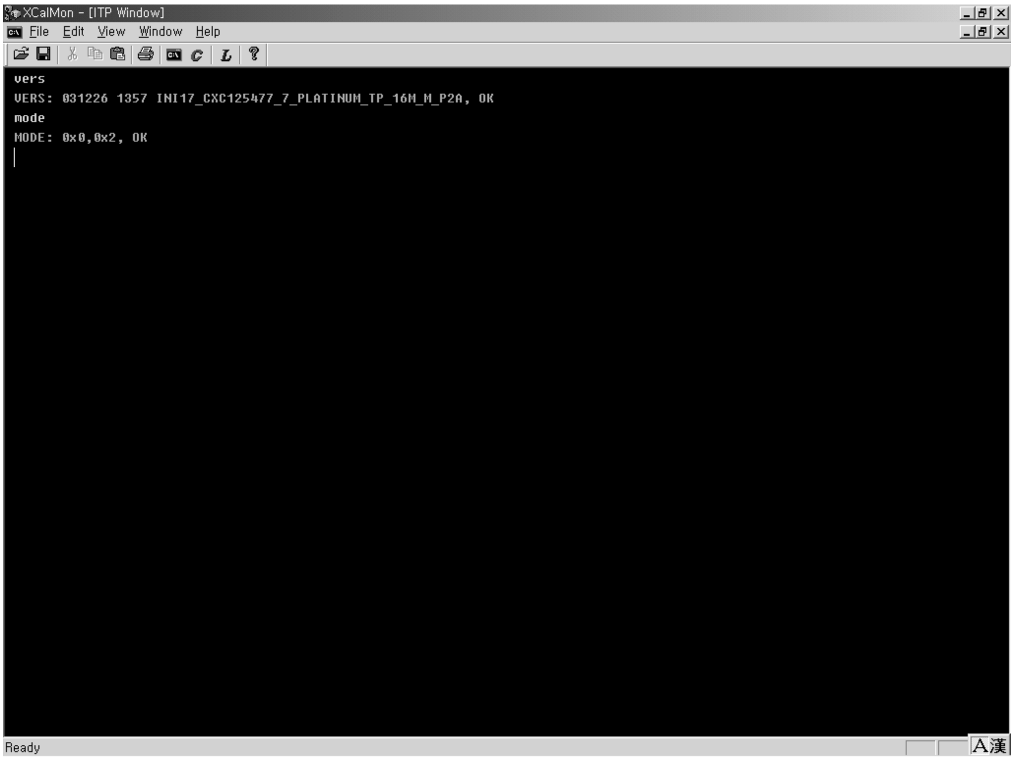


Figure 8-6. XCALMON ITP Command Window

B. Calibration Tree Window Icon

When you click the calibration window icon ”C”, then you should see the calibration tree window. That will be shown all calibration items. If you want to calibrate U8110 mobile phone for all calibration items, you should select “Calibration” and push “F4” button in your keyboard.
Also there are four tap view in calibration window.
- OUTPUT : All results of calibration
- STATUS : Summary of calibration result
- INSTRUMENT : Control and view instrument connection status
- UART : Control and view UART connection status

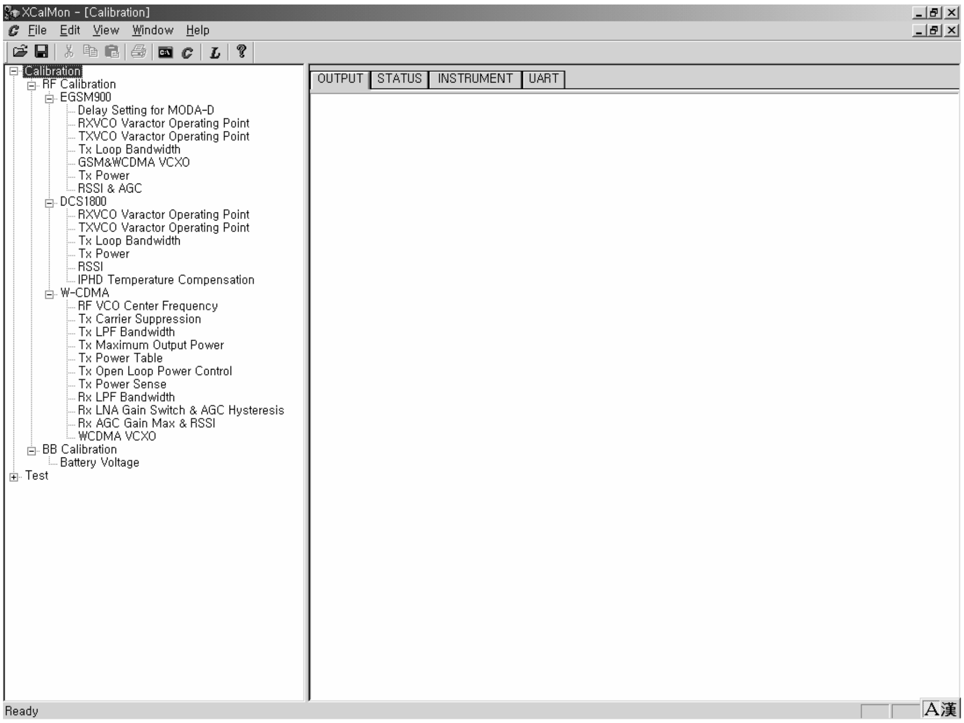


Figure 8-7. XCALMON Calibration Tree Window (OUTPUT Tab)

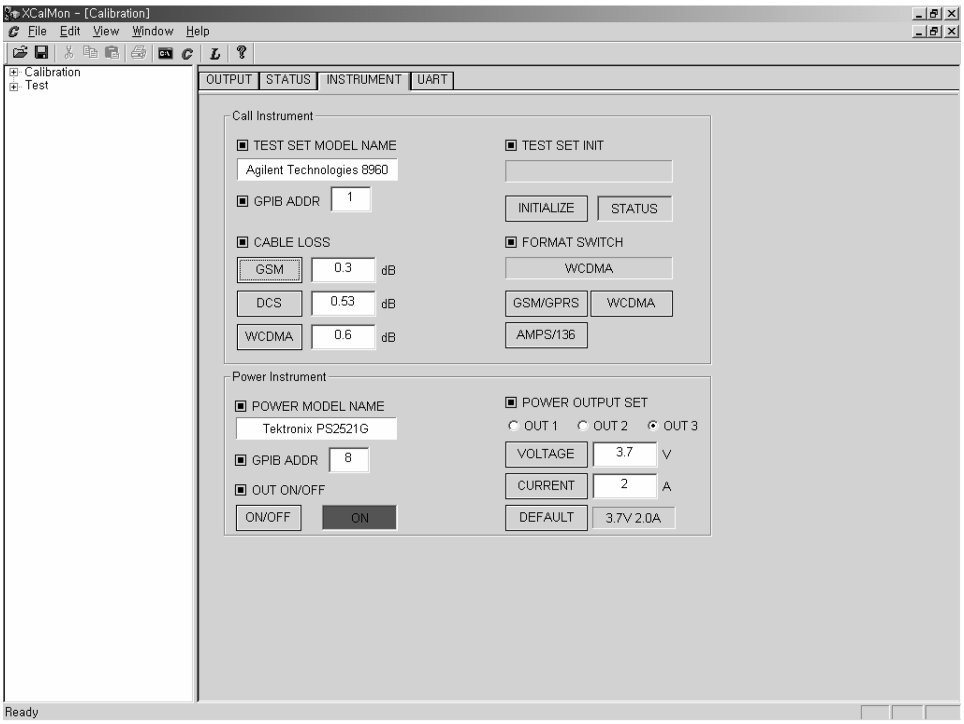


Figure 8-8. XCALMON Calibration Tree Window (INSTRUMENT Tab)

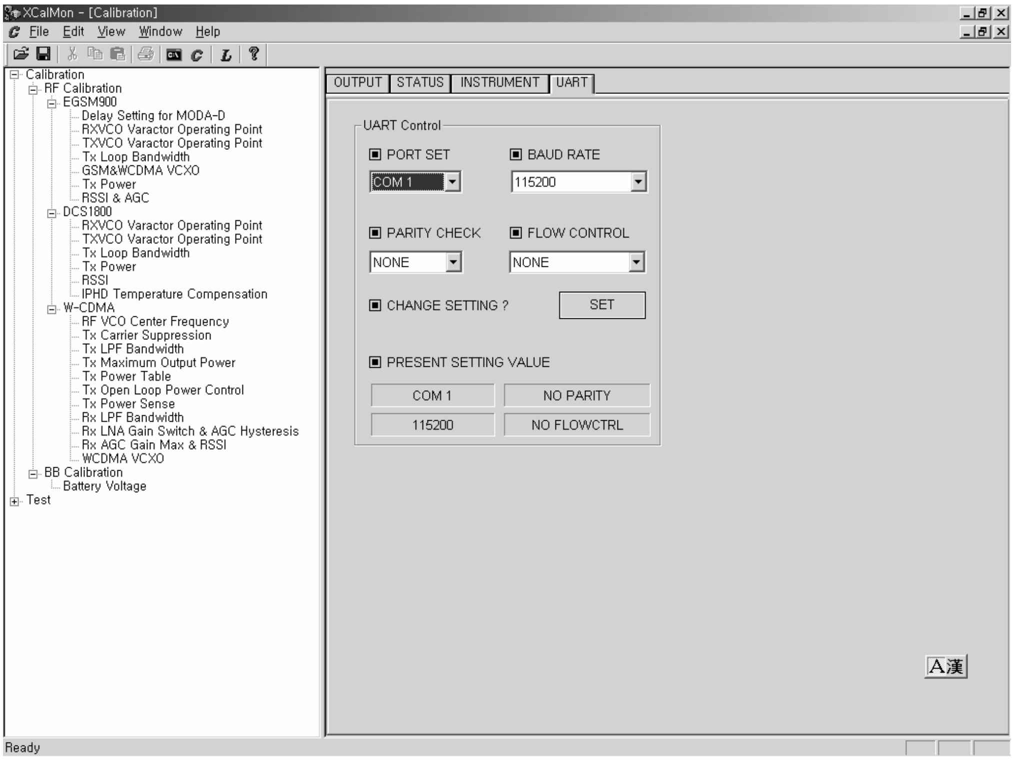


Figure 8-9. XCALMON Calibration Tree Window (UART Tab)

C. ITP Starting Window Using Production Loader

When you click the ITP starting window icon”L”, then you should see the ITP starting window. That dialog window just wait for power-on of U8110 mobile phone. When it will occur power-on, it automatically start ITP running.

If you want to change the start address of ITP, you could change that address directly.

To change ITP start address is possible when we download “Production loader” previously.

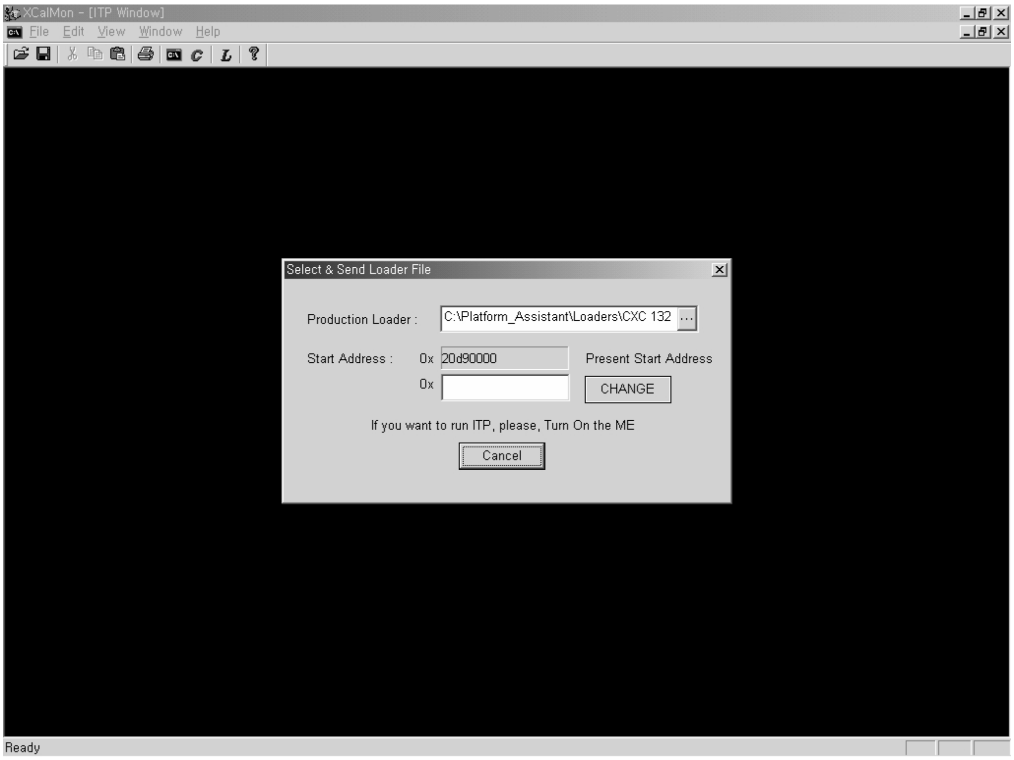


Figure 8-10. XCALMON ITP Starting Window (Using Production Loader)

8.4.3 Calibration Procedure

Calibration procedure of XCALMON was the same as below procedure.
- Configuration of calibration
- Running ITP using production loader
- Calibration start using XCALMON
- Verification of calibration result

A. Configuration of Calibration

Configure to calibrated U8110 mobile phone like Figure7-1. If configuration will be accomplished, start XCALMON program.

B. Running ITP Using Production Loader

If XCALMON will be executed, you should run ITP using “L” ITP starting icon at first.
Click the “L” icon, then you will see the ITP start window like Figure7-10.
When you will turn on the U8110 mobile phone, the production loader will be downloaded automatically like Figure7-11 and then it will execute the ITP at once.
If the ITP will operate normally, you should see the characters “TP, OK” in ITP command window like Figure7-12.

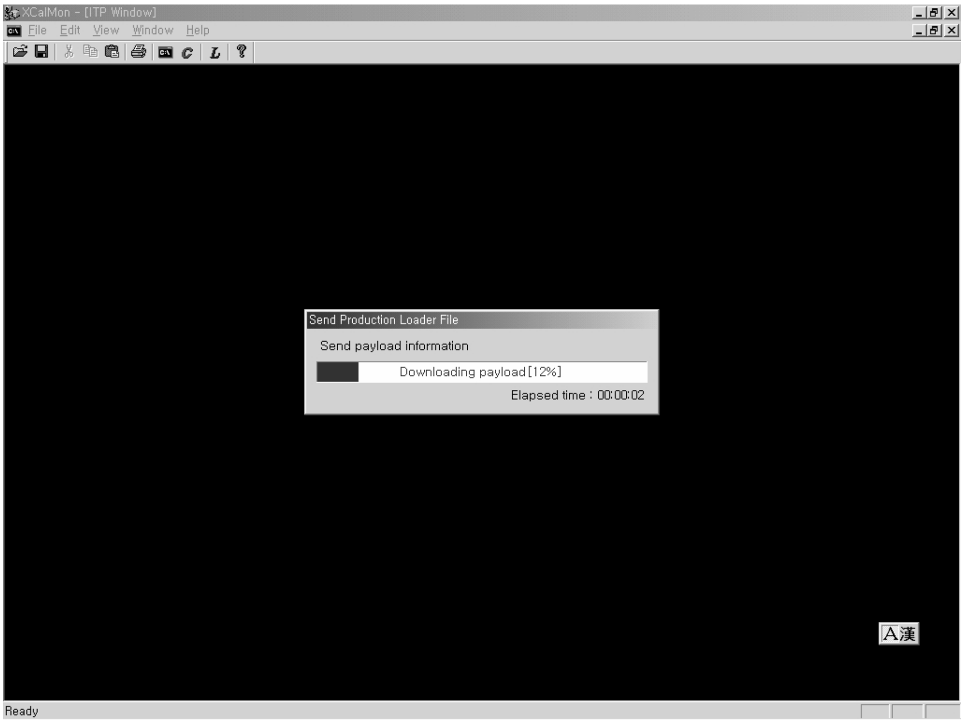


Figure 8-11. Production Loader Downloading

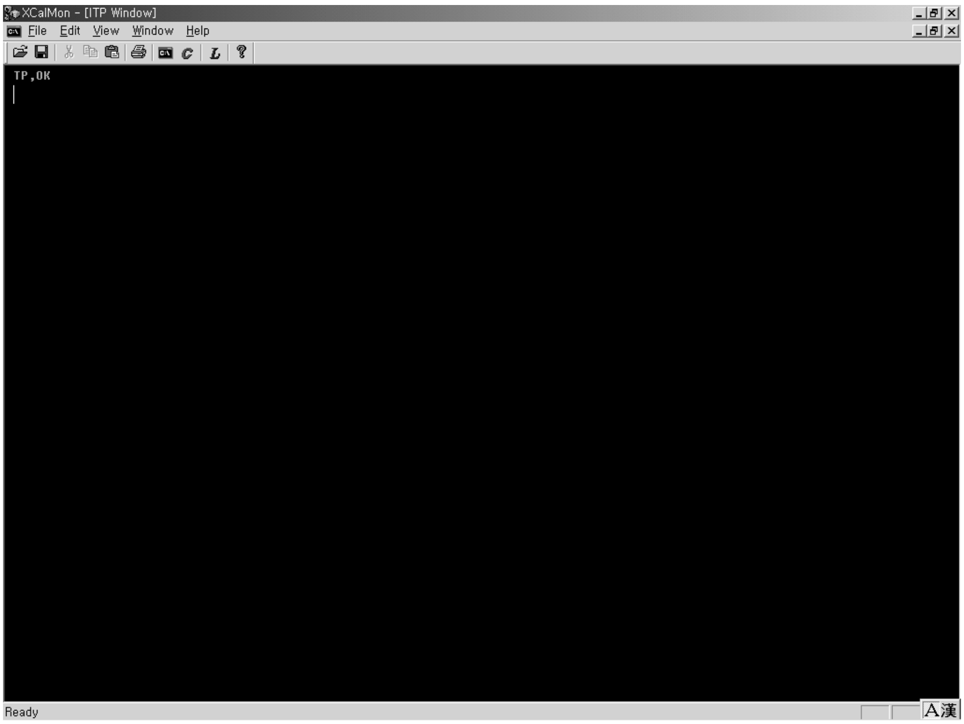


Figure 8-12. ITP Start Complete Window

C. Calibration Start Using XCALMON

If you want to calibrate U8110 mobile phone, click the calibration icon “C”.
And then you will see the calibration tree window like Figure7-6.
To start calibration, you should select “Calibration” item and push “F4” button in your keyboard.

D. Verification of calibration result

If the calibration will be ended, you will see several message window and the result of calibration through OUTPUT & STATUS tab view.
The detail explanation of those will be described in chapter 7.4.4

8.4.4 Calibration Result Message

If the calibration is over without error, “PASS” message window will show up like Figure7-13. On the contrary, if the calibration is over with some error, “FAIL” message window will show up like Figure7-14.
Additionally, in all of the cases, it is possible to check the calibration result with OUTPUT & STATUS tab view.

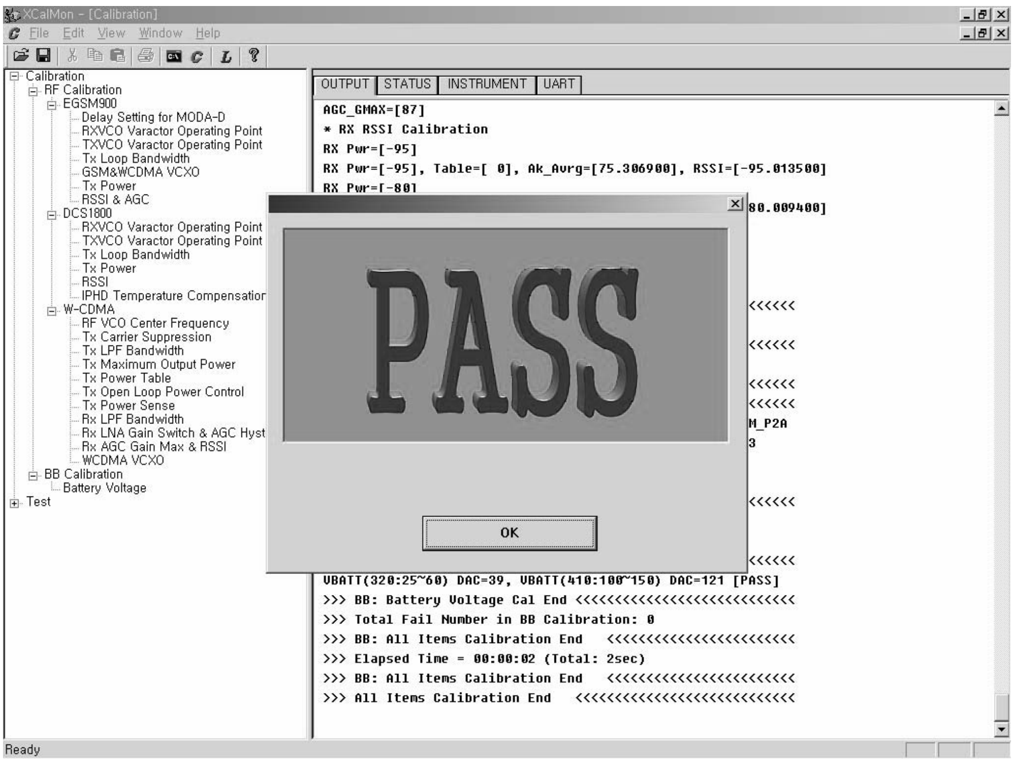


Figure 8-13. Calibration PASS Message Window

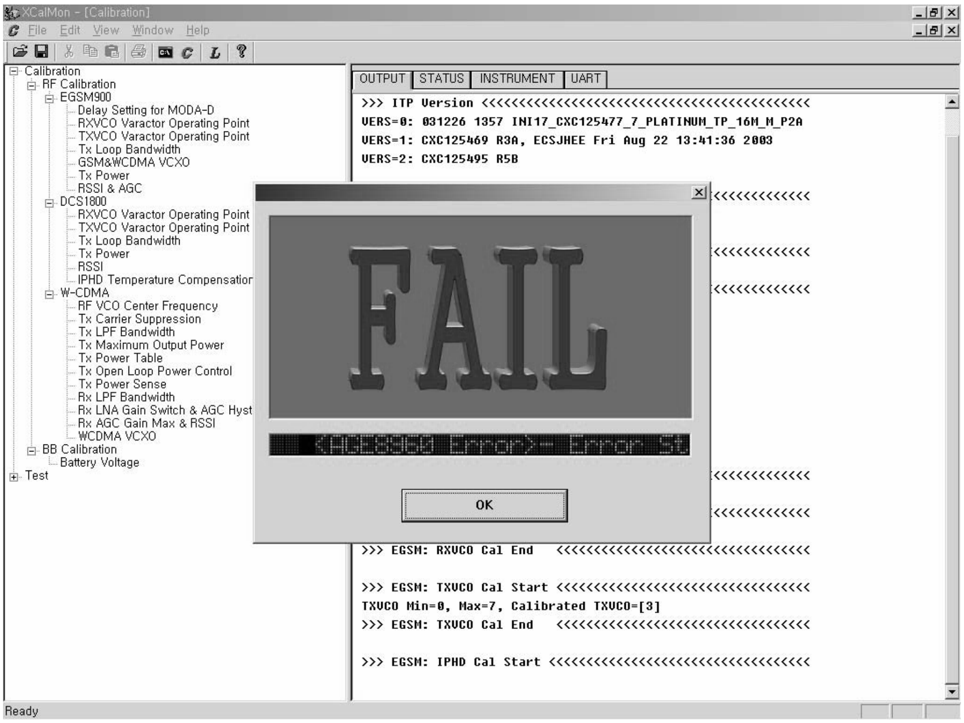


Figure 8-14. Calibration FAIL Message Window

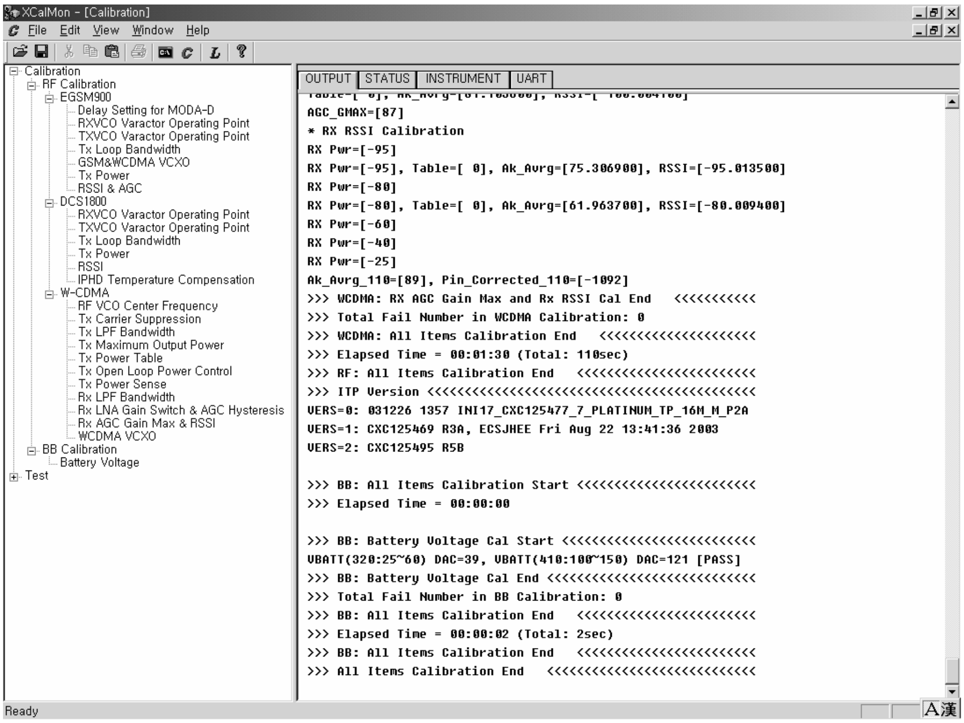


Figure 8-15. Calibration Result from OUTPUT Tab View

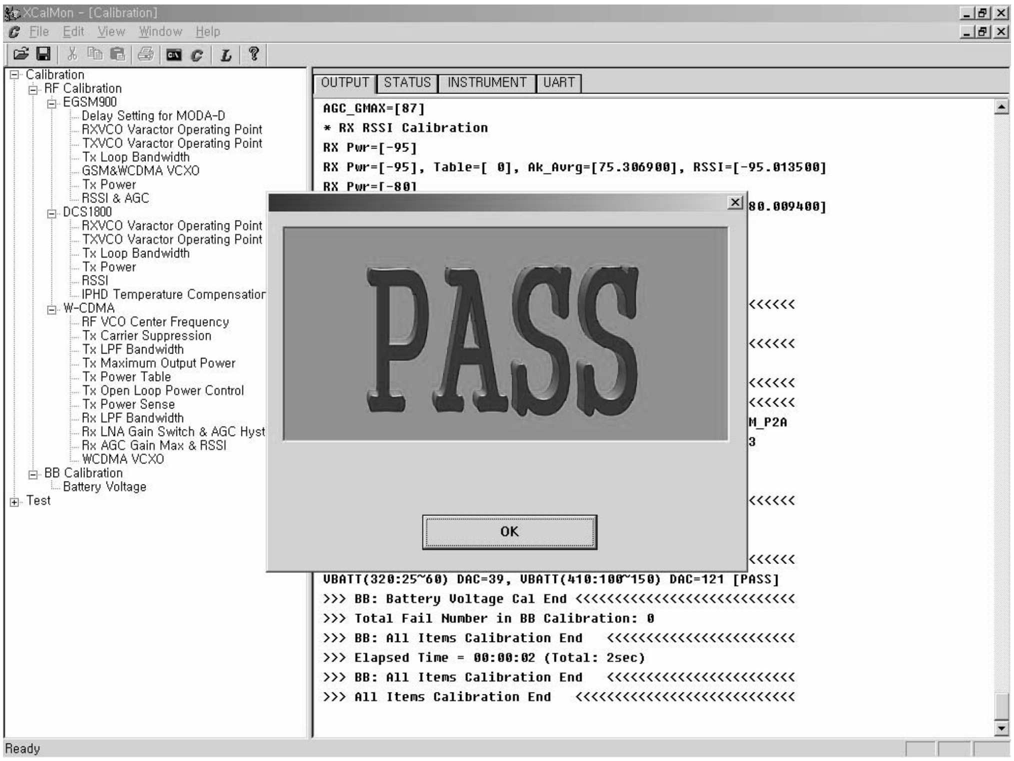
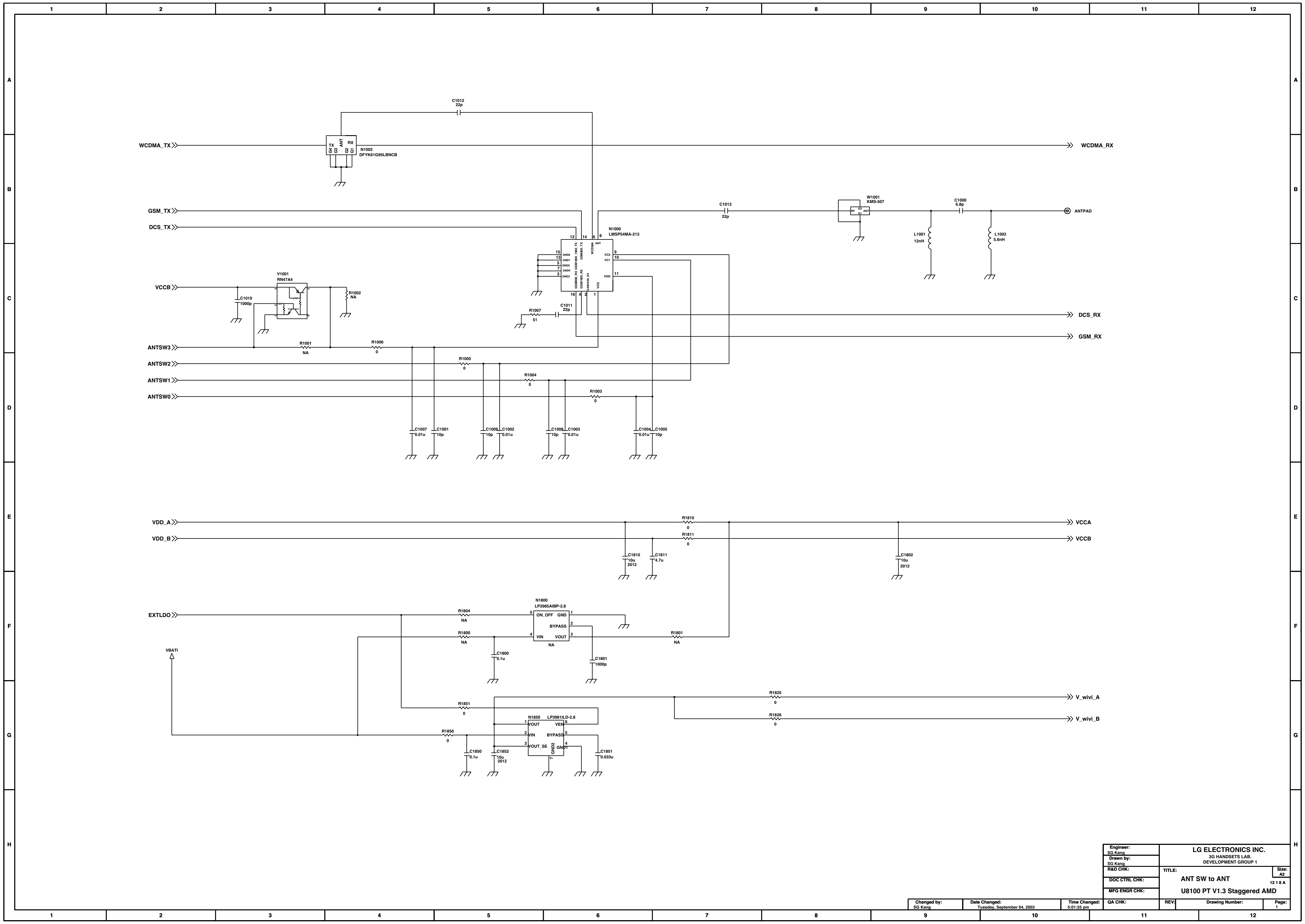
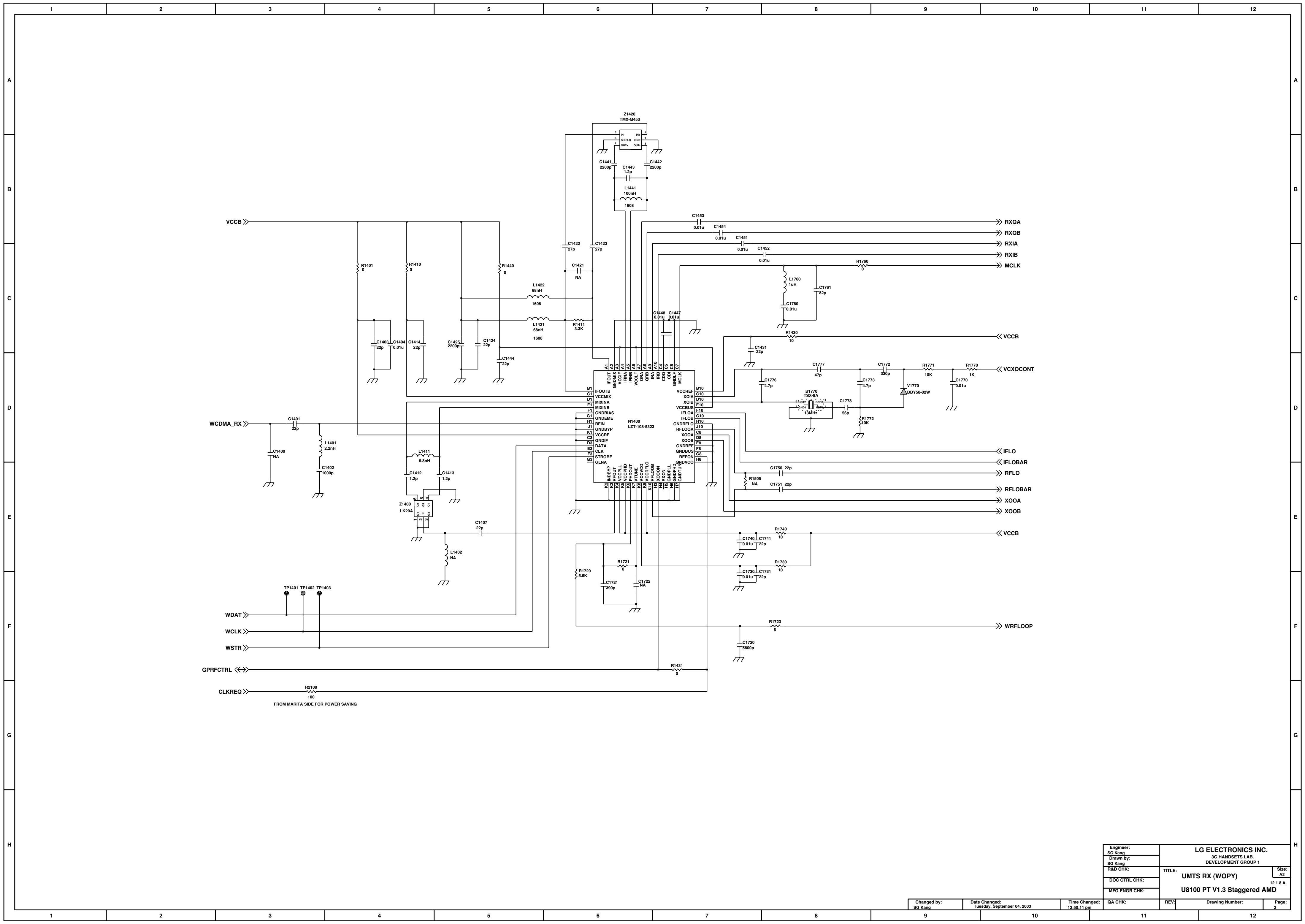


Figure 8-16. Calibration Result from STATUS Tab View

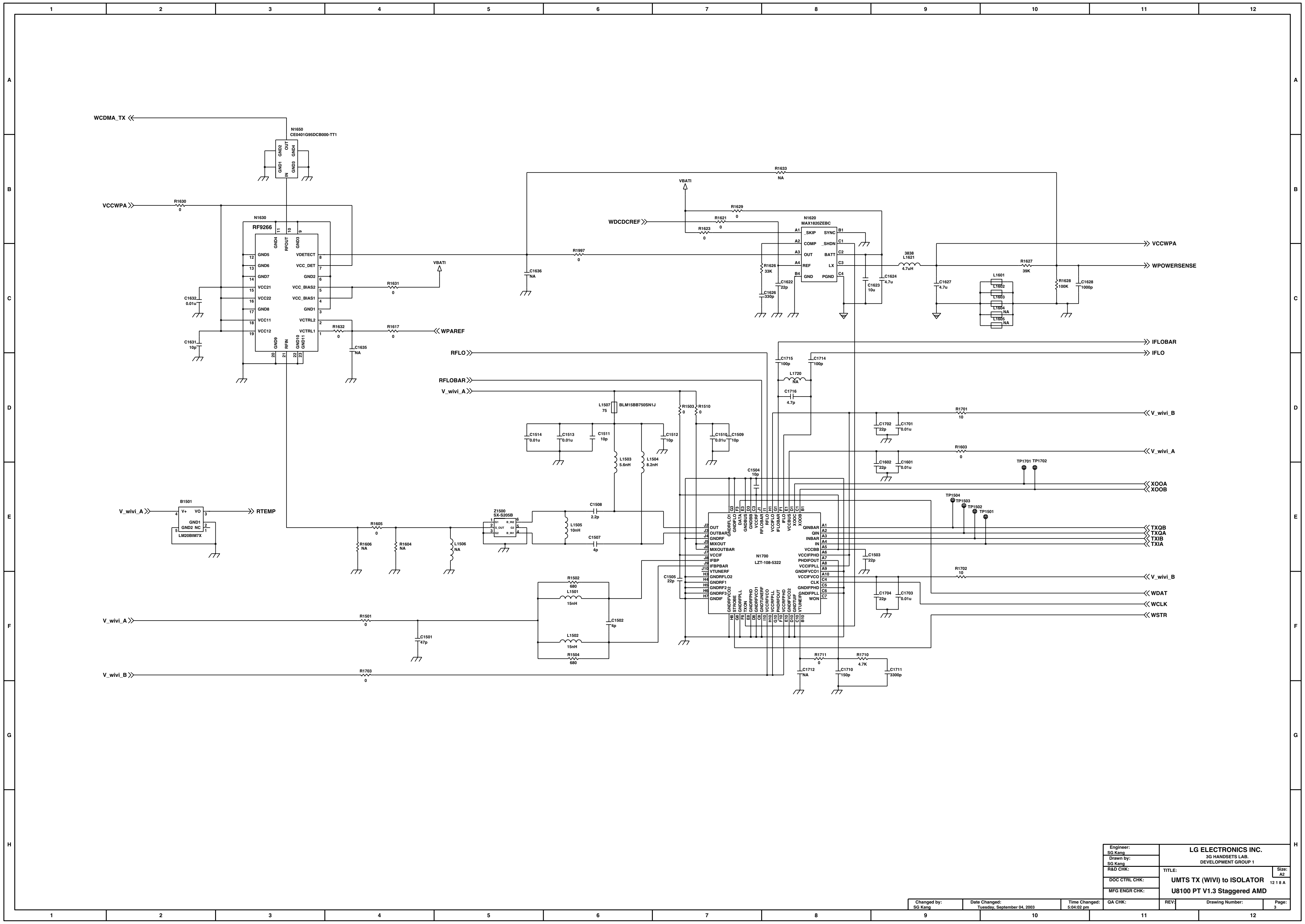
9. CIRCUIT DIAGRAM



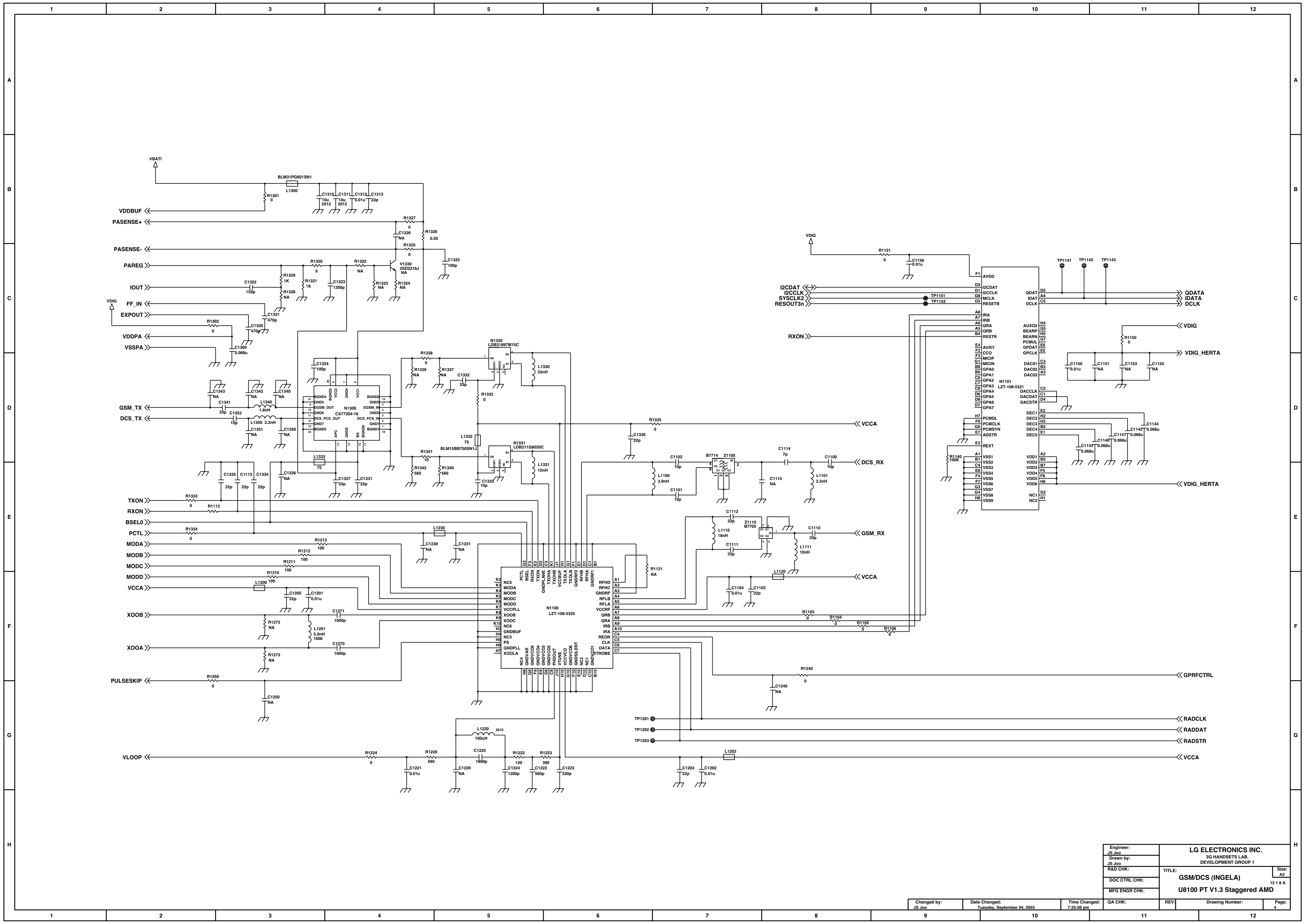
9. CIRCUIT DIAGRAM



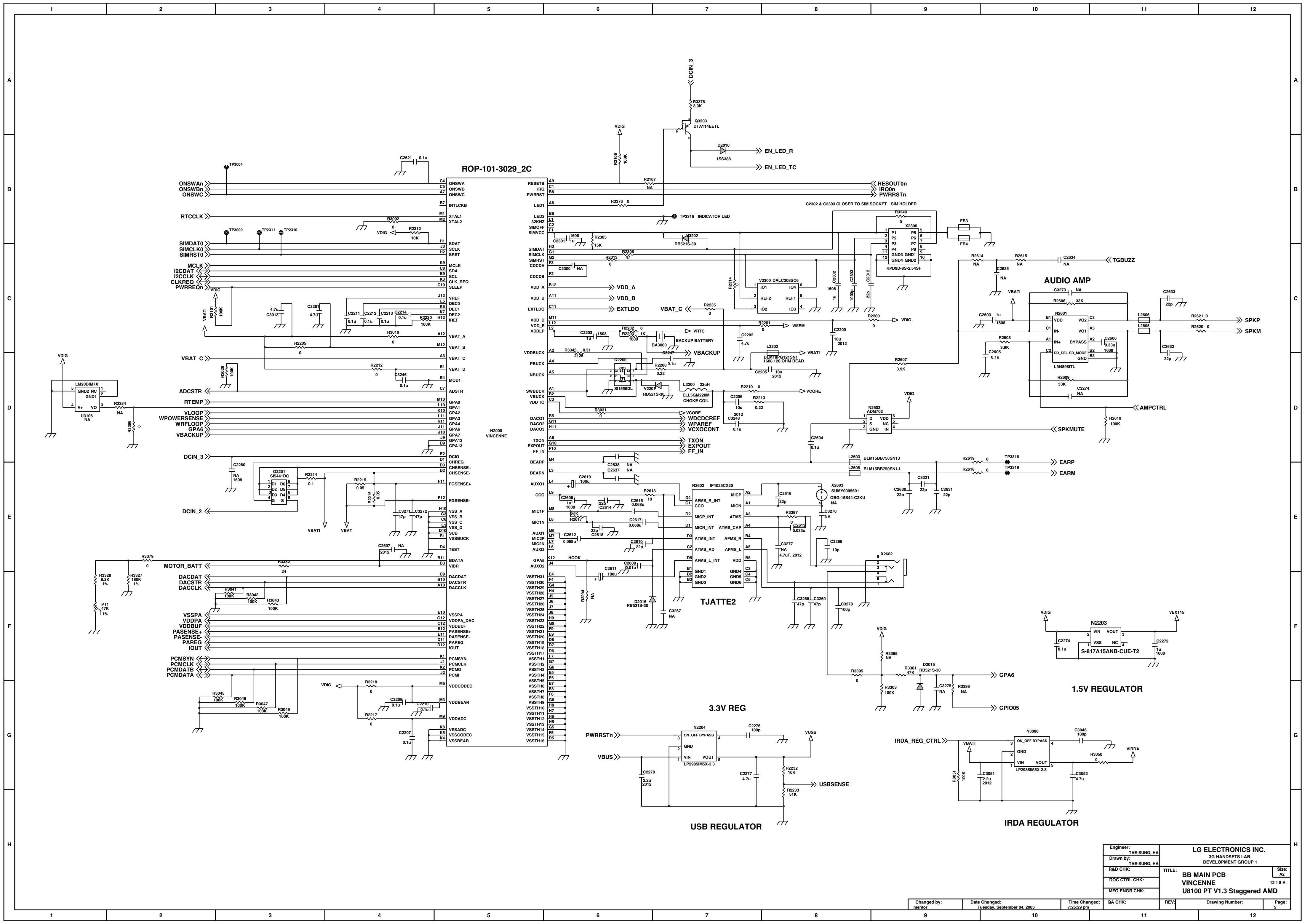
9. CIRCUIT DIAGRAM



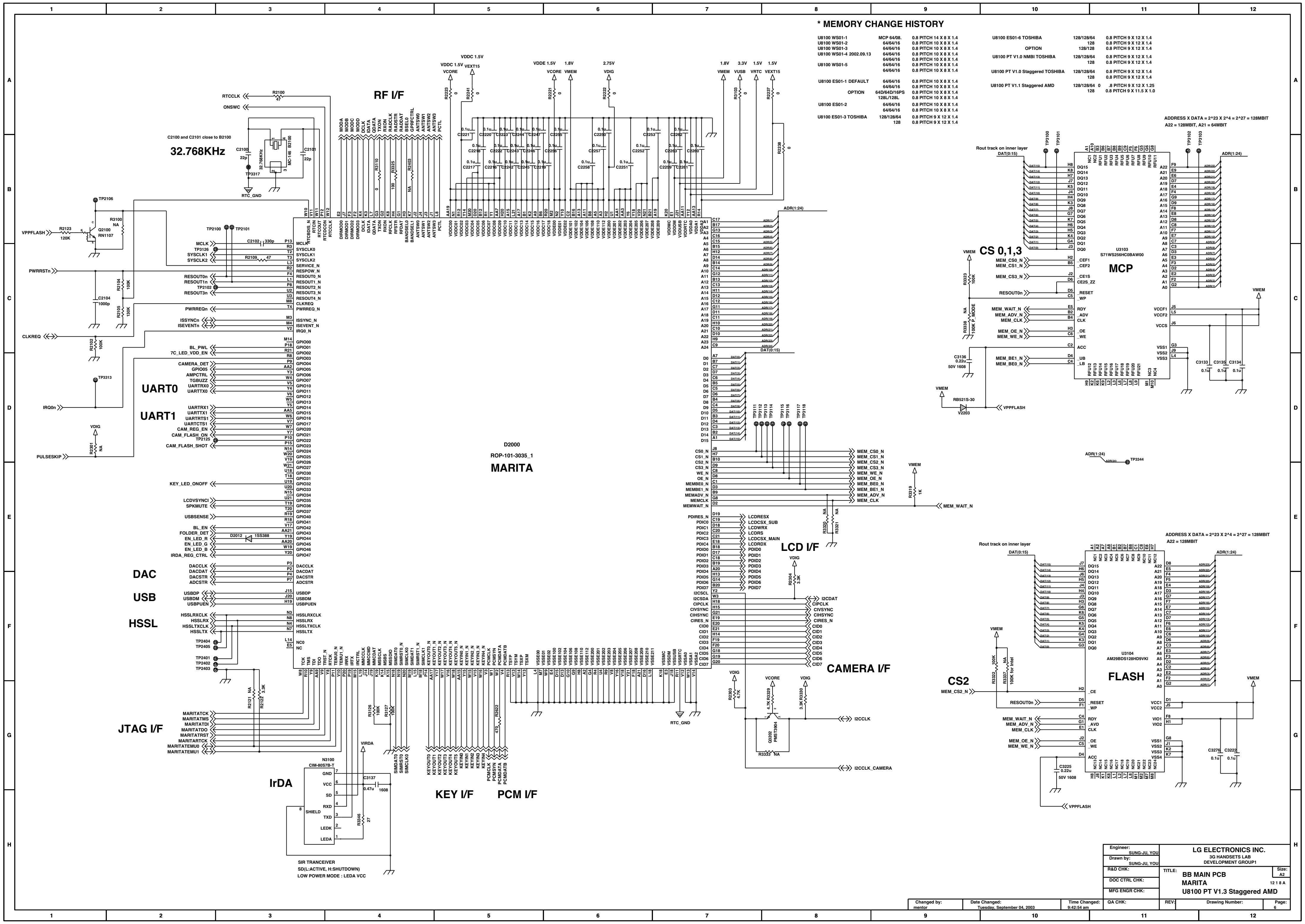
9. CIRCUIT DIAGRAM



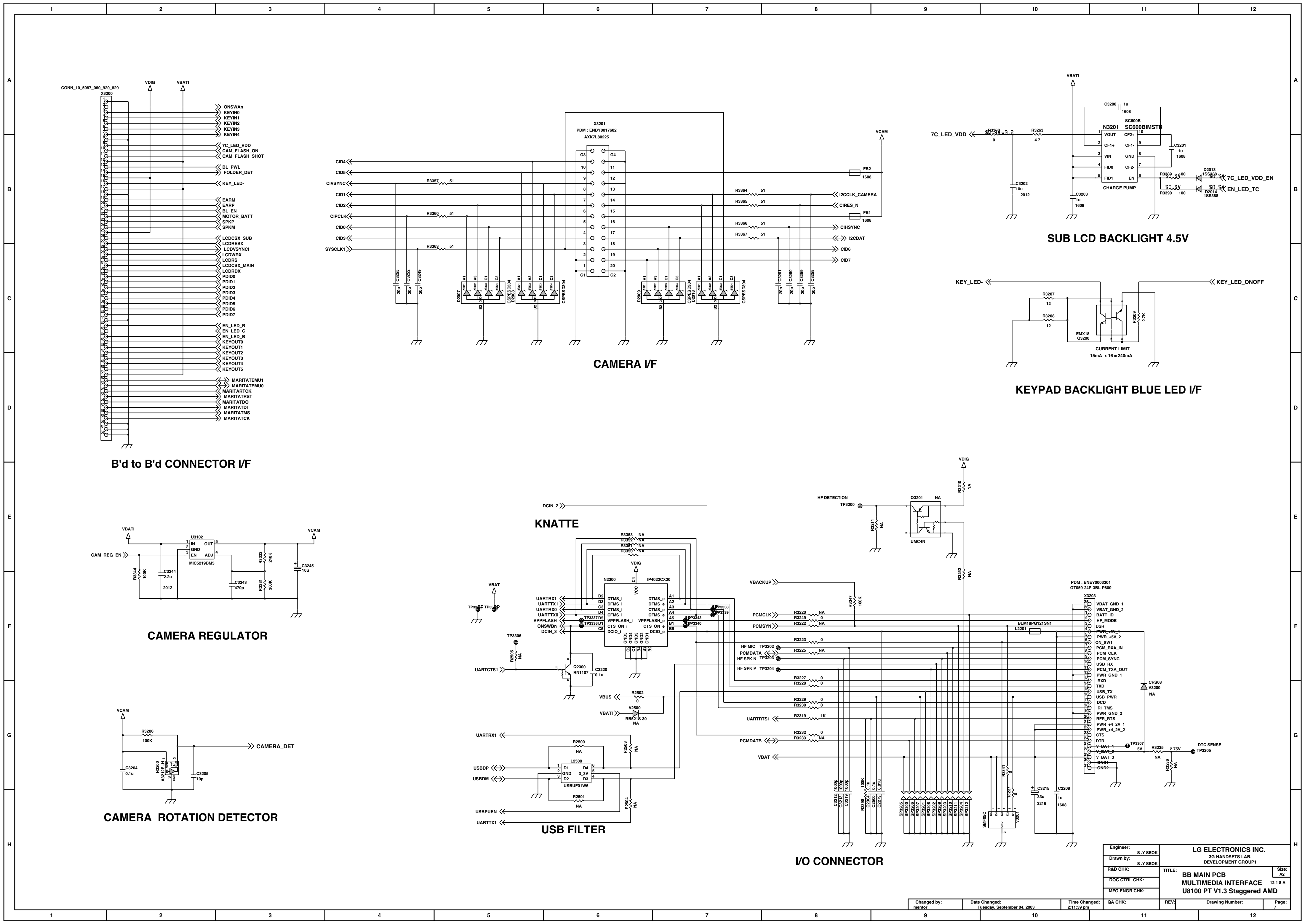
9. CIRCUIT DIAGRAM



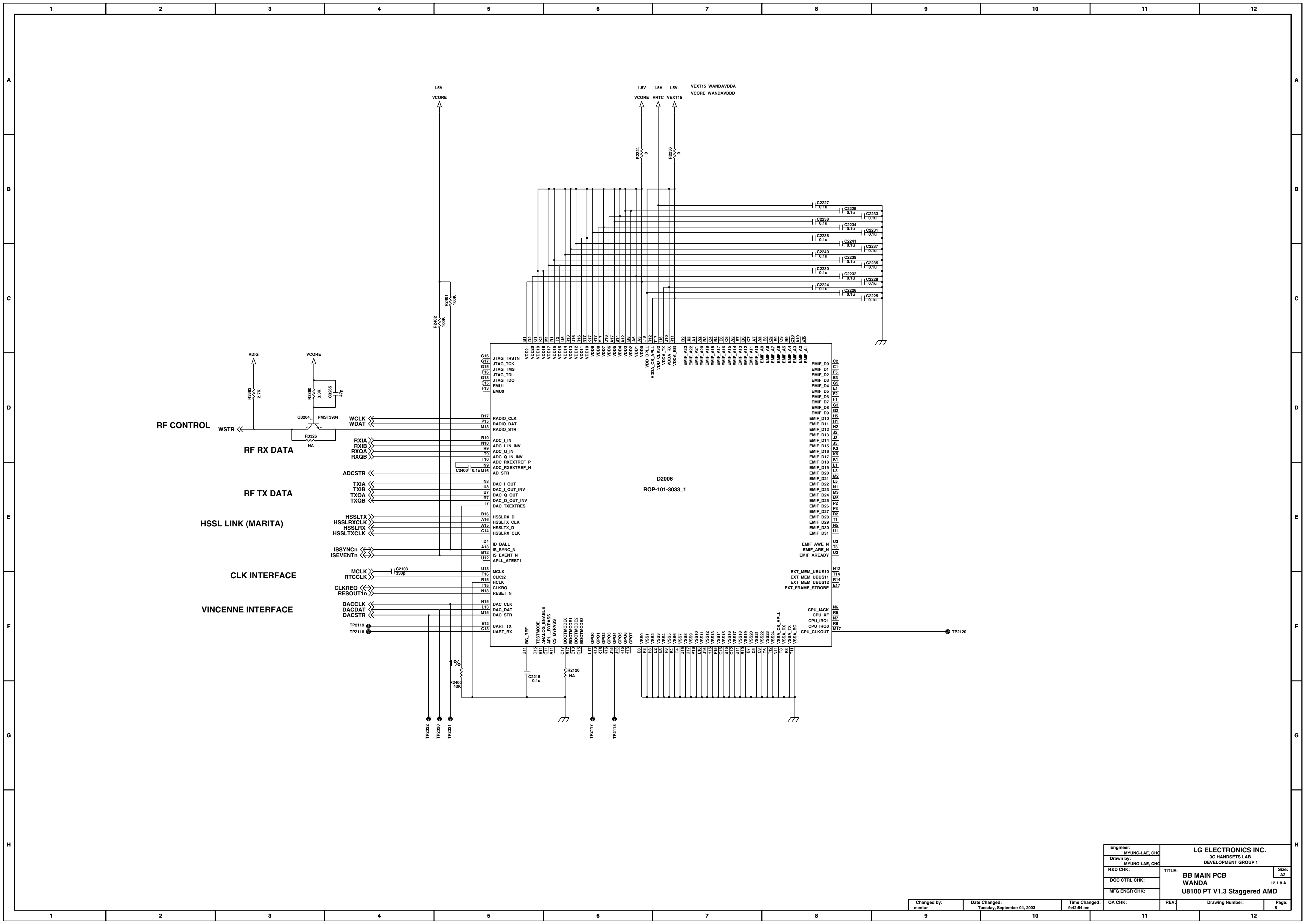
9. CIRCUIT DIAGRAM



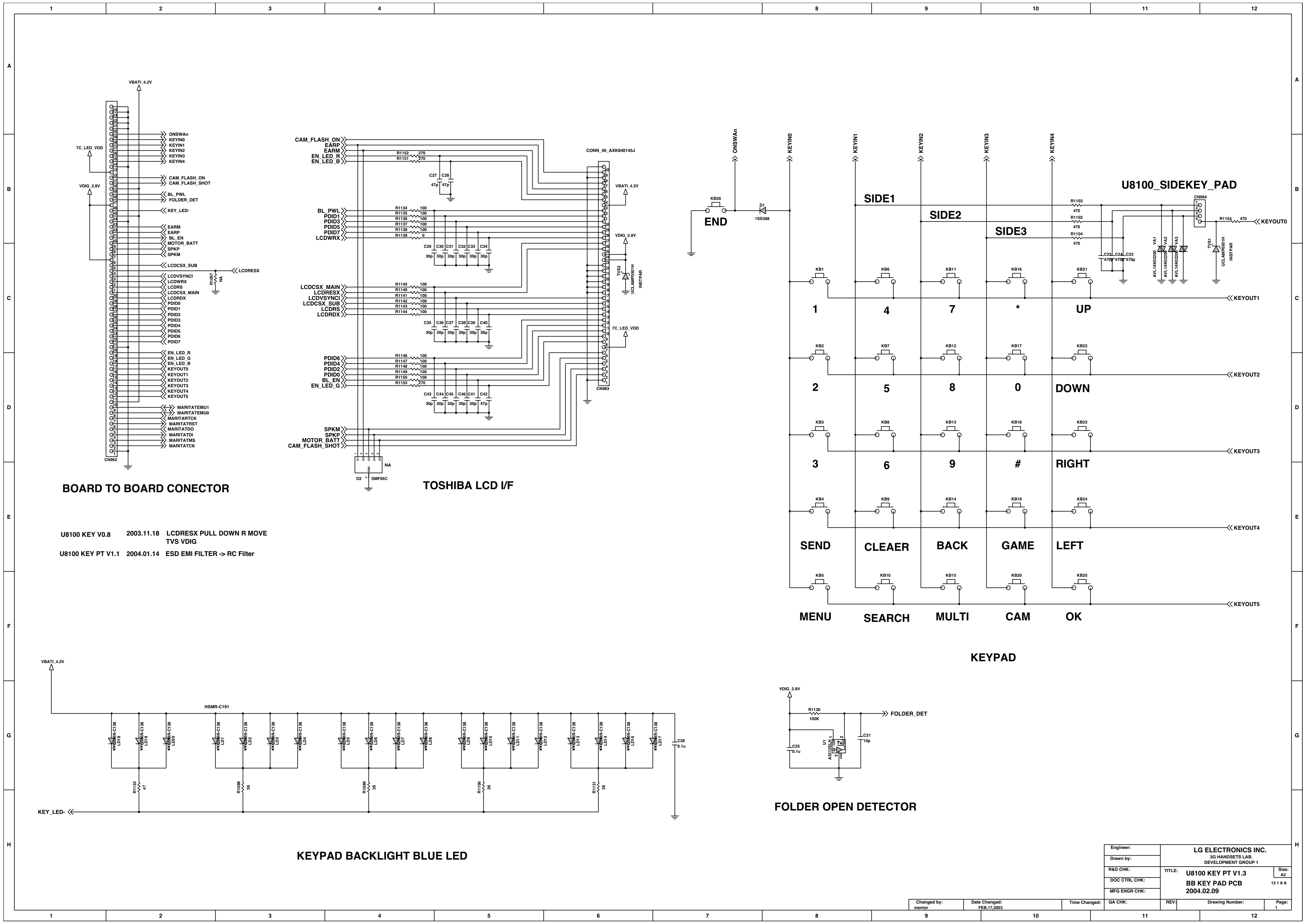
9. CIRCUIT DIAGRAM



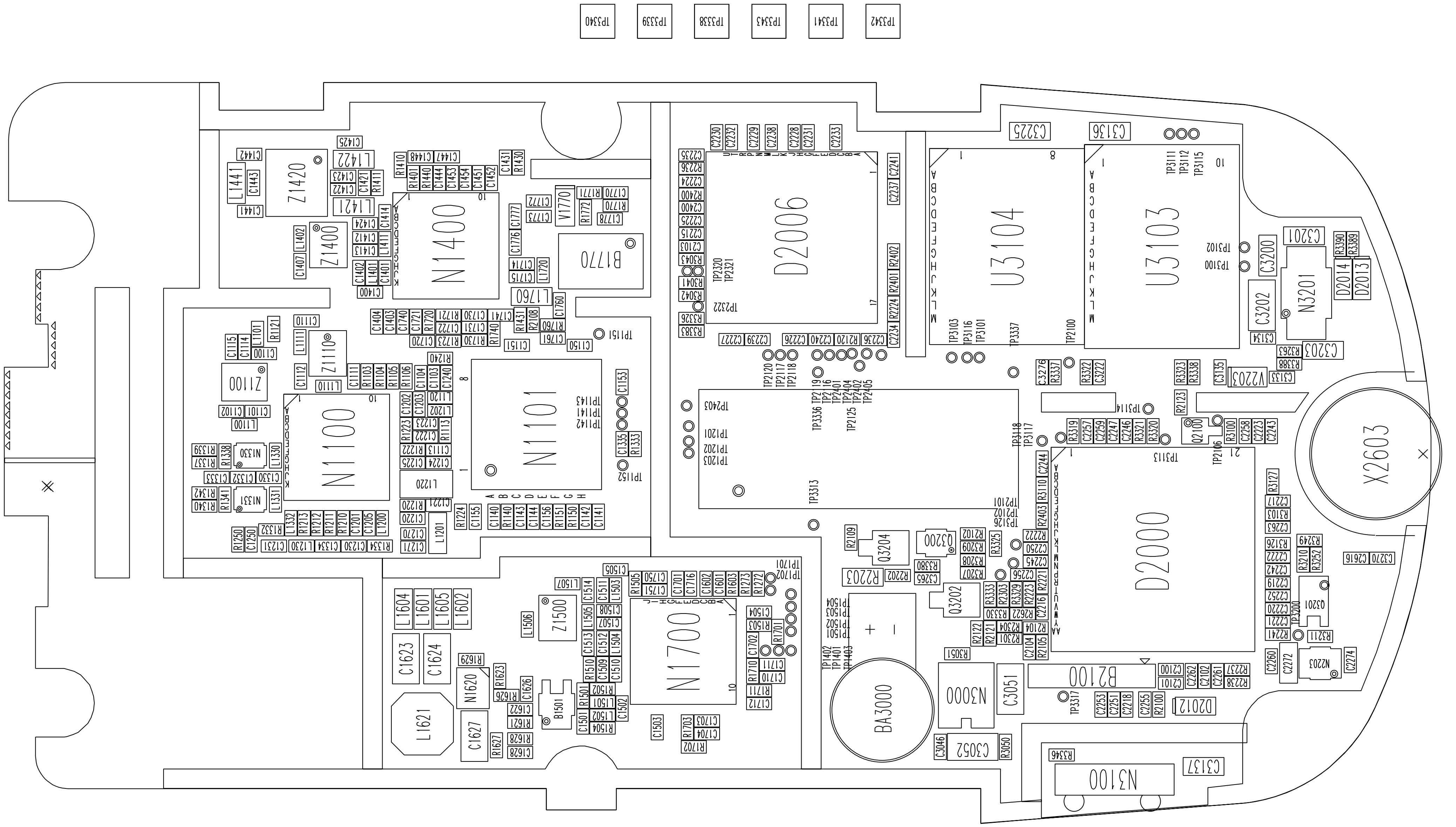
9. CIRCUIT DIAGRAM



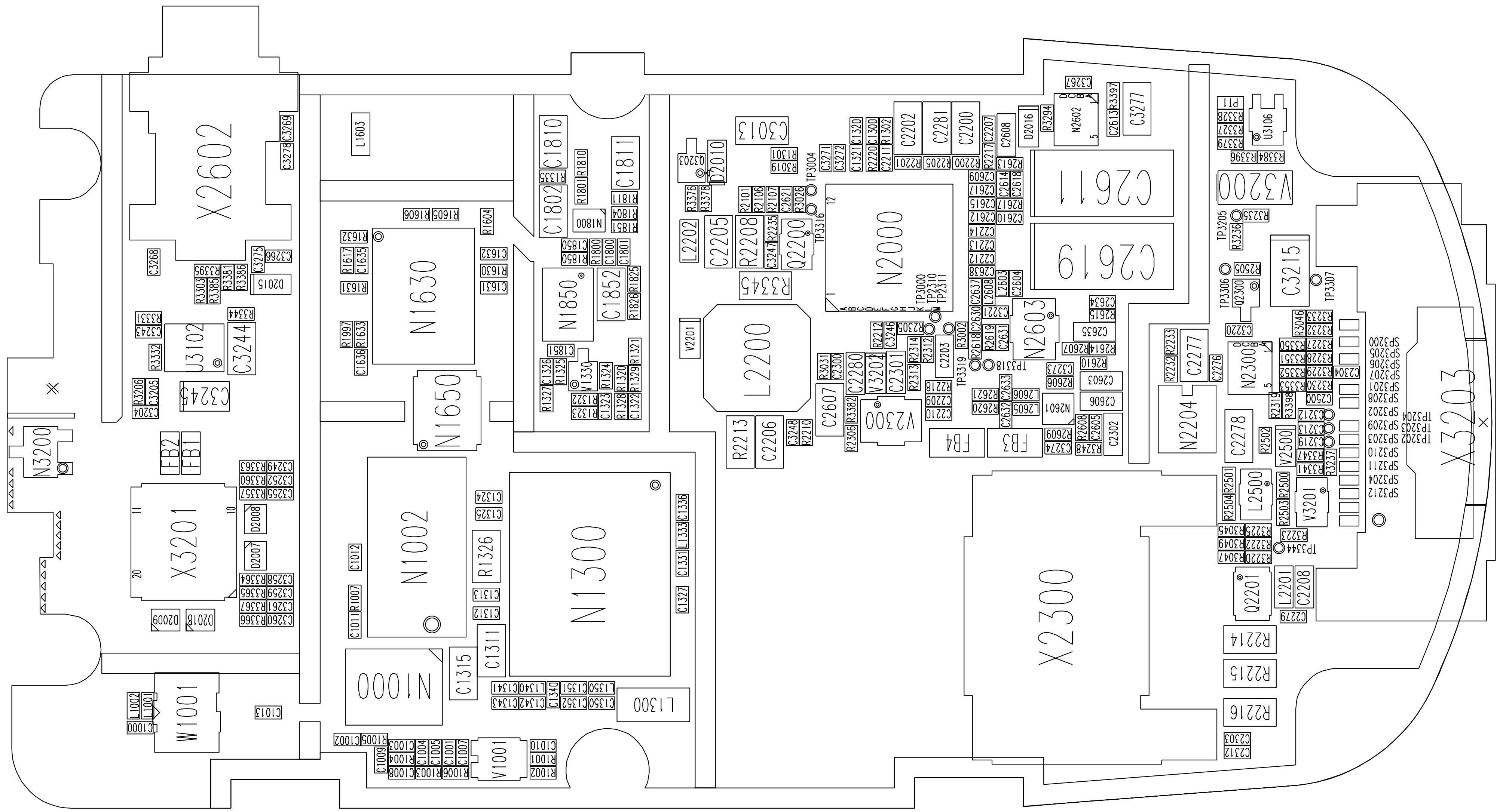
9. CIRCUIT DIAGRAM



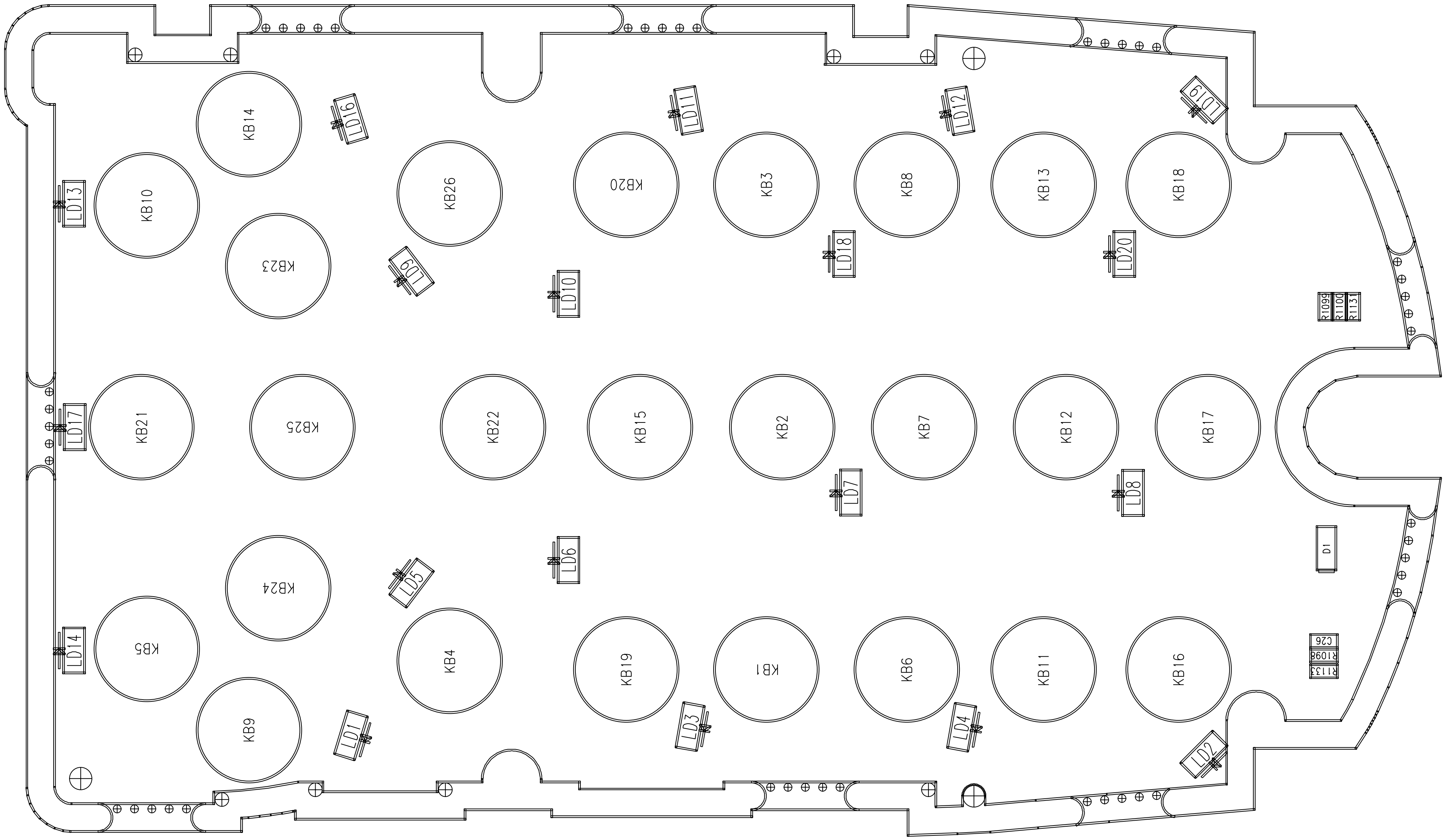
10. PCB LAYOUT



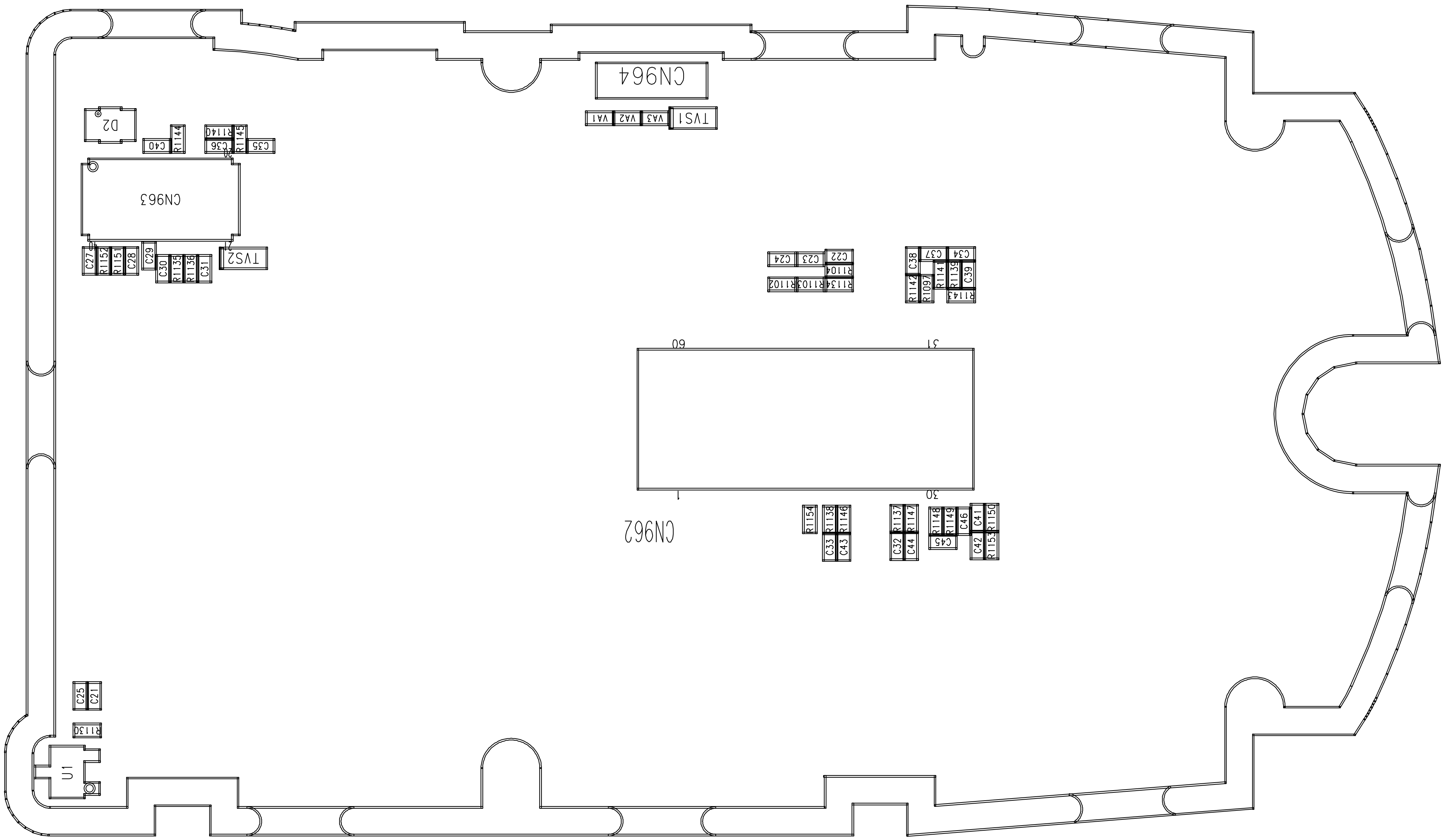
10. PCB LAYOUT



10. PCB LAYOUT

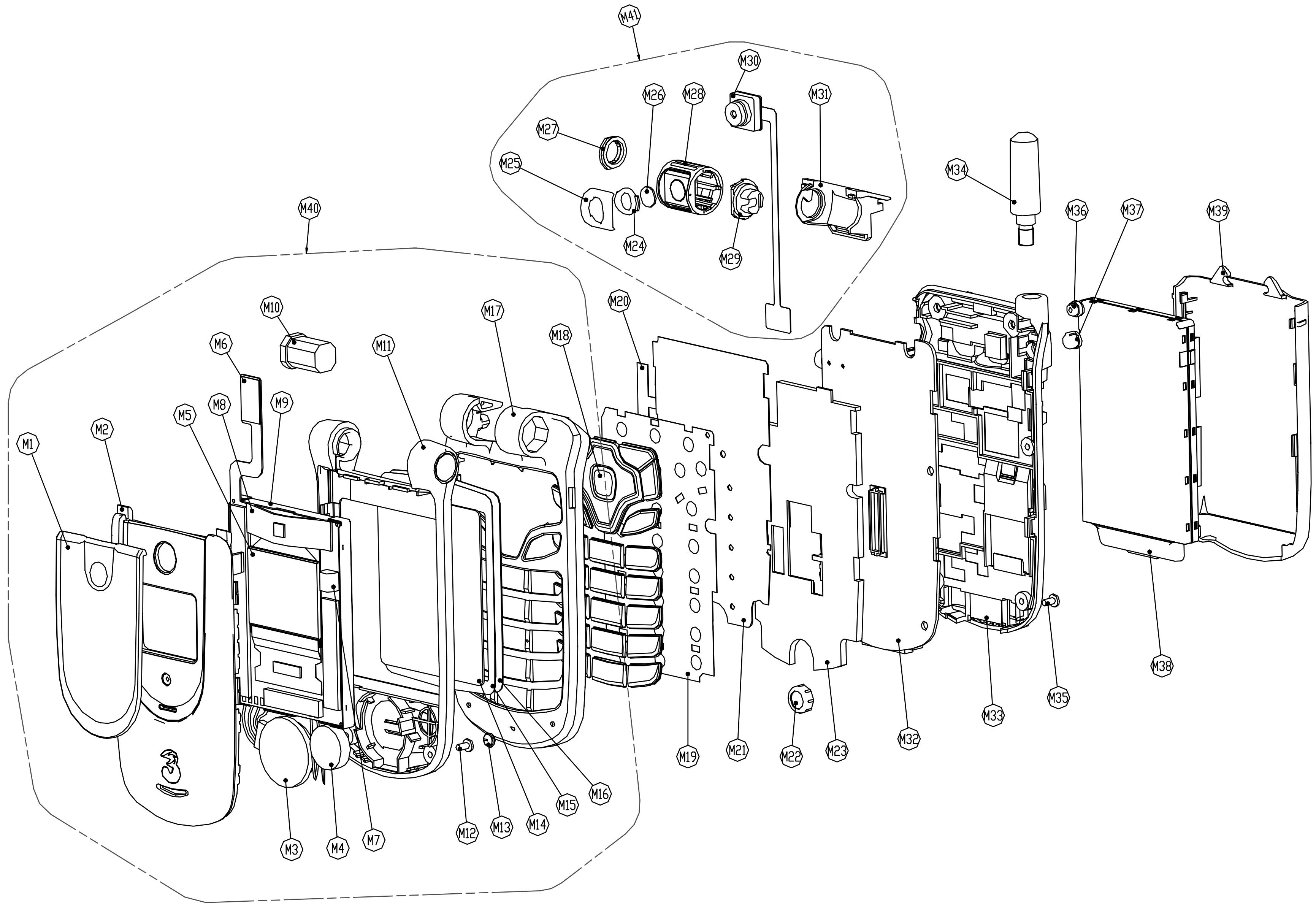


10. PCB LAYOUT



11. EXPLODED VIEW & REPLACEMENT PART LIST

11.1 EXPLODED VIEW



11.2 Replacement Parts
<Mechanic component>

Level	Location No.	Description	Part Number	Specification	SVC	Color	Remark
1		IMT,FOLDER	TIFF0001002		N	Silver	
2	ABEZ00	BOX ASSY	ABEZ0037901	BOX ASSY(for U8110 HUK)	N	Silver	
3	MBAD00	BAG,VINYL(PE)	MBAD0005201	BAG,VINYL(PE)_GSM Phone(LDPE 0.05t x 85 x 195)	Y	Dark Blue	
3	MBAZ00	BAG	MBAZ0002401	BAG(for G5300iVDF to pallet)(255*325)	Y	Silver	
3	MBEE00	BOX,MASTER	MBEE0044101	BOX,MASTER(for U8110 HUK)	N	Silver	
3	MBEF00	BOX,UNIT	MBEF0053401	BOX,UNIT(for U8110 HUK)	Y	Silver	
3	MLAJ00	LABEL,MASTER BOX	MLAJ0002201	LABEL,MASTER BOX(G4010 for Cingular)	N	Metalic Silver	
3	MLAQ00	LABEL,UNIT BOX	MLAQ0001601		Y	Dark Gray	
3	MPAD00	PACKING,SHELL	MPAD0004601	PACKING,SHELL(for U8110 HUK_Upper(Top))	Y	Silver	
3	MPAD01	PACKING,SHELL	MPAD0004602	PACKING,SHELL(for U8110 HUK_Lower(Bottom))	Y	Dark Blue	
3	MPBZ00	PAD	MPBZ0043101	PAD(for H3G_Substitute for H3G Manual)	Y	Dark Blue	
3	MPCY00	PALLET	MPCY0009501	PALLET(G7100 for Orange UK_EUR)	N	Black	
3	MPCY01	PALLET	MPCY0010901	PALLET(for H3G Main package_Cap)	N	Dark Blue	
3	MPCY02	PALLET	MPCY0010902	PALLET(for H3G Main package_Angle)	N	Dark Blue	
2	AMBA00	MANUAL ASSY,OPERATION	AMBA0030501	U8110 Manual ASSY for Hutchison in U.K.	Y		
3	MMBB00	MANUAL,OPERATION	MMBB0113401	U8110 User Manual for Hutchison in UK	Y		
2	APEY00	PHONE	APEY0070022	U8110 HUKSV	N	Silver	
3	ABGA00	BUTTON ASSY,DIAL	ABGA0002401		Y	Silver	M18
3	ACGG00	COVER ASSY,FOLDER	ACGG0033302		Y	Silver	M40
4	ACGH00	COVER ASSY,FOLDER(LOWER)	ACGH0012002		Y	Silver	M11
5	MCCZ00	CAP	MCCZ0005402		N		
5	MCJH00	COVER,FOLDER(LOWER)	MCJH0009603		N	Silver	
5	MDAC00	DECO,SIDE	MDAC0006301	0.2t	N	Silver	
5	MDAH	DECO,RECEIVER	MDAH0002001	INNER_2	N	Silver	
5	MDAH00	DECO,RECEIVER	MDAH0001901	OUTER DECO_1	N	Silver	
5	MGAD00	GASKET,SHIELD FORM	MGAD0035201	5.0x4.5x3.0 KW2000 FOLDER LOWER	Y	Gold	M7
5	MMAZ00	MAGNET	MMAZ0000101	D3*1.5t	Y		
5	MTAA	TAPE,DECO	MTAA0023301	DECO SIDE	Y		
5	MTAA00	TAPE,DECO	MTAA0023101	DECO RECEIVER OUTER	Y		
5	MTAA01	TAPE,DECO	MTAA0023201	DECO RECEIVER INNER	Y		
4	ACGJ00	COVER ASSY,FOLDER(UPPER)	ACGJ0028701		Y	Silver	M2
5	MCJJ00	COVER,FOLDER(UPPER)	MCJJ0021501		N	Silver	
5	MDAY00	DECO	MDAY0006801	0.2t	N		

Level	Location No.	Description	Part Number	Specification	SVC	Color	Remark
5	MFBC00	FILTER,SPEAKER	MFBC0007401		Y		
5	MICA00	INSERT,FRONT	MICA0001201	LG-G510,511,512 common use, DIA = 1.7mm+2.3t	Y		
5	MPBG00	PAD,LCD	MPBG0018201	2.2t	Y	Silver	
5	MPBQ00	PAD,LCD(SUB)	MPBQ0013101		Y	Black	
5	MTAE00	TAPE,WINDOW(SUB)	MTAE0013301	0.2t	Y		
4	ACGK00	COVER ASSY,FRONT	ACGK0020902		Y	Silver	M17
5	MBJL00	BUTTON,SIDE	MBJL0008102		N		
5	MCCC00	CAP,EARPHONE JACK	MCCC0007801		N	Silver	
5	MCJK00	COVER,FRONT	MCJK0014602		N	Silver	
5	MICB00	INSERT,FRONT(LOWER)	MICB0000601		N		
5	MWAG00	WINDOW,IRDA	MWAG0002301		N	Brown	
4	ALAY00	LCD ASSY	ALAY0005301		N		
5	AFBZ00	FRAME ASSY	AFBZ0004402		Y		M9
6	MFEZ00	FRAME	MFEZ0002302		N		
6	MPBG00	PAD,LCD	MPBG0010602	0.3t	N	Gray	
6	MPBS00	PAD,FOLDER	MPBS0002301	55.80*41.80 t0.3	N	Silver	
5	MGAD0	GASKET,SHIELD FORM	MGAD0044101	0.2t_LCD	Y	Silver	
5	MGAD00	GASKET,SHIELD FORM	MGAD0035201	5.0x4.5x3.0 KW2000 FOLDER LOWER	Y	Gold	
5	SACY00	PCB ASSY,FLEXIBLE	SACY0016001		Y		M8
6	EDLM00	DIODE,LED,MODULE	EDLM0004301	WHITE ,3 LED,3.5*3.5*1.0 ,R/TP ,MINI FLASH LED	Y		
6	R1	RES,CHIP	ERHY0000203	10 ohm,1/16W,J,1005,R/TP	Y		
6	R2	RES,CHIP	ERHY0000203	10 ohm,1/16W,J,1005,R/TP	Y		
6	R3	RES,CHIP	ERHY0000203	10 ohm,1/16W,J,1005,R/TP	Y		
6	SPCY00	PCB,FLEXIBLE	SPCY0026701	POLYI , mm,DOUBLE ,	Y		
4	AWAB00	WINDOW ASSY,LCD	AWAB0009201	IN-MOLD	Y	Dark Blue	M1
5	BFAA00	FILM,INMOLD	BFAA0014001	Dark Blue	N	Dark Blue	
5	MWAF00	WINDOW,LCD(SUB)	MWAF0017001		N	Dark Blue	
4	GMZZ00	SCREW MACHINE	GMZZ0003201	3.5 mm,3.5 mm,MSWR3(FN) ,N ,STR ,- , M1.7X3.5 DIA3.5	Y	Silver	M12
4	MCCH00	CAP,SCREW	MCCH0012101	FOLDER	Y	Gray	M13
4	MDAF00	DECO,FOLDER(LOWER)	MDAF0003203		Y	Metalic Silver	M16
4	MHFD00	HINGE,FOLDER	MHFD0006901		Y	Metalic Silver	M10
4	MTAA00	TAPE,DECO	MTAA0023401	DECO FOLDER LOWER	Y		M15
4	MTAB	TAPE,PROTECTION	MTAB0036801	KW2000, U8100, U8110, U8120	Y		
4	MTAB00	TAPE,PROTECTION	MTAB0020101	KW2000,FOLDER LOWER	Y		
4	MWAC00	WINDOW,LCD	MWAC0025801		Y		M14
4	SJMY00	VIBRATOR,MOTOR	SJMY0004201	3 V,0.12 A,12*3.4 ,G8000 VIBRATOR	Y		M4

Level	Location No.	Description	Part Number	Specification	SVC	Color	Remark
4	SUVT00	TWO-WAY MODE SPEAKER	SUVT0002701	8 ohm,32 ohm,90 dB,108 dB,19 mm,2-WAY MODE SPEAKER for KW-2000	Y		M3
4	SVLM00	LCD MODULE	SVLM0005401	, ,	Y		M5
3	ACGM00	COVER ASSY,REAR	ACGM0017802		Y	Silver	M33
4	ACFY00	CONTACT ASSY,ANTENNA	ACFY0000501	LG-G510,511,512 common use, MAIN REAR	Y		
4	MCJN00	COVER,REAR	MCJN0011802		Y	Silver	
4	MDAK00	DECO,REAR	MDAK0001102		Y	Silver	
4	MGAD00	GASKET,SHIELD FORM	MGAD0044101	0.2t_LCD	Y	Silver	M6
4	MIDZ	INSULATOR	MIDZ0039401		N	Dark Blue	
4	MIDZ00	INSULATOR	MIDZ0036101		N	Silver	
4	MLEA	LOCKER,BATTERY	MLEA0008901	RIGHT	N	Silver	
4	MLEA00	LOCKER,BATTERY	MLEA0008801	LEFT	N	Silver	
4	MPBT00	PAD,CAMERA	MPBT0004601	2.2t	Y	Silver	
4	MSDC00	SPRING,LOCKER	MSDC0003901		Y		
3	ACGN00	COVER ASSY,CAMERA	ACGN0001101		Y	Silver	M41
4	ACGP00	COVER ASSY,CAMERA(FRONT)	ACGP0000301		N	Silver	M28
5	MCJP00	COVER,CAMERA(FRONT)	MCJP0000901		N	Silver	
5	MMAZ00	MAGNET	MMAZ0000301	2500 Gauss (+-500)	N	Metalic Silver	
5	MSDZ00	SPRING	MSDZ0000801	0.15t	N	Gold	
5	MTAA00	TAPE,DECO	MTAA0035901		N	Silver	
4	MBIC00	BUSHING,CAMERA(LEFT)	MBIC0000201		N	White	M27
4	MBIZ00	BUSHING	MBIZ0001301		N	Silver	M31
4	MCCK00	CAP,CAMERA	MCCK0000301		N		M29
4	MDAD00	DECO,CAMERA	MDAD0002501		N	Black	M24
4	MDAD01	DECO,CAMERA	MDAD0002601	Cr	N	Metalic Silver	M25
4	MWAE00	WINDOW,CAMERA	MWAE0000301	0.5t	N		M26
4	SMZY00	MODULE,ETC	SMZY0006501	VGA CMOS CAMERA MODULE	Y		M30
3	GMZZ00	SCREW MACHINE	GMZZ0003201	3.5 mm,3.5 mm,MSWR3(FN) ,N ,STR ,- , M1.7X3.5 DIA3.5	Y	Silver	M35
3	MCCF00	CAP,MOBILE SWITCH	MCCF0008501		Y	Silver	M37
3	MCCH00	CAP,SCREW	MCCH0012201	REAR	Y	Silver	M36
3	MCJA00	COVER,BATTERY	MCJA0004202		Y	Silver	M39
3	MFEA00	FRAME,SHIELD	MFEA0003501		Y		M23
3	MLAK00	LABEL,MODEL	MLAK0007202		Y	Silver	

11.2 Replacement Parts
<Main component>

Level	Location No.	Description	Part Number	Specification	SVC	Color	Remark
3	SAEY00	PCB ASSY,KEYPAD	SAEY0025801		Y		M21
4	ADCA00	DOME ASSY,METAL	ADCA0010901		N		M19
4	SAEA00	PCB ASSY,KEYPAD,AUTO	SAEA0010301		N		
5	C21	CAP,CERAMIC,CHIP	ECCH0000110	10 pF,50V,D,NP0,TC,1005,R/TP	N		
5	C22	CAP,CERAMIC,CHIP	ECCH0000139	470 pF,50V,K,X7R,HD,1005,R/TP	N		
5	C23	CAP,CERAMIC,CHIP	ECCH0000139	470 pF,50V,K,X7R,HD,1005,R/TP	N		
5	C24	CAP,CERAMIC,CHIP	ECCH0000139	470 pF,50V,K,X7R,HD,1005,R/TP	N		
5	C25	CAP,CERAMIC,CHIP	ECCH0000182	0.1 uF,10V ,K ,X5R ,HD ,1005 ,R/TP	N		
5	C26	CAP,CERAMIC,CHIP	ECCH0000182	0.1 uF,10V ,K ,X5R ,HD ,1005 ,R/TP	N		
5	C27	CAP,CERAMIC,CHIP	ECCH0000122	47 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C28	CAP,CERAMIC,CHIP	ECCH0000122	47 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C29	CAP,CERAMIC,CHIP	ECCH0000118	30 pF,50V,J,NP0,TC,1005,R/TP	Y		
5	C30	CAP,CERAMIC,CHIP	ECCH0000118	30 pF,50V,J,NP0,TC,1005,R/TP	Y		
5	C31	CAP,CERAMIC,CHIP	ECCH0000118	30 pF,50V,J,NP0,TC,1005,R/TP	Y		
5	C32	CAP,CERAMIC,CHIP	ECCH0000118	30 pF,50V,J,NP0,TC,1005,R/TP	Y		
5	C33	CAP,CERAMIC,CHIP	ECCH0000118	30 pF,50V,J,NP0,TC,1005,R/TP	Y		
5	C34	CAP,CERAMIC,CHIP	ECCH0000118	30 pF,50V,J,NP0,TC,1005,R/TP	Y		
5	C35	CAP,CERAMIC,CHIP	ECCH0000118	30 pF,50V,J,NP0,TC,1005,R/TP	Y		
5	C36	CAP,CERAMIC,CHIP	ECCH0000118	30 pF,50V,J,NP0,TC,1005,R/TP	Y		
5	C37	CAP,CERAMIC,CHIP	ECCH0000118	30 pF,50V,J,NP0,TC,1005,R/TP	Y		
5	C38	CAP,CERAMIC,CHIP	ECCH0000118	30 pF,50V,J,NP0,TC,1005,R/TP	Y		
5	C39	CAP,CERAMIC,CHIP	ECCH0000118	30 pF,50V,J,NP0,TC,1005,R/TP	Y		
5	C40	CAP,CERAMIC,CHIP	ECCH0000118	30 pF,50V,J,NP0,TC,1005,R/TP	Y		
5	C41	CAP,CERAMIC,CHIP	ECCH0000118	30 pF,50V,J,NP0,TC,1005,R/TP	Y		
5	C42	CAP,CERAMIC,CHIP	ECCH0000122	47 pF,50V,J,NP0,TC,1005,R/TP	Y		
5	C43	CAP,CERAMIC,CHIP	ECCH0000118	30 pF,50V,J,NP0,TC,1005,R/TP	Y		
5	C44	CAP,CERAMIC,CHIP	ECCH0000118	30 pF,50V,J,NP0,TC,1005,R/TP	Y		
5	C45	CAP,CERAMIC,CHIP	ECCH0000118	30 pF,50V,J,NP0,TC,1005,R/TP	Y		
5	C46	CAP,CERAMIC,CHIP	ECCH0000118	30 pF,50V,J,NP0,TC,1005,R/TP	Y		
5	CN962	CONNECTOR,BOARD TO BOARD	ENBY0004302	60 PIN,0.5 mm,STRAIGHT ,Au ,B to B CNT(Socket)	N		
5	CN963	CONNECTOR,BOARD TO BOARD	ENBY0013004	40 PIN,0.4 mm,ETC ,Au over Ni ,	N		
5	D1	DIODE,SWITCHING	EDSY0010401	1-1G1A ,40 V,300 A,R/TP ,Silicon Epitaxial Schottky Barrier Type Diode	N		
5	LD1	DIODE,LED,CHIP	EDLH0004502	BLUE ,1608 ,R/TP ,0.35T	Y		
5	LD10	DIODE,LED,CHIP	EDLH0004502	BLUE ,1608 ,R/TP ,0.35T	Y		
5	LD11	DIODE,LED,CHIP	EDLH0004502	BLUE ,1608 ,R/TP ,0.35T	Y		
5	LD12	DIODE,LED,CHIP	EDLH0004502	BLUE ,1608 ,R/TP ,0.35T	Y		

Level	Location No.	Description	Part Number	Specification	SVC	Color	Remark
5	LD13	DIODE,LED,CHIP	EDLH0004502	BLUE ,1608 ,R/TP ,0.35T	Y		
5	LD14	DIODE,LED,CHIP	EDLH0004502	BLUE ,1608 ,R/TP ,0.35T	Y		
5	LD16	DIODE,LED,CHIP	EDLH0004502	BLUE ,1608 ,R/TP ,0.35T	Y		
5	LD17	DIODE,LED,CHIP	EDLH0004502	BLUE ,1608 ,R/TP ,0.35T	Y		
5	LD18	DIODE,LED,CHIP	EDLH0004502	BLUE ,1608 ,R/TP ,0.35T	Y		
5	LD19	DIODE,LED,CHIP	EDLH0004502	BLUE ,1608 ,R/TP ,0.35T	Y		
5	LD2	DIODE,LED,CHIP	EDLH0004502	BLUE ,1608 ,R/TP ,0.35T	Y		
5	LD20	DIODE,LED,CHIP	EDLH0004502	BLUE ,1608 ,R/TP ,0.35T	Y		
5	LD3	DIODE,LED,CHIP	EDLH0004502	BLUE ,1608 ,R/TP ,0.35T	Y		
5	LD4	DIODE,LED,CHIP	EDLH0004502	BLUE ,1608 ,R/TP ,0.35T	Y		
5	LD5	DIODE,LED,CHIP	EDLH0004502	BLUE ,1608 ,R/TP ,0.35T	Y		
5	LD6	DIODE,LED,CHIP	EDLH0004502	BLUE ,1608 ,R/TP ,0.35T	Y		
5	LD7	DIODE,LED,CHIP	EDLH0004502	BLUE ,1608 ,R/TP ,0.35T	Y		
5	LD8	DIODE,LED,CHIP	EDLH0004502	BLUE ,1608 ,R/TP ,0.35T	Y		
5	LD9	DIODE,LED,CHIP	EDLH0004502	BLUE ,1608 ,R/TP ,0.35T	Y		
5	R1098	RES,CHIP	ERHY0006603	36 ohm,1/16W ,J ,1005 ,R/TP	N		
5	R1099	RES,CHIP	ERHY0006603	36 ohm,1/16W ,J ,1005 ,R/TP	N		
5	R1100	RES,CHIP	ERHY0006603	36 ohm,1/16W ,J ,1005 ,R/TP	N		
5	R1102	RES,CHIP	ERHY0000233	470 ohm,1/16W,J,1005,R/TP	N		
5	R1103	RES,CHIP	ERHY0000233	470 ohm,1/16W,J,1005,R/TP	N		
5	R1104	RES,CHIP	ERHY0000233	470 ohm,1/16W,J,1005,R/TP	N		
5	R1130	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP	N		
5	R1131	RES,CHIP	ERHY0006603	36 ohm,1/16W ,J ,1005 ,R/TP	N		
5	R1133	RES,CHIP	ERHY0000213	47 ohm,1/16W,J,1005,R/TP	N		
5	R1134	RES,CHIP	ERHY0000220	100 ohm,1/16W,J,1005,R/TP	Y		
5	R1135	RES,CHIP	ERHY0000220	100 ohm,1/16W,J,1005,R/TP	Y		
5	R1136	RES,CHIP	ERHY0000220	100 ohm,1/16W,J,1005,R/TP	Y		
5	R1137	RES,CHIP	ERHY0000220	100 ohm,1/16W,J,1005,R/TP	Y		
5	R1138	RES,CHIP	ERHY0000220	100 ohm,1/16W,J,1005,R/TP	Y		
5	R1139	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	Y		
5	R1140	RES,CHIP	ERHY0000220	100 ohm,1/16W,J,1005,R/TP	Y		
5	R1141	RES,CHIP	ERHY0000220	100 ohm,1/16W,J,1005,R/TP	Y		
5	R1142	RES,CHIP	ERHY0000220	100 ohm,1/16W,J,1005,R/TP	Y		
5	R1143	RES,CHIP	ERHY0000220	100 ohm,1/16W,J,1005,R/TP	Y		
5	R1144	RES,CHIP	ERHY0000220	100 ohm,1/16W,J,1005,R/TP	Y		
5	R1145	RES,CHIP	ERHY0000220	100 ohm,1/16W,J,1005,R/TP	Y		
5	R1146	RES,CHIP	ERHY0000220	100 ohm,1/16W,J,1005,R/TP	Y		
5	R1147	RES,CHIP	ERHY0000220	100 ohm,1/16W,J,1005,R/TP	Y		
5	R1148	RES,CHIP	ERHY0000220	100 ohm,1/16W,J,1005,R/TP	Y		

Level	Location No.	Description	Part Number	Specification	SVC	Color	Remark
5	R1149	RES,CHIP	ERHY0000220	100 ohm,1/16W,J,1005,R/TP	Y		
5	R1150	RES,CHIP	ERHY0000220	100 ohm,1/16W,J,1005,R/TP	Y		
5	R1151	RES,CHIP	ERHY0000228	270 ohm,1/16W,J,1005,R/TP	N		
5	R1152	RES,CHIP	ERHY0000228	270 ohm,1/16W,J,1005,R/TP	N		
5	R1153	RES,CHIP	ERHY0000228	270 ohm,1/16W,J,1005,R/TP	Y		
5	R1154	RES,CHIP	ERHY0000233	470 ohm,1/16W,J,1005,R/TP	Y		
5	SPEY00	PCB,KEYPAD	SPEY0019202	FR-4 ,.4 mm,DOUBLE ,	N		
5	TVS1	DIODE,TVS	EDTY0007301	SOD-523 ,5 V,240 W,R/TP ,SINGLE LINE TVS DIODE FOR ESD	N		
5	TVS2	DIODE,TVS	EDTY0007301	SOD-523 ,5 V,240 W,R/TP ,SINGLE LINE TVS DIODE FOR ESD	N		
5	U1	IC	EUSY0129501	SC-74A FIT ,3 PIN,R/TP ,HALL EFFECT SWITCH	N		
5	VA1	VARISTOR	SEVY0000702	14 V,10% ,SMD ,	N		
5	VA2	VARISTOR	SEVY0000702	14 V,10% ,SMD ,	N		
5	VA3	VARISTOR	SEVY0000702	14 V,10% ,SMD ,	N		
4	SAKY00	PCB ASSY,SIDEKEY	SAKY0002602		N		M20
3	SAFY00	PCB ASSY,MAIN	SAFY0084201		Y		M32
4	MLAB00	LABEL,A/S	MLAB0000601	HUMIDITY STICKER	Y		
4	SAFA00	PCB ASSY,MAIN,AUTO	SAFA0031301		N		
5	B1501	IC	EUSY0170601	SC70 ,5 PIN,R/TP ,TEMPERATURE SENSOR	N		
5	B1770	X-TAL	EXXY0016801	13 MHz,19 PPM,10 pF,40 ohm,SMD ,5*3.20*0.7 ,	Y		
5	B2100	X-TAL	EXXY0004601	0.32768 MHz,20 PPM,12.5 pF,65000 ohm,SMD ,6.9*1.4*1.3 ,	Y		
5	C1000	CAP,CERAMIC,CHIP	ECCH0001001	6.8 pF,50V ,C ,NP0 ,TC ,1005 ,R/TP	Y		
5	C1001	CAP,CERAMIC,CHIP	ECCH0000110	10 pF,50V,D,NP0,TC,1005,R/TP	N		
5	C1002	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP	N		
5	C1003	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP	N		
5	C1004	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP	N		
5	C1005	CAP,CERAMIC,CHIP	ECCH0000110	10 pF,50V,D,NP0,TC,1005,R/TP	N		
5	C1007	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP	N		
5	C1008	CAP,CERAMIC,CHIP	ECCH0000110	10 pF,50V,D,NP0,TC,1005,R/TP	N		
5	C1009	CAP,CERAMIC,CHIP	ECCH0000110	10 pF,50V,D,NP0,TC,1005,R/TP	N		
5	C1010	CAP,CERAMIC,CHIP	ECCH0000143	1 nF,50V,K,X7R,HD,1005,R/TP	N		
5	C1011	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C1012	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C1013	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C1100	CAP,CERAMIC,CHIP	ECCH0000110	10 pF,50V,D,NP0,TC,1005,R/TP	N		
5	C1101	CAP,CERAMIC,CHIP	ECCH0000110	10 pF,50V,D,NP0,TC,1005,R/TP	N		
5	C1102	CAP,CERAMIC,CHIP	ECCH0000110	10 pF,50V,D,NP0,TC,1005,R/TP	N		
5	C1103	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C1104	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP	N		

Level	Location No.	Description	Part Number	Specification	SVC	Color	Remark
5	C1110	CAP,CERAMIC,CHIP	ECCH0000186	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	N		
5	C1111	CAP,CERAMIC,CHIP	ECCH0000186	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	N		
5	C1112	CAP,CERAMIC,CHIP	ECCH0000186	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	N		
5	C1113	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C1114	CAP,CERAMIC,CHIP	ECCH0000108	7 pF,50V,D,NP0,TC,1005,R/TP	N		
5	C1140	CAP,CERAMIC,CHIP	ECCH0000165	68 nF,6.3V,K,X5R,HD,1005,R/TP	N		
5	C1141	CAP,CERAMIC,CHIP	ECCH0000165	68 nF,6.3V,K,X5R,HD,1005,R/TP	N		
5	C1142	CAP,CERAMIC,CHIP	ECCH0000165	68 nF,6.3V,K,X5R,HD,1005,R/TP	N		
5	C1143	CAP,CERAMIC,CHIP	ECCH0000165	68 nF,6.3V,K,X5R,HD,1005,R/TP	N		
5	C1144	CAP,CERAMIC,CHIP	ECCH0000165	68 nF,6.3V,K,X5R,HD,1005,R/TP	N		
5	C1150	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP	N		
5	C1156	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP	N		
5	C1201	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP	N		
5	C1202	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP	N		
5	C1203	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C1205	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C1221	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP	N		
5	C1222	CAP,CERAMIC,CHIP	ECCH0000140	560 pF,50V,K,X7R,HD,1005,R/TP	N		
5	C1223	CAP,CERAMIC,CHIP	ECCH0000137	330 pF,50V ,K ,X7R ,HD ,1005 ,R/TP	N		
5	C1224	CAP,CERAMIC,CHIP	ECCH0000144	1.2 nF,50V,K,X7R,HD,1005,R/TP	N		
5	C1225	CAP,CERAMIC,CHIP	ECCH0000146	1.8 nF,50V,K,X7R,HD,1005,R/TP	N		
5	C1270	CAP,CERAMIC,CHIP	ECCH0000143	1 nF,50V,K,X7R,HD,1005,R/TP	N		
5	C1271	CAP,CERAMIC,CHIP	ECCH0000143	1 nF,50V,K,X7R,HD,1005,R/TP	N		
5	C1300	CAP,CERAMIC,CHIP	ECCH0000165	68 nF,6.3V,K,X5R,HD,1005,R/TP	N		
5	C1311	CAP,CERAMIC,CHIP	ECCH0006501	10 uF,6.3V ,K ,X5R ,TC ,2012 ,R/TP	Y		
5	C1312	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP	N		
5	C1313	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C1315	CAP,CERAMIC,CHIP	ECCH0006501	10 uF,6.3V ,K ,X5R ,TC ,2012 ,R/TP	Y		
5	C1320	CAP,CERAMIC,CHIP	ECCH0000139	470 pF,50V,K,X7R,HD,1005,R/TP	N		
5	C1321	CAP,CERAMIC,CHIP	ECCH0000139	470 pF,50V,K,X7R,HD,1005,R/TP	N		
5	C1322	CAP,CERAMIC,CHIP	ECCH0000130	150 pF,50V,J,SL,TC,1005,R/TP	N		
5	C1323	CAP,CERAMIC,CHIP	ECCH0000144	1.2 nF,50V,K,X7R,HD,1005,R/TP	N		
5	C1324	CAP,CERAMIC,CHIP	ECCH0000128	100 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C1325	CAP,CERAMIC,CHIP	ECCH0000128	100 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C1327	CAP,CERAMIC,CHIP	ECCH0000186	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	N		
5	C1330	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C1331	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C1332	CAP,CERAMIC,CHIP	ECCH0000186	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	N		
5	C1333	CAP,CERAMIC,CHIP	ECCH0000110	10 pF,50V,D,NP0,TC,1005,R/TP	N		

Level	Location No.	Description	Part Number	Specification	SVC	Color	Remark
5	C1334	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C1335	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C1341	CAP,CERAMIC,CHIP	ECCH0000186	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP	N		
5	C1352	CAP,CERAMIC,CHIP	ECCH0000110	10 pF,50V,D,NP0,TC,1005,R/TP	N		
5	C1401	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C1402	CAP,CERAMIC,CHIP	ECCH0000143	1 nF,50V,K,X7R,HD,1005,R/TP	N		
5	C1403	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C1404	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP	N		
5	C1407	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C1412	CAP,CERAMIC,CHIP	ECCH0000701	1.2 pF,50V ,C ,NP0 ,TC ,1005 ,R/TP	N		
5	C1413	CAP,CERAMIC,CHIP	ECCH0000701	1.2 pF,50V ,C ,NP0 ,TC ,1005 ,R/TP	N		
5	C1414	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C1422	CAP,CERAMIC,CHIP	ECCH0000117	27 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C1423	CAP,CERAMIC,CHIP	ECCH0000117	27 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C1424	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C1425	CAP,CERAMIC,CHIP	ECCH0000147	2.2 nF,50V,K,X7R,HD,1005,R/TP	N		
5	C1431	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C1441	CAP,CERAMIC,CHIP	ECCH0000147	2.2 nF,50V,K,X7R,HD,1005,R/TP	N		
5	C1442	CAP,CERAMIC,CHIP	ECCH0000147	2.2 nF,50V,K,X7R,HD,1005,R/TP	N		
5	C1443	CAP,CERAMIC,CHIP	ECCH0000701	1.2 pF,50V ,C ,NP0 ,TC ,1005 ,R/TP	N		
5	C1444	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C1447	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP	N		
5	C1448	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP	N		
5	C1451	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP	N		
5	C1452	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP	N		
5	C1453	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP	N		
5	C1454	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP	N		
5	C1501	CAP,CERAMIC,CHIP	ECCH0000122	47 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C1502	CAP,CERAMIC,CHIP	ECCH0000105	4 pF,50V,C,NP0,TC,1005,R/TP	N		
5	C1503	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C1504	CAP,CERAMIC,CHIP	ECCH0000110	10 pF,50V,D,NP0,TC,1005,R/TP	N		
5	C1505	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C1507	CAP,CERAMIC,CHIP	ECCH0000105	4 pF,50V,C,NP0,TC,1005,R/TP	N		
5	C1508	CAP,CERAMIC,CHIP	ECCH0000901	2.2 pF,50V ,C ,NP0 ,TC ,1005 ,R/TP	N		
5	C1509	CAP,CERAMIC,CHIP	ECCH0000110	10 pF,50V,D,NP0,TC,1005,R/TP	N		
5	C1510	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP	N		
5	C1511	CAP,CERAMIC,CHIP	ECCH0000110	10 pF,50V,D,NP0,TC,1005,R/TP	N		
5	C1512	CAP,CERAMIC,CHIP	ECCH0000110	10 pF,50V,D,NP0,TC,1005,R/TP	N		
5	C1513	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP	N		

Level	Location No.	Description	Part Number	Specification	SVC	Color	Remark
5	C1514	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP	N		
5	C1601	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP	N		
5	C1602	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C1622	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C1623	CAP,CERAMIC,CHIP	ECCH0006501	10 uF,6.3V ,K ,X5R ,TC ,2012 ,R/TP	Y		
5	C1624	CAP,CERAMIC,CHIP	ECCH0003803	4.7 uF,10V ,Z ,Y5V ,HD ,2012 ,R/TP	N		
5	C1626	CAP,CERAMIC,CHIP	ECCH0000137	330 pF,50V ,K ,X7R ,HD ,1005 ,R/TP	N		
5	C1627	CAP,CERAMIC,CHIP	ECCH0003803	4.7 uF,10V ,Z ,Y5V ,HD ,2012 ,R/TP	N		
5	C1628	CAP,CERAMIC,CHIP	ECCH0000143	1 nF,50V,K,X7R,HD,1005,R/TP	N		
5	C1631	CAP,CERAMIC,CHIP	ECCH0000110	10 pF,50V,D,NP0,TC,1005,R/TP	N		
5	C1632	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP	N		
5	C1701	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP	N		
5	C1702	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C1703	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP	N		
5	C1704	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C1710	CAP,CERAMIC,CHIP	ECCH0000130	150 pF,50V,J,SL,TC,1005,R/TP	N		
5	C1711	CAP,CERAMIC,CHIP	ECCH0000149	3.3 nF,50V,K,X7R,HD,1005,R/TP	N		
5	C1714	CAP,CERAMIC,CHIP	ECCH0000128	100 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C1715	CAP,CERAMIC,CHIP	ECCH0000128	100 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C1716	CAP,CERAMIC,CHIP	ECCH0000181	4.7 pF,50V ,C ,NP0 ,TC ,1005 ,R/TP	N		
5	C1720	CAP,CERAMIC,CHIP	ECCH0000152	5.6 nF,25V,K,X7R,HD,1005,R/TP	N		
5	C1721	CAP,CERAMIC,CHIP	ECCH0000138	390 pF,50V,K,X7R,HD,1005,R/TP	N		
5	C1730	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP	N		
5	C1731	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C1740	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP	N		
5	C1741	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C1750	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C1751	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C1760	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP	N		
5	C1761	CAP,CERAMIC,CHIP	ECCH0000127	82 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C1770	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP	N		
5	C1772	CAP,CERAMIC,CHIP	ECCH0000137	330 pF,50V ,K ,X7R ,HD ,1005 ,R/TP	N		
5	C1773	CAP,CERAMIC,CHIP	ECCH0000181	4.7 pF,50V ,C ,NP0 ,TC ,1005 ,R/TP	N		
5	C1776	CAP,CERAMIC,CHIP	ECCH0000181	4.7 pF,50V ,C ,NP0 ,TC ,1005 ,R/TP	N		
5	C1777	CAP,CERAMIC,CHIP	ECCH0000122	47 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C1778	CAP,CERAMIC,CHIP	ECCH0000124	56 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C1800	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C1801	CAP,CERAMIC,CHIP	ECCH0000143	1 nF,50V,K,X7R,HD,1005,R/TP	N		
5	C1802	CAP,CERAMIC,CHIP	ECCH0006501	10 uF,6.3V ,K ,X5R ,TC ,2012 ,R/TP	Y		

Level	Location No.	Description	Part Number	Specification	SVC	Color	Remark
5	C1810	CAP,CERAMIC,CHIP	ECCH0006501	10 uF,6.3V ,K ,X5R ,TC ,2012 ,R/TP	Y		
5	C1811	CAP,CERAMIC,CHIP	ECCH0006501	10 uF,6.3V ,K ,X5R ,TC ,2012 ,R/TP	N		
5	C1850	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C1851	CAP,CERAMIC,CHIP	ECCH0000161	33 nF,16V,K,X7R,HD,1005,R/TP	N		
5	C1852	CAP,CERAMIC,CHIP	ECCH0006501	10 uF,6.3V ,K ,X5R ,TC ,2012 ,R/TP	Y		
5	C2100	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C2101	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C2102	CAP,CERAMIC,CHIP	ECCH0000137	330 pF,50V ,K ,X7R ,HD ,1005 ,R/TP	N		
5	C2103	CAP,CERAMIC,CHIP	ECCH0000137	330 pF,50V ,K ,X7R ,HD ,1005 ,R/TP	N		
5	C2104	CAP,CERAMIC,CHIP	ECCH0000143	1 nF,50V,K,X7R,HD,1005,R/TP	N		
5	C2200	CAP,CERAMIC,CHIP	ECCH0006501	10 uF,6.3V ,K ,X5R ,TC ,2012 ,R/TP	Y		
5	C2202	CAP,CERAMIC,CHIP	ECCH0003803	4.7 uF,10V ,Z ,Y5V ,HD ,2012 ,R/TP	N		
5	C2203	CAP,CERAMIC,CHIP	ECCH0000276	1 uF,10V,Z,Y5V,HD,1608,R/TP	N		
5	C2205	CAP,CERAMIC,CHIP	ECCH0006501	10 uF,6.3V ,K ,X5R ,TC ,2012 ,R/TP	Y		
5	C2206	CAP,CERAMIC,CHIP	ECCH0006501	10 uF,6.3V ,K ,X5R ,TC ,2012 ,R/TP	Y		
5	C2207	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2208	CAP,CERAMIC,CHIP	ECCH0000276	1 uF,10V,Z,Y5V,HD,1608,R/TP	N		
5	C2209	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2210	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2211	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2212	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2213	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2214	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2215	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2216	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2217	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2218	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2219	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2220	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2221	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2222	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2223	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2224	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2225	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2226	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2227	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2228	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2229	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2230	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		

Level	Location No.	Description	Part Number	Specification	SVC	Color	Remark
5	C2231	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2232	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2233	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2234	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2235	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2236	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2237	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2238	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2239	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2240	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2241	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2242	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2243	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2244	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2245	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2246	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2247	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2250	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2251	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2252	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2253	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2255	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2256	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2257	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2258	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2259	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2260	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2261	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2262	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2263	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2272	CAP,CERAMIC,CHIP	ECCH0000276	1 uF,10V,Z,Y5V,HD,1608,R/TP	N		
5	C2274	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2276	CAP,CERAMIC,CHIP	ECCH0000128	100 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C2277	CAP,CERAMIC,CHIP	ECCH0003803	4.7 uF,10V ,Z ,Y5V ,HD ,2012 ,R/TP	N		
5	C2278	CAP,CERAMIC,CHIP	ECCH0000380	2.2 uF,16V ,Z ,Y5V ,HD ,2012 ,R/TP	N		
5	C2279	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP	N		
5	C2281	CAP,CERAMIC,CHIP	ECCH0003803	4.7 uF,10V ,Z ,Y5V ,HD ,2012 ,R/TP	N		
5	C2301	CAP,CERAMIC,CHIP	ECCH0000276	1 uF,10V,Z,Y5V,HD,1608,R/TP	N		
5	C2302	CAP,CERAMIC,CHIP	ECCH0000276	1 uF,10V,Z,Y5V,HD,1608,R/TP	N		

Level	Location No.	Description	Part Number	Specification	SVC	Color	Remark
5	C2303	CAP,CERAMIC,CHIP	ECCH0000143	1 nF,50V,K,X7R,HD,1005,R/TP	N		
5	C2304	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2312	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C2400	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2500	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2603	CAP,CERAMIC,CHIP	ECCH0000276	1 uF,10V,Z,Y5V,HD,1608,R/TP	N		
5	C2604	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2605	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2606	CAP,CERAMIC,CHIP	ECCH0000275	0.33 uF,16V,Z,Y5V,HD,1608,R/TP	N		
5	C2608	CAP,CERAMIC,CHIP	ECCH0000276	1 uF,10V,Z,Y5V,HD,1608,R/TP	N		
5	C2609	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP	N		
5	C2610	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C2611	CAP,TANTAL,CHIP,MAKER	ECTZ0002802	100 uF,6.3V ,M ,L_ESR ,ETC ,R/TP	N		
5	C2612	CAP,CERAMIC,CHIP	ECCH0000165	68 nF,6.3V,K,X5R,HD,1005,R/TP	N		
5	C2613	CAP,CERAMIC,CHIP	ECCH0000161	33 nF,16V,K,X7R,HD,1005,R/TP	N		
5	C2614	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C2615	CAP,CERAMIC,CHIP	ECCH0000165	68 nF,6.3V,K,X5R,HD,1005,R/TP	N		
5	C2616	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C2617	CAP,CERAMIC,CHIP	ECCH0000165	68 nF,6.3V,K,X5R,HD,1005,R/TP	N		
5	C2618	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C2619	CAP,TANTAL,CHIP,MAKER	ECTZ0002802	100 uF,6.3V ,M ,L_ESR ,ETC ,R/TP	N		
5	C2621	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C2630	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C2631	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C2632	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C2633	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C3013	CAP,CERAMIC,CHIP	ECCH0003803	4.7 uF,10V ,Z ,Y5V ,HD ,2012 ,R/TP	N		
5	C3046	CAP,CERAMIC,CHIP	ECCH0000128	100 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C3051	CAP,CERAMIC,CHIP	ECCH0000380	2.2 uF,16V ,Z ,Y5V ,HD ,2012 ,R/TP	N		
5	C3052	CAP,CERAMIC,CHIP	ECCH0003803	4.7 uF,10V ,Z ,Y5V ,HD ,2012 ,R/TP	N		
5	C3133	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C3134	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C3135	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C3136	CAP,CERAMIC,CHIP	ECCH0000274	0.22 uF,16V,Z,Y5V,HD,1608,R/TP	N		
5	C3137	CAP,CERAMIC,CHIP	ECCH0000279	0.47 uF,10V ,Z ,Y5V ,HD ,1608 ,R/TP	N		
5	C3200	CAP,CERAMIC,CHIP	ECCH0000276	1 uF,10V,Z,Y5V,HD,1608,R/TP	N		
5	C3201	CAP,CERAMIC,CHIP	ECCH0000276	1 uF,10V,Z,Y5V,HD,1608,R/TP	N		
5	C3202	CAP,CERAMIC,CHIP	ECCH0006501	10 uF,6.3V ,K ,X5R ,TC ,2012 ,R/TP	Y		
5	C3203	CAP,CERAMIC,CHIP	ECCH0000276	1 uF,10V,Z,Y5V,HD,1608,R/TP	N		

Level	Location No.	Description	Part Number	Specification	SVC	Color	Remark
5	C3204	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C3205	CAP,CERAMIC,CHIP	ECCH0000110	10 pF,50V,D,NP0,TC,1005,R/TP	N		
5	C3212	CAP,CERAMIC,CHIP	ECCH0000143	1 nF,50V,K,X7R,HD,1005,R/TP	N		
5	C3213	CAP,CERAMIC,CHIP	ECCH0000143	1 nF,50V,K,X7R,HD,1005,R/TP	N		
5	C3215	CAP,TANTAL,CHIP,MAKER	ECTZ0000318	33 uF,10V ,M ,L_ESR ,ETC ,R/TP	N		
5	C3219	CAP,CERAMIC,CHIP	ECCH0000143	1 nF,50V,K,X7R,HD,1005,R/TP	N		
5	C3220	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C3221	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C3222	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C3225	CAP,CERAMIC,CHIP	ECCH0000274	0.22 uF,16V,Z,Y5V,HD,1608,R/TP	N		
5	C3243	CAP,CERAMIC,CHIP	ECCH0000139	470 pF,50V,K,X7R,HD,1005,R/TP	N		
5	C3244	CAP,CERAMIC,CHIP	ECCH0000380	2.2 uF,16V ,Z ,Y5V ,HD ,2012 ,R/TP	N		
5	C3245	CAP,TANTAL,CHIP,MAKER	ECTZ0003601	10 uF,10V ,M ,STD ,2012 ,R/TP	Y		
5	C3246	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C3247	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C3248	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	N		
5	C3249	CAP,CERAMIC,CHIP	ECCH0000114	20 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C3252	CAP,CERAMIC,CHIP	ECCH0000114	20 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C3255	CAP,CERAMIC,CHIP	ECCH0000114	20 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C3258	CAP,CERAMIC,CHIP	ECCH0000114	20 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C3259	CAP,CERAMIC,CHIP	ECCH0000114	20 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C3260	CAP,CERAMIC,CHIP	ECCH0000114	20 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C3261	CAP,CERAMIC,CHIP	ECCH0000114	20 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C3265	CAP,CERAMIC,CHIP	ECCH0000122	47 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C3266	CAP,CERAMIC,CHIP	ECCH0000110	10 pF,50V,D,NP0,TC,1005,R/TP	Y		
5	C3268	CAP,CERAMIC,CHIP	ECCH0000122	47 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C3269	CAP,CERAMIC,CHIP	ECCH0000122	47 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C3271	CAP,CERAMIC,CHIP	ECCH0000122	47 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C3272	CAP,CERAMIC,CHIP	ECCH0000122	47 pF,50V,J,NP0,TC,1005,R/TP	N		
5	C3276	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP	Y		
5	C3278	CAP,CERAMIC,CHIP	ECCH0000128	100 pF,50V,J,NP0,TC,1005,R/TP	Y		
5	D2000	IC	EUSY0135001	u289 BGA ,289 PIN,R/TP ,ASIC / BASEBAND CONTROLLER / MARITA	Y		
5	D2006	IC	EUSY0135201	u181 BGA ,181 PIN,R/TP ,ASIC / WCDMA AIR INTERFACE / WANDA	Y		
5	D2007	DIODE,TVS	EDTY0006701	CSP ,15 KV,200 mW,R/TP ,4 CHANNEL ESD ARRAY	N		
5	D2008	DIODE,TVS	EDTY0006701	CSP ,15 KV,200 mW,R/TP ,4 CHANNEL ESD ARRAY	N		
5	D2009	DIODE,TVS	EDTY0006701	CSP ,15 KV,200 mW,R/TP ,4 CHANNEL ESD ARRAY	N		

Level	Location No.	Description	Part Number	Specification	SVC	Color	Remark
5	D2010	DIODE,SWITCHING	EDSY0010401	1-1G1A ,40 V,300 A,R/TP ,Silicon Epitaxial Schottky Barrier Type Diode	N		
5	D2012	DIODE,SWITCHING	EDSY0010401	1-1G1A ,40 V,300 A,R/TP ,Silicon Epitaxial Schottky Barrier Type Diode	N		
5	D2013	DIODE,SWITCHING	EDSY0010401	1-1G1A ,40 V,300 A,R/TP ,Silicon Epitaxial Schottky Barrier Type Diode	N		
5	D2014	DIODE,SWITCHING	EDSY0010401	1-1G1A ,40 V,300 A,R/TP ,Silicon Epitaxial Schottky Barrier Type Diode	N		
5	D2015	DIODE,SWITCHING	EDSY0011901	EMD2 ,30 V,1 A,R/TP ,VF=1.5V(IF=200mA) , IR=30uA(VR=10V)	N		
5	D2016	DIODE,SWITCHING	EDSY0011901	EMD2 ,30 V,1 A,R/TP ,VF=1.5V(IF=200mA) , IR=30uA(VR=10V)	N		
5	D2018	DIODE,TVS	EDTY0006701	CSP ,15 KV,200 mW,R/TP ,4 CHANNEL ESD ARRAY	N		
5	FB1	FILTER,BEAD,CHIP	SFBH0002302	120 ohm,1608 ,CHIP BEAD, 2000mA	N		
5	FB2	FILTER,BEAD,CHIP	SFBH0002302	120 ohm,1608 ,CHIP BEAD, 2000mA	N		
5	FB3	FILTER,BEAD,CHIP	SFBH0008901	30 ohm,2012 ,3000mA, BEAD for LARGE CURRENT	Y		
5	FB4	FILTER,BEAD,CHIP	SFBH0008901	30 ohm,2012 ,3000mA, BEAD for LARGE CURRENT	Y		
5	L1001	INDUCTOR,CHIP	ELCH0005003	12 nH,J ,1005 ,R/TP ,	Y		
5	L1002	INDUCTOR,CHIP	ELCH0001407	5.6 nH,S,1005,R/TP	Y		
5	L1100	INDUCTOR,CHIP	ELCH0001420	3.9 nH,S ,1005 ,R/TP ,CDMA	N		
5	L1101	INDUCTOR,CHIP	ELCH0001405	3.3 nH,S,1005,R/TP	N		
5	L1110	INDUCTOR,CHIP	ELCH0001402	18 nH,J,1005,R/TP	N		
5	L1111	INDUCTOR,CHIP	ELCH0001001	10 nH,J,1005,R/TP	Y		
5	L1120	FILTER,BEAD,CHIP	SFBH0007103	75 ohm,1005 ,CHIP BEAD, 300mA	Y		
5	L1200	FILTER,BEAD,CHIP	SFBH0007103	75 ohm,1005 ,CHIP BEAD, 300mA	Y		
5	L1201	INDUCTOR,CHIP	ELCH0007404	5.6 uH,K ,1608 ,R/TP ,	N		
5	L1202	FILTER,BEAD,CHIP	SFBH0007103	75 ohm,1005 ,CHIP BEAD, 300mA	Y		
5	L1220	INDUCTOR,CHIP	ELCH0007403	100 uH,K ,2012 ,R/TP ,	N		
5	L1230	FILTER,BEAD,CHIP	SFBH0007103	75 ohm,1005 ,CHIP BEAD, 300mA	N		
5	L1300	FILTER,BEAD,CHIP	SFBH0007802	600 ohm,3216 ,CHIP FERRITE BEAD	N		
5	L1330	INDUCTOR,CHIP	ELCH0005006	33 nH,J ,1005 ,R/TP ,	N		
5	L1331	INDUCTOR,CHIP	ELCH0001401	15 nH,J,1005,R/TP	N		
5	L1332	FILTER,BEAD,CHIP	SFBH0007103	75 ohm,1005 ,CHIP BEAD, 300mA	N		
5	L1333	FILTER,BEAD,CHIP	SFBH0007103	75 ohm,1005 ,CHIP BEAD, 300mA	N		
5	L1340	INDUCTOR,CHIP	ELCH0005010	1.8 nH,S ,1005 ,R/TP ,	N		
5	L1350	INDUCTOR,CHIP	ELCH0001427	2.2 nH,S ,1005 ,R/TP ,	N		
5	L1401	INDUCTOR,CHIP	ELCH0001427	2.2 nH,S ,1005 ,R/TP ,	N		
5	L1411	INDUCTOR,CHIP	ELCH0001408	6.8 nH,S,1005,R/TP	N		
5	L1421	INDUCTOR,CHIP	ELCH0000716	68 nH,J,1608,R/TP	N		
5	L1422	INDUCTOR,CHIP	ELCH0000716	68 nH,J,1608,R/TP	N		
5	L1441	INDUCTOR,CHIP	ELCH0001511	100 nH,J,1608,R/TP	N		
5	L1501	INDUCTOR,CHIP	ELCH0001401	15 nH,J,1005,R/TP	N		

Level	Location No.	Description	Part Number	Specification	SVC	Color	Remark
5	L1502	INDUCTOR,CHIP	ELCH0001401	15 nH,J,1005,R/TP	N		
5	L1503	INDUCTOR,CHIP	ELCH0001407	5.6 nH,S,1005,R/TP	N		
5	L1504	INDUCTOR,CHIP	ELCH0001004	8.2 nH,J,1005,R/TP	N		
5	L1505	INDUCTOR,CHIP	ELCH0001001	10 nH,J,1005,R/TP	N		
5	L1507	FILTER,BEAD,CHIP	SFBH0007103	75 ohm,1005 ,CHIP BEAD, 300mA	N		
5	L1601	FILTER,BEAD,CHIP	SFBH0002302	120 ohm,1608 ,CHIP BEAD, 2000mA	N		
5	L1602	FILTER,BEAD,CHIP	SFBH0002302	120 ohm,1608 ,CHIP BEAD, 2000mA	N		
5	L1603	FILTER,BEAD,CHIP	SFBH0002302	120 ohm,1608 ,CHIP BEAD, 2000mA	N		
5	L1621	INDUCTOR,SMD,POWER	ELCP0005101	4.7 uH,M ,3.8*3.8*1.8 ,R/TP ,	N		
5	L1760	INDUCTOR,CHIP	ELCH0003811	1000 nH,K ,1608 ,R/TP ,COIL TYPE	N		
5	L2200	INDUCTOR,SMD,POWER	ELCP0004701	22 uH,M ,5.2*5.2*1.5 ,R/TP ,	N		
5	L2201	FILTER,BEAD,CHIP	SFBH0002302	120 ohm,1608 ,CHIP BEAD, 2000mA	N		
5	L2202	FILTER,BEAD,CHIP	SFBH0002302	120 ohm,1608 ,CHIP BEAD, 2000mA	N		
5	L2500	IC	EUSY0163501	SOT323-6L ,6 PIN,R/TP ,EMI FILTER & LINE TERMINATION for USB	N		
5	L2603	FILTER,BEAD,CHIP	SFBH0007103	75 ohm,1005 ,CHIP BEAD, 300mA	N		
5	L2605	FILTER,BEAD,CHIP	SFBH0007103	75 ohm,1005 ,CHIP BEAD, 300mA	N		
5	L2606	FILTER,BEAD,CHIP	SFBH0007103	75 ohm,1005 ,CHIP BEAD, 300mA	N		
5	L2608	FILTER,BEAD,CHIP	SFBH0007103	75 ohm,1005 ,CHIP BEAD, 300mA	N		
5	N1000	FILTER,SEPERATOR	SFAY0003101	900 ,2100 ,1.0 dB,1.4 dB,40 dB,40 dB,ETC ,5.2*4.0*1.8 ANTENNA SWITCH MODULE	N		
5	N1002	DUPLEXER,IMT	SDMY0000301	1950 MHz,2140 MHz,1.25 dB,2.0 dB,25 dB,15 dB,10*5.3*1.94 ,SMD ,	N		
5	N1100	IC	EUSY0132801	56 ball ,56 PIN,R/TP ,RFIC	Y		
5	N1101	IC	EUSY0133101	BGA64 ,64 PIN,R/TP ,U8000 RF IC	Y		
5	N1300	PAM	SMPY0002901	30 dBm,45 %,80 A,50 dBc,23.5 dB,11.6*9.1*1.5 ,SMD ,	Y		
5	N1330	TRANSFORMER,MATCHING	STMY0018402	6 PIN,SMD ,GSM Tx Balun	Y		
5	N1331	TRANSFORMER,MATCHING	STMY0018401	6 PIN,SMD ,DCS TX BALUN	Y		
5	N1400	IC	EUSY0133001	uBGA ,56 PIN,R/TP ,U8000 RF IC	Y		
5	N1620	IC	EUSY0136001	3 X 4 UCSP ,10 PIN,R/TP ,600 mA BUCK REGULATORS / DYNAMIC OUTPUT VOLTAGE	Y		
5	N1630	PAM	SMPY0002801	26 dBm,40 %,83 A,-58 dBc,23.5 dB,8.0*6.0*1.4 ,SMD ,	Y		
5	N1650	ISOLATOR,IMT	SQMY0000201	1950 MHz,4.0*4.0*1.9 ,SMD ,1920~1980MHz	N		
5	N1700	IC	EUSY0132901	56 ,56 PIN,R/TP ,WCDMA TXIC Wivi	Y		
5	N1850	IC	EUSY0122502	LLP-6 ,6 PIN,R/TP ,300mA CMOS LDO / 2.8V	Y		
5	N2000	IC	EUSY0132701	u143 BGA ,143 PIN,R/TP ,ASIC / POWER MANAGEMENT IC / VINCENNE	Y		
5	N2203	IC	EUSY0122402	SC-82AB ,4 PIN,R/TP ,CMOS LDO 1.5V OUTPUT/ 2.0 X 2.1	Y		
5	N2204	IC	EUSY0171302	SOT-23 ,5 PIN,R/TP ,150mA 3.3V LDO	Y		
5	N2300	IC	EUSY0171401	CSP ,20 PIN,R/TP ,7 CHANNEL ESD FILTER ARRAY, KNATTE	N		

Level	Location No.	Description	Part Number	Specification	SVC	Color	Remark
5	N2601	IC	EUSY0196101	BUMP MICRO SMD ,9 PIN,R/TP ,1W AUDIO AMP	Y		
5	N2602	IC	EUSY0171201	CSP ,25 PIN,R/TP ,6 CHANNEL ESD FILTER, EMP SOLUTION	Y		
5	N2603	IC	EUSY0148801	SOT23-6 ,6 PIN,R/TP ,SPST SWITCH / 2 OHM	Y		
5	N3000	IC	EUSY0171301	SOT-23 ,5 PIN,R/TP ,150mA 2.8V LDO	Y		
5	N3100	IC	EUSY0122301	SURFACE MOUNT ,7 PIN,R/TP ,IRDA DATA 1.3 LOW POWER TRANSCEIVER / 115.2kb/s	Y		
5	N3200	IC	EUSY0129501	SC-74A FIT ,3 PIN,R/TP ,HALL EFFECT SWITCH	Y		
5	N3201	IC	EUSY0088502	MSOP-10 ,10 PIN,R/TP ,CHARGER PUMP // LED DRIVER / 4.5V 120mA	Y		
5	PT1	THERMISTOR	SETY0005701	NTC ,47 Kohm,SMD ,F GRADE	Y		
5	Q2100	TR,BJT,NPN	EQBN0013301	2-2H1A ,100 mW,R/TP ,VEBO=6V	N		
5	Q2200	TR,FET,P-CHANNEL	EQFP0003601	SOT-363 ,0.27 W,20 V,0.66 A,R/TP ,Dual(P-channel:PD=0.27W,VDS=-8V,ID=0.57	N		
5	Q2201	TR,FET,P-CHANNEL	EQFP0004401	1206-8 chipFET ,2.5 W,-20 V,20 A,R/TP ,3.10*1.975*1.1(t)	N		
5	Q2300	TR,BJT,NPN	EQBN0013301	2-2H1A ,100 mW,R/TP ,VEBO=6V	N		
5	Q3200	TR,BJT,NPN	EQBN0013701	EMT6 ,150 mW,R/TP ,DUAL TRANSISTORS	N		
5	Q3202	TR,BJT,NPN	EQBN0014901	SOT323 ,200 mW,R/TP ,NPN SWITCHING TR	N		
5	Q3203	TR,BJT,PNP	EQBP0002401	EMT3 ,.201 W,R/TP ,	N		
5	Q3204	TR,BJT,NPN	EQBN0014901	SOT323 ,200 mW,R/TP ,NPN SWITCHING TR	N		
5	R1003	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1004	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1005	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1006	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1007	RES,CHIP	ERHY0000214	51 ohm,1/16W,J,1005,R/TP	N		
5	R1103	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1104	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1105	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1106	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1113	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1140	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP	N		
5	R1150	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1151	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1210	RES,CHIP	ERHY0000220	100 ohm,1/16W,J,1005,R/TP	N		
5	R1211	RES,CHIP	ERHY0000220	100 ohm,1/16W,J,1005,R/TP	N		
5	R1212	RES,CHIP	ERHY0000220	100 ohm,1/16W,J,1005,R/TP	N		
5	R1213	RES,CHIP	ERHY0000220	100 ohm,1/16W,J,1005,R/TP	N		
5	R1220	RES,CHIP	ERHY0000235	560 ohm,1/16W,J,1005,R/TP	N		
5	R1222	RES,CHIP	ERHY0000222	120 ohm,1/16W,J,1005,R/TP	N		
5	R1223	RES,CHIP	ERHY0000231	390 ohm,1/16W,J,1005,R/TP	N		
5	R1224	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		

Level	Location No.	Description	Part Number	Specification	SVC	Color	Remark
5	R1240	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1250	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1301	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1302	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1320	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1321	RES,CHIP	ERHY0000241	1K ohm,1/16W,J,1005,R/TP	N		
5	R1325	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1326	RES,CHIP	ERHY0008601	0.05 ohm,1/4W ,J ,2012 ,R/TP	N		
5	R1327	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1329	RES,CHIP	ERHY0000241	1K ohm,1/16W,J,1005,R/TP	N		
5	R1332	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1333	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1334	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1335	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1338	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1340	RES,CHIP	ERHY0000224	180 ohm,1/16W,J,1005,R/TP	N		
5	R1341	RES,CHIP	ERHY0000210	30 ohm,1/16W,J,1005,R/TP	N		
5	R1342	RES,CHIP	ERHY0000224	180 ohm,1/16W,J,1005,R/TP	N		
5	R1401	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1410	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1411	RES,CHIP	ERHY0000250	3.3K ohm,1/16W,J,1005,R/TP	N		
5	R1430	RES,CHIP	ERHY0000203	10 ohm,1/16W,J,1005,R/TP	N		
5	R1431	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1440	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1501	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1502	RES,CHIP	ERHY0000111	680 ohm,1/16W,F,1005,R/TP	N		
5	R1503	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1504	RES,CHIP	ERHY0000111	680 ohm,1/16W,F,1005,R/TP	N		
5	R1510	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1603	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1605	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1617	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1621	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1623	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1626	RES,CHIP	ERHY0000138	33K ohm,1/16W,F,1005,R/TP	N		
5	R1627	RES,CHIP	ERHY0000271	39K ohm,1/16W,J,1005,R/TP	N		
5	R1628	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP	N		
5	R1629	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1630	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		

Level	Location No.	Description	Part Number	Specification	SVC	Color	Remark
5	R1631	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1632	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1701	RES,CHIP	ERHY0000203	10 ohm,1/16W,J,1005,R/TP	N		
5	R1702	RES,CHIP	ERHY0000203	10 ohm,1/16W,J,1005,R/TP	N		
5	R1703	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1710	RES,CHIP	ERHY0000254	4.7K ohm,1/16W,J,1005,R/TP	N		
5	R1711	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1720	RES,CHIP	ERHY0000255	5.6K ohm,1/16W,J,1005,R/TP	N		
5	R1721	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1723	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1730	RES,CHIP	ERHY0000203	10 ohm,1/16W,J,1005,R/TP	N		
5	R1740	RES,CHIP	ERHY0000203	10 ohm,1/16W,J,1005,R/TP	N		
5	R1760	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1770	RES,CHIP	ERHY0000241	1K ohm,1/16W,J,1005,R/TP	N		
5	R1771	RES,CHIP	ERHY0000261	10K ohm,1/16W,J,1005,R/TP	N		
5	R1772	RES,CHIP	ERHY0000261	10K ohm,1/16W,J,1005,R/TP	N		
5	R1810	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1811	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1825	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1826	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1850	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1851	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R1997	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R2100	RES,CHIP	ERHY0000213	47 ohm,1/16W,J,1005,R/TP	N		
5	R2101	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP	N		
5	R2102	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP	N		
5	R2104	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP	N		
5	R2105	RES,CHIP	ERHY0000283	130K ohm,1/16W,J,1005,R/TP	N		
5	R2106	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP	N		
5	R2108	RES,CHIP	ERHY0000220	100 ohm,1/16W,J,1005,R/TP	N		
5	R2109	RES,CHIP	ERHY0000213	47 ohm,1/16W,J,1005,R/TP	N		
5	R2122	RES,CHIP	ERHY0000250	3.3K ohm,1/16W,J,1005,R/TP	N		
5	R2123	RES,CHIP	ERHY0000282	120K ohm,1/16W,J,1005,R/TP	N		
5	R2200	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R2201	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R2202	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R2203	RES,CHIP	ERHY0000445	1K ohm,1/16W,J,1608,R/TP	N		
5	R2205	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R2208	RES,CHIP	ERHY0008701	0.22 ohm,1/4W ,J ,2012 ,R/TP	N		

Level	Location No.	Description	Part Number	Specification	SVC	Color	Remark
5	R2210	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R2212	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R2213	RES,CHIP	ERHY0008701	0.22 ohm,1/4W ,J ,2012 ,R/TP	N		
5	R2214	RES,CHIP	ERHY0008602	0.1 ohm,1/4W ,J ,2012 ,R/TP	N		
5	R2215	RES,CHIP	ERHY0008601	0.05 ohm,1/4W ,J ,2012 ,R/TP	N		
5	R2216	RES,CHIP	ERHY0008601	0.05 ohm,1/4W ,J ,2012 ,R/TP	N		
5	R2217	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R2218	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R2220	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP	N		
5	R2221	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R2222	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R2223	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R2224	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R2232	RES,CHIP	ERHY0000261	10K ohm,1/16W,J,1005,R/TP	N		
5	R2233	RES,CHIP	ERHY0000274	51K ohm,1/16W,J,1005,R/TP	N		
5	R2235	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R2236	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R2237	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R2238	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R2241	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R2303	RES,CHIP	ERHY0000254	4.7K ohm,1/16W,J,1005,R/TP	N		
5	R2304	RES,CHIP	ERHY0000250	3.3K ohm,1/16W,J,1005,R/TP	N		
5	R2305	RES,CHIP	ERHY0000263	15K ohm,1/16W,J,1005,R/TP	N		
5	R2306	RES,CHIP	ERHY0000213	47 ohm,1/16W,J,1005,R/TP	N		
5	R2312	RES,CHIP	ERHY0000261	10K ohm,1/16W,J,1005,R/TP	N		
5	R2313	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R2314	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R2319	RES,CHIP	ERHY0000241	1K ohm,1/16W,J,1005,R/TP	N		
5	R2400	RES,CHIP	ERHY0000143	43K ohm,1/16W,F,1005,R/TP	N		
5	R2401	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP	N		
5	R2402	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP	N		
5	R2502	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R2606	RES,CHIP	ERHY0000138	33K ohm,1/16W,F,1005,R/TP	N		
5	R2607	RES,CHIP	ERHY0000252	3.9K ohm,1/16W,J,1005,R/TP	N		
5	R2608	RES,CHIP	ERHY0000252	3.9K ohm,1/16W,J,1005,R/TP	N		
5	R2609	RES,CHIP	ERHY0000138	33K ohm,1/16W,F,1005,R/TP	N		
5	R2610	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP	N		
5	R2613	RES,CHIP	ERHY0000203	10 ohm,1/16W,J,1005,R/TP	N		
5	R2617	RES,CHIP	ERHY0000266	22K ohm,1/16W,J,1005,R/TP	N		

Level	Location No.	Description	Part Number	Specification	SVC	Color	Remark
5	R2618	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R2619	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R2620	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R2621	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R2622	RES,CHIP	ERHY0000233	470 ohm,1/16W,J,1005,R/TP	N		
5	R3002	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R3019	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R3026	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP	N		
5	R3031	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R3041	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP	N		
5	R3042	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP	N		
5	R3043	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP	N		
5	R3045	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP	N		
5	R3046	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP	N		
5	R3047	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP	N		
5	R3049	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP	N		
5	R3050	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R3051	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP	N		
5	R3103	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R3110	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R3126	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP	N		
5	R3127	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP	N		
5	R3206	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP	N		
5	R3207	RES,CHIP	ERHY0000204	12 ohm,1/16W,J,1005,R/TP	N		
5	R3208	RES,CHIP	ERHY0000204	12 ohm,1/16W,J,1005,R/TP	N		
5	R3209	RES,CHIP	ERHY0000249	2.7K ohm,1/16W,J,1005,R/TP	N		
5	R3223	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R3227	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R3228	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R3229	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R3230	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R3232	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R3237	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R3248	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R3249	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R3263	RES,CHIP	ERHY0000202	4.7 ohm,1/16W,J,1005,R/TP	N		
5	R3303	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP	N		
5	R3319	RES,CHIP	ERHY0000241	1K ohm,1/16W,J,1005,R/TP	N		
5	R3322	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP	N		

Level	Location No.	Description	Part Number	Specification	SVC	Color	Remark
5	R3323	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP	N		
5	R3325	RES,CHIP	ERHY0000220	100 ohm,1/16W,J,1005,R/TP	N		
5	R3327	RES,CHIP	ERHY0000160	180K ohm,1/16W,F,1005,R/TP	N		
5	R3328	RES,CHIP	ERHY0008603	8.2 Kohm,1/16W ,F ,1005 ,R/TP	N		
5	R3329	RES,CHIP	ERHY0000254	4.7K ohm,1/16W,J,1005,R/TP	N		
5	R3330	RES,CHIP	ERHY0000250	3.3K ohm,1/16W,J,1005,R/TP	N		
5	R3331	RES,CHIP	ERHY0000290	300K ohm,1/16W,J,1005,R/TP	N		
5	R3332	RES,CHIP	ERHY0000288	240K ohm,1/16W,J,1005,R/TP	N		
5	R3341	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R3344	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP	N		
5	R3345	RES,CHIP	ERHY0000714	0.51 ohm,1/8W ,J ,2012 ,R/TP	Y		
5	R3346	RES,CHIP	ERHY0000209	27 ohm,1/16W,J,1005,R/TP	N		
5	R3347	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP	N		
5	R3357	RES,CHIP	ERHY0000214	51 ohm,1/16W,J,1005,R/TP	N		
5	R3360	RES,CHIP	ERHY0000214	51 ohm,1/16W,J,1005,R/TP	N		
5	R3363	RES,CHIP	ERHY0000214	51 ohm,1/16W,J,1005,R/TP	N		
5	R3364	RES,CHIP	ERHY0000214	51 ohm,1/16W,J,1005,R/TP	N		
5	R3365	RES,CHIP	ERHY0000214	51 ohm,1/16W,J,1005,R/TP	N		
5	R3366	RES,CHIP	ERHY0000214	51 ohm,1/16W,J,1005,R/TP	N		
5	R3367	RES,CHIP	ERHY0000214	51 ohm,1/16W,J,1005,R/TP	N		
5	R3376	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R3378	RES,CHIP	ERHY0000250	3.3K ohm,1/16W,J,1005,R/TP	N		
5	R3379	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R3380	RES,CHIP	ERHY0000250	3.3K ohm,1/16W,J,1005,R/TP	N		
5	R3381	RES,CHIP	ERHY0000273	47K ohm,1/16W,J,1005,R/TP	N		
5	R3382	RES,CHIP	ERHY0000202	4.7 ohm,1/16W,J,1005,R/TP	Y		
5	R3383	RES,CHIP	ERHY0000249	2.7K ohm,1/16W,J,1005,R/TP	N		
5	R3388	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R3389	RES,CHIP	ERHY0000220	100 ohm,1/16W,J,1005,R/TP	N		
5	R3390	RES,CHIP	ERHY0000220	100 ohm,1/16W,J,1005,R/TP	N		
5	R3395	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R3396	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R3397	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP	N		
5	R3398	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP	N		
5	SPFY00	PCB,MAIN	SPFY0061403	FR-4 ,.8 mm,NMBI 8 ,	N		
5	U3102	IC	EUSY0045305	SOT-23-5 ,5 PIN,R/TP ,ADj. V / 500 mA PEAK LDO REGULATOR	Y		
5	U3103	IC	EUSY0192901	BGA ,115 PIN,R/TP ,256FLASH 64PSRAM (1.8V)	Y		
5	U3104	IC	EUSY0192801	FBGA ,80 PIN,R/TP ,128M FLASH MEMORY(1.8V)	Y		
5	V1001	TR,BJT,ARRAY	EQBA0002501	USV ,200 mW,R/TP ,NPN // PNP & R. BUILT-IN TR	N		

Level	Location No.	Description	Part Number	Specification	SVC	Color	Remark
5	V1770	DIODE,VARIABLE CAP	EDVY0001801	SCD80 ,0.09 pF,R/TP ,	N		
5	V2201	DIODE,SWITCHING	EDSY0011901	EMD2 ,30 V,1 A,R/TP ,VF=1.5V(IF=200mA) , IR=30uA(VR=10V)	N		
5	V2203	DIODE,SWITCHING	EDSY0011901	EMD2 ,30 V,1 A,R/TP ,VF=1.5V(IF=200mA) , IR=30uA(VR=10V)	N		
5	V2300	DIODE,TVS	EDTY0007001	SOT23-6 ,9 V, W,R/TP ,TVS DIODE ARRAY	N		
5	V3201	DIODE,TVS	EDTY0006401	SC70-6L ,5 V,100 W,R/TP ,	N		
5	V3202	DIODE,SWITCHING	EDSY0011901	EMD2 ,30 V,1 A,R/TP ,VF=1.5V(IF=200mA) , IR=30uA(VR=10V)	N		
5	W1001	CONN,RF SWITCH	ENWY0003001	STRAIGHT ,SMD ,0.6 dB,3.8X3.0X3.6T	Y		
5	X2300	CONN,SOCKET	ENSY0009901	8 PIN,ETC ,SMD ,2.54 mm,2.2T UIM CONNECTOR WITH BRIDGE	Y		
5	X2602	CONN,JACK/PLUG,EARPHONE	ENJE0003401	, PIN,	Y		
5	X3200	CONNECTOR,BOARD TO BOARD	ENBY0004202	60 PIN,0.5 mm,STRAIGHT ,Au ,B to B CNT(Header)	Y		
5	X3201	CONNECTOR,BOARD TO BOARD	ENBY0017602	20 PIN,0.4 mm,STRAIGHT ,AU ,0.9t, SOCKET for CAMERA	N		
5	X3203	CONN,RECEPTACLE	ENEY0004101	24 PIN,3 , ,25.3*10*(3+1.5)T	Y		
5	Z1100	FILTER,SAW	SFSY0012901	1842.5 MHz,2.0*2.5*0.8 ,SMD , DCS RX RF SAW	Y		
5	Z1110	FILTER,SAW	SFSY0013001	942.5 MHz,2.0*2.5*0.8 ,SMD ,GSM RX RF SAW	Y		
5	Z1400	FILTER,SAW	SFSY0014201	2140 MHz,2.5*2.0*0.8 ,SMD ,WCDMA Rx RF SAW	Y		
5	Z1420	FILTER,SAW	SFSY0012501	190 MHz,3.8*3.8*1.2 ,SMD ,WCDMA RX IF SAW	N		
5	Z1500	FILTER,SAW	SFSY0014301	1900 MHz,2.5*2.0*1.0 ,SMD ,UMTS Tx RF SAW	N		
3	SBEY00	BATTERY,ETC	SBEY0002901	1.5 V,1.15 mAh,U8100 BACK-UP BATTERY 1.9T	Y		M38
3	SNMF00	ANTENNA,MOBILE,FIXED	SNMF0007401	, dB,U8100 DUAL BAND(GSM,WCDMA)	Y		M34
3	SUMY00	MICROPHONE	SUMY0005601	ASSY ,-44 dB,6.0*1.8 ,U8100 MIC	Y		M22

11.3 Accessory

Level	Location No.	Description	Part Number	Specification	SVC	Color	Remark
2	MHBY00	HANDSTRAP	MHBY0000404	130mm	Y	Dark Gray	
2	SBPL00	BATTERY PACK,LI-ION	SBPL0072201	3.7 V,1200 mAh,1 CELL,PRISMATIC ,U8150 STD BATTERY PACK	Y		
2	SGDY00	DATA CABLE	SGDY0005601	DK-40G ,K8000 24PIN I/O + USB A TYPE	Y		
2	SGEY00	EAR PHONE/EAR MIKE SET	SGEY0003701	U8110 ,Cresyn	Y		
2	SSAD00	ADAPTOR,AC-DC	SSAD0007835	FREE ,50 Hz,5.2 V,800 mA,CE,CB ,UK(IO.24P)	Y		
2	WSYY00	SOFTWARE	WSYY0115011	V074I	N		
2	WSYY01	SOFTWARE	WSYY0115211	Bundle CD SW Version 1.0	N		