



Service Manual



Service Manual

U8550

Model : U8550



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1. INTRODUCTION

1. INTRODUCTION

1.1 Purpose

This manual provides the information necessary to repair, calibration, description and download the features of this model.

1.2 Regulatory Information

A. Security

Toll fraud, the unauthorized use of telecommunications system by an unauthorized part (for example, persons other than your company's employees, agents, subcontractors, or person working on your company's behalf) can result in substantial additional charges for your telecommunications services. System users are responsible for the security of own system.

There are may be risks of toll fraud associated with your telecommunications system. System users are responsible for programming and configuring the equipment to prevent unauthorized use. The manufacturer does not warrant that this product is immune from the above case but will prevent unauthorized use of common-carrier telecommunication service of facilities accessed through or connected to it. The manufacturer will not be responsible for any charges that result from such unauthorized use.

B. Incidence of Harm

If a telephone company determines that the equipment provided to customer is faulty and possibly causing harm or interruption in service to the telephone network, it should disconnect telephone service until repair can be done. A telephone company may temporarily disconnect service as long as repair is not done.

C. Changes in Service

A local telephone company may make changes in its communications facilities or procedure. If these changes could reasonably be expected to affect the use of the phones or compatibility with the network, the telephone company is required to give advanced written notice to the user, allowing the user to take appropriate steps to maintain telephone service.

D. Maintenance Limitations

Maintenance limitations on the phones must be performed only by the manufacturer or its authorized agent. The user may not make any changes and/or repairs expect as specifically noted in this manual. Therefore, note that unauthorized alternations or repair may affect the regulatory status of the system and may void any remaining warranty.

E. Notice of Radiated Emissions

This model complies with rules regarding radiation and radio frequency emission as defined by local regulatory agencies. In accordance with these agencies, you may be required to provide information such as the following to the end user.

F. Pictures

The pictures in this manual are for illustrative purposes only; your actual hardware may look slightly different.

G. Interference and Attenuation

A phone may interfere with sensitive laboratory equipment, medical equipment, etc. Interference from unsuppressed engines or electric motors may cause problems.

H. Electrostatic Sensitive Devices

ATTENTION

Boards, which contain Electrostatic Sensitive Device (ESD), are indicated by the  sign. Following information is ESD handling:

- Service personnel should ground themselves by using a wrist strap when exchange system boards.
- When repairs are made to a system board, they should spread the floor with anti-static mat which is also grounded.
- Use a suitable, grounded soldering iron.
- Keep sensitive parts in these protective packages until these are used.
- When returning system boards or parts like EEPROM to the factory, use the protective package as described.

1. INTRODUCTION

1.3 Abbreviations

For the purpose of this manual, following abbreviations apply.

APC	Automatic Power Control
BB	Baseband
BER	Bit Error Ratio
CC-CV	Constant Current - Constant Voltage
CLA	Cigar Lighter Adapter
DAC	Digital to Analog Converter
DCS	Digital Communication System
dBm	dB relative to 1 milliwatt
DSP	Digital Signal Processing
DTC	DeskTop Charger
EEPROM	Electrical Erasable Programmable Read-Only Memory
EL	Electroluminescence
ESD	Electrostatic Discharge
FPCB	Flexible Printed Circuit Board
GMSK	Gaussian Minimum Shift Keying
GPIB	General Purpose Interface Bus
GPRS	General Packet Radio Service
GSM	Global System for Mobile Communications
IQUI	International Portable User Identity
IF	Intermediate Frequency
LCD	Liquid Crystal Display
LDO	Low Drop Output
LED	Light Emitting Diode
OPLL	Offset Phase Locked Loop
PAM	Power Amplifier Module
PCB	Printed Circuit Board
PGA	Programmable Gain Amplifier
PLL	Phase Locked Loop

I. Introduction

1.3 Abbreviations

For the purpose of this manual, following abbreviations apply.

PSTN	Public Switched Telephone Network
RF	Radio Frequency
RLR	Receiving Loudness Rating
RMS	Root Mean Square
RTC	Real Time Clock
SAW	Surface Acoustic Wave
SIM	Subscriber Identity Module
SLR	Sending Loudness Rating
SRAM	Static Random Access Memory
UMTS	Universal Mobile Telephony System

2. PERFORMANCE

2. PERFORMANCE

2.1 System Overview

Item	Specification
Shape	GSM900/1800/1900 & WCDMA Folder- Dual Mode Handset
Size	90 x 55 x 24.7mm
Weight	134g (with Standard Battery)
Power	1400mA Li-Polymer
Talk Time	Over 180 Min (WCDMA, Tx=12 dBm, Voice) Over 220 Min (GSM, Tx=Max, Voice)
Standby Time	Over 165 hrs (WCDMA, DRX=1.28) Over 223 hrs (GSM, Paging period=9)
Antenna	Fixed Type (Fixed Screw)
Main LCD	220 x 220 TFT LCD 262K Color
Sub LCD	128 x 160 TFT LCD 262K Color
Main/Sub LCD BL	White LED Backlight
Vibrator	Yes (Cylinder Type)
LED Indicator	Blue
C-MIC	Yes
Receiver	Yes
Earphone Jack	Yes
SIM Socket	Yes (3.0V/1.8V)
Volume Key	Push Type(+,-)
Voice Key	Push Type (Memo)
External Memory	T - Flash Socket
I/O Connect	24 Pin

2. PERFORMANCE

2.2 Usable environment

1) Environment

Item	Spec.	Unit
Voltage	4.0 (Typ), 3.4 (Min), (Shut Down: 3.2)	V
Operating Temp.	-20 ~ + 60	°C
Storage Temp.	-30 ~ + 85	°C
Humidity	max. 85	%

2) Environment(Accessory)

Item	Spec.	Min	Typ.	Max	Unit
Power	Available power	100	220	240	Vac

* CLA: 12~24V(DC)

2.3 Radio Performance

1) Transmitter -GSM Mode

No	Item	GSM		DCS/PCS		
1	Conducted Spurious Emission	MS allocated Channel	100k ~ 1GHz	-39dBm	9k ~ 1GHz	-39dBm
					1G ~ 1710MHz	-33dBm
		Idle Mode	1G ~ 12.75GHz	-33dBm	1710M ~ 1785MHz	-39dBm
					1785M ~ 12.75GHz	-33dBm
			100k ~ 880MHz	-60dBm	100k ~ 880MHz	-60dBm
			880M ~ 915MHz	-62dBm	880M ~ 915MHz	-62dBm
			915M ~ 1000Mz	-60dBm	915M ~ 1000MHz	-60dBm
			1G ~ 1.71GHz	-50dBm	1G ~ 1.71GHz	-50dBm
			1.71G ~ 1.785GHz	-56dBm	1.71G ~ 1.785GHz	-56dBm
			1.785G ~ 12.75GHz	-50dBm	1.785G ~ 12.75GHz	-50dBm

2. PERFORMANCE

No	Item		GSM		DCS/PCS	
1	Radiated Spurious Emission	MS allocated Channel	30M ~ 1GHz	-36dBm	30M ~ 1GHz	-36dBm
			1G ~ 4GHz	-30dBm	1G ~ 1710MHz	-30dBm
		Idle Mode	1710M ~ 1785MHz	-36dBm	1785M ~ 4GHz	-30dBm
			30M ~ 880MHz	-57dBm	30M ~ 880MHz	-57dBm
			880M ~ 915MHz	-59dBm	880M ~ 915MHz	-59dBm
			915M ~ 1000Mz	-57dBm	915M ~ 1000MHz	-57dBm
			1G ~ 1.71GHz	-47dBm	1G ~ 1.71GHz	-47dBm
1.71G ~ 1.785GHz	-53dBm	1.71G ~ 1.785GHz	-53dBm			
1.785G ~ 4GHz	-47dBm	1.785G ~ 4GHz	-47dBm			
2	Frequency Error		±0.1ppm		±0.1ppm	
3	Phase Error		±5(RMS)		±5(RMS)	
			±20(PEAK)		±20(PEAK)	
4	Frequency Error Under Multipath and Interference Condition		3dB below reference sensitivity		3dB below reference sensitivity	
			RA250: ±200Hz		RA250: ±250Hz	
			HT100: ±100Hz		HT100: ±250Hz	
			TU50: ±100Hz		TU50: ±150Hz	
			TU3: ±150Hz		TU1.5: ±200Hz	
5	Output RF Spectrum	Due to modulation	0 ~ 100kHz	+0.5dB	0 ~ 100kHz	+0.5dB
			200kHz	-30dB	200kHz	-30dB
			250kHz	-33dB	250kHz	-31dB
			400kHz	-60dB	400kHz	-33dB
			600 ~ 1800kHz	-66dB	600 ~ 1800kHz	-60dB
			1800 ~ 3000kHz	-69dB	1800 ~ 6000kHz	-60dB
			3000 ~ 6000kHz	-71dB	≥6000kHz	-73dB
			≥6000kHz	-77dB		
		Due to Switching transient	400kHz	-19dB	400kHz	-22dB
			600kHz	-21dB	600kHz	-24dB
			1200kHz	-21dB	1200kHz	-24dB
			1800kHz	-24dB	1800kHz	-27dB

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No	Item	GSM			DCS/PCS		
7	Intermodulation attenuation		-		Frequency offset	800kHz	
					Intermodulation product should be Less than 55dB below the level of Wanted signal		
8	Transmitter Output Power	Power control Level	Power (dBm)	Tolerance (dB)	Power control Level	Power (dBm)	Tolerance (dB)
		5	33	±3	0	30	±3
		6	31	±3	1	28	±3
		7	29	±3	2	26	±3
		8	27	±3	3	24	±3
		9	25	±3	4	22	±3
		10	23	±3	5	20	±3
		11	21	±3	6	18	±3
		12	19	±3	7	16	±3
		13	17	±3	8	14	±3
		14	15	±3	9	12	±4
		15	13	±3	10	10	±4
		16	11	±5	11	8	±4
		17	9	±5	12	6	±4
		18	7	±5	13	4	±4
		19	5	±5	14	2	±5
						15	0
9	Burst timing	Mask IN			Mask IN		

2. PERFORMANCE

2) Transmitter-WCDMA Mode

No	Item	Specification
1	Maximum Output Power	Class3: +24dBm(+1/-3dB) Class4: +21dBm(±2dB)
2	Frequency Error	±0.1ppm
3	Open Loop Power control in uplink	±9dB@normal, ±12dB@extreme
4	Inner Loop Power control in uplink	Adjust output(TPC command) cmd 1dB 2dB 3dB +1 +0.5/1.5 +1/3 +1.5/4.5 0 -0.5/+0.5 -0.5/+0.5 -0.5/+0.5 -1 -0.5/-1.5 -1/-3 -1.5/-4.5 group(10equal command group) +1 +8/+12 +16/+24
5	Minimum Output Power	-50dBm(3.84MHz)
6	Out-of-synchronization handling of output power	Qin/Qout:DPCCH quality levels Toff@DPCCH/lor:-22->-28dB Ton@DPCCH/lor:-24->-18dB
7	Transmit OFF Power	-56dBm(3.84M)
8	Transmit ON/OFF Time Mask	±25us PRACH, CPCH, uplink compressed mode
9	Change of TFC	±25us power varies according to the data rate DTX: DPCH off (minimize interference between UE)
10	Power setting in uplink compressed	±3dB(after 14slots transmission gap)
11	Occupied Bandwidth(OBW)	5MHz(99%)
12	Spectrum emission Mask	-35-15*(Δf-2.5)dBc@ Δf=2.5~3.5MHz, 30k -35-1*(Δf-3.5)dBc@ Δf=3.5~7.5MHz, 1M -39-10*(Δf-7.5)dBc@ Δf=7.5~8.5MHz, 1M -49 dBc@ Δf=8.5~12.5MHz, 1M

2. PERFORMANCE

No	Item	Specification
13	Adjacent Channel Leakage Ratio(ACLR)	33dB@5MHz, ACP>-50dBm 43dB@10MHz, ACP>-50dBm
14	Spurious Emissions *: additional requirement	-36dBm@f=9~150KHz, 1k BW -36dBm@f=150KHz~30MHz, 10k -36dBm@f=30~1000MHz, 100k -30dBm@f=1~12.75GHz, 1M -41dBm*@1893.5~1919.6MHz, 300k -67dBm*@925~935MHz, 100k -79dBm*@935~960MHz, 100k -71dBm*@1805~1880MHz, 100k
15	Transmit Intermodulation	-31dBc@5MHz, Interferer -40dBc -41dBc@10MHz, Interferer -40dBc
16	Error Vector Magnitude(EVM)	17.5% (>-20dBm) (@12.2k, 1DPDCH+1DPCCH)
17	Transmit OFF Power	-15dB@SF=4, 768kbps, multi-code transmission

3)Receiver - GSM Mode

No	Item	GSM	DCS/PCS
1	Sensitivity (TCH/FS Class II)	-105dBm	-105dBm
2	Co-Channel Rejection (TCH/FS Class II, RBER, TUhigh/FH)	C/Ic=7dB	C/Ic=7dB
3	Adjacent Channel Rejection	200kHz	C/Ia1=-12dB
		400kHz	C/Ia2=-44dB
4	Intermodulation Rejection	Wanted Signal: -98dBm 1'st interferer: -44dBm 2'st interferer: -45dBm	Wanted Signal: -96dBm 1'st interferer: -44dBm 2'st interferer: -44dBm
5	Blocking Response (TCH/FS Class II, RBER)	Wanted Signal: -101dBm Unwanted Signal: Depend on freq.	Wanted Signal: -101dBm Unwanted Signal: Depend on freq.

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4) Receiver - WCDMA Mode

No	Item	Specification
18	Reference Sensitivity Level	-106.7dBm(3.84M)
19	Maximum Input Level	-25dBm(3.84MHz) -44dBm/3.84MHz(DPCH_Ec) UE@+20dBm output power(class3)
20	Adjacent Channel Selectivity(ACS)	33dB UE@+20dBm output power(class3)
21	In-band Blocking	-56dBm/3.84MHz@10MHz UE@+20dBm output power(class3)
		-44dBm/3.84MHz@15MHz UE@+20dBm output power(class3)
22	Out-band Blocking	-44dBm/3.84MHz@f=2050~2095 & 2185~2230MHz, band a) UE@+20dBm output power(class3)
		-30dBm/3.84MHz@f=2025~2050 & 2230~2255MHz, band a) UE@+20dBm output power(class3)
		-15dBm/3.84MHz@f=1~2025 & 2255~12500MHz, band a) UE@+20dBm output power(class3)
23	Spurious Response	-44dBm CW UE@+20dBm output power(class3)
24	Intermodulation Characteristic	-46dBm CW@10MHz & -46dBm/3.84MHz@20MHz UE@+20dBm output power(class3)
25	Spurious Emissions	-57dBm@f=9KHz~1GHz, 100k BW
		-47dBm@f=1~12.75GHz, 1M
		-60dBm@f=1920~1980MHz, 3.84MHz
		-60dBm@f=2110~2170MHz, 3.84MHz

2. PERFORMANCE

5) Bluetooth Mode

5.1) Transmitter

1	Out Power	Class 2 : -6~4dBm		
2	Power Density	Power density < 20dBm per 100kHz EIRP		
3	Power Control	Option 2dB ≤ step size ≤ 8dB		
4	TX Output Spectrum -Frequency range	fmax & fmin @ below the level of -30dBm(100kHz BW) within 2.4GHz~2.4835GHz		
5	TX Output Spectrum -20dB Bandwidth	≤ 1MHz		
6	Tx Output Spectrum -Adjacent channel Po	≤ -20dBm @ C/I = 2MHz ≤ -40dBm @ C/I ≥ 3MHz		
7	Modulation Characteristics	140kHz ≤ delta f1 avg ≤ 175kHz delta f2max ≥ 115kHz at least 99.9% of all delta f2max delta f2avg/deata f1 avg ≥ 0.8		
8	Init. Carrier Freq. Tolerance	≤ ±75KHz		
9	Carrier Frequency Drift	1 slot : ≤ ± 25kHz 3 slot : ≤ ± 40kHz 5 slot : ≤ ± 40kHz Maximum drift rate ≤ 20KHz/50usec		
10	Out of Band Spurious Emissions	Freq.Range	Operating	Standby
		30MHz~1GHz	-36dBm	-57dBm
		Above 1GHz~12.75GHz	-30dBm	-47dBm
		1.8~1.9GHz	-47dBm	-47dBm
		5.15~5.3GHz	-47dBm	-47dBm

2. PERFORMANCE

5.2) Receiver

11	Sensitivity single slot packets	BER \leq 0.1%@-70dBm	
12	Sensitivity multi slot packets	BER \leq 0.1%@-70dBm	
13	C/I performance	BER \leq 0.1%@ (Low, Mid, High Frequency) 2405MHz, 2441MHz, 2477MHz	
		Interference	Ratio
		Co-Channel interference, C/I co-channel	11dB
		Adjacent(1MHz)interference, C/I 1MHz	0dB
		Adjacent(2MHz)interference, C/I 2MHz	-30dB
		Adjacent(\geq 3MHz)interference, C/I \geq 3MHz	-40dB
		Adjacent(\geq 3MHz)interference to in band	-9dB
		mirror frequency, C/I image \pm 1MHz	-20dB
14	Blocking Characteristic	BER \leq 0.1%@wanted signal -67dBm	
		interfering Signal Frequency	Power Level
		30MHz~2000MHz	-10dBm
		2000MHz~2400MHz	-27dBm
		2500MHz~3000MHz	-27dBm
		3000MHz~12.75GHz	-10dBm
15	Intermodulation Performance	BER \leq 0.1%@wanted signal -64dBm static sinwave signal at f1=-39dBm a BT modulated signal f2=-39dBm(payload PRBS15)	
16	Maximum Input Level	BER \leq 0.1%@-20dBm	

2. PERFORMANCE

2.4 Current Consumption

(VT test : Speaker off, LCD backlight On)

	Stand by	Voice Call	VT
WCDMA	165Hours=8.48mA (DRX=1.28)	180Min=467mA (Tx=12dBm)	130Min=646mA (Tx=12dBm)
GSM	223Hours=6.28mA (paging=9period)	220Min=380mA (Tx=Max)	

2.5 RSSI

TBD

	GSM	WCDMA(TBD)
BAR 4 → 3	-91 ±2dBm	-87 ±2dBm
BAR 3 → 2	-96 ±2dBm	-97 ±2dBm
BAR 2 → 1	-101 ±2dBm	-107 ±2dBm
BAR 1 → 0	-106 ±2dBm	-112 ±2dBm

2.6 Battery Bar

Indication	Voltage
BAR 4 → 3 (65%)	3.87 ± 0.05V
BAR 3 → 2 (43%)	3.77 ± 0.05V
BAR 2 → 1 (24%)	3.72 ±0.05V
BAR 1 → Icon Blinking (3%)	3.54 ±0.05V
Low voltage, warning message	3.54 ±0.03V(Talk: 1min. interval) -3% 3.50 ±0.03V(Standby: 3min. Inverval) -2%
Power OFF	3.15 ±0.03V ↓ (WCDMA Talk) 3.23 ±0.03V ↓ (else)

2. PERFORMANCE

2.7 Sound Pressure Level

		No	Test Item		Specification	
A C O U S T I C	MS	1	Sending Loudness Rating (SLR)		NOM	8±3dB
					MAX	
		2	Receiving Loudness Rating (RLR)		NOM	-1±3dB
					MAX	
		3	Side Tone Masking Rating (STMR)		NOM	17dB over
					MAX	
		4	Echo Loss (EL)		NOM	40dB over
					MAX	
	5	Sending Distortion (SD)		refer to TABLE 30.3		
	6	Receiving Distortion (RD)		refer to TABLE 30.4		
	7	Idle Noise-Sending (INS)		NOM	-64dBm0p under	
				MAX		
	8	Idle Noise-Receiving (INR)		NOM	-47dBPA under	
				MAX		
	9	Sending Loudness Rating (SLR)		NOM	8±3dB	
				MAX		
10	Receiving Loudness Rating (RLR)		NOM	-1±3dB		
			MAX			
11	Side Tone Masking Rating (STMR)		NOM	25dB over		
			MAX			
12	Echo Loss (EL)		NOM	40dB over		
			MAX			
13	Sending Distortion (SD)		refer to TABLE 30.3			
14	Receiving Distortion (RD)		refer to TABLE 30.4			
15	Idle Noise-Sending (INS)		NOM	-55dBm0p under		
			MAX			
16	Idle Noise-Receiving (INR)		NOM	-45dBPA under		
			MAX			
17	TDMA NOISE –.GSM: Power Level: 5 DCS: Power Level: 0 (Cell Power: -90 ~ -105dBm) –.Acoustic(Max Vol.) MS/HEADSET SLR: 8±3dB MS/HEADSET RLR: -13±1dB/-15dB (SLR/RLR: mid-Value Setting)		MS	GSM	SEND	-62dBm under
					REV.	
				DCS	SEND	
					REV.	
		Headset	GSM	SEND	REV.	
			DCS	SEND	REV.	

2.8 Charging

- **Normal mode:** Complete Voltage: 4.2V
Charging Current: 800mA
- **Await mode:** In case of During a Call, should be kept 3.9V
(GSM: It should be kept 3.9V in all power level
WCDMA: It will not be kept 3.9V in some power level)
- **Extend await mode:** At Charging prohibited temperature(-20C under or 60C over)
(GSM: It should be kept 3.7V in all power level
WCDMA: It will not be kept 3.7V in some power level)

3. Technical Brief

3. Technical Brief

3.1 Digital Baseband(DBB) & Multimedia Processor

3.1.1 General Description

A. Features

- CPU ARM946 running at 104 MHz
 - 32 kB Instruction Cache, 16 kB Data Cache, 128 kB Instruction TCM and 128 kB Data TCM
 - 8 channel DMAC
- DSP C55x (LEAD3) Megastar (MGS3_2.0B) running at 170 MHz
 - 144 kWord ROM, 32 kWord DARAM, 32 kWord SARAM
 - 7 channel DMAC
 - Dedicated API channel to DSP memory (not locked up to other DMA channels)
- UMTS Access
 - Support for WCDMA/GSM Dual Mode
 - GSM/GPRS network signaling (from Layer 1 to 3)
 - WCDMA Ciphering and Integrity
 - High Speed Serial Link (HSSL) to the WCDMA Modem (at Layer 1)
 - GSM AMR
 - Multislot Class 8
 - HSCSD 14.4 kb/s
- MMI
 - Keypad Interface
 - Tone Generator Interface
 - Camera Data and Programmable Display Interfaces
 - Enhanced graphics support for QCIF display
- Operation and Services
 - I²C™, Interface
 - SIM Interfaces
 - General Purpose I/O (GPIO) Interface
 - External Memory Interface that supports FLASH, SRAM and PSRAM
 - JTAG
 - RTC
- Data Communication
 - IrDA® (SIR)
 - UARTs (ACB, EDB (RS232), Bluetooth® HCI)
 - Slave USB
- Package
 - 12 by 12 mm 289 pin FPBGA Production Package

3.1.2 Hardware Architecture

The hardware structure is delivered as five separate hardware macros to the top-level design, also depicted in Figure.

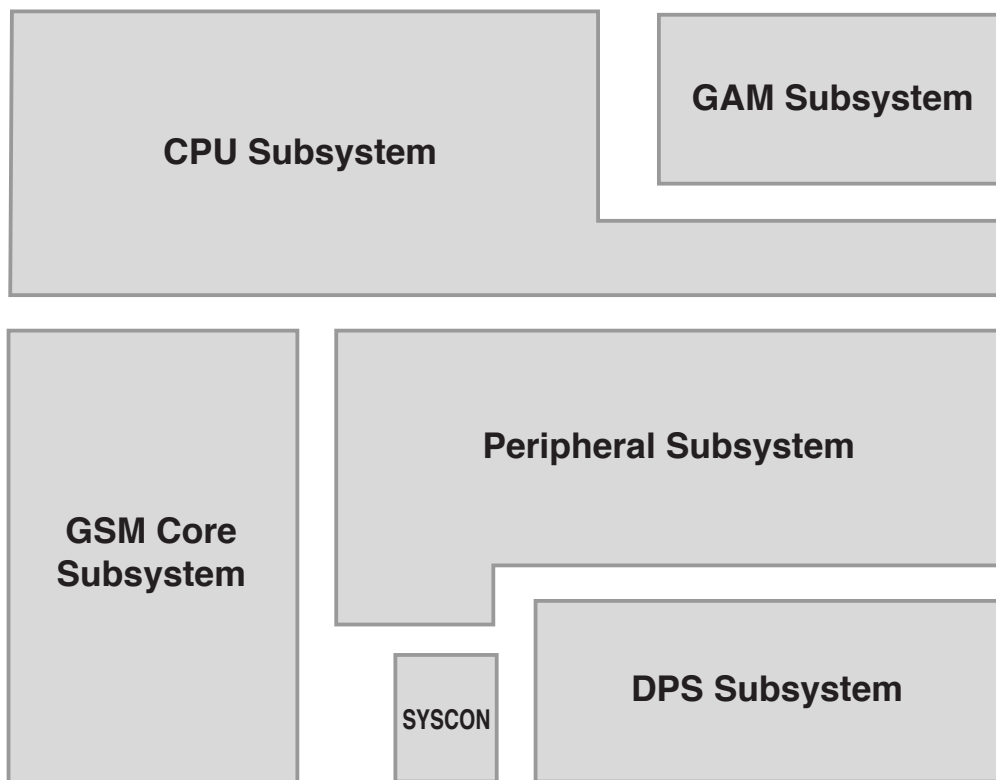


Figure 3-1-1 Simplified Block Diagram of Ericsson DB 2000

3. Technical Brief

A. Block Diagram

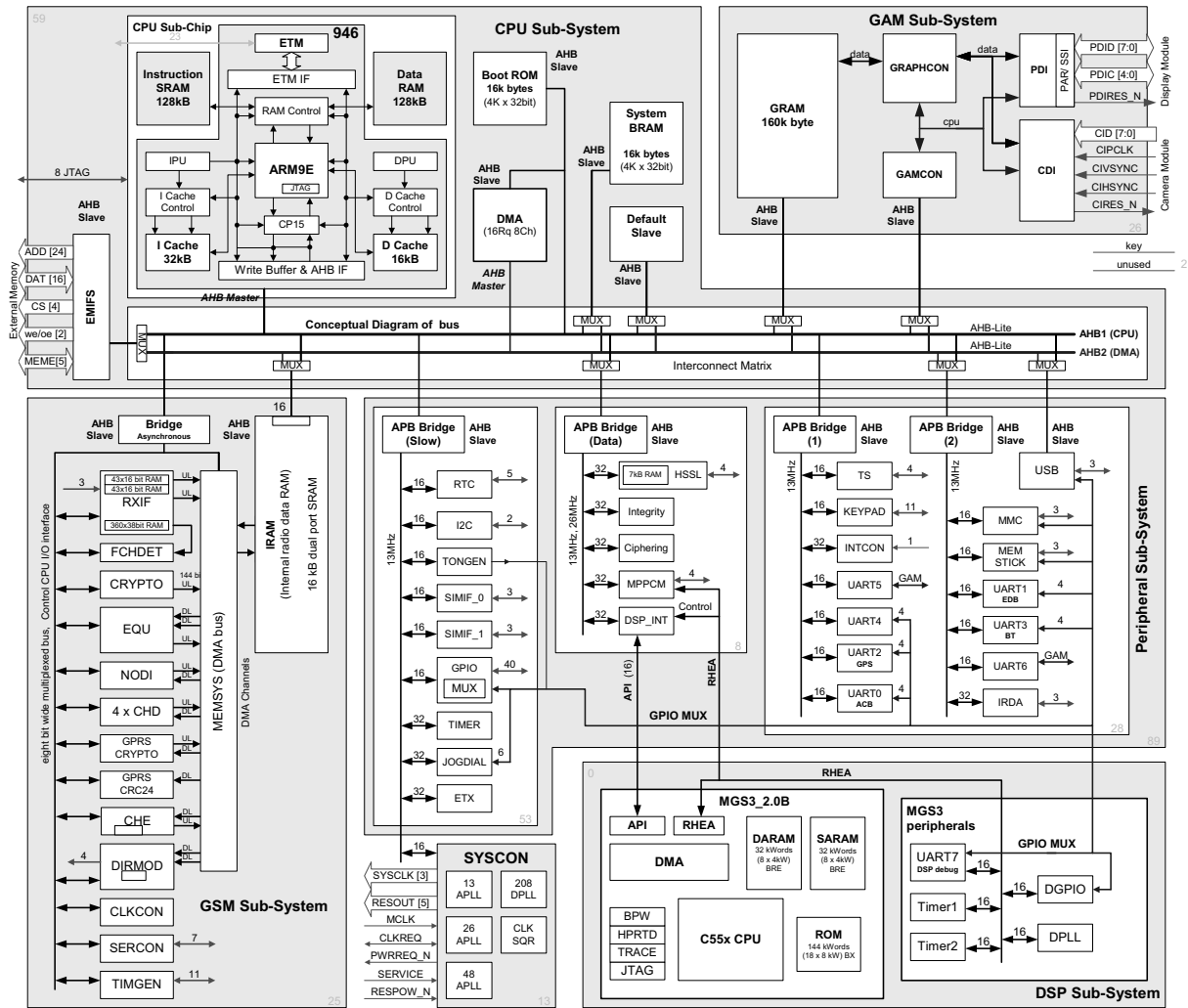


Figure 3-1-2 Detailed Block Diagram of Ericsson DB 2000

B. CPU Hardware Subsystem

The CPU subsystem incorporates:

- CPU Sub chip
- Backplane
- JTAG
- DMA Controller
- System Buffer RAM
- Boot ROM
- External Memory Interface (EMIF) for connection to external SRAM and Flash memories. The bus architecture is built on the ARM AMBA standard with multi-layer AHB (Advanced High-speed Bus) and APB (Advanced Peripheral Bus) for the peripheral buses. There are two AHB busses, the CPU AHB and the DMA AHB.

Clocks to the CPU subsystem are distributed from the system control (SYSCON) backplane clocking. The reset lines are all asynchronously asserted low and synchronously negated high. The CPU subsystem has separate clocking and reset for the ARM946, AHB system, EMIF and DMAC.

C. Peripheral Hardware Subsystem

There are 29 peripherals within the peripheral hardware subsystem. With the exception of the USB, all hardware peripheral blocks are APB slave peripherals. From an architecture hierarchy perspective, the SYSCON block is an APB slave on the slow APB bridge, but resides at the top level of the ASIC. The APB provides a simple interface to support low-performance peripherals. Within the peripheral subsystem, there are four separate APB busses with AHB to APB (AHB2APB) bridges to the multi-layer AHB.

D. DSP Hardware Subsystem

The DSP subsystem provides support for processor intensive activity, such as voice coding and multimedia application support. The DSP subsystem includes the standard C55x™ Core (LEAD3) from Texas Instruments with associated memory system and peripherals.

E. GAM Hardware Subsystem

The Graphics Accelerator Module (GAM) subsystem provides hardware support in the creation of visual imagery and the transfer of this data to the display. GAM also provides support for the camera module. The visual data could be graphics, still images or video.

The GAM subsystem consists of five modules:

- GRAM - graphics memory (160 kB).
- GAMCON - GAM controller.
- GRAPHCON - graphics controller.
- PDI/SSI - programmable display interface for parallel/serial displays.
- CDI - camera data interface.

3. Technical Brief

F. GSM Hardware Subsystem

The GSM subsystem is a stand-alone sub-chip incorporating GSM modem and interface to GSM radio together with memory control (MEMSYS) and internal RAM (IRAM).

The hardware peripheral blocks are RXIF, FCHDET, CRYPTO, EQU, NODI, 4 x CHD, GPRS CRYPTO, GPRS CRC24, CHE, DIRMOD, CLKCON, SERCON, TIMGEN, MEMSYS and IRAM.

The peripherals are accessible to the AHB (CPU-only) by an asynchronous I/O bridge.

The dual port IRAM is accessible to the AHB (CPU and DMA) by a synchronous AHB slave interface.

G. System Control Subsystem

The system controller subsystem (SYSCON) is primarily responsible for generating clock signals and distributing the clock and reset signals within the ASIC and certain external devices. The GSM core, GAM and DSP subsystems include their own system controllers that are sourced from SYSCON. SYSCON consists of analog and digital PLL clocks and a clock squarer. The block is a slave peripheral on the slow APB bus under control of the CPU.

The programming of SYSCON controls the fundamental modes of operation within the ASIC.

Individual blocks can also be reset and their clocks held inactive by accessing the appropriate control registers. SYSCON also controls the requesting protocol through which different subblocks in Ericsson DB 20000 can request clocks derived from the system clock.

The system controller also stores the chip-ID number in a read only register.

3.1.3 External memory interface

There are four independent chip selects (CS0, CS1, CS2, CS3) provided for external memories and each has an address range of 256 Mb.

RF calibration data, Audio parameters and battery calibration data etc are stored in flash memory area.

A. U8550

- 1-MCP used (512Mb flash memory + 128Mb PSRAM)
- 4-CS (Chip Select) are used

Interface Spec.						
Device	Part Name	Maker	Read Access Time			Write Access Time
			Async	Page	Burst	
Flash	RD38F4455LLYBQ1	Intel	85 ns	25 ns	14 ns at 54MHz	90 ns
PSRAM			85 ns	25 ns	10 ns at 66MHz	85 ns

Table 3-1-1. External Memory Interface Spec. of U8550

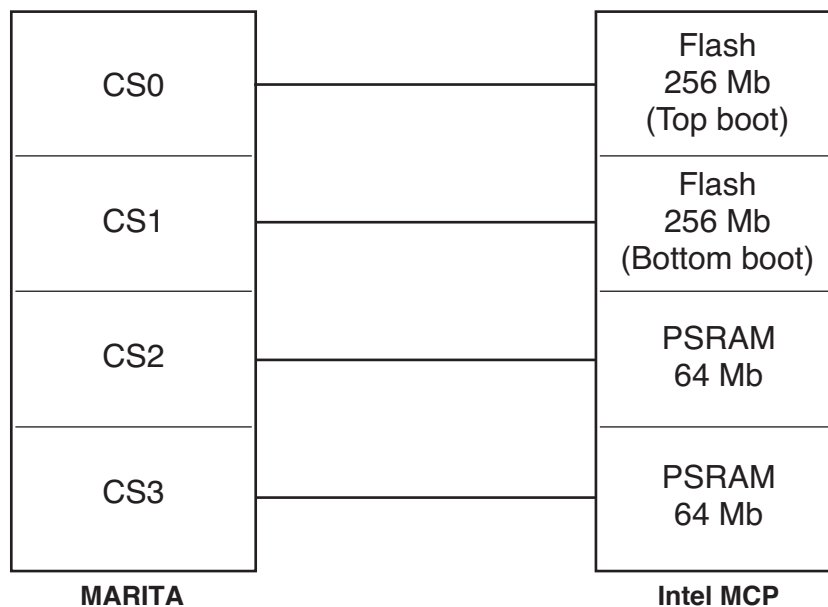


Figure 3-1-3. External Memory Configuration of U8550

3. Technical Brief

3.1.4 RF Interface

A. MARITA Interface

Marita controls GSM RF part using these signals through GSM RF chip-Ingela.

- RFCLK, RFDAT, RFSTR : Control signals for Ingela
- TXON, RXON : Control signals for TX and RX part of Ingela
- PCTL : Control signal for GSM TX PAM
- BANDSELO : Band selection signal for GSM or DCS
- ANTSW[0:3] : Control signals for antenna switch
- DCLK, IDATA, QDATA : GSM/DCS RX Data
- DIRMOD[A:D] : GSM/DCS TX Data

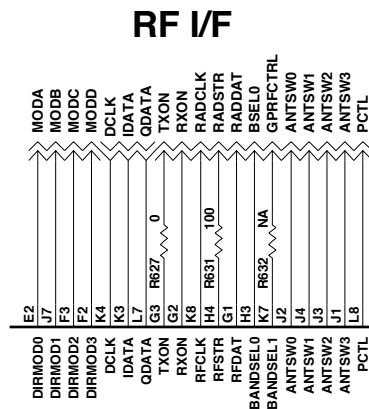


Figure 3-1-4. Schematic of MARITA RF Interface

B. WANDA Interface

Wanda controls WCDMA RF part using these signals through W-CDMA RF chip-Wopy & Wivi.

- WCLK, WDAT, WSTR : Control signals for Wivi & Wopy
- RXIA, RXIB, RXQA, RXQB : WCDMA RX Data
- TXIA, TXIB, TXQA, TXQB : WCDMA TX Data
- HSSLRX_D, HSSLRX_CLK : Marita & Wanda Communication Signal
- HSSLTX_D, HSSLTX_CLK : Marita & Wanda Communication Signal

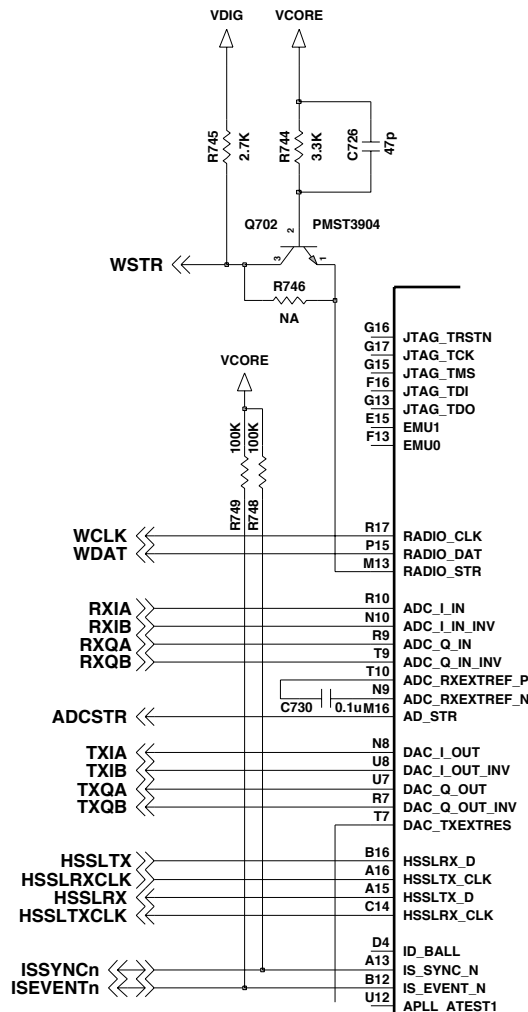


Figure 3-1-5. Schematic of WANDA RF Interface

3. Technical Brief

3.1.5 SIM Interface

SIM interface scheme is shown in Figure 3-1-6

SIMDAT0, SIMCLK0, SIMRST0 ports are used to communicate DBB(MARITA) with ABB(VINCENNE) and filter.

SIM (Interface between DBB and ABB)	
SIMDAT0	SIM card bidirectional data line
SIMCLK0	SIM card reference clock
SIMRST0	SIM card async/sync reset

Table 3-1-2. SIM Interface

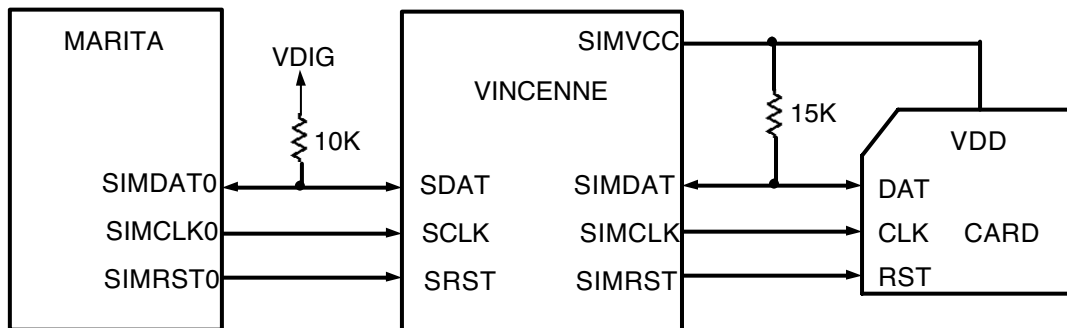


Figure 3-1-6. SIM Interface Scheme

3.1.6 UART Interface

UART signals are connected to MARITA GPIO through IO connector and Bluetooth interface.

UART0		
Resource	Name	Note
GPIO10	UARTRX0	Receive Data
GPIO11	UARTTX0	Transmit Data
UART3 for the bluetooth		
GPIO24	UARTRX3	Receive Data
GPIO25	UARTTX3	Transmit Data
GPIO26	UARTCTS3	Clear To Send
GPIO27	UARTRTS3	Request To Send

Table 3-1-3. UART Interface

3. Technical Brief

3.1.7 GPIO (General Purpose Input/Output) map

In total 40 allowable resources. This model is using 22 resources.

GPIO Map, describing application, I/O state, and enable level are shown in below table 3-1-4.

IO #	Application	IO	Resource	Inactive State	Active State
GPIO00	VGA_IO_OFF	O	GPIO	Low	High
GPIO01	I2C_VGA_EN	O	GPIO	Low	High
GPIO02	CAM28_VGA_EN	O	GPIO	Low	High
GPIO03	PULSESKIP (Not used)	-	-	-	-
GPIO04	Not used	-	-	-	-
GPIO05	CIRES_N_MEGA	O	GPIO	High	Low
GPIO06	HS_AMP_EN	O	GPIO	Low	High
GPIO07	Not used	-	-	-	-
GPIO10	UARTRX0	I	UART0	High	Low
GPIO11	UARTTX0	O	UART0	High	Low
GPIO12	AUDIO_AMP_EN	O	GPIO	Low	High
GPIO13	HS_SPK_SEL	O	GPIO	Low(Headset)	High(Speaker)
GPIO14	Not used	-	-	-	-
GPIO15	Not used	-	-	-	-
GPIO16	Not used	-	-	-	-
GPIO17	I2C_MEGA_EN	O	GPIO	Low	High
GPIO20	CAM28_EN	O	GPIO	Low	High
GPIO21	Not used	-	-	-	-
GPIO22	3D_OFF	O	GPIO	Low	High
GPIO23	Not used	-	-	-	-
GPIO24	UARTRX3	I	UART3	High	Low
GPIO25	UARTTX3	O	UART3	High	Low
GPIO26	UARTCTS3	I	UART3	-	-
GPIO27	UARTRTS3	O	UART3	-	-
GPIO30	Not used	-	-	-	-
GPIO31	CAM18_EN	O	GPIO	Low	High
GPIO32	KEY_LED_ONOFF	O	GPIO	Low	High
GPIO33	Not used	-	-	-	-
GPIO34	BTF_REG_EN	O	GPIO	Low	High
GPIO35	Not used	-	-	-	-
GPIO36	3D_CTRL2	O	GPIO	Low	High
GPIO37	TF_DETECT	I	GPIO	Low	High
GPIO40	USBSENSE	I	GPIO	Low	High
GPIO41	3D_CTRL1	O	GPIO	Low	High
GPIO42	Not used	-	-	-	-
GPIO43	FOLDER_DET	I	GPIO	Low(Closed)	High(Open)
GPIO44	Not used	-	-	-	-
GPIO45	TP601 (Not used)	-	-	-	-
GPIO46	BL_SLEEP_EN	O	GPIO	Low	High
GPIO47	Not used	-	-	-	-

Table 3-1-4. MARITA GPIO Map Table

3.1.8 USB

The USB block supports the implementation of a "full-speed" device fully compliant to USB 2.0 standard. It provides an interface between the CPU (embedded local host) and the USB wire, and handles USB transactions with minimal CPU intervention.

The USB specification allows up to 15 pairs of endpoints. Data for each endpoint is buffered in RAM within the USB block and is read/written from the endpoint FIFO using DMA transfers or FIFO register access. High-speed (high throughput) endpoints can use DMA while slower endpoints can use FIFO register access. The USB block can request up to six DMA channels, three for IN endpoints and three for OUT endpoints.

USB Function	Note
USBDP	USB differential (+) line
USBDM	USB differential (-) line
USBSENSE (GPIO40)	USB detection (input)
USBPUEN	USB Pull-up control
VDDUSB	Power supply for MARITA USB block

Table 3-1-5. USB Signal Interface of MARITA

USB regulator input voltage is 5V and uses external USB device power through IO Connector.

Output voltage is 3.3V and supplies to MARITA USB block.

USB is detected by MARITA GPIO40(USBSENES).

- $V_{USB} / (10K + 51K) = V_{USBSENSE} / 51K$

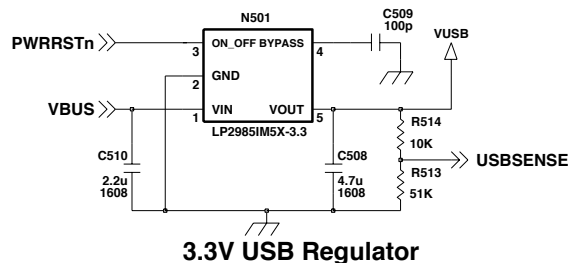


Figure 3-1-7. Schematic of USB Regulator

3. Technical Brief



Figure 3-1-8. Schematic of MARITA USB block

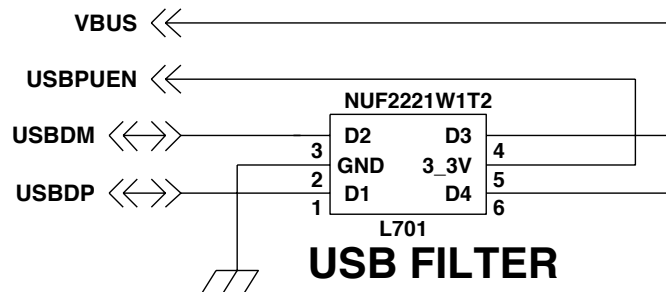


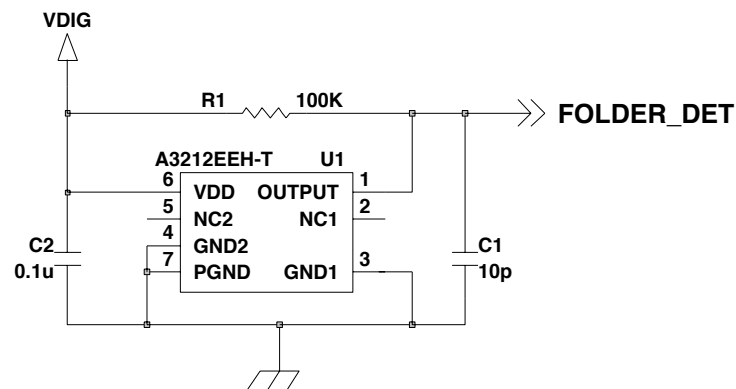
Figure 3-1-9. Schematic of USB filter

3.1.9 Folder ON/OFF Detection

There is a magnet to detect the folder status, opened or closed.

If a magnet is close to the hall-effect switch(U1 on Keypad), the voltage at Pin 1 of U1 goes to 0V. Otherwise 2.8V.

This folder signal is delivered to MARITA GPIO43(FOLDER_DET).



Folder Detect

Figure 3-1-10. Folder ON/OFF Detector

3. Technical Brief

3.1.10 Bluetooth Interface

U8550 supports Bluetooth operation using Philips' BGB202/S2 Bluetooth module.

A. General Description

The Bluetooth interface utilizes the UART interface for control signals going to and from the Bluetooth module. The UART is also used for data transmissions. It uses the PCM interface for transmitting audio to and from the Bluetooth module.

The Bluetooth module uses both the 13 MHz master clock signal and the 32,768 kHz low-frequency clock signal for internal timing within the Bluetooth module. The intention is to use the low-frequency clock as a low-power timing provider and to use the 13 MHz as a high precision timing reference used mainly by the Bluetooth radio during operation. The clock request mechanism is used to minimize current consumption for the total system. The intention is to use the CLKREQ signal to ask for the master clock when needed, for example, when the Bluetooth radio is operating.

B. UART Interface

The UART interface is a standard interface and it includes the handshake signals RTS and CTS.

The following speeds can be achieved:

9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600, and 1843200 bauds/s.

C. PCM Interface

The PCM interface is used to send audio to and from the Bluetooth module. The interface is a synchronous interface using a PCM clock and a PCM sync signal for synchronization. Two data signals are used for data, one in each direction. The PCM clock signal operates at frequencies as high as 1 MHz. The word length of the audio data can be 8 or 16 bits. Furthermore, the PCM interface has a function known as MP-PCM, which is an addressing scheme, used to have more than two devices talking on the bus. To add this function, the data pins have to be bi-directional. Additionally, the position of the audio data relative to the frame sync pulse must be selectable. During the periods within a frame that a device is not transmitting audio data, it must put both PCM data signals in a high-impedance state to allow other devices access.

D. Master Clock and Clock Request Interface

The master clock (MCLK) is a 13 MHz signal used as the high precision clock signal for the Bluetooth module. The signal can be switched on and off by the platform. The master clock request (CLKREQ) is used by the Bluetooth module to ask for the master clock.

If the Bluetooth module asserts the signal high, it gets the master clock. The other alternative for the Bluetooth module is to set the clock request output to high impedance state, indicating that it does not need the master clock. The Bluetooth module receives the master clock, if other parts of the chipset request it.

E. Low Frequency Clock Interface

The low-frequency clock signal (RTCCLK) is used by the Bluetooth module as a low-power clock. The clock is used in different Bluetooth modes, like sniff and park, to have a correct timing on the Bluetooth air interface without having the master clock running. The low-frequency clock is always present, in some applications even when the chipset is powered down.

F. BGB202/S2

- General
 - Full module (BB+RF) : Only need to external antenna and reference clock
 - Bluetooth Specification version 1.1
 - Dimensions : 7 x 8 x 1.3 mm
 - Power class 2 : 10m
- Radio Part
 - Fully integrated near-zero-IF receiver with high sensitivity (typical -82dBm)
 - Advanced DC offset compensation for improved reception quality
 - RSSI with high dynamic range
 - Programmable output pre-amplifier
 - Fully integrated low phase noise VCO operating in the 5 GHz frequency range
 - Internal shielding for better EMI (Electro Magnetic Interference) immunity.
- Baseband Part
 - Embedded ARM7TDMI microprocessor
 - 224 kBytes embedded ROM, 32 kBytes SRAM and 8 kBytes internal RAM (iRAM) for BB controller
 - Watchdog timer and Two 32-bit system timers
 - Bluetooth controller including scrambling, CRC generation/checking, FEC encoding/decoding and ciphering according the Specification of the Bluetooth System, Version 1.1
 - Bluetooth connections supporting : Maximum 3 active connections (ACL)
One voice connection (SCO)
 - CVSD transcoder
 - RF interface
 - RSSI measurement
 - On-chip 1.8 V voltage regulator
 - 8-bit D/A and A/D conversion for various purposes, e.g. PA control
 - Power-on reset
 - System clock crystal oscillator
 - Low-power crystal oscillator for a low-frequency clock input
 - System clock request signal for control of external clock source
 - Microprocessor interfaces including UART, I2C-bus, combined PCM/IOM® and general purpose I/O-pins
 - PATCH mechanism for code updates and corrections
- Firmware
 - Interface drivers
 - Bluetooth controller driver
 - Link Controller (LC)
 - Link Manager (LM)
 - Host Controller Interface (HCI)

3. Technical Brief

G. U8550 Bluetooth Schematic

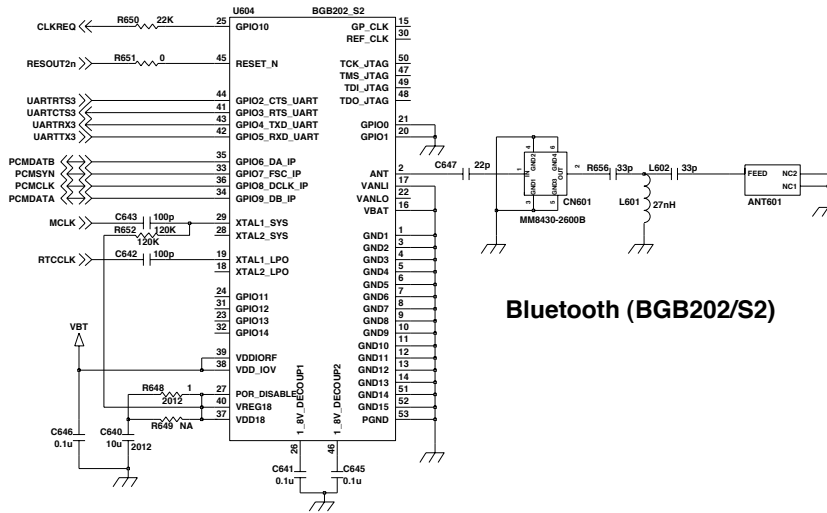


Figure 3-1-11. Schematic of Bluetooth module (BGB202/S2)

- Clock
 - Clock request
 - Connected to CLKREQ of MARITA and VINCENNE, input to WOPY
 - Fast clock : 13MHz
 - Supplied MCLK from WOPY
 - Frequency deviation : ± 10 ppm
 - If level of MCLK is less than 400mVpp, connect to 1.8V through R652(120K)
 - Slow clock : 32.768kHz
 - Supplied RTCCLK from MARITA
- Power
 - Supplied 2.85V from external regulator (U510, controlled by GPIO34 of MARITA)
 - NRESET, UART, PCM, GPIO[2-9]
 - 1.8V is generated by internal regulator of BGB202/S2
 - Baseband core, GPIO[10-14], SysClkReq, JTAG
- Reset
 - RESOUT2n signal of MARITA controls BGB202/S2 reset.
- UART
 - Connected to UART3 of MARITA
 - HCI interface between MARITA and BGB202/S2
- PCM
 - Audio signal interface between MARITA/VINCENNE and BGB202/S2
- ANT
 - 2.4GHz, 50 ohm matching
 - Antenna switch(CN601) is used for Bluetooth calibration

3.1.11 TransFlash Interface

U8550 supports the TransFlash interface as external memory card.

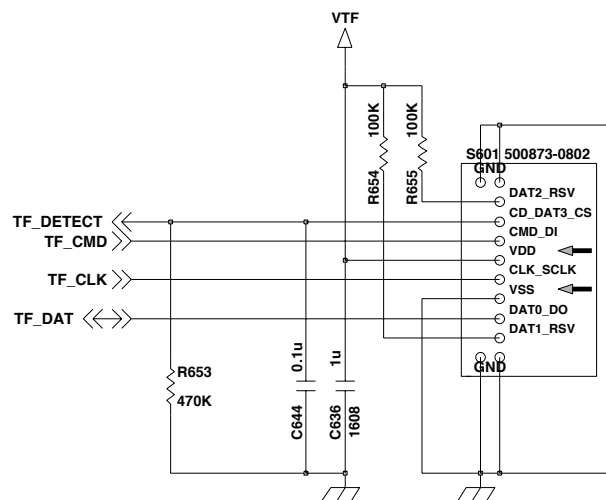
TransFlash has 4-data line, but U8550 uses only 1-data line.

All control and data line is connected to MARITA

TransFlash Interface	
TF_DETECT	Card detection, connected to GPIO37 of MARITA
TF_CMD	Command/Response
TF_CLK	Clock
TF_DAT	Data line
VTF	Supply voltage from 2.85V external regulator(U510)

Table 3-1-6. TransFlash Interface

- Card detection
 - When there are no card in TransFlash socket, TF_DETECT pin is Low.
 - If card is inserted in socket, because TransFlash has internal pull-up, TF_DETECT pin changes High.
 - VTF is always supply power.
 - If card is removed, TF_DETECT pin changes Low.



Trans-Flash

Figure 3-1-12. TransFlash and Schematic of TransFlash Interface

3. Technical Brief

3.1.12 Power On Sequence

- ① User presses END key and then ONSWAN signal is changed to Low.
- ② VINCENNE initiates the internal oscillator and powers on the regulators.
- ③ VINCENNE generates a power for MARITA.
- ④ VINCENNE releases the power reset signal(PWRRSTn) and generates an interrupt(IRQ0n) to MARITA.

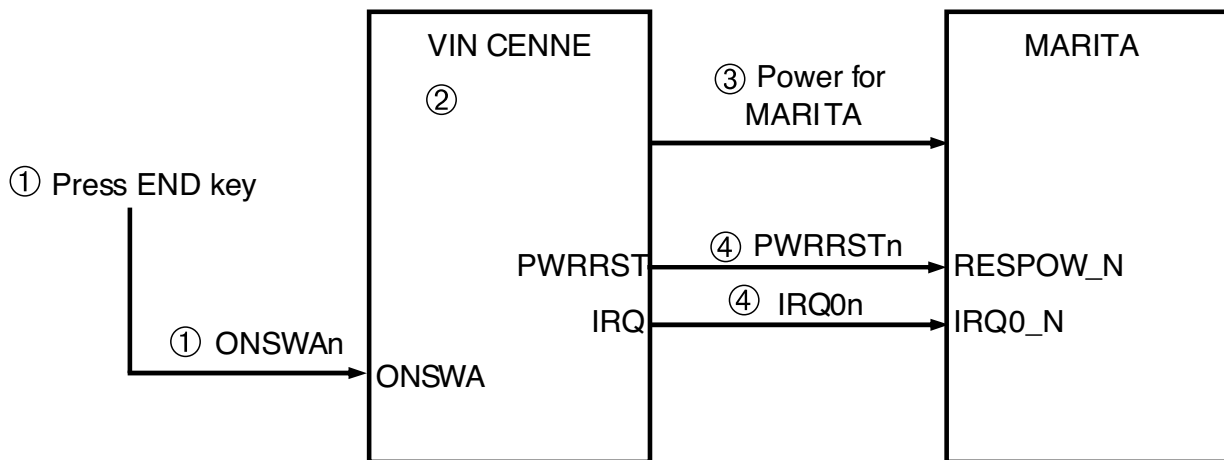


Figure 3-1-13. Power On Sequence

3.1.13 Keypad

There are 26 buttons, 3 side keys and 3 MOD keys.
 'END' key is connected to ONSWAN for Vincenne.

	KEYIN0	KEYIN1	KEYIN2	KEYIN3	KEYIN4
KEYOUT0		SIDE1	SIDE2	SIDE3	
KEYOUT1	MENU	SEARCH	MULTI	CAM	OK
KEYOUT2	1	4	7	*	UP
KEYOUT3	2	5	8	0	DOWN
KEYOUT4	3	6	9	#	RIGHT
KEYOUT5	SEND	CLEAR	BACK	GAME	LEFT

Table 3-1-7. Key Matrix Mapping Table

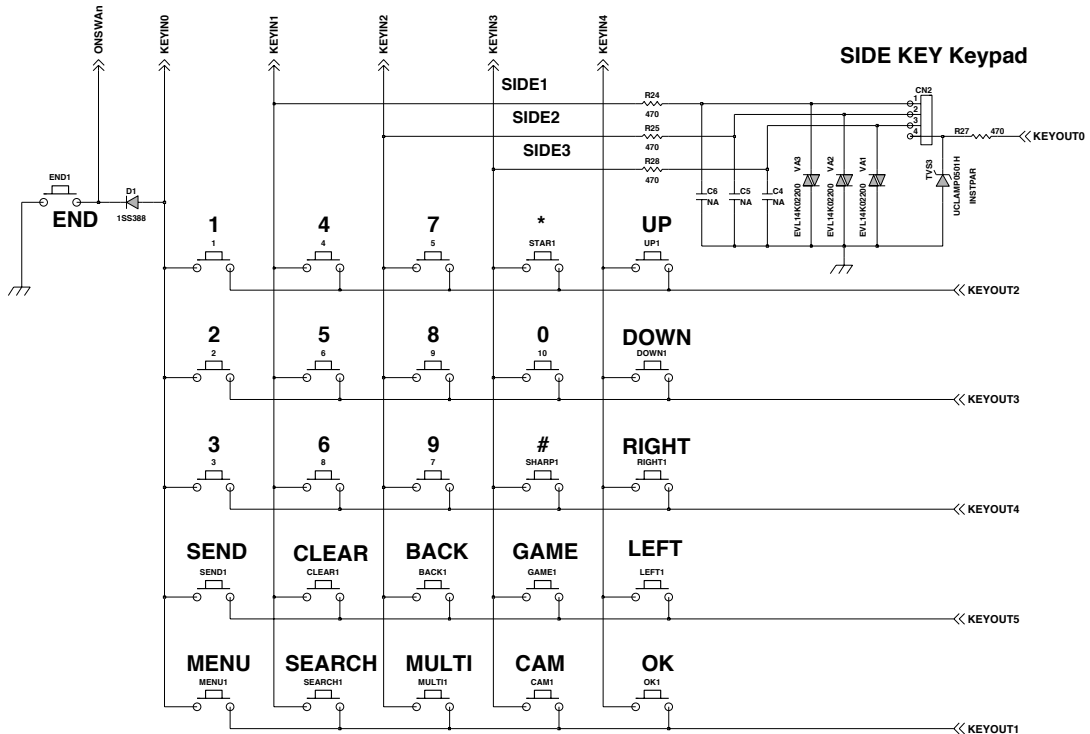


Figure 3-1-14. Schematic of Keypad

3. Technical Brief

	KEYIN1	KEYIN2	KEYIN3
GND	RIGHT	CENTER	LEFT

Table 3-1-8. MOD Key Matrix Mapping Table

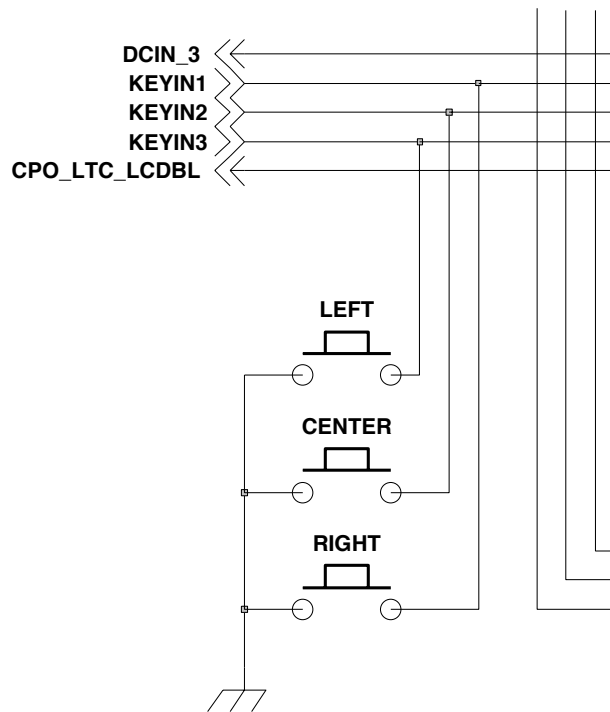


Figure 3-1-15. Schematic of MOD Keypad

3.2 GAM Hardware Subsystem

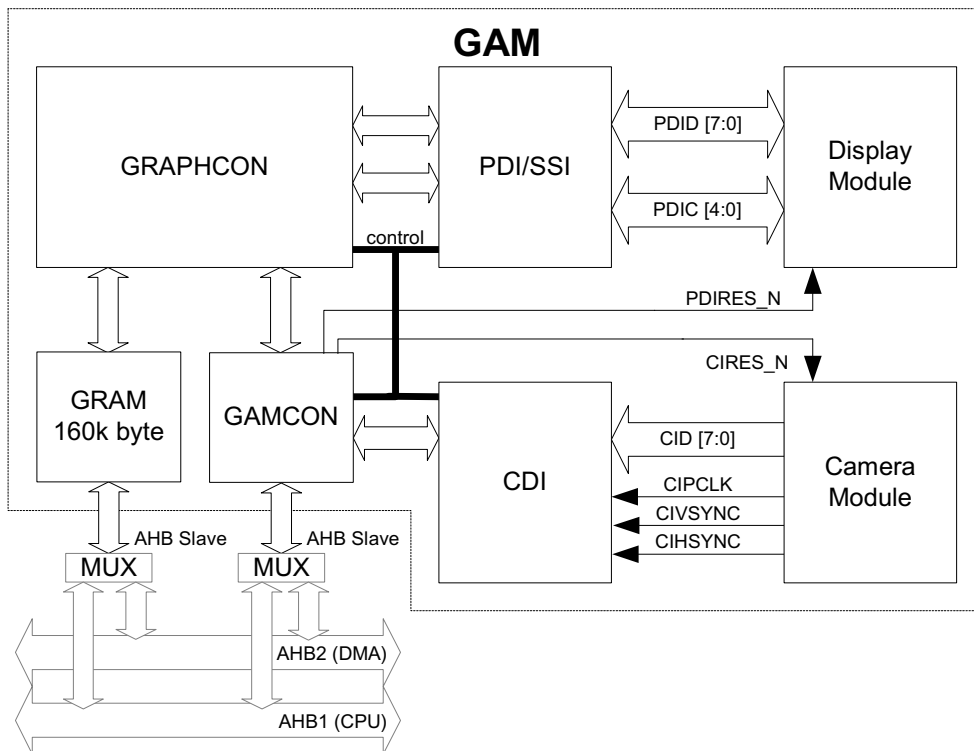


Figure 3-2-1. GAM Subsystem Functional Block Diagram

3.2.1 General Description

The Graphics Accelerator Module (GAM) subsystem provides hardware support in the creation of visual imagery and the transfer of this data to the display. GAM also provides support for the camera module. The visual data could be graphics, still images or video. The GAM subsystem consists of five modules:

- GRAM : graphics memory (160 kB).
- GAMCON : GAM controller.
- GRAPHCON : graphics controller.
- PDI/SSI : programmable display interface for parallel/serial displays.
- CDI : camera data interface.

3. Technical Brief

3.2.2 Block Description

A. GAM Controller(GAMCON)

The GAM Controller (GAMCON) is responsible for clock gating and distribution within the GAM module. GAMCON receives the HCLK from SYSCON and distributes to GRAPHCON, GRAM, PDI and CDI. GAMCON also distributes the GAM reset signal to GRAPHCON, GRAM, PDI and CDI.

The reset signals CIRESET_N and PDIRESET_N are distributed from GAMCON to the camera and display module respectively, see Figure 2.28. The CIPCLK is used to clock the received data into the camera data interface. The CIPCLK can be in the range of 100 kHz to 16 MHz.

B. Graphics RAM (GRAM) Block

GAM includes 160 kB of graphics memory (GRAM) in order to support display screen sizes of QCIF + alfa display size and three frame buffers when decoding QCIF video.

The GRAM can be accessed in 8, 16 or 32-bit mode. Write access takes a single AHB clock cycle. Non-sequential read and the first access of a sequential read access takes two AHB clock cycles. Subsequent sequential read access take a single AHB clock cycle.

The GRAM contains both frame buffer and temporary data. There are three image areas with one used for normal MMI graphics and the other two areas used for still images, video frames or camera frames. The three image areas can be combined into one frame buffer.

GRAM is required to transfer a VGA (640 by 480 pixels) image from the camera data interface (CDI) over DMA at 100 MBit/s, within a 50 ms timeframe. The GRAM is used as a buffer, but the average transfer bandwidth required is approximately 3 Mword/s (32-bit word), that is 12 MByte/s.

C. Graphics Controller (GRAPHCON) Block

GRAPHCON is controlled by the application CPU and can perform operations on pixels and image areas. Images can be moved and merged with other images and text.

The GRAPHCON block receives graphical objects from GRAM and performs the appropriate graphical manipulation. The resulting data is transferred to the display interface (PDI).

GRAPHCON can receive images from the camera data interface (CDI) and send them to the PDI automatically. GRAPHCON performs conversion from YUV to RGB and can scale (zoom) still or video images.

D. Programmable Display Interface (PDI) Block

The programmable display interface (PDI) is designed to interface both parallel and serial display modules. The display data is transferred from the 32 word FIFO on GAMCON to the display module via the PDI block. The PDI block is built around a micro controller and executes 16-bit instruction words to individually control the I/O ports. It has a 128 byte program memory, programmable by the CPU, which can store up to 64 instructions.

The CPU transfers all set-up and control data to the display. Data is transferred to PDI as 32-bit words, which in turn writes 8-bit data to the display. The programmable PDI block is configured at the software build stage, to support either parallel interface such as PPI or serial interface such as SSI or I2C.

E. Camera Data Interface (CDI) Block

The camera data interface (CDI) block is designed to support a range of still image camera modules. An 8-bit parallel bus supports data transfer from the camera module to the CDI.

The pixel clock is an output clock from the camera module to the CDI and qualifies the data on the parallel bus. One byte of data is captured on each rising edge of the pixel clock. CDI allows the pixel clock to be in the range of 100 kHz to 16 MHz.

The horizontal synchronization line is an input from the camera module and defines one scanline of image data. The horizontal synchronization line can be programmed to be active high or low. The vertical synchronization line is an input from the camera module and defines one image frame (image height) of data. The vertical synchronization line can be programmed to be active high or low.

The frame rate can be adjusted by skipping frames and various interrupts are used to inform the application CPU regarding the progress of incoming images and potential errors. The normal data format on the data bus is YUV 4:2:2 (raw binary image data) according to the CCIR-656 standard. A function within the CDI can be programmed to reorder the YUV parameters as they pass through the CDI. In addition, the CDI is able to detect the end of an image and perform some truncation as well as overflow conditions. There is nothing preventing the use of other data types such as JPEG or RGB (as long as the timing is followed), but only YUV data can be sent to the display.

Camera images can also be sent to a DMA channel to store the image in external memory.

The I2C interface and GPIO are part of the interface to the camera module, but they are not part of the CDI block. The I2C is used to set-up and control the camera module.

The camera module I2C lines must go high impedance when the supply is removed from the camera. The I2C commands needed to control the camera, as well as the functional behavior of the module, are also different for each implementation.

The ON-signal (GPIO) is used to power-on the camera from Standby or Off mode (implementation dependent). This signal must be held low when the mobile equipment is powered down and during the mobile equipment reset period. The GPIO pin can also be an input or high impedance during mobile equipment reset and start. In this case, it must have pull-down to ground.

The camera module reset signal is an output to the camera module.

3. Technical Brief

3.2.3 Camera & Camera FPC Interface

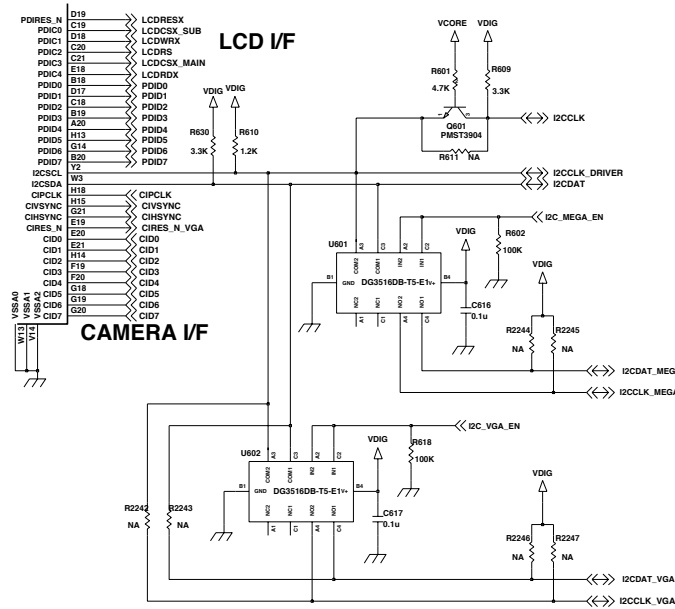


Figure 3-2-2. Camera Interface (in Marita)

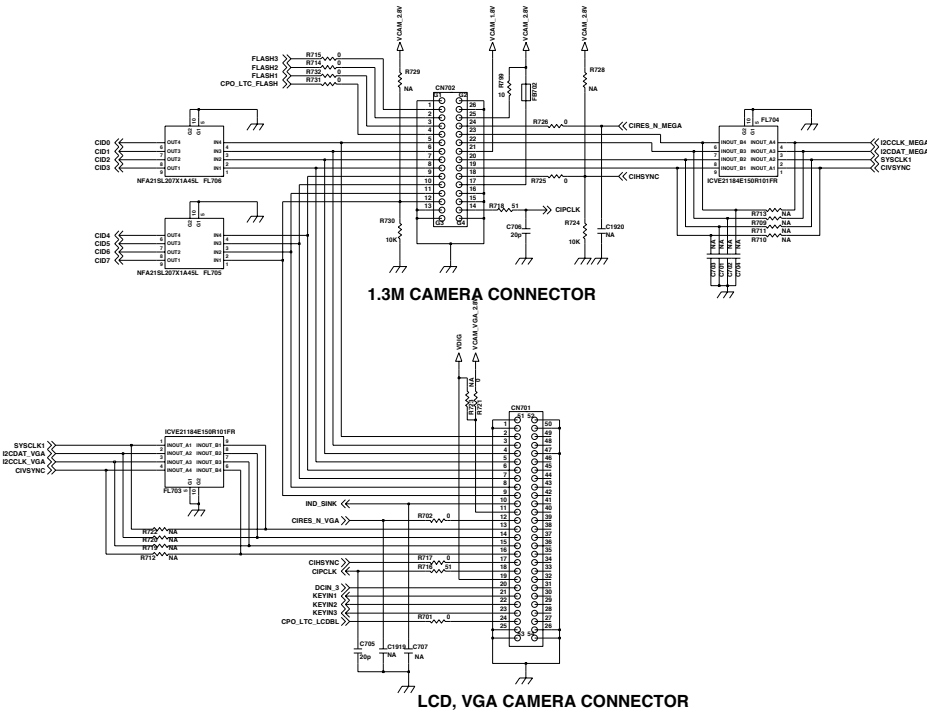


Figure 3-2-3. Main Board to FPCB Connector(50pin,26pin - Main Board)

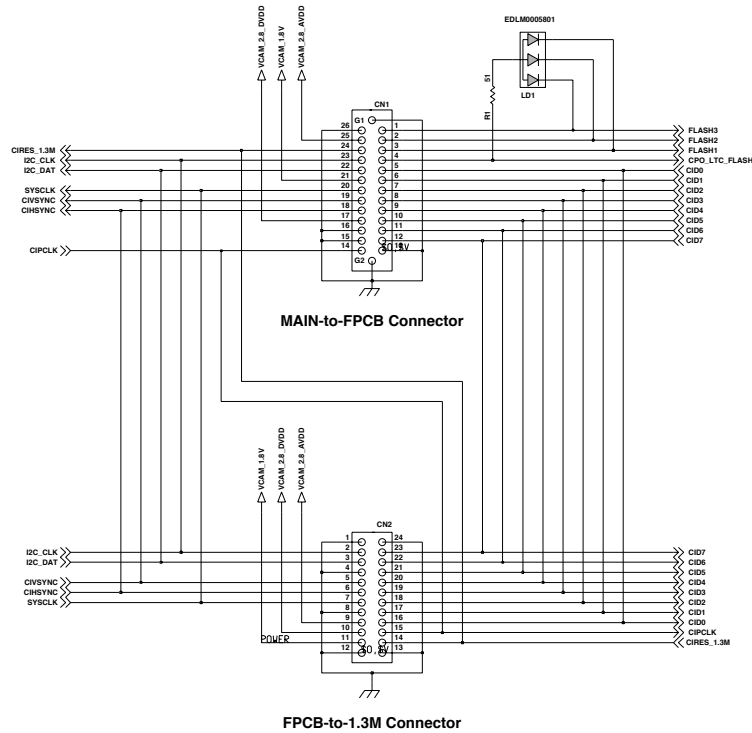


Figure 3-2-4. Main Board to camera FPCB Connector(26pin - FPCB)
FPCB to 1.3M camera Connector(24pin - FPCB)

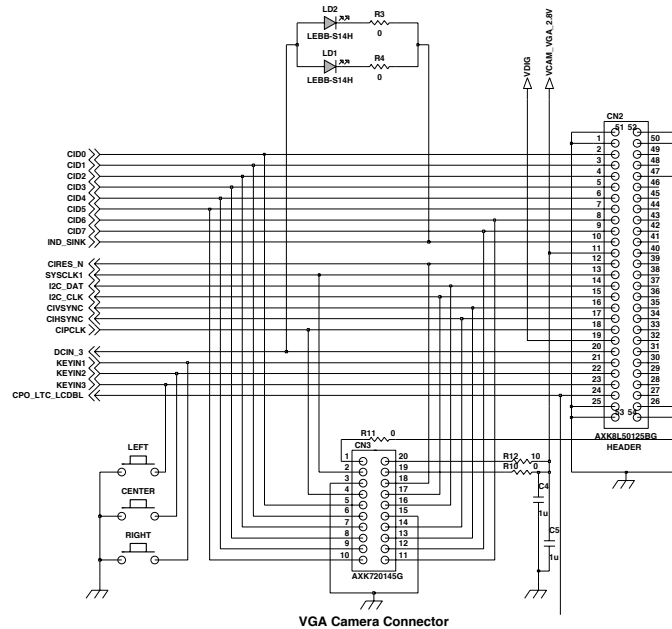


Figure 3-2-5. Main Board to LCD FPCB Connector(50pin - FPCB)
FPCB to VGA camera Connector(20pin - FPCB)

The 1.3M Camera module is connected to main board (AXK7L26227) with Camera FPCB (AXK8L26125). The VGA Camera module is connected to main board (AXK7L50227) with Camera & LCD FPCB (AXK8L50125). 1.3M Camera module is connected to FPCB with 24-pin Board to Board connector (14-5602-024-000-829 - 1.3M Camera). VGA Camera module is connected to FPCB with 20-pin Board to Board connector (AXK720145 - VGA Camera). Its interface is dedicated camera interface port in Marita. The camera port supply 13MHz master clock to camera module and receive 17MHz pixel clock (15fps), vertical sync signal, horizontal sync signal, reset signal and 8bits YUV data from camera module. The camera module is controlled by I2C port.

NO	Pin Name	I/O	Description
1	GND	O	Analog Ground
2	D7	O	Digital video data bit[7]
3	D6	O	Digital video data bit[6]
4	D5	O	Digital video data bit[5]
5	D4	O	Digital video data bit[4]
6	D3	O	Digital video data bit[3]
7	D2	O	Digital video data bit[2]
8	D1	O	Digital video data bit[1]
9	D0	O	Digital video data bit[0]
10	PCLK	O	Clock for output data
11	RESET	I	Reset
12	STANDBY	P	Digital Ground
13	DGND	P	Digital Ground
14	DVDD	P	Digital Core Voltage(1.8V)
15	DVDD	P	Digital interface Voltage(2.8V)
16	AVDD	P	Analog Voltage(2.8V)
17	GND	P	Interface Ground
18	MCLK	I	System Clock
19	HREF	O	Horizontal sync signal
20	VSYNC	O	Vertical sync signal
21	GND	P	Interface Ground
22	SDA	I/O	Serial data I/O for I2C bus
23	SCK	I/O	Clock for output data
24	GND	P	Analog Ground

Table 3-2-1. Interface between 1.3M Camera Module and FPCB (in FPCB)

NO	Pin Name	I/O	Description
1	STANDBY	In	Standby mode
2	MCLK	In	System Clock Input
3	GND	Gnd	Frame Synchronous Signal
4	PCLK	Out	Pixel Clock
5	D0	Out	Image data output
6	D1	Out	Image data output
7	D2	Out	Image data output
8	D3	Out	Image data output
9	D4	Out	Image data output
10	D5	Out	Image data output
11	D6	Out	Image data output
12	D7	Out	Image data output
13	VSYNC	Out	Vertical Synchronization Reference
14	HSYNC	Out	Horizontal Synchronization Reference
15	GND	Gnd	Ground
16	SDA	In/Out	Serial Bus Data
17	SCL	In/Out	Serial Bus Clock
18	RESET	In	Reset
19	DVDD 2.8V	Power	2.8V Digital Power
20	AVDD 2.8V	Power	2.8V Analog Power

Table 3-2-2. Interface between VGA Camera Module and FPCB (in FPCB)

3.2.4 Camera Regulator

GPIO_31 enables the 1.8V Camera Regulator for the 1.3M Camera Digital Core. GPIO_20 enables the MEGA_2.8V Camera and GPIO_02 enables the VGA_2.8V Camera Regulator.

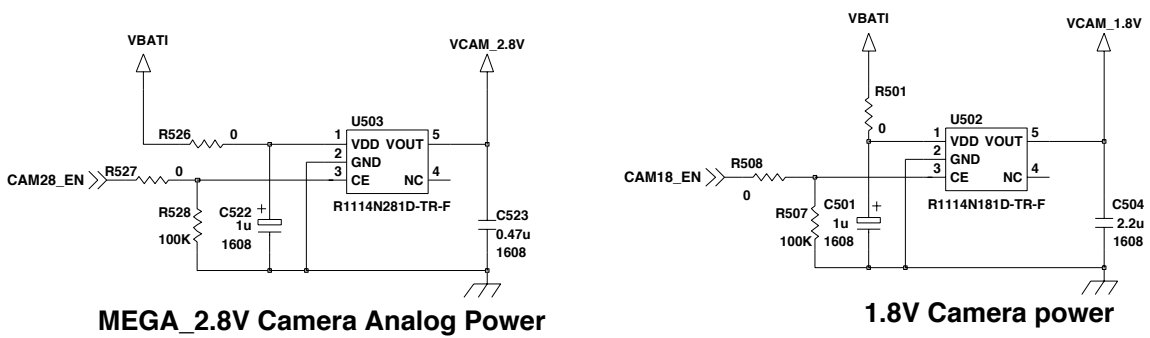


Figure 3-2-6. 1.3M 2.8V and 1.8V Camera Regulator

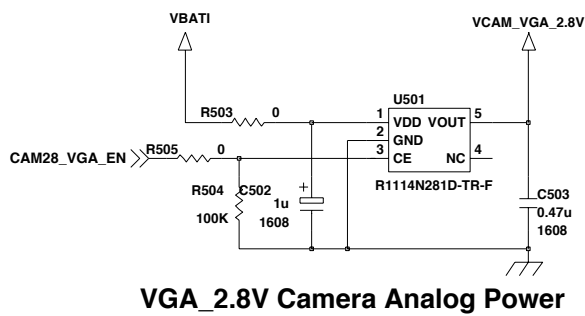


Figure 3-2-7. VGA 2.8V Camera Regulator

3. Technical Brief

3.2.5 Display & LCD FPC Interface

LCD module include device in table 3-2-3

Device	Type
Main LCD	220 X RGB X 220 262K Color TFT LCD
Sub LCD	128 X RGB X 160 262K Color TFT LCD
Main/Sub LCD Backlight	5 White LEDs (simultaneously)

Table 3-2-3. Devices in LCD Module

The LCD Module is connected to FPCB with the 40-pin Board to Board Connector (AXK8L40125) and Receiver, 2 blue Indicator/backlight LEDs are connected by soldering in the Camera & LCD FPCB. The Main&Sub LCD are controlled by 8-bit PDI (Parallel Data Interface) in Marita. In case of power off mode, if TA is inserted, 2 blue Indicator LEDs are turned-on.

NO	Pin Name	Pin Type	Description
Indicator LEDs			
20	DCIN_3	O	Indicator LEDs Power
10	IND_SINK	I	Indicator LEDs Ground
Receiver Terminal			
48	EARM	O	Receiver Minus
49	EARP	O	Receiver Plus

Table 3-2-4. Interface between Camera&LCD FPCB and Receiver, Vibrator, Indicator LEDs and Camera Flash LEDs

3. Technical Brief

NO	Pin Name	Pin Type	Description	Unused Pin
1	VCC	-	The Logic Power Supply for LDI and LCM	-
2	VCI	-	The Analogue Power Supply for LDI and LCM	-
3	S_RESET	I	Sub Reset Pin. Initialize the LSI at the low level	-
4	M_RESET	I	Main Reset Pin. Initialize the LSI at the low level	-
5	SUB_CS	I	Sub Chip Select, Active low	-
6	D0	I/O	Bi-Direction Data Bus	GND
7 L	D1	I/O	Bi-Direction Data Bus	GND
8	D2	I/O	Bi-Direction Data Bus	GND
9	D3	I/O	Bi-Direction Data Bus	GND
10	D4	I/O	Bi-Direction Data Bus	GND
11	D5	I/O	Bi-Direction Data Bus	GND
12	D6	I/O	Bi-Direction Data Bus	GND
13	D7	I/O	Bi-Direction Data Bus	GND
14	MLED	I	Anode of LEDS	-
15	MLE1	O	Cathode of LED1	-
16	MLE2	O	Cathode of LED2	-
17	MLE3	O	Cathode of LED3	-
18	MLE4	O	Cathode of LED4	-
19	GND	-	Ground	-
20	GND	-	Ground	-
21	MLED5	O	Cathode of LED5	-
22	MAIN_IF2	I	Main Mode Select2 (See Table 7.1)	-
23	SUB_IF2	I	Sub Mode Select2 (See Table 7.2)	-
24	GND	-	Ground	-
25	BST	O	Indicate the start of Vertical Blank.	OPEN
26	D15	I/O	Bi-Direction Data Bus	GND
27	D14	I/O	Bi-Direction Data Bus	GND
28	D13	I/O	Bi-Direction Data Bus	GND
29	D12	I/O	Bi-Direction Data Bus	GND
30	D11	I/O	Bi-Direction Data Bus	GND
31	D10	I/O	Bi-Direction Data Bus	GND
32	D9	I/O	Bi-Direction Data Bus	GND
33	D8	I/O	Bi-Direction Data Bus	GND
34	_WR	I	Write-Strobe Signal. Active low	-
35	MAIN_CS	I	Main Chip Select, Active low	VCC
36	RS	I	Select Register. High: Control, Low: Index/Status	VCC
37	MAIN_IF1	I	Main Mode Select1(See Table 7.1)	-
38	ID_MAKER	-	Connected to Ground	OPEN
39	SUB_IF1	I	Sub Mode Select1(See Table 7.2)	-
40	_RD	I	Read-Strobe Signal. Active low	VCC

Table 3-2-5. Interface between LCD module and FPCB(in FPCB)

3. Technical Brief

3.2.6 Main&Sub LCD Backlight Illumination

There are 5 white LEDs for the Main LCD and the Sub LCD Backlight circuit which are driven by the Charge Pump(LTC3206EUF). I2C is used for the backlight brightness control. GPIO_46 enables the Charge Pump IC.

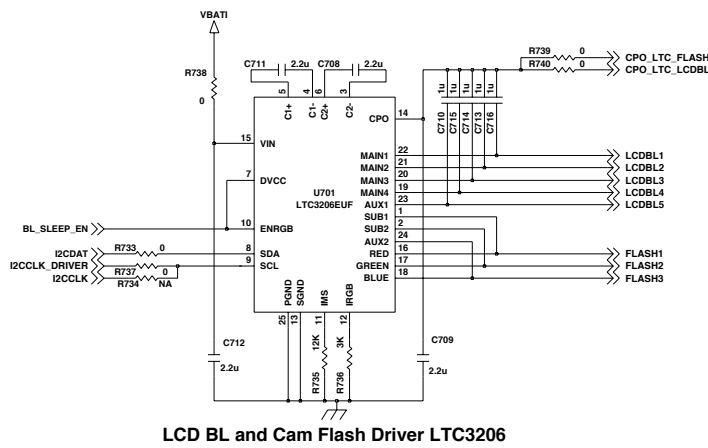


Figure 3-2-8. Charge Pump Circuit for Main&Sub LCD Backlight

3.2.7 Camera Flash LED Illumination

Camera Flash is composed of one White LED module(LEWW-S35LA with 3 LEDs). The Charge Pump(LTC3206EUF) control similarly the flash LED current respectively.

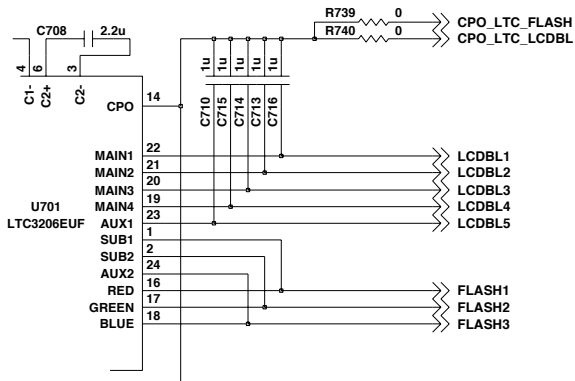


Figure 3-2-9. Camera Flash Charge Pump Circuit

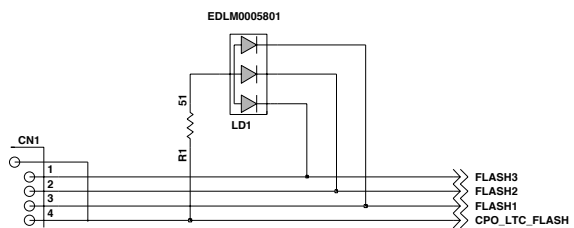


Figure 3-2-10. Camera Flash LEDs Circuit (in FPCB)

3.2.8 Keypad Illumination

There are 19 blue LEDs in key board backlight circuit, which are driven by GPIO32 (KEY_LED_ONOFF) line form Marita.

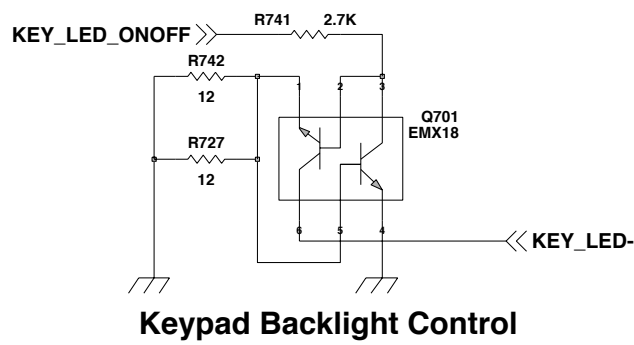


Figure 3-2-11. Keypad Backlight Blue LED Interface

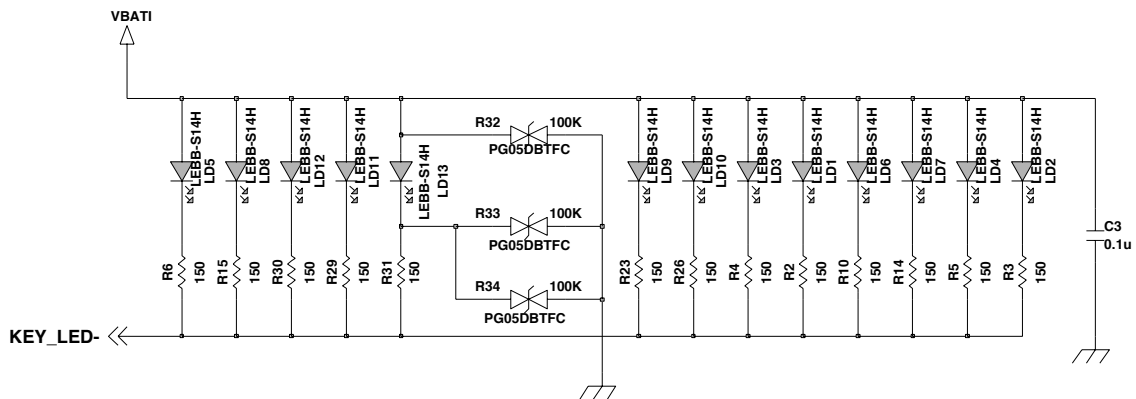


Figure 3-2-12. Keypad Backlight Circuit

3. Technical Brief

3.3 LCD Module

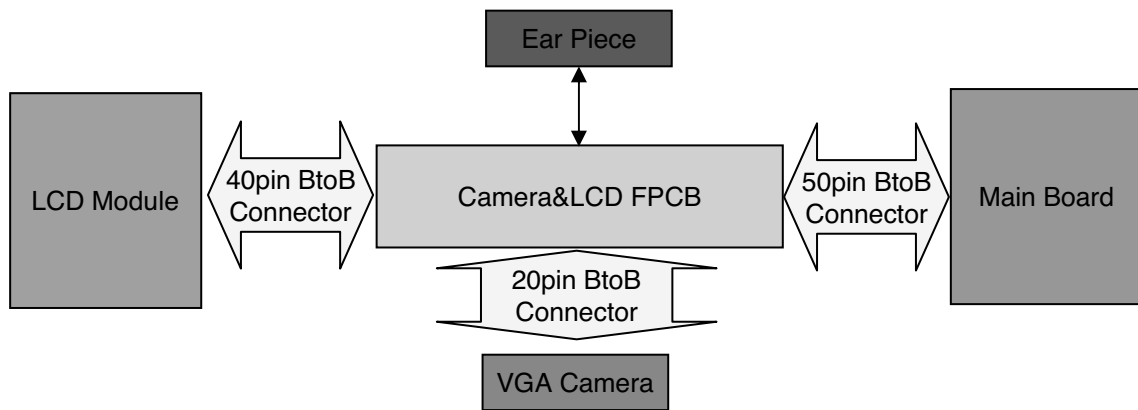


Figure 3-3-1. LCD Module Block Diagram

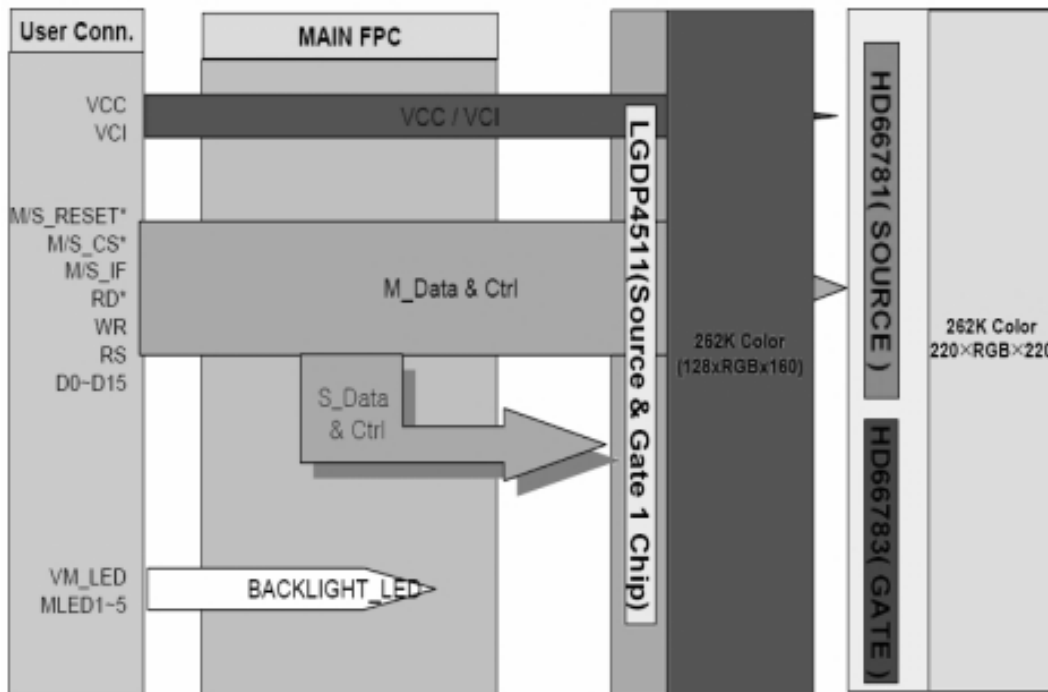


Figure 3-3-2. LCD Module (Main & Sub LCD)

3.4 Analog Baseband (ABB) Processor

3.4.1 Overview of Audio path

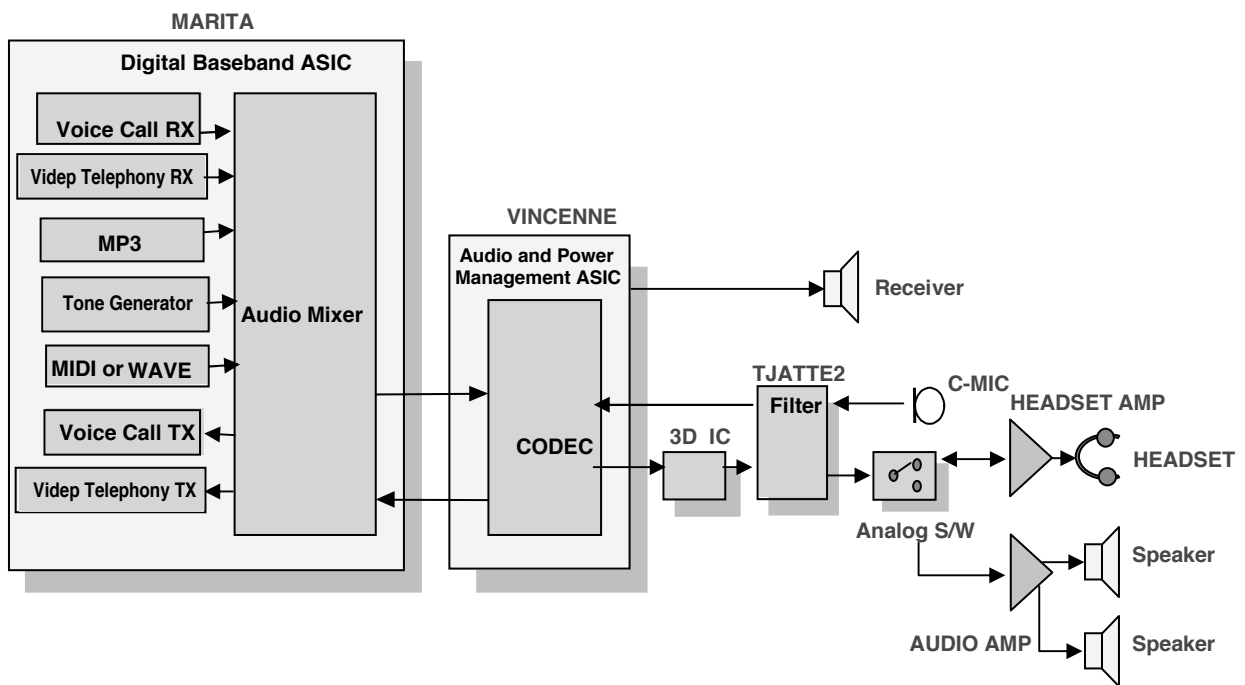


Figure 3-4-1. Audio Path Block Diagram

3. Technical Brief

3.4.2 Audio Signal Processing & Interface

Audio signal processing is divided Uplink path and downlink path.

The uplink path amplifies the audio signal from MIC and converts this analog signal to digital signal and then transmit it to DBB Chip (MARITA).

This transmitted signal is reformed to fit in GSM & WCDMA Frame format and delivered to RF Chip.

The downlink path amplifies the signal from DBB chip (MARITA) and outputs it to Receiver (or Speaker). The audio interface consists of PCM encoding and decoding circuitry, microphone amplifiers and earphone drivers.

The PCM encoder and decoder blocks are two-channel, 16-bit circuits with programmable gain amplifiers (PGA).

The decoder has a receive volume control. The audio inputs and outputs can be switched to normal or auxiliary ports.

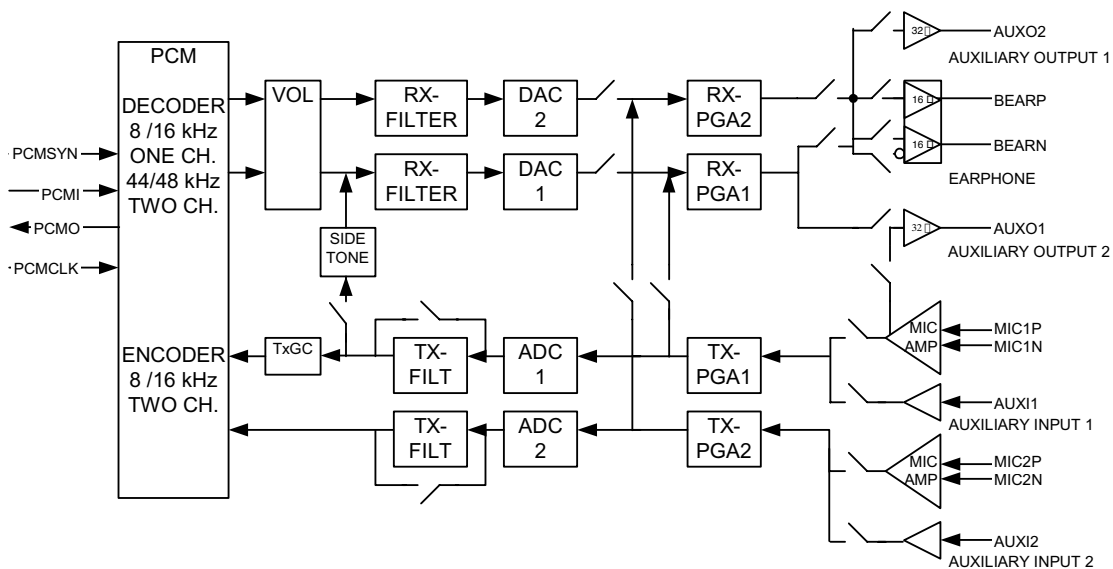


Figure 3-4-2. Audio Interface Detailed Diagram (VINCENNE)

3. Technical Brief

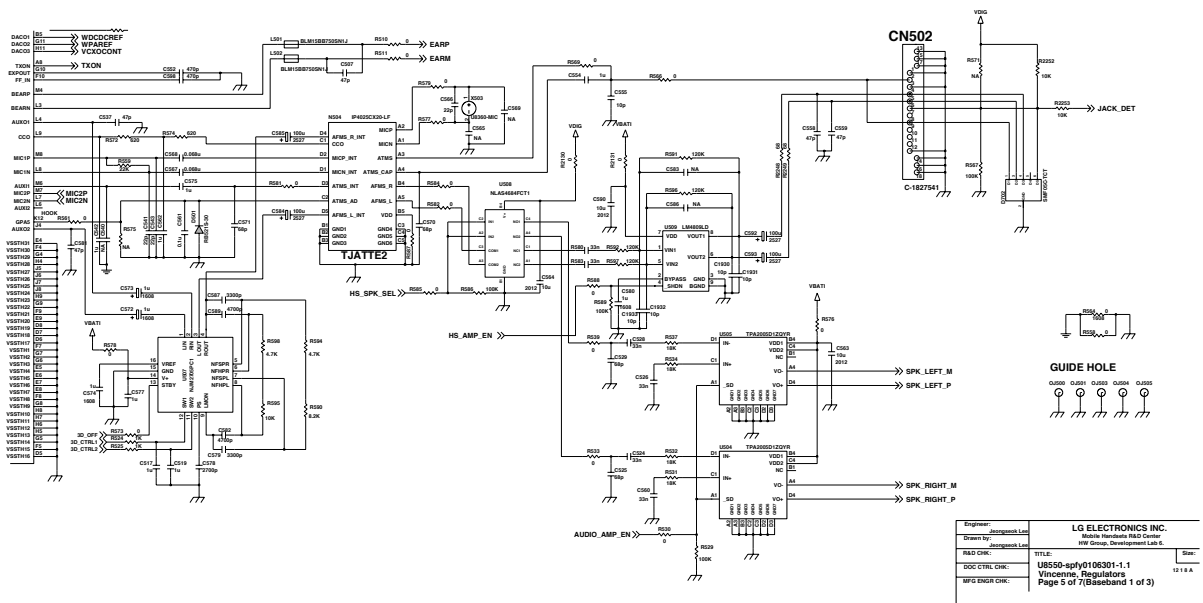


Figure 3-4-3. Schematic of Audio Path

3. Technical Brief

3.4.3 Audio Mode

Audio Mode includes three states(Voice call, Midi, MP3)

Each states is sorted by the total 7 Modes according to external Devices.

(Receiver,Loud Speaker,Headset) Video Telephony Mode Operate on state of the WCDMA Call.

Mode		VINCENNE In / Out Port	
		IN	OUT
Voice call	Receiver Mode	MIC1P/MIC1N	BEARP/BEARN
	Loud Speaker Mode	MIC2P/MIC2N	AUXO1/AUXO2
	Headset Mode	AUXI1	AUXO1/AUXO2
	Video Telephony Mode	MIC2P/MIC2N	AUXO1/AUXO2
MIDI	Only Loud Speaker		AUXO1/AUXO2
MP3	Loud Speaker Mode		AUXO1/AUXO2
	Headset Mode		AUXO1/AUXO2

Table 3-4-1. Audio Mode

3.4.4 Voice Call

A. Voice call Downlink Mode(Receiver, Speaker, Headset)

This section provides a detailed description of the Voice Call RX functions.

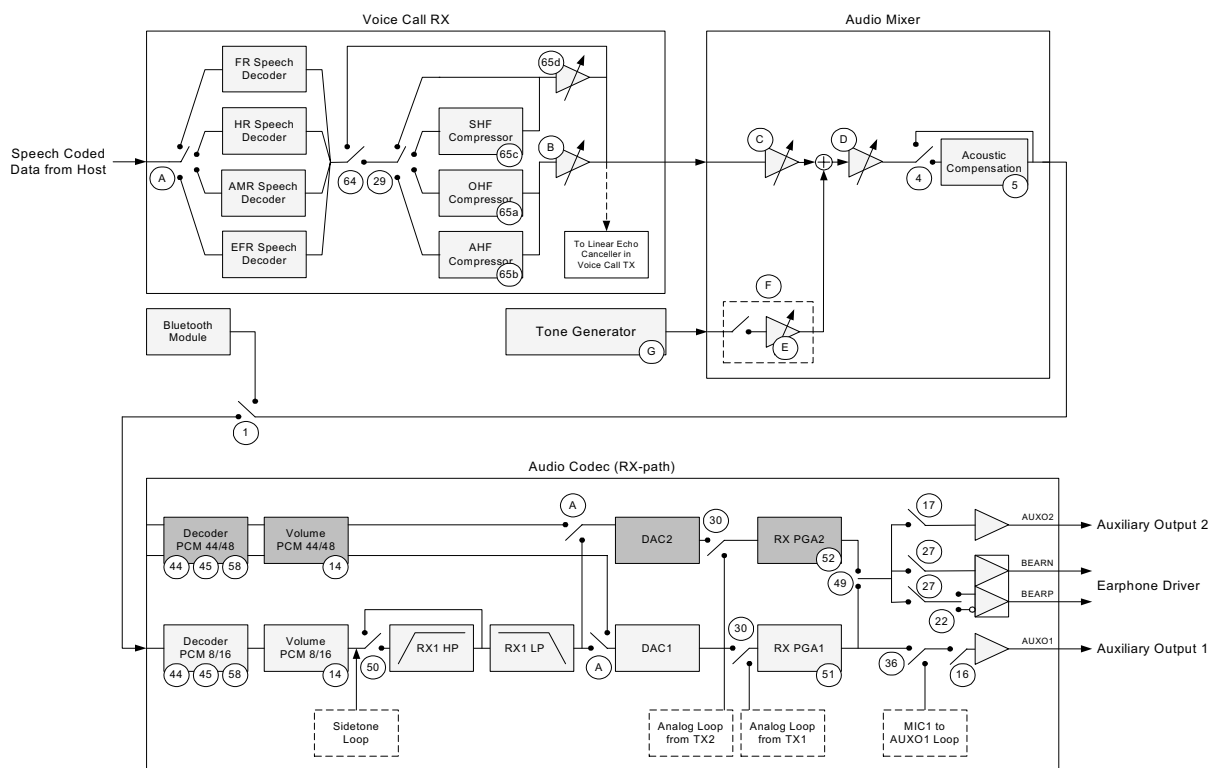


Figure 3-4-4. Voice Call Downlink Scheme

3. Technical Brief

The voice decoder accepts a serial input stream of linear PCM coded speech. The receive band-pass filter is the next step in the CODEC receive path. Following the filter is the DAC, followed by a PGA enabling to adjust or trim the circuit in the product for different sensitivity of the earphone and spread in the RX path. **The final step in the receive path is the earphone amplifier and the auxiliary output. The auxiliary audio amplifier is intended to drive low impedance headphones.** The earphone amplifier and the auxiliary audio outputs can be powered down (muted) via I2C. Both the earphone driver and one of the auxiliary drivers can simultaneously provide an output signal during voice decoding.

- **Receiver Mode** : Earphone amplifier → BEARP/N Port → Receiver(32Ω)
- **Loud Speaker / Video Telephony Mode** : Auxiliary audio amplifier → AUXO1/2 → SURROUND AUDIO PROCESSOR(NJM2705) → TJATTE2 → Analog S/W(NLAS4684) → AUDIO AMP(TPA2005D1) → Speaker(8Ω)
- **Headset Mode** : Auxiliary audio amplifier → AUXO1/2 → SURROUND AUDIO PROCESSOR (NJM2705) → TJATTE2 → Analog S/W(NLAS4684) → HEADSET AMP(LM4809LD) → Head Phone

Loud Speaker Mode has four GPIO switching control ports. It is **3D_CTRL1/2**, **HS_SPK_SEL** and **Audio_AMP_EN**. **HS_SPK_SEL** controls analog switch(NLAS4684) and **Audio_AMP_EN** controls shutdown of AUDIOAMP(LM4809LD). **Video Telephony Mode** has same paths with Loud Speaker Mode.

Mode	3D IC		HS_SPK_SEL	AUDIO_AMP_EN
	3D_CTRL1	3D_CTRL2		
Receiver	--	--	--	--
Headset (amr)	Low	Low	Low	Low
Headset (mp3)	High	Low	Low	Low
Loud Speaker, VT	Low	Low	High	High
3D Speaker (mp3)	Low	High	High	High

Table 3-4-2. Speaker Phone Mode GPIO Control State

B. Voice call Uplink Mode(Receiver, Speaker, Headset)

This section provides a detailed description of the Voice Call TX functions.

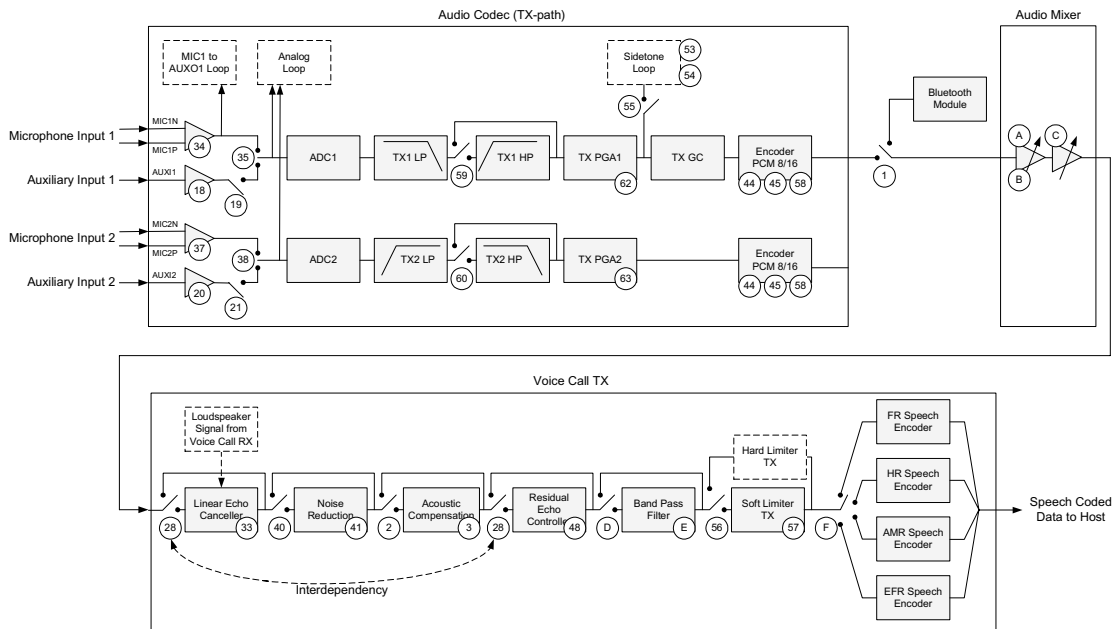


Figure 3-4-5. Voice Call Uplink Scheme

The Uplink supports two microphones and two auxiliary inputs to the speech encoder blocks.

Both microphone inputs are compatible with an electric microphone.

The VINCENNE internal voltage source (CCO) provides the necessary drive current for the electric microphone. The voltage source is via I2C programmable to supply 2.2V or 2.4V.

But the voltage source of our Model is to supply 2.4V.

The auxiliary audio inputs can be used as an alternative source of speech, a source from an external microphone or as an analog loop connection. Figure 3.4.4.2 shows that the audio inputs are fed to the transmit PGAs, which enables to adjust the total gain in the product for different sensitivities of the microphones and spread in the transmit paths. The ADCs are followed by the transmit band pass filters, which accept the maximum output swing that the microphone preamplifiers can deliver without clipping, and maintain a good signal-to-noise ratio. The high pass filter in the TX-paths can be disabled via I2C; still removing the DC offset from the signal.

For one of the two transmit paths, a transmit gain control amplifier precedes the final encoding of the PCM output.

3. Technical Brief

3.4.5 MIDI (Ring Tone Play)

This section provides a detailed description of the MIDI and WAV-file functions.

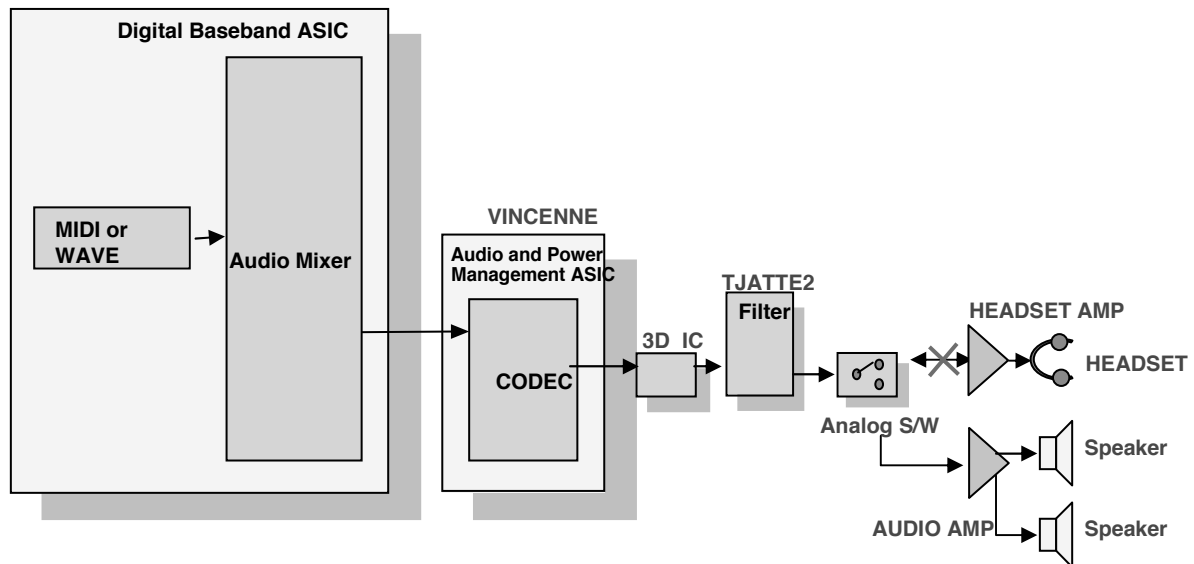


Figure 3-4-6. MIDI Scheme

In Figure 3-4-6, External MIDI path is the same as Voice Loudspeaker downlink Mode, except source in MARITA (DSP and Audio Mixer).

- MIDI : MARITA PCM Decoder → Auxiliary audio amplifier → AUXO1/2 Port → SURROUND AUDIO PROCESSOR(NJM2705) → TJATTE2 → Analog S/W (NLAS4684) → 2 Mono AUDIO AMP(TPA2005D1) → 2 Speaker(8Ω)

3.4.6 MP3 (Audio Player)

This section provides a detailed description of the MP3 file functions.

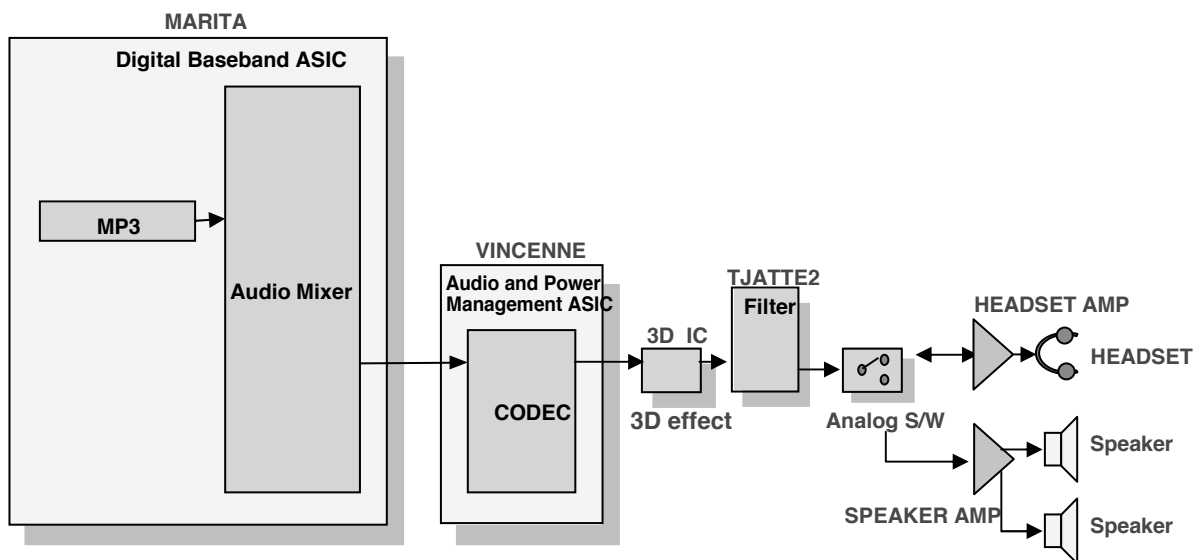


Figure 3-4-7. MP3 Scheme

MP3 function supports PCM 44/48KHz sampling rate. The PCM44/48 RX-path is intended to be used as a 3D surround music headphones and two speakers.

Analog switch(NLAS4684) controls the audio path to the headset or two speakers.

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3.4.7 Video Telephony

This section provides a description of the Video Telephony functions.

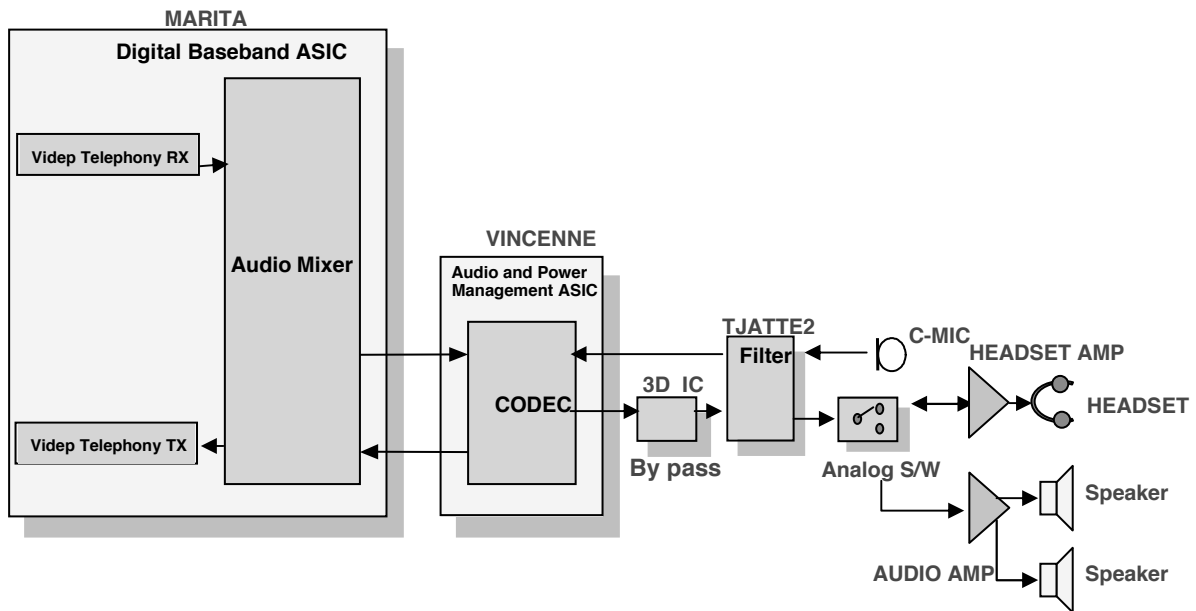


Figure 3-4-8. Video Telephony Scheme

Video Telephony Mode has same paths with Loud Speaker Mode.

3.4.8 Audio Part Main Components

There are 8 components in U8550 schematic Diagram. Part Number marked on U8550 Schematic Diagram.

N0	ITEM	Part Name	Part Number
1	Speaker	EMS1514TLW1P	
2	C-MIC	OBG-415S44	X503
3	3D IC	NJM2705	U507
4	Audio AMP	TPA2005D1	U504, U505
5	Headset AMP	LM4809LD	U509
6	TJATTE2	IP4025CS20	N504
7	Ear-JACK	C-1827541	CN502
8	Analog Switch	NLAS4684	U508

Table 3-4-5 Audio Component List

A. TJATTE2 Description

The TJATTE2 is a 6-channel RC low pass filter array that is designed to provide filtering of undesired RF signals in the 800-2700 MHz frequency band.

In addition, the TJATTE2 incorporates diodes to provide protection to downstream components from Electrostatic Discharge (ESD) voltages as high as 8 kV.

PIN	DESCRIPTION	PIN	DESCRIPTION	PIN	DESCRIPTION	PIN	DESCRIPTION
A1	MICN	B1	GND	C1	CCO	D1	MICN-int
A2	MICP	B2	GND	C2	ATMS_AD	D2	MICP-int
A3	ATMS	B3	GND	C3	GND	D3	ATMS-int
A4	ATMS-cap	B4	AFMS_R	C4	GND	D4	AFMS_R-int
A5	AFMS_L	B5	VDD	C5	GND	D5	AFMS_L-int

Table 3-4-4. TJATTE2 Pin Description

3. Technical Brief

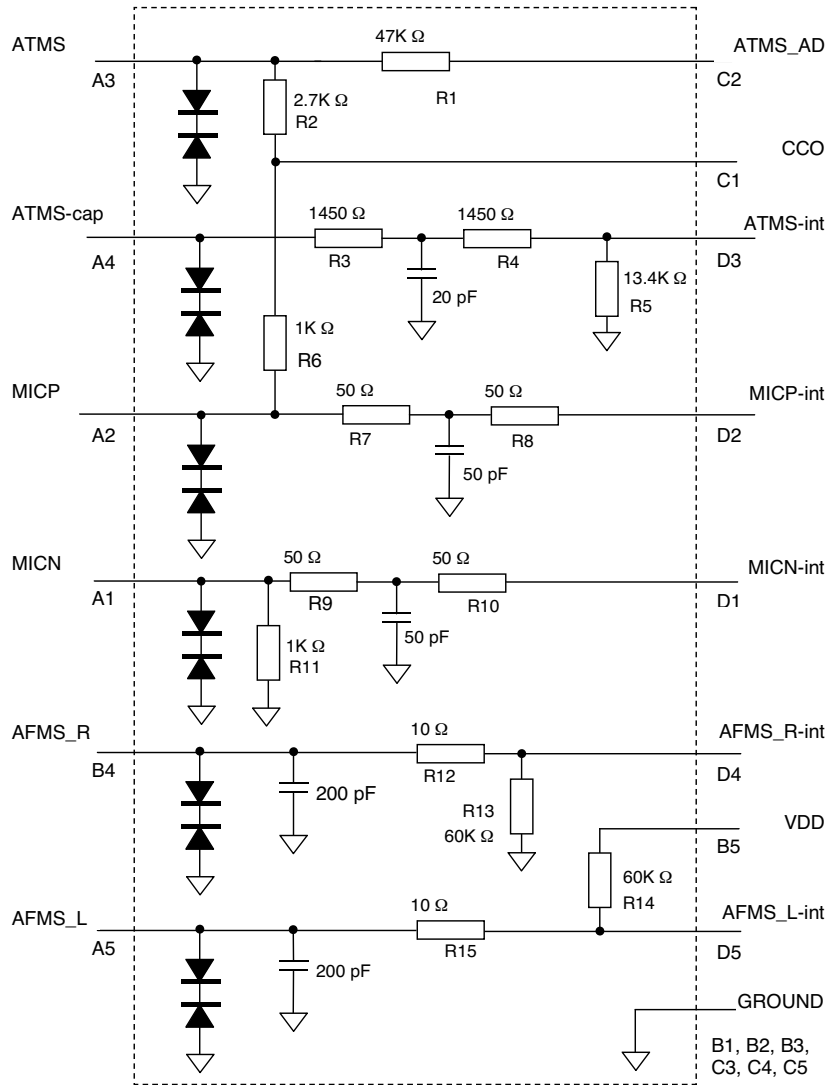


Figure 3-4-9. TJATTE2 Block Diagram

3.4.9 GPADC(General Purpose ADC) and AUTOADC2

The GPADC consists of a 14 input MUX and an 8-bit ADC. The analog input signal is selected with the MUX and converted in the ADC.

The GPADC has a built in controller, AUTOADC2, which is able to operate in the background without software intervention. The AUTOADC2 periodically measures the battery voltage or current. (Fig.2) shows the schematic of GPADC part. The GPADC channel spec is as following (Table 2).

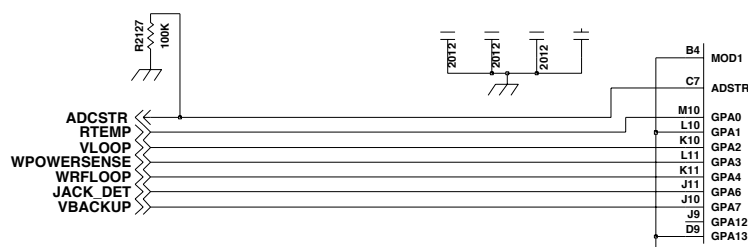


Figure 3-4-10. Schematic of GPADC and AUTOADC2

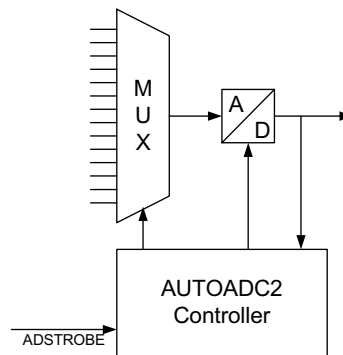


Figure 3-4-11. GPADC and AUTOADC2 Block diagram

ADC 6 channels		
Resource	Name	Description
GPA0	RTEMP	Radio temperature sense
GPA2	VLOOP	Loop voltage sense
GPA3	WPOWERSENSE	Reference voltage for PAM
GPA4	WRFLOOP	Lock inform
GPA6	GPA6	Headset detect
GPA7	VBACKUP	Backup battery

Table 3-4-5. GPADC channel spec

3. Technical Brief

3.4.10 Charger control

A programmable charger in AB2000 is used for battery charging. It is possible to set limits for the output voltage at CHSENSE- and the output current from DCIO via the sense resistor to CHSENSE-. The voltage at CHSENSE- and the current feed to CHSENSE- cannot be measured directly by the GPADC. Instead, the two measuring amplifiers translate these inputs to a voltage proportional to the input and within the range of the GPADC. Figure 3-4-12 shows the schematic of charging control part. This section provides a detailed description of the Voice Call RX functions.

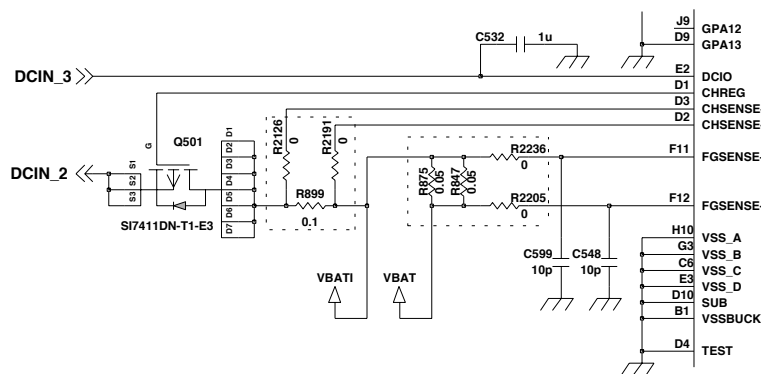


Figure 3-4-12. Schematic of charging control part

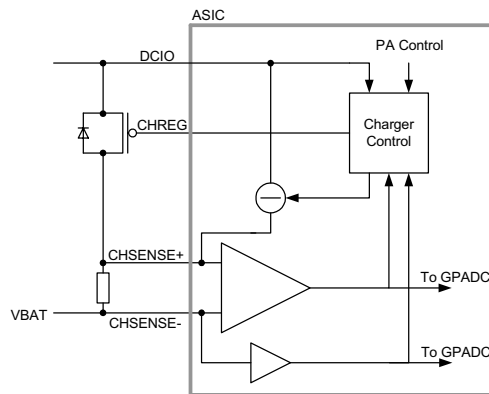


Figure 3-4-13. Battery charging block diagram

Name	Type	Unused	Description
CHSENSE+	Analog	VBAT	Current sensing input positive
CHSENSE-	Analog	VBAT	Current sensing input negative

Table 3-4-6. Charger Control channel spec

3.4.11 Fuel Gauge

AB2000(VINCENNE) supports the measurement of the current consumption/charging current in the U8550 with a fuel gauge block. By constantly integrating the current flowing into and out of the battery, the fuel gauge block is used to determine the remaining battery capacity.

The function of the fuel gauge block is schematically described in Figure 3-4-15. A sense resistor $R_{FGSENSE}$ is connected in series with the battery. The voltage across the resistor, equivalent to the current entering/leaving the battery, is integrated using an ADC block.

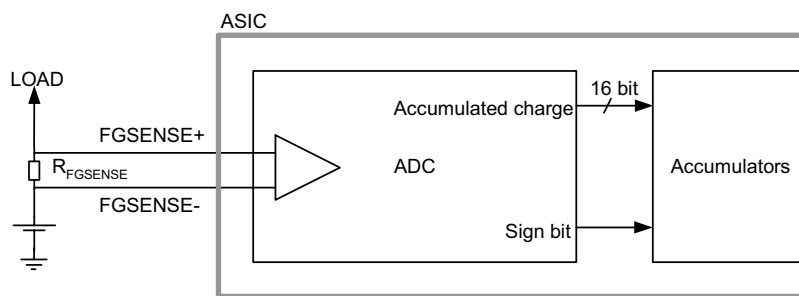


Figure 3-4-14. The analog front-end of the fuel gauge block

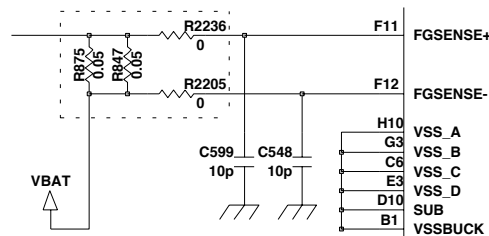


Figure 3-4-15. Schematic of the fuel gauge block

Name	Type	Unused	Description
FGSENSE+	Analog	VBAT	Fuel gauge current sensing input positive
FGSENSE-	Analog	VBAT	Fuel gauge current sensing input negative

Table 3-4-7. Fuel Gauge channel spec

3. Technical Brief

3.4.12 Battery Temperature Measurement

The BDATA node, the constant current source, feed the battery data output while monitoring the voltage at the battery data node with GPADC. This battery data is converted to the battery temperature. Figure 3-4-16 shows the schematic of battery temperature measurement part.

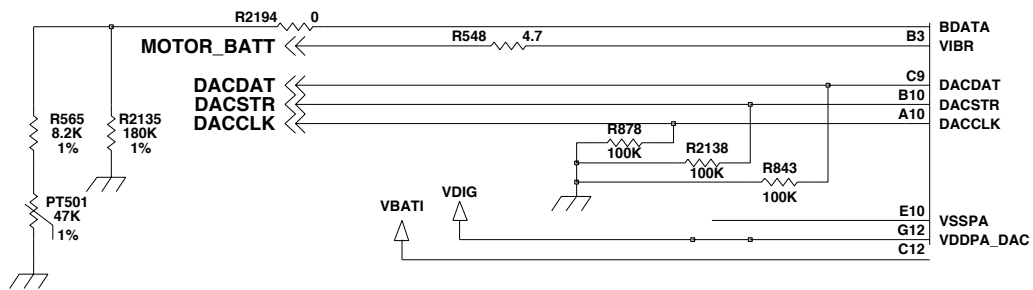


Figure 3-4-16. Battery Temperature Measurement

Name	Type	Unused	Description
BDATA	Digital Input/Output	Unconnected	current output

Table 3-4-7. BDATA channel spec

3.4.13 Charging Part

The charging block in AB2000 processes the charging operation by using VBAT voltage. It is enabled or disabled by the assertion/negation of the external signal DCIO. Part of the charging block are activated and deactivated depending on the level of VBAT. Figure 3-4-17 shows the schematic of charging part.

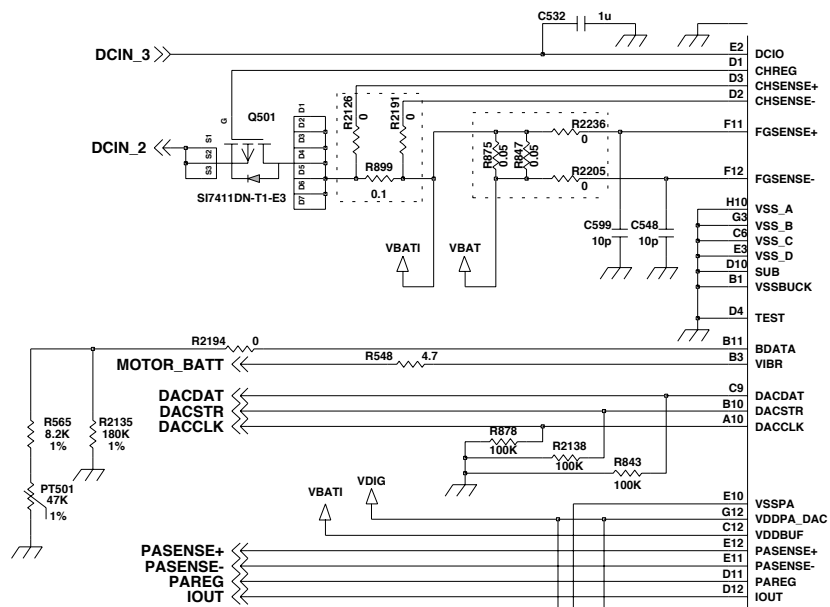


Figure 3-4-17. Schematic of Charging Part

When VBAT is below a certain value, 3.2V, a current generator take care of initial charging of the CHSENSE+ node and internal trickle charge signal is active. This part of the charging block is powered on and active when DCIO is asserted. The DCIO signal is asserted when its voltage is above the voltage at VBAT. As soon as generator is turned off and all parts of the charging block are functional and active.

Battery block indication as shown in Figure 3-4-18

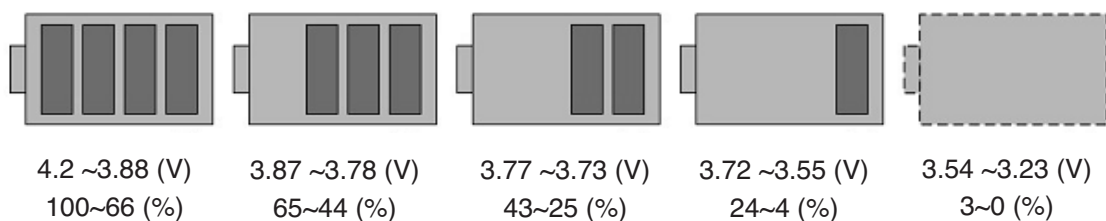


Figure 3-4-18. Battery Block Indication

3. Technical Brief

A. Trickle charging

When the VBAT is below a certain value, 3.2V, a current generator take care of internal trickle charge signal is active. The charging current is set to 50mA.

Parameter	Min	Typ	Max	Unit
Trickle current	30	50	60	mA

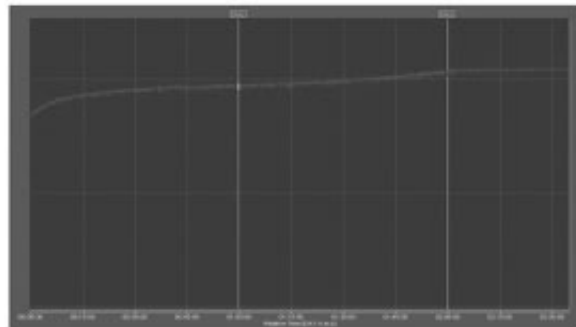
Table 3-4-8. Trickle charging spec

B. Normal charging

When the VBAT voltage is within limits or the internal regulators are turned on, the current source for trickle charging is turned off and all parts of the charging block are active.

The charging method is 'CCCV' (Constant Current Constant Voltage) This charging method is used for Lithium chemistry battery packs. The CCCV method regulates the charge current and the VBAT voltage. This charging method prevents the battery voltage to go above the charge set in the CCCV algorithm. Figure 3-4-19 shows the charging voltage(a) and charging current change(b).

(a) Charging voltage



(b) Charging current

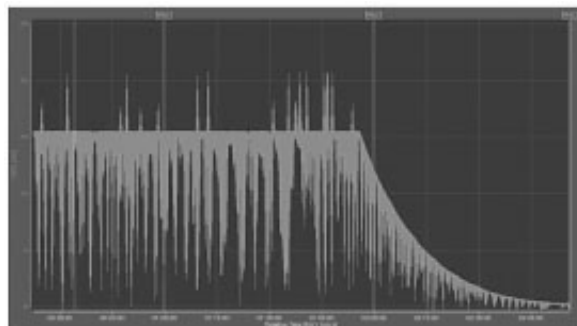


Figure 3-4-19. CCCV charging method

- Charging Method : CCCV (Constant Current Constant Voltage)
- Maximum Charging Voltage : 4.2V
- Maximum Charging Current : 700mA
- Nominal Battery Capacity : 1400 mAh
- Charger Voltage : 4.6V
- Charging time : Max 3.5h
- Full charge indication current (icon stop current) : 80mA
- Low battery POP UP : Idle - 3.50V, Dedicated - 3.54V
- Low battery alarm interval : Idle - 3 min, Dedicated - 1 min
- Cut-off voltage : WCDMA call - 3.15V, ELSE - 3.23V

C. Charging of Extended Temperature

When the battery temperature is outside the normal charging specification, the battery voltage, VBAT is maintained at 3.7V.

- Under 0°C : Extended temperature
- From 0°C to 45°C : Normal charging temperature
- Over 45°C : Extended temperature

3. Technical Brief

3.5 Voltage Regulation

3.5.1 Internal Regulation

There are LDO (Low Drop Output) regulators and BUCK converter in AB2000 (Vincenne) chip. LDO regulators and BUCK converter generate the following voltages : 1.5V, 1.8V and 2.75V. The output of these LDOs supply VDD-A, VDD-B and VDIG with 2.75V. BUCK converter steps down the VBAT to 1.5V for VCORE and VRTC, and to 1.8V for VMEM voltage. The output of these LDOs and BUCK converter are as following (Table 1). (Fig.1) shows the power supply of each module in U8550.

3.5.2 External Regulation

- 1.5V LDO - supply 1.5V for Wanda core
- 1.5V LDO - supply 1.5V for Marita PLL
- 2.4V LDO - supply 2.4V for SPK_MIC_BIAS
- 2.8V LDO - supply 2.8V for Mega Camera
- 2.8V LDO - supply 2.8V for VGA Camera
- 2.85V LDO - supply 2.8V for Bluetooth and TransFlash
- 3.3V LDO - supply 3.3V for USB
- CHARGER PUMP : supply up to 400mA continuous output current for LCD back light and Camera Flash LED

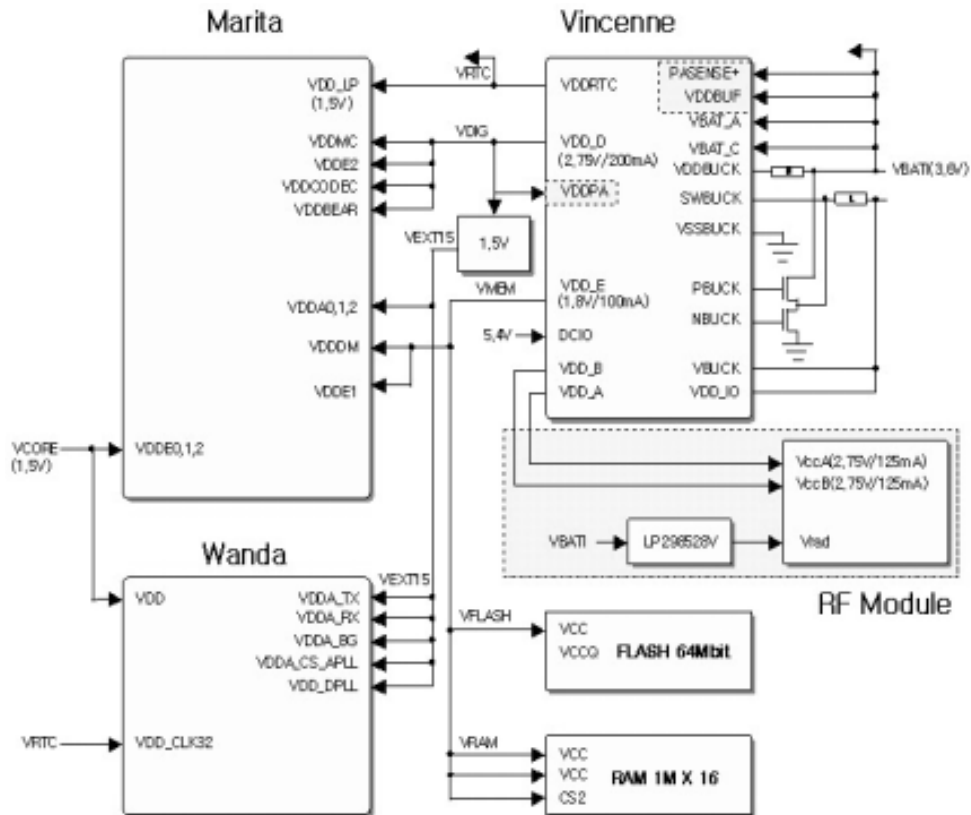


Figure 3-5-1. Power supply scheme

Pin	Name	Type	Output voltage	Description
B12	VDD_A	Power Supply	2.75V	Supply output
A11	VDD_B	Power Supply	2.75V	Supply output
M11	VDD_D	Power Supply	2.75V	Supply output
L12	VDD_E	Power Supply	1.8V	Supply output
L2	VDDL	Power Supply	1.5V	Low Power supply output
A2	VDDBUCK	Power Supply	Unused: VBAT	Buck converter switch supply
B1	VSSBUCK	Power Supply	GND	Buck converter switch ground

Table 3-5-1. LDO and BUCK

3. Technical Brief

3.6 General Description of RF Part

The RF part includes a tri-band GSM/DCS/PCS part (900, 1800 and 1900MHz) and W-CDMA part for IMT-2000 (UL 1900MHz, dl 2100MHz). It also contains Antenna Switch, WCDMA duplexer, WCDMA Power Amplifier and GSM Power Amplifier.

The whole structure of Radio part is shown in Figure 3-6-1.

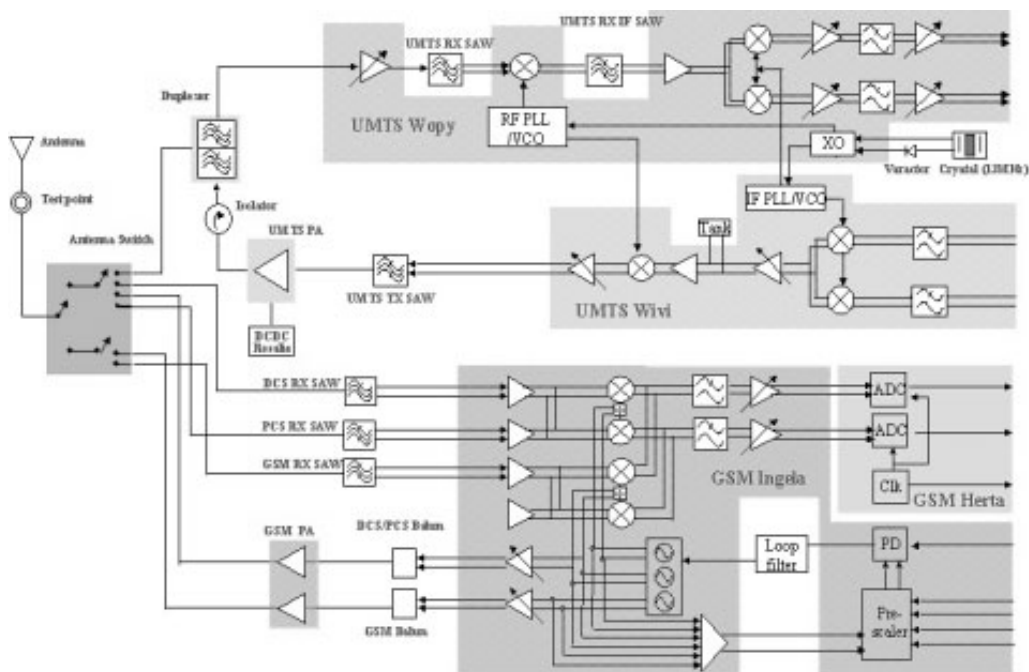


Figure 3-6-1. Block diagram of RF part

Starting at the antenna end, an antenna switch provides switching capability needed for four frequency bands (900, 1800, 1900 and 2100MHz). For the W-CDMA part, duplexer is included to facilitate the simultaneous transmission and reception required for the FDD mode.

The main components in the radio are Wopy (W-CDMA receiver ASIC), Wivi(W-CDMA transmitter ASIC), Ingela(GSM/GPRS transceiver) and two power amplifiers.

The mixed-signal circuit ASIC, Vincenne provides power supply for the main RF components.

The control flow for the Radio is shown in Figure 3-6-2

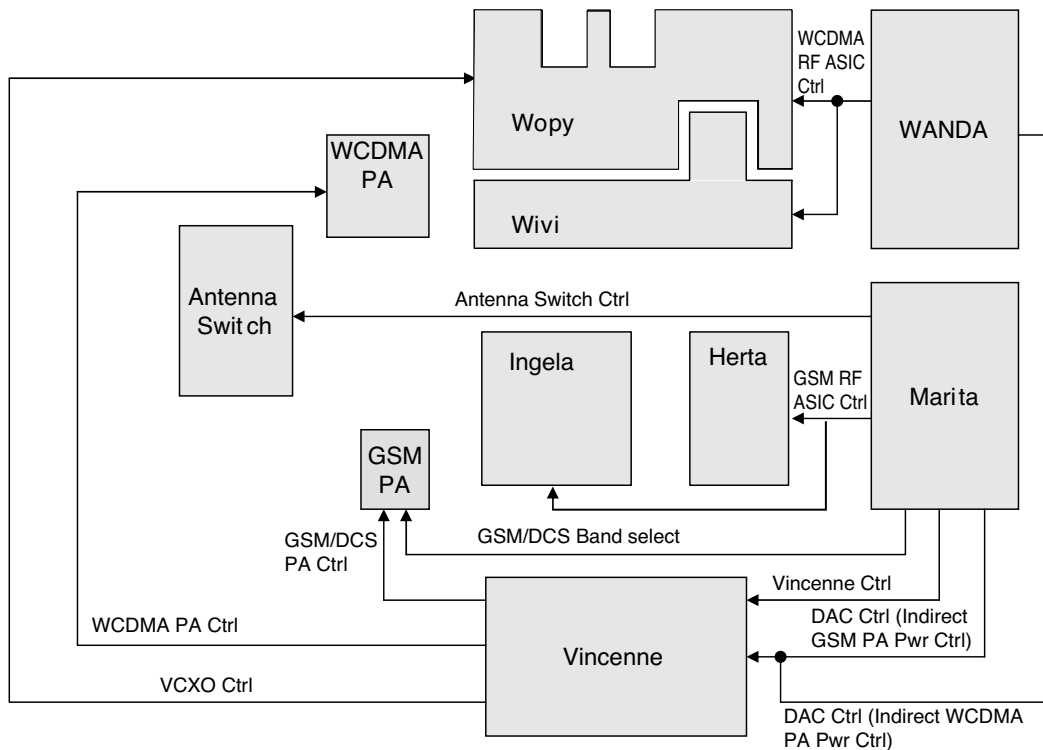


Figure 3-6-2. RF control signal flow diagram

The MARITA(the main processor) controls the overall radio system. In the GSM/GPRS air interface mode, this control is handled via direct interfaces to individual RF components.

The MARITA(the main processor) also handles the antenna switch mechanism for selection of mode. In the W-CDMA mode, the RF system is managed via the Wanda (WCDMA digital base-band coprocessor ASIC) and its DSP processor.

3. Technical Brief

3.7 GSM Mode

3.7.1 Receiver

The received RF signal on the antenna connector arrives via antenna switch at external band pass filters for band selectivity. One filter is required per supported GSM band.

The corresponding LNA amplifies the signal for optimum noise suppression.

The LNA output signal is mixed with the on-channel LO generated by the proper VCO and transformed into a Q and an I signal. The I and Q signals are low pass filtered with two parallel high dynamic range filters.

Finally, the filtered I and Q signals are converted by a sigma-delta converter into two 13 Mbps digital bit streams by Herta(A/D converter), then fed to the Marita baseband ASIC.

A. Front end

RF Front end consists of antenna, antenna switch(FL101), three RF SAWs(FL402, FL403, Z401) and triple band LNAs integrated in transceiver(N405). The Received RF signals (GSM 925MHz ~ 960MHz, DCS 1805MHz ~ 1880MHz, PCS 1930MHz ~ 1990MHz) are fed into the antenna or coaxial connector. An antenna matching circuit is between the antenna and the coaxial connector.

The Antenna Switch(FL101) is used to select the signal path, which is one of WCDMA, GSM RX, GSM TX, DCS RX, DCS/PCS TX and PCS Rx. The control signals VC1, VC2 and VCG of antenna switch (FL101) are connected to Marita baseband ASIC(D601) to control the signal path.

For example, when the GSM RX path is turned on, the received RF signal, which has passed through the antenna switch, is filtered by GSM RF SAW filter to suppress any unwanted signal except GSM RX band. The filtered RF signal is amplified by an LNA integrated in the transceiver IC(N405) and is passed to a direct conversion demodulator. The process for DCS RX is also the same as GSM RX case. The logic for antenna switch is given below Table 3-7-1.

	VC1	VC2	VCG
GSM TX	0V	0V	2.8V ~ 3.0V
GSM RX	0V	0V	0V
DCS/PCS TX	2.8V ~ 3.0V	2.8V ~ 3.0V	0V
DCS RX	0V	2.8V ~ 3.0V	0V
PCS RX	2.8V ~ 3.0V	0V	0V
WCDMA	0V	0V	0V

Table 3-7-1. Antenna Switch logic

B. Receiver Block

The circuit contains one frequency down-conversion section for each receive band and a common base band amplifier and filter section. The GSM900 RF part consists of a low noise amplifier followed by high dynamic range mixers.

The DCS 1800 and PCS 1900 RF part also have low noise amplifier connected to the other mixers.

The amplified RF signal is mixed with the quadrature local oscillator signal to create in-phase (I) and quadrature phase (Q) baseband signals. The I and Q signals are then buffered and low pass filtered. The same baseband circuitry is used for all bands.

Balanced signals are used for minimizing cross talk due to package parasitics. An impedance level at RF of 150 ohms for the GSM 900 input and 50 ohms for the DCS 1800/PCS 1900 input is chosen to minimize current consumption at best noise performance.

The low gain mode in GSM 900 is used in high input signal mode. There is no gain switch in DCS 1800/PCS 1900.

Figure 3-7-1 shows a block diagram of the receiver block.

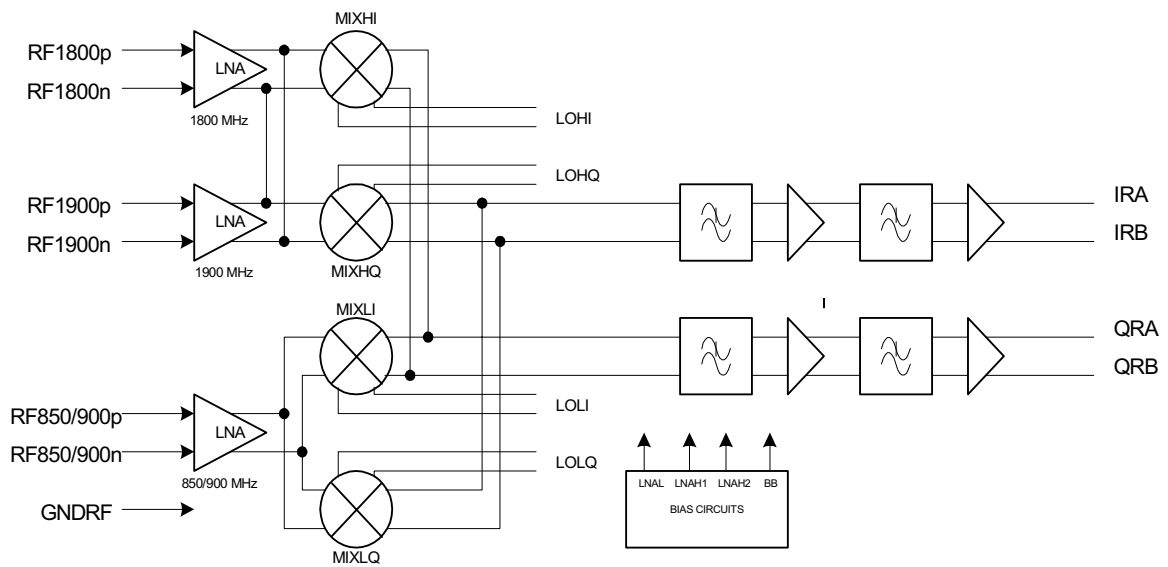


Figure 3-7-1. Block diagram of receiver part

3. Technical Brief

C. LO Block

The LO signals from the receive VCO section drive the dividers for GSM 900, DCS 1800 and PCS 1900 respectively to provide quadrature LO signals to the receive mixers. The LO signal is also supplied to the prescaler and transmit output buffer.

Figure 3-7-2 shows a block diagram of the LO block.

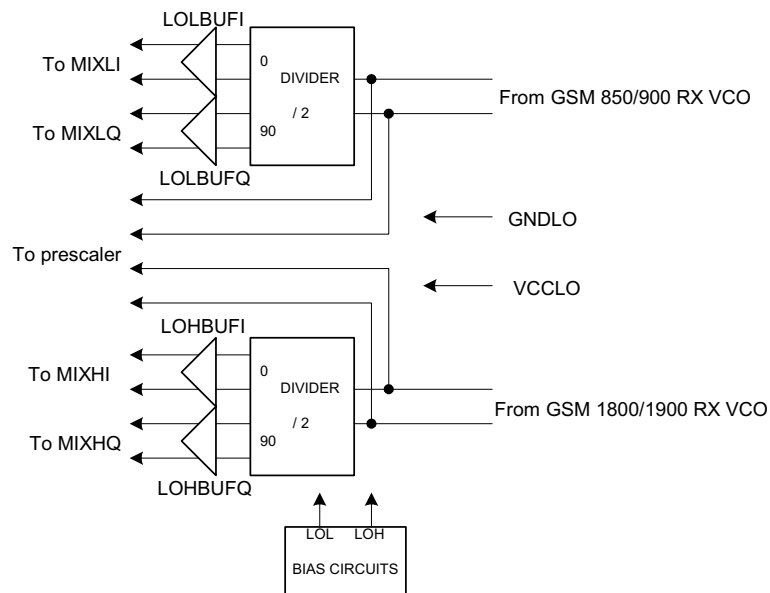


Figure 3-7-2. Block diagram of the LO part

D. VCO Block

The VCOs are fully integrated balanced LC oscillators with on-chip resonators.

The receive VCOs run on double frequency.

Different frequency ranges can be selected in the VCOs for GSM, DCS and PCS band operation.

The VCOs are supplied from a separated external voltage regulator to avoid frequency pushing and up conversion of low frequency noise. A separate ground pin is also used as varactor ground reference to prevent DC voltage drop changes from affecting the VCO frequency.

Figure 3-7-3 shows a block diagram of the VCO block.

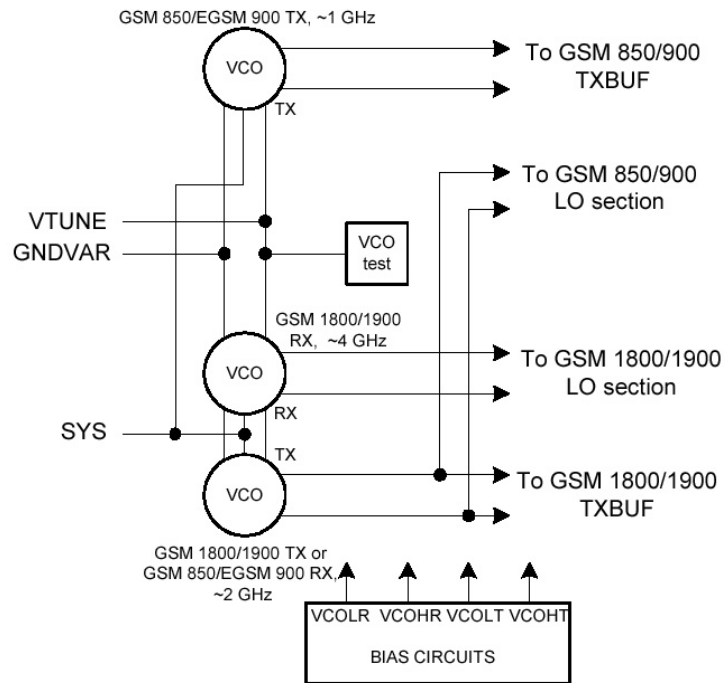


Figure 3-7-3. Block diagram of the VCO part

3. Technical Brief

E. PLL Block

The PLL consists of a programmable prescaler with multiple division ratios and a phase and frequency detector with a charge pump with programmable output current. Channel frequency selection and transmitter modulation is controlled via the prescaler modulus inputs MODA ~ MODD and the prescaler offset value N offset. The MODA ~ MODD signals could be delayed 0, 5, 10 or 15 ns with MD bits to be synchronized with the XO signal.

Figure 3-7-4 shows a block diagram of the PLL block.

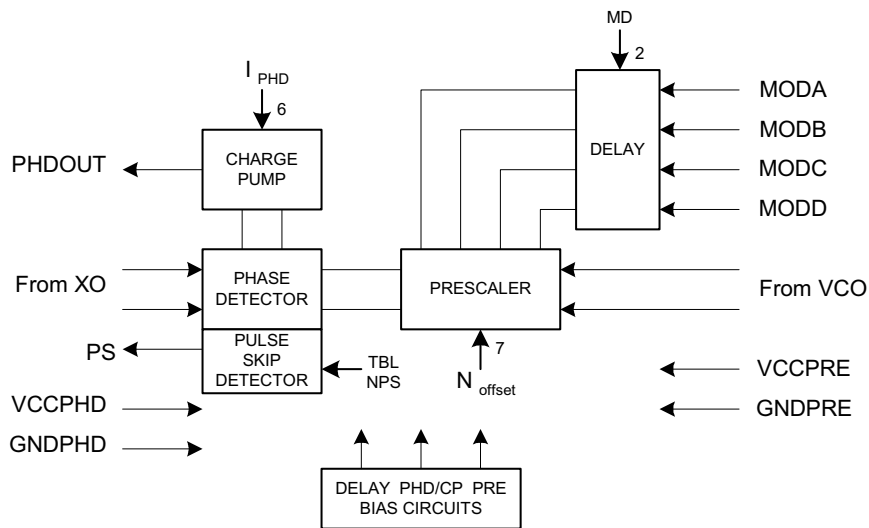


Figure 3-7-4. Block diagram of the PLL part

3.7.2 Transmitter

A 4-bit sigma-delta bit stream comes from the Marita ASIC including both channel information and the GMSK phase information. Via the 3-wire control bus also driven from Marita, the selection of transmitter band is made. The 4bits from the bit stream provides the fine-tuning of the division ratio before going to the divider of the used VCO (low band, 900MHz or high band, 1800/1900MHz).

The modulated VCO signal is fed to the output buffer. One buffer is available for each of the low and high bands. Trimming capability is included for best match versus the PA used.

The GSM/GPRS transceiver, Ingela, output is passed to the dual-band PA that after amplification feeds the signal via a low pass filter to the antenna switch and further to the antenna.

The transmit block consists of two differential high power transmit output buffers with controllable output power. The modulated transmit signal from the VCO buffer is amplified to a level suitable to drive the external power amplifier. The buffer outputs are of open collector type and must be terminated into a suitable load.

Figure 3-7-5 shows a block diagram of the transmitter block.

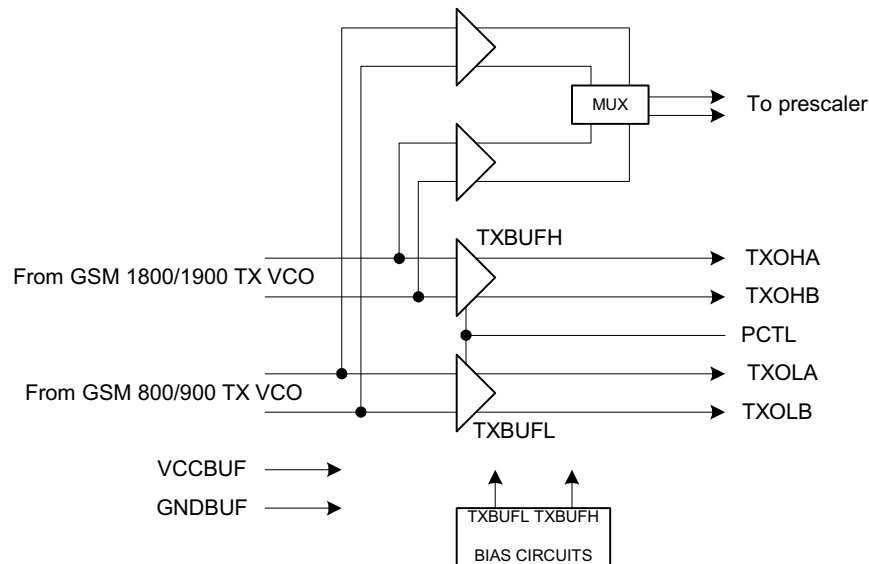


Figure 3-7-5. Block diagram for the transmitter

3. Technical Brief

A. Power Amplifier

The Power Amplifier (N401) is intended for use in EGSM and DCS/PCS mobile equipment.

It is a module with two parallel amplifier chains, with one chain for the EGSM transmitter section and one for the DCS/PCS transmitter section. Each chain amplifies the RF signal from the respective transmitter to the antenna. The power amplifier supports class 10.

Band selection and the output power level of the RF amplifier are controlled by discrete signals V_{band} and V_{apc} respectively from the digital baseband controller ASIC(Marita).

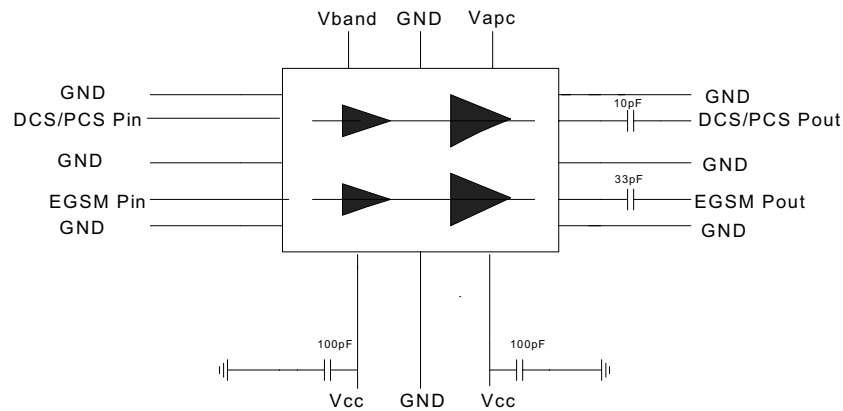


Figure 3-7-6. Block diagram of the Power Amplifier with Two Parallel chains

3.8 WCDMA Mode

3.8.1 Receiver

The received RF signal on the antenna connector arrives via the antenna switch to the duplexer. The duplexer directs the signal to the LNA, which resides in Wopy (W-CDMA Receive ASIC) as every other active part of the radio receiver. The LNA has two different gain settings.

From the output of the LNA, the signal is fed to the input of a RF SAW filter, and then appears at the differential output of the filter. The differential output of the RF SAW filter is connected to the differential mixer input, and the received signal is down-converted to a 190MHz IF frequency (with the RFLO signal) by the mixer.

At 190MHz, the signal is filtered in a differential (input and output) IF SAW filter, with the approximate bandwidth of 4MHz, and then again the signal is fed to Wopy (W-CDMA Receive ASIC), this time to the differential IF input, which also has a LNA.

From the 190MHz, the signal is mixed down to base-band I and Q which represented signals (using the IFLO signal). Finally the signals are filtered in low pass filters and amplified in baseband VGAs.

The I and Q represented signals appear at the output of Wopy (W-CDMA Receive ASIC) as differential voltages.

The large signal gain provided by the processing steps from the antenna down to base-band gives a DC offset at the outputs of Wopy (W-CDMA Receive ASIC). To eliminate this, there are DC-offset compensation loops included, one in the VGA of each of the I and the Q signals.

A. IFLO Section

The balanced IFLO signal from an external IFVCO drives the divider to provide quadrature LO signals to the RxIF mixers. The LO buffers amplifies the signal to a suitable amplitude and DC level to drive the RxIF mixers.

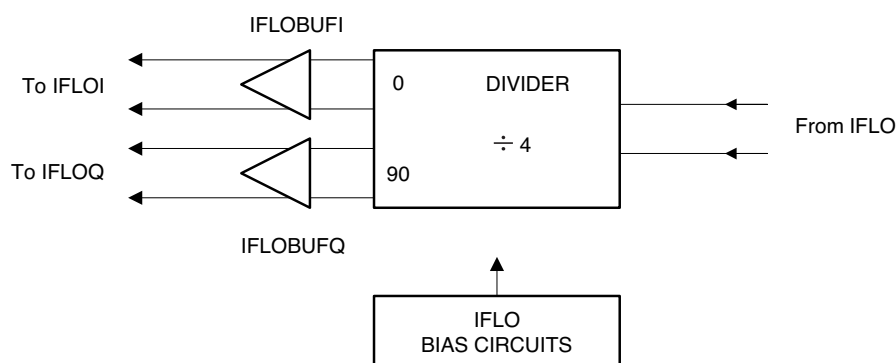


Figure 3-8-1. Block diagram of the IFLO section

3. Technical Brief

B. RFLO Section

The VCO is a fully integrated balanced LC oscillator with on-chip resonator. An on-chip varactor is used to control the frequency over the desired tuning range.

A separate external voltage regulator supplies the VCO with power to avoid frequency pushing and up conversion of low frequency noise. A separate ground pin is also used as varactor ground reference to prevent DC voltage drop changes from affecting the VCO frequency. Via the serial interface, the VTUNE voltage can be set to $VCC/2$ to check the center frequency of the VCO. The PLL consists of a programmable prescaler with multiple division ratios and a phase and frequency detector with a charge pump with programmable output current.

Channel frequency selection is set via the serial interface.

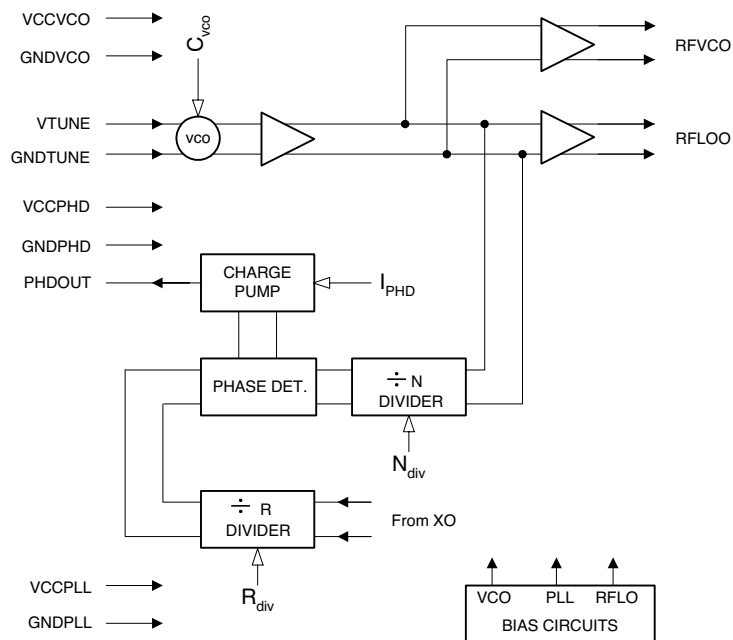


Figure 3-8-2. Block diagram of the RFLO section

C. Reference Section

The reference block consists of a balanced oscillator and a buffer amplifier. The crystal unit and the feedback capacitors are external. The current consumption when only the reference oscillator and the output buffer are activated must be kept to an absolute minimum.

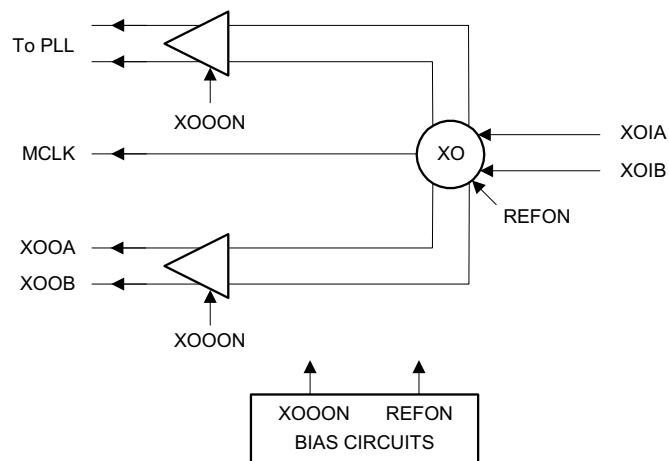


Figure 3-8-3. Block diagram of the Reference section

3. Technical Brief

3.8.2 Transmitter

Analogue differential signals (currents), representing I and Q, are sent to the radio ASCI Wivi (W-CDMA Transmitter ASIC) from the D/A converter in Wanda (W-CDMA digital base-band coprocessor ASIC). The signals are filtered in a reconstruction filter and then modulated up to 380MHz (using the IFLO signal). The signal is then amplified in a VGA and filtered in an external filter (an LC filter). After filtering, the signal is mixed to its final frequency (using the RFLO) and amplified in a differential output RF buffer with two different gain settings (high gain or low gain).

The differential RF signal is fed into a SAW filter with a single ended output, and is then amplified in a stand-alone RF buffer. After the RF buffer, the signal is filtered again in a SAW filter before it is fed to the PA (Power Amplifier).

In the PA the signal is amplified for the last time before leaving the radio. After the PA, the signal is sent through an isolator and through the duplexer, which directs the transmit signal to the antenna connector via the antenna switch.

The PA has variable supply voltage, which adapts itself by means of a control loop so that the linearity of the PA is kept constant. The variable supply voltage is provided from the battery through a DC/DC converter and a signal linearity detector sits at the PA output. The detected signal at the PA output is compared with a reference (supplied by the Vincenne, the mixedsignalcircuit ASIC), and the error signal is used in a loop filter, which provides the control signal to the DC/DC converter.

A. Reconstruction Filters

The reconstruction filters consist of input buffers that provide the correct DC biasing for the preceding DAC in the digital baseband controller, and a low-pass filter for removing the unwanted high frequency components from the baseband input waveform.

The filter inputs are adapted for use with a current-source type of input signal.

B. IQ-modulator

The IQ-modulator receives the incoming I and Q analog baseband signals at baseband frequency and converts them to an intermediate frequency of 380MHz.

C. Variable Gain Amplifier(VGA)

Comprising two cascaded variable gain amplifiers, the VGA-together with the RF mixer-controls the power of the transmitter.

The first of these two amplifiers, the so-called QVGA, enables fine-tuning of the transmitter by varying the gain in 0.25dB steps, that is 0/0.25/0.5/0.75dB. The second amplifier provides a 54dB gain range in 1 dB steps (54steps = 55 levels).

D. IF Band Pass Filter (IFBP)

The IF filter suppresses spurious signals and eliminates unwanted frequency components generated in the IQ modulator and subsequently amplified in the VGA. The filter is tuned using an external RLC load as shown in Figure 3-8-4.

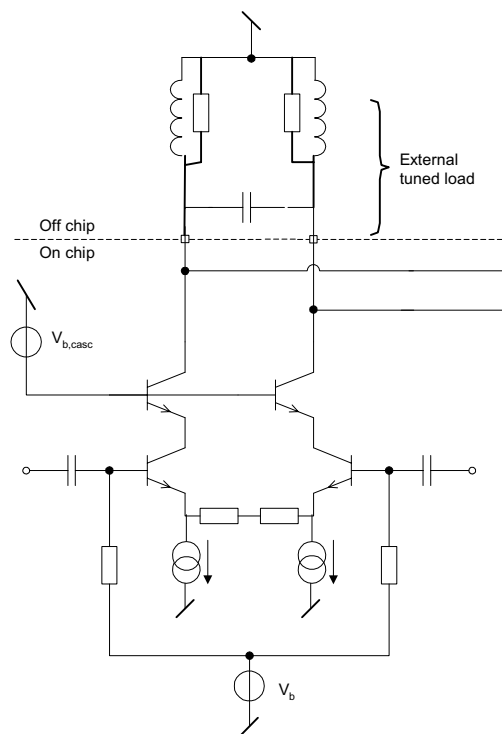


Figure 3-8-4. Principle Schematic of the IFBP

3. Technical Brief

E. RF Mixer and Buffer

The RF mixer converts the signal output from the IF BP filter from an intermediate frequency (IF) to the final radio frequency (RF). The mixer can be switched between three different gain levels: high gain (HG), medium gain (MG), and low gain (LG).

The LO buffer provides the buffering for either an internal LO signal generated within the internal RFPLL, or an external LO signal applied to the RFLO/RFLOBAR pins.

External DC blocking is necessary for the external LO signal.

The RF buffer is used to drive an external PA stage. The buffer is of an open-collector design.

The gain switching together with the VGA amplifier at IF will enable an output power control in 0.25 dB steps over no less than 80dB.

The programmable bias in the high and mid-gain settings is specified as a reduction of bias current from the maximum bias condition. It should achieve a reduction of bias current from the nominal value of 17mA to 3mA (signal ended) in 7 steps.

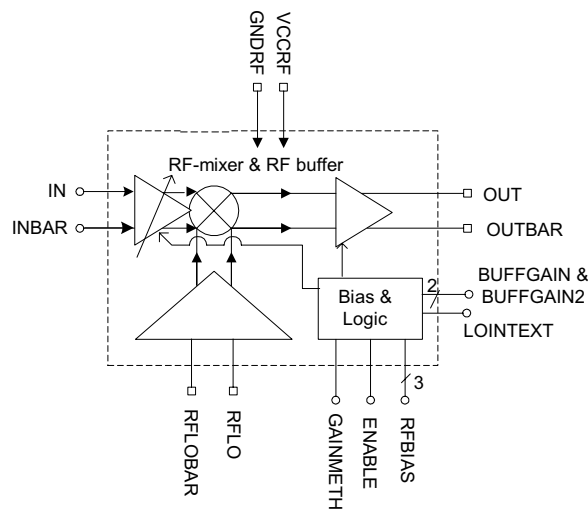


Figure 3-8-5. Block Diagram of RF Mixer and Buffer

F. Power Amplifier

The N302(RF9266) is a high-power, high-efficiency linear amplifier module targeting W-CDMA transmitter ASIC. The module is fully matched to 50Ω for easy system integration and utilizes advanced GaAs HBT process technology. The PA features an integrated RF power output detection network and is compatible with DC-DC converter operation in DC power management applications. Additionally, a variable bias-current allows the idle current to be adjusted for optimum performance at a given RF output power.

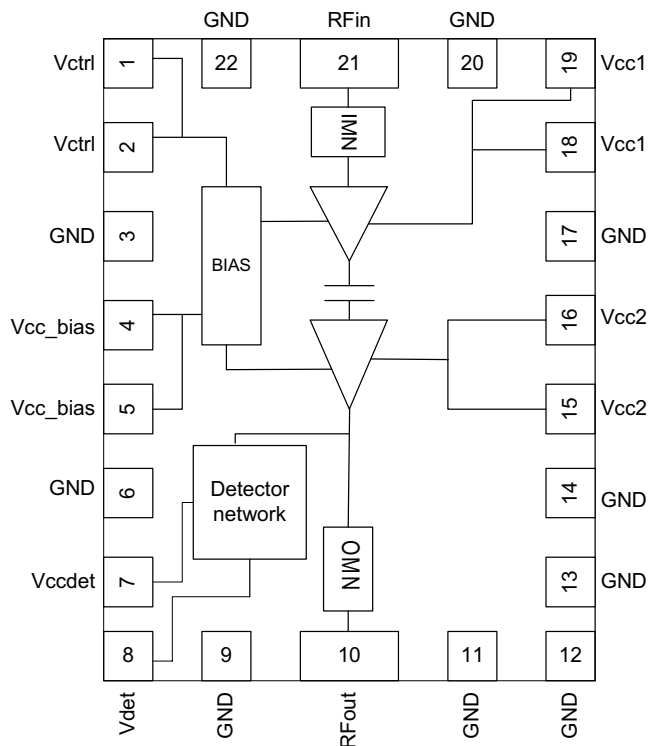


Figure 3-8-6. Block Diagram of W-CDMA power amplifier

3. Technical Brief

3.8.3 Frequency Generation

The Wopy (W-CDMA Receive ASIC) contains the active elements for a 13MHz VCXO, which is designed to be the reference frequency of the UE.

There are two synthesizers in the W-CDMA part of the radio, an intermediate frequency (IF) synthesizer and a radio frequency (RF) synthesizer. They generate the Intermediate Frequency Local Oscillator (IFLO) and Radio Frequency Local Oscillator (RFLO) signals. Both synthesizers are used in both the transmitter and the receiver, which gives the radio a fixed duplex distance of 190MHz.

The RF synthesizer is in the Wopy (W-CDMA Receive ASIC), except for the loop filter, which is external. The 13MHz clock is used as the reference, and the phase detector frequency is 200kHz. The programmable divider makes the RF synthesizer cover the 2300~2360MHz band.

The IF synthesizer is in the Wivi (W-CDMA Transmitter ASIC), except for the loop filter.

The 13MHz is used as the reference, and the phase detector frequency is 1MHz. The IF VCO runs at 1520MHz given that the (programmable) reference divider is set to 13.

The synthesizers are controlled by Wanda (W-CDMA digital base-band coprocessor ASIC) via the serial bus to Wivi (W-CDMA Transmitter ASIC) and Wopy (W-CDMA Receive ASIC).

A. IF PLL

The IF LO frequency synthesis comprises the four following parts:

- Input buffer: A 13MHz input buffer with DC-biasing provided at source.
- VCO: Operating on 1.52GHz which is 4times the TX-IF frequency (380MHz) and 8 times the RX-IF (190MHz), this is a fully integrated balanced LC oscillator with on-chip resonator. On-chip varactors are used to tune the VCO frequency.
- Prescaler
- Phase-detector with charge pump

For maintaining check on the VCO center frequency, the tuning voltage is set to $V_{cc}/2$. External DC blocking capacitors must be used on the IFLO/IFLOBAR signals.

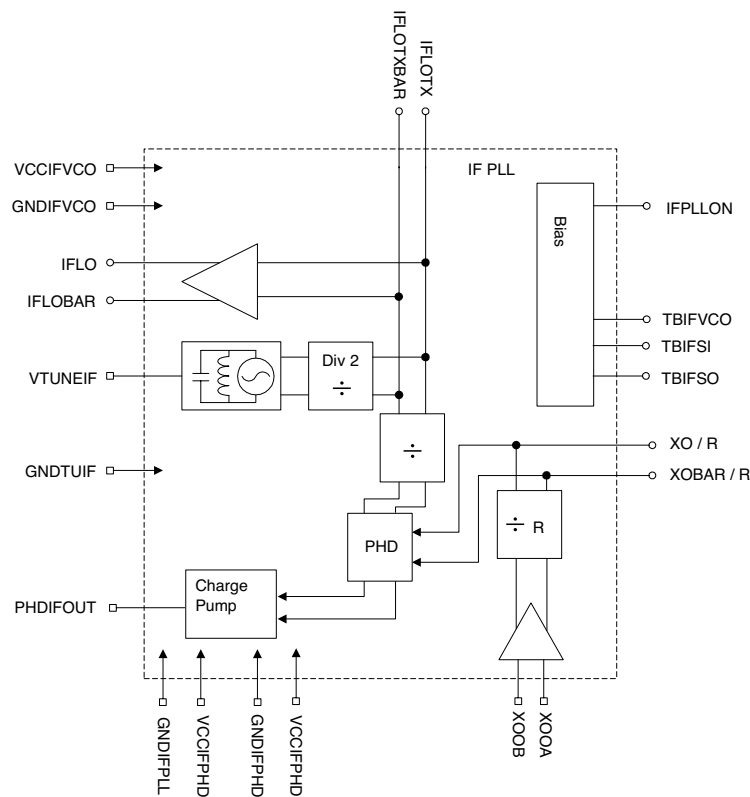
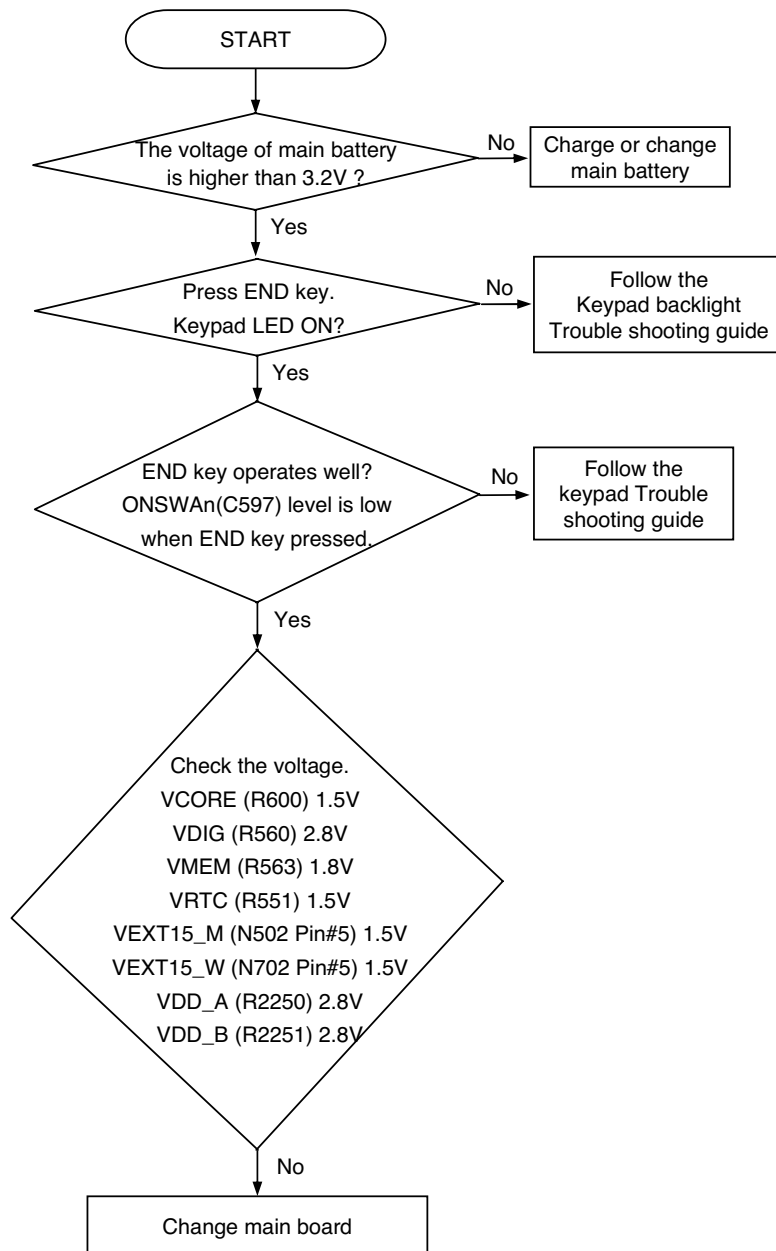


Figure 3-8-7. Block Diagram of Frequency Synthesizer Part (IF PLL)

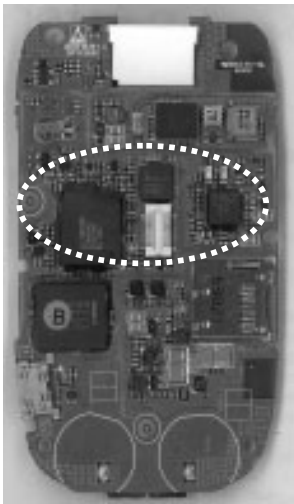
4. TROUBLE SHOOTING

4. TROUBLE SHOOTING

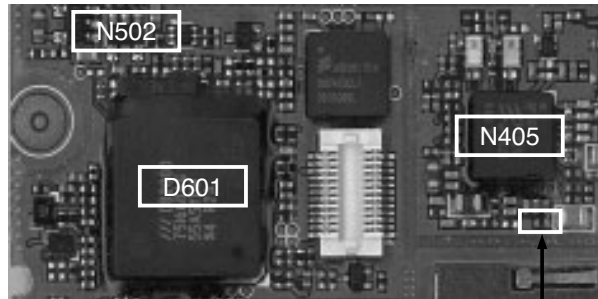
4.1 Power ON Trouble



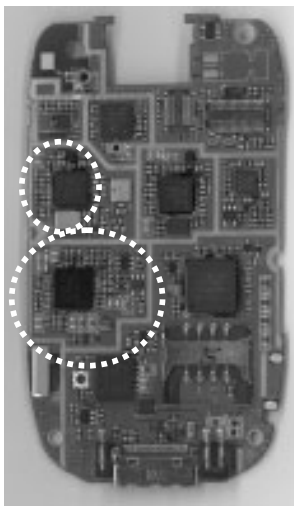
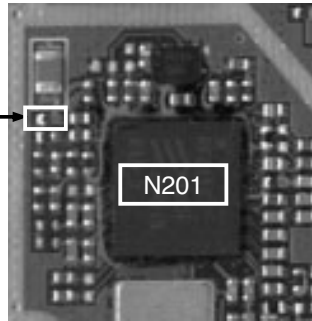
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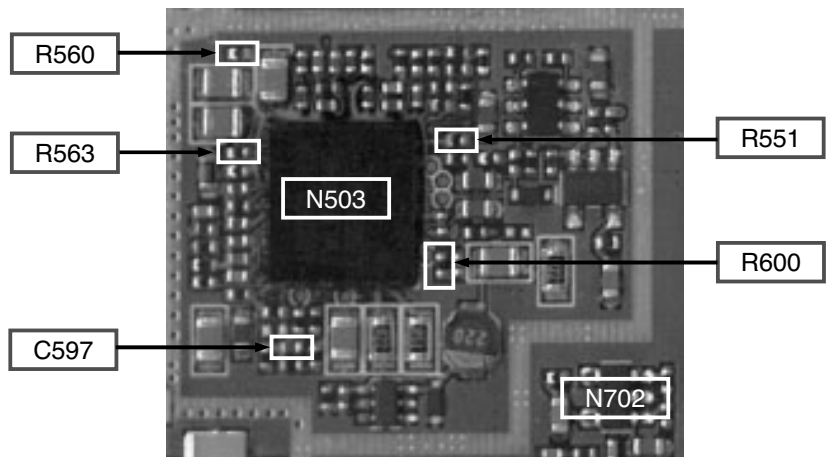
<Top view>



R2250

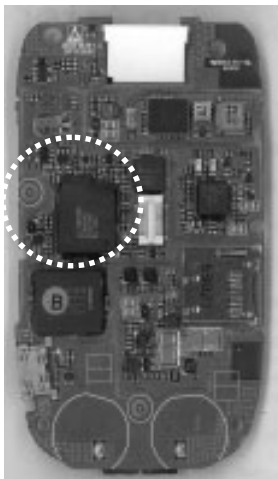
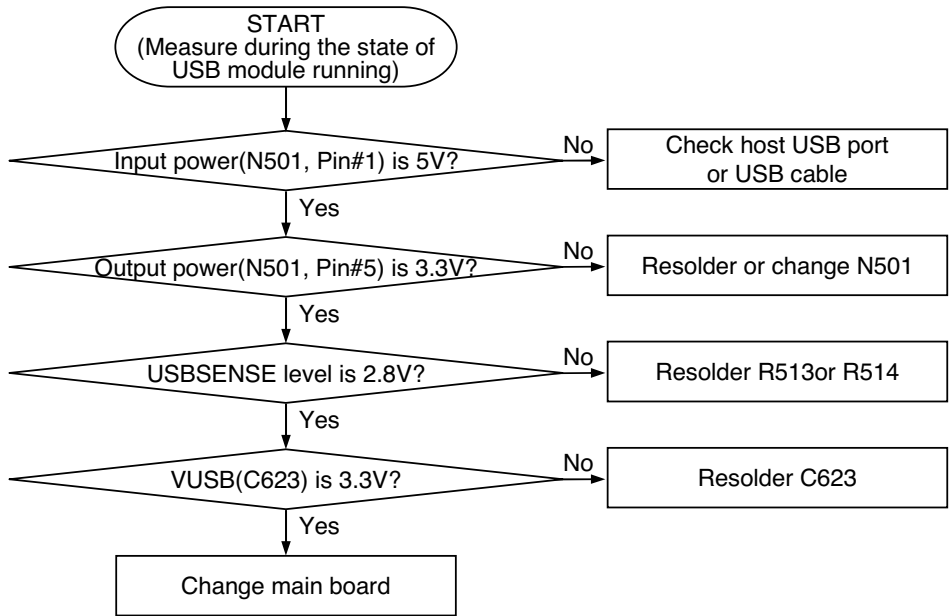


<Bottom view>

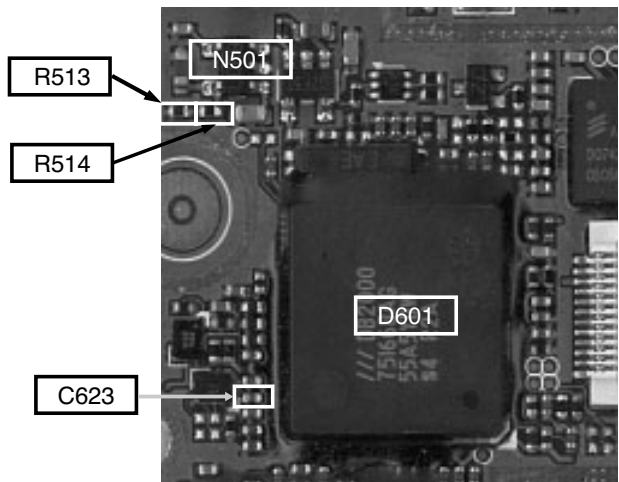


4. TROUBLE SHOOTING

4.2 USB Trouble



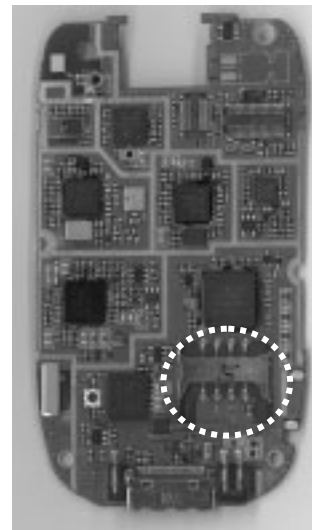
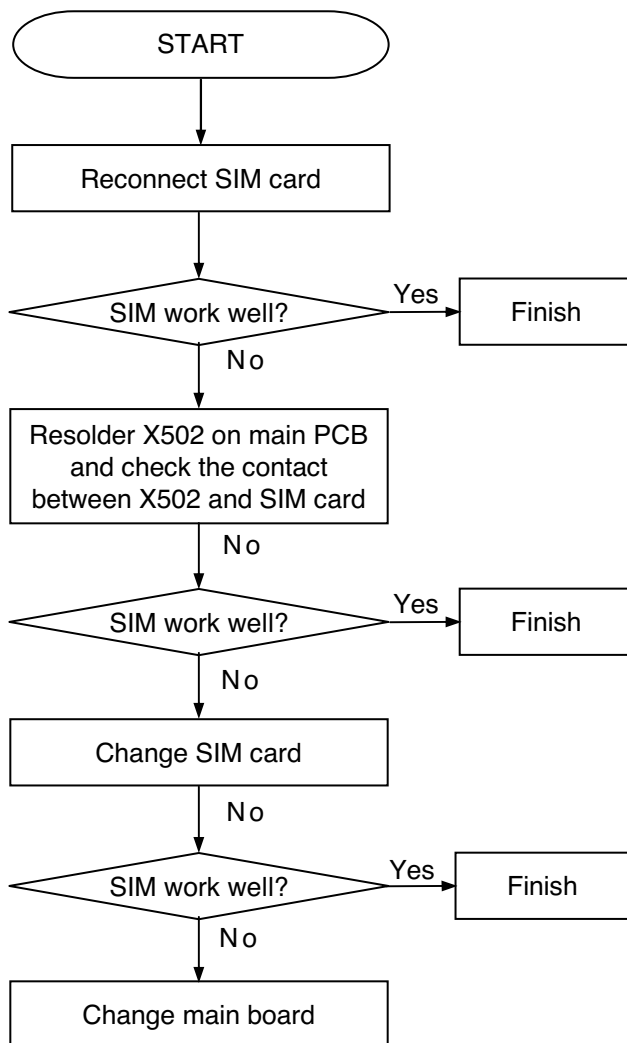
<Top view>



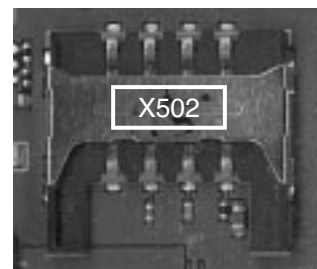
4.3 SIM Detect Trouble

- **SIM control path**

- MARITA generates SIM interface signals(2.75V level) to VINCENNE.
- Vincenne converts SIM interface signals to 3V/5V.

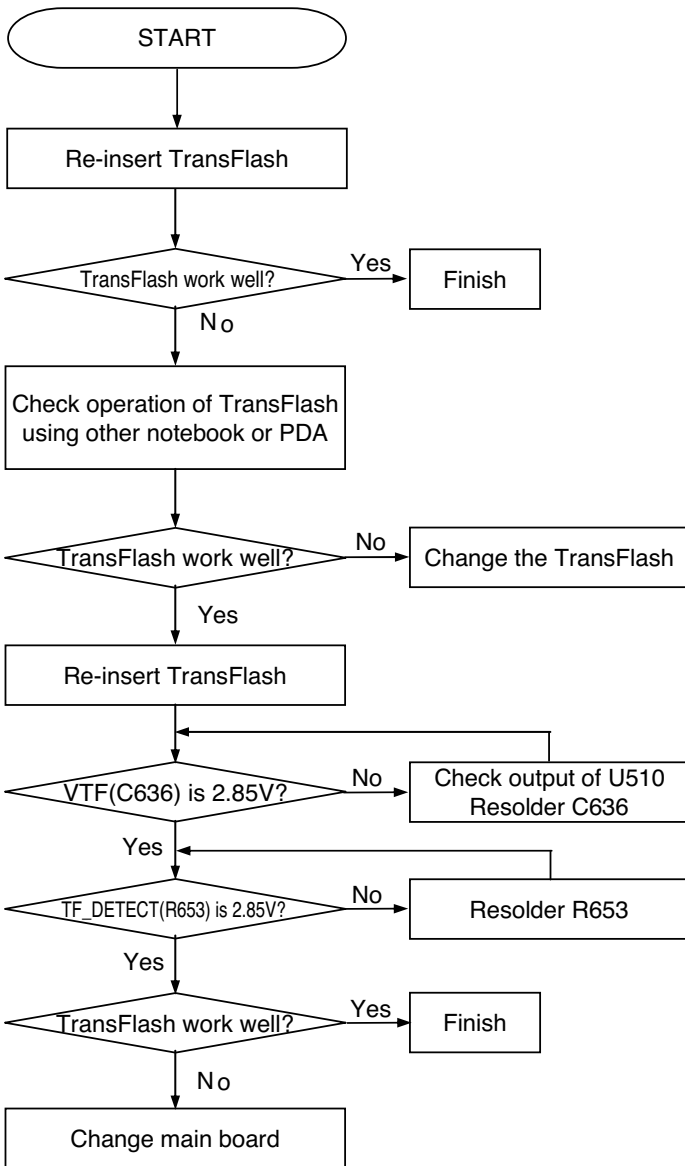


<Bottom view>

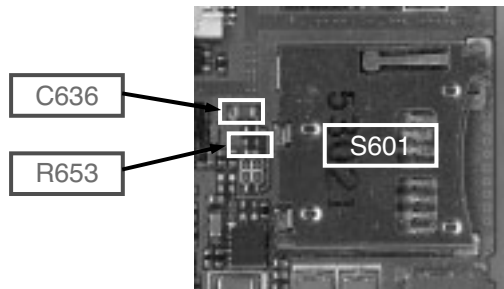


4. TROUBLE SHOOTING

4.4 TransFlash Trouble

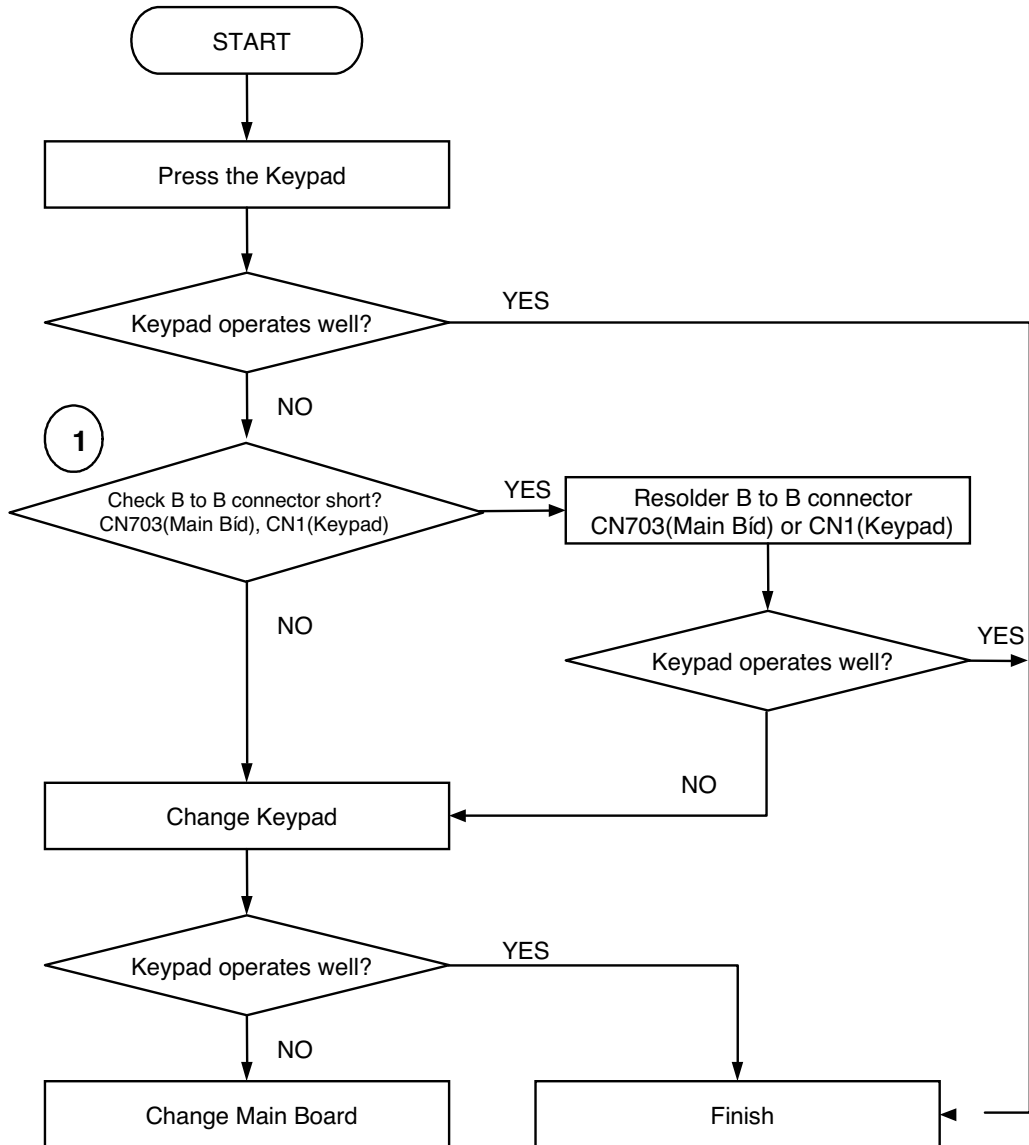


<Top view>



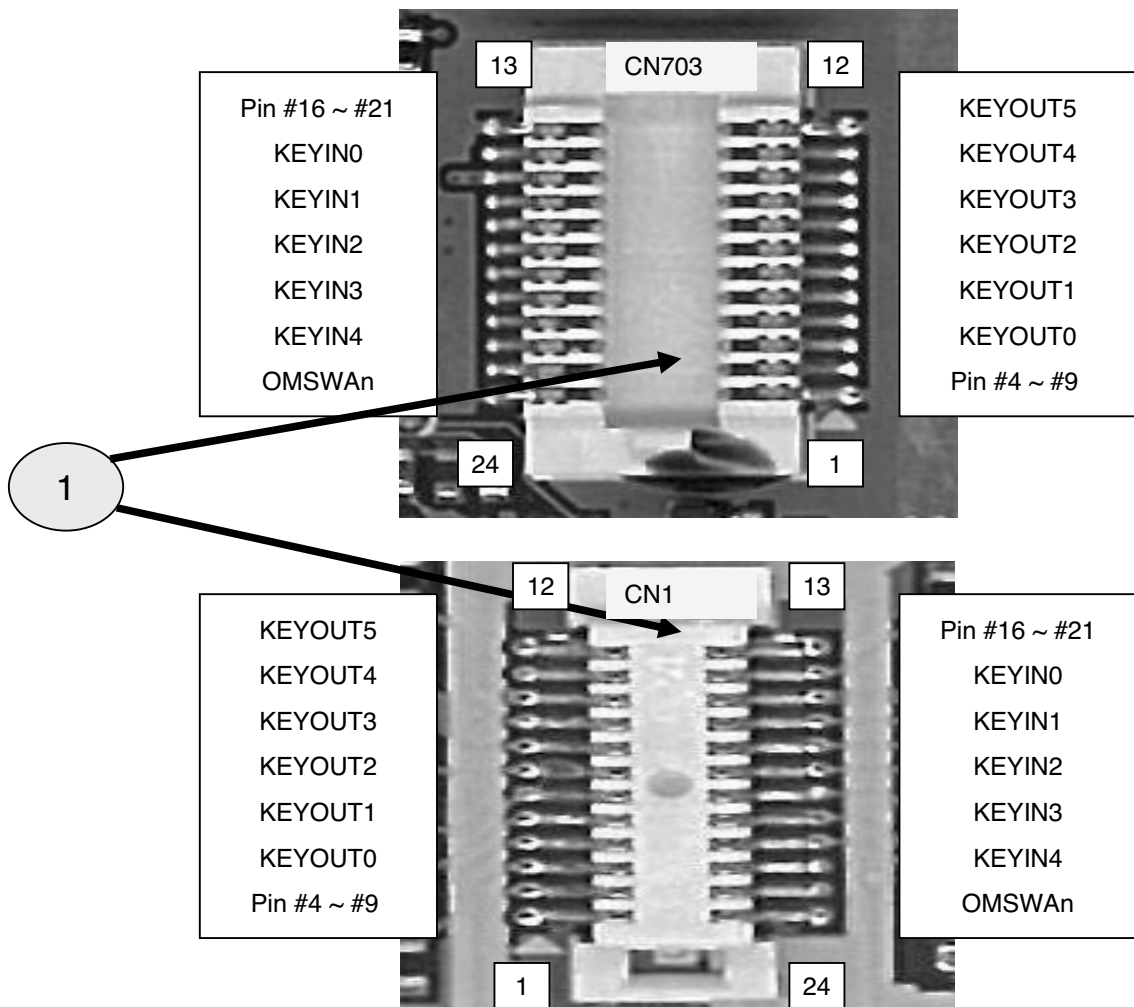
4-5 Keypad Trouble

Keypad signals to MARITA and VINCENNE through board-to-board connector.



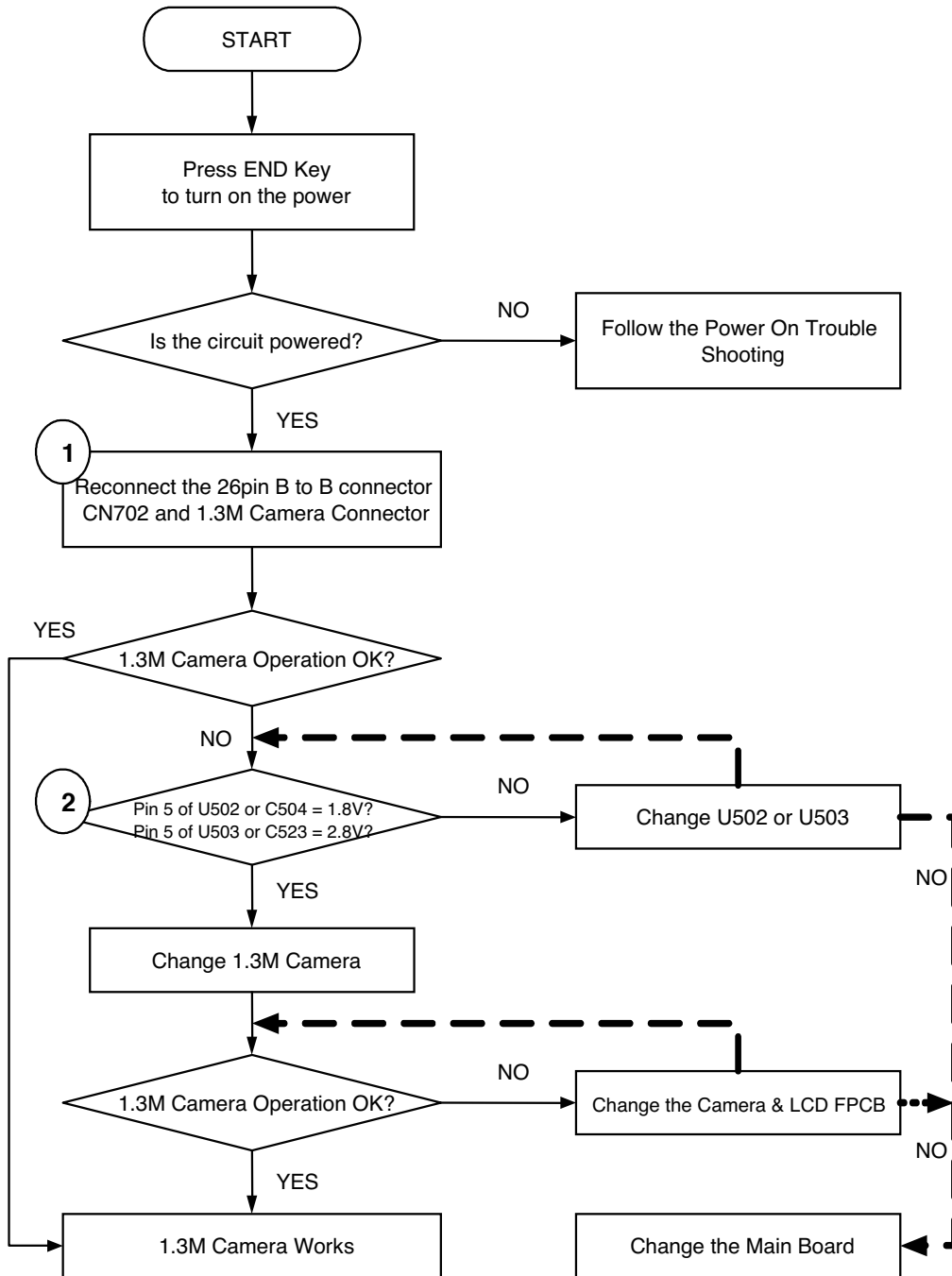
4. TROUBLE SHOOTING

Keypad signals to MARITA and VINCENNE through board-to-board connector.

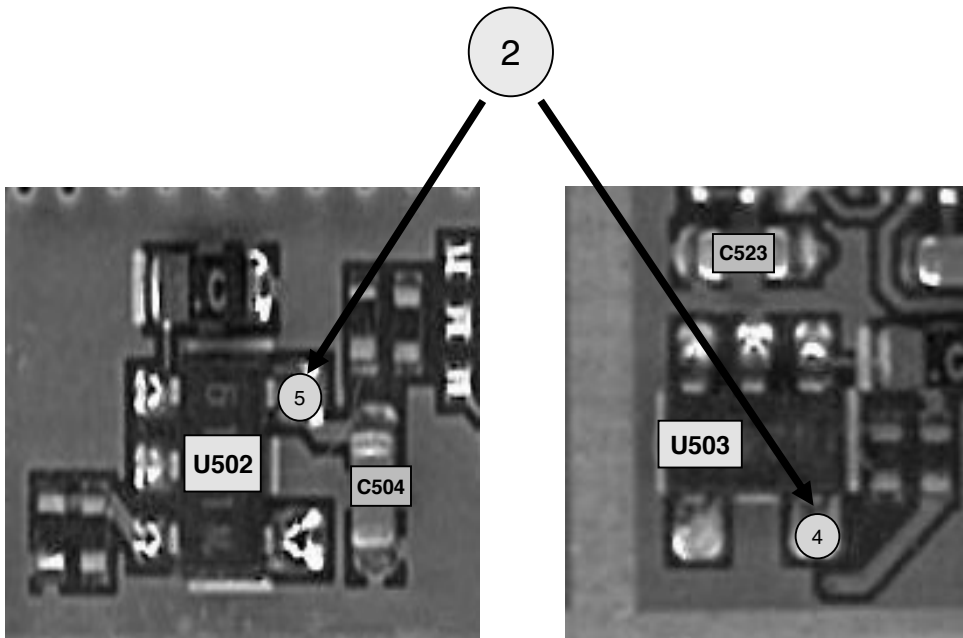
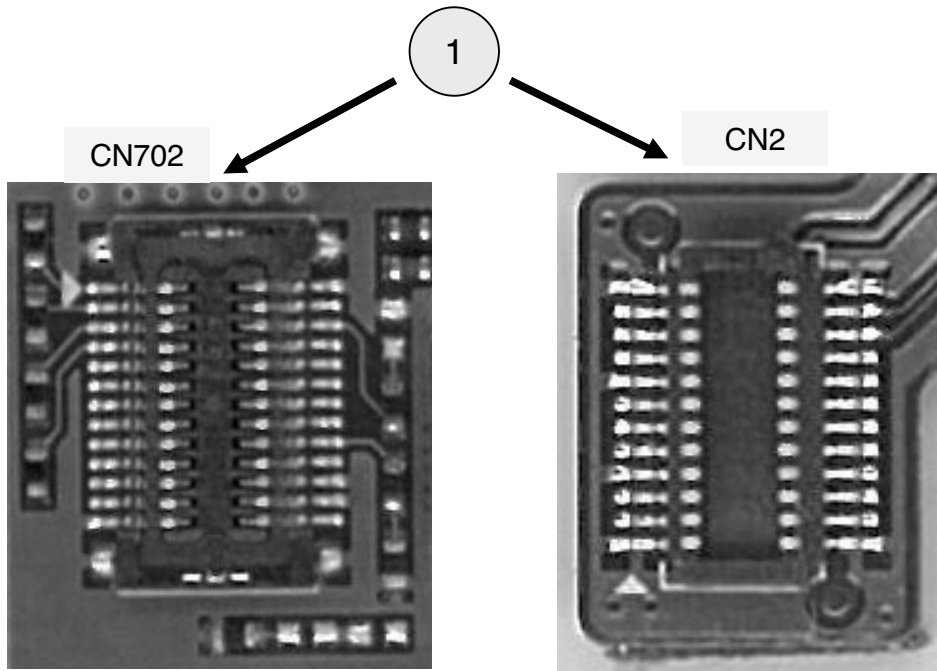


4-6 1.3M Camera Trouble

Camera control signals are generated by Marita

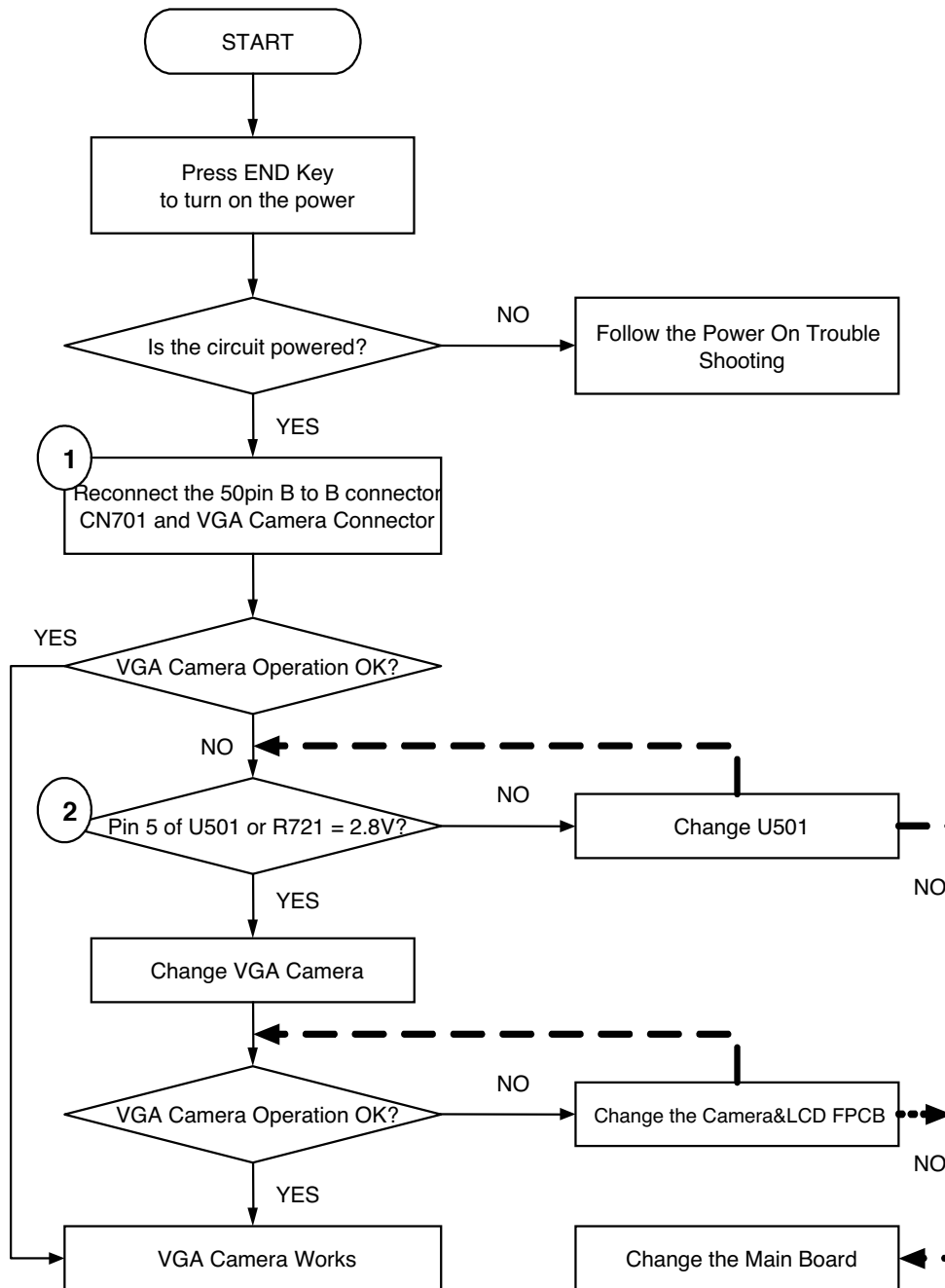


4. TROUBLE SHOOTING

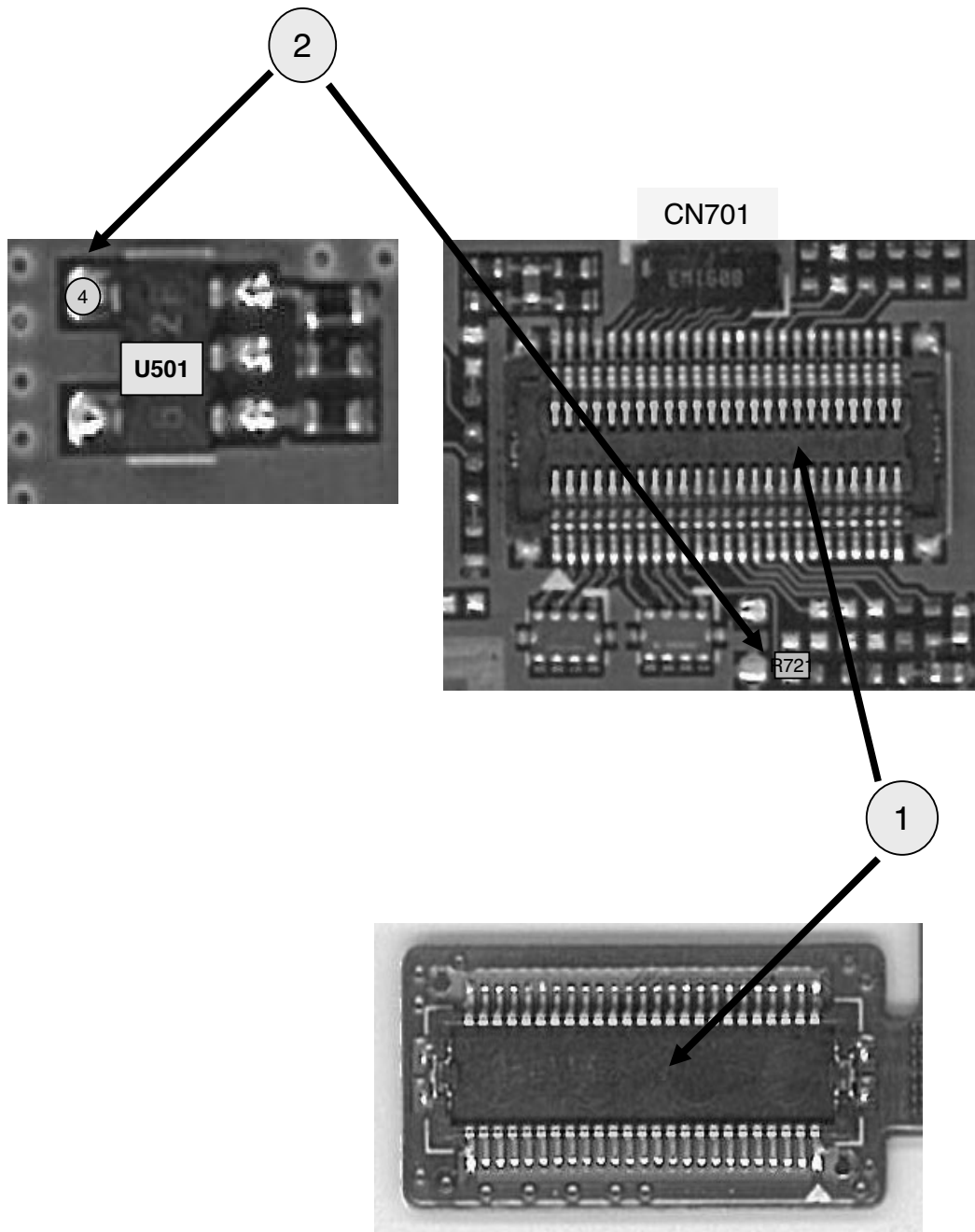


4-7 VGA Camera Trouble

Camera control signals are generated by Marita

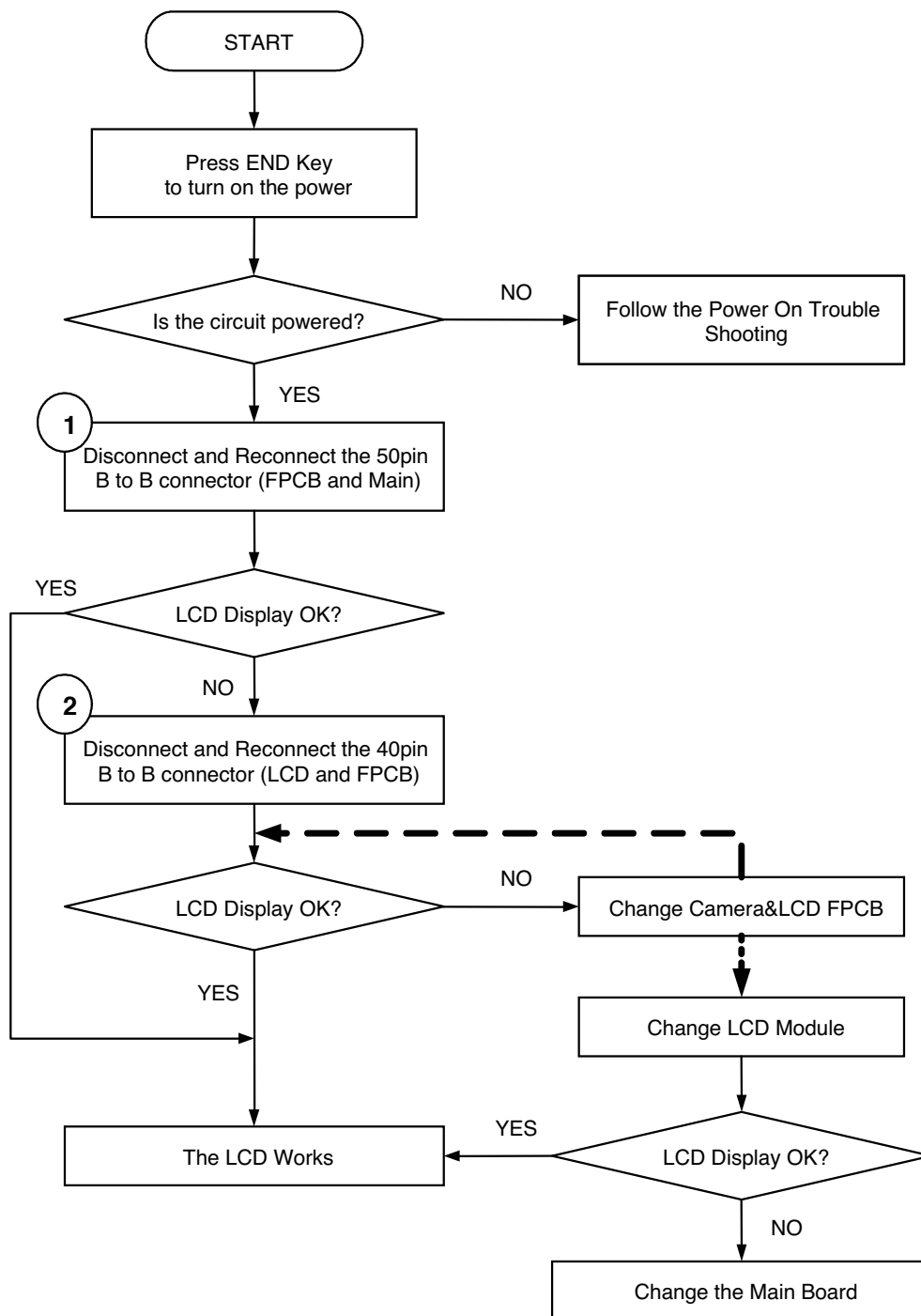


4. TROUBLE SHOOTING

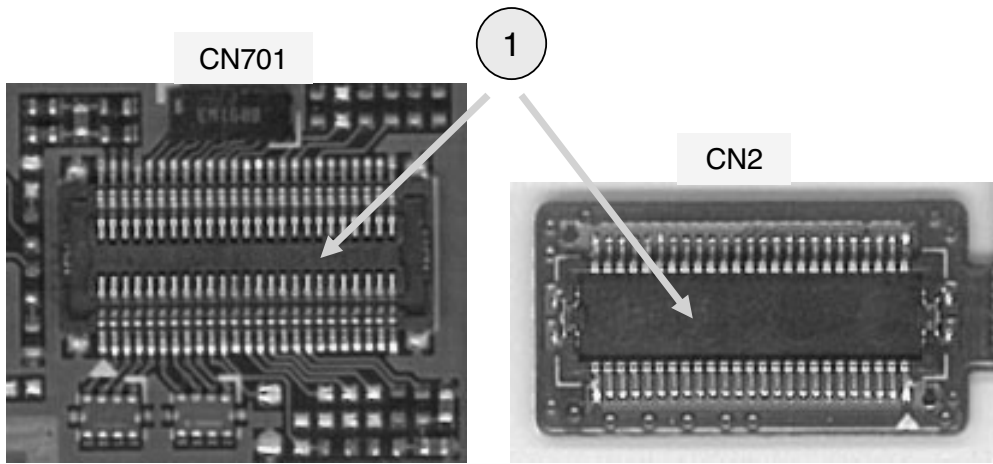


4-8 Main LCD Trouble

LCD control signals are generated by Marita

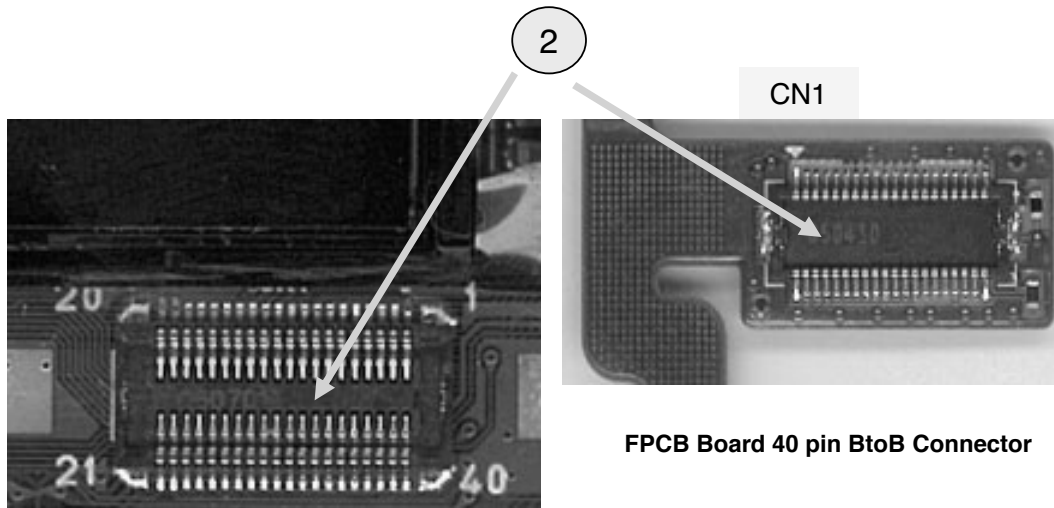


4. TROUBLE SHOOTING



Main Board 50 pin B to B Connector

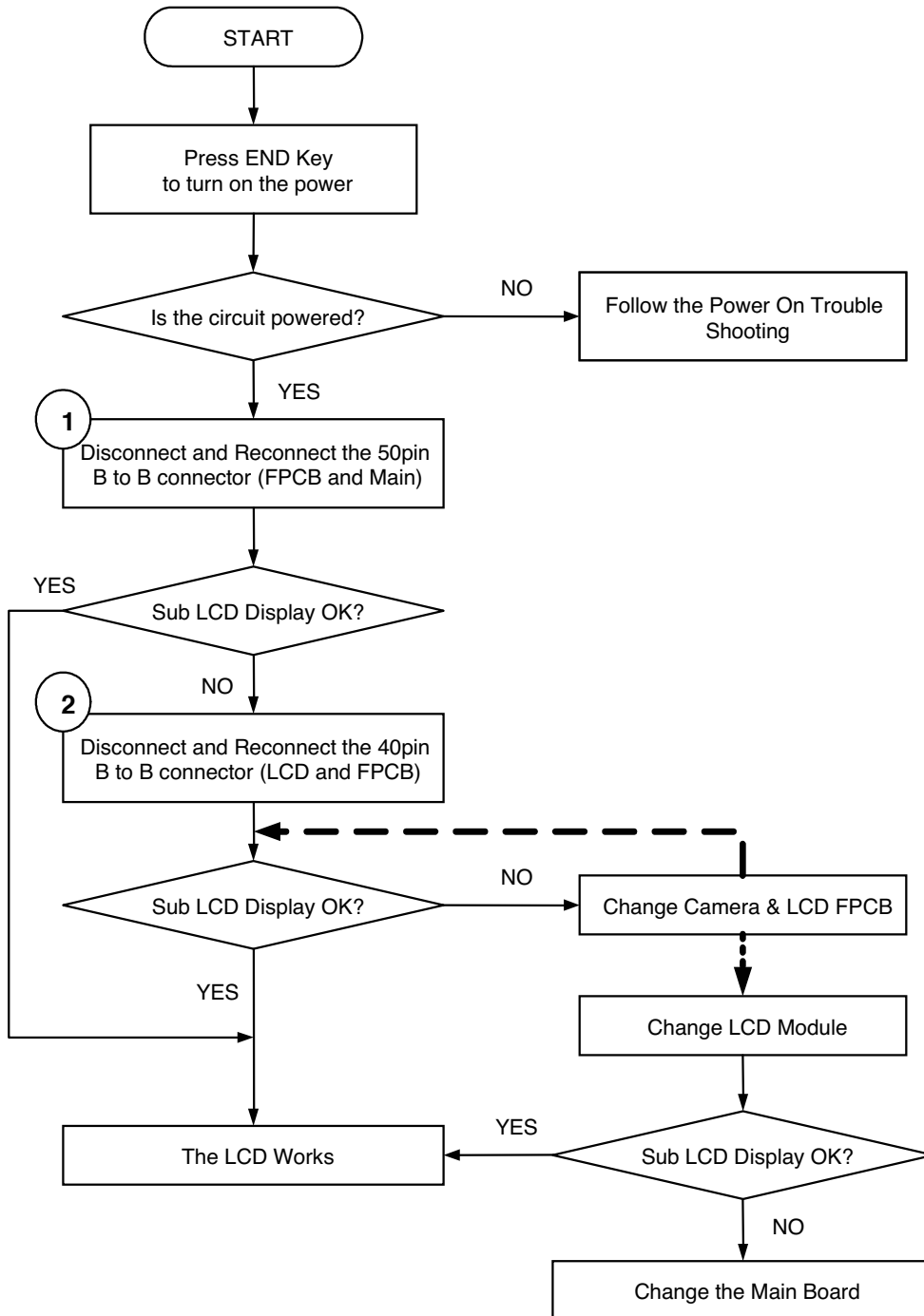
FPCB Board 50 pin B to B Connector



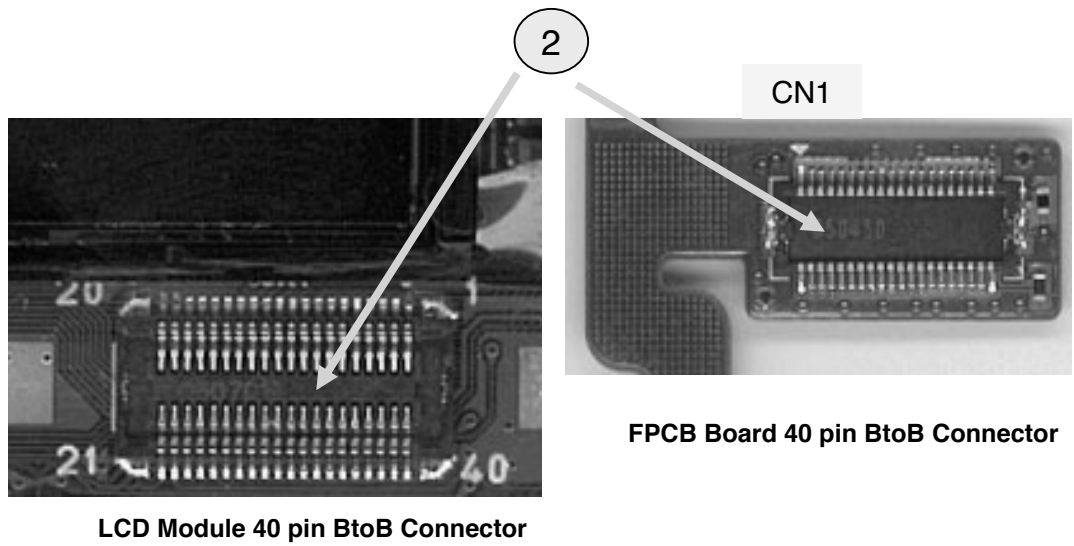
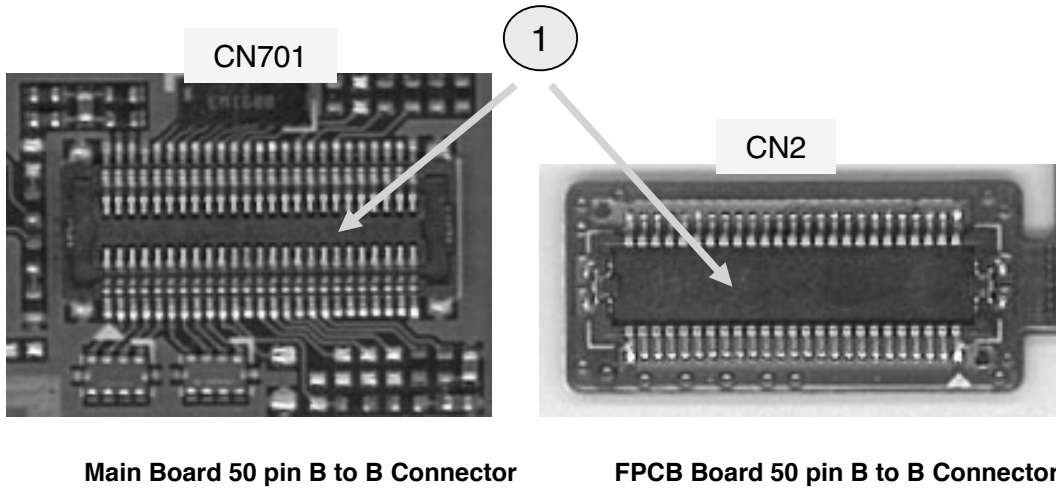
LCD Module 40 pin BtoB Connector

FPCB Board 40 pin BtoB Connector

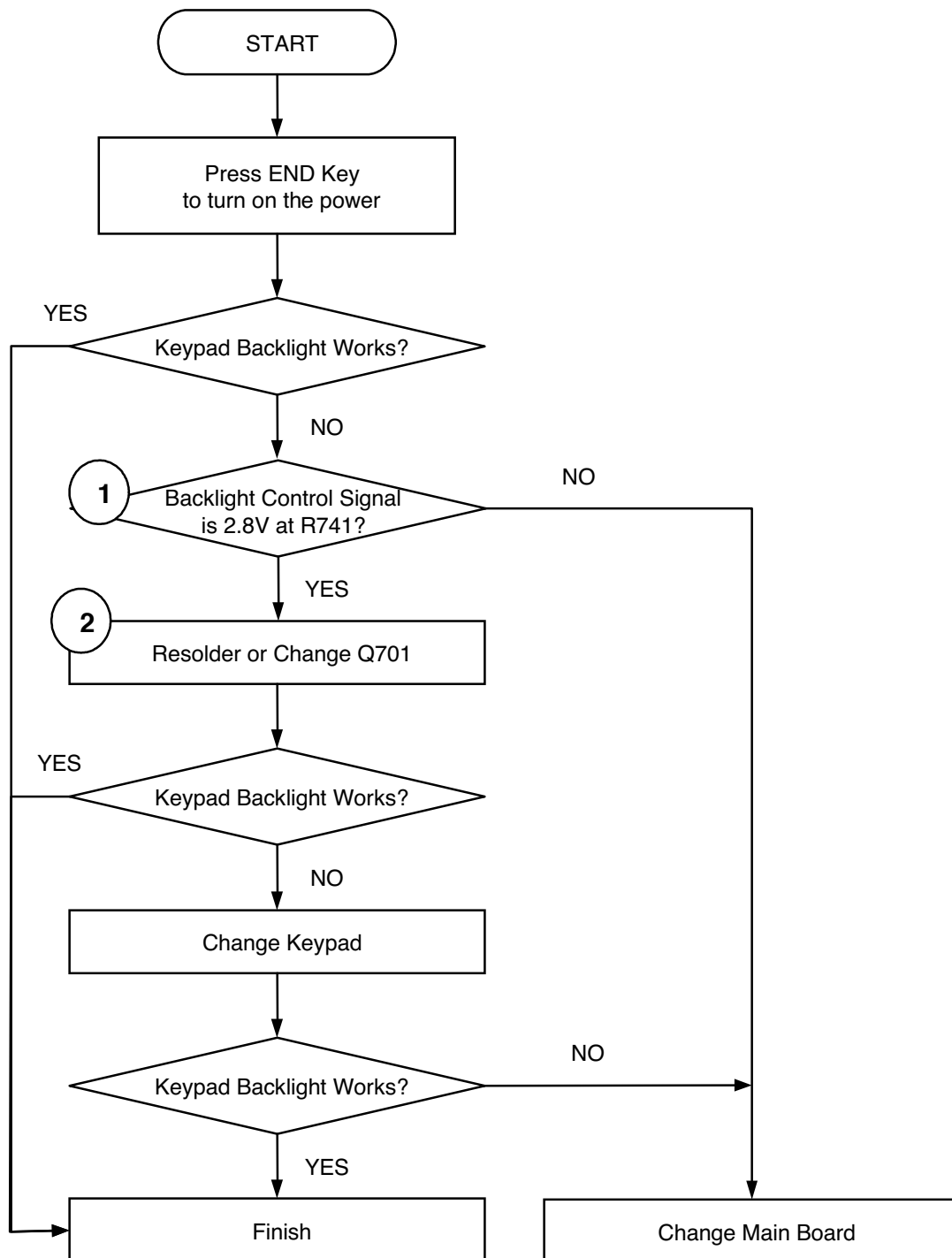
4-9 Sub LCD Trouble



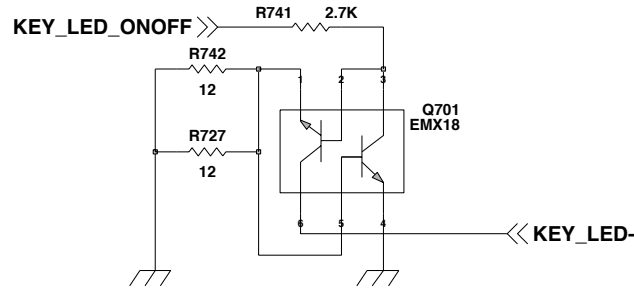
4. TROUBLE SHOOTING



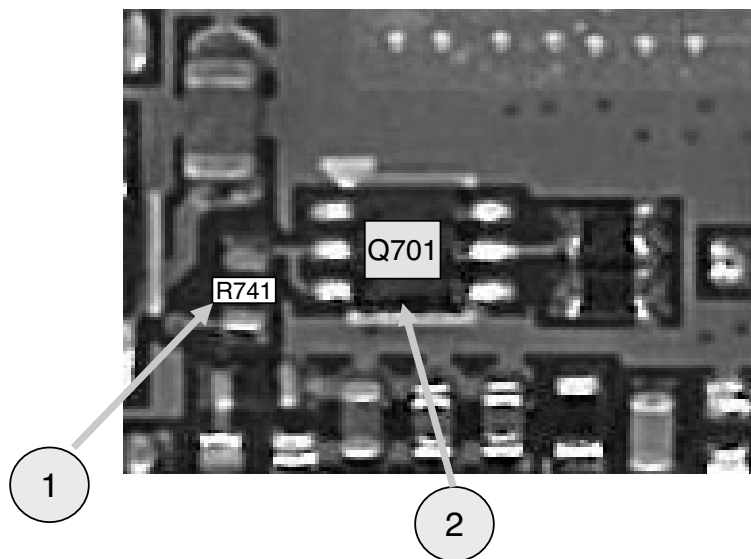
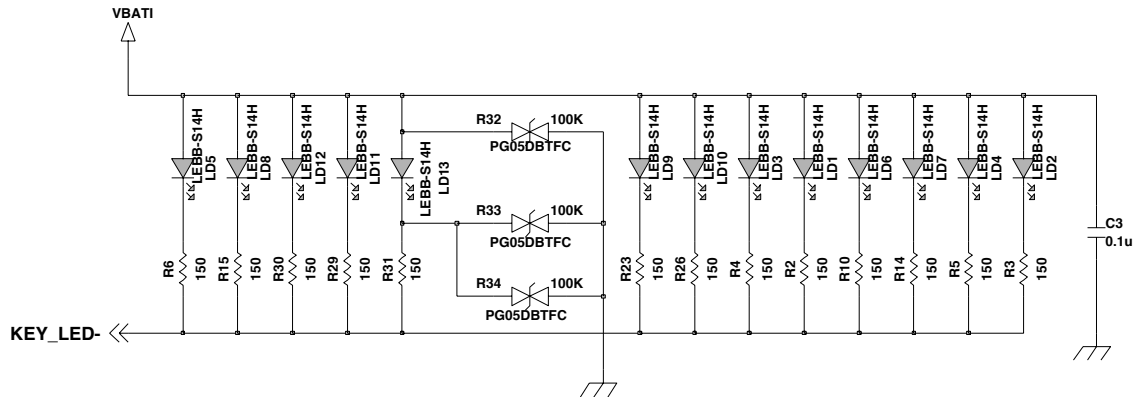
4-10 Keypad Backlight Trouble



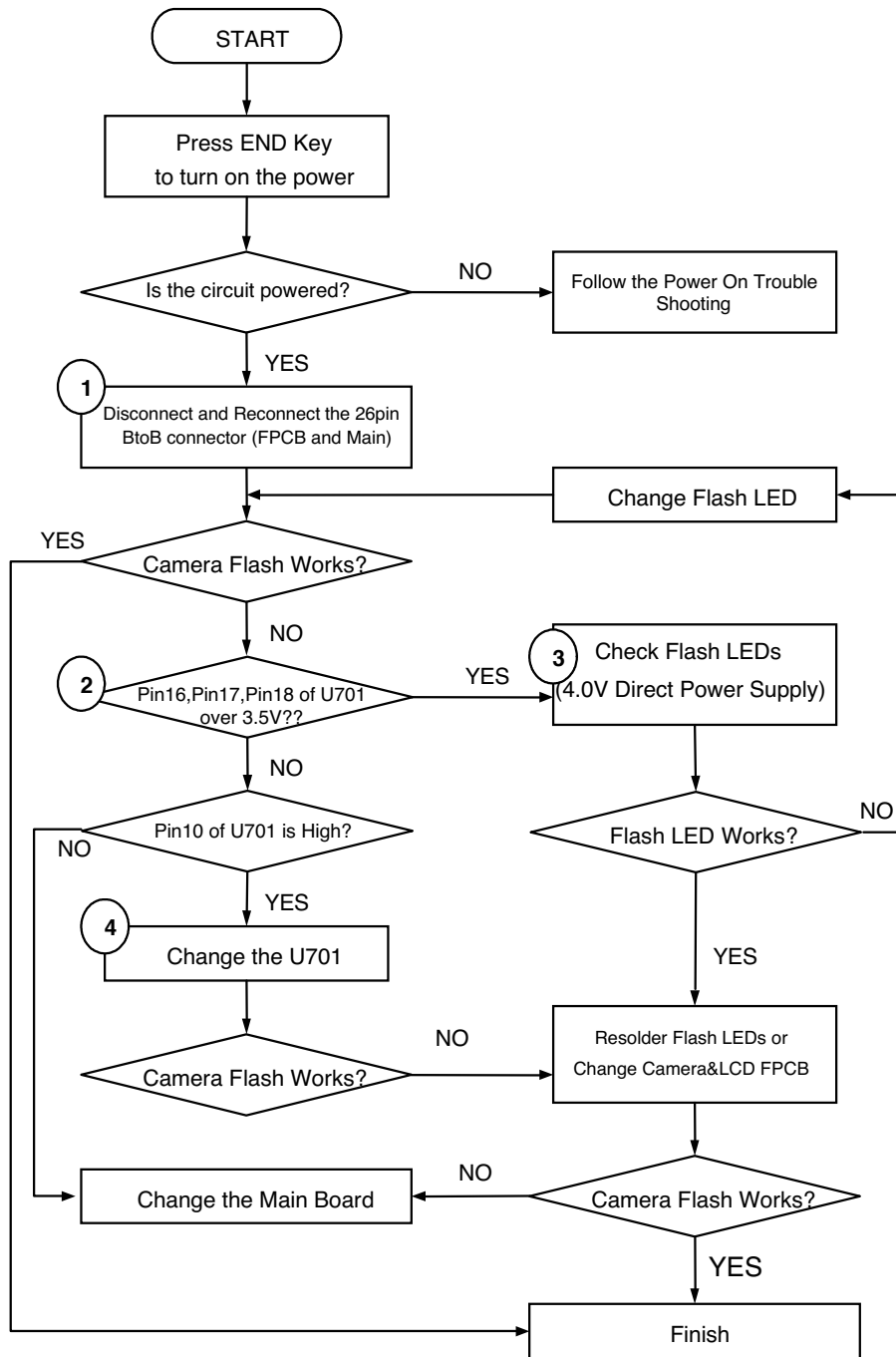
4. TROUBLE SHOOTING



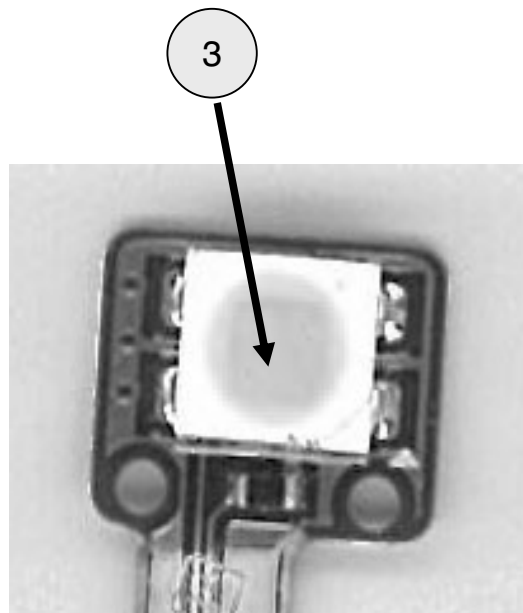
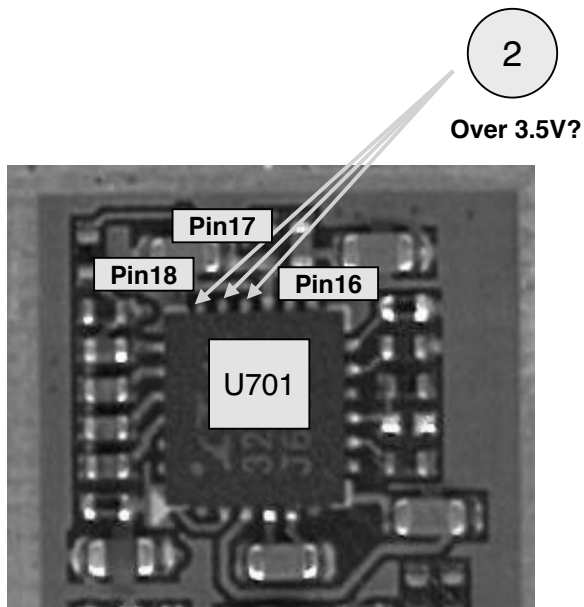
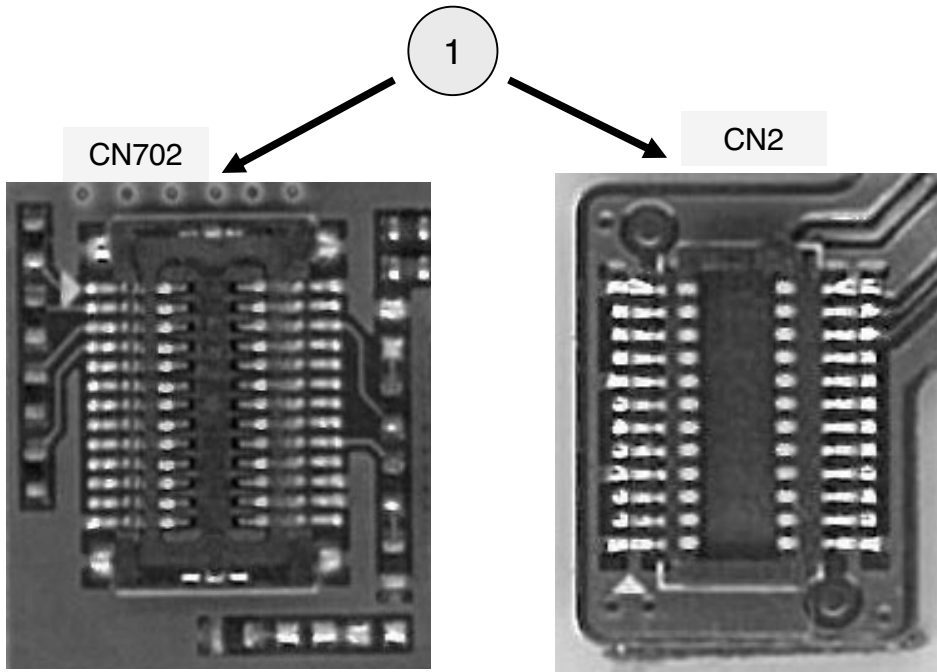
Keypad Backlight Control



4-11 Camera Flash Trouble



4. TROUBLE SHOOTING



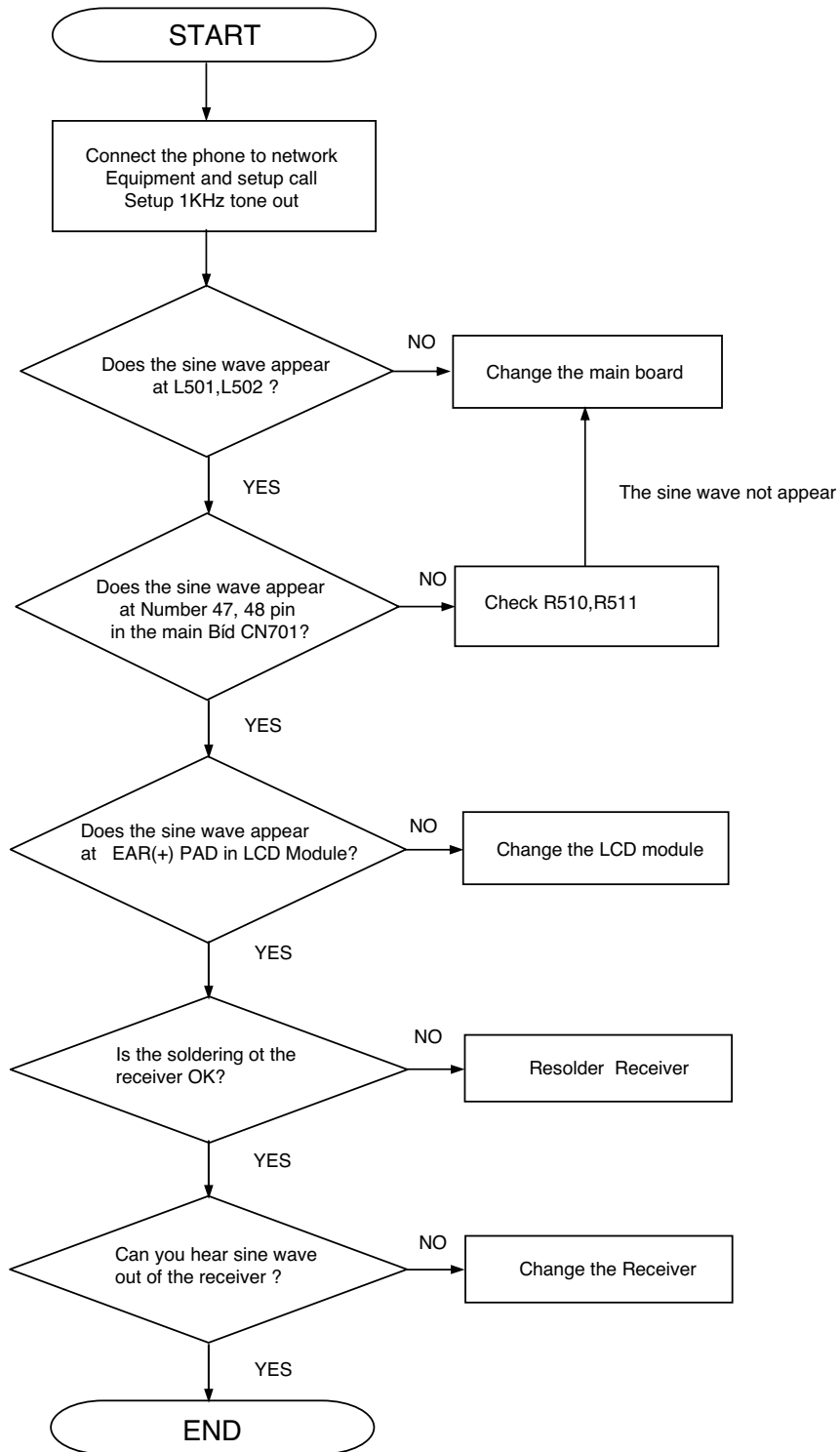
4.12 Audio Trouble

4.12.1 Receiver

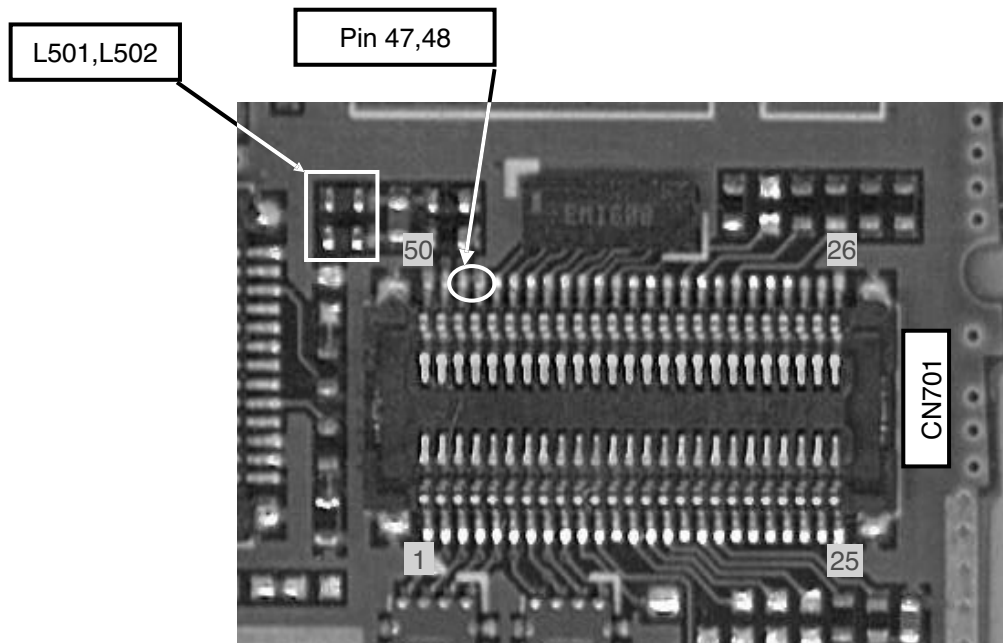
- Signals to the receiver
 - Receiver signals are generated at Vincenne
 - BEARP, BEARM
 - Receiver path :
 - Vincenne (BEARP, BEARM) →
 - CN701 on main board →
 - LCD Module →
 - Receiver

♣ Note : It is recommended that engineer should check the soldering of R, L, C along the corresponding path before every step.

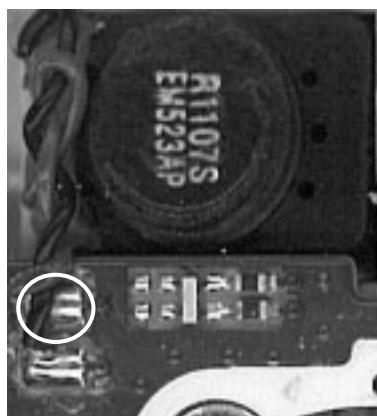
4. TROUBLE SHOOTING



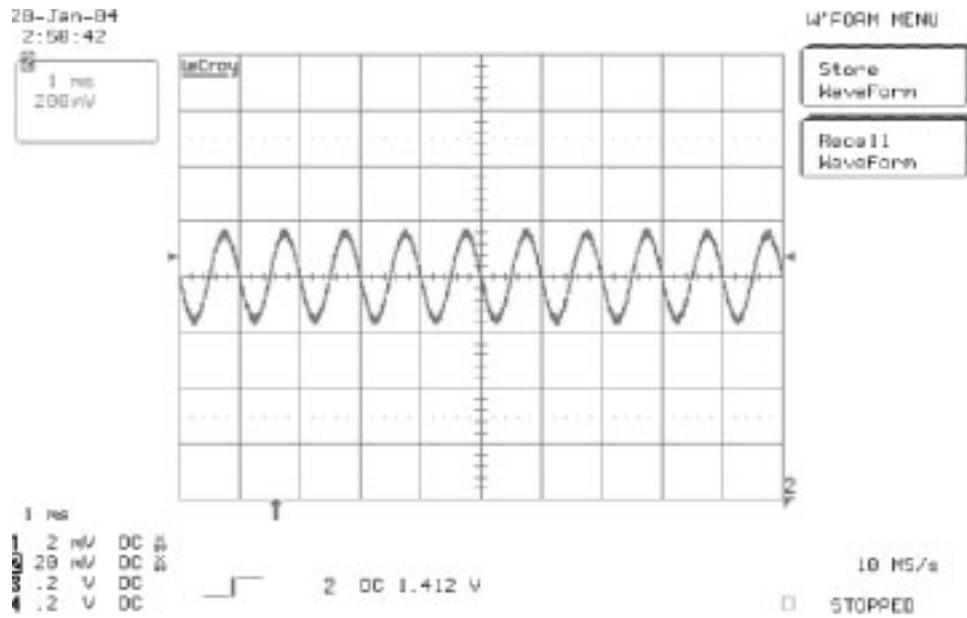
4. TROUBLE SHOOTING



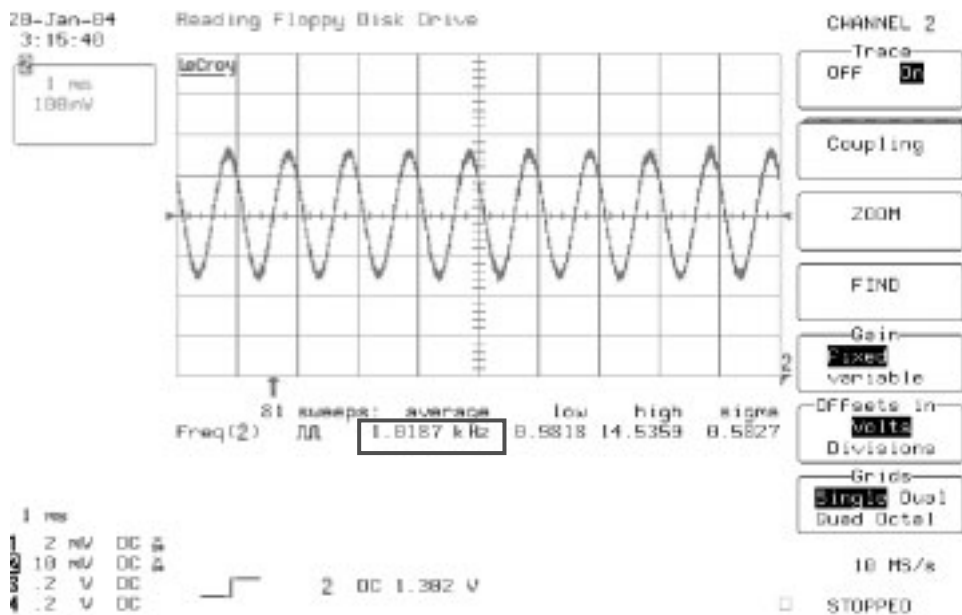
B SIDE



4. TROUBLE SHOOTING



Measured 1kHz Sine Wave Signal



Measured 1kHz Sine Wave Signal

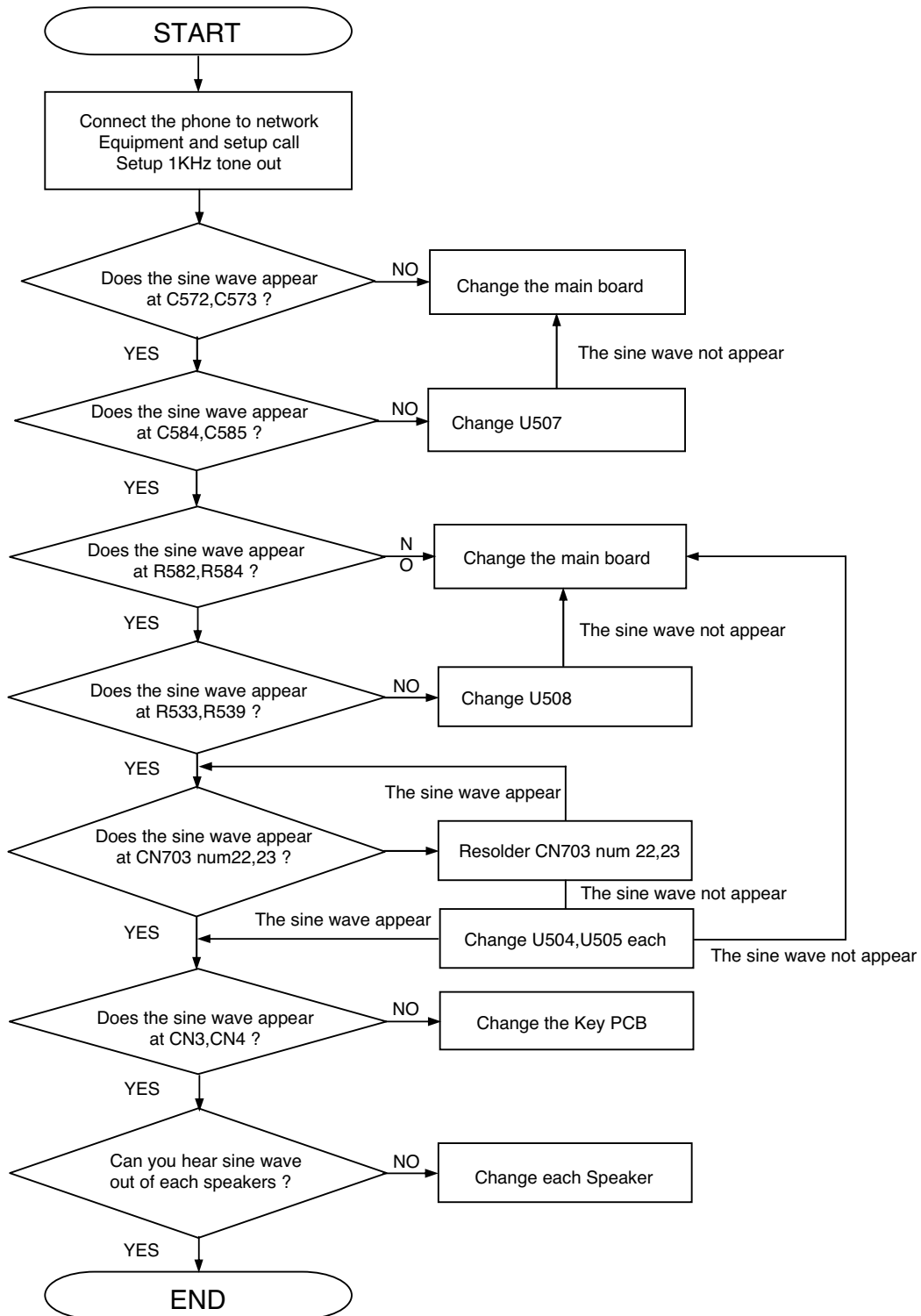
4.12.2 Speaker (Voice Loud Speaker,Midi, MP3,Key Tone)

Signals to the speaker

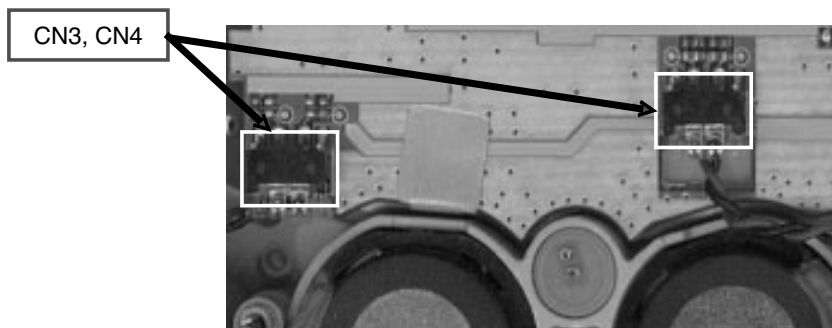
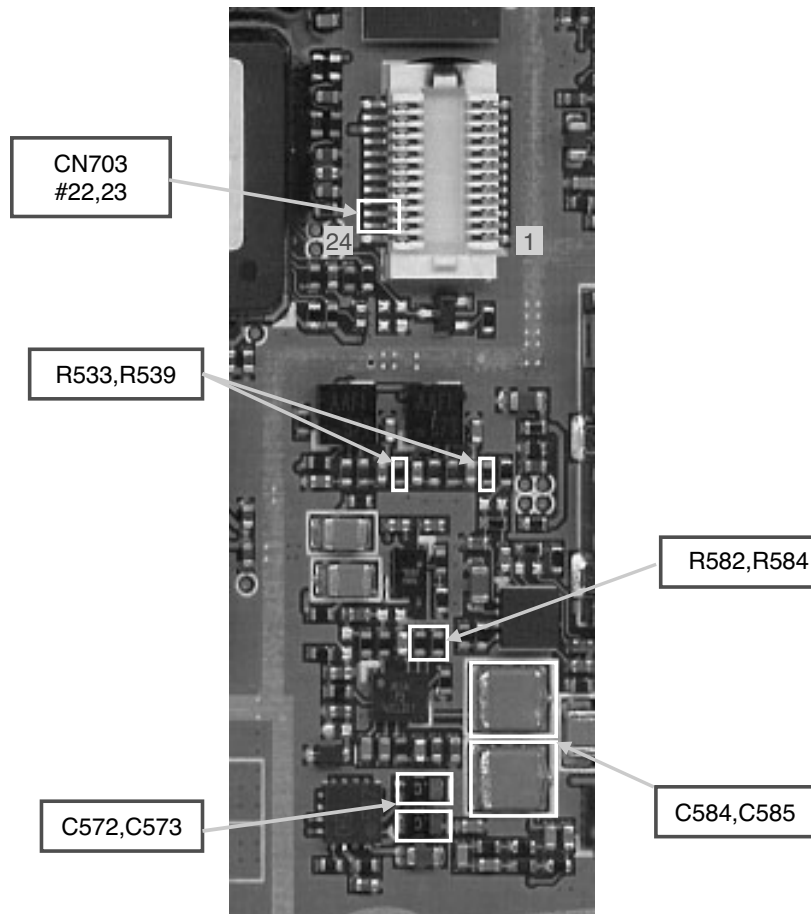
- AUXO1/Right, AUXO2/Left
 - AUXO1/Right, AUXO2/Left
- Speaker path :
 - Vincenne (AUXO1/Right, AUXO2/Left) →
 - U507(Surround Audio Processor) on the main board →
 - C584,C585 on the main board →
 - N504(ADG) on the main board →
 - U508(Analog Switch) on the main board →
 - U504,U505(Speaker Amp) on the main board →
 - CN703 on the main board →
 - CN3, CN4 on the Key PCB →
 - Speaker

♣ Note : It is recommended that engineer should check the soldering of R, L, C along the corresponding path before every step.

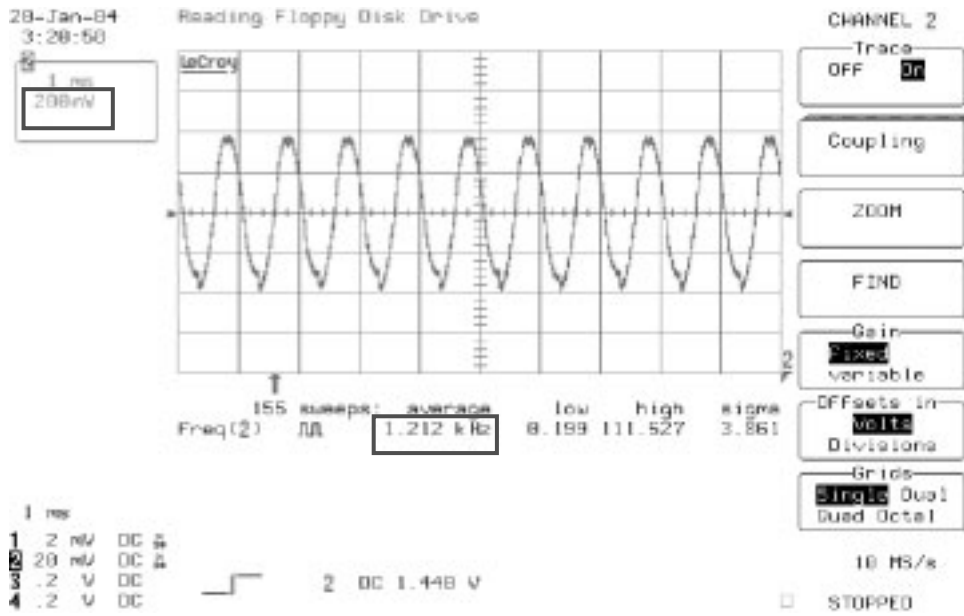
4. TROUBLE SHOOTING



4. TROUBLE SHOOTING



4. TROUBLE SHOOTING



Measured 1kHz Sine Wave Signal

4.12.3 Microphone (Voice call, Voice Recorder, Video Recorder)

- **Microphone Signal Flow**

- MIC is enable by MIC Bias
- MICBAS, MICIP, MICIN signals to ABB (Vincenne)

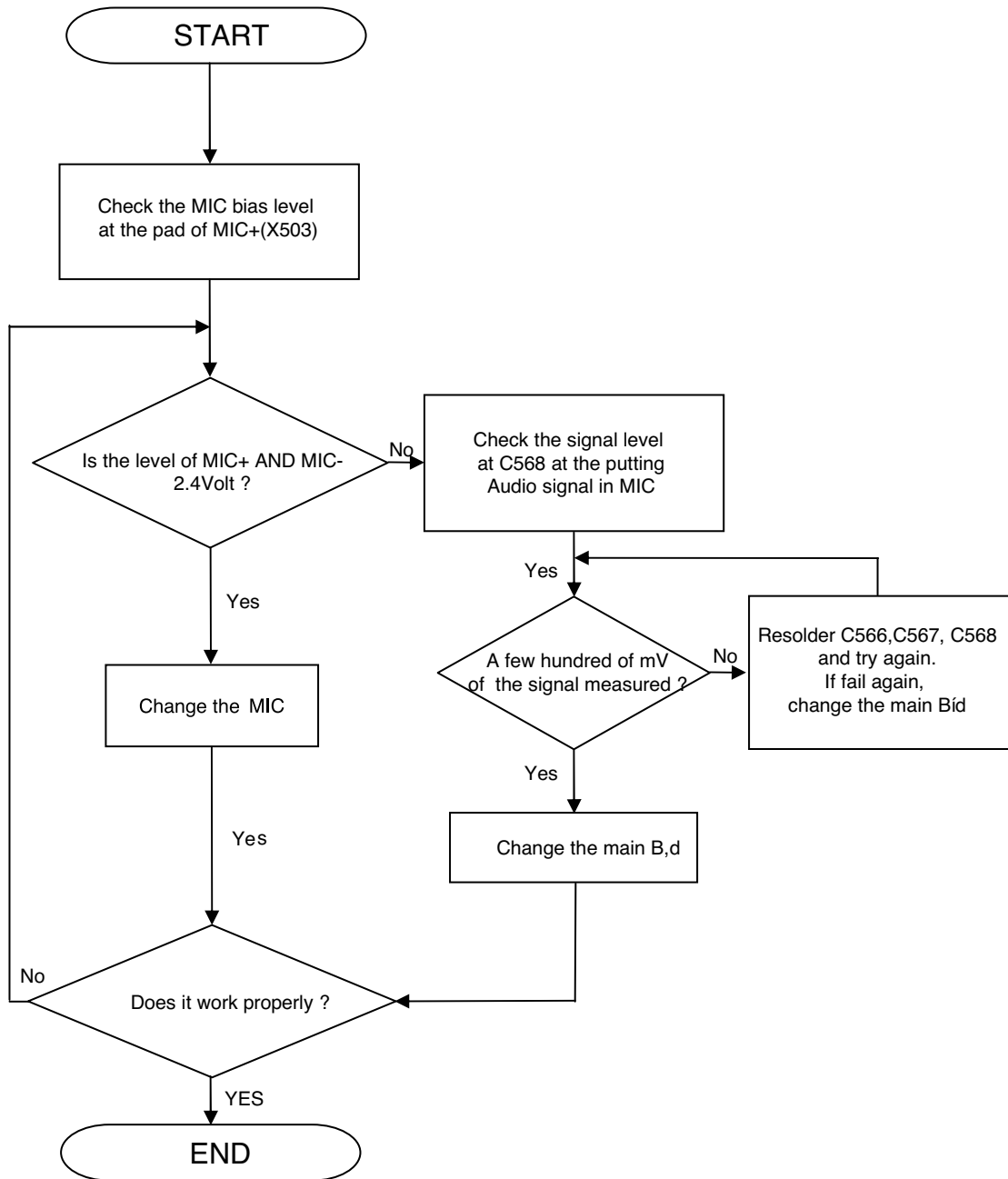
- **Check Points**

- Microphone bias
- Audio signal level of the microphone
- Soldering of components

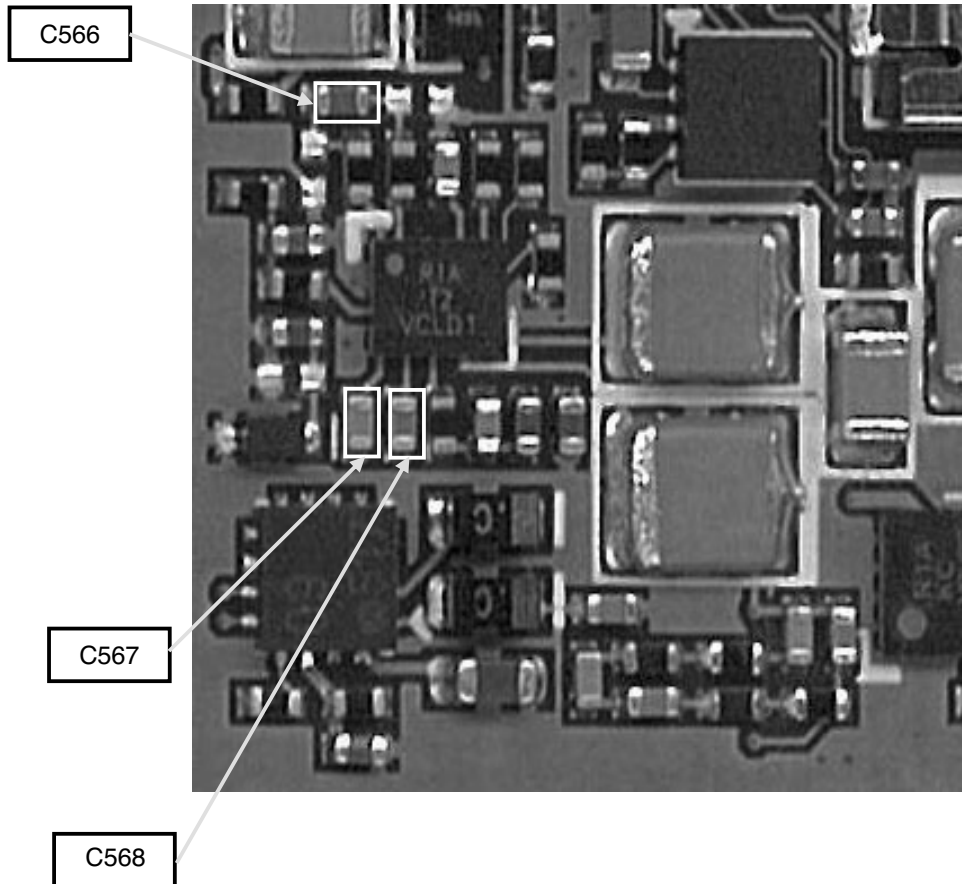
- **Signal from the MIC :**

- MIC →
- N504(TJATTE2) on main board →
- C567,C568 on main board →
- Vincenne

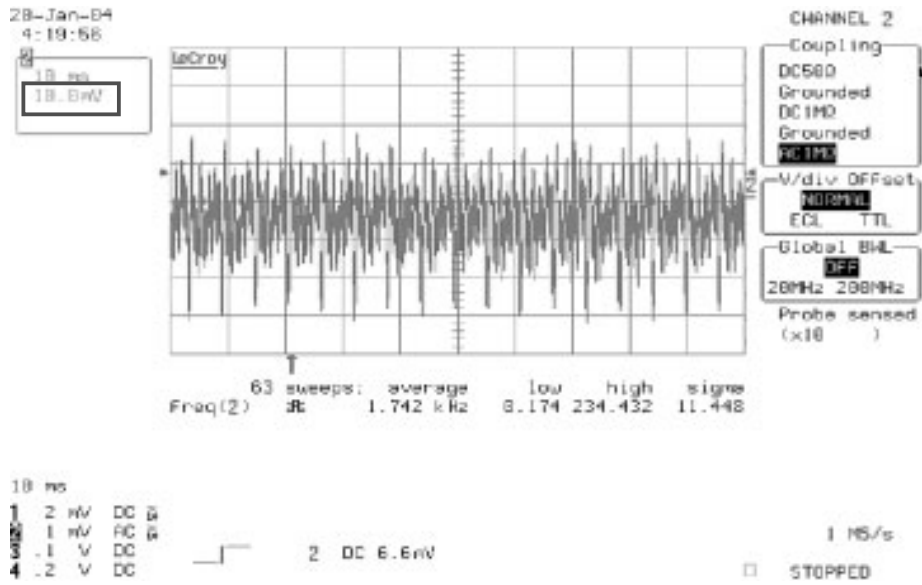
4. TROUBLE SHOOTING



4. TROUBLE SHOOTING

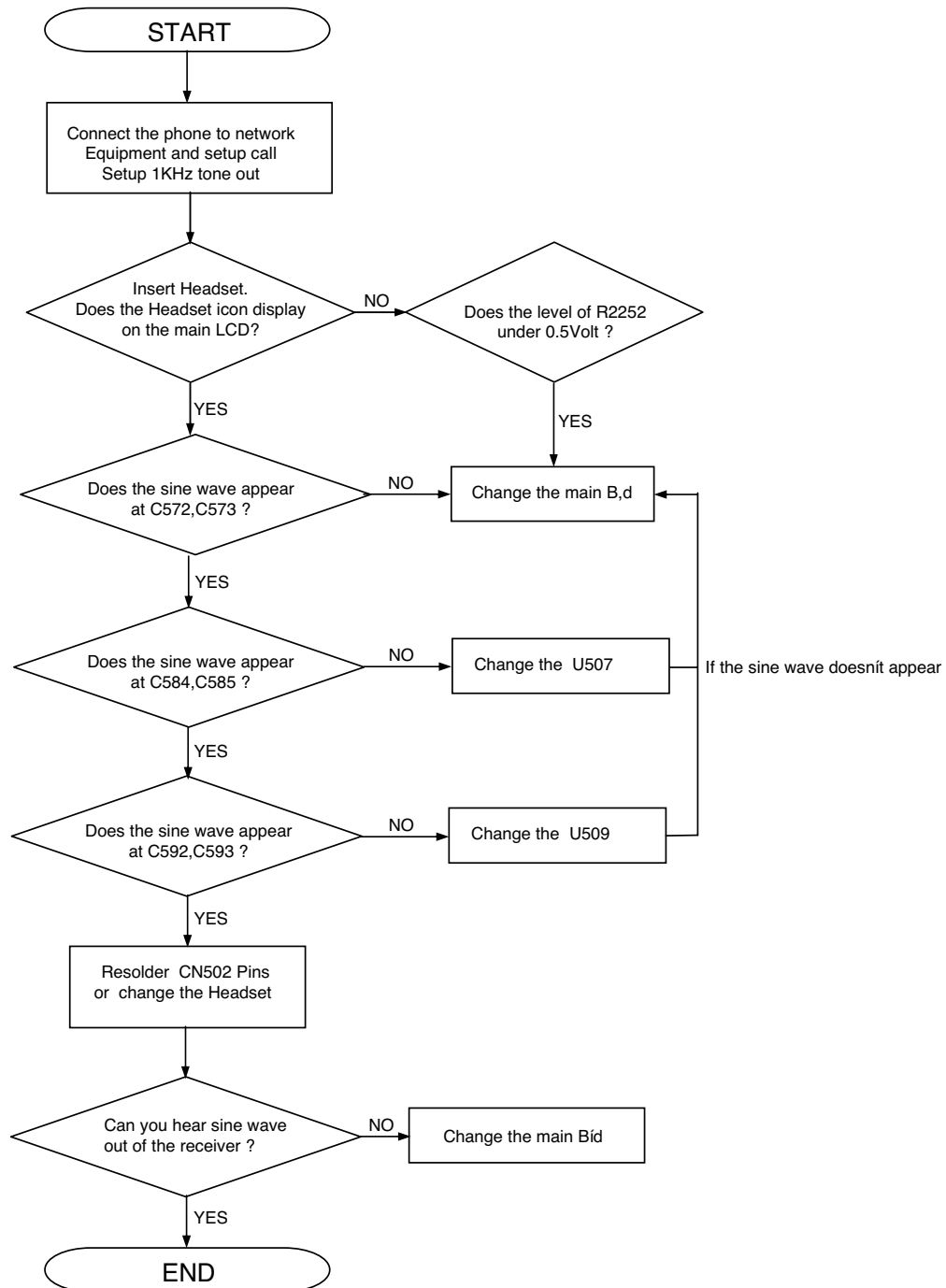


4. TROUBLE SHOOTING



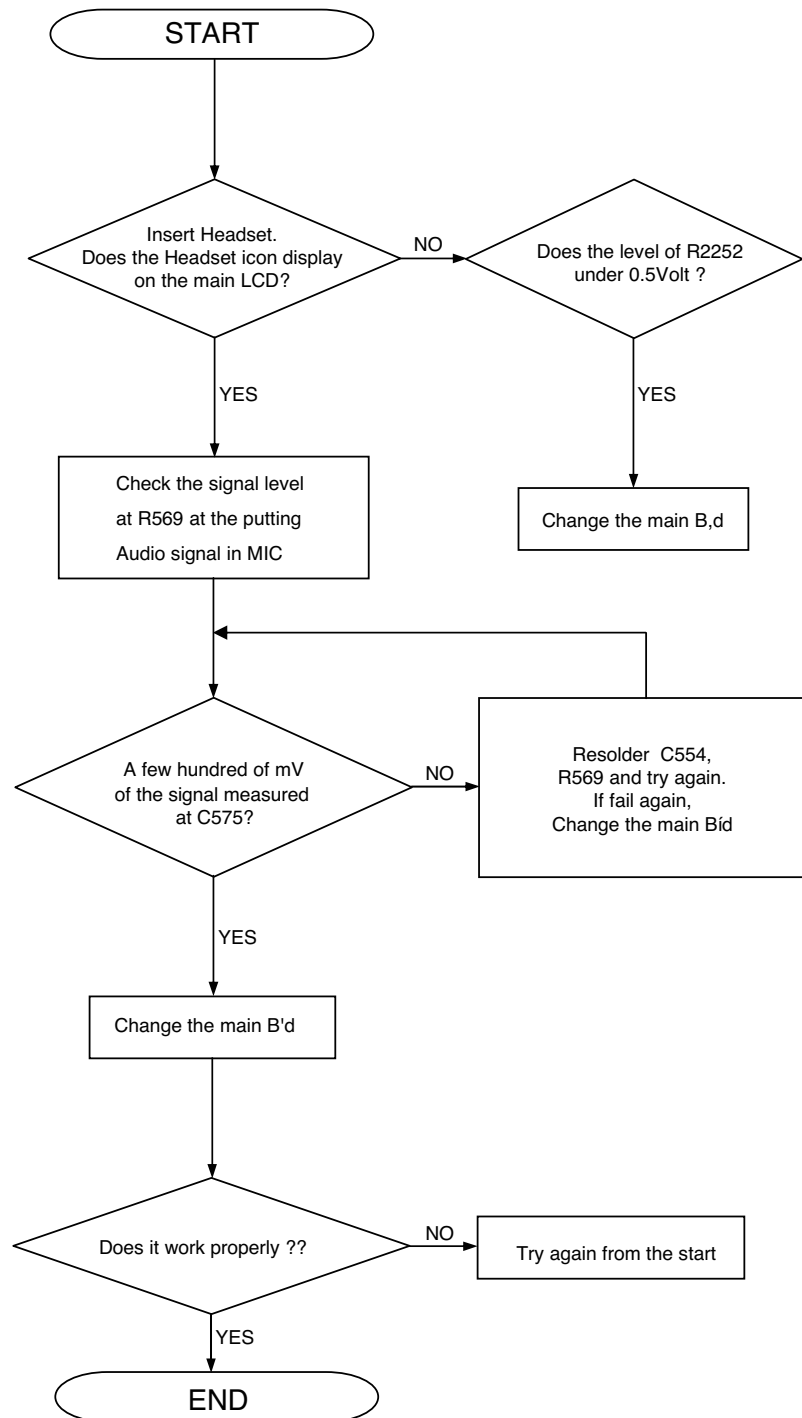
Measured Some Noise Signal

4.12.4 Headset - Receiver(Voice call, Video Telephony,MP3)

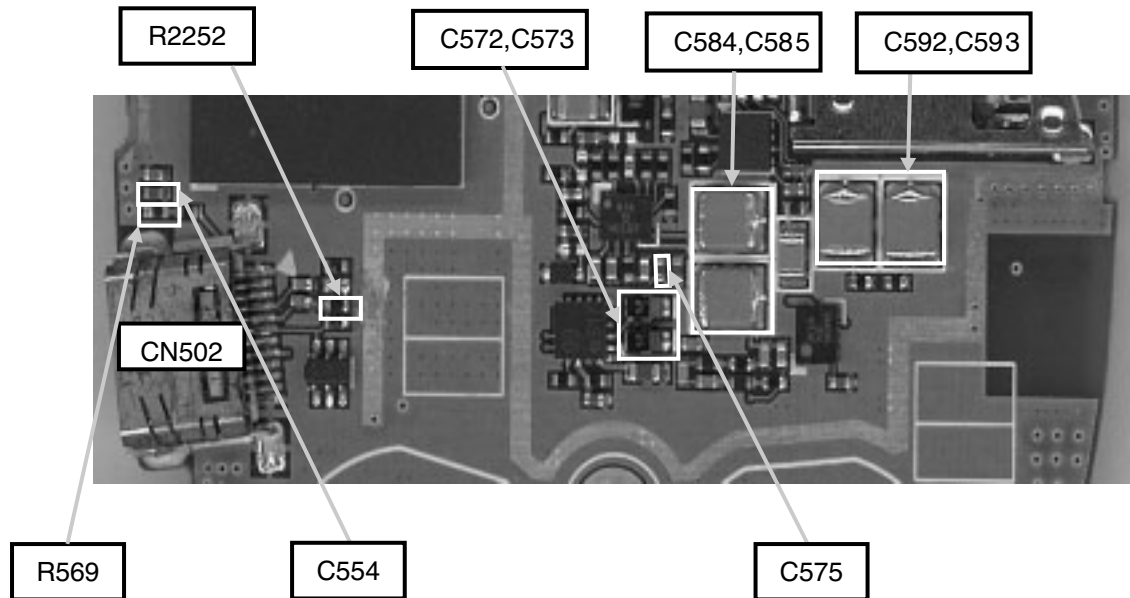


4. TROUBLE SHOOTING

4.12.5 Headset - MIC(Voice call, Video Telephony)



4.12.6 Headset



4. TROUBLE SHOOTING

4.13 Charger Trouble

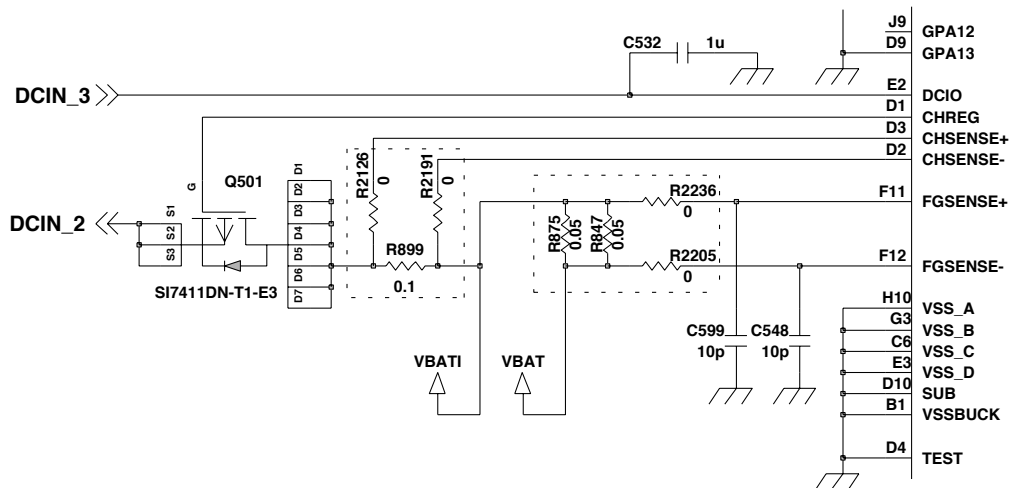
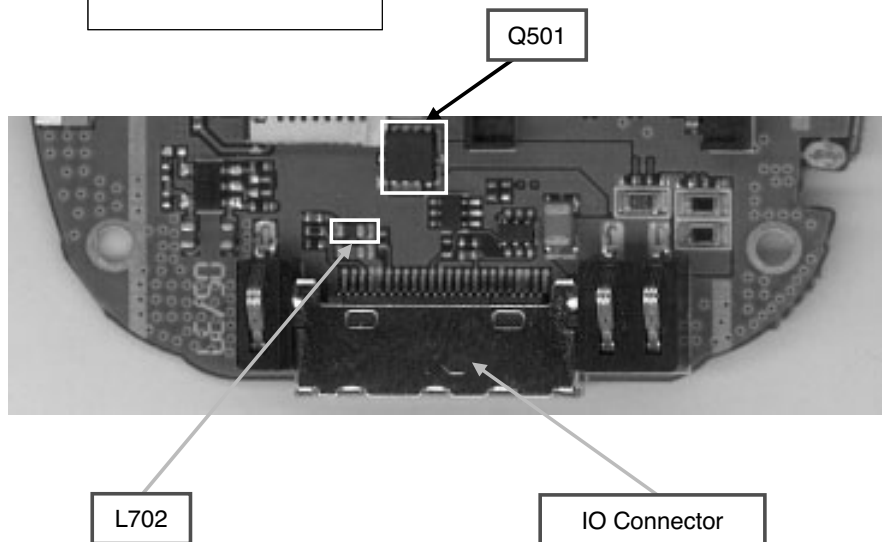
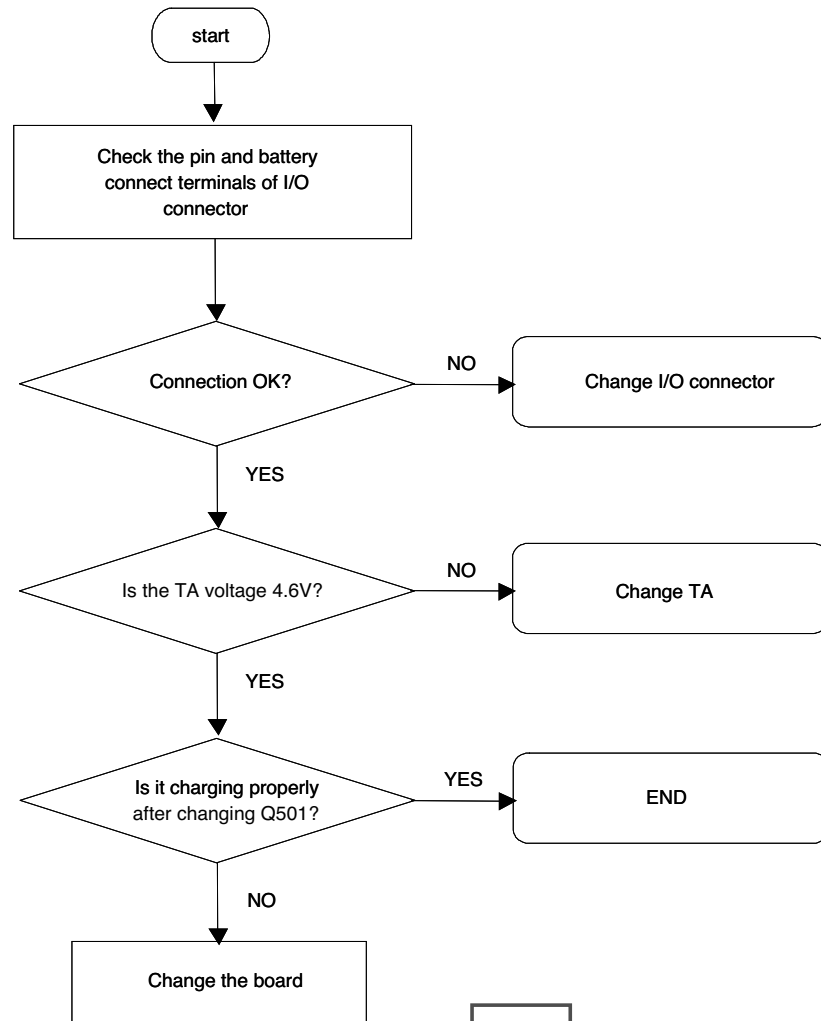


Figure 4-13-1. Main Battery Charging Path

- **Charging Procedure**
 - Connecting TA and Charger Detection
 - Control the charging current by AB2000(Vincenne)
 - Charging current flows into the battery
- **Check Point**
 - Connection of TA
 - Charging current path
 - Battery
- **Trouble shooting setup**
 - Connect TA and battery to the phone
- **Trouble Shooting Procedure**
 - Check the charger connecter
 - Check the Charging current Path
 - Check the battery

4. TROUBLE SHOOTING



4. TROUBLE SHOOTING

4.14 RF Component

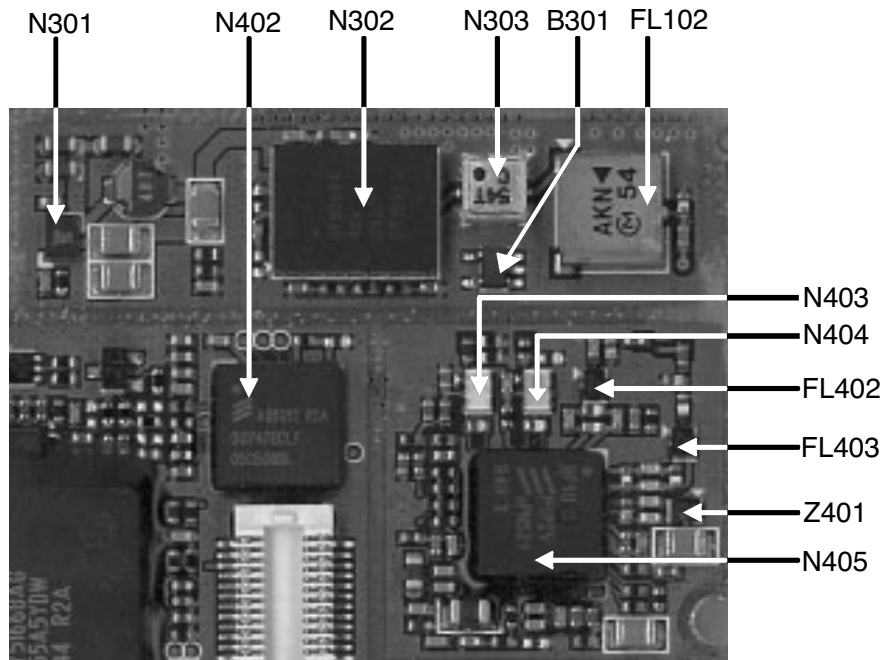


Figure 4-14-1. RF component (Top)

Reference	Description	Reference	Description
N301	VOLTAGE_REGULATOR	N403	DCS_TX_BALUN
N402	HERTA (GSM ADC)	N404	GSM_TX_BALUN
N302	WCDMA PAM	FL402	DCS_RX_SAW
N303	ISOLATOR	FL403	PCS_RX_SAW
B301	TEMP_SENSOR	Z401	GSM_RX_SAW
FL102	DUPLEXER	N405	GSM TRANSCEIVER

4. TROUBLE SHOOTING

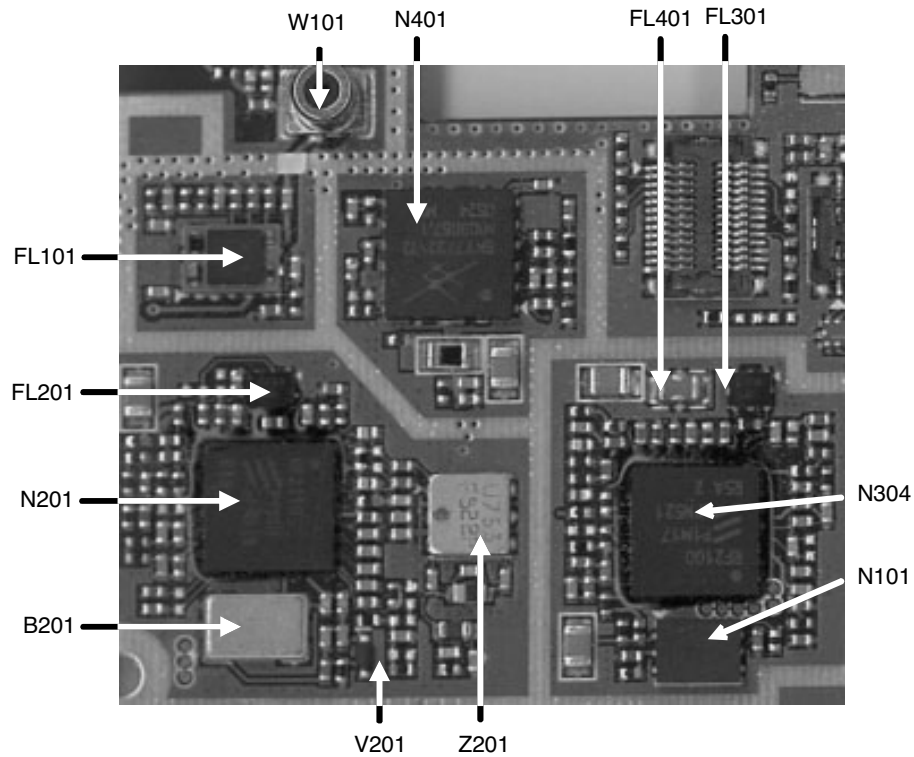
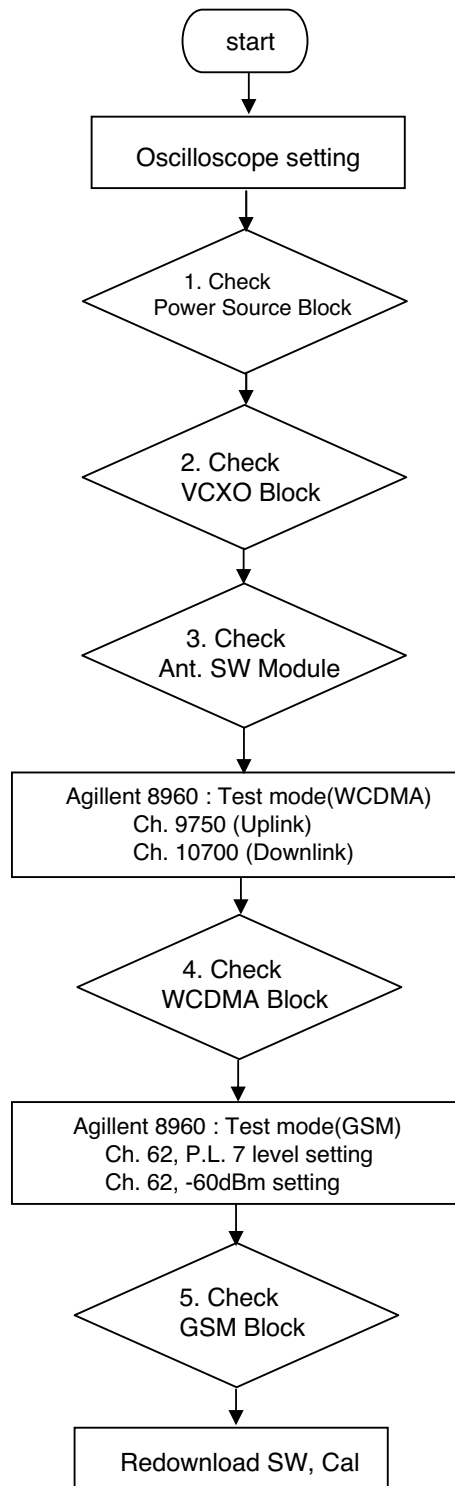


Figure 4-14-2. RF component (Bottom)

Reference	Description	Reference	Description
W101	TEST CONNECTOR	Z201	WCDMA RX IF SAW
N401	GSM PAM	V201	DIODE/VARIABLE CAP
FL401	EMI FILTER	B201	CRYSTAL
FL301	WCDMA TX RF SAW	N201	WCDMA RX IC (WOPY)
N304	WCDMA TX IC (WIVI)	FL201	WCDMA RX RF SAW
N101	REGULATOR	FL101	ANT SW MODULE

4. TROUBLE SHOOTING

4.15 Procedure to check



4.16 Checking Common Power Source Block

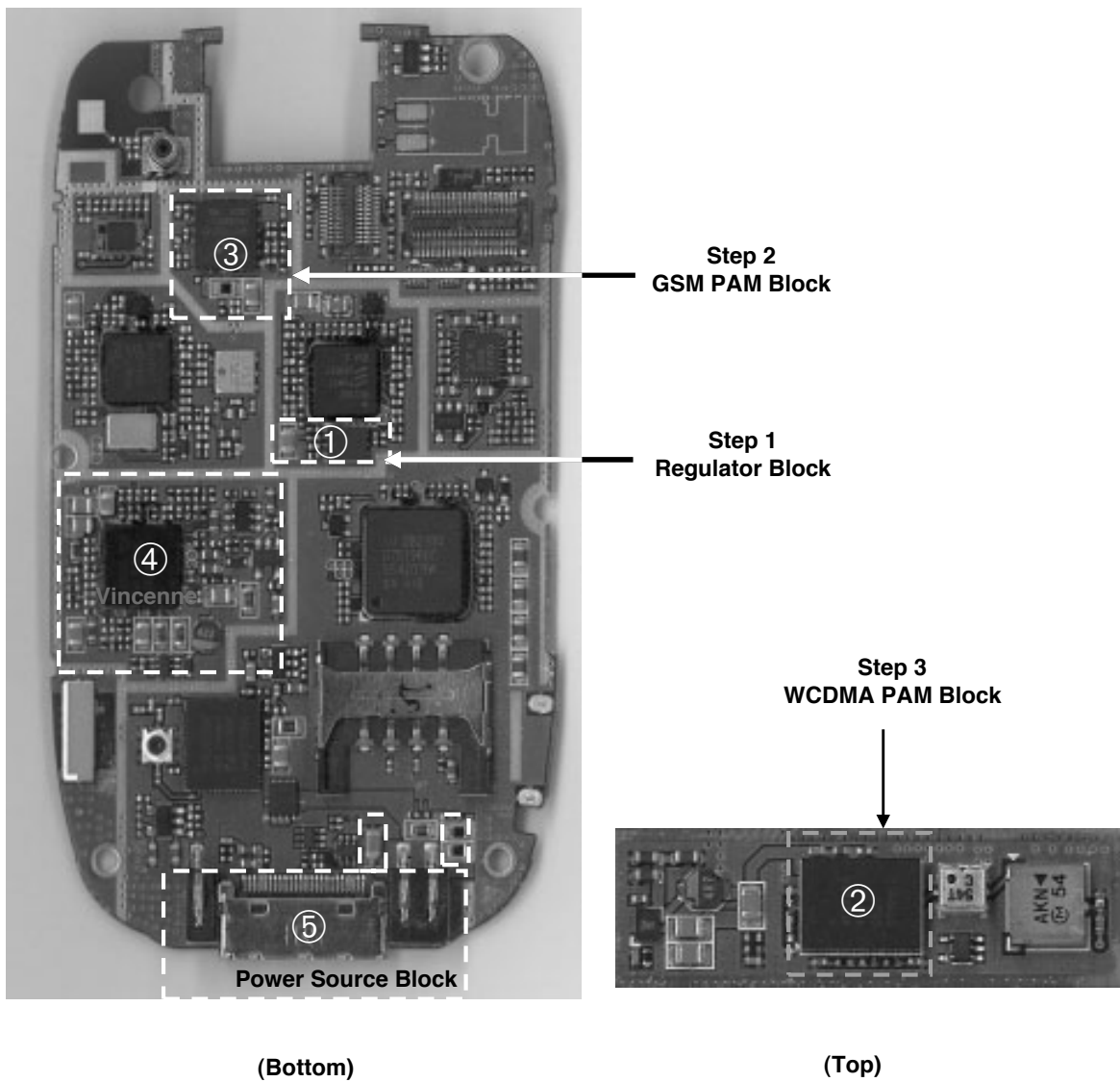
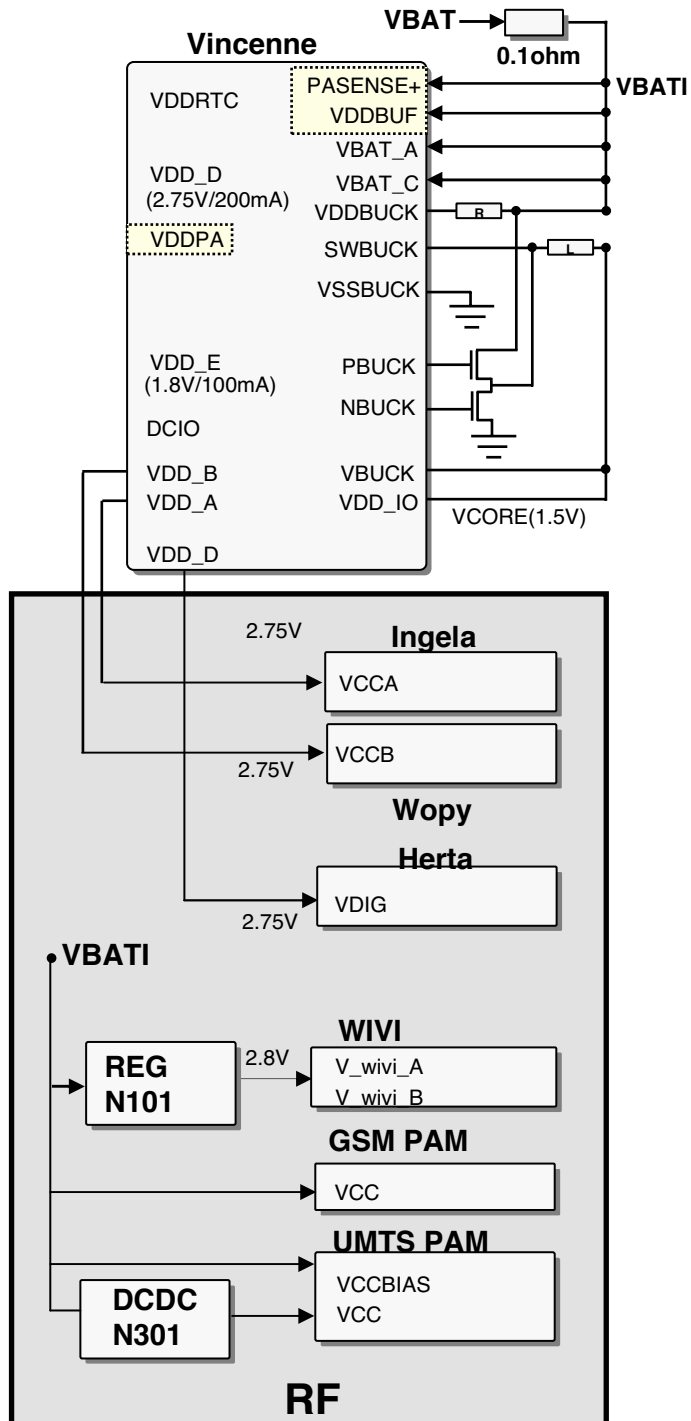


Figure 4-16-1. Common Source Block

4. TROUBLE SHOOTING

4.16 Checking Common Power Source Block Diagram



4.16.1 Step 1

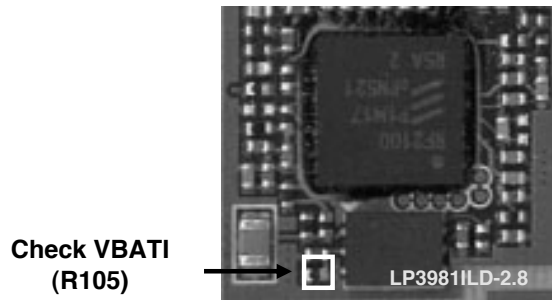


Figure 4-16-2. Step 1 : Regulator Block ①

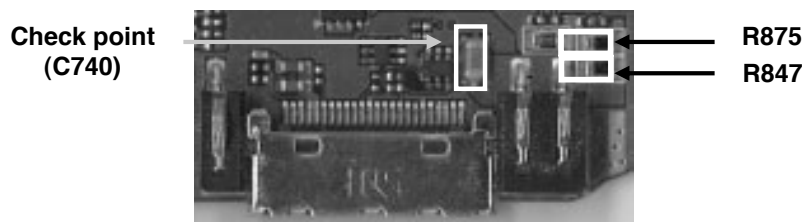
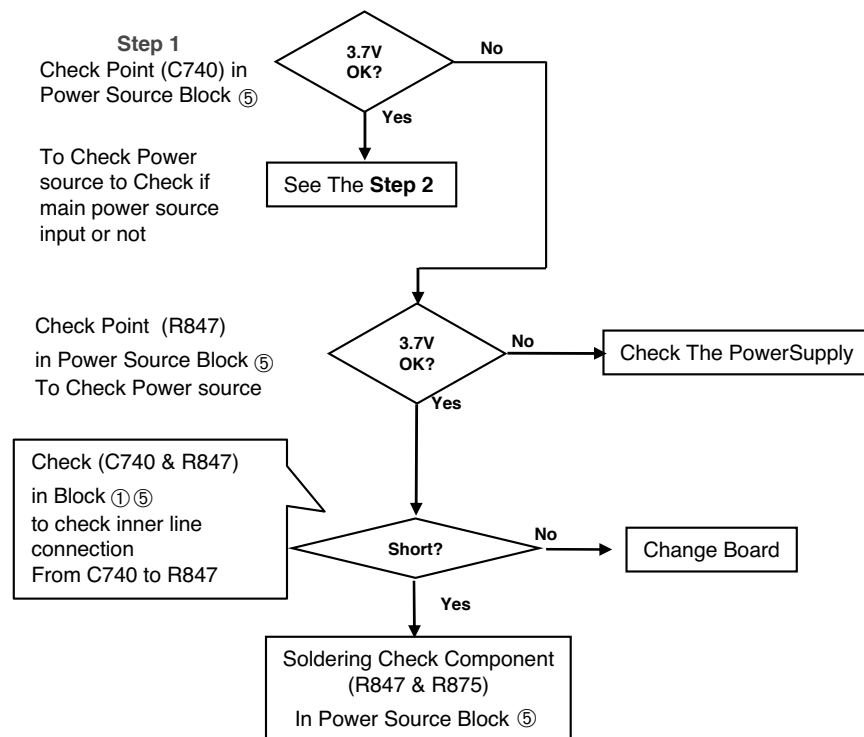


Figure 4-16-3. Power Source Block ⑤



4. TROUBLE SHOOTING

4.16.2 Step 2

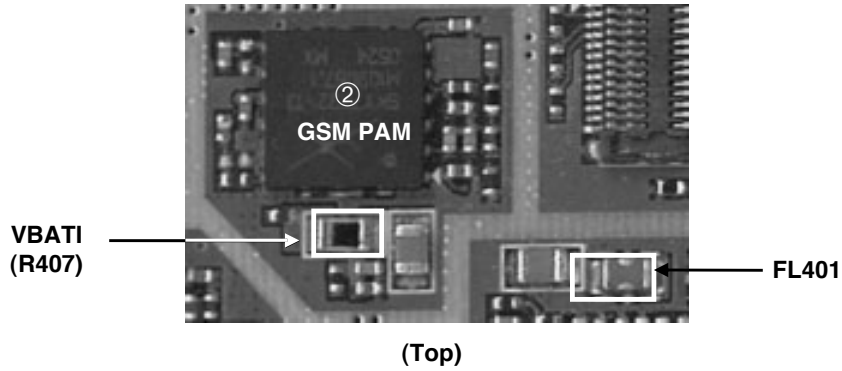
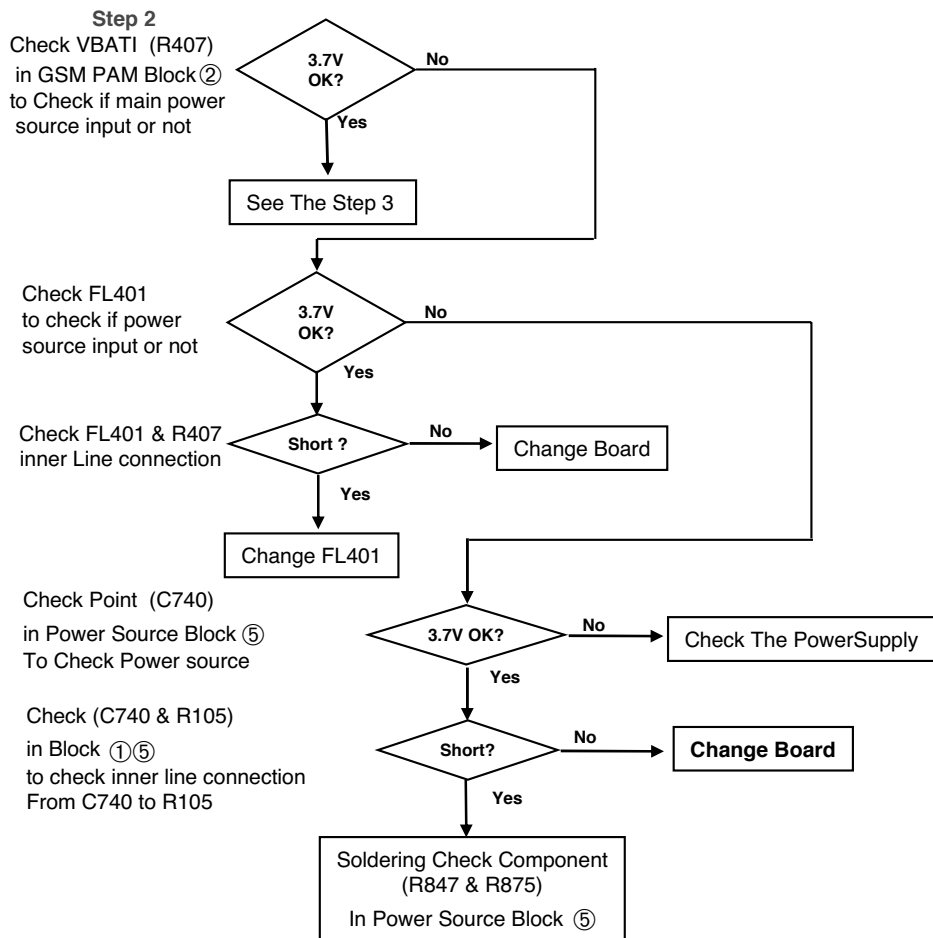


Figure 4-16-4. Step 2 :GSM PAM Block ②



4.16.3 Step 3

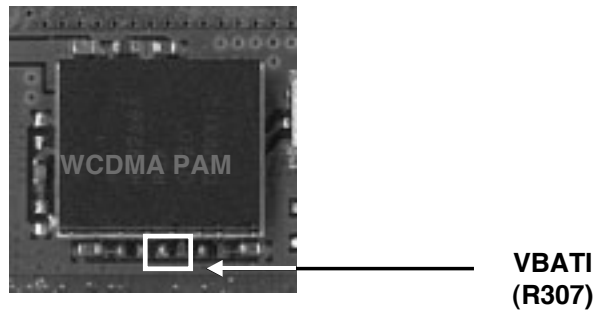


Figure 4-16-5. Step 3 :WCDMA PAM Block ③

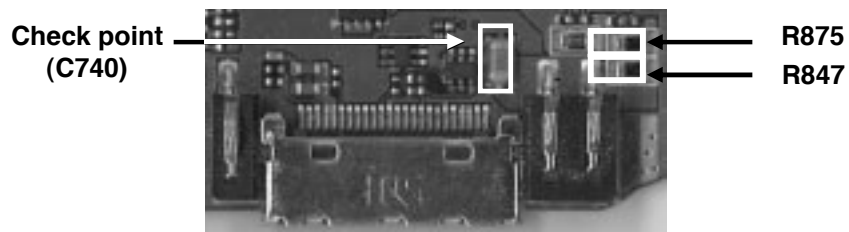
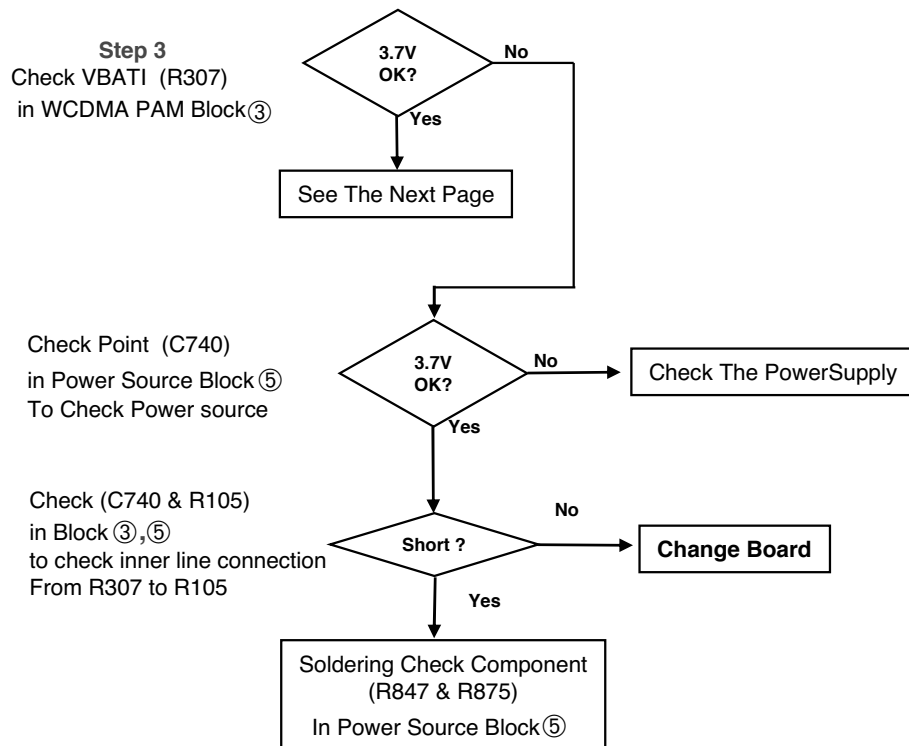


Figure 4-16-6. PAM Power Source ⑤



4. TROUBLE SHOOTING

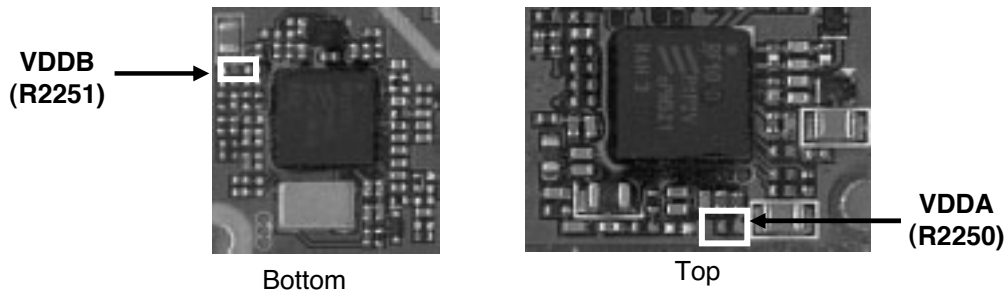
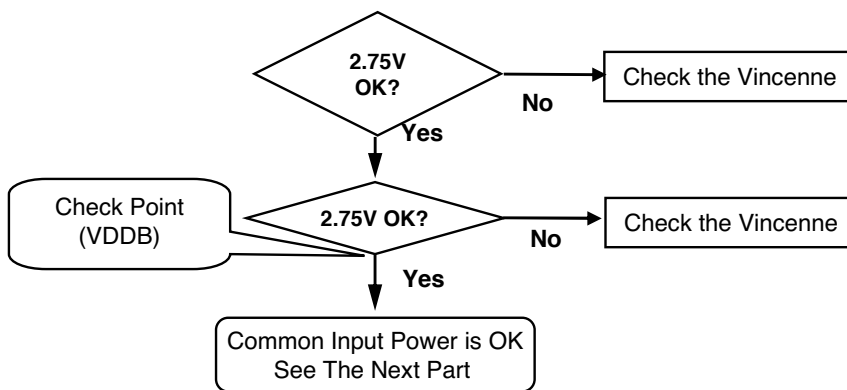
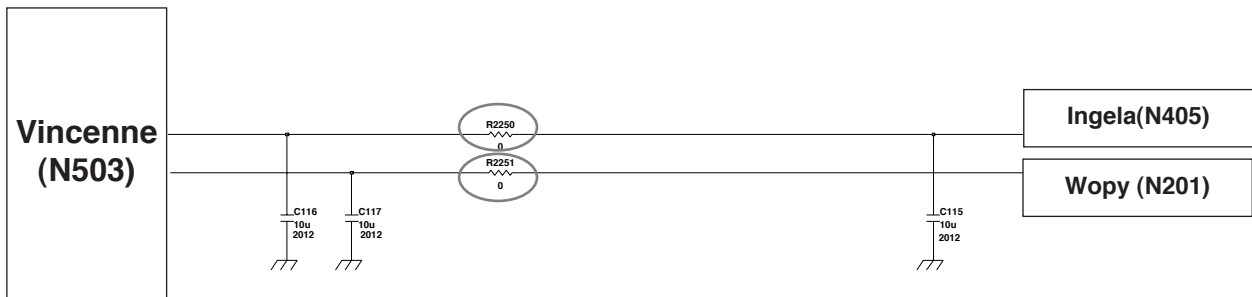


Figure 4-16-7. Power for Radio ASIC



4.16.5 Checking Regulator Part

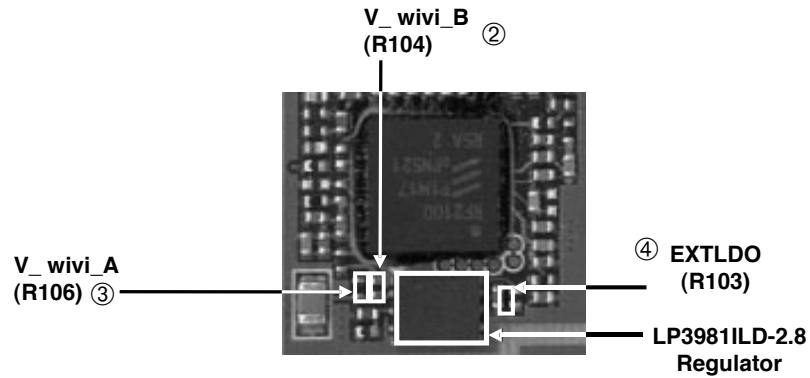


Figure 4-16-8. Regulator Block

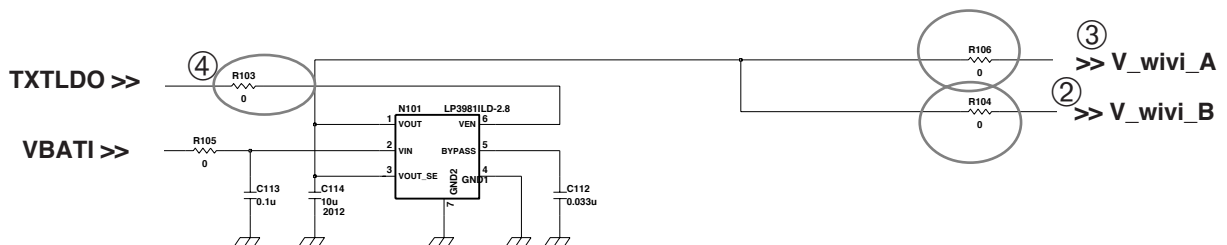
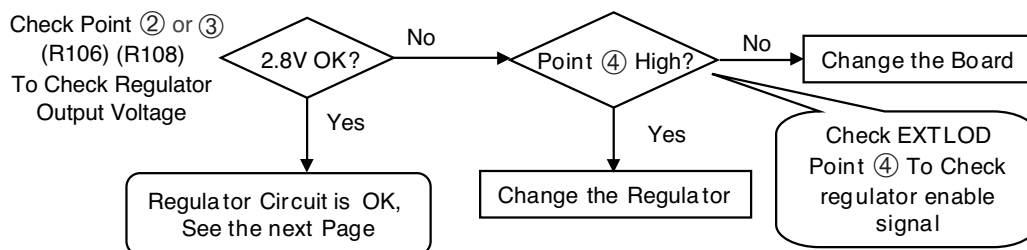


Figure 4-16-9. Regulator Circuit Diagram



4. TROUBLE SHOOTING

4.17 Checking VCXO Block

The reference frequency (13MHz) from B201 (Crystal) is used WCDMA TX part and BB part. Therefore you have to check below 3 point.

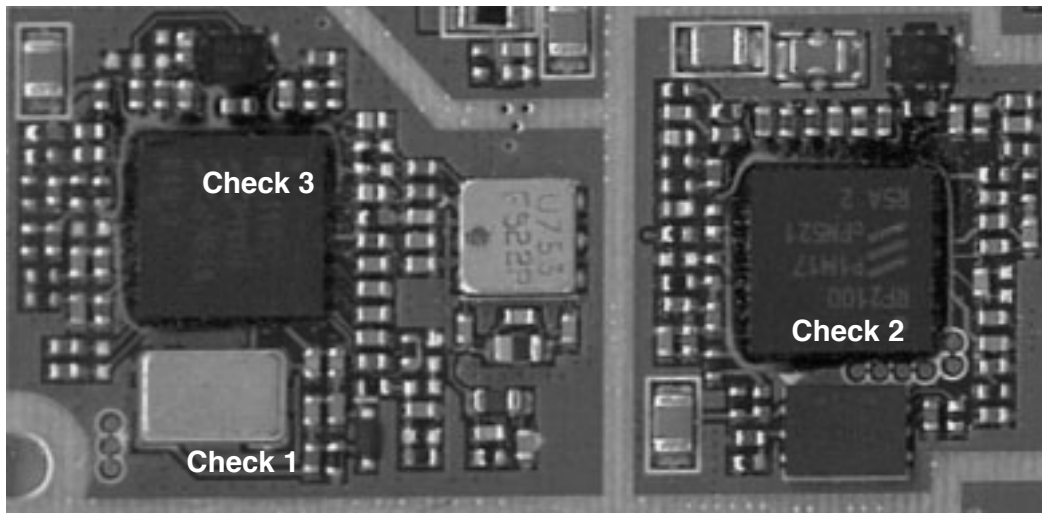


Figure 4-17-1. Bottom Place

4. TROUBLE SHOOTING

Check 1. Crystal part

If you already check this crystal part, you can skip check 1.

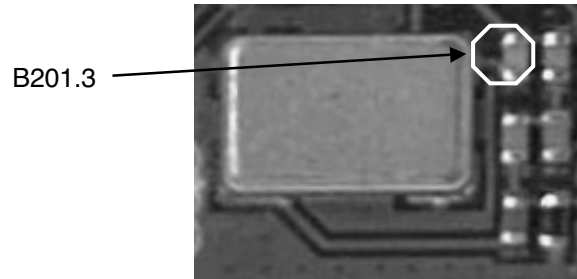


Figure 4-17-2. Test Point (Crystal Part)

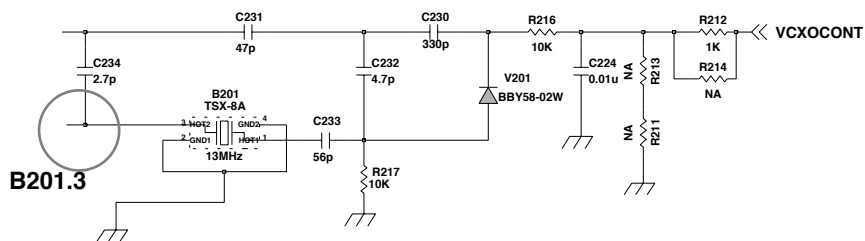


Figure 4-17-3. Schematic of the Crystal Part

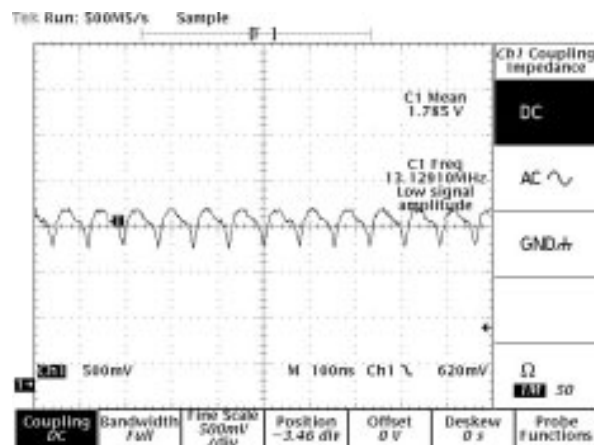


Figure 4-17-4. 13MHz at B201.3

4. TROUBLE SHOOTING

Check 2. 13MHz at TX part

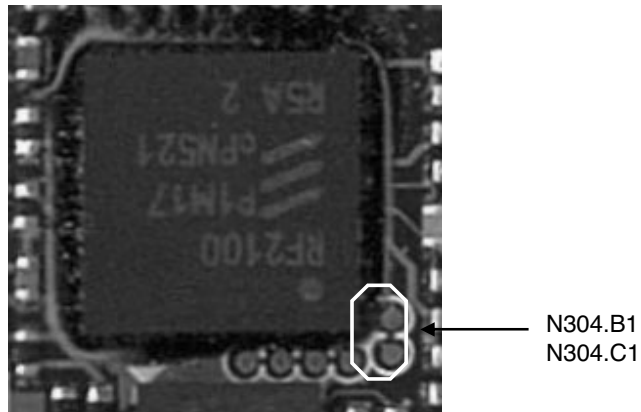


Figure 4-17-5. Test point (13MHz at TX part)

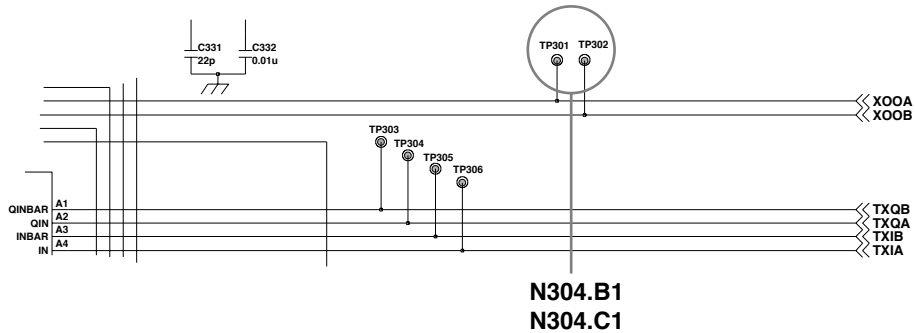


Figure 4-17-6. Schematic of the Tx Part

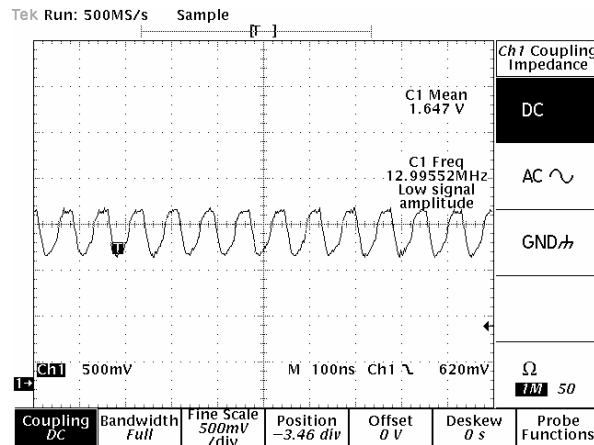


Figure 4-17-7. 13MHz at N304.B1,C1

4. TROUBLE SHOOTING

Check 3. 13MHz at BB part

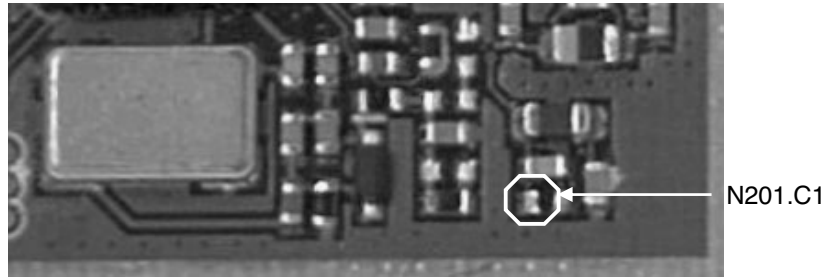


Figure 4-17-8. Test point (13MHz at BB part)

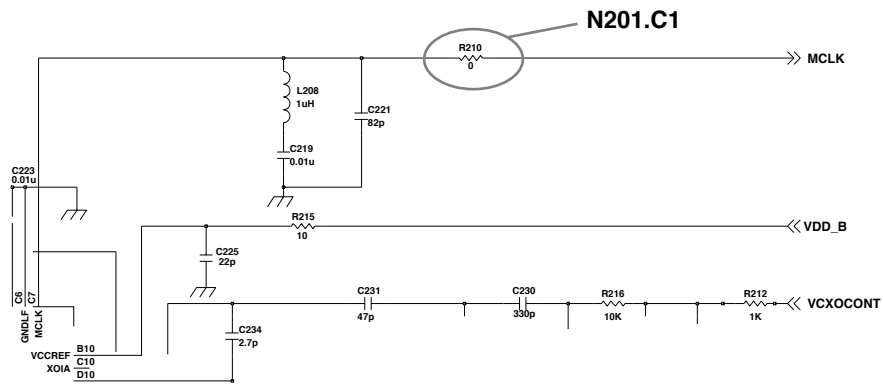


Figure 4-17-9. Schematic (13MHz at BB Part)

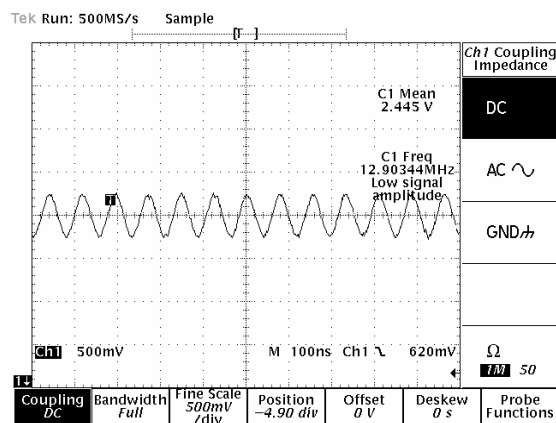
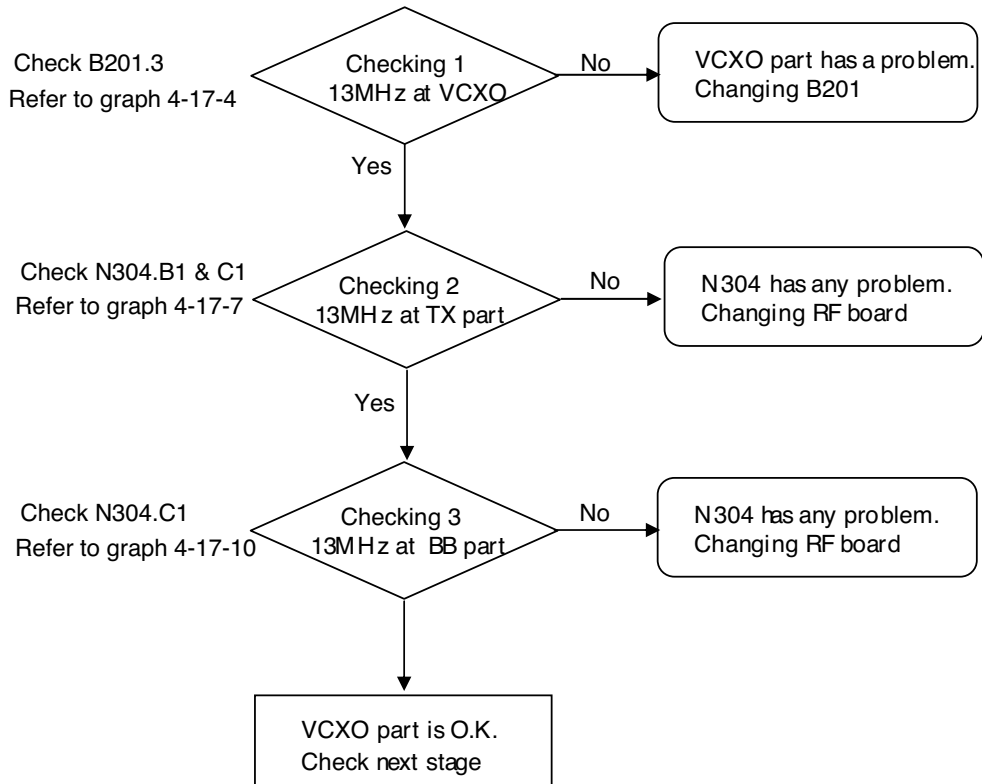


Figure 4-17-10. 13MHz at N201.C1

4. TROUBLE SHOOTING



4.18 Checking Ant. SW Module Block

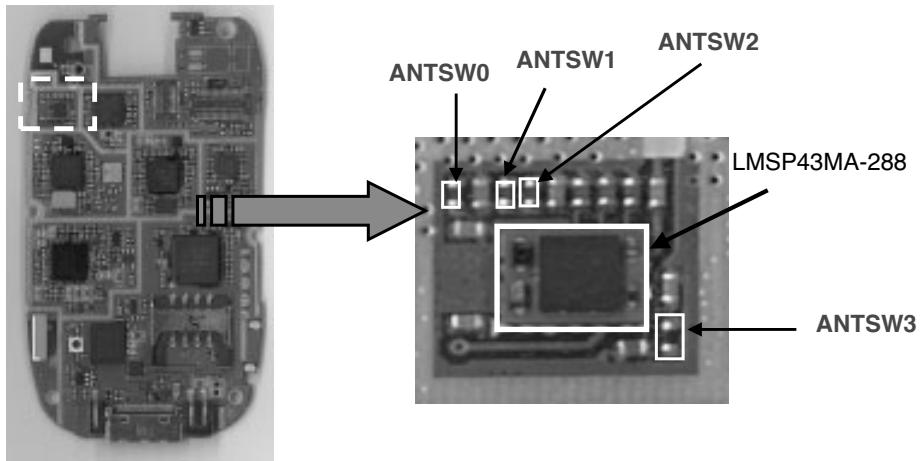


Figure 4-18-1. Antenna Switch Block(Bottom)

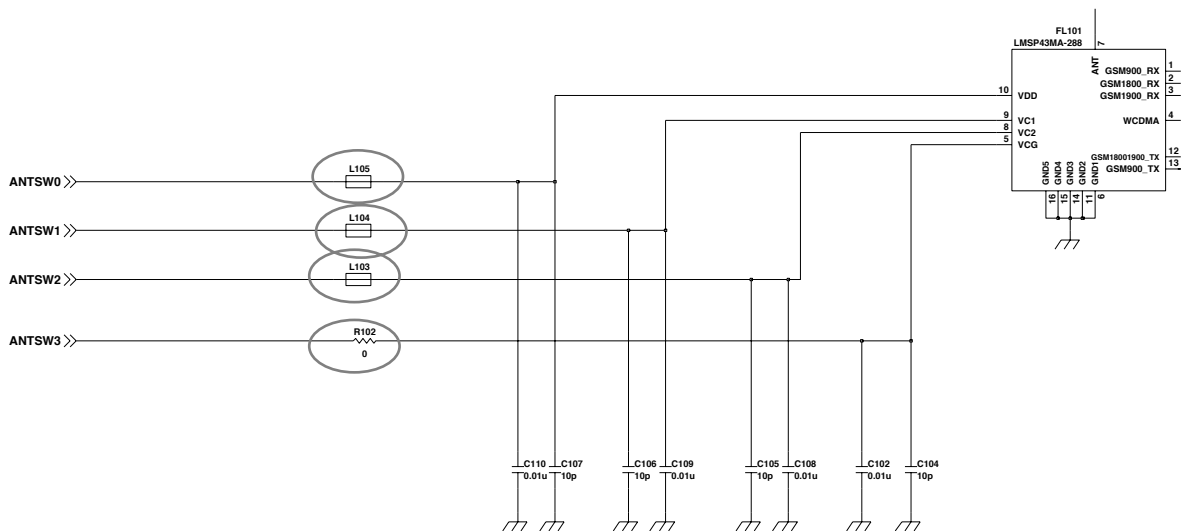
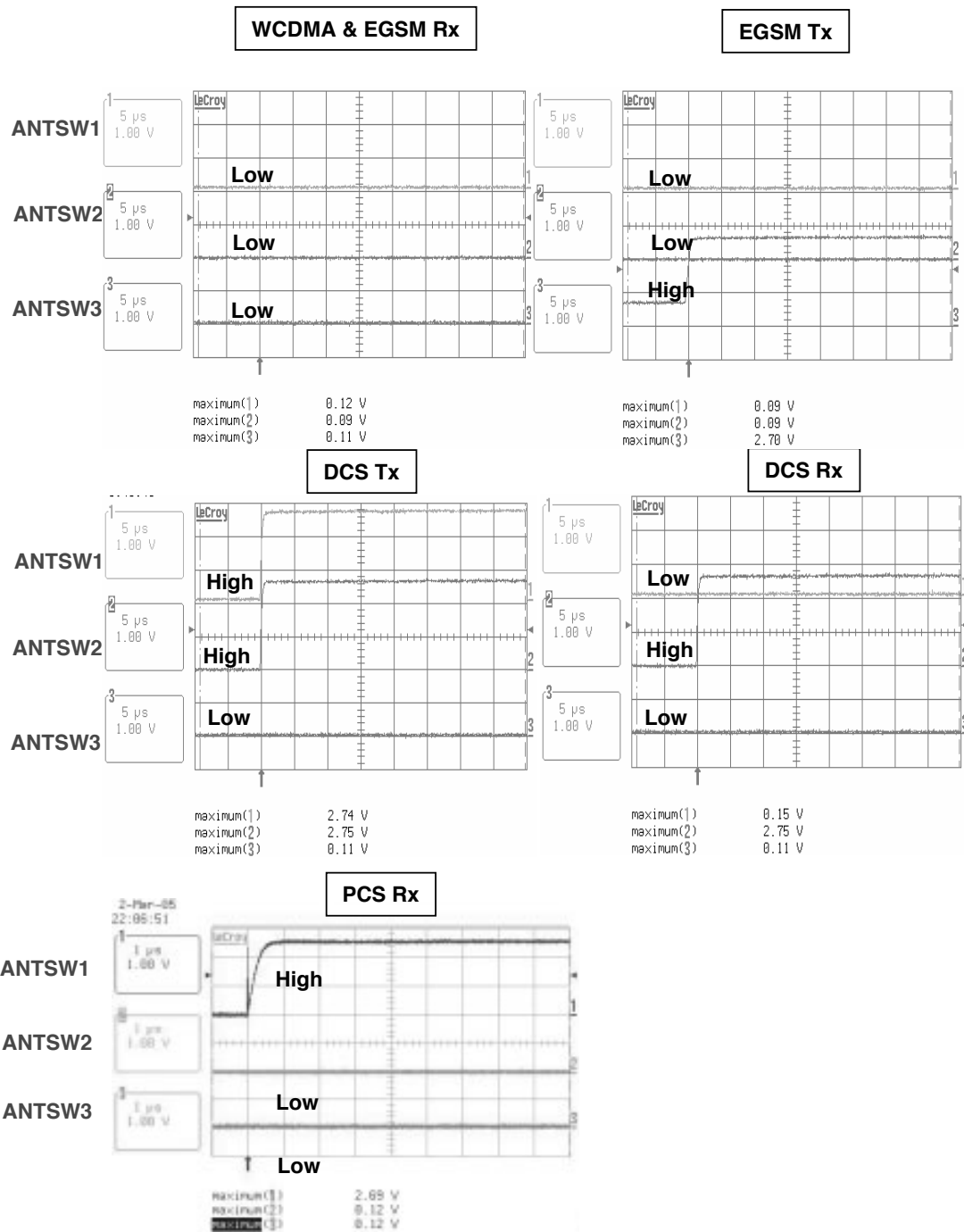


Figure 4-18-2. Schematic of Antenna Switch Block(Bottom)

4. TROUBLE SHOOTING

4.19 Checking Antenna Switch Block input logic

4.19.1 Mode Logic by TP Command



4. TROUBLE SHOOTING

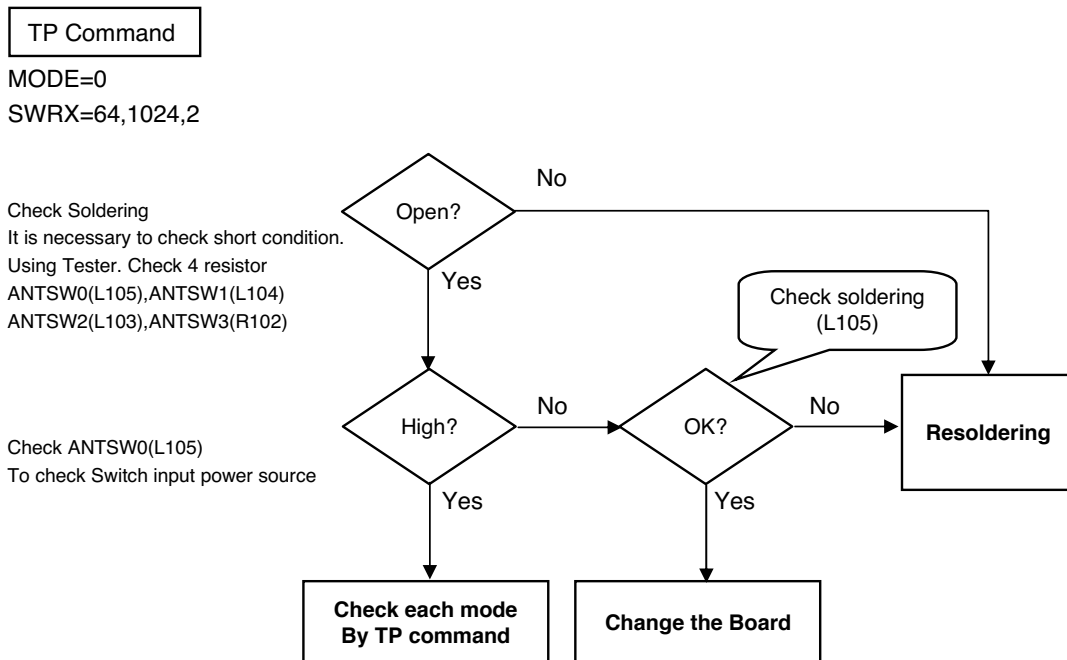
Band	ANTSW0	ANTSW1	ANTSW2	ANTSW3
EGSM Tx	H	L	L	H
EGSM Rx	H	L	L	L
DCS Tx	H	H	H	L
DCS Rx	H	L	H	L
PCS RX	H	H	L	L
WCDMA	H	L	L	L

Figure 4-19-1. Antenna Switch Module Logic

4. TROUBLE SHOOTING

4.19.2 Checking Switch Block power source

* Before Checking this part, must check common power source(through Vincenne) part



A. EGSM Rx mode

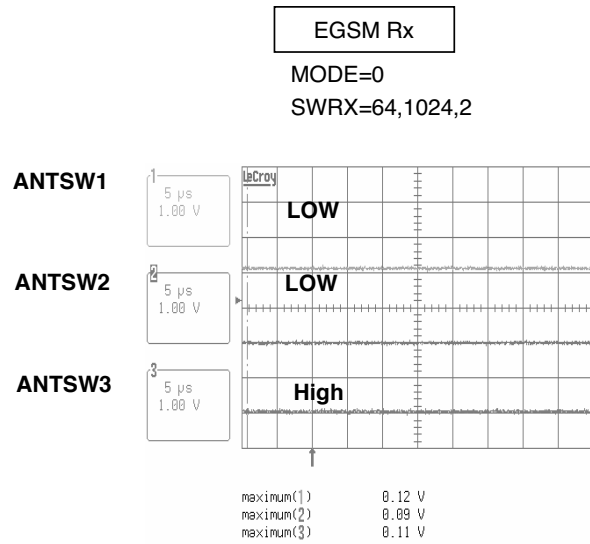


Figure 4-19-2. EGSM Rx Mode

B. EGSM Tx mode

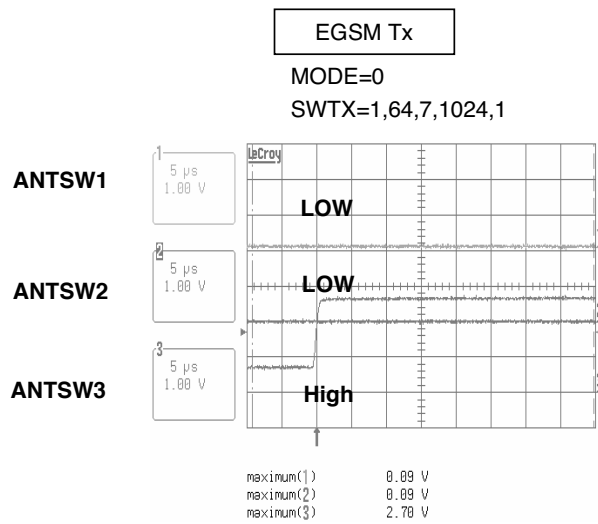


Figure 4-19-3. EGSM Tx Mode

4. TROUBLE SHOOTING

C. DCS Rx mode

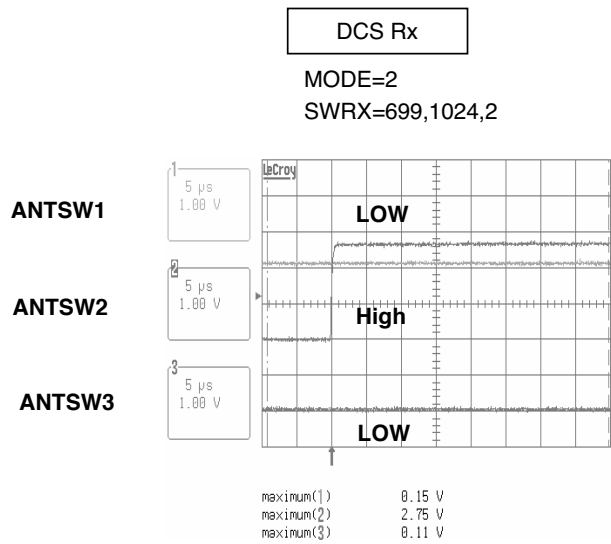


Figure 4-19-4. DCS Rx Mode

D. PCS Rx mode

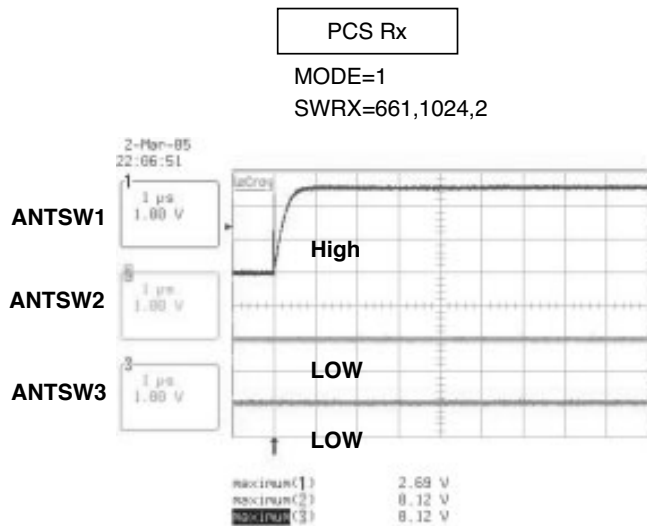


Figure 4-19-5. PCS Rx Mode

4. TROUBLE SHOOTING

E. DCS / PCS Tx mode

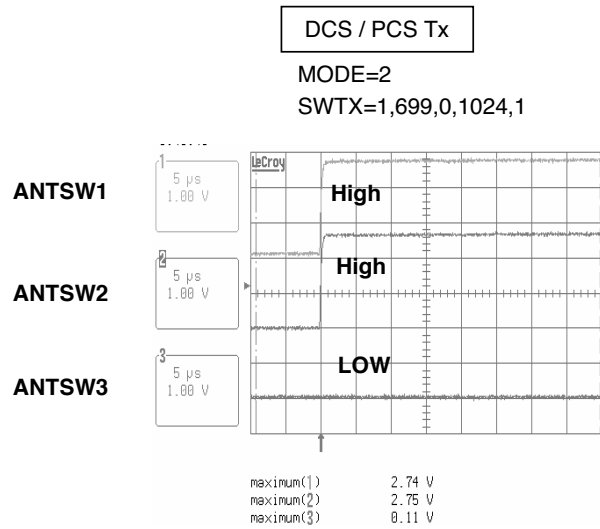


Figure 4-19-6. DCS / PCS Tx Mode

4. TROUBLE SHOOTING

F. WCDMA mode

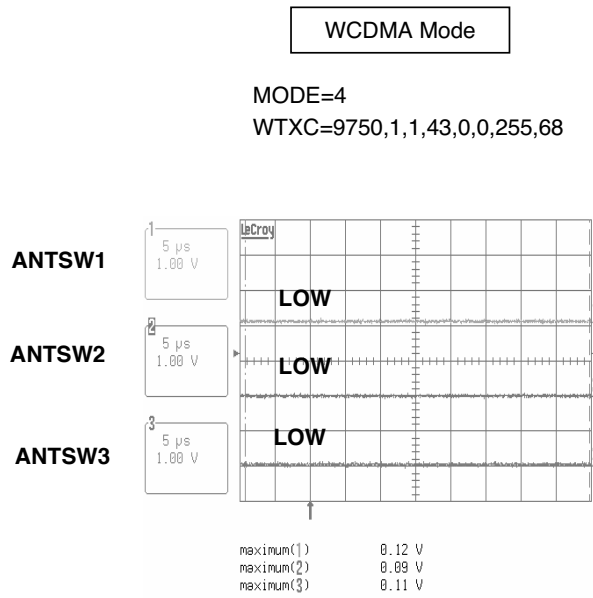
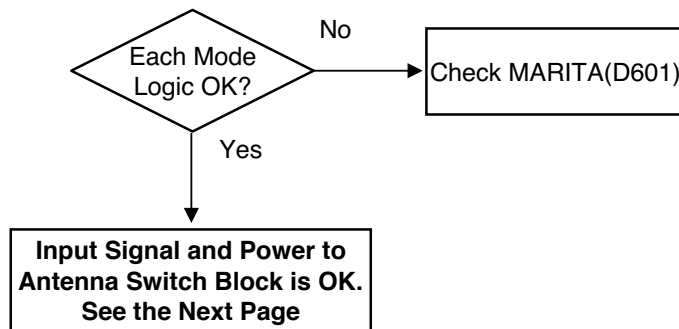
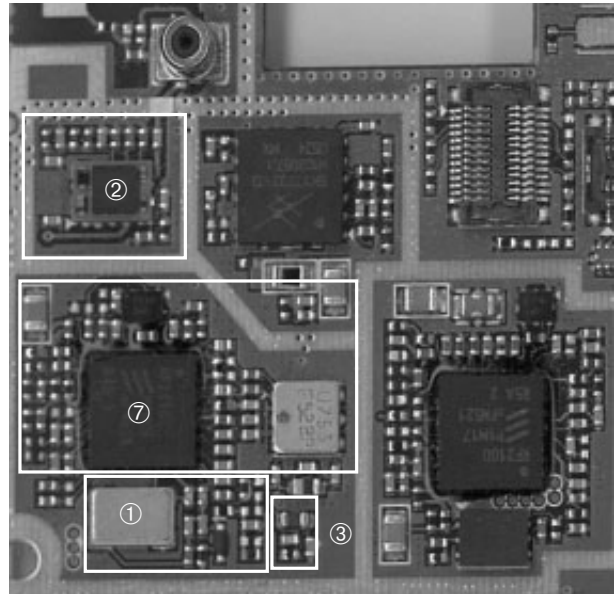
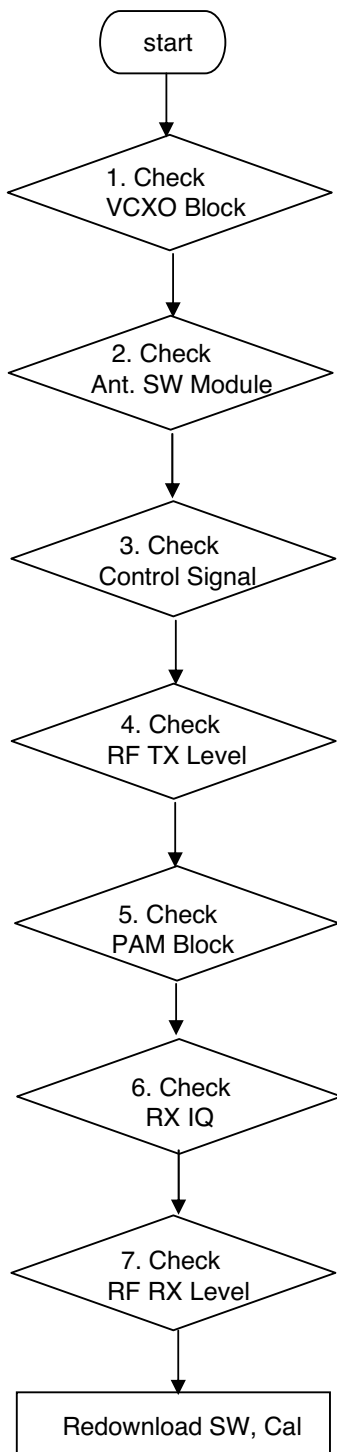


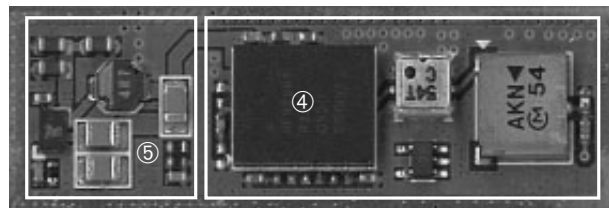
Figure 4-19-7. WCDMA Mode



4.20 Checking WCDMA Block



Bottom View



Top View

4. TROUBLE SHOOTING

4.20.1 Checking VCXO Block

Refer to 4.17

4.20.2 Checking Ant. SW module

Refer to 4.18

4.20.3 Checking Control Signal

First of all, you have to check control signal. (data, clk, strobe)

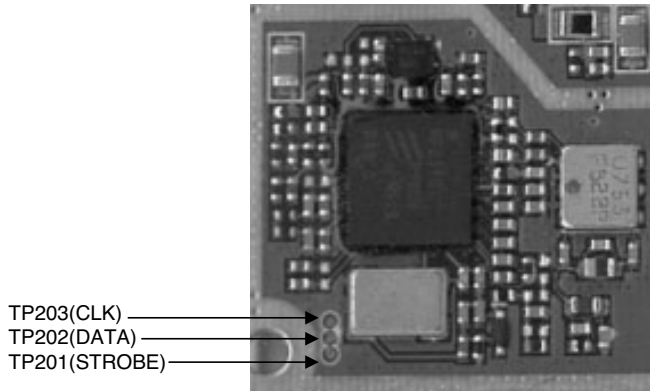


Figure 4-20-1. Test point (Control Signal)

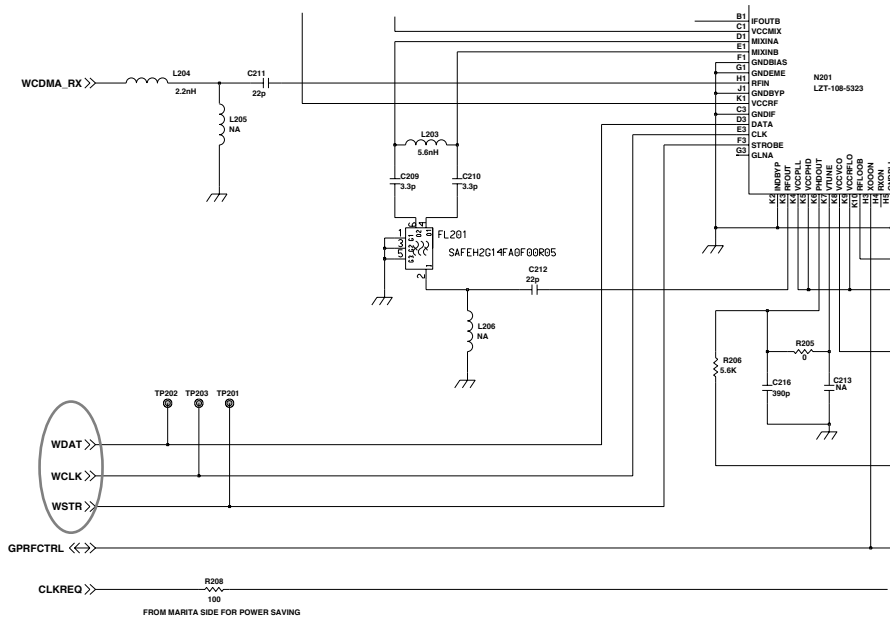


Figure 4-20-2. Schematic (Control Signal)

4. TROUBLE SHOOTING

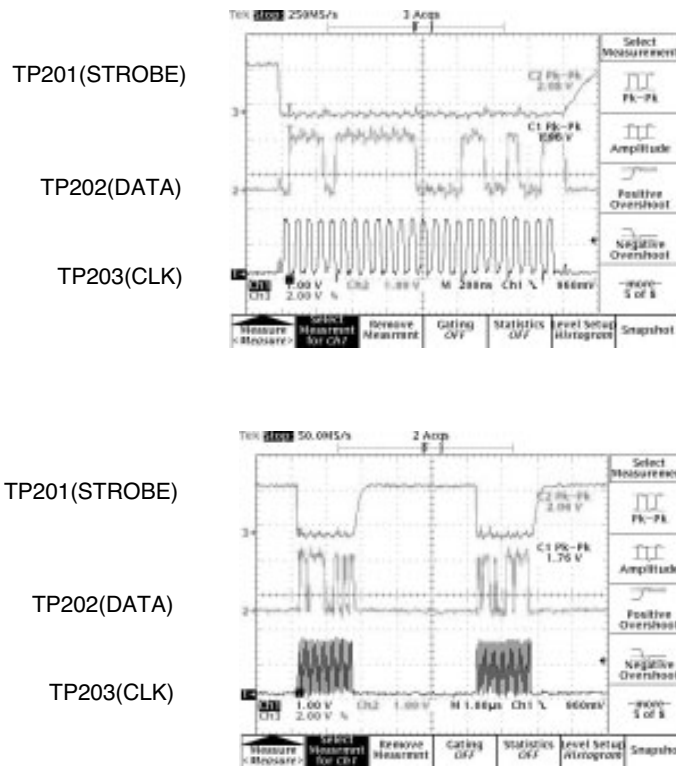
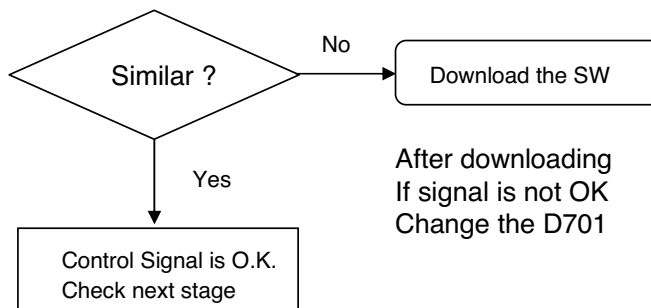


Figure 4-20-3. Control Signal

Check TP201, TP202
TP203. Check shape
and pk-pk level
Refer to Graph 4-30



4. TROUBLE SHOOTING

4.20.4 Checking RF TX Level

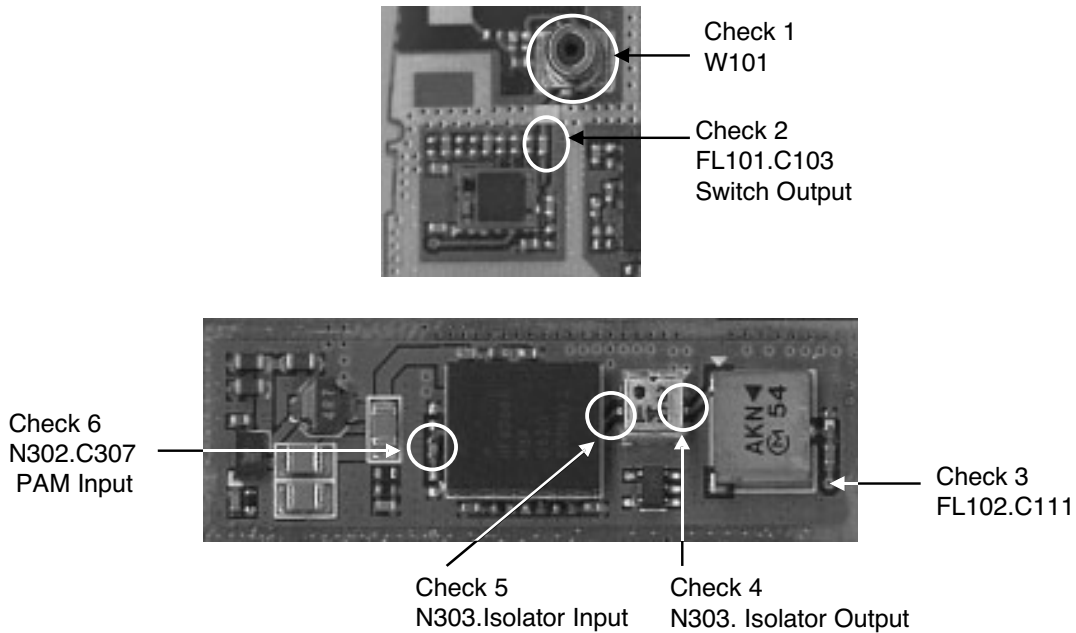


Figure 4-20-4. Test point (RF TX Level)

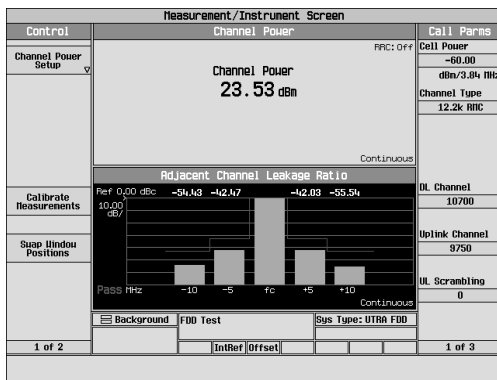


Fig. 4-20-5 Output Level at RF test connector (W101)

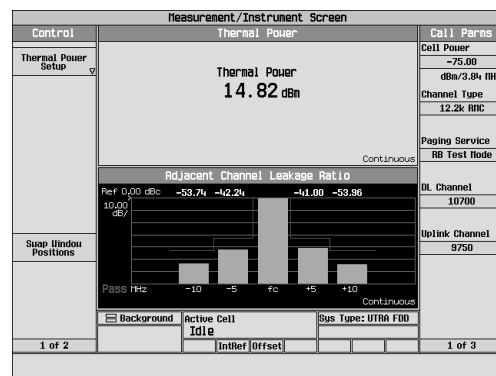


Fig. 4-20-6 Output Level at Switch Output (FL101 , C103)

4. TROUBLE SHOOTING

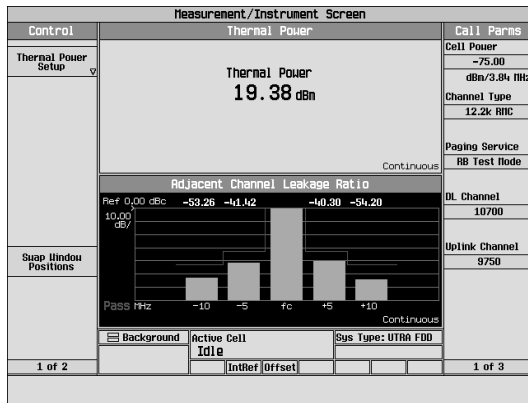


Fig. 4-20-7 Output Level at FL102.C111



Fig. 4-20-8 Output Level at Isolator Output (N303.Out)

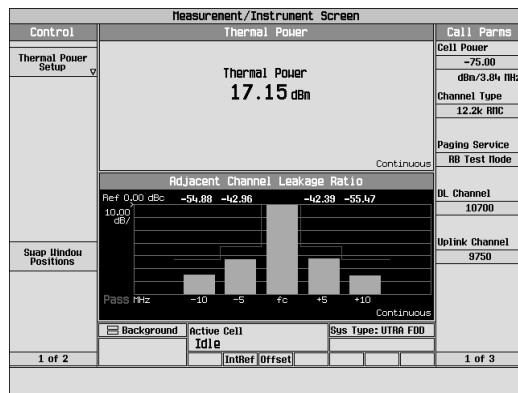


Fig. 4-20-9 Output Level at Isolator Input (N303.In)

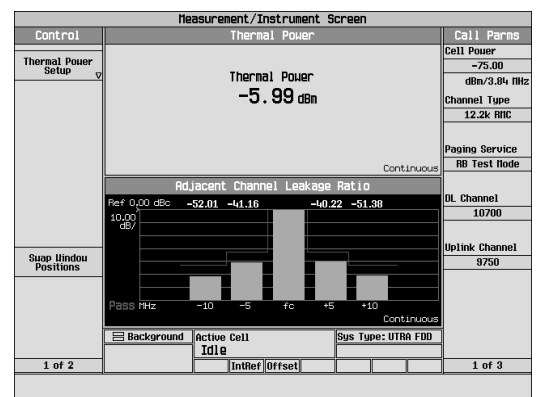


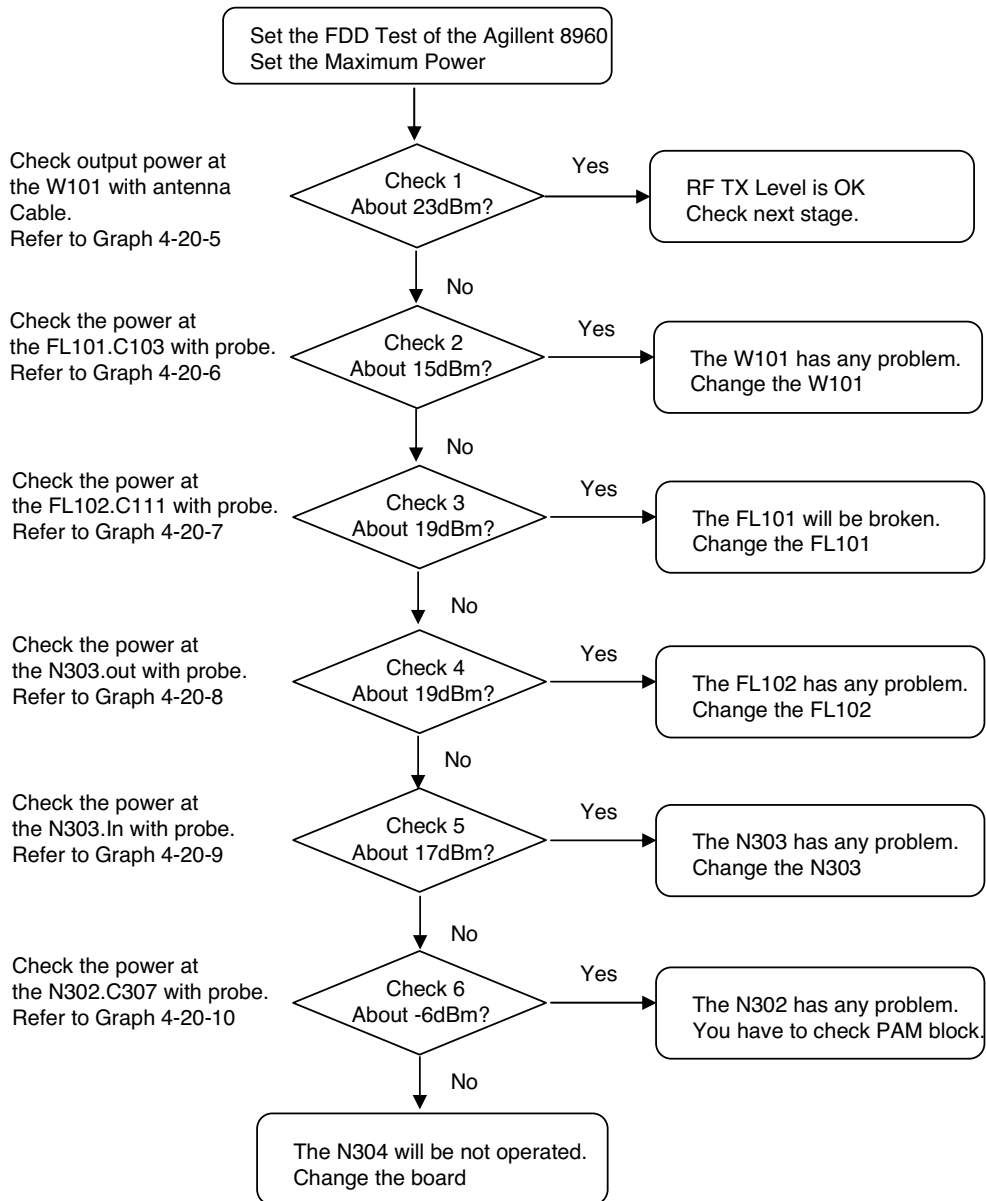
Fig. 4-20-10 Output Level at PAM Input (N302,C307)



Fig. 4-20-11 Output Level at Wivi Output (N304.C320)

4. TROUBLE SHOOTING

To verify that the phone fulfils requirements on maximum output power.



4.20.5 Checking PAM Block

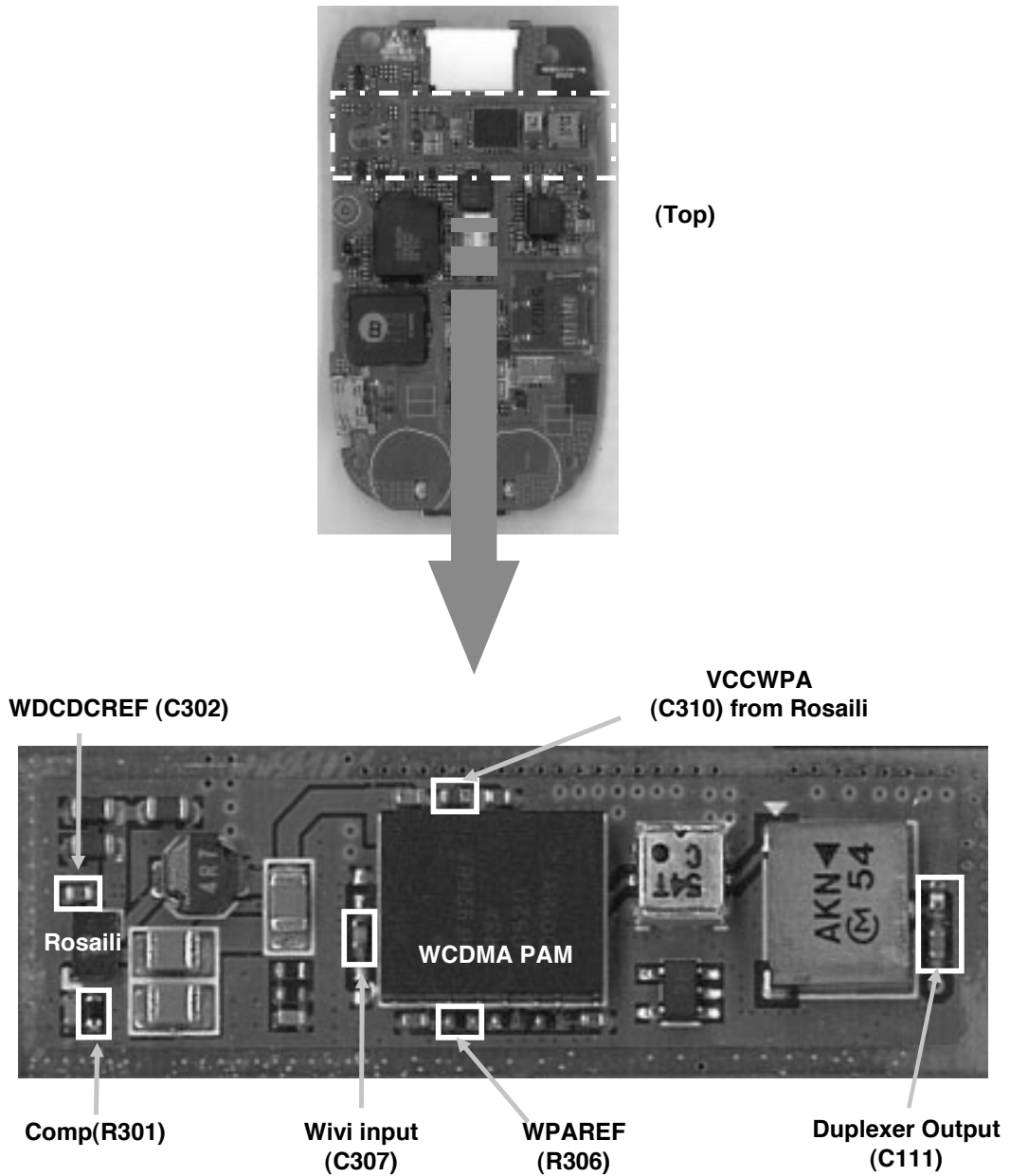


Figure 4-20-12. Test point

4. TROUBLE SHOOTING

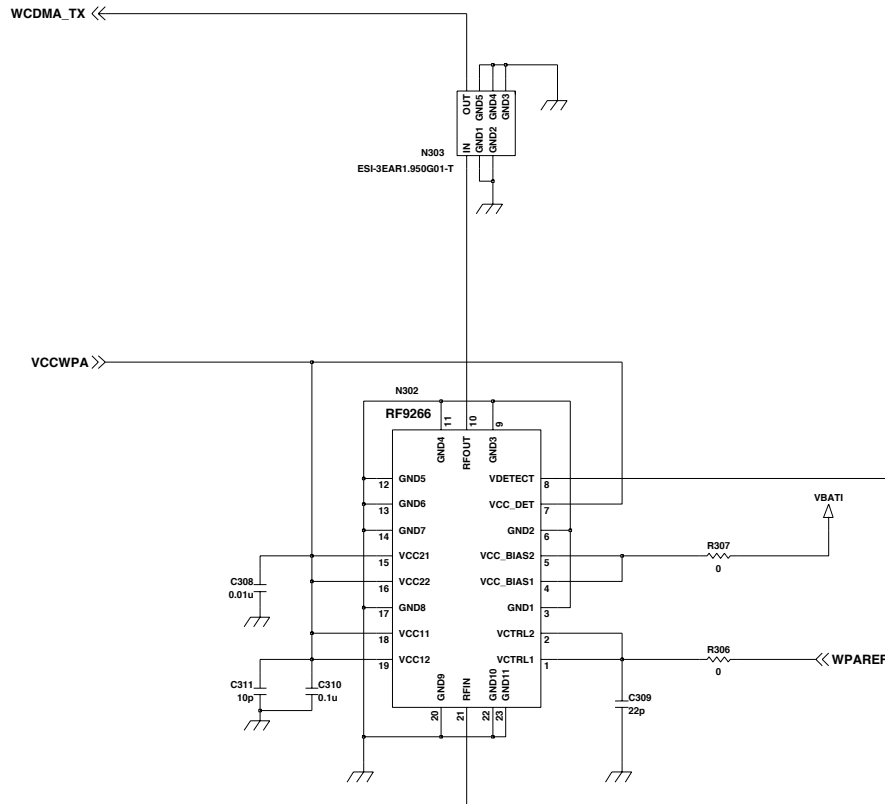


Figure 4-20-13. Schematic(PAM)

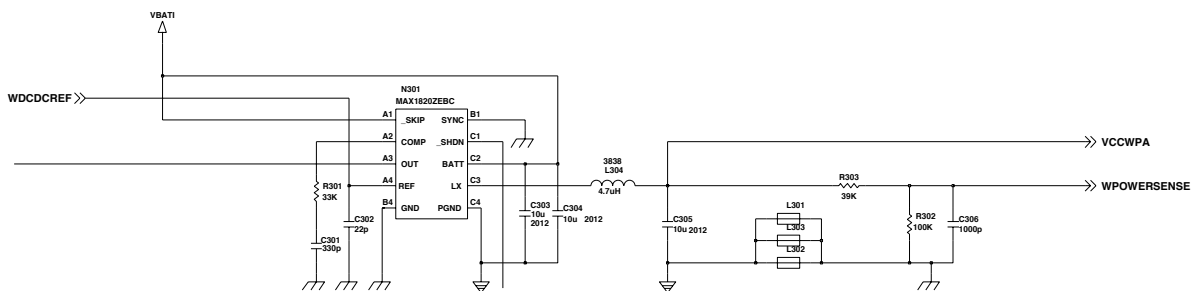
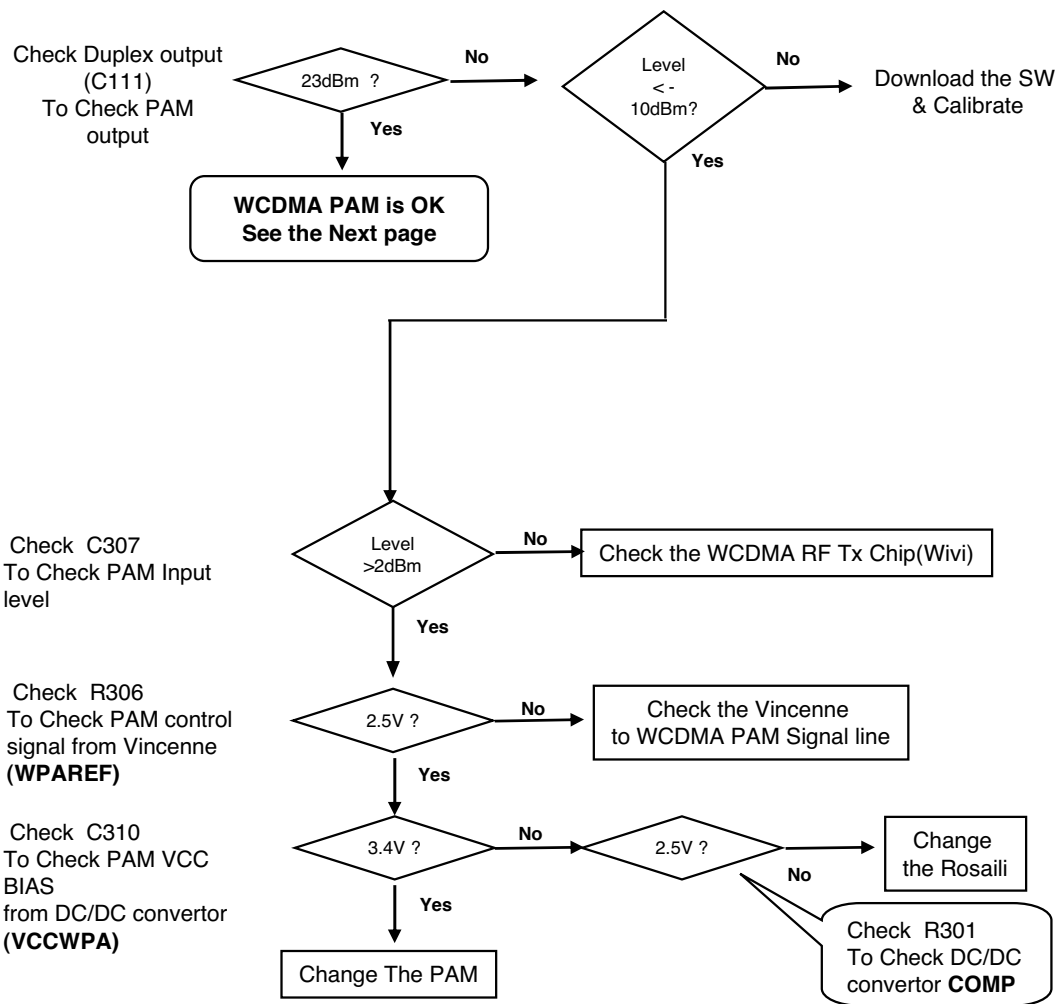


Figure 4-20-14. Schematic(DC-DC convertor:Rosaili)

4. TROUBLE SHOOTING

TP Command
-mode =4
-wtxc = 9750,1,1,43,0,0,255,68



4.20.6 Checking RX I,Q

To verify the RX path you have to check the pk-pk level and the shape of the RX I,Q.

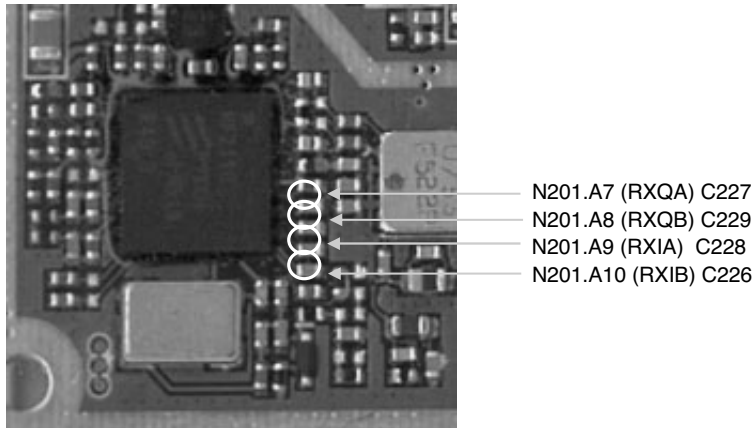


Figure 4-20-15. WCDMA RF RX IC (Bottom)

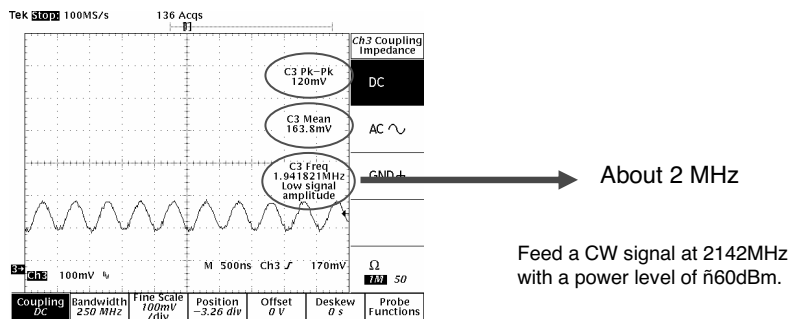


Figure 4-20-16. RX I,Q signal (CW:2142MHz)

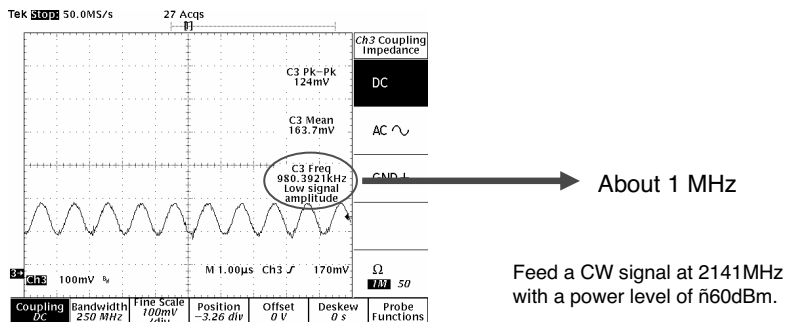


Figure 4-20-17. RX I,Q signal (CW:2141MHz)

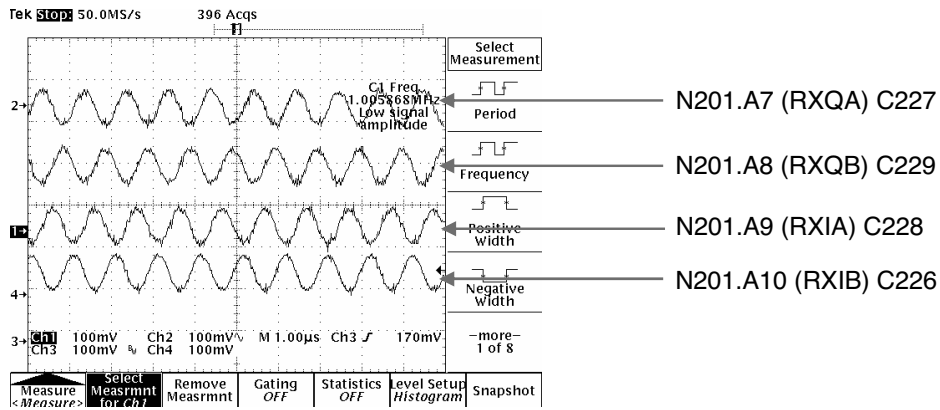
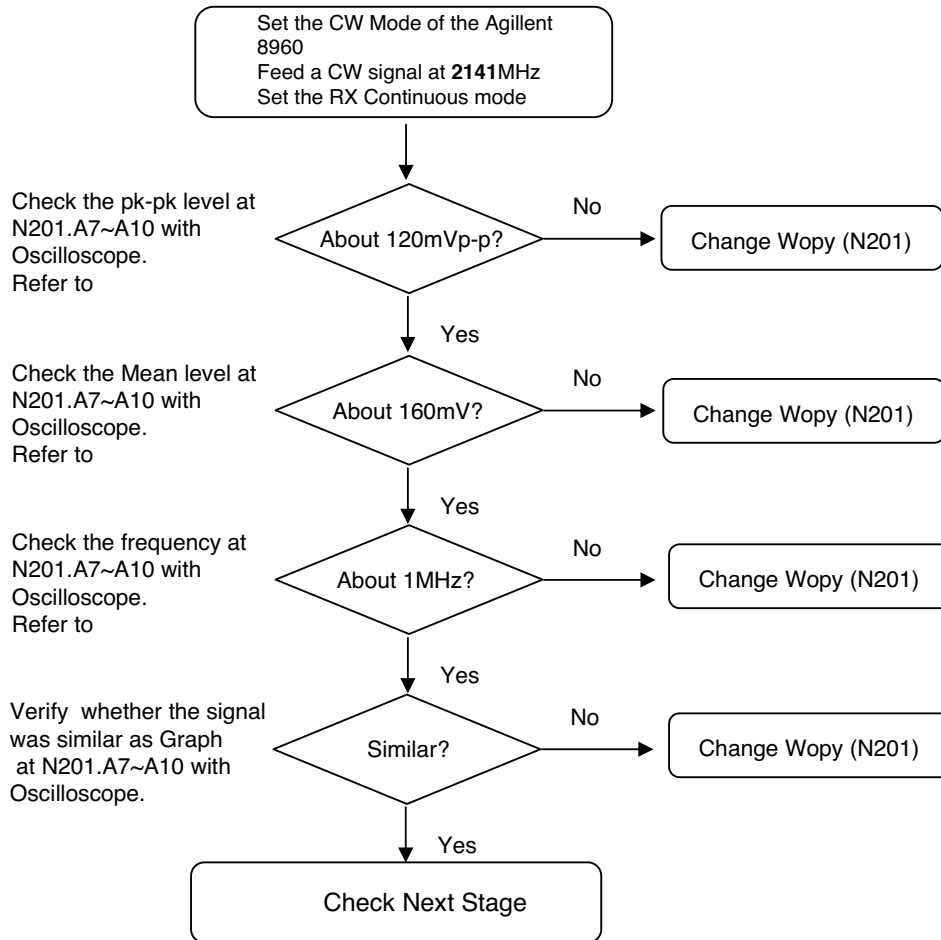
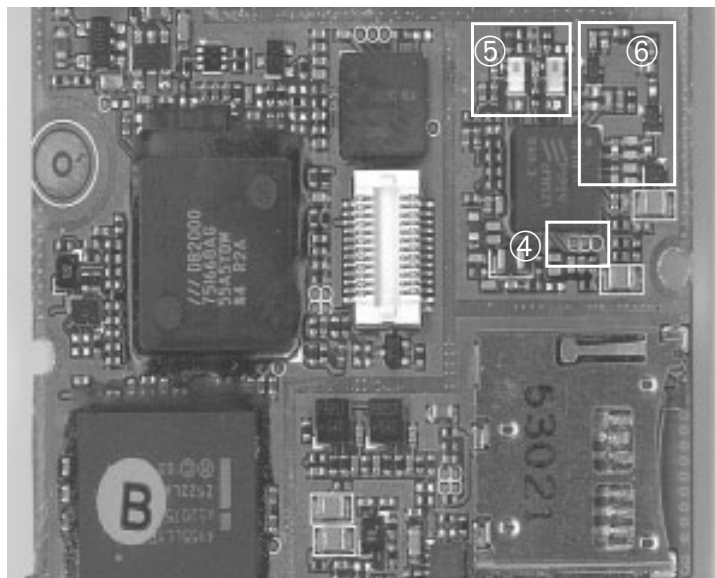
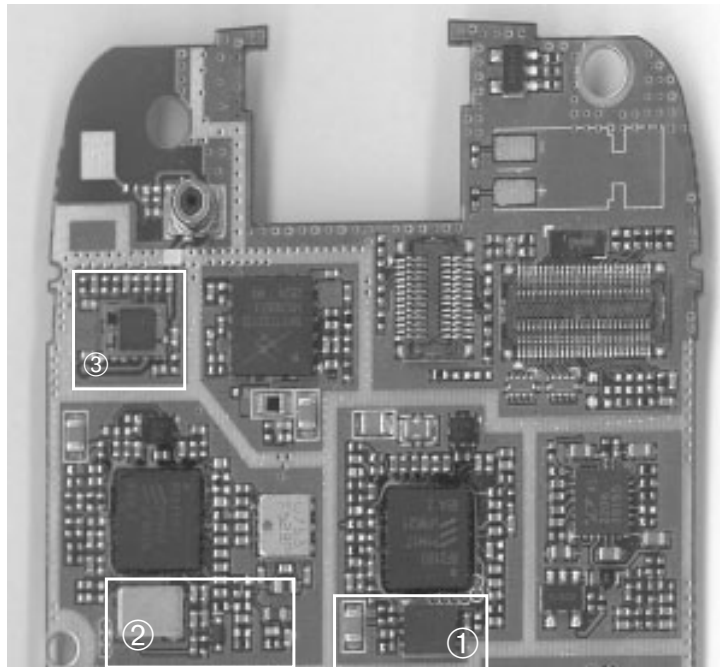
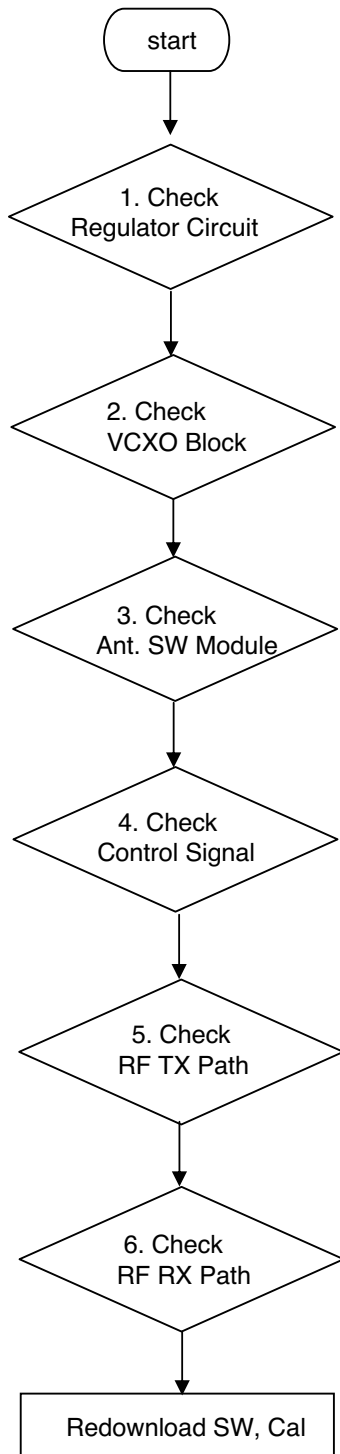


Figure 4-20-18. RX I, Q signal



4. TROUBLE SHOOTING

4.21 Checking GSM Block



4.21.1 Checking Regulator Circuit

Refer to 4.16 Checking Power Source block

IF you already check this point while checking power source block , You can skip this test.

4.21.2 Checking VCXO Block

Refer to 4.17 Checking VCXO block

IF you already check this point while checking VCXO block , You can skip this test.

4.21.3 Checking Ant. SW Module

Refer to 4.18 Checking Ant. SW Module

IF you already check this point while checking Ant. SW module , You can skip this test.

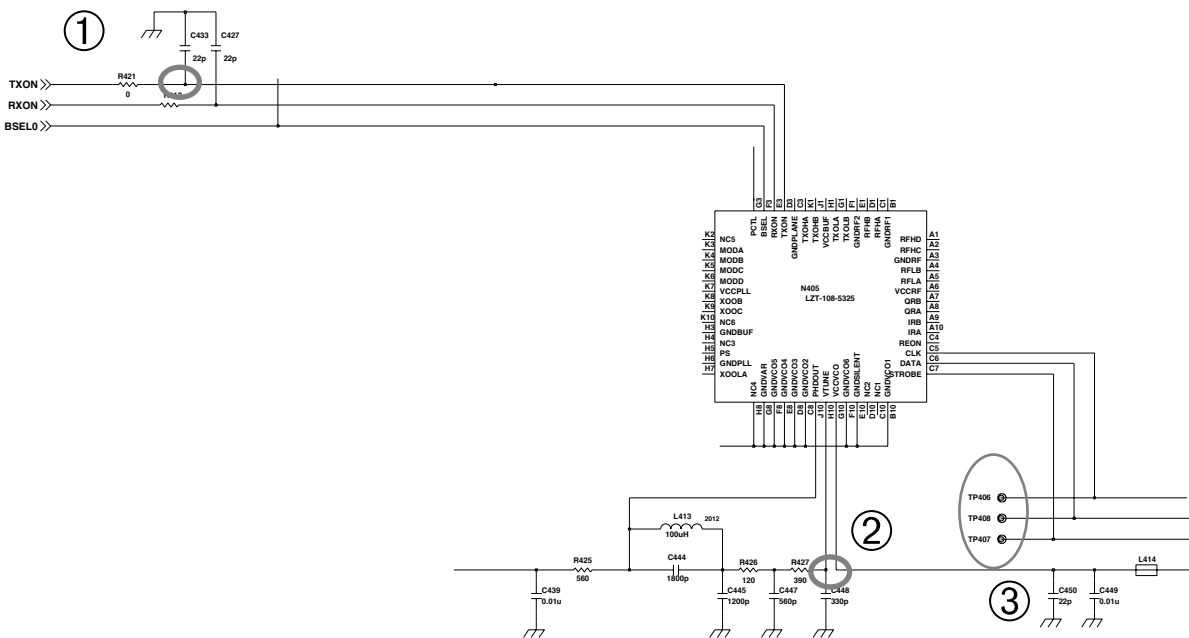
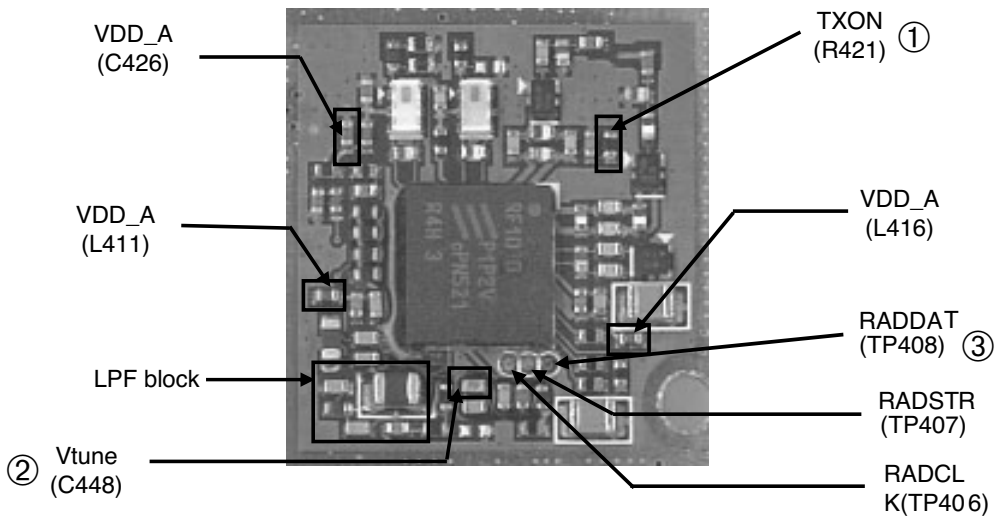
4. TROUBLE SHOOTING

4.21.4 Checking Control Signal

Test Program Script

MODE=0

SWTX=1,64,7,1024,1



4. TROUBLE SHOOTING

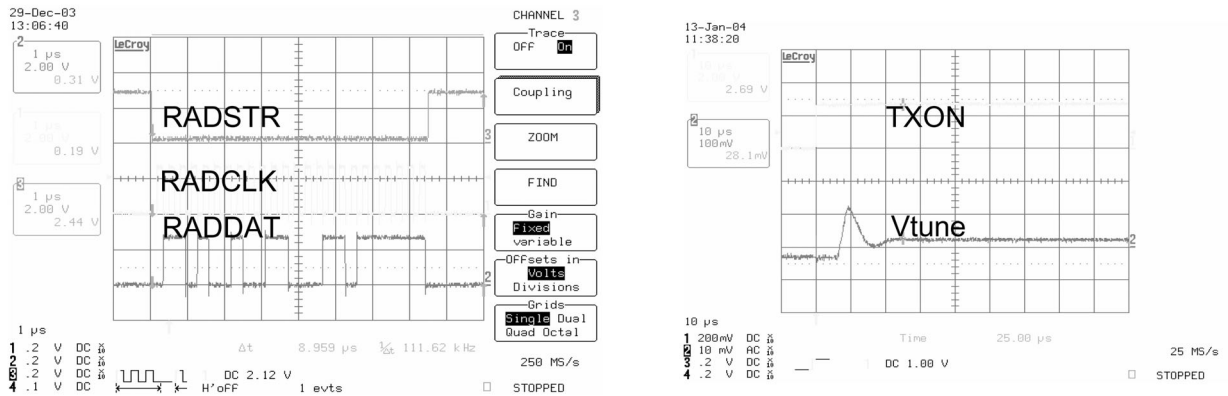
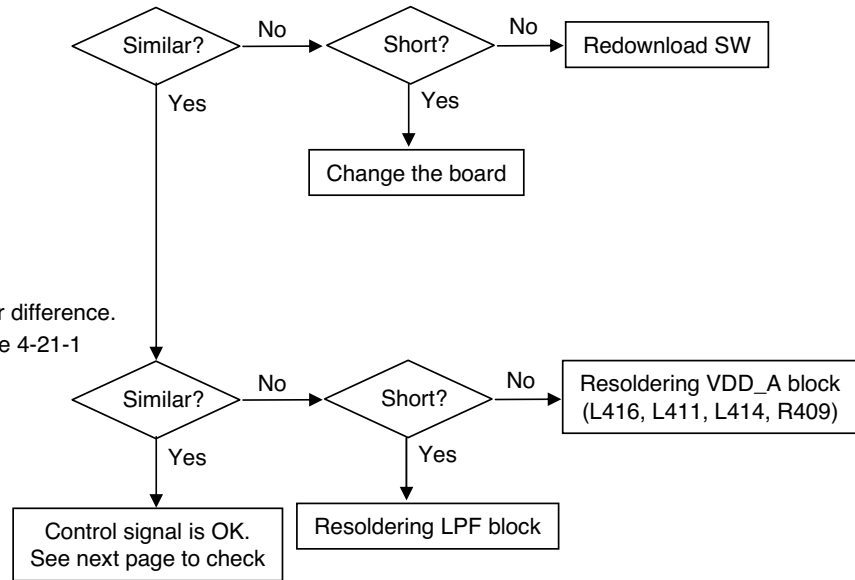


Figure 4-21-1. GSM RF Control signal

Check TP406,TP408,TP407.
 Check if there is any Major difference.
 Refer to left side of Figure 4-21-1



Check R421,C448.
 Check if there is any Major difference.
 Refer to right side of Figure 4-21-1

4. TROUBLE SHOOTING

4.21.5 Checking RF Tx Path

A. GSM Tx path Level

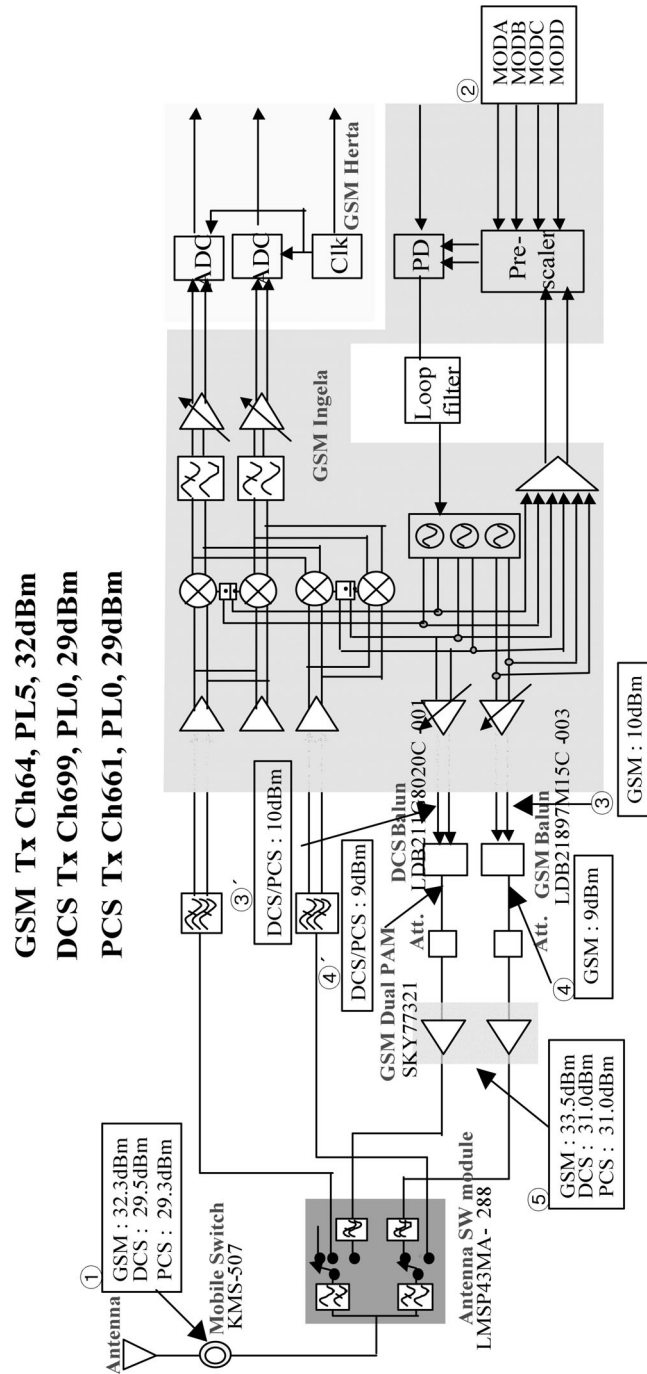


Figure 4-21-2. GSM/DCS/PCS Tx Path Level

4. TROUBLE SHOOTING

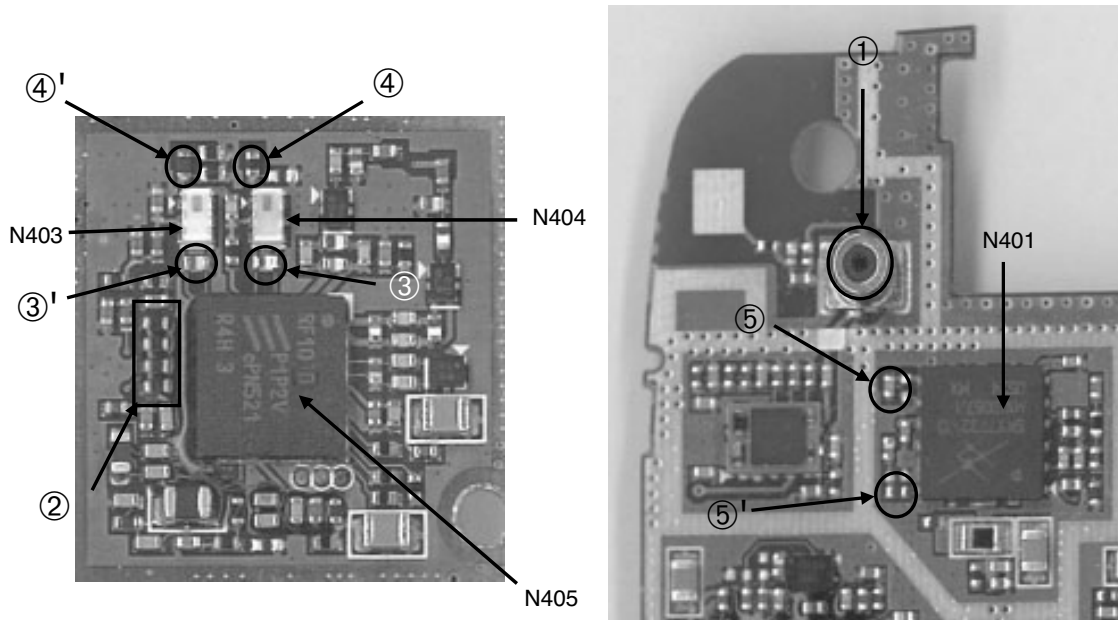
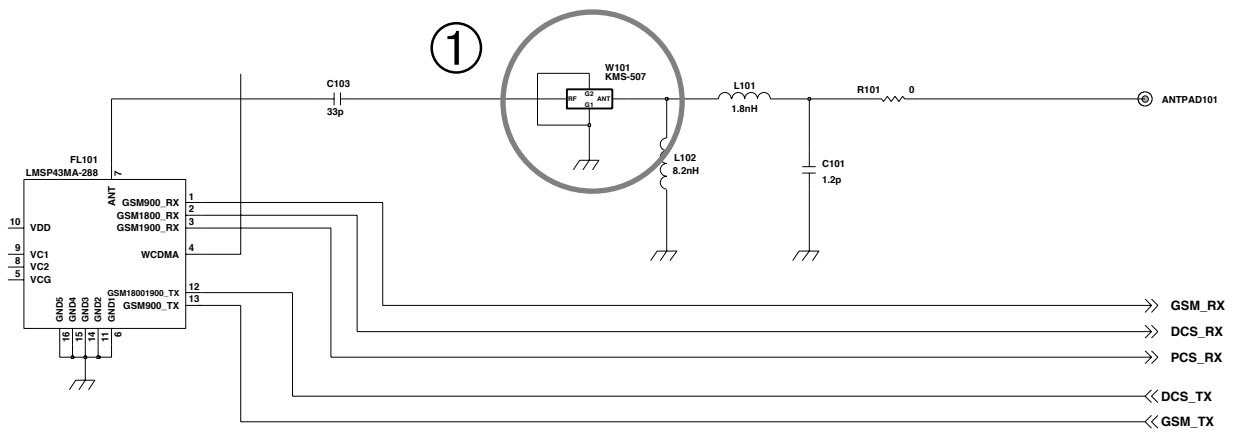


Figure 4-21-3. Test Point of GSM/DCS/PCS Tx Path



4. TROUBLE SHOOTING

B. GSM Tx Output Level Check

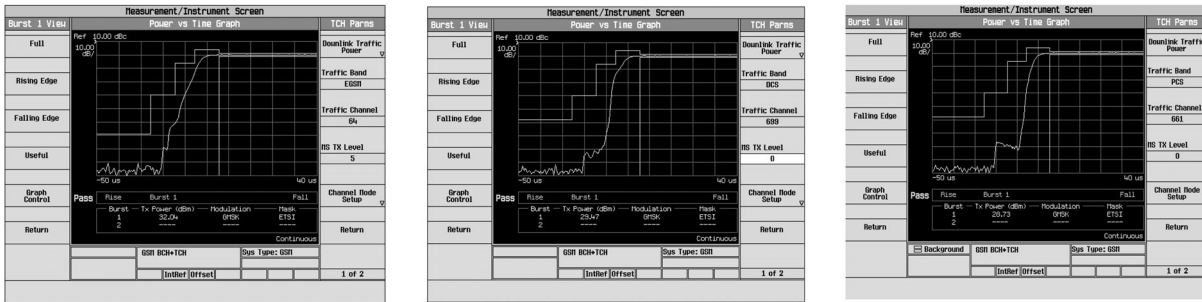


Figure 4-21-4. GSM/DCS/PCS Tx Level at ①

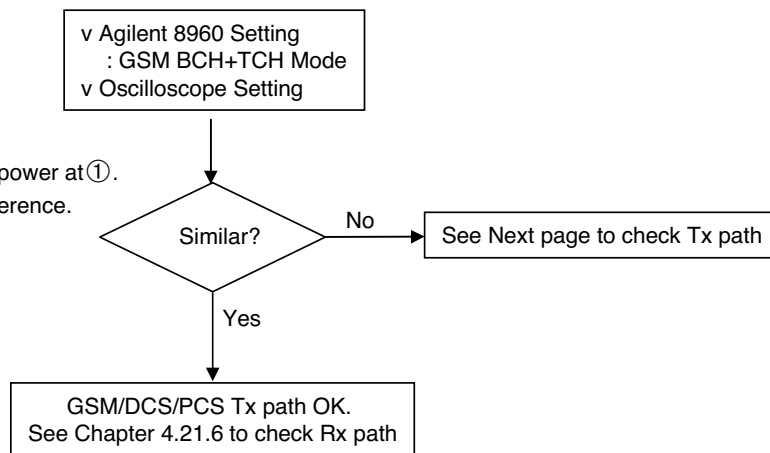
Test Program Script

1. GSM Tx
MODE=0
SWTX=1,64,5,1024,1

2. DCS Tx
MODE=2
SWTX=1,699,0,1024,1

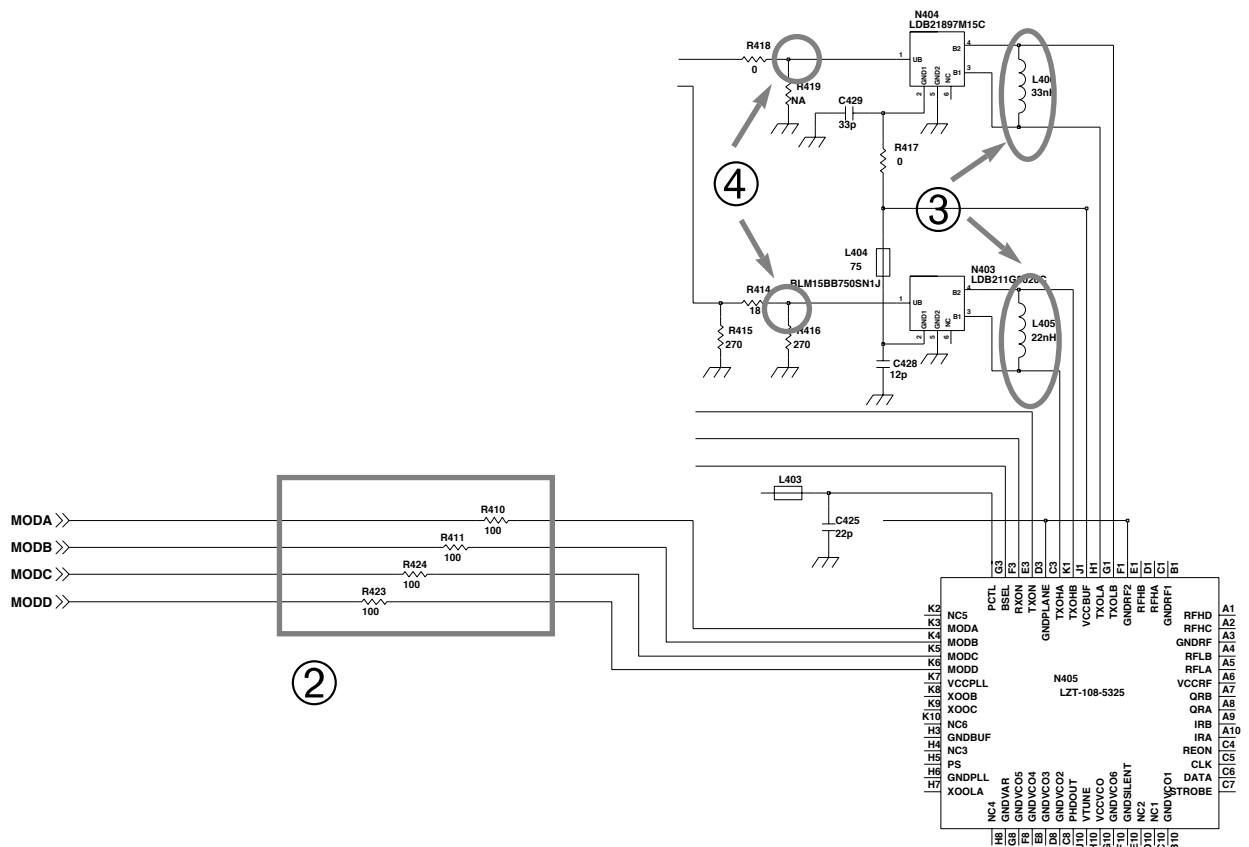
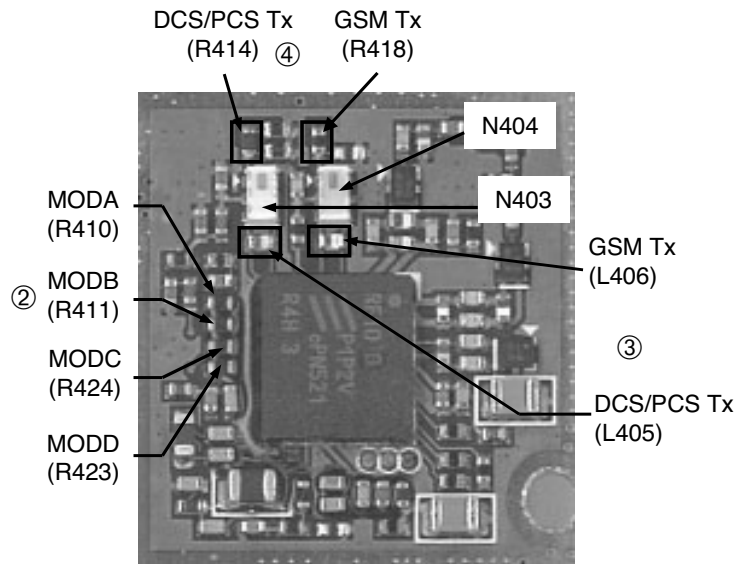
3. PCS Tx
MODE=1
SWTX=1,661,0,1024,1

Check GSM/DCS/PCS output power at ①.
Check if there is any Major difference.
Refer to Figure 4-21-4.
GSM>32dBm
DCS>29dBm
PCS>29dBm



4. TROUBLE SHOOTING

C. GSM RF Transceiver IN/OUT Signal Check



4. TROUBLE SHOOTING

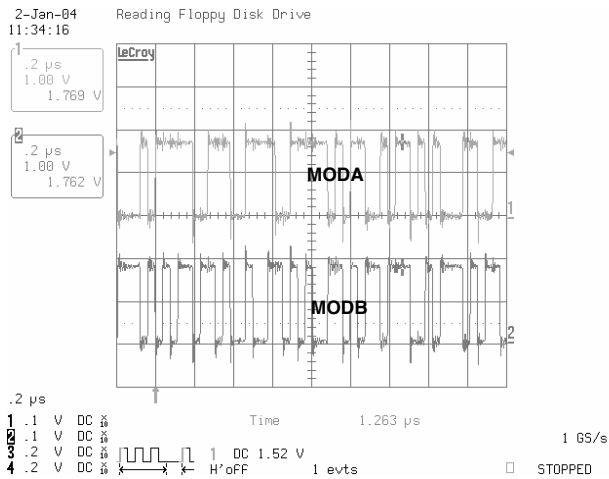
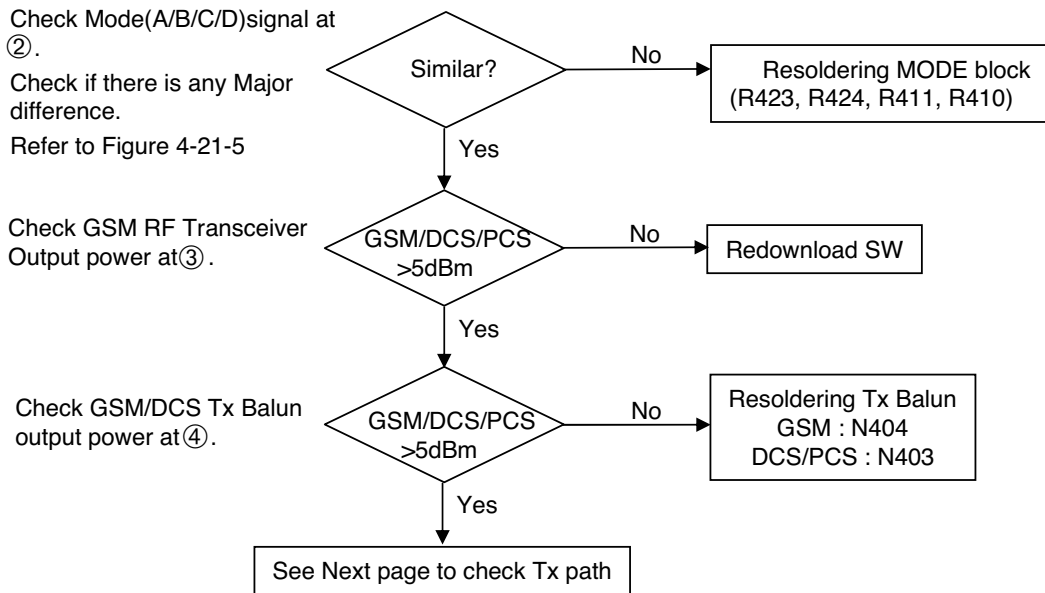
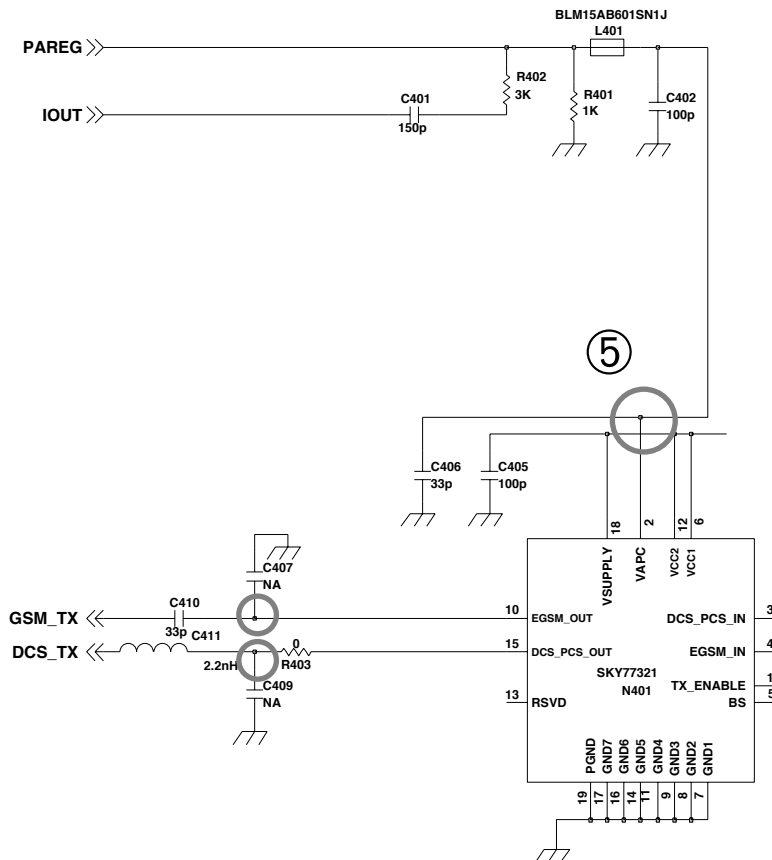
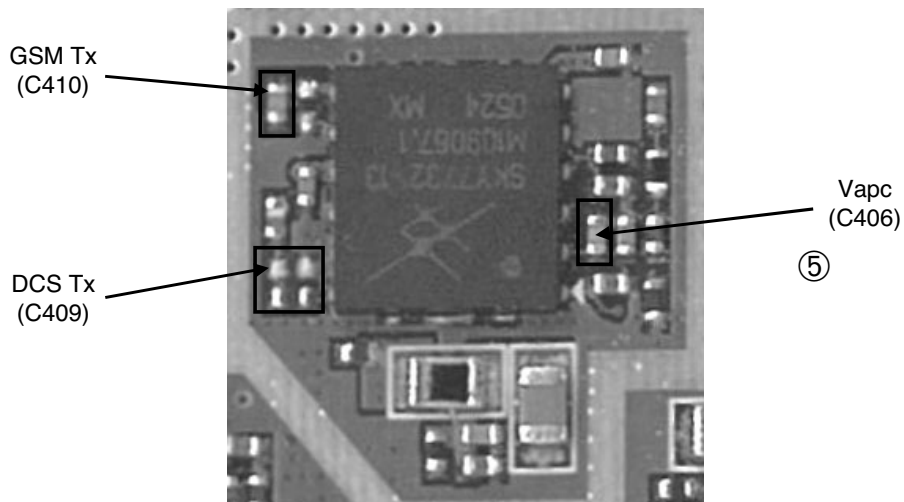


Figure 4-21-5. GSM/DCS/PCS Tx MODE signal



4. TROUBLE SHOOTING

D. GSM PAM Check



4. TROUBLE SHOOTING

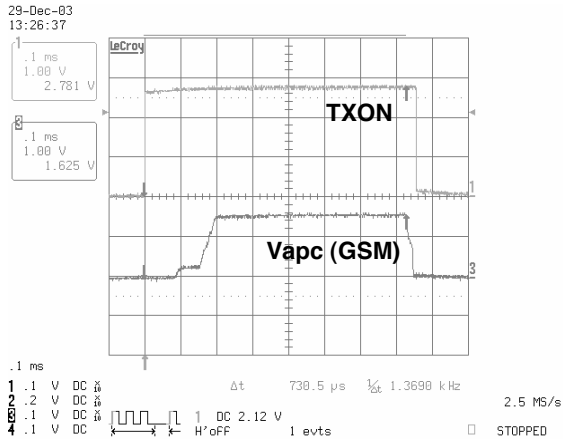


Figure 4-21-6. GSM Tx control signal

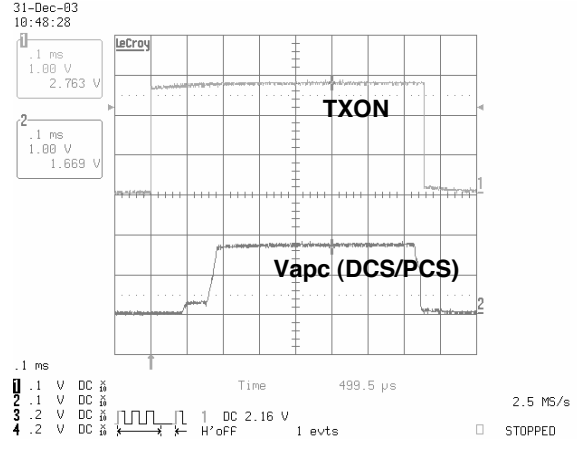
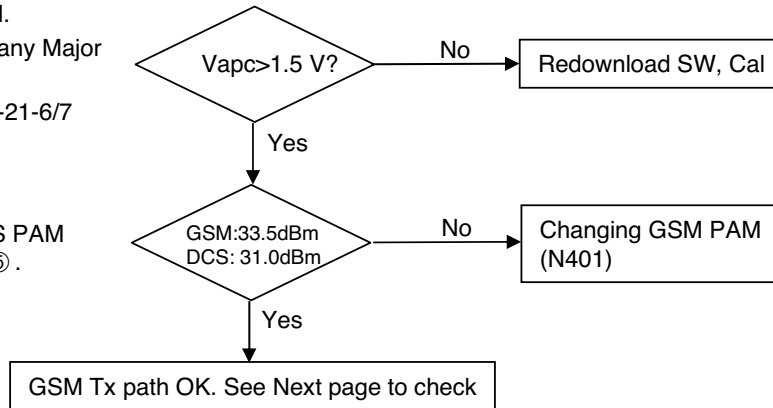


Figure 4-21-7. DCS/PCS Tx control signal

Check Vapc level.
 Check if there is any Major difference.
 Refer to Graph 4-21-6/7

Check GSM/DCS PAM output power at ⑤.



4.21.5 Checking RF Tx Path

A. GSM Tx path Level

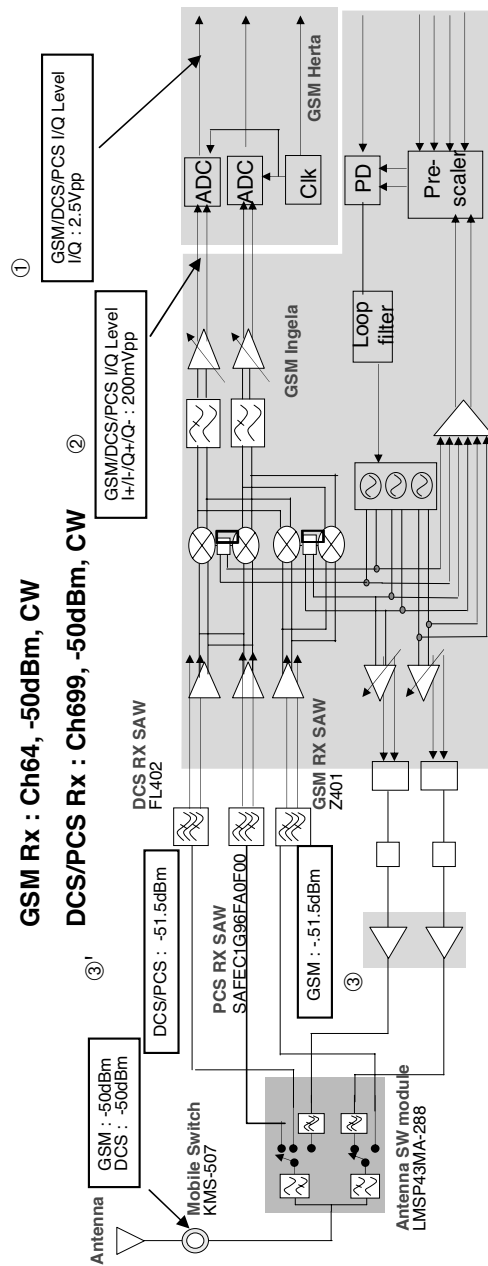
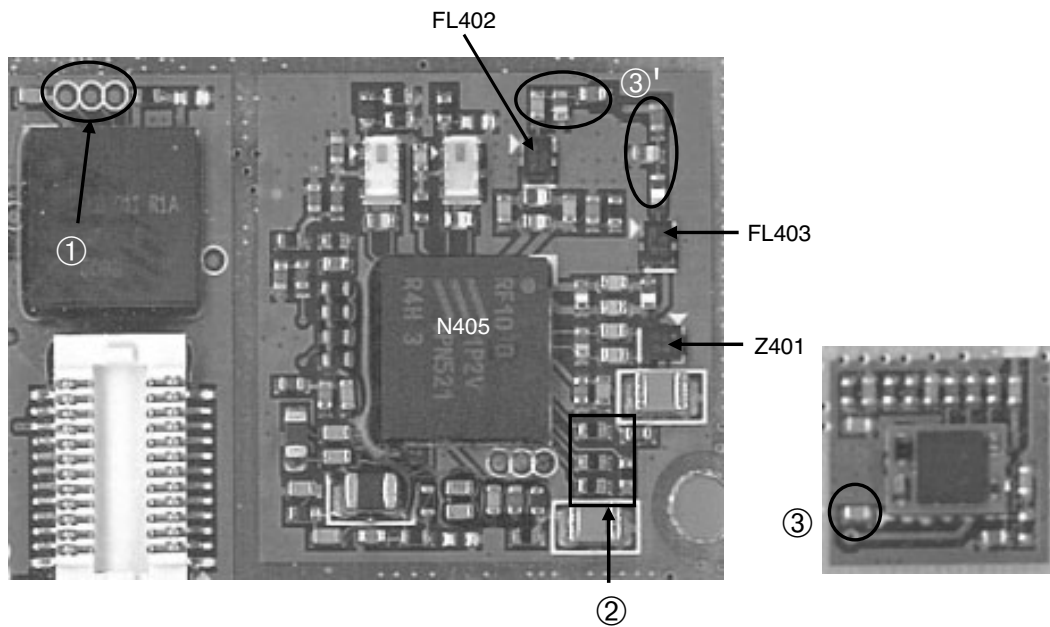


Figure 4-21-2. GSM/DCS/PCS Tx Path Level

4. TROUBLE SHOOTING



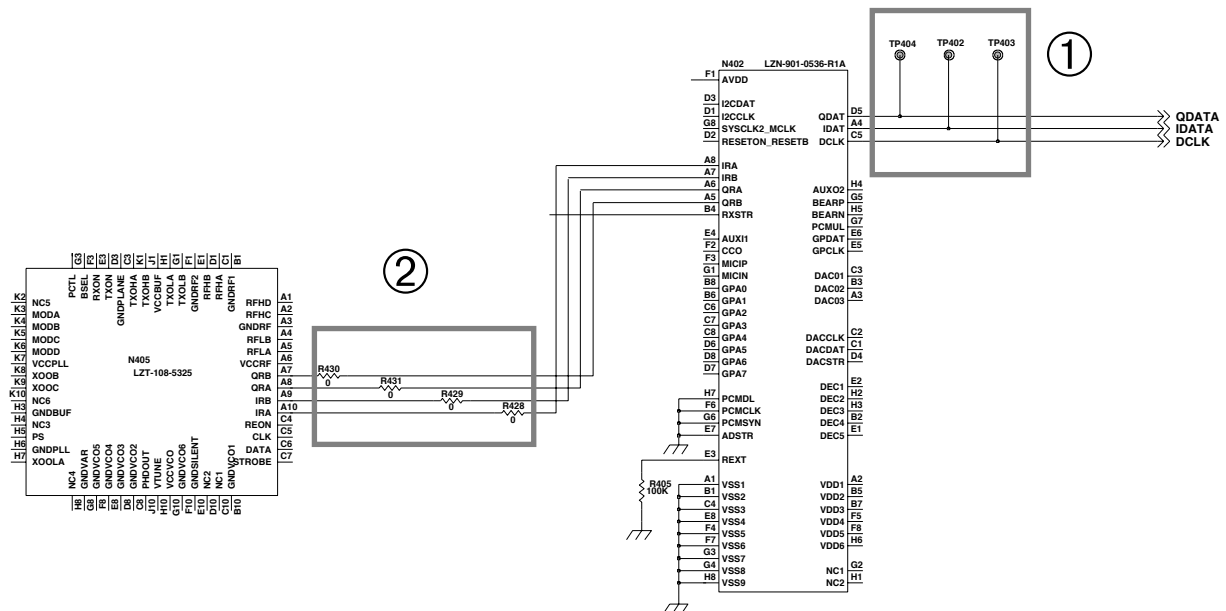
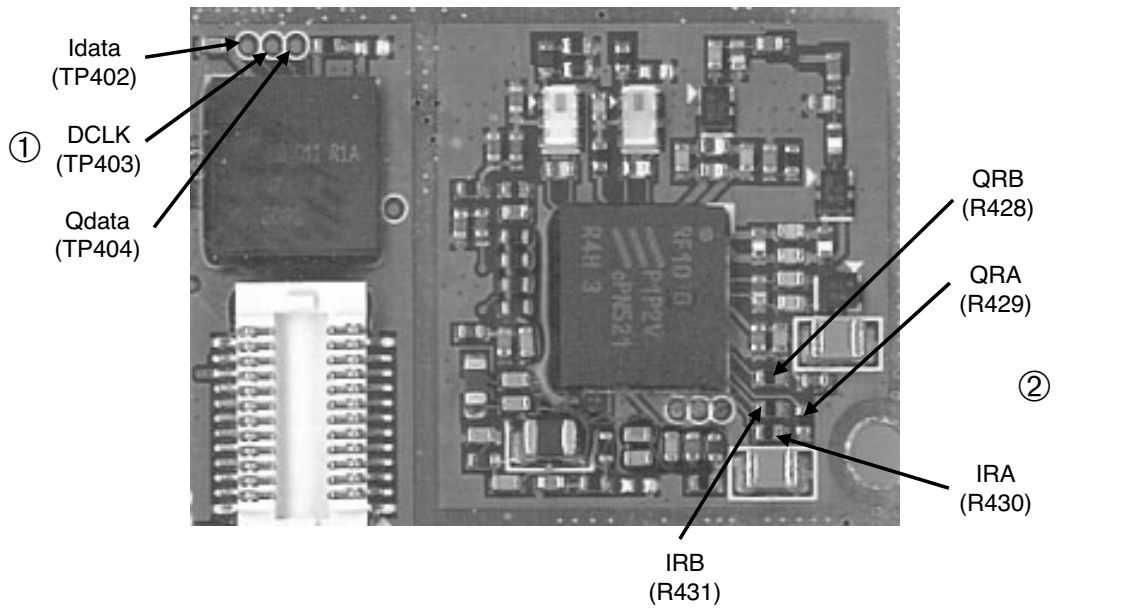
Test Program Script

- | | |
|--------------------|---------------------|
| 1. GSM Tx | 2. DCS/PCS Tx |
| MODE=0 | MODE=2(DCS),1(PCS) |
| SWTX=1,64,5,1024,1 | SWTX=1,699,0,1024,1 |

v Agilent 8960 Setting
CW Mode
GSM : -50dBm@Ch65(948MHz)
DCS : -50dBm@Ch700(1842.8MHz)
PCS : -50dBm@ch700(1889.0MHz)
v Oscilloscope Setting

4. TROUBLE SHOOTING

B. GSM I/Q Signal Check



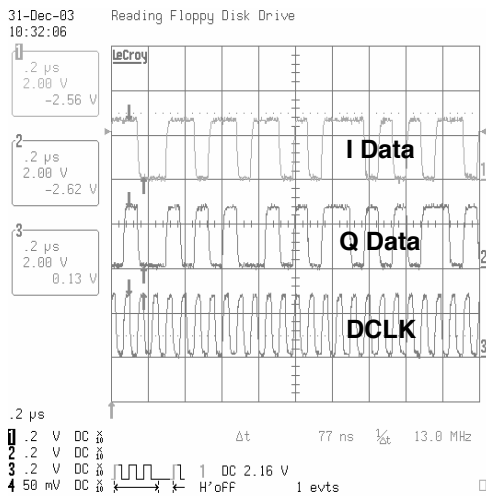


Figure 4-21-9. Herta IQ data and DCLK

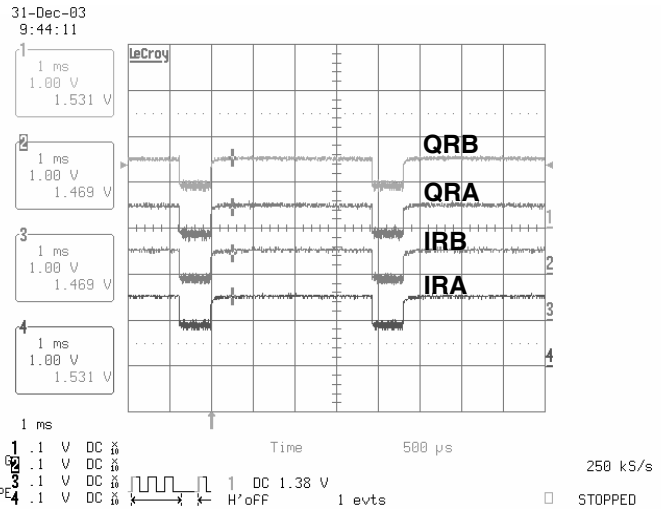


Figure 4-21-10. Ingela IQ signal

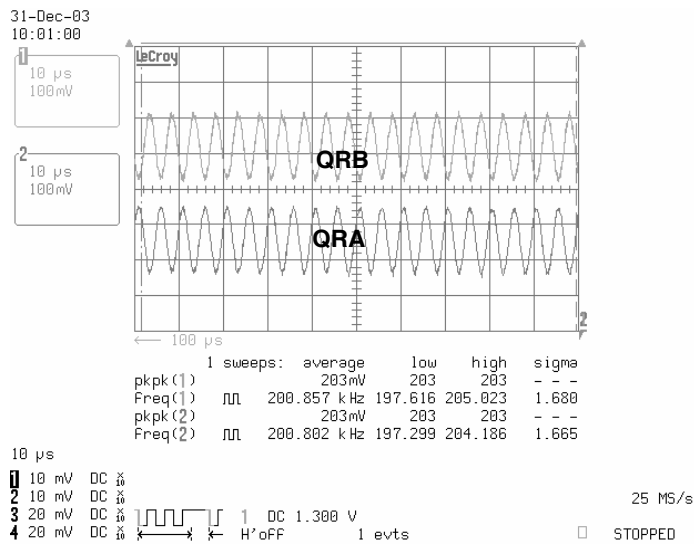
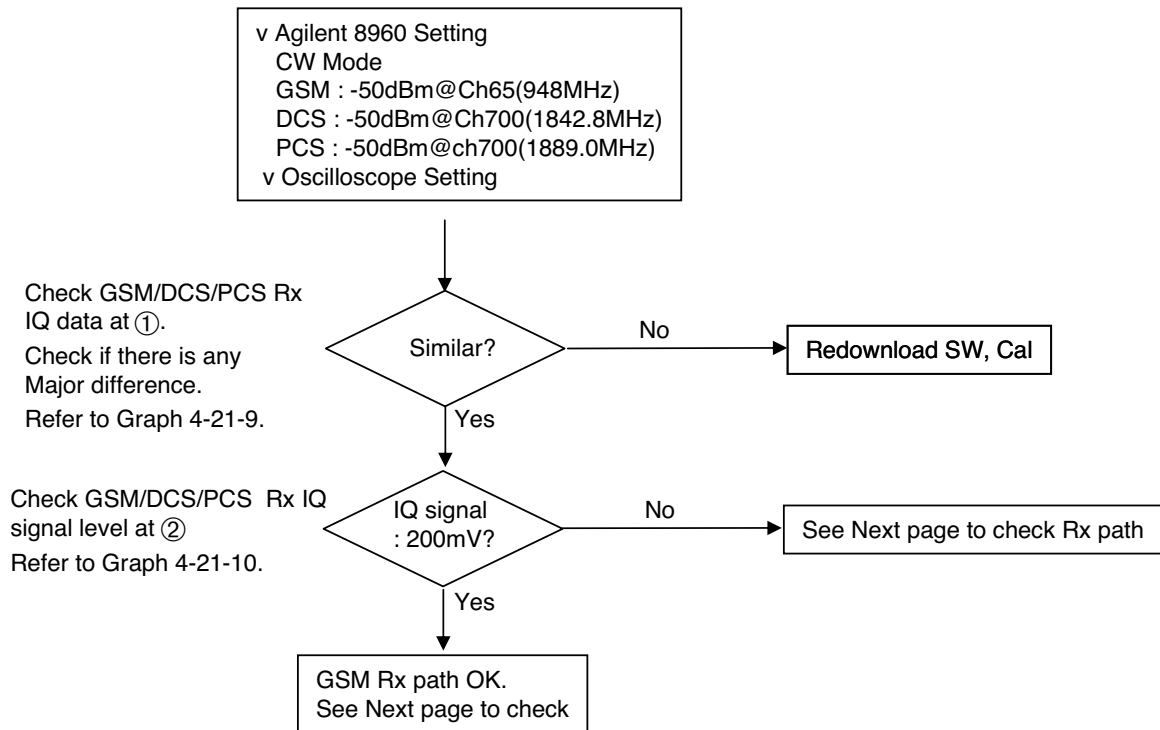


Figure 4-21-11. Ingela IQ signal



C. GSM RF Level Check

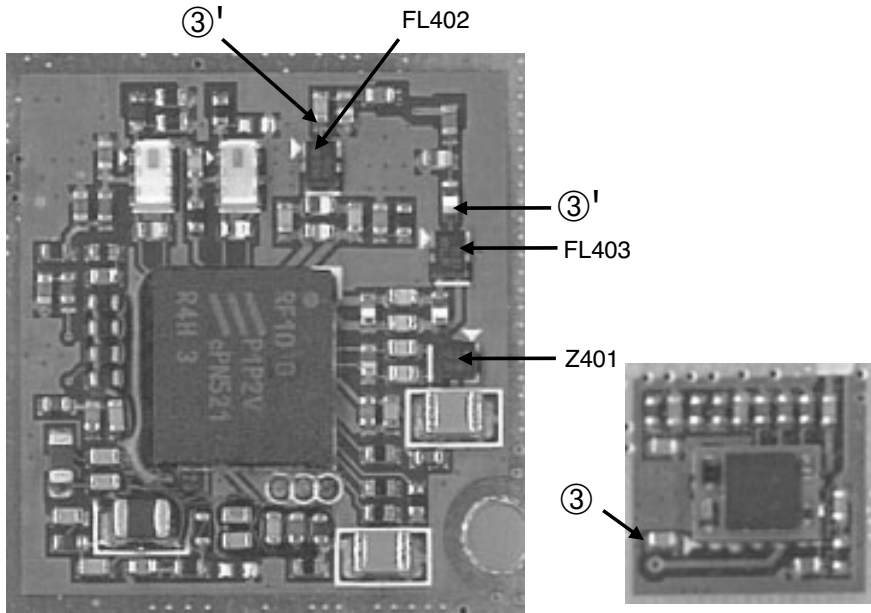
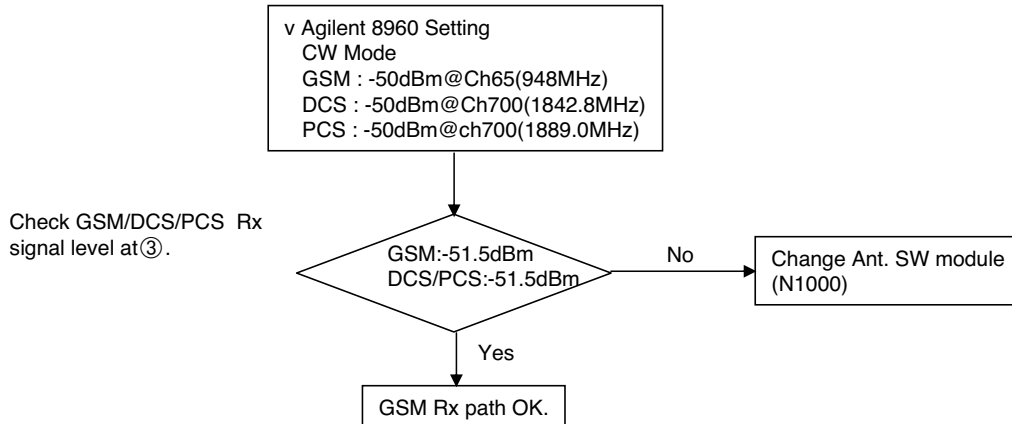
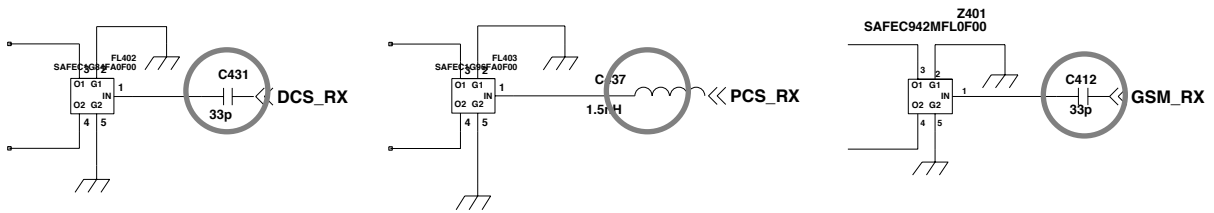
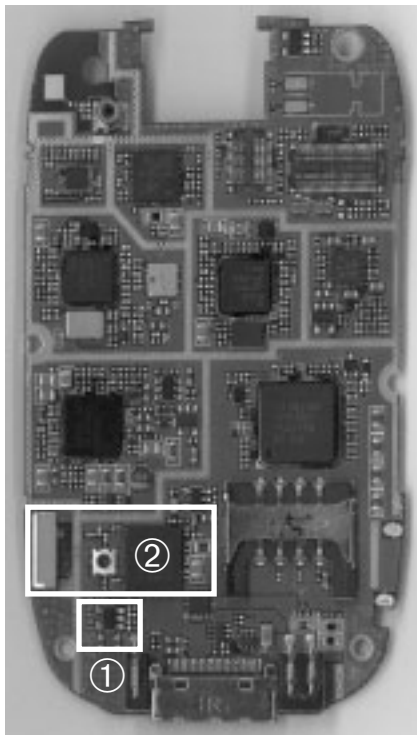


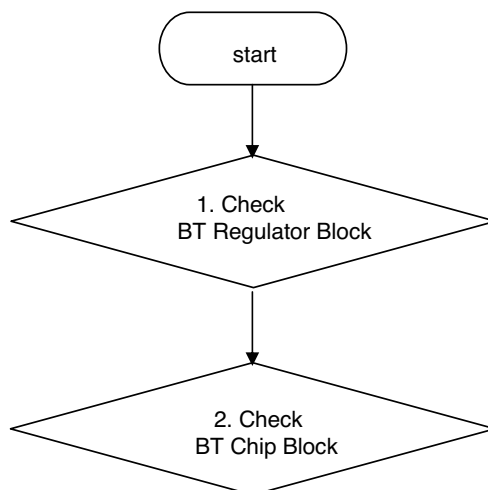
Figure 4-21-12. GSM/DCS/PCS Rx path



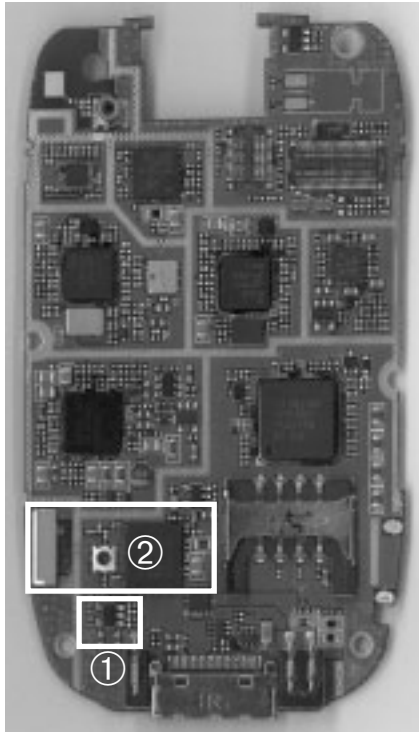
4.22 Checking Bluetooth Block



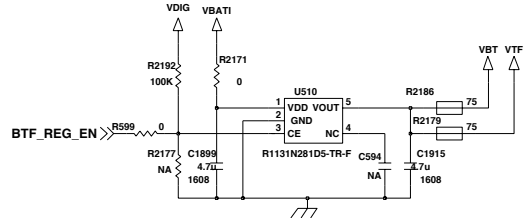
<Bottom view>



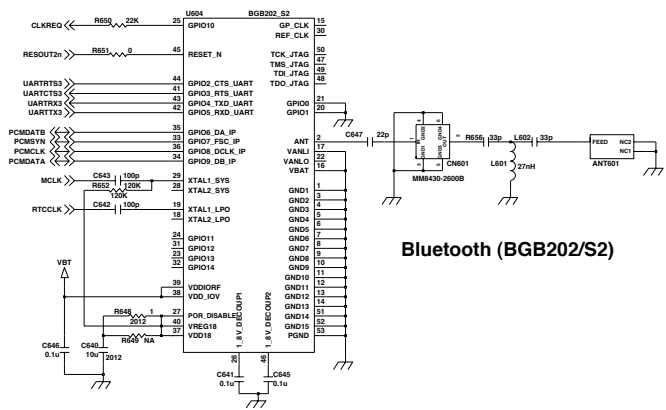
**** BT - Bluetooth**



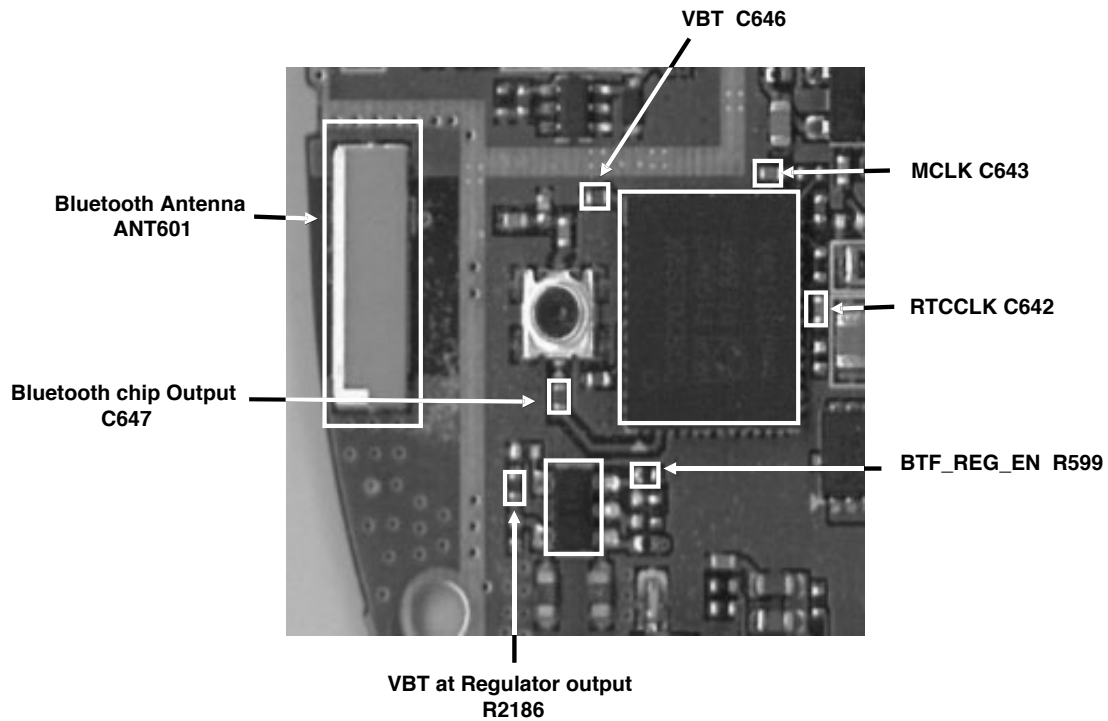
<Bottom view>



BT and T-Flash Regulator-2.85V

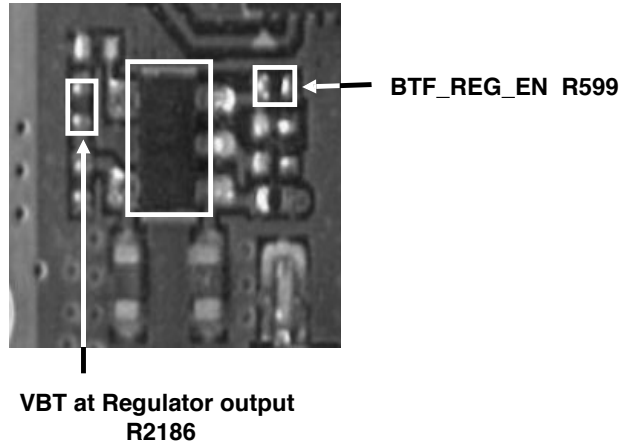


Bluetooth (BGB202/S2)



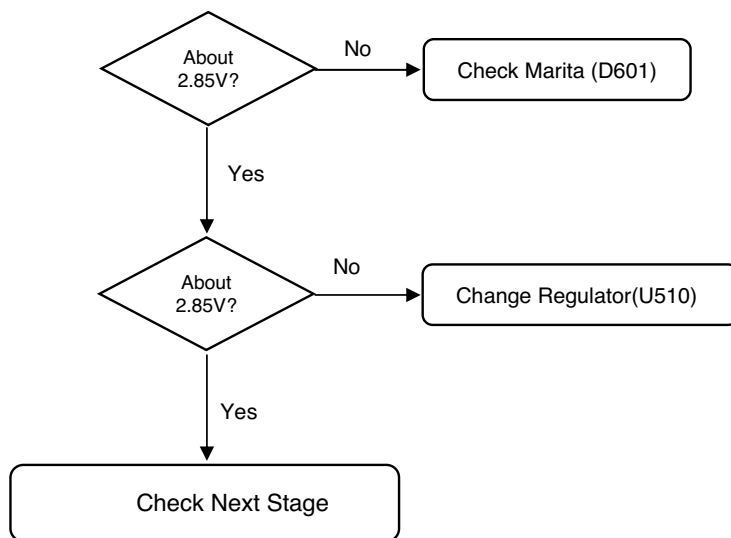
Checking Bluetooth Regulator Block

TP Command
 -pctr = 3,4,1
 -pdin = 3,4
 -pdou = 3,4,1
 -brts =1
 -ltcx = 3
 -dacc =0,2 responded value
 -Btfa=1,1
 -Btfa=1,2

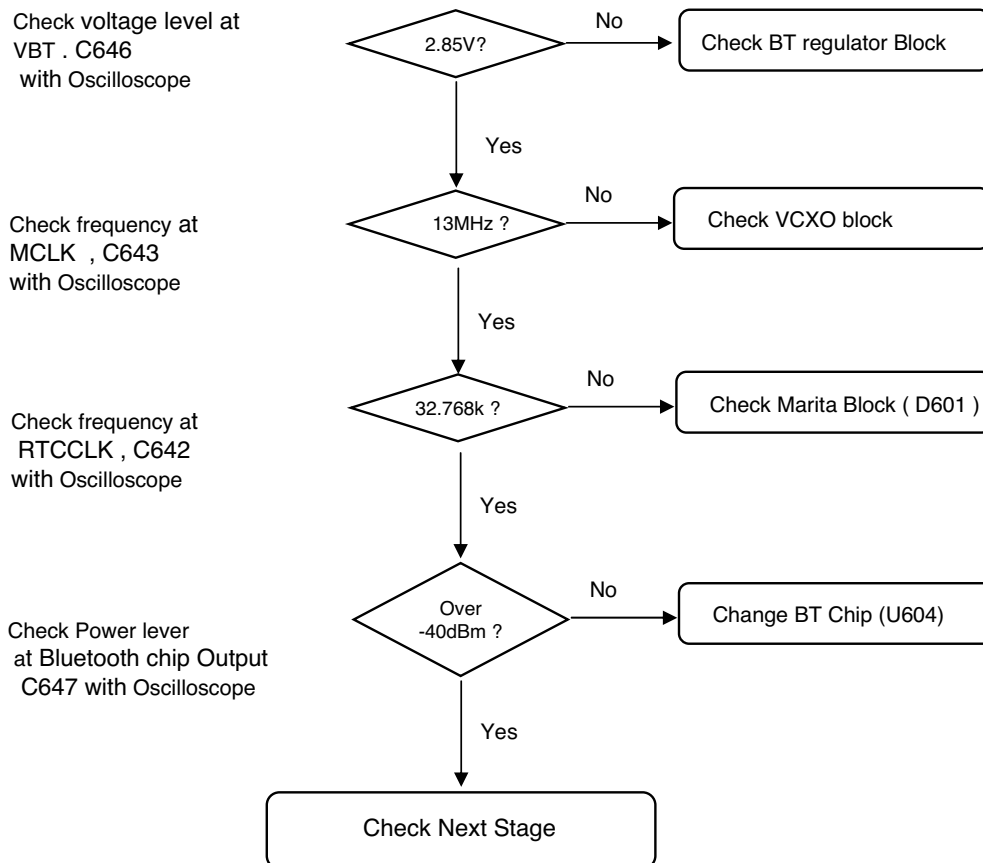
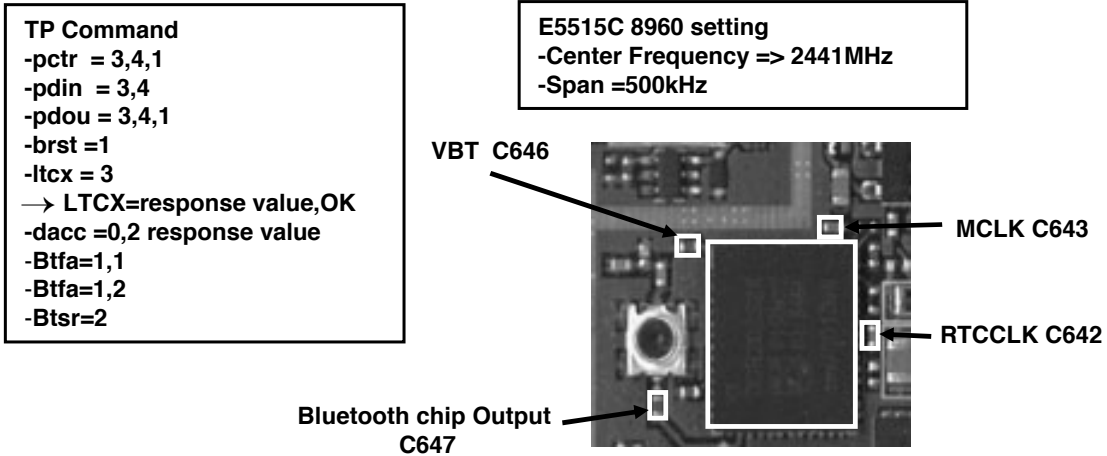


Check voltage level at
 BTF_REG_EN . R599
 with Oscilloscope

Check voltage level
 At VBT.R2186
 with Oscilloscope



Checking Bluetooth Block



5. BLOCK DIAGRAM

5.1 GSM & WCDMA RF Block

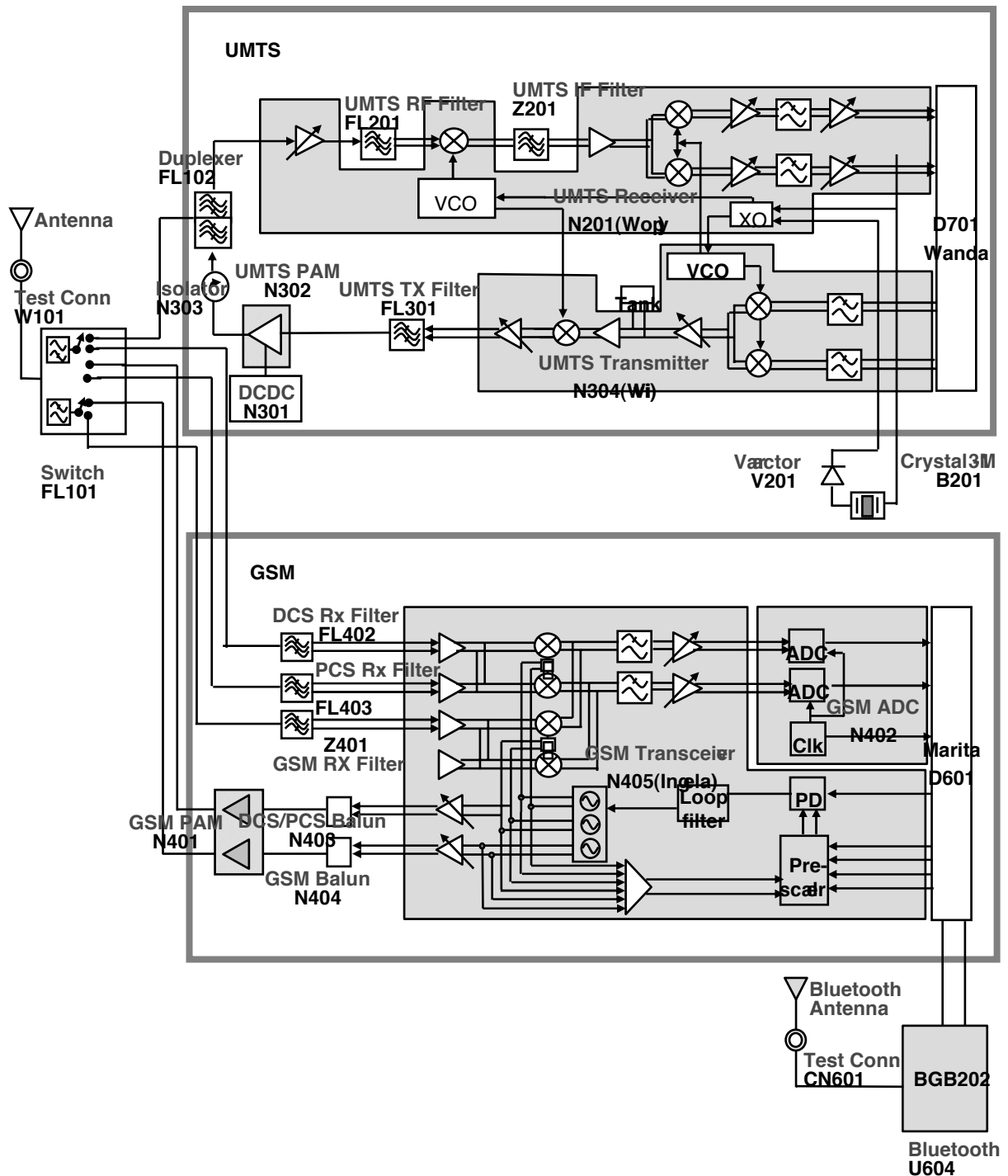


Figure 5-1-1. RF Block Diagram

5. BLOCK DIAGRAM

5. BLOCK DIAGRAM

Block	Ref. Name	Part Name	Function	Comment
Common	FL101	LMSP43MA-288	Switch	Band select
	W101	KMS-507	Test Connector	Calibration, etc
	B201	TSX-8A_13MHz	Crystal	Reference -13M
WCDMA	FL102	DFYY61G95LBNBC-TT1	Duplexer	TRX
	N201	LZT-108-5323	Receiver	RX
	FL201	SAFEH2G14FA0F00R00	RX RF Filter	RX
	Z201	TMXU753	RX IF Filter	RX
	N301	MAX1820ZEBC	DC/DC	TX
	N302	RF9266	PAM	TX
	N303	ESMI-3EAL1.95G01-T	Isolator	TX
	N304	LZT-108-5322	Transmitter	TX
	FL301	SAFEH1G95FL0F00R00	TX RF Filter	TX
	D701	ROP-101-3033_1	Analog Baseband	TRX
GSM	FL402	SAFEB1G84FA0F00	DCS RX Filter	Direct Conversion
	Z401	SAFEB942MFL0F00	GSM RX Filter	Direct Conversion
	FL403	SAFEB1G96FA0F00	PCS RX Filter	Direct Conversion
	N405	LZT-108-5325	Transceiver	TRX
	N401	SKY77321	PAM	GSM/DCS/PCS Tri
	N404	LDB21897M15C-003	GSM Balun	TX
	N403	LDB211G8020C-001	DCS/PCS Balun	TX
	D601	ROP-101-3035-_1	Modem	
Bluetooth	U604	BGB202_S2	Bluetooth	

Table 5-1-1. RF Part Component List

6. DOWNLOAD

6.1 The Purpose of Downloading Software

- To make a phone operate at the first manufacturing
 - A phone = Hardware + Software
 - A phone cannot operate with hardware alone.
 - The hardware with the suitable software can operate properly.
- To upgrade the software of the phone
 - The software of the phone may be changed to enhance the performance of the phone.
 - The older version software of the phone can be replaced to the newer version.
- Download Tools
 - FlashRW : Download tool for U8XX0 software

6.2 Download Environment Setup

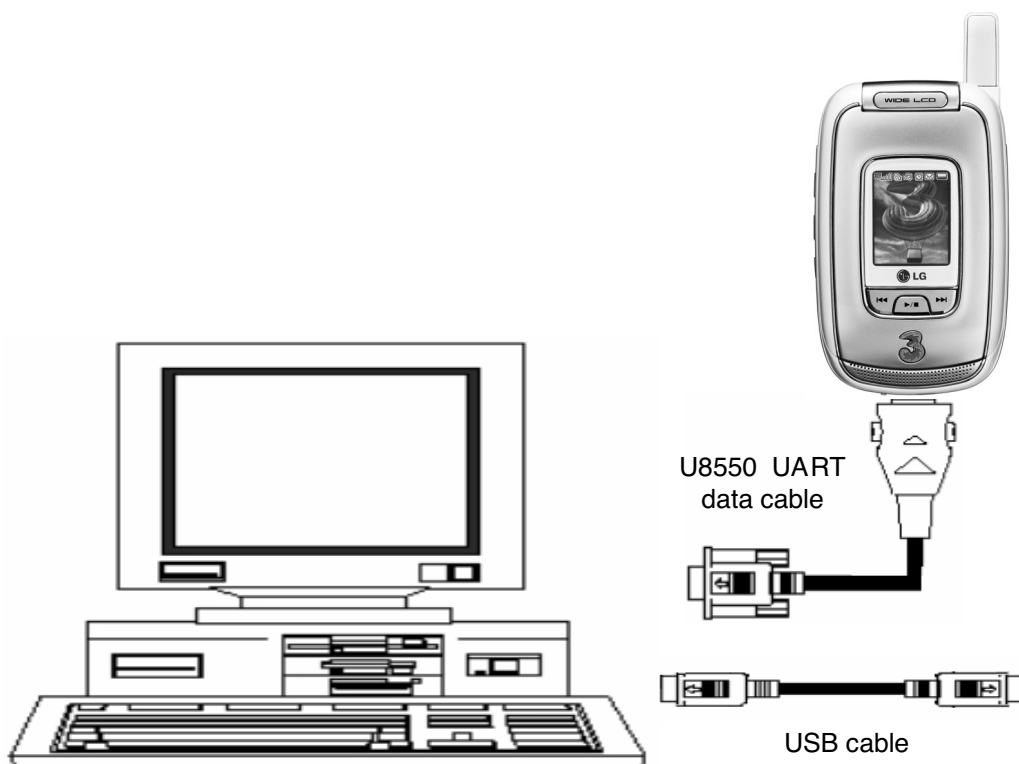


Figure 6-2-1. U8XX0 Download can be done via UART & USB

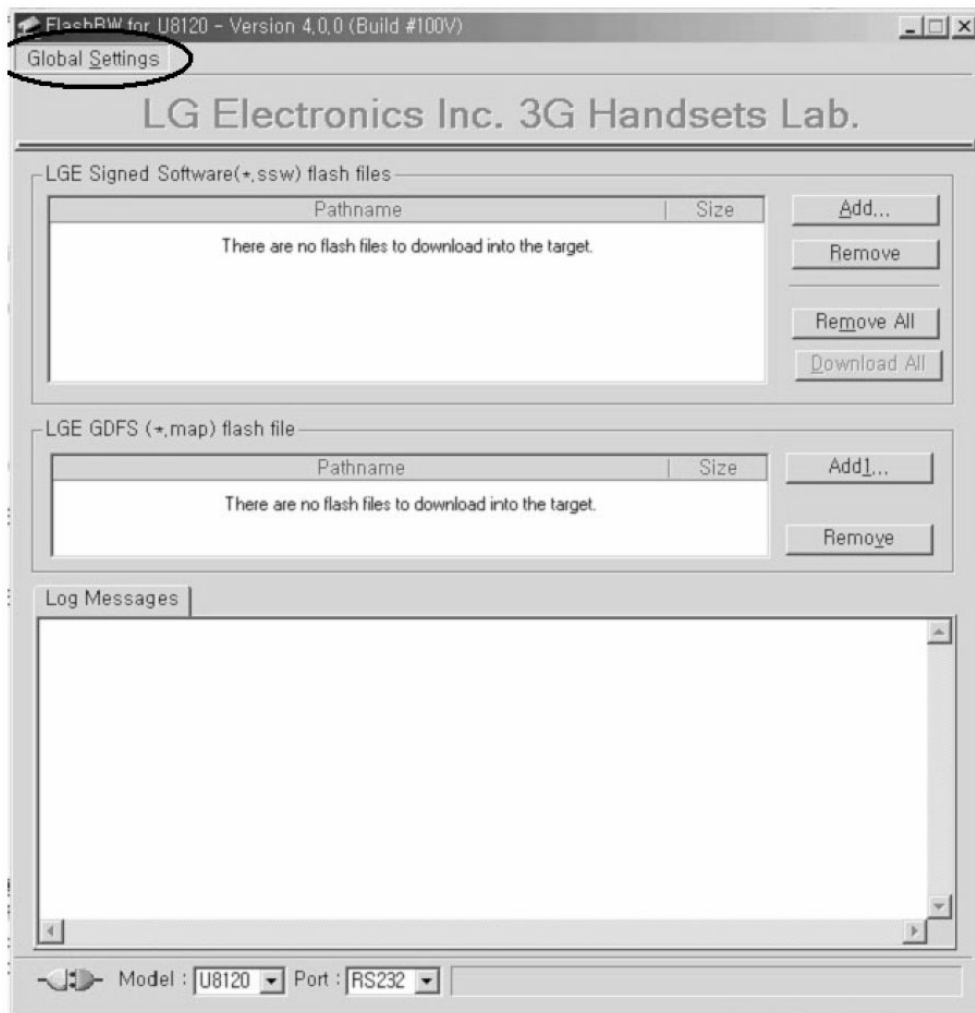
6. DOWNLOAD

6. DOWNLOAD

6.3 U8XXX Download

6.3.1. U8XXX Download(1) - FlashRW configuration

- A. Execute FlashRW_V200_Red.exe
- B. Press the “Global Settings” on the top menu to configure FlashRW environment.



6. DOWNLOAD

C. Select Loader File for Product.

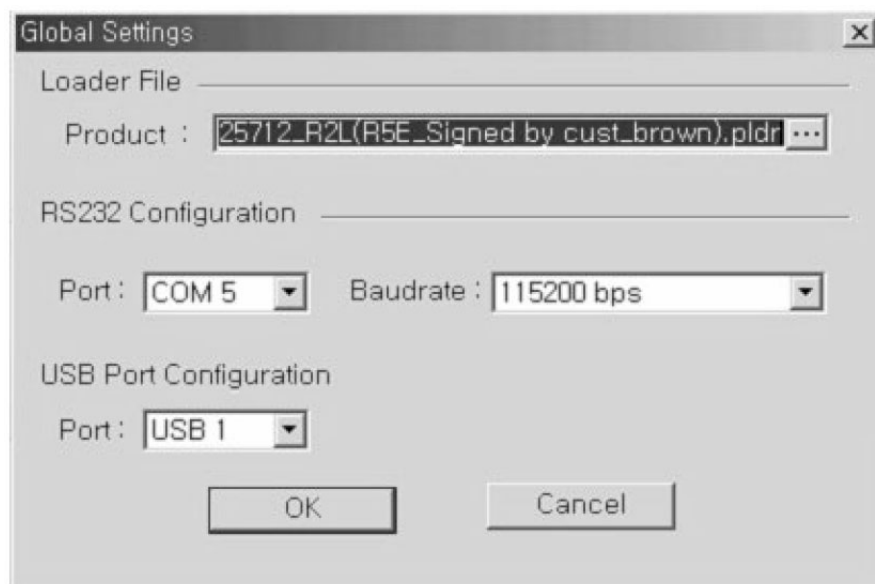
You can use browse button to select Loader File.

You must select only cxc1325414_R3V_u8550R. fldr for U8550.

Loader File is provided with FlashRW.

D. Select Port configurations for both RS232 Port and USB Port.

Baudrate should be 115200bps.



You have to do FlashRW configuration only at the first time of installation

6. DOWNLOAD

6.3.1. U8XXX Download(2) - Phone Model Selection

- A. Press Button for Model.
- B. Select Model U8120 for U8550.



6. DOWNLOAD

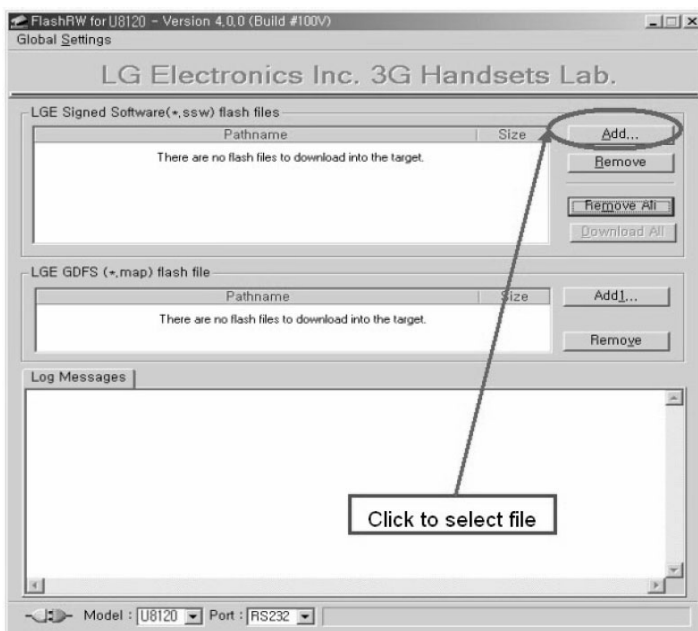
6.3.1. U8XXX Download(3) - Download file selection

A. 1. Press “Add” button to select LGE SSW files to download.

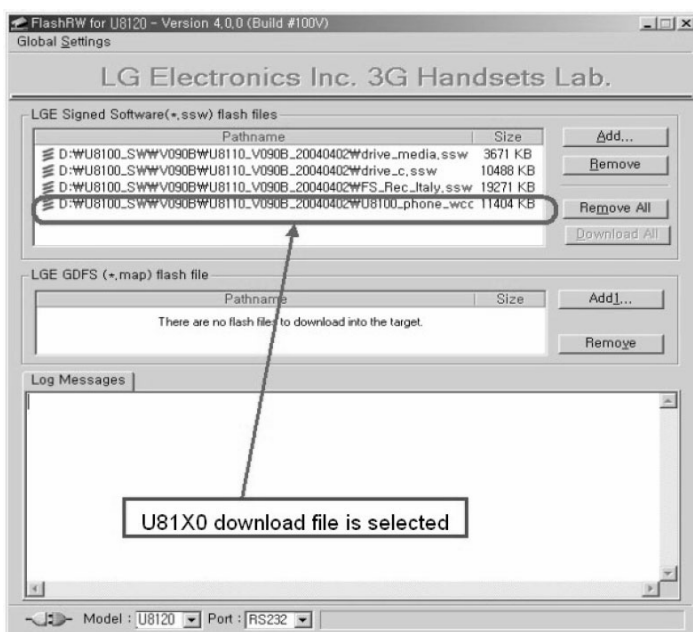
B. Don't Press “Add1” button to select LGE GDFS file to download.

If you download old released LGE GDFS file, The phone will break down.

This “Add1” button will be used for upgraded if needed. Only When LGE propose this action, you must press this button.




<Before Select>



<After Select>

6. DOWNLOAD

6.3.1. U8XXX Download(4) - Connect & Download

- Click on connector icon() to connect to the phone Check the Dialog Box that say "Please,switch on the target".
- Connect the phone to PC via Cable for Downloading. Phone should be turned off.
- Turn the phone on to connect to PC.



6.3.1. U8XXX Download(5) - USB Driver Install

A. If you use FlashRW Tool firstly, Error will happen because of USB Driver uninstalled.

You have to do FlashRW USB Driver Installation only at the first time of installation



6. DOWNLOAD

B. Push “the Next Button” in Found New Hardware Wizard

C. Select “Search for a suitable driver for my device” in Found New Hardware Wizard



6. DOWNLOAD

D. Select “Specify a location” in Found New Hardware Wizard

E. Push “the Browse Button” , and then select “USB driver Information file” This File is provided with FlashRW.



6. DOWNLOAD

F. Push “the Next Button” in Found New Hardware Wizard

G. Push “the Finish Button” in Found New Hardware Wizard

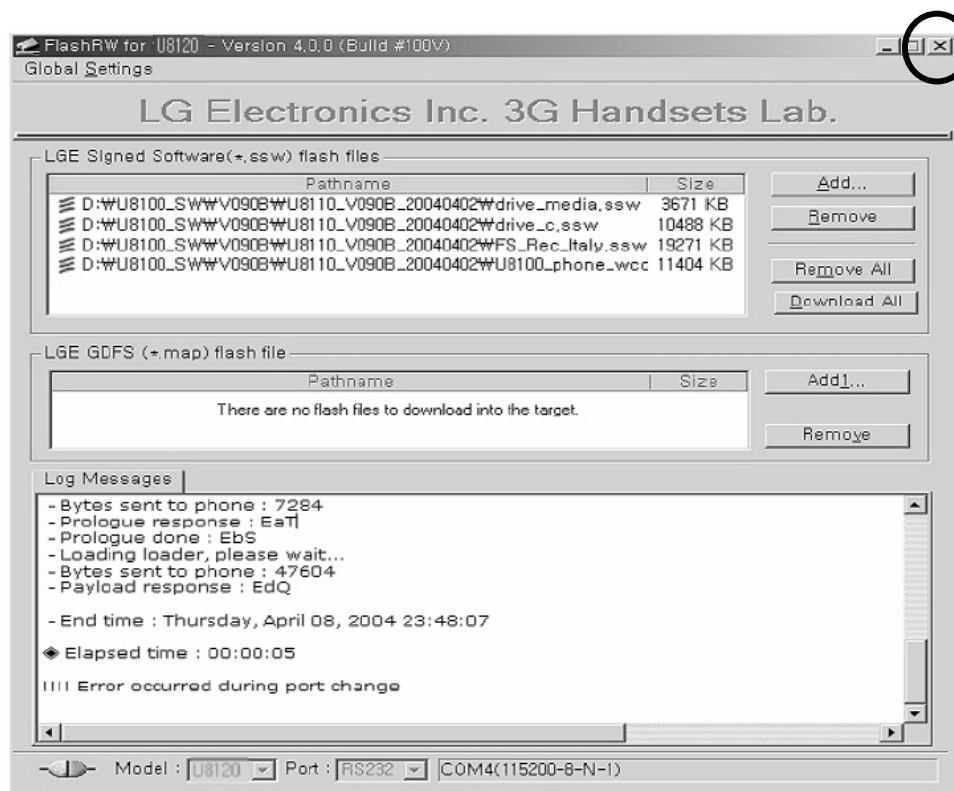


6. DOWNLOAD

H. Close FlashRW.exe

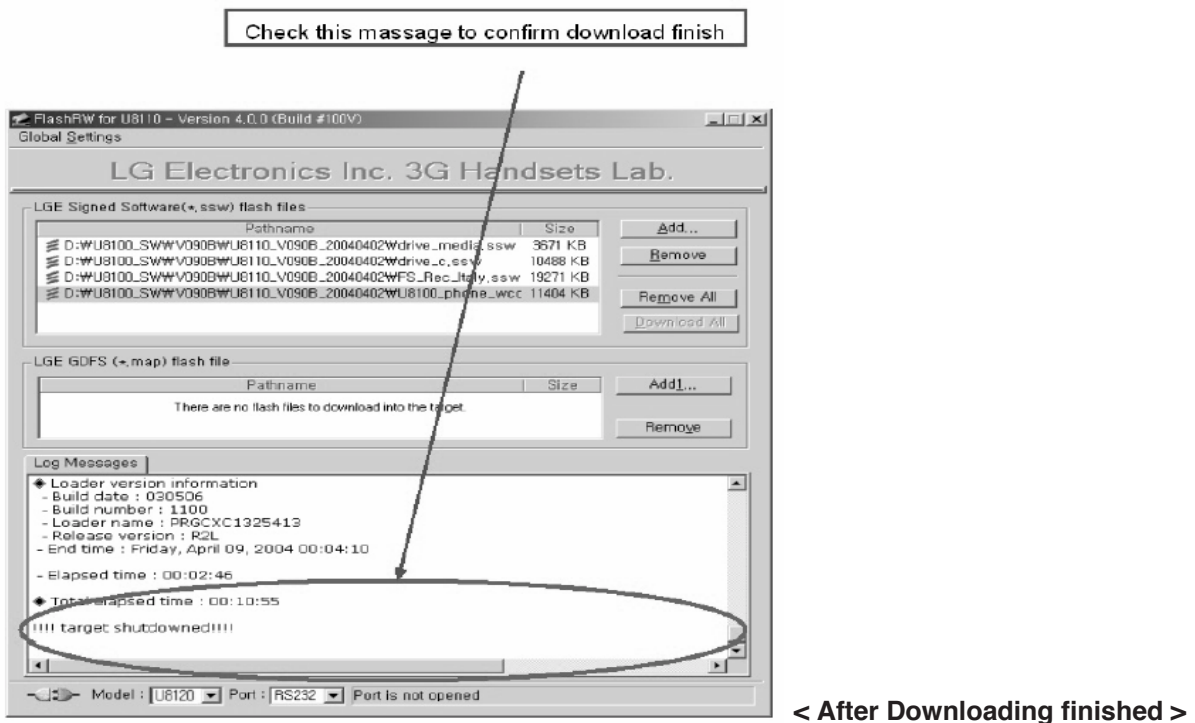
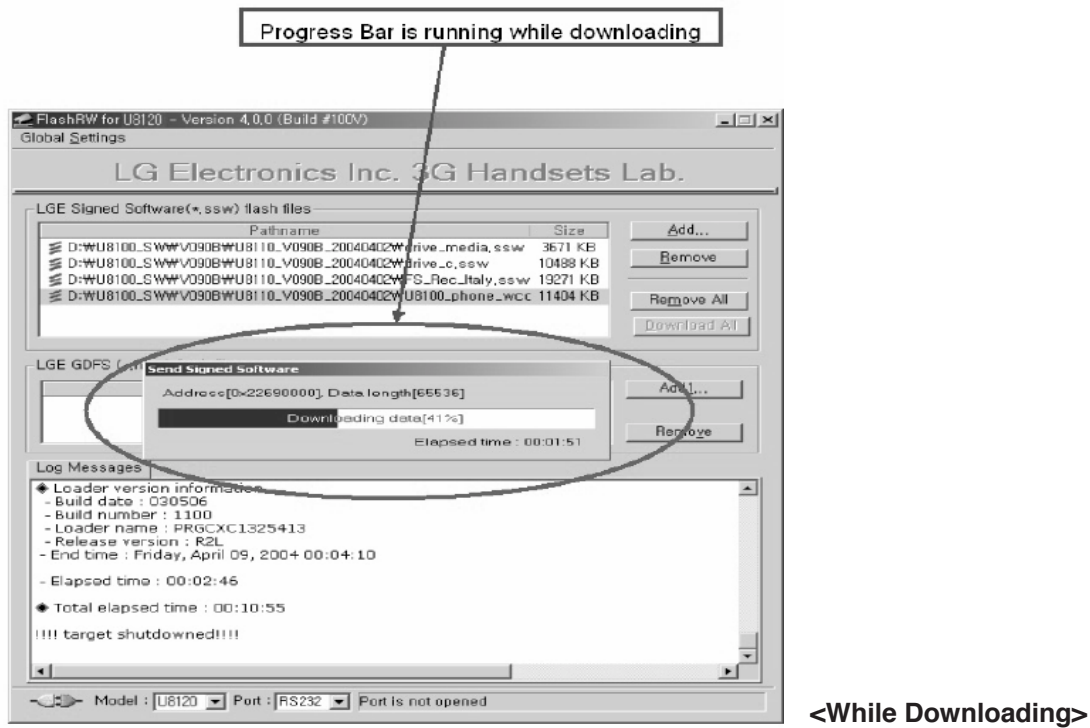
I. Remove & Insert Main battery to reset the phone

This action for USB Driver Install is done only at the first time of installation. If you want to download software, just do as same as U8XXX Download (4) - Connect & Download says



6. DOWNLOAD

6.3.1. U8XXX Download(6) - Connect & Download



6.3.1. U8XXX Download(7) - Trouble shooting

Check these questions when trouble happens.

- A. Check if UART & USB Port configuration is right.
- B. Do not change RS-232 baud rate(115200BPS). It is fixed and never changed.
- C. Check if UART & USB Cable is connected.
- D. You can't select any GDFS File. If you do, Trouble will happen in the phone.
- E. Don't disconnect downloading cable while downloading LGE SSW images into phone.

6. DOWNLOAD

7. CALIBRATION

7.1 General Description

This document describes the construction and the usage of the software used for the calibration of LG's GSM/GPRS/WCDMA Multimedia Mobile Phone (U8550). The calibration menu and their results are displayed in PC terminal by Mobile phone.

This calibration software includes GSM, DCS, WCDMA Band RF parts calibration and Battery calibration. This calibration software was called "XCALMON(eXtended CALibration and MONitor program)". From now on, the calibration software will be called XCALMON in this document.

7.2 XCALMON Environment

7.2.1 H/W Environment

- PC with RS-232 Interface & GPIB card installed
- GSM/GPRS/WCDMA Multimedia Mobile Set (U8550)
- Agilent 8960 Series 10 E5515C Instrument (E1985B ver 04.08)
- Tektronix PS2521G Power Supply
- ETC (GPIB cable, Serial cable, RF cable, Power cable, Dummy battery)

7.2.2 S/W Environment

- National Instrument GPIB & VISA (ver 2.60 full) driver install
- Agilent 8960 VXI driver(E1960) install
- XCALMON EXE files
- OS : Window98, Window2000, WindowXP
- Serial port configuration :
Baud rate: 115200 / Char length: 8bit / No Parity/ No Flow control Stop bits: 1 bit

7.2.3 Configuration Diagram of Calibration Environment

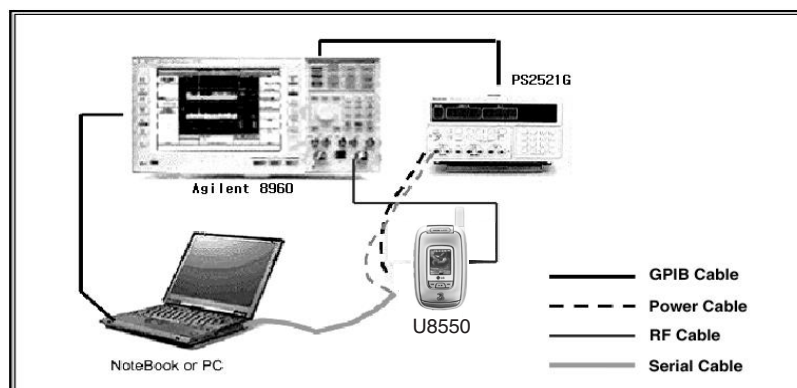


Figure 7-1. Calibration Configuration Figure

7.3 Calibration Explanation

7.3.1 Overview

In this section, it is explained each calibration item in the XCALMON. Also the explanation includes technical information such as basic formula of calibration and settings for key parameters in each calibration procedure.

At first, when any of calibration is done, the results are displayed in the XCALMON result window and the result of calibration will be stored in GDFS(Global Data Flash Storage).

7.3.2 Calibration Items

A. EGSM 900 Band

- MODA-D(MD bit) Delay Calibration
- RXVCO Varactor Operating Point Calibration
- TXVCO Varactor Operating Point Calibration
- TX Loop Bandwidth Calibration
- VCXO Calibration
- TX Power Calibration
- RSSI and AGC Calibration

B. DCS 1800 Band

- RXVCO Varactor Operating Point Calibration
- TXVCO Varactor Operating Point Calibration
- TX Loop Bandwidth Calibration
- TX Power Calibration
- RSSI Calibration

C. WCDMA Band

- RF VCO Center Frequency Calibration
- TX Carrier Suppression Calibration
- TX LPF Bandwidth Calibration
- TX Maximum Output Power Calibration
- TX Power Table Calibration
- TX Open Loop Power Control Calibration
- RX LPF Bandwidth Calibration
- RX LNA Gain Switch and AGC Hysteresis Calibration
- RX AGC Gain Max and Rx RSSI Calibration

7. CALIBRATION

7.3.3 EGSM 900 Calibration Items

A. MOD-A(MD bit) Delay Calibration

- Purpose

The procedure is designed to calibrate the timing alignment between the MODA-D signals and the reference signal (13 MHz). It also ensures that the MOD signals have stable values when they are clocked into the divider of the Phase-Locked Loop (PLL).

- Procedure Proposal

1. Set the ME to mid channel in the GSM TX band.
2. Set the delay setting in default mode, that is, no delay.
3. Wait approximately 300 us to 400 us to allow the PLL to lock.
4. Measure the RMS phase error. A threshold value of > 20 deg indicates that the PLL is running in the forbidden time region.
5. Save the RMS phase error result locally.
6. Step up the delay setting according to Table 10.1 below.
7. Repeat from step 4.
8. Choose delay setting that gives maximum distance to the consecutive field of corrupted RMS phase error values in the vector.
9. Store delay setting both to the GD_RF_Mod_Delay and to the GD_DirMod_Mod_Delay.
10. Reset the radio.

Index	DIMC	MD
[0]	0	00(0)
[1]	0	01(1)
[2]	0	10(2)
[3]	0	11(3)
[4]	1	00(0)
[5]	1	01(1)
[6]	1	10(2)
[7]	1	11(3)

Table 7-1. Delay Settings for the MOD-A

B. RXVCO Varactor Operating Point Calibration

- Purpose

To adjust the varactor diode to a pre-determined operating point, so that the loop voltage of the RXVCO (measured with an ADC in AB 2000) is within the valid range. This is necessary to secure that all RX channels can be reached.

- Procedure Proposal

1. Put the ME in static RX mode.
2. Measure the loop voltage with the AB 2000 ADC for all CVCO settings, that is, 0 ~ 7. Find a CVCO value that fulfills the requirements on loop voltage for low and high channel.
3. If there are several CVCO values that fulfill the loop voltage requirements, then the optimum CVCO value is the one that centers the loop voltage within the specified limits.
4. Store the selected CVCO in the memory.
(GD_RX_VCO_Centre_Frequency_Adjustment_Band)
5. Reset the radio.

C. TXVCO Varactor Operating Point Calibration

- Purpose

To adjust the varactor diode to a pre-determined operating point, so that the loop voltage of the TXVCO (measured with an ADC in AB 2000) is within the valid range. This is necessary to secure that all TX channels can be reached.

- Procedure Proposal

1. Put the phone in static TX mode.
2. Measure the loop voltage with the AB 2000 ADC for all CVCO settings, that is, 0 ~ 7. Find a CVCO value that fulfills the requirements on loop voltage for low and high channel.
3. If there are several CVCO values that fulfill the loop voltage requirements, then the optimum CVCO value is the one that centers the loop voltage within the specified limits.
4. Store the selected CVCO in the memory.
(GD_TX_VCO_Centre_Frequency_Adjustment_Band)
5. Reset the radio.

D. TX Loop Bandwidth Calibration

- Purpose

The loop bandwidth is calibrated to match the pre-filtering of the modulation in DB 2000 by adjusting the phase detector current.

Note: This also indirectly adjusts the VCO gain that can otherwise not be calibrated.

This will ensure a correct transfer function for the modulation and keep phase error to a minimum.

7. CALIBRATION

- Procedure Proposal

1. Put the ME in switched TX mode on mid channel in frequency interval 11 for EGSM (with random modulation).
2. Measure the RMS phase error at the RF connector.
3. Tune the phase detector current (IPHD) until the phase error is minimized. If two IPHD settings gave the same RMS, choose the lowest value. Measure 10 bursts for each value.
4. Calculate and store the IPHD values in GDFS (GD_IPHD_8Temperature_and_24Channel_Compensation_Band)
5. The offsets in the table are steps in the IPHD Table 10.2 and all offsets refer to the calibrated value (Trim) at mid channel in room temperature.

Frequency Interval																								
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
0	-2	-2	-2	-2	-1	-1	-1	-1	-1	0	0	0	0	0	1	1	1	1	1	1	2	2	2	2
1	-2	-2	-2	-2	-1	-1	-1	-1	-1	0	0	0	0	0	1	1	1	1	1	1	2	2	2	2
2	-2	-2	-2	-2	-1	-1	-1	-1	-1	0	0	0	0	0	1	1	1	1	1	1	2	2	2	2
3	-2	-2	-2	-2	-1	-1	-1	-1	-1	0	0	0	0	0	1	1	1	1	1	1	2	2	2	2
5	-2	-2	-2	-2	-1	-1	-1	-1	-1	0	0	0	0	0	1	1	1	1	1	1	2	2	2	2
4	-2	-2	-2	-2	-1	-1	-1	-1	-1	0	0	0	0	0	1	1	1	1	1	1	2	2	2	2
6	-2	-2	-2	-2	-1	-1	-1	-1	-1	0	0	0	0	0	1	1	1	1	1	1	2	2	2	2
7	-2	-2	-2	-2	-1	-1	-1	-1	-1	0	0	0	0	0	1	1	1	1	1	1	2	2	2	2

Table 10-2. IPHD Compensation for EGSM Band

E. VCXO Calibration

- Purpose

This procedure aims to calibrate the value of DAC3 to establish a VCXO-frequency that is sufficiently close to 13 MHz at room temperature. It also ensures that the VCXO tuning range is sufficient, and that the temperature compensation table for VCXO is completed accordingly.

Note: The frequencies in this section are related to the 13 MHz VCXO-frequency. Depending on the calibration procedure, the 13 MHz VCXO frequency can be acquired by first measuring an EGSM, DCS, or W-CDMA RF frequency at the antenna and then translating the measured frequency to the 13 MHz VCXO frequency.

- Procedure Proposal

1. Put the ME in switched low power TX mode with a modulated carrier on a mid channel. Use the calibrated value of the cap array and phase detector current.
2. Tune DAC3 in AB 2000 (VCXOCONT) to end and mid values, and check tuning range.

Acquire the following VCXO (13 MHz) frequencies:

fmin = 13 MHz VCXO-frequency @ DAC3=1

fmid = 13 MHz VCXO-frequency @ DAC3=1024

fmax = 13 MHz VCXO-frequency @ DAC3=2047

Note that it is necessary to translate the measured RF-frequency (EGSM, DCS, or W-CDMA) to the 13 MHz VCXO-frequency.

3. Acquire the ME temperature, TCal, from the temperature sensor in ME.

4. Store fmin, fmid, fmax and TCal for calculation.

5. Calculate the DAC-value, VCXOCONTCal, that gives zero frequency error at the mid channel, using piecewise linear interpolation, and store the value in the memory (GD_RF_SYNT_CONFIG_ID and GD_VCXO)

6. Calculate

$K_LO = (fmid - fmin)/1023$

$K_HI = (fmax - fmid)/1023$

Each value is then multiplied by 100 and rounded to nearest integer, with the results stored in the memory (GD_RF_SYNT_CONFIG_ID).

$AFC_DAC_STEP_LO = ROUND(100*K_LO)$

$AFC_DAC_STEP_HI = ROUND(100*K_HI)$

where ROUND(x) = x rounded to the nearest integer.

F. TX Power Calibration

- Purpose

These procedures describe how to tune the different power levels of the power amplifier to output powers corresponding to values in GSM 05.05, and explain how to calculate intermediate power levels that will ensure a good power versus time performance.

- Procedure Proposal

1. Reset the DIRMOD-block, and select a ,mid channel using the trimmed value on the capacity array for VCO tuning and a default IPHD value as phase detector current. Turn on dummy burst modulation.
2. Use the Multi-burst method to characterize the relation between output power and the DACvalue. Then store the DAC values that give the closest approximations to the power targets defined in Table 10-3.
3. To avoid yield problems with the power template and switching transients spectrum a margin to the compression point of the PA should be observed. However, the output power must be kept within the tolerances specified in Table 10-3.
4. Store DAC values in memory (GD_FullPower_Band).
5. Initiate the intermediate value calculation, which calculates and store the values in memory (GD_IntermediatePower_Up/Down_1..7_Band).
6. The difference between the transmitter power at two adjacent power control levels, measured at the same frequency, shall not be less than 0.5 dB and not more than 3.5 dB.

7. CALIBRATION

Parameter	Target Full Power (dBm)	Tolerances (dB)	
PL 5	33.0	+0.5 – 1.0	Vol
PL 6	31.0	±0.3	Vol
PL 7	29.0	±0.5	Vol
PL 8	27.0	±0.5	Vol
PL 9	25.0	±0.5	Vol
PL 10	23.0	±0.5	Vol
PL 11	21.0	±0.5	Vol
PL 12	19.0	±0.5	Vol
PL 13	17.0	±0.5	Vol
PL 14	15.0	±0.5	Vol
PL 15	13.0	±0.5	Vol
PL 16	11.0	±0.5	Vol
PL 17	9.0	±0.5	Vol
PL 18	7.0	±0.5	Vol
PL 19	5.0	±0.5	Vol

Table 10-3. Target Power Levels for EGSM

G. RSSI and AGC Calibration

- Purpose

This procedure satisfies the two following requirements:

Calibrate an absolute power level on the antenna to a corresponding RSSI value. This value together with a pre-defined slope figure is then used to calculate the RSSI value of an arbitrary received antenna power. The formula $y=kx+m$ is used. (Where k is the slope value, x the RSSI value, y the actual level, and m is an offset value.)

Calculate the attenuation when the Low Noise Amplifier is switched off in the receiver branch.

The attenuation value is stored in the flash memory and used when very high input signals are fed into the ME.

- Procedure Proposal

1. Select switched receiver on a mid EGSM Channel.
2. Feed a modulated -68.5 dBm signal, on the same mid EGSM-Channel to the antenna input.
Measure the RSSI value, calculate the RSSI table and store the value in GDFS as parameter: GD_RXLEVS_DBM_BURST_M_BAND.
3. On the same channel, now feed a modulated -50 dBm signal and measure the RSSI value.
4. Switch off the LNA, using the command $FREC=3,0,1$, and measure the RSSI value.

5. Calculate the difference between on and off (converting the result to ,real dB attenuation) and store the result in GD_MPH_RX_AGC_Parameters_Band.

7.3.4 DCS 1800 Calibration Items

A. RXVCO Varactor Operating Point Calibration

- Purpose

To adjust the varactor diode to a pre-determined operating point, so that the loop voltage of the RXVCO (measured with an ADC in AB 2000) is within the valid range. This is necessary to secure that all RX channels can be reached.

- Procedure Proposal

1. Put the ME in static RX mode.
2. Measure the loop voltage with the AB 2000 ADC for all CVCO settings, that is, 0 ~ 7. Find a CVCO value that fulfills the requirements on loop voltage for low and high channel.
3. If there are several CVCO values that fulfill the loop voltage requirements, then the optimum CVCO value is the one that centers the loop voltage within the specified limits.
4. Store the selected CVCO in the memory.
(GD_BAND_RX_VCO_Centre_Frequency_Adjustment)
- 5 Reset the radio.

B. TXVCO Varactor Operating Point Calibration

- Purpose

To adjust the varactor diode to a pre-determined operating point, so that the loop voltage of the TXVCO (measured with an ADC in AB 2000) is within the valid range. This is necessary to secure that all TX channels can be reached.

- Procedure Proposal

1. Put the phone in static TX mode.
2. Measure the loop voltage with the AB 2000 ADC for all CVCO settings, that is, 0 ~ 7. Find a CVCO value that fulfills the requirements on loop voltage for low and high channel.
3. If there are several CVCO values that fulfill the loop voltage requirements, then the optimum CVCO value is the one that centers the loop voltage within the specified limits.
4. Store the selected CVCO in the memory.
(GD_BAND_TX_VCO_Centre_Frequency_Adjustment)
5. Reset the radio.

C. TX Loop Bandwidth Calibration

- Purpose

The loop bandwidth is calibrated to match the pre-filtering of the modulation in DB 2000 by adjusting the phase detector current.

Note: This also indirectly adjusts the VCO gain that can otherwise not be calibrated. This will ensure a correct transfer function for the modulation and keep phase error to a minimum.

7. CALIBRATION

- Procedure Proposal

1. Put the ME in switched TX mode on mid channel in frequency interval 11 for DCS (with random modulation).
2. Measure the RMS phase error at the RF connector.
3. Tune the phase detector current (IPHD) until the phase error is minimized. If two IPHD settings gave the same RMS, choose the lowest value. Measure 10 bursts for each value.
4. Calculate and store the IPHD values in GDFS
(GD_IPHD_8Temperature_and_24Channel_Compensation_Band)
5. The offsets in the table are steps in the IPHD Table 10.4 and all offsets refer to the calibrated value (Trim) at mid channel in room temperature.

Frequency Interval																								
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
0	-6	-6	-5	-4	-4	-3	-3	-2	-2	-1	-1	0	0	1	1	2	2	3	3	4	4	5	5	5
1	-6	-6	-5	-4	-4	-3	-3	-2	-2	-1	-1	0	0	1	1	2	2	3	3	4	4	5	5	5
2	-6	-6	-5	-4	-4	-3	-3	-2	-2	-1	-1	0	0	1	1	2	2	3	3	4	4	5	5	5
3	-6	-6	-5	-4	-4	-3	-3	-2	-2	-1	-1	0	0	1	1	2	2	3	3	4	4	5	5	5
4	-6	-6	-5	-4	-4	-3	-3	-2	-2	-1	-1	0	0	1	1	2	2	3	3	4	4	5	5	5
5	-6	-6	-5	-4	-4	-3	-3	-2	-2	-1	-1	0	0	1	1	2	2	3	3	4	4	5	5	5
6	-6	-6	-5	-4	-4	-3	-3	-2	-2	-1	-1	0	0	1	1	2	2	3	3	4	4	5	5	5
7	-6	-6	-5	-4	-4	-3	-3	-2	-2	-1	-1	0	0	1	1	2	2	3	3	4	4	5	5	5

Table 10-4. IPHD Compensation for DCS Band

D. TX Power Calibration

- Purpose

To tune the different DCS power levels of the power amplifier to output powers corresponding to values in GSM 05.05 and calculate the intermediate levels that ensure a good power versus time performance.

- Procedure Proposal

1. Reset the DIRMOD-block, and select a ,mid channel using the trimmed value on the capacity array for VCO tuning and a default IPHD value as phase detector current. Turn on dummy burst modulation.
2. Use the Multi-burst method to characterize the relation between output power and the DACvalue. Then store the DAC values that give the closest approximations to the power targets defined in Table 10-5.

7. CALIBRATION

3. To avoid yield problems with the power template and switching transients spectrum a margin to the compression point of the PA should be observed. However, the output power must be kept within the tolerances specified in Table 10-5.
4. Store DAC values in memory (GD_FullPower_Band).
5. Initiate the intermediate value calculation, which calculates and store the values in memory (GD_IntermediatePower_Up/Down_1..7_Band).
6. The difference between the transmitter power at two adjacent power control levels, measured at the same frequency, shall not be less than 0.5 dB and not more than 3.5 dB.

Parameter	Target Full Power (dBm)	Tolerances (dB)	
PL 0	30.0	+0.5 – 1	Vol
PL 1	28.0	±0.3	Vol
PL 2	26.0	±0.5	Vol
PL 3	24.0	±0.5	Vol
PL 4	22.0	±0.5	Vol
PL 5	20.0	±0.5	Vol
PL 6	18.0	±0.5	Vol
PL 7	16.0	±0.5	Vol
PL 8	14.0	±0.5	Vol
PL 9	12.0	±0.5	Vol
PL 10	10.0	±0.5	Vol
PL 11	8.0	±0.5	Vol
PL 12	6.0	±0.5	Vol
PL 13	4.0	±0.5	Vol
PL 14	2.0	±0.5	Vol
PL 15	0.0	±1	Vol

Table 10-5. Target Power Levels for DCS

7. CALIBRATION

E. RSSI Calibration

- Purpose

This procedure calibrates an absolute power level on the antenna against a corresponding RSSI value. This value together with a pre-defined slope figure is then used to calculate the RSSI value of an arbitrary received antenna power. The formula $y=kx+m$ is used. (Where k is the slope value, x the RSSI value, y the actual level, and m is an offset value).

- Procedure Proposal

1. Select switched receiver on a mid DCS-Channel.
2. Feed a modulated -68.5 dBm signal, on the same mid DCS Channel to the antenna input.
Measure the RSSI value, calculate the RSSI table, and store it to the memory (GD_BAND_RXLEVS_DBM_BURST_M[2])-1 byte.

7.3.5 WCDMA Calibration Items

A. RF VCO Center Frequency Calibration

- Purpose

This procedure is designed to calibrate the RFVCO (Radio Frequency Voltage Controlled Oscillator) center frequency of the Ericsson RF 2110 (hereafter referred to as the RF 2100) and ensure that all channels can be reached with sufficient margin.

The objective of the calibration is to determine a CVCO (Center VCO) value that guarantees the functionality of the RFLO (Radio Frequency Local Oscillator).

- Procedure Proposal

1. Start the VCXO and RFVCO. VCXOCONT is set to its calibrated value, Ericsson AB 2000 DAC3.
2. Measure the loop voltage (WRFLOOP), with the AB 2000 ADC (GPA4), for all CVCO settings, that is, 0-7. Find a CVCO value that fulfills the requirements on loop voltage for low and high channel. If there are several CVCO values that fulfill the loop voltage requirements, then the optimum CVCO value is that that centers the loop voltage within the specified limits.
3. Store the calibrated CVCO value in GD_RF_SYNT_CONFIG_ID.

B. TX Carrier Suppression Calibration

- Purpose

DC offset compensation the carrier, to the wanted signal at the IQ-modulator output. The leakage is caused by imperfections in the baseband IQ-path and inside the IQ-modulator. It impairs the modulation accuracy and results in a high vector magnitude (EVM). The outcome of the calibration is values for RECDCl and RECDcQ that minimize the carrier.

- Procedure Proposal

1. Set the ME in TX mode on mid-channel. Use typical TX settings. Generate 960 kHz squarewave on both I and Q with amplitude = 8 (sine-wave could be used instead). Start with the best value from earlier calibrated units on RECDCl on RECDcQ.

2. Measure the relative power between the 1950 MHz carrier and 1949.04 MHz at the antenna output. Jump to step 6 if the requirement is met.
3. Step RECDCl from 0 to 3. Set TXON = 0 and wait 1 ms before changing RECDCl from 3 to 5. Set TXON = 1, wait 1 ms and continue with stepping from 5 to 7.
4. Set RECDCl to the value that minimizes the 1950 MHz carrier. If this involves a change of sign the TXON switching and delay sequence in point 3 must be executed. Jump to 6 if the requirement is met.
5. Find and set RECDcQ to the value that minimizes the 1950 MHz carrier. This can be made by stepping RECDcQ from 0 to 7 with the TXON switching and delay sequence in step 3.
6. If the requirements are not met, repeat steps 3, 4 and, if necessary, 5 once with the new RECDCl and RECDcQ (found in 4 and 5) as initial values. Otherwise proceed with step 6.
7. Save the final dBc value (for statistics), RECDCl and RECDcQ. Store the calibrated parameters in GD_RF_TX_CONFIG_ID.

C. TX LPF Bandwidth Calibration

- Purpose

The low pass filters within the Ericsson DB 2100 (hereafter referred to as DB 2100) are designed to prevent spurious emissions output from the TX IQ-D/A (Digital-Analog) converters ® without adversely affecting the signal or causing a deterioration of the modulation accuracy.

The objective of this calibration is to determine the values for LPQ and LPBW that offer the best trade off against the system-related requirements. These settings determine the cut-off frequency and should always have the same value.

- Procedure Proposal

1. Use typical TX settings. Generate a 960 kHz square-wave at baseband without phase shift between I and Q. The amplitude should be about 50% of full scale.
2. Measure the relative power between 1952.88 MHz ($f_c + 3 \cdot 960$ kHz) and 1949.04 MHz ($f_c \ominus 960$ kHz) in dB at the antenna output. Find the setting of LPQ = LPBW between 3 and 15 that obtains the dBc value closest to the typical value. Start with the best value from earlier calibrated units. Spectrum analyzer settings (example):
RBW = 300 kHz, Span = 8 MHz.
3. Set LPQ=LPBW to the found value in 2. Also save the dBc and the decided LPQ = LPBW value for statistics. Store the calibrated parameters in GD_RF_TX_CONFIG_ID.

D. TX Maximum Output Power Calibration

- Purpose

These procedures verify that the ME can meet the requirements on maximum output power. The calibration aims to establish WPABias, VGA and QVGA settings that fulfill ACLR requirements for maximum output power, both in high, medium, and low gain mode.

These calibrations are designed to conform to the ME maximum output power and ACLR requirements specified in 3GPP Spec TS34.121.

- Procedure Proposal

1. Use typical TX settings, mid channel.
2. Set gain to the best value based upon previous calibrated units.

7. CALIBRATION

3. Measure output power as broadband power.
4. If the ACLR requirements, described in Table 11 are not met, calculate the test step necessary to achieve the correct power. Use correlation from earlier calibrated units to calculate the new gain setting (default correlation between VGA and output power is 1 dB and for QVGA 0.25dB).
5. Measure ACLR at this power level.
6. If the ACLR requirement is not met, reduce VGA and QVGA.
7. Measure and store the temperature at this point. This provides the value for TPmax.
8. This power and gain setting is to be used in calibration of TX power table.
9. Set gain to maximum power in medium gain mode and measure ACLR at this power level. RFBias should be set to 1 and WPABias should be set to the same value as for maximum output power.
10. If the requirements are not met, step the gain down and measure ACLR until the requirements are met. The correlation between ACLR and output power is that 1 dB in power equals typical 3 dB in ACLR. Use correlation from earlier calibrated units to calculate the new gain setting.
11. This power, Pmax meas MG, is input to the calibration of TX power table.
12. Set gain to maximum power in low gain mode and measure ACLR at this power level. RFBias should be set to 1 and WPABias should be set to the same value as for maximum output power.
13. If the requirements are not met, step the gain down and measure ACLR until the requirements are met. Use known correlation from earlier calibrated units to calculate the new gain setting.
14. This power, Pmax meas LG, and gain setting provides input to the calibration of TX power table.

E. TX Power Table Calibration

- Purpose

The calibration data contained within the TX Power Table controls the gain for all types of power change; including, the inner-loop power control and maximum output power of the platform.

The purpose of this calibration is to complete the TX Power gain table with values for VGA, QVGA, RFBias, WPABias, and WDCDCREF that meet the specified requirements for innerloop power-control and Maximum output power. The size of hysteresis area must also be found.

These calibrations are designed to conform to the ME maximum output power, inner loop power control, change of TFC and (PRACH preamble tolerances) requirements specified in 3GPP Spec TS34.121.

- Procedure Proposal

This calibration consists of two parts: first measurements and then an off-line calculation. The measurement results are used for characterizing the hardware so that proper settings can be calculated for all tables. Settings and limitations are also used from maximum output calibration.

1. Perform measurements

- (1) VGA behavior in LG (Low Gain) mode. PABias should not be offset and RFBias should be 1.
- (2) VGA behavior in MG (Medium Gain mode). PABias should not be offset and RFBias should be 1.
- (3) QVGA behavior in LG mode
- (4) IQ-Gain behavior in LG mode.
- (5) WPABias gain step size. Every eighth setting is measured twice. For better accuracy take the average of each step pair. Interpolate the gain steps in between the averaged measured values.
- (6) WDCDCREF gain step size. Every fifth setting is measured twice. For better accuracy take the average of each step pair. Interpolate the gain steps in between the averaged measured values.

7. CALIBRATION

- (7) Size of step between LG/MG and MG/HG and between each setting of RFBias (1-7). The main purpose is to find the relative difference at different frequencies. Distribute with equal frequency offset except if there are known ,worst-case frequencies. Measured at 5 channels, maximum and minimum steps reported. Average value of minimum and maximum should be used in following calculations.
- (8) Measure properties: Measure the following properties using a modulated signal: WPA-gain expansion versus output power on mid channel.
 Compensation needed for maximum output power over the band (13 channels).
2. Perform offline calculations
- (1) Calculate the compensation values for Table 10-6. Store these values in GD_RF_TXGAIN_TB_SEL_ID.
- (2) Extract the range of needed compensation tables (minimum and maximum).
- (3) Calculate the expected compensation for each table in dB (use ,table 0 for the table that is ,0 dB or closest to ,0 dB) and spread out the rest to achieve equidistant compensations.
- (4) Calculate and store the 24 sets of tables, GD_RF_TX_GAIN_TB0_ID to GD_RF_TX_GAIN_TB23_ID. Each set of tables shall include:
- One High-gain table: 44 bytes.
 - One Low-gain table: 44 bytes.
 - One RFBias table: 22 bytes.
 - One WDCDCRef table: 44 bytes.
 - One WPABias table: 44 bytes.
 - One value for IQ-Gain: 1 bit (will occupy 1 byte).
 - One value for TABLE_OVERLAP: 1 byte.
 - One value for UPPER_LIMIT: 1 byte.
- (5) Calculate the actual compensation (for maximum output power) that each of these 24 tables will give. Store this in GD_RF_TX_FREQ_INT_ID.
3. Store data in GDFS

Temp.	UARFCN											
	9612	9637	9662	9687	9712	9737	9763	9788	9813	9838	9863	9888
-15												
0												
15												
30												
45												
60												
75												
90												

Table 10-6.The Complete Gain Compensation Table

7. CALIBRATION

E. TX Open Loop Power Control Calibration

- Purpose

The purpose of the calibration of open loop power control is to store parameters for the Open Loop Power Control algorithm. This is a pure off-line calculation. Use data (positions and output power, in dBm) from table 0. Curve fitting should be done preferably with minimum square method.

System related requirements:

- Open loop power control
- Maximum allowed UL TX Power
- UE Transmitted power

- Procedure proposal

1. Create a curve fitting for the low-gain region, use positions with a power greater than -50 dBm:
Position = B3 * Pout + A3
2. Extract A3 and B3.
3. The power level (output power) at the highest position in the low-gain region sets the parameter P2.
4. Divide the high-gain region into two regions at the split between mid-gain and high-gain. The output power at this position sets the parameter P1.
5. Do a curve fitting for the mid-gain region (where RFBias > 0) of the highgain region, use power-levels from P2: Position = B2 * Pout + A2
6. Extract A2 and B2
7. Do a curve fitting for the high-gain region (where RFBias = 0) of the highgain region: Position = B1 * Pout + A1
8. Extract A1 and B1
9. Save A1, A2, A3, B1, B2, B3, P1 and P2 in GD_RF_TX_GAIN_PARAM_ID.

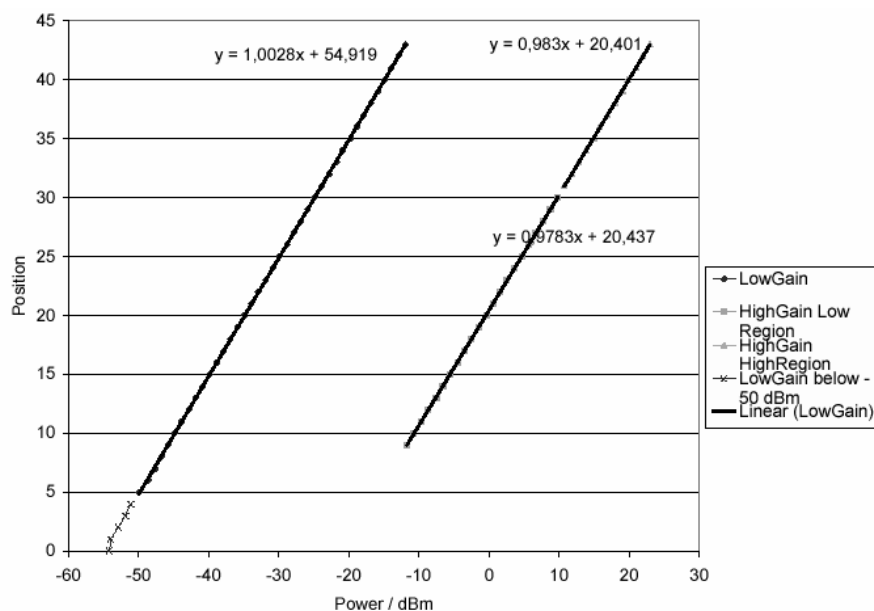


Figure 7-2. Example of Position versus Power and Calculated Equations

F. RX LPF Bandwidth Calibration

- Purpose

This procedure calibrates the LPF bandwidth. The bandwidth of the channel filters will affect system parameters as reception sensitivity and adjacent channel selectivity. The procedure also verifies that the IF-filter is properly matched.

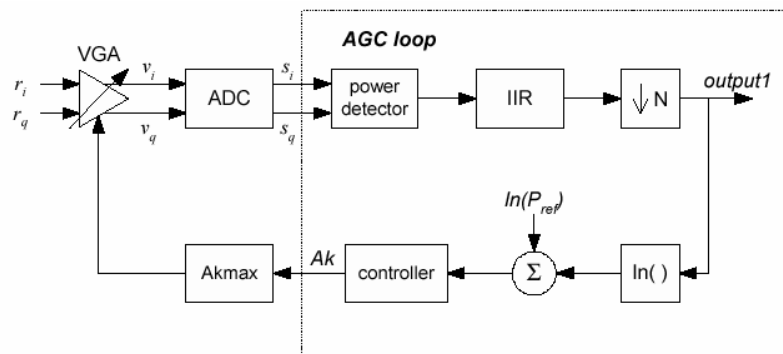


Figure 7-3. AGC Block Diagram (Parameter Ak, Output1, and Pref)

- Procedure Proposal

1. Feed a CW carrier at 2140 MHz with a power of -60dBm into the antenna connector.
2. Set UE in RX-mode on 10695ch.
3. Set the AGC_UL and AGC_LL to minimum. GLNA is forced to high gain mode.
4. Set RF 2110 LPQ and LPBW to 8, that is, LPQ=LPBW=8.
5. Get Ak (output2) from N slots. Calculate Average_Ak (Ak_{IB}) according to the equation below. N should be as large as possible, with respect to time consumption.

$$Average_Ak = 10 \cdot \log \left(\frac{1}{N} \sum_{n=1}^N 10^{\frac{Ak_n}{10}} \right)$$

Equation 1

6. Set UE on 10705ch and get Ak (output2). Calculate Average_Ak (Ak_{LB}) according to the Equation 1.
7. Calculate IF-filter symmetry using the following equation.
 $IF_SYM = Ak_{IB} - Ak_{LB}$
8. Set UE on 10685ch and get Ak (output2). Calculate Ak (Ak_{OB}) according to the Equation 1.
9. Calculate selectivity level using following equation.
 $Ak_{SE} = Ak_{OB} - Ak_{IB}$
10. If the requirement is not met, decrease LPBW and LPQ one step and repeat from 8.
11. Store the resulting LPBW and LPQ in GD_RF_RX_CONFIG_ID.

7. CALIBRATION

F. RX LNA Gain Switch and AGC Hysteresis Calibration

- Purpose

This procedure calibrates the gain correction parameter of A_k in the AGC algorithm between $GLNA=0$ and $GLNA=1$; that is, it establishes the gain difference in the LNA between high gain mode and low gain mode. It also calibrates AGC_UL and AGC_LL , the upper and lower A_k values where the AGC should switch between high and low LNA gain (AGC hysteresis).

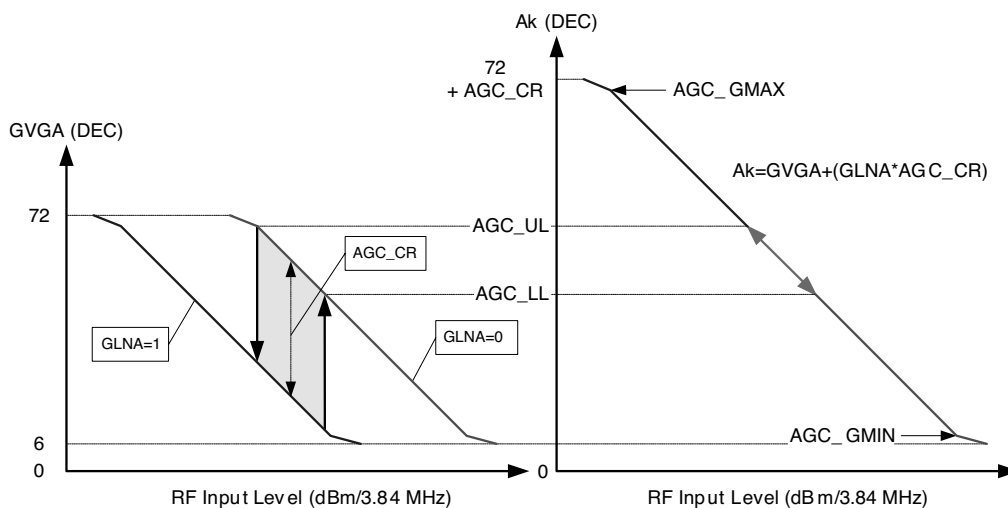


Figure 10-4. LNA Gain Switch and AGC Hysteresis Parameters

1. Set the UE in RX-mode on 10695ch.
2. Feed a CW carrier at 2140 MHz with a power level of -65dBm.
3. Set the AGC_UL and AGC_LL to maximum. $GLNA$ is forced to low gain mode.
4. Get average A_k from Equation 1 and save it. (A_{k_LG})
5. Set the AGC_UL and AGC_LL to minimum. $GLNA$ is forced to high gain mode.
6. Get average A_k . (A_{k_HG})
7. $(A_{k_LG}) - (A_{k_HG}) = (\text{Correction})$.
8. Round off (Correction) to integer (AGC_CR) and store it in GDFS (GD_RF_RX_CONFIG_ID). AGC_CR is an AGC algorithm parameter and is set to DB 2100 RFIF.
9. Calculate $AGC_LL=8+AGC_CR$ and $AGC_UL=18+AGC_CR$ and store them in GDFS (GD_RF_RX_CONFIG_ID). AGC_LL and AGC_UL are AGC algorithm parameters and are set to DB 2100 RFIF.

G. RX AGC Gain Max and RX RSSI Calibration

- Purpose

To prevent wind up in AGC algorithm, this procedure calibrates the absolute power levels at the antenna connector against RSSI values and the maximum gain setting for AGC. Reference [6] specifies that the reporting range of the RSSI should be between -100 dBm to -25 dBm.

The specified accuracy requirement is applied to the received power from -94 through -50 dBm. This is the last RX calibration. LPBW, LPQ, AGC_CR, AGC_LL and AGC_UL must be calibrated according to above calibrations respectively and applied to this calibration. Initially, the AGC anti-wind up is turned on using AGC_GMAX=127. Use the calibrated value after step 2, otherwise the AGC wind up may occur at the beginning of the RSSI calibration.

- Procedure Proposal

1. Set the ME in RX-mode on channel 10695.
2. Feed a CW carrier at 2140 MHz with a power level of -105 dBm. Get average_Ak (output2), add 6 to the value and store it in GDFS as AGC_GMAX (GD_RF_RX_CONFIG_ID), rounded off to an integer. Set the AGC parameter AGC_GMAX to the calibrated value.
3. Clear Ak ,table 0.
4. Change the CW carrier power level to -95 dBm.
5. Read Ak value (output2) and calculate Average_Ak (Equation 1). Store Pin_Corrected (Equation 2) at Ak=round(Average_Ak). N in Equation 1 should be as large as possible.
$$\text{Pin_Corrected} = \text{Pin} - \text{round}(\text{Average_Ak}) + \text{Average_Ak} \quad \text{Equation 2}$$
6. Then increase the output level of the signal generator to -80, -60, -40 and -25 dBm and store the corrected RF input level and Ak to the memory respectively.
7. Use the average Ak values and Pin_Corrected from the two lowest power levels (-95 and - 80 dBm) to extrapolate Ak and Pin_Corrected for -110 dBm according to:
$$\text{Average_Ak_110} = 2 * \text{Average_Ak_95} - \text{Average_Ak_80}$$
$$\text{Pin_Corrected_110} = \text{Pin_Corrected_95} - \text{Pin_Corrected_80}$$
8. Store Average_Ak_110 and Pin_Corrected_110 according to step 4.
9. Perform the interpolation. AK_BANK_SEL in DB 2100 shall be set to 0.
10. Measure the ME temperature (T) and save for offline calculations.
11. Store the result to GDFS. (GD_RF_RX_AK_TB0_ID). When stored in GDFS, the first position in the table (Ak=0) should be replaced with the table number (0-23) in bcd format and the second position (Ak=1) set to 0xffff to flag that the table is calibrated. Position 2 to 5 should be set to zero.
12. Perform the offline calculations and check the requirements.

7. CALIBRATION

7.3.6 Baseband Calibration Item

A. Battery Voltage Calibration

- Purpose

Calibrates the voltage table for the power management functionality. Some voltage measurements in the remaining test will be done with calculated voltage levels from this test.

- Procedure Proposal

1. Send the command LVBA=0 to reset local values in Test Program.
2. Set voltage on VBATT to 3.20 V.
3. Send the command LVBA=5,0x140 to read the low voltage level from ADC.
4. Set voltage on VBATT to 4.10 V.
5. Send the command LVBA=5,0x19A to read the high voltage level from ADC.
6. Send the command LVBA=1 to store local values into global data.
7. Send the command LVBA=3 to view and record values stored in global data.

Voltage Level on VBATT (V)	Min.	Typ.	Max.	Unit
3.2	19	2E	3C	HEX
	25	42	60	DEC
4.1	64	7E	96	HEX
	100	125	150	DEC

Table 10-7. Battery Voltage Calibration Limits

7.4 Program Operation

7.4.1 XCALMON Program Overview

When you try to calibrate the U8550 mobile phone, you should make a configuration of calibration environment like Figure7-1. And if you finish making configuration, please execute the XCALMON program. Running the XCALMON program, you should show XCALMON program window like Figure7-5.

If XCALMON program would be executed, it checks the connection of instruments and initializes them automatically. The result of checking and initializing instruments was shown like Figure7-6.

XCALMON supports three functions.

- Calibration of EGSM 900, DCS 1800, and WCDMA band
- Instrument (Agilent8960, Tektronix PS2521G) control
- UART communication with U8550 mobile phone

XCALMON has three windows and each window support different function.

- ITP(Integrated Test Program) starting window using production loader
- Calibration tree window
- Command window which supports interactive ITP commands like Hyper terminal

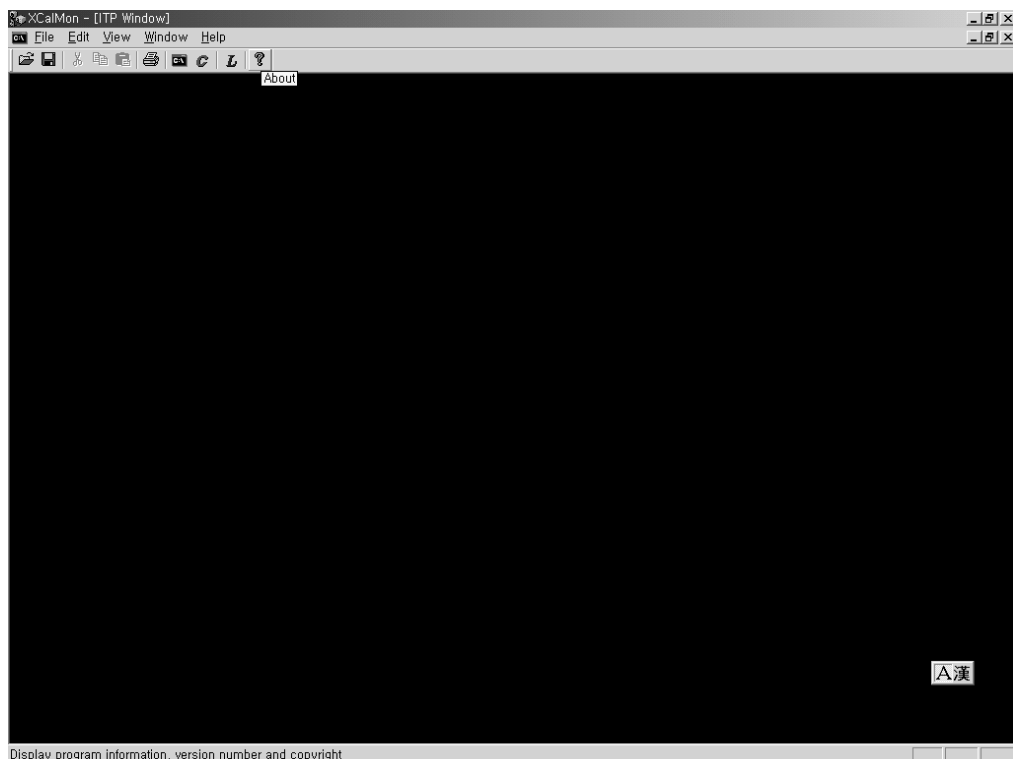


Figure 7-5. XCALMON Window

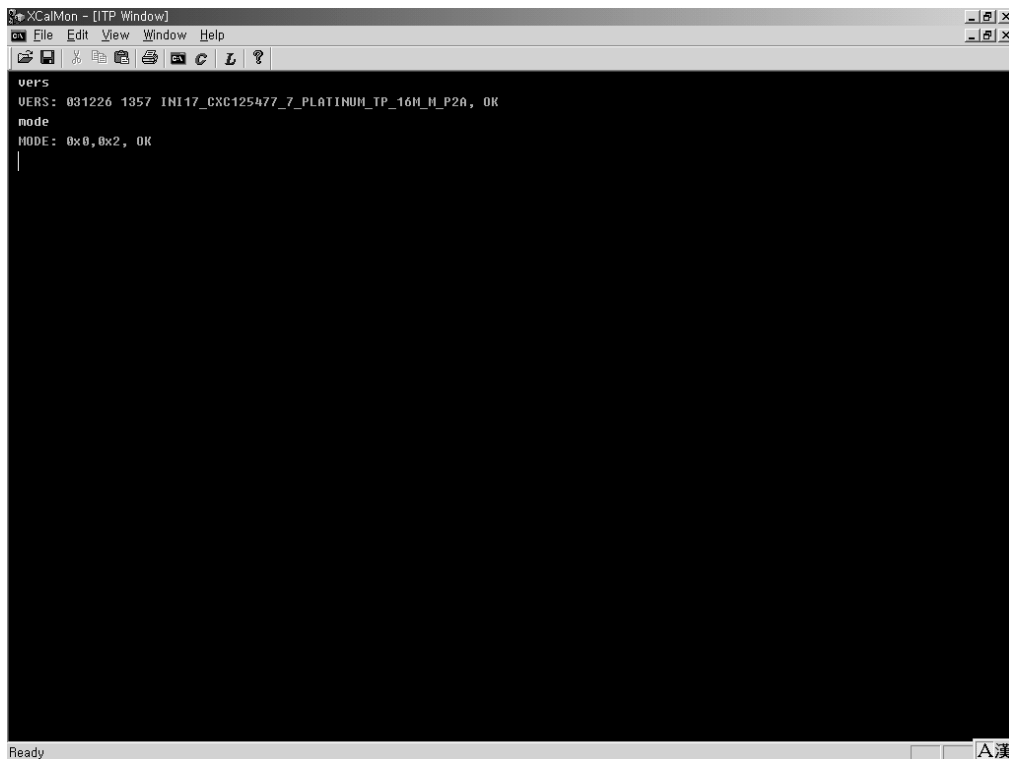
7. CALIBRATION

7.4.2 XCALMON Icon Description

A. DOS Window Icon

When you click the DOS window icon, then you should see the ITP command window like DOS window of DOS-operating system. In ITP command window, you should communicate with U8550 mobile phone which is running in ITP mode.

For example, if you will enter command “VERS” and enter the return key, you should get the response of the present running ITP version information from U8550 mobile phone.



```
XCALMon - [ITP Window]
File Edit View Window Help
VERS
VERS: 031226 1357 IN117_CXC125477_7_PLATINUM_TP_16M_M_P2A, OK
node
MODE: 0x0,0x2, OK
Ready
```

Figure 7-6. XCALMON ITP Command Window

B. Calibration Tree Window Icon

When you click the calibration window icon “C”, then you should see the calibration tree window. That will be shown all calibration items. If you want to calibrate U8550 mobile phone for all calibration items, you should select “Calibration” and push “F4” button in your keyboard.

Also there are four tap view in calibration window.

- OUTPUT : All results of calibration
- STATUS : Summary of calibration result
- INSTRUMENT : Control and view instrument connection status
- UART : Control and view UART connection status

7. CALIBRATION

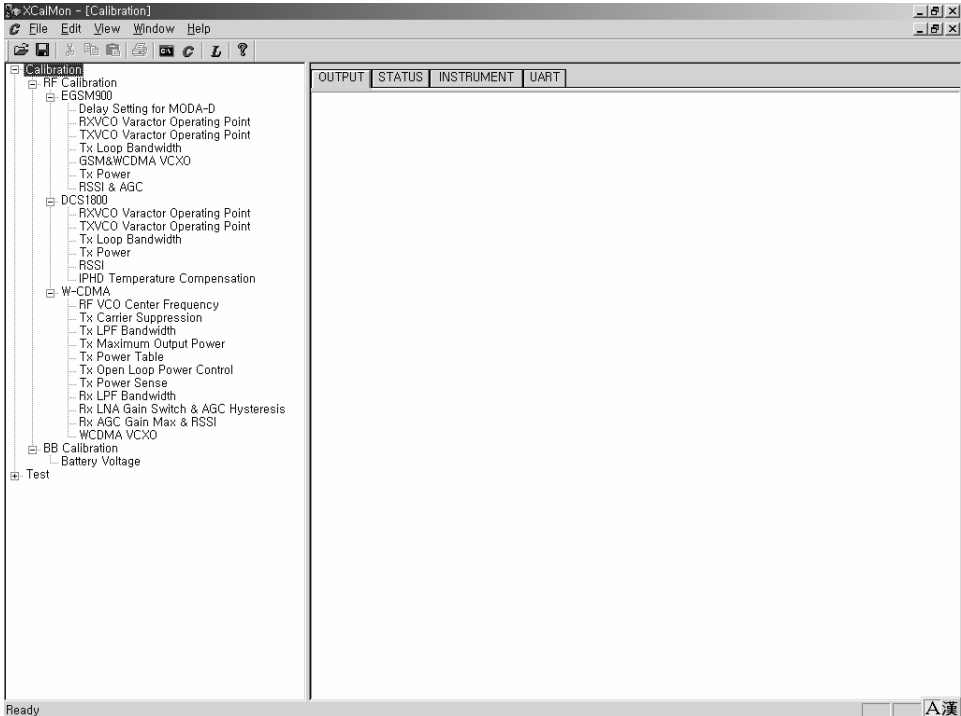


Figure 7-7. XCALMON Calibration Tree Window (OUTPUT Tab)

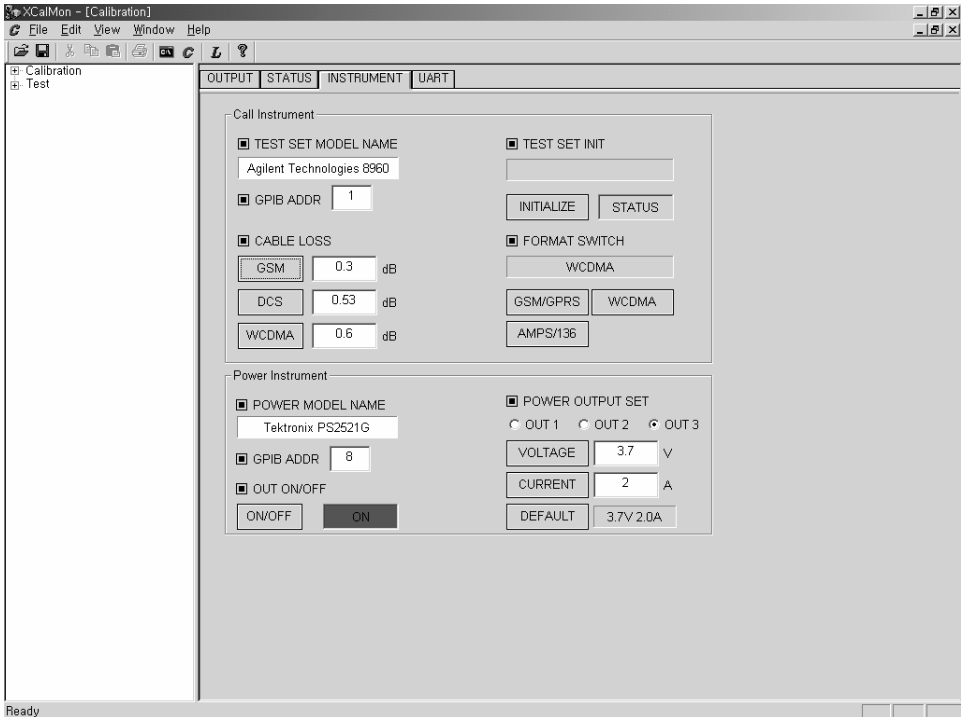


Figure 7-8. XCALMON Calibration Tree Window (INSTRUMENT Tab)

7. CALIBRATION

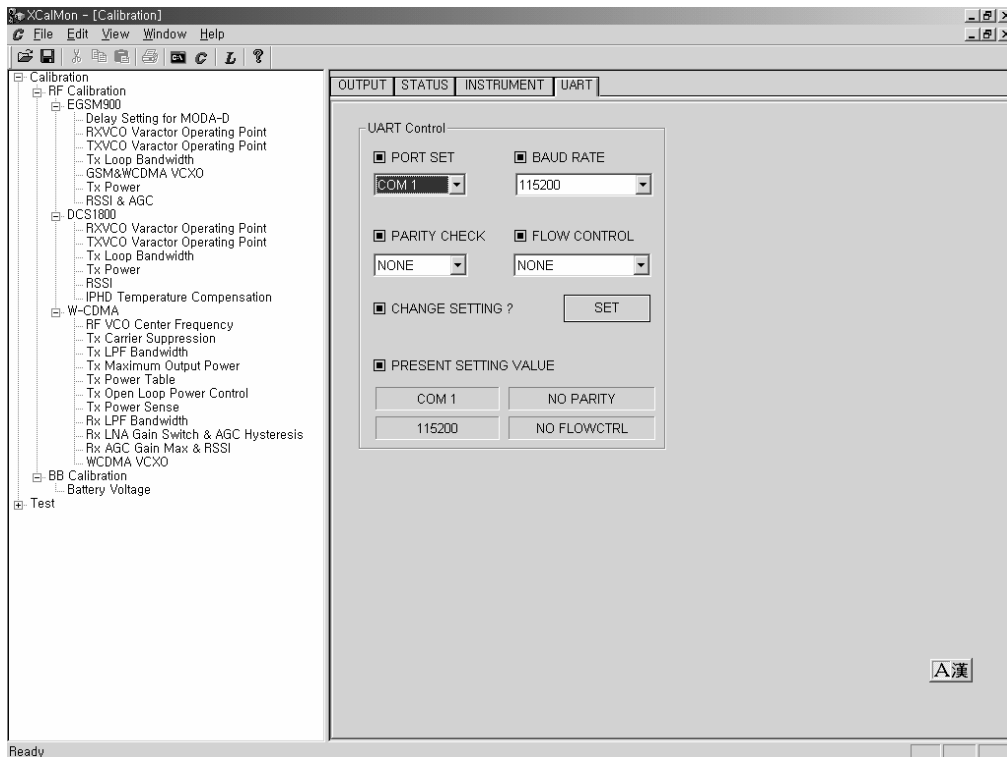


Figure 7-9. XCALMON Calibration Tree Window (UART Tab)

C. ITP Starting Window Using Production Loader

When you click the ITP starting window icon "L", then you should see the ITP starting window. That dialog window just wait for power-on of U8550 mobile phone. When it will occur power-on, it automatically start ITP running.

If you want to change the start address of ITP, you could change that address directly.

To change ITP start address is possible when we download "Production loader" previously.

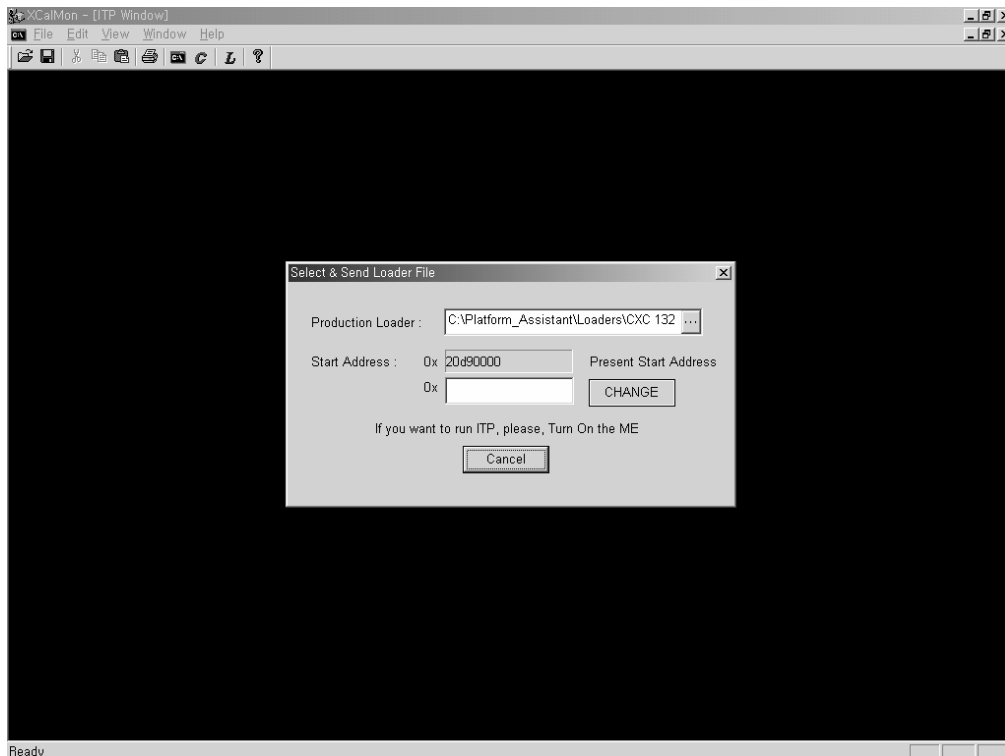


Figure 7-10. XCALMON ITP Starting Window (Using Production Loader)

7.4.3 Calibration Procedure

Calibration procedure of XCALMON was the same as below procedure.

- Configuration of calibration
- Running ITP using production loader
- Calibration start using XCALMON
- Verification of calibration result

A. Configuration of Calibration

Configure to calibrated U8550 mobile phone like Figure7-1. If configuration will be accomplished, start XCALMON program.

B. Running ITP Using Production Loader

If XCALMON will be executed, you should run ITP using “L” ITP starting icon at first.

Click the “L” icon, then you will see the ITP start window like Figure7-10.

When you will turn on the U8550 mobile phone, the production loader will be downloaded automatically like Figure7-11 and then it will execute the ITP at once.

If the ITP will operate normally, you should see the characters “TP, OK” in ITP command window like Figure7-12.

7. CALIBRATION

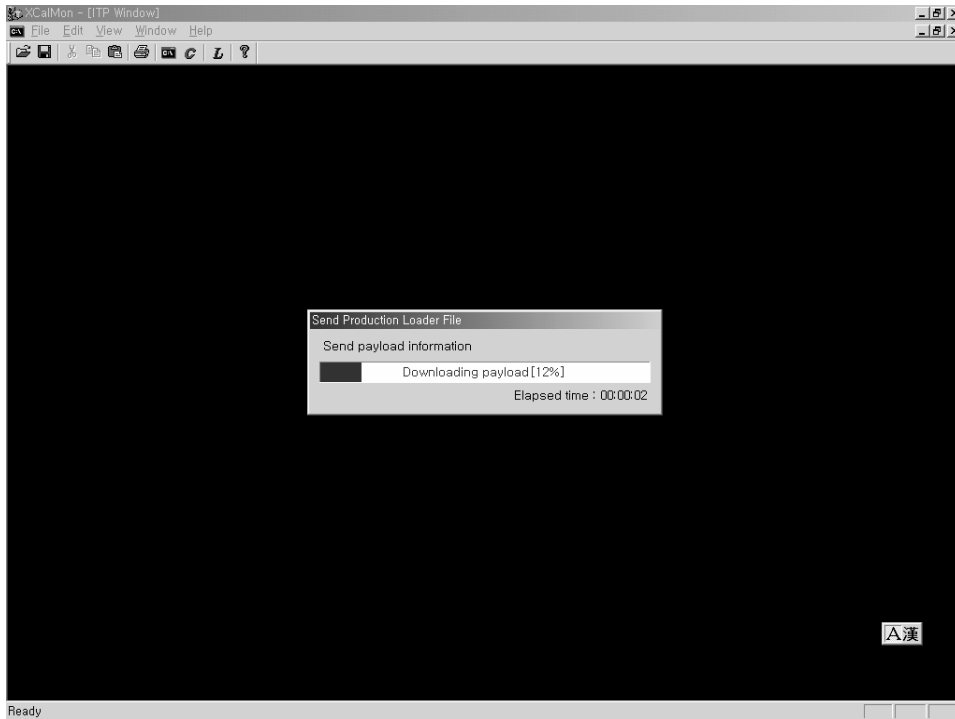


Figure 7-11. Production Loader Downloading

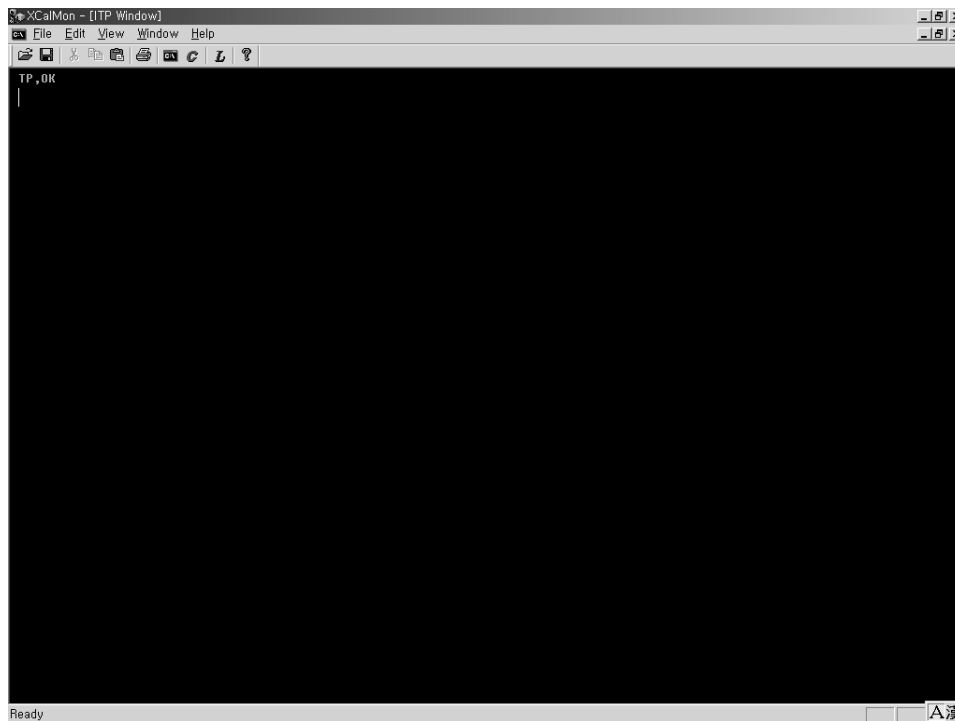


Figure 7-12. ITP Start Complete Window

C. Calibration Start Using XCALMON

If you want to calibrate U8550 mobile phone, click the calibration icon “C”.
And then you will see the calibration tree window like Figure7-6.
To start calibration, you should select “Calibration” item and push “F4” button in your keyboard.

D. Verification of calibration result

If the calibration will be ended, you will see several message window and the result of calibration through OUTPUT & STATUS tab view.
The detail explanation of those will be described in chapter 7.4.4

7.4.4 Calibration Result Message

If the calibration is over without error, “PASS” message window will show up like Figure7-13.
On the contrary, if the calibration is over with some error, “FAIL” message window will show up like Figure7-14. Additionally, in all of the cases, it is possible to check the calibration result with OUTPUT & STATUS tab view.

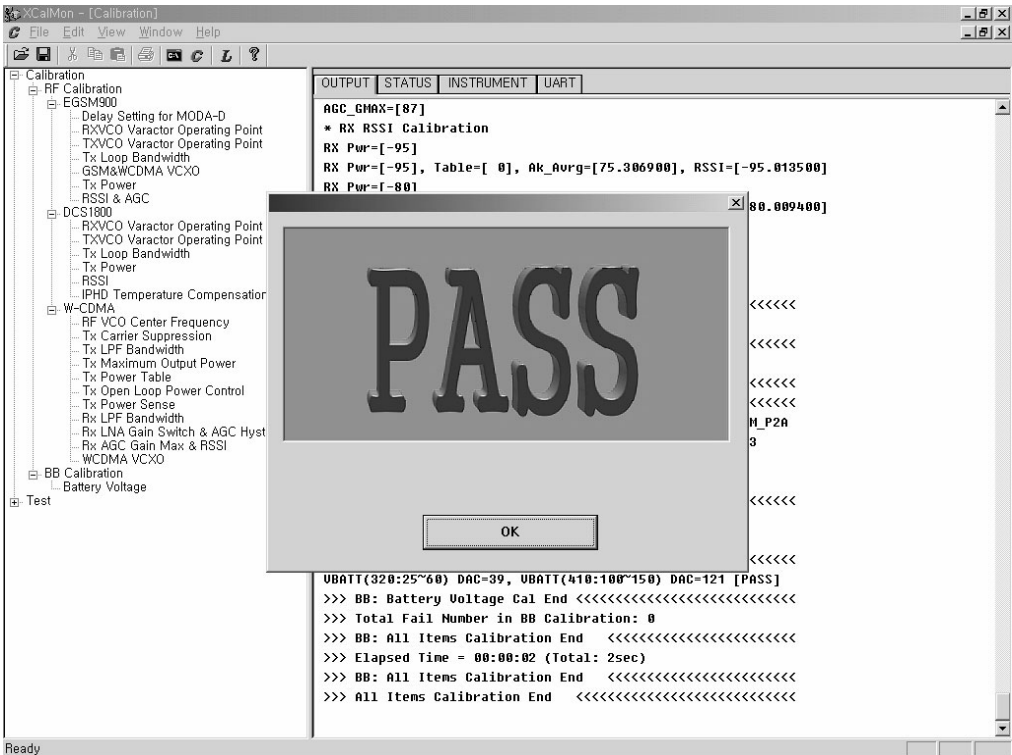


Figure 7-13. Calibration PASS Message Window

7. CALIBRATION

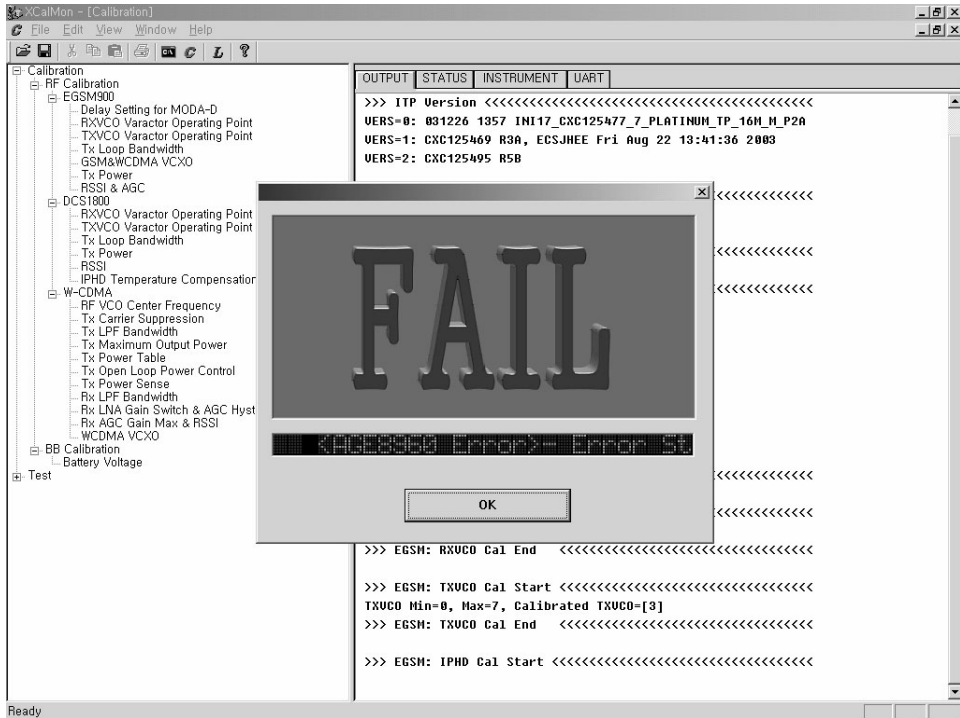


Figure 7-14. Calibration FAIL Message Window

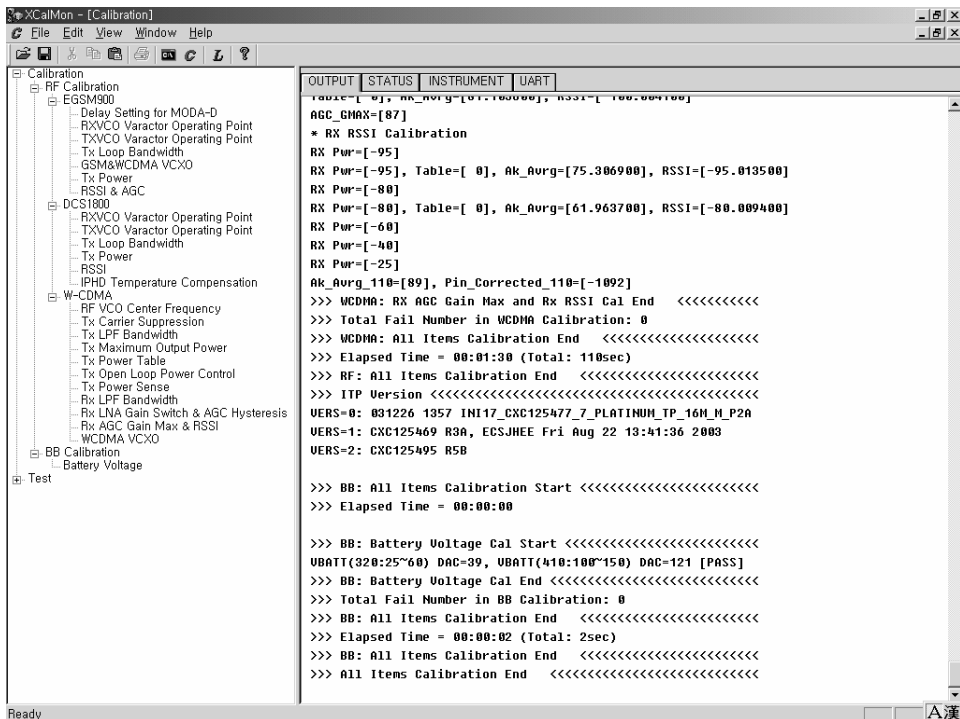
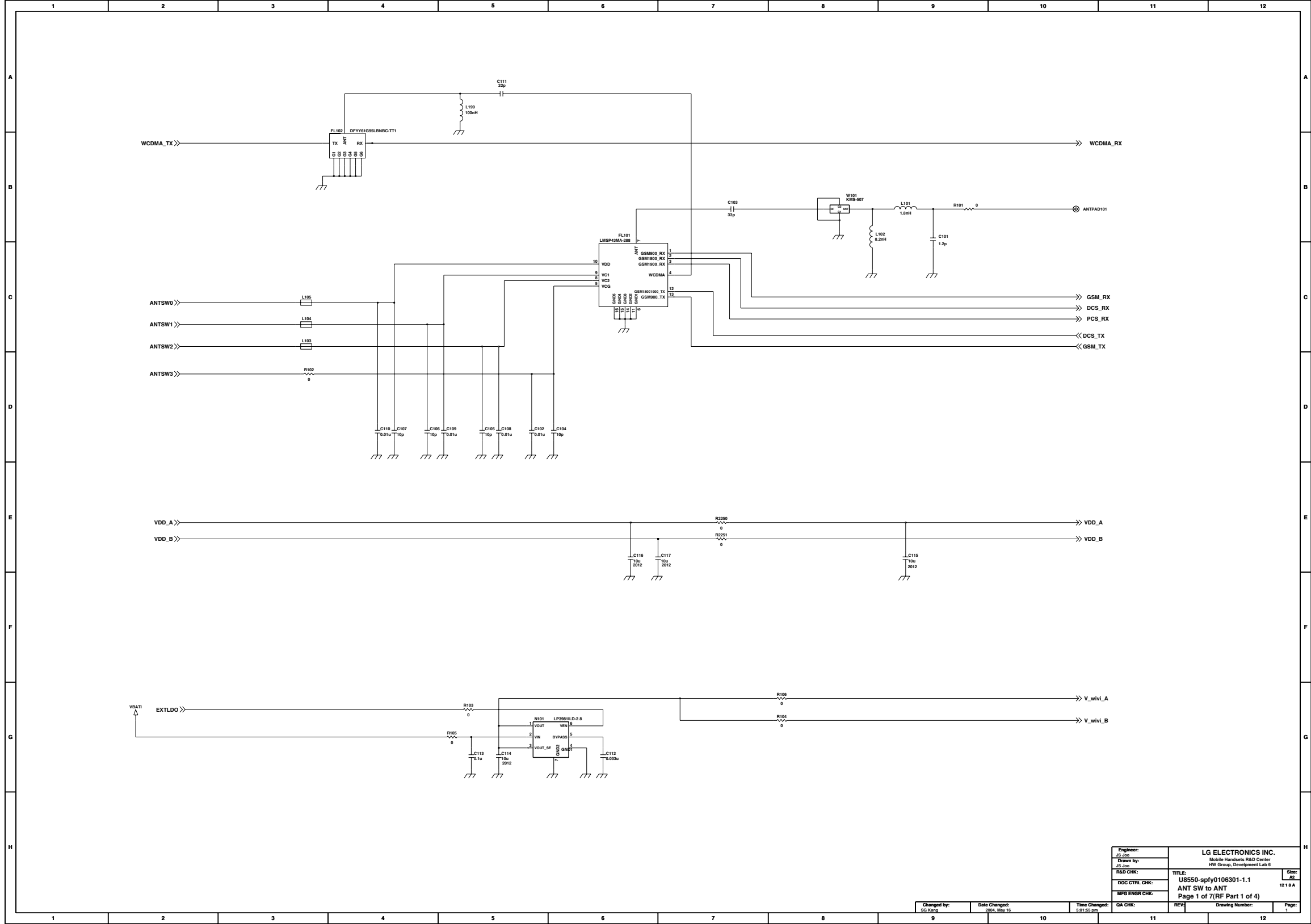


Figure 7-15. Calibration Result from OUTPUT Tab View



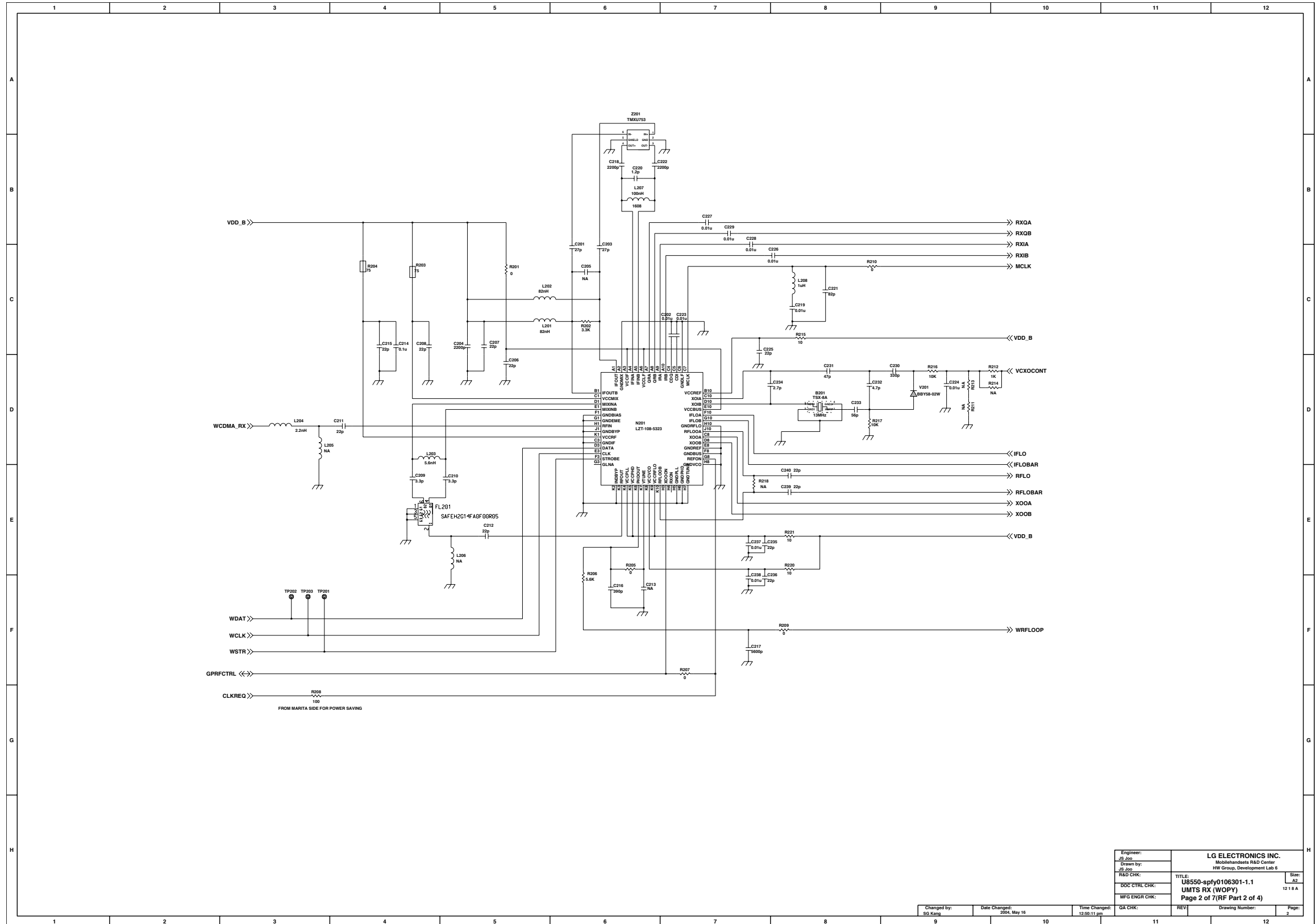
8. CIRCUIT DIAGRAM



Engineer:	LG ELECTRONICS INC.		
Drawn By:	Mobile Handsets R&D Center		
Rev:	HW Group, Development Lab.8		
R&D CHK:	TITLE:	Size:	
DOC CTRL CHK:	U8550-sply0106301-1.1	1214A	
MFG ENGR CHK:	ANT SW to ANT		
	Page 1 of 7(RF Part 1 of 4)		

Changed by:	Date Changed:	Time Changed:	QA CHK:	REV:	Drawing Number:	Page:
SG Kang	2008, May 15	8:01:03 pm				1

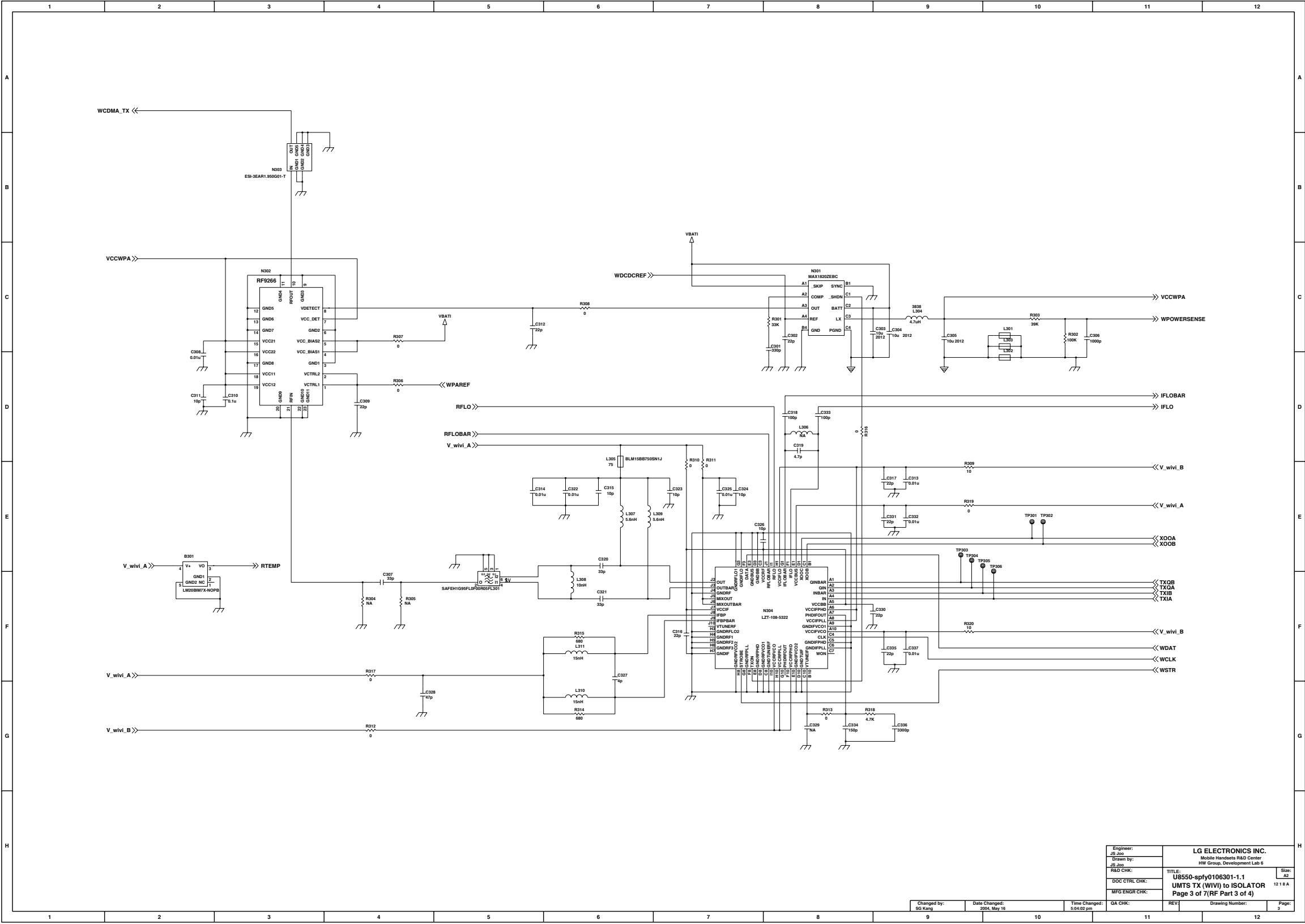
8. CIRCUIT DIAGRAM



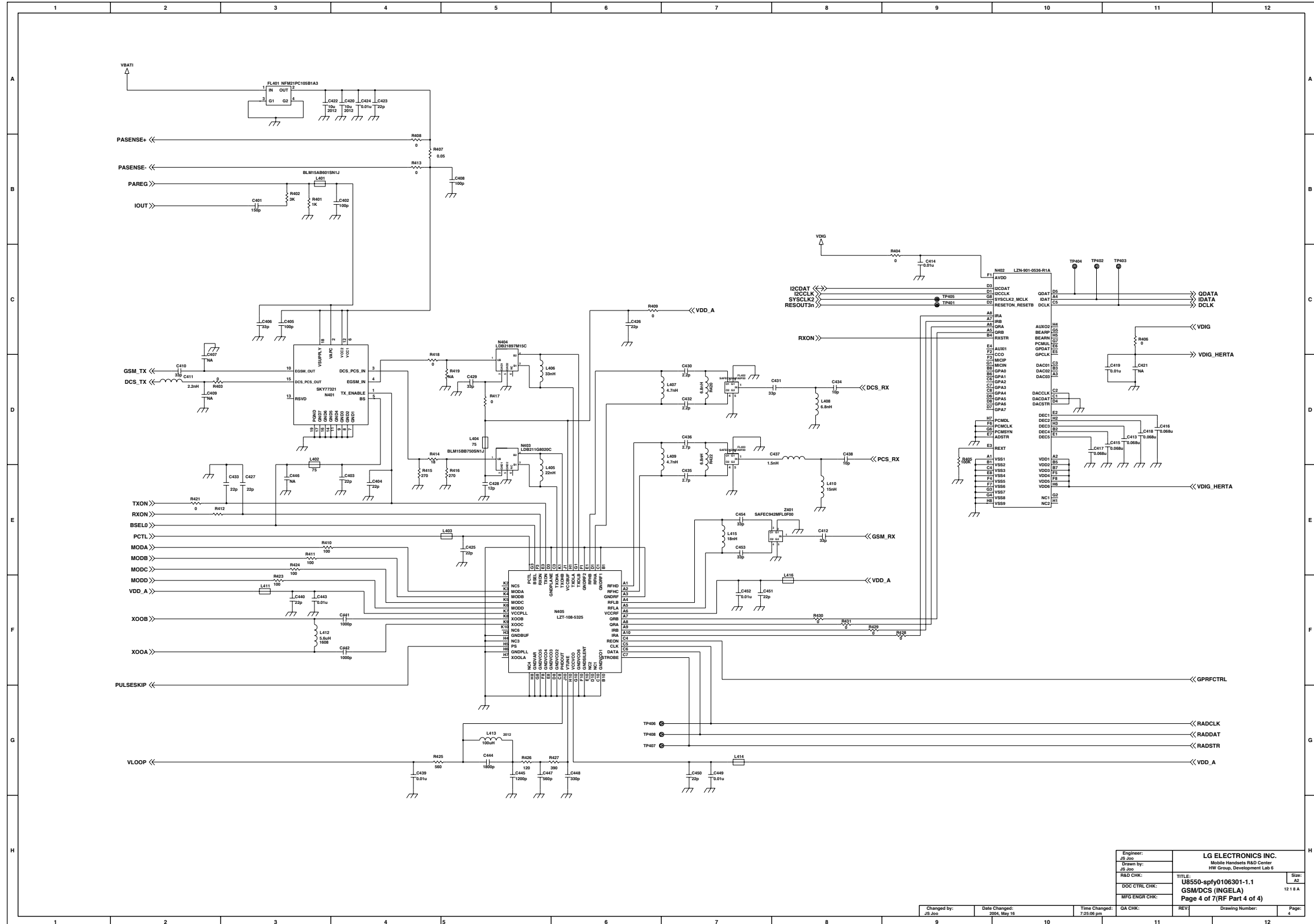
Engineer:	JH_200	LG ELECTRONICS INC.
Drawn by:	JH_200	Mobilehandsets R&D Center
RFID CHK:		HW Group, Development Lab 6
DOC CTRL CHK:		TITLE: U8550-sply0106301-1.1
MFG ENGR CHK:		UMTS RX (WOPY)
		Page 2 of 7(RF Part 2 of 4)

Changed by:	Date Changed:	Time Changed:
SG King	2004 May 16	12:50:11 pm

8. CIRCUIT DIAGRAM

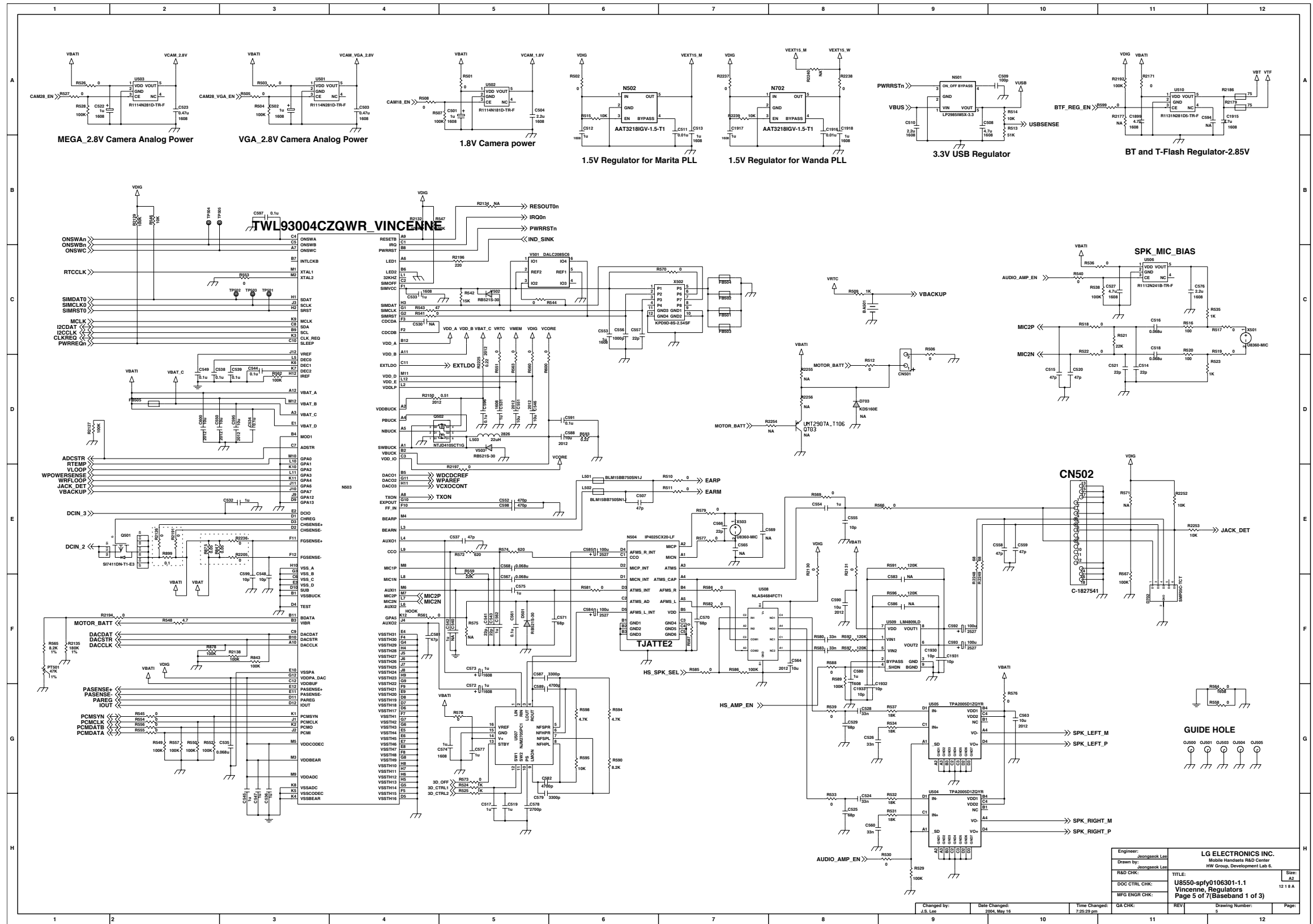


8 CIRCUIT DIAGRAM



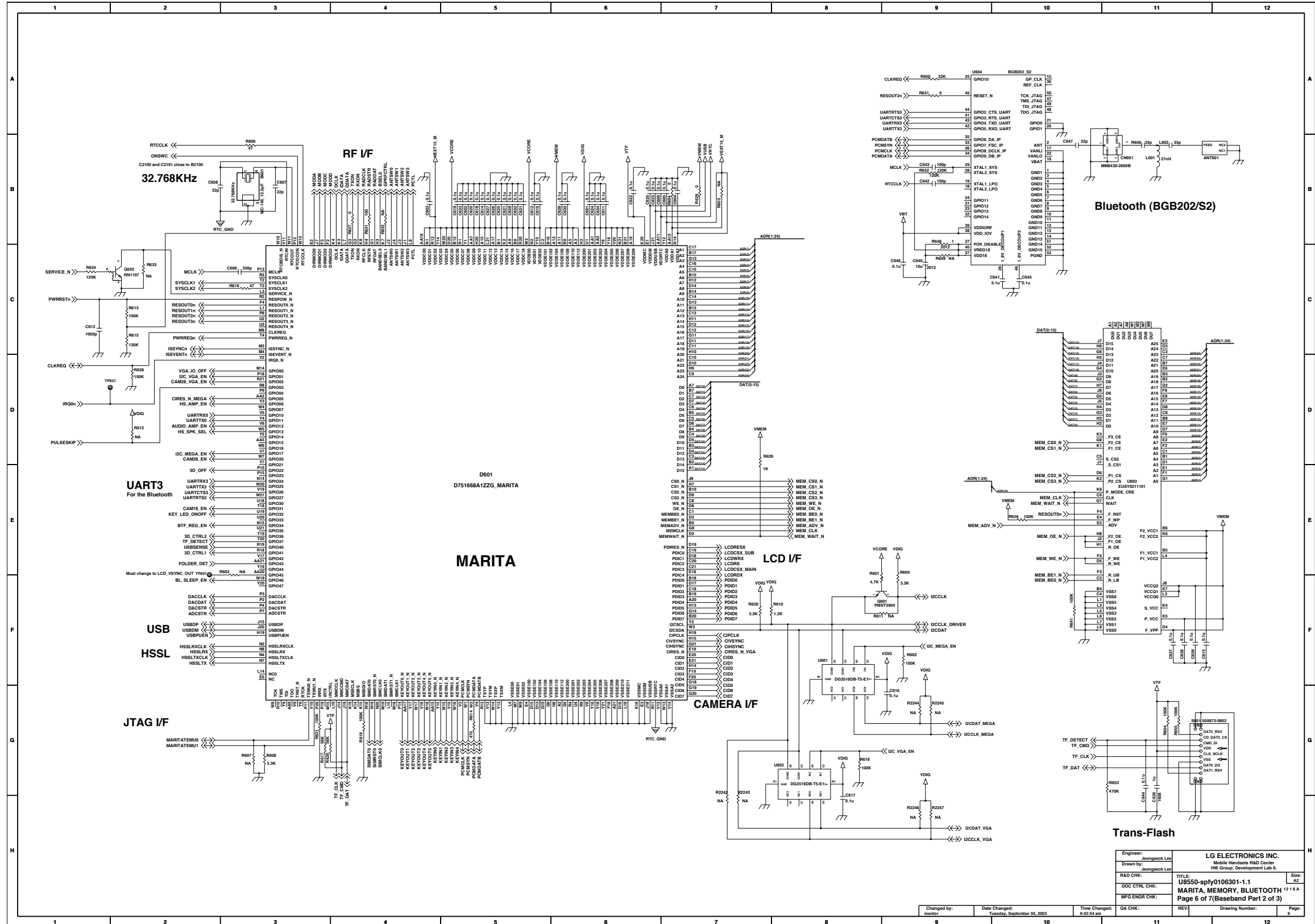
Engineer:	LG ELECTRONICS INC.		
Drawn by:	Mobile Handsets R&D Center		
Drawn by:	HW Group, Development Lab 6		
R&D CHK:	TITLE:	U8550-sply0106301-1.1	Size: 12.1 x A
DDC CTRL CHK:	GSM/DCS (INGELA)		Page 4 of 7 (RF Part 4 of 4)
MFG ENGR CHK:	Page 4 of 7 (RF Part 4 of 4)		
Changed by:	Date Changed:	Time Changed:	QA CHK: REV: Drawing Number: Page:
JR-204	2004, May 18	7:25:05 pm	4

8. CIRCUIT DIAGRAM



Engineer: Jeongeuk Lee	LG ELECTRONICS INC.	
Drawn by: Jeongeuk Lee	Mobile Handsets R&D Center HW Group, Development Lab 6.	
R&D CHK: Jeongeuk Lee	TITLE: U8550-spy0106301-1.1	Size: 12.8 A
DOC CTRL CHK: Jeongeuk Lee	Vincenne_Regulators	
MFG ENGR CHK: Jeongeuk Lee	Page 5 of 7 (Sheetband 1 of 3)	
Changed by: J.S. Lee	Date Changed: 2004_May_16	Time Changed: 7:25:29 pm
QA CHK: Jeongeuk Lee	REV: 5	Drawing Number: 5

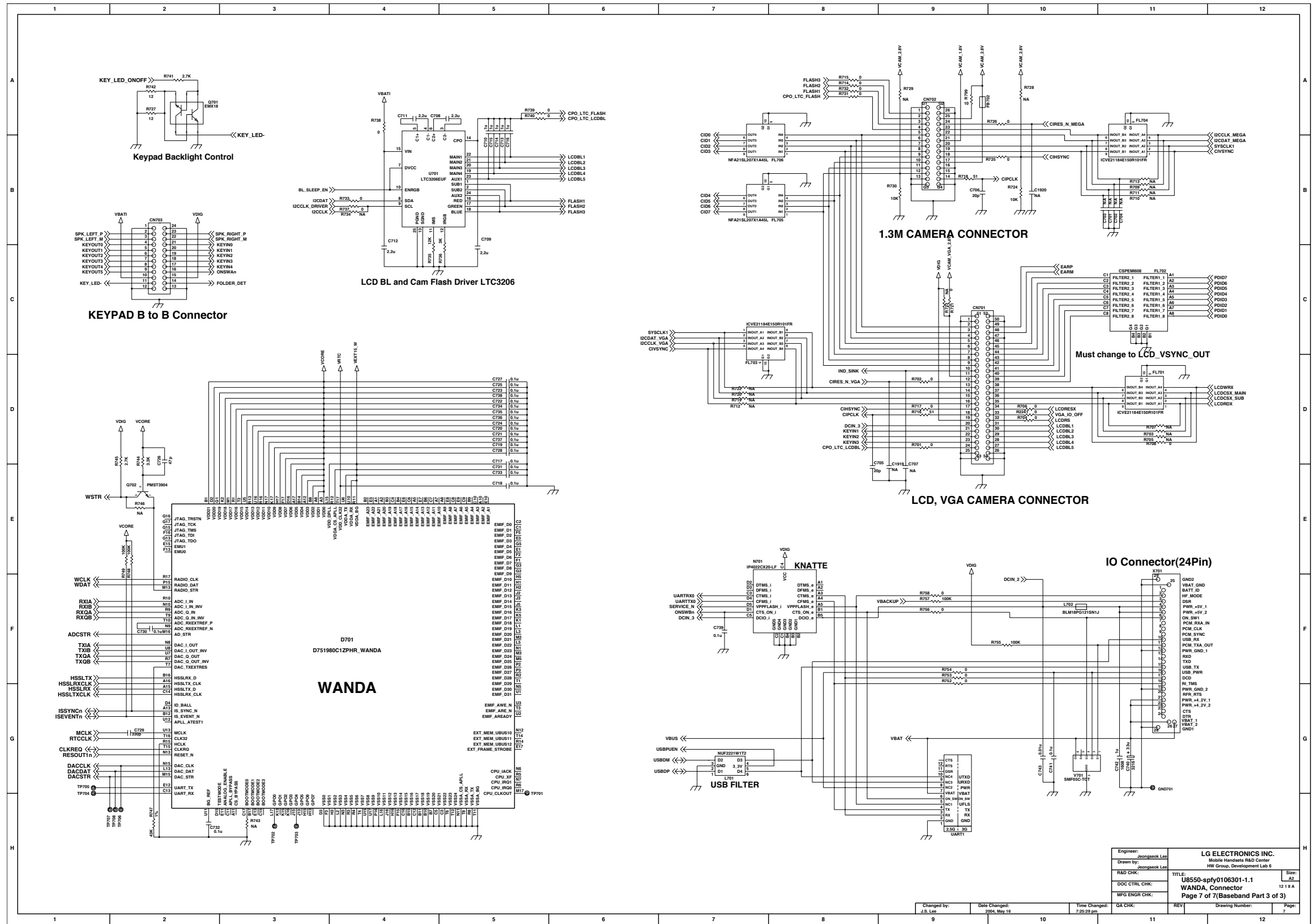
8. CIRCUIT DIAGRAM



Engineer:	Jhongseok Lee	LG ELECTRONICS INC.	
Drawn by:	Jhongseok Lee	Mobile Handsets R&D Center	
R&D CHK:		NW Group, Development Lab. 8	
DOC CTRL CHK:		TITLE:	U8550-spy0106301-1.1
MFG ENGR CHK:		MARITA, MEMORY, BLUETOOTH	
		Page 5 of 7 (Baseband Part 2 of 3)	

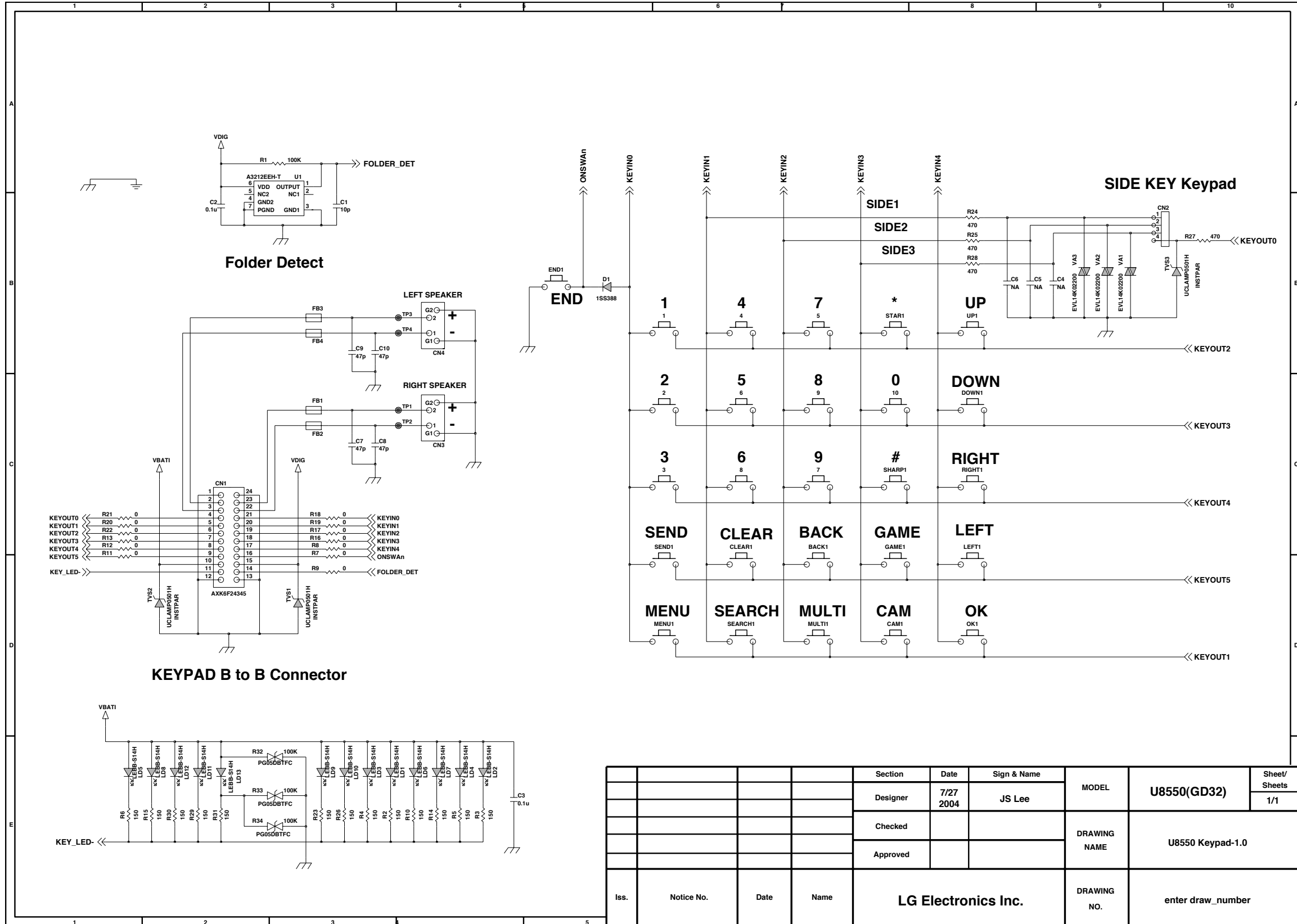
Changed by:	Date Changed:	Time Changed:	GA CHK:	REV:	Drawing Number:	Page:
maniv	Tuesday, September 04, 2003	9:42:54 a.m.				6

8. CIRCUIT DIAGRAM



Engineer: Jeongseok Lee	LG ELECTRONICS INC.	
Drawn by: Jeongseok Lee	Mobile Handsets R&D Center HW Group, Development Lab 6	
R&D CHK: Jeongseok Lee	TITLE: UB850-apply0106301-1.1	Size: A4
DOC CTRL CHK:	WANDA Connector	12 / 8 A
MFG ENGR CHK:	Page 7 of 7(Baseband Part 3 of 3)	
Changed by: J.S. Lee	Date Changed: 2004, May 16	Time Changed: 7:25:29 pm
QA CHK:	REVIEW	Drawing Number: Page: 7

8. CIRCUIT DIAGRAM

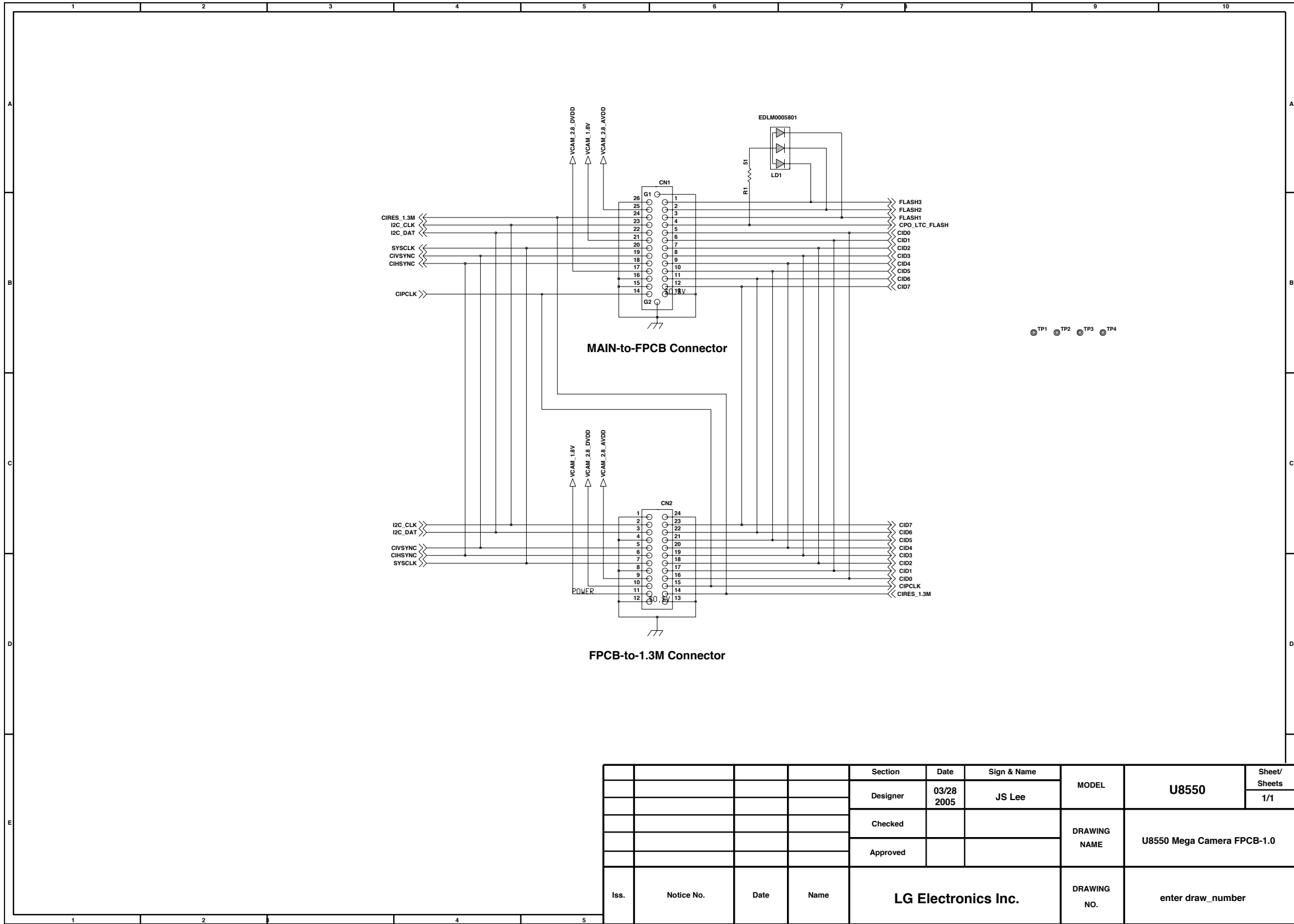


LGIC(42)-A-5505-10:01

LG Electronics Inc.

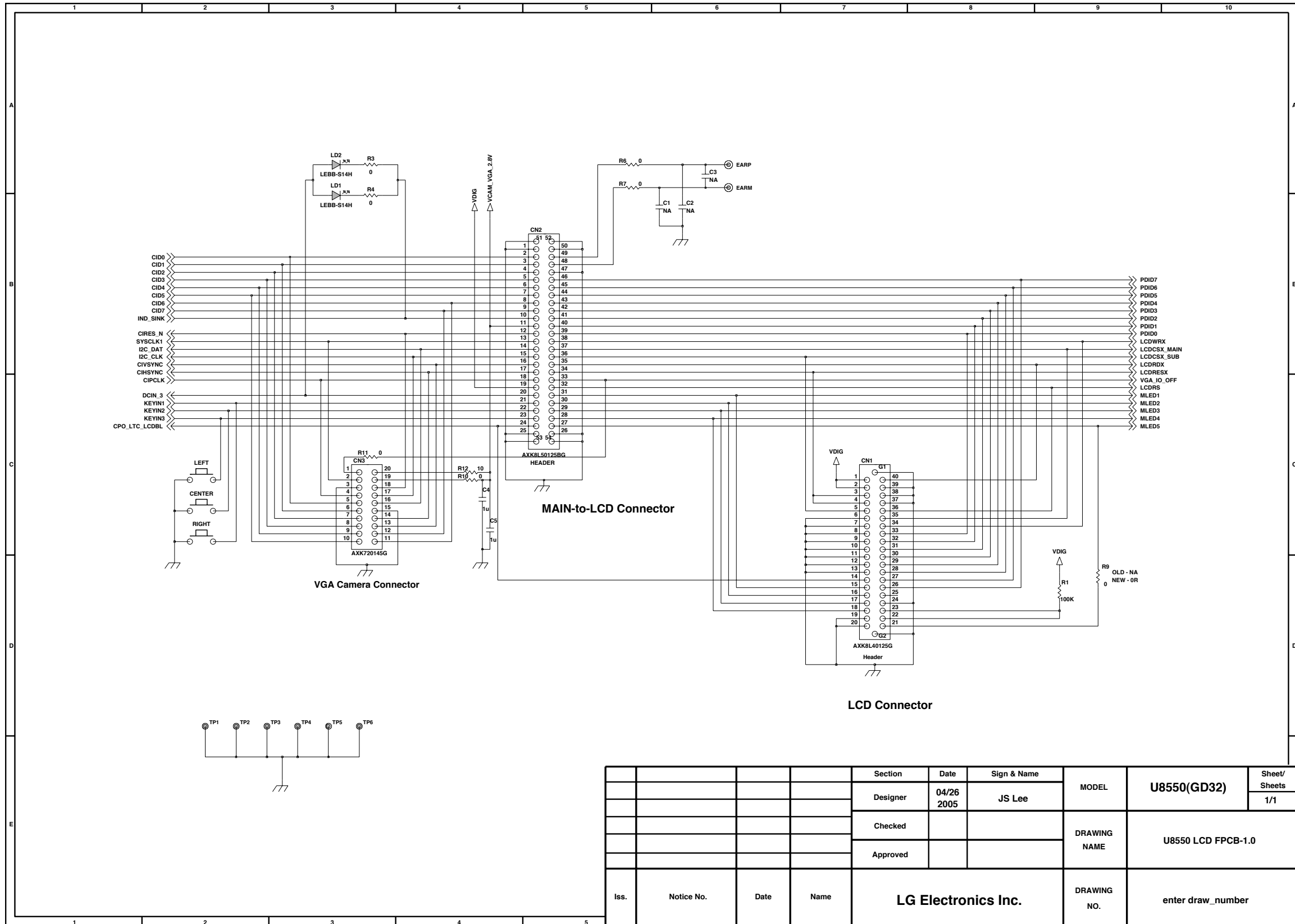
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				Designer	7/27 2004	JS Lee			1/1
				Checked			DRAWING NAME	U8550 Keypad-1.0	
				Approved					
Iss.	Notice No.	Date	Name	LG Electronics Inc.			DRAWING NO.	enter draw_number	

8. CIRCUIT DIAGRAM



				Section	Date	Sign & Name	MODEL	U8550	Sheet/
				Designer	03/28 2005	JS Lee			1/1
				Checked			DRAWING NAME	U8550 Mega Camera FPCB-1.0	
				Approved					
Iss.	Notice No.	Date	Name	LG Electronics Inc.			DRAWING NO.	enter draw_number	

8. CIRCUIT DIAGRAM



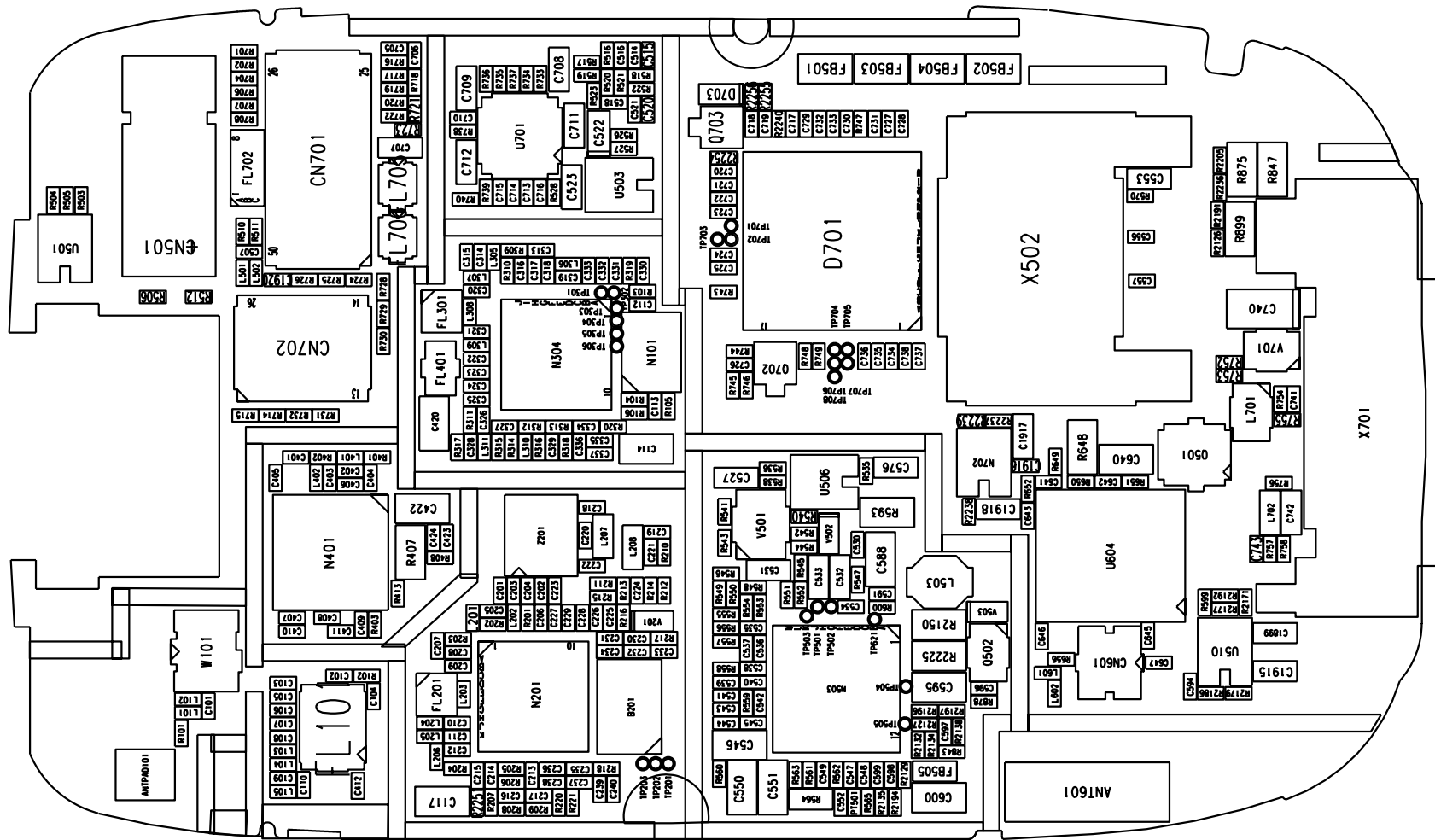
				Section	Date	Sign & Name	MODEL	U8550(GD32)	Sheet/ Sheets
				Designer	04/26 2005	JS Lee			1/1
				Checked			DRAWING NAME	U8550 LCD FPCB-1.0	
				Approved					
Iss.	Notice No.	Date	Name	LG Electronics Inc.			DRAWING NO.	enter draw_number	

9. PCB LAYOUT



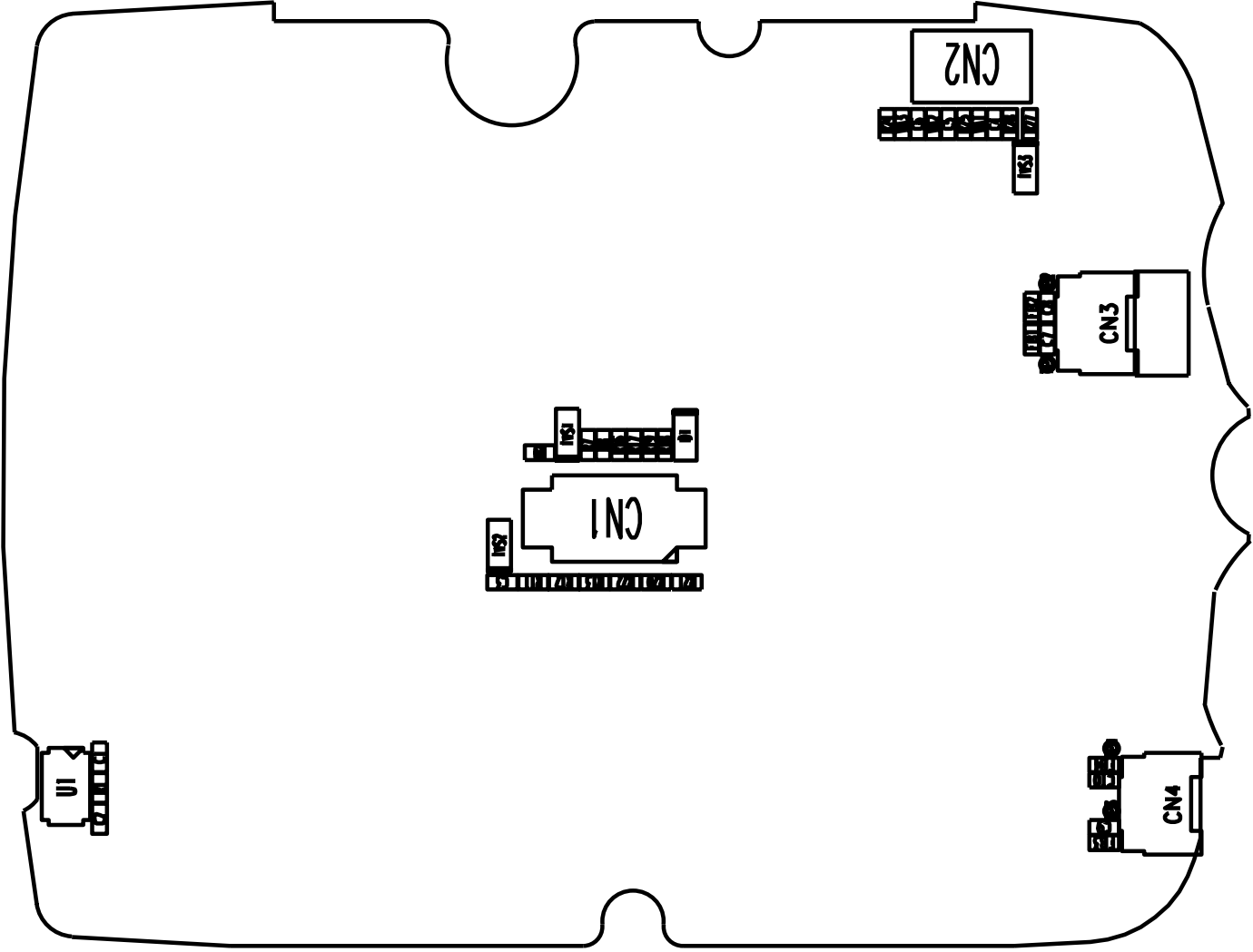
U8550-SPFY0106301-1.1-1-TOP

9. PCB LAYOUT



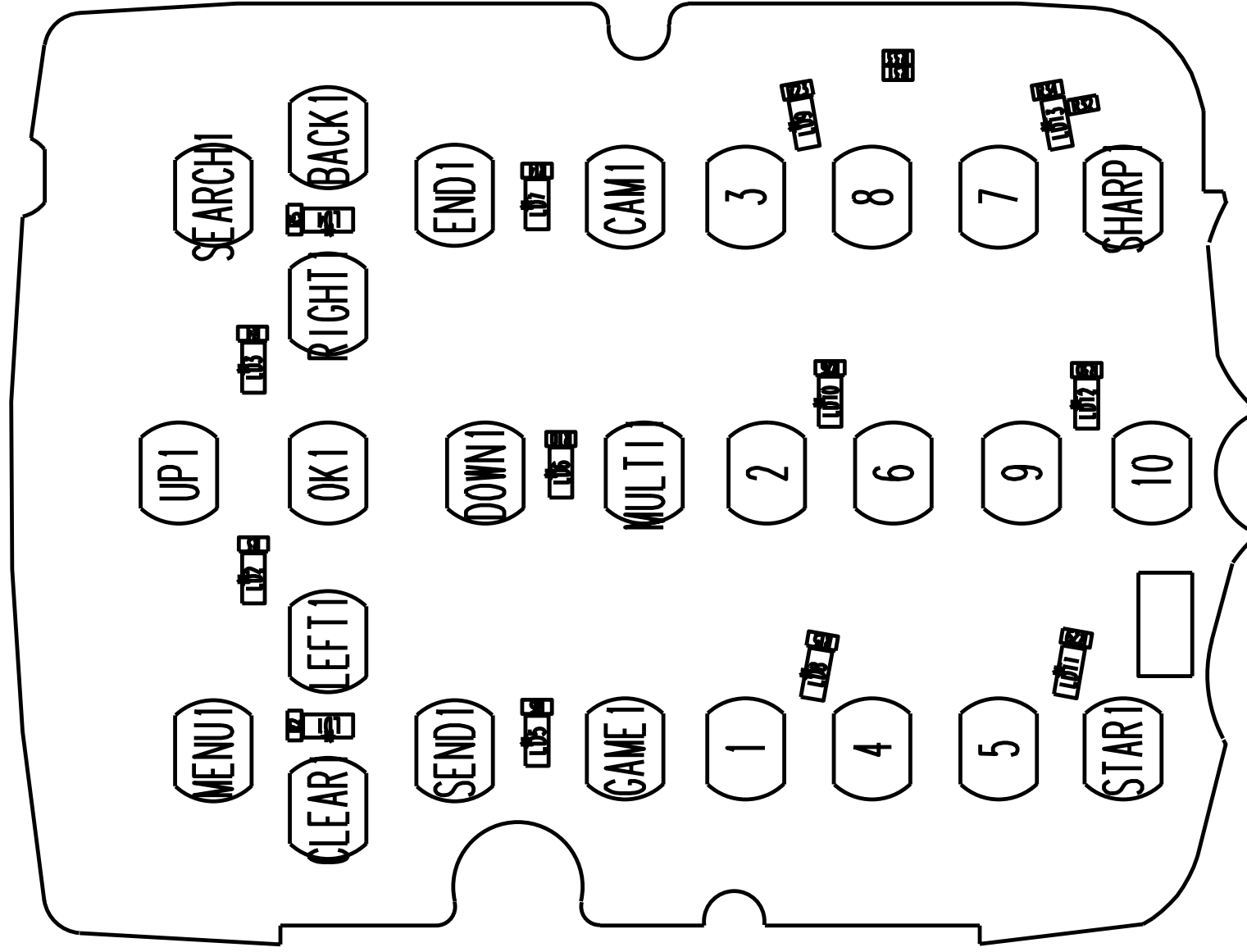
U8550-SPFY0106301-1.1-BTM

9. PCB LAYOUT



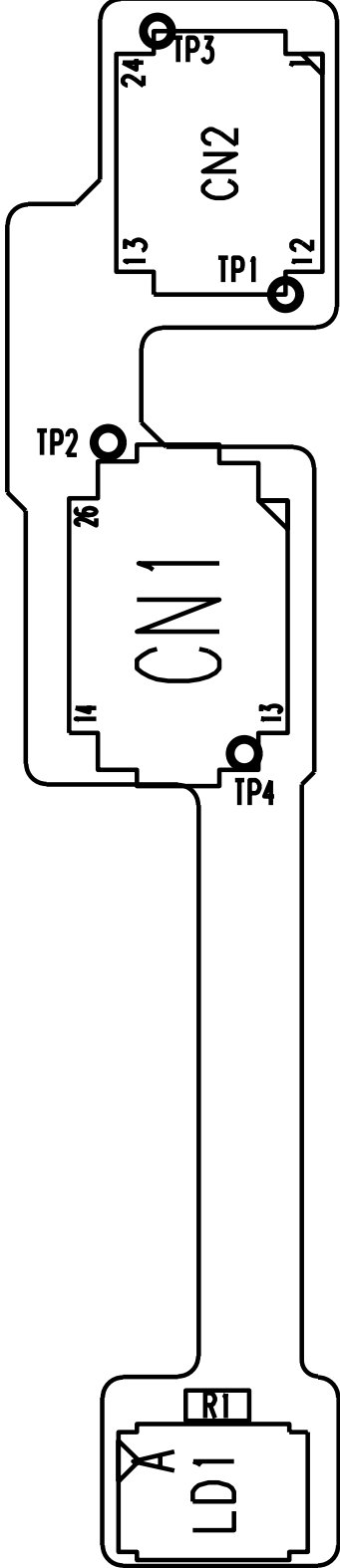
U8550-SPEY0035701-1.0-BTM

9. PCB LAYOUT



U8550-SPEY0035701-1.0-TOP

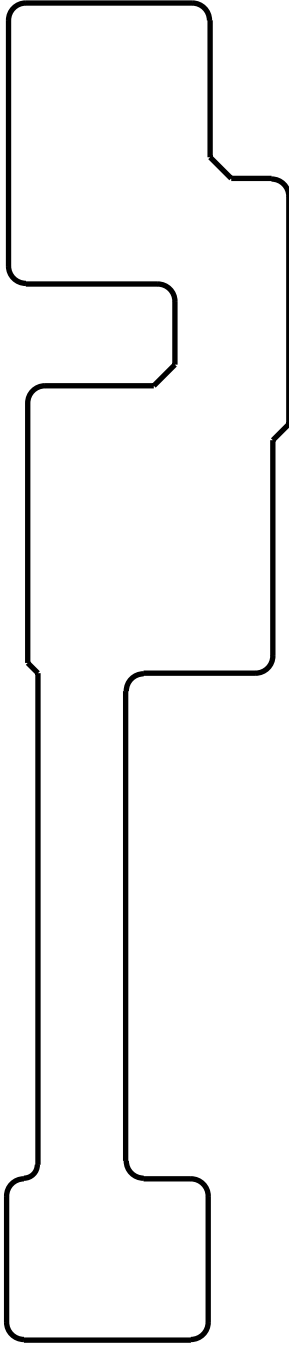
9. PCB LAYOUT



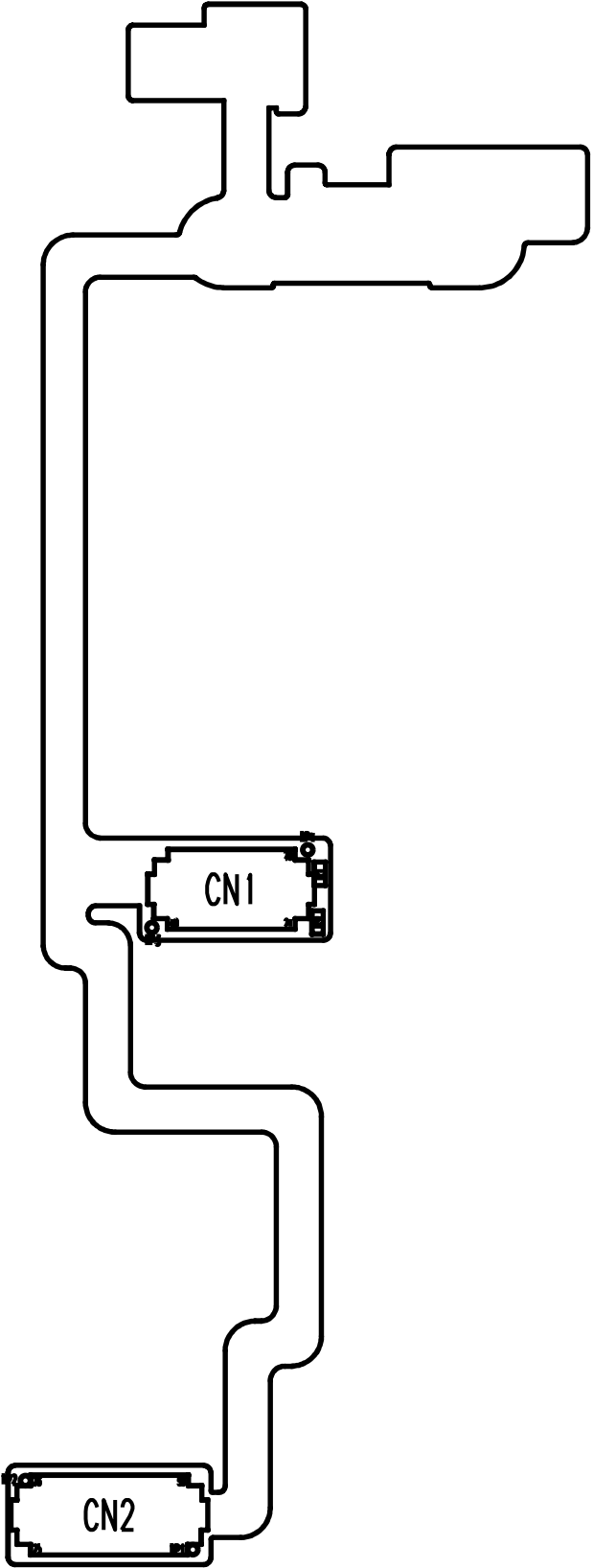
U8550-CAMERA-SPCY0058201-1.0-TOP

9. PCB LAYOUT

U8550-CAMERA-SPCY0058201-1.0-BOTTOM

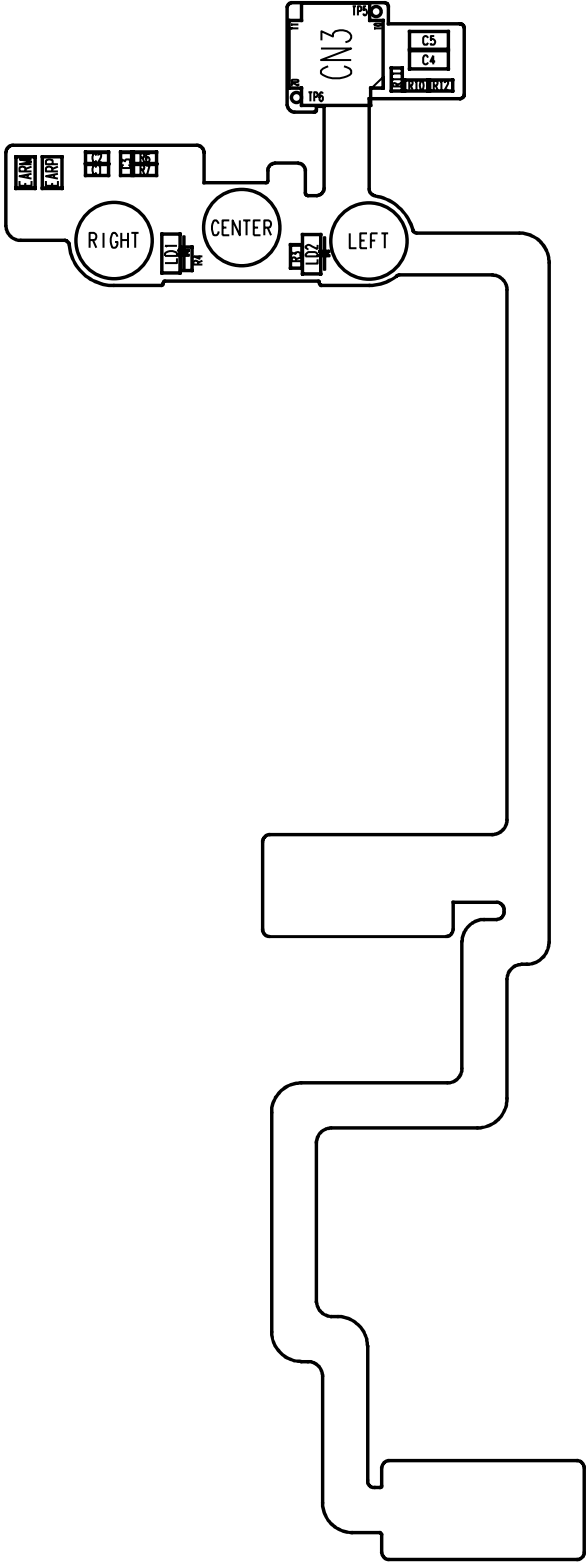


9. PCB LAYOUT



U8550-LCD-FPCB-1.0-TOP

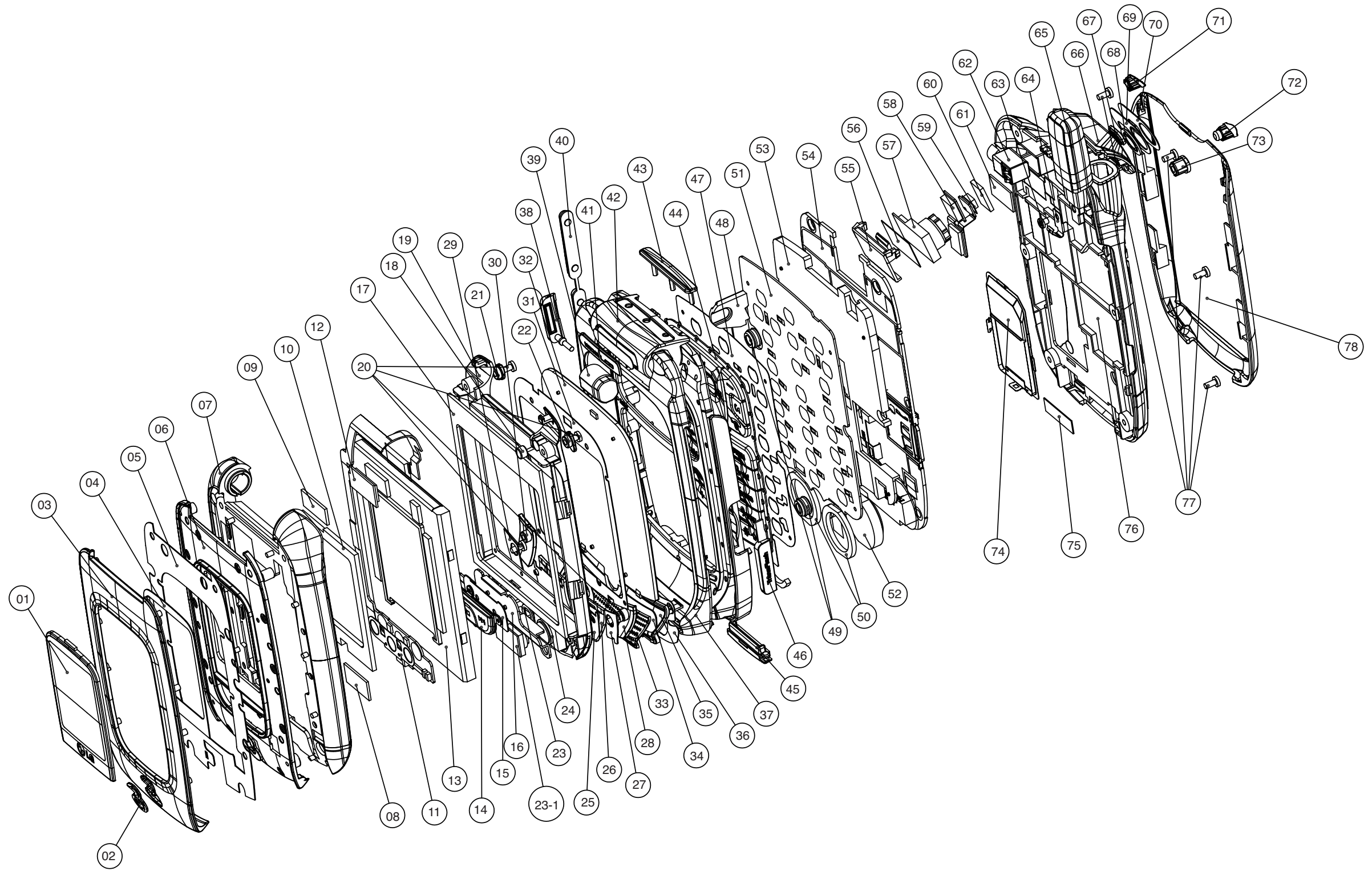
9. PCB LAYOUT



U8550-LCD-FPCB-1.0-BOTTOM

10. EXPLODED VIEW & REPLACEMENT PART LIST

10.1 EXPLODED VIEW



NO	DESCRIPTION	Q'TY	DRAWING NO	REMARK	NO	DESCRIPTION	Q'TY	DRAWING NO	REMARK
1	WINDOW LCD(SUB)	1	AWAZ00071##	01:SILVER, 02:GREEN, 03:ORANGE	40	BUTTON,SIDE	1	MBJL0022901	
2	DECO(3 LOGO)	1	MDAY0006801		41	PLATE,FACE	1	MPFC0070301	
3	DECO FOLDER(UPPER)	1	MDAE00304##	01:SILVER, 02:GREEN, 03:ORANGE	42	COVER,FRONT	1	MCJK00418##	01:SILVER, 02:GREEN, 03:ORANGE
4	TAPE,WINDOW(SUB)	1	MTAE0023901		43	STOPPER	1	MSGY00111##	01:SILVER, 02:GREEN, 03:ORANGE
5	TAPE,DECO	1	MTAA0094701		44	KEYPAD,DIAL	1	MKAA00126##	01:SILVER, 02:GREEN, 03:ORANGE
6	DECO,WINDOW	1	MDAM0006901		45	CAP_RECPTACLE	1	MCCE00212##	01:SILVER, 02:GREEN, 03:ORANGE
7	COVER,FOLDER(UPPER)	1	MCJJ0034201		46	CAP,MULTIMEDIA CARD	1	MCCG00031##	01:SILVER, 02:GREEN, 03:ORANGE
8	PAD,FLEXIBLE FPCB	1	MPBF0012401		47	DOME ASSY,METAL	1	ADCA0035301	
9	GASKET(CINNECTOR)	1	MGAD0096801		48	STPPER,HINGE	1	MSGB0010901	
10	PAD,LCD(SUB)	1	MPBQ0024101		49	MIKE	2	SGEY0003707	
11	DOME ASSY METAL	1	ADCA0035201		50	PAD,SPEAKER	2	MPBN0022601	
12	PCB ASSY,FLEXIBLE(LCD)	1	SACY0038001		51	PCB ASSY,KEYPAD	1	SAEY0044401	
13	LCD MODULE	1	SVLM0015201		52	SPEAKER	2	SUSY0017501	
14	KEYPAD(MOD)	1	MKAZ00233##	01:SILVER, 02:GREEN, 03:ORANGE	53	FRAME,SHILED	1	MFEA0007801	
15	TAPE,BUTTON	1	MTAG0001101		54	PCB ASSY,MAIN	1	SAFY0134601	
16	BRACKET(MOD)	1	MBFZ0022101		55	BRACKET,CAMERA	1	MBFP0003001	
17	PAD,LCD(MAIN)	1	MPBG0034601		56	TAPE(CAMERA MEGA)	1	MTAZ0083001	
18	MAGNET	1	MMAA0001801		57	CAMERA,MEGA	1	SVCY0007701	
19	COVER,FOLDER(LOWER)	1	MCJH0026901		58	PCB ASSY,FLEXIBLE(CAMERA)	1	SACY0038101	
20	SCREW MACHINE,BIND	4	GMEY0009201		59	TAPE(CAMERA FPCB)	1	MTAZ0083201	
21	CAP,SCREW(FOLDER,L,UP)	1	MCCH0054501		60	GASKET(MEGA CAMERA FPCB)	1	MGAD0102701	
22	CAP,SCREW(FOLDER,R,UP)	1	MCCH0054601		61	GASKET(CONNECTOR)	1	MGAD0096701	
23	PAD,CAMERA	1	MPBT0019601		62	VIBRATOR,MOTOR	1	SJMY0007007	
23-1	CAMERA,VGA	1	SVCY0009101		63	SCREW MACHINE,BIND	1	GMEY0009201	
24	RECEIVER	1	SURY0009501		64	CONTACT,ANTENNA	1	MCIA0014801	
25	TAPE,DECO	1	MTAA0094601		65	ANTENNA	1	SNGF00110##	01:GREEN, 02:ORANGE, 03:SILVER
26	DECO,FOLDR(LOWER)	1	MDAF00074##	01:SILVER, 02:GREEN, 03:ORANGE	66	DECO,REAR	1	MDAK00072##	01:SILVER, 02:GREEN, 03:ORANGE
27	TAPE(R,DOWN)	1	MTAZ0086801		67	WINDOW,FLASH	1	MWAH0001601	
28	CAP,SCREW(FOLDER,R,DOWN)	1	MCCH00548##	01:SILVER, 02:GREEN, 03:ORANGE	68	WINDOW,CAMERA	1	MWAE0009301	
29	TAPE(L,DOWN)	1	MTAZ0086901		69	TAPE(DECO CAMERA)	1	MTAA0095201	
30	CAP,SCREW(FOLDER,L,DOWN)	1	MCCH00547##	01:SILVER, 02:GREEN, 03:ORANGE	70	DECO,CAMERA	1	MDAD00130##	01:SILVER, 02:GREEN, 03:ORANGE
31	TAPE,WINDOW(MAIN)	1	MTAD0037101		71	CAP,SCREW(MAIN,L)	1	MCCH0054901	
32	WINDOW,LCD(MAIN)	1	AWAB00183##	01:SILVER, 02:GREEN, 03:ORANGE	72	CAP,SCREW(MAIN,R)	1	MCCH0055001	
33	DECO,SPEAKER	1	MDAN00068##	01:SILVER, 02:GREEN, 03:ORANGE	73	CAP,MOBILE SWITCH	1	MCCF0030501	
34	TAPE(DECO SPEAKER)	1	MTAA0094901		74	HOLDER,CARD	1	MHGB0001401	
35	BRACKET,SPEAKER	1	MBFK0001901		75	GASKET(REAR)	1	MGAD0096901	
36	TAPE(BRACKET SPEAKER)	1	MTAA0094801		76	COVER,REAR	1	MCJN0037501	
37	DECO,FRONT	1	MDAG0012501		77	SCREW MACHINE,BIND	6	GMEY0009201	
38	CAP,EARPHONE JACK	1	MCCC00252##	01:SILVER, 02:GREEN, 03:ORANGE					
39	HINGE,FOLDER	1	MHFD0011201						

10. EXPLODED VIEW & REPLACEMENT PART LIST

10.2 Replacement Parts <Mechanic component>

Note: This Chapter is used for reference, Part order is ordered by SBOM standard on GCSC

Level	Location No.	Description	Part Number	Specification	Color	Remark
1		IMT,FOLDER	TIFF0009903		Green	
2	AAAY00	ADDITION	AAAY0128401		Green	
3	MCJA00	COVER,BATTERY	MCJA0021801	PC, UV SPRAY	White	
2	APEY00	PHONE	APEY0224002	GREEN COLOR	Green	
3	ACGG00	COVER ASSY,FOLDER	ACGG0061902		Green	
4	ABFZ00	BRACKET ASSY	ABFZ0005801	MOD BUTTON SUPPORT BRACKET ASS'Y	Without Color	
5	MBFZ00	BRACKET	MBFZ0022101	SUS 0.5T PRESS, NON-COATING	Without Color	16
5	MTAZ00	TAPE	MTAZ0083301		Without Color	
4	ACGH00	COVER ASSY, FOLDER(LOWER)	ACGH0035502		Green	
5	MCJH00	COVER,FOLDER(LOWER)	MCJH0026901	PC, UV,	Silver	19
5	MDAF00	DECO,FOLDER(LOWER)	MDAF0007402		Green	26
5	MFBB00	FILTER,RECEIVER	MFBB0012601		Black	
5	MMAA00	MAGNET,SWITCH	MMAA0001801	DIA3.0x2.0t	Without Color	18
5	MPBG00	PAD,LCD	MPBG0034601	MAIN LCD PAD	Without Color	17
5	MPBT00	PAD,CAMERA	MPBT0019601		Black	23
5	MTAA00	TAPE,DECO	MTAA0094601		Without Color	25
5	MTAD00	TAPE,WINDOW	MTAD0037101	0.15T	Without Color	31
5	MTAZ00	TAPE	MTAZ0086801		Without Color	27
5	MTAZ01	TAPE	MTAZ0086901		Without Color	29
4	ACGJ00	COVER ASSY, FOLDER(UPPER)	ACGJ0046802		Green	
5	MCJJ00	COVER,FOLDER(UPPER)	MCJJ0034201		Silver	7
5	MDAE00	DECO,FOLDER(UPPER)	MDAE0030402		Green	3
5	MDAM00	DECO,WINDOW(SUB)	MDAM0006901	AL DICASTING	Silver	6
5	MDAY00	DECO	MDAY0006801	0.2t	Without Color	2
5	MGAD00	GASKET,SHIELD FORM	MGAD0096801	LCD LEFT	BROWN GOLD	9

10. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	Part Number	Specification	Color	Remark
5	MGAD01	GASKET,SHIELD FORM	MGAD0097801	LCD-UPPER CONTACT, 2POINT	Without Color	
5	MKAZ00	KEYPAD	MKAZ0023302		Green	14
5	MPBF00	PAD,FLEXIBLE PCB	MPBF0012401		Black	8
5	MPBQ00	PAD,LCD(SUB)	MPBQ0024101		Black	10
5	MTAA00	TAPE,DECO	MTAA0094701		Without Color	5
5	MTAE00	TAPE,WINDOW(SUB)	MTAE0023901		Without Color	4
5	MTAG00	TAPE,BUTTON	MTAG0001101	MOD KEY FIX TAPE	Without Color	15
4	ACGK00	COVER ASSY,FRONT	ACGK0056402		Green	
5	MBFK00	BRACKET,SPEAKER	MBFK0001901	CHROME PLATING	Without Color	35
5	MBJL00	BUTTON,SIDE	MBJL0022901	ABS+URETHANE CHROME PLATING	Without Color	40
5	MCCC00	CAP,EARPHONE JACK	MCCC0025202	PC+URETHANE UV COATING	Green	38
5	MCCE00	CAP,RECEPTACLE	MCCE0021202	URETHANE SPRAY	Green	45
5	MCCG00	CAP,MULTIMEDIA CARD	MCCG0003102	PC+URETHANE UV COATING	Green	46
5	MCJK00	COVER,FRONT	MCJK0041802		Green	42
5	MDAG00	DECO,FRONT	MDAG0012501	PC,UV	Without Color	37
5	MDAN00	DECO,SPEAKER	MDAN0006802		Green	33
5	MPBN00	PAD,SPEAKER	MPBN0022601		Black	50
5	MPFC00	PLATE,FACE	MPFC0070301	SUS 0.2T	Without Color	41
5	MSGY00	STOPPER	MSGY0011102		Green	43
5	MTAA00	TAPE,DECO	MTAA0094801		Without Color	36
5	MTAA01	TAPE,DECO	MTAA0094901		Without Color	34
5	MTAA02	TAPE,DECO	MTAA0095001		Without Color	
4	AWAB00	WINDOW ASSY,LCD	AWAB0018302	MAIN LCD INMOLD WINDOW	Green	32
5	BFAA00	FILM,INMOLD	BFAA0032102	BLACK	Black	
5	MWAC00	WINDOW,LCD	MWAC0054301	PMMA, INMOLD	Without Color	
4	AWAZ00	WINDOW ASSY	AWAZ0007102	SUB WINDOW	Green	1
5	BFAA00	FILM,INMOLD	BFAA0029201	A	Transparent	
5	MWAF00	WINDOW,LCD(SUB)	MWAF0027901	PMMA, TRANSPARENT INMOLD + SILK	Silver	
4	GMEY00	SCREW MACHINE,BIND	GMEY0009201	1.4 mm,3.5 mm,MSWR3(BK) ,B ,+ ,HEAD D=2.7mm	Black	20,63,77

10. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	Part Number	Specification	Color	Remark
4	MCCH00	CAP,SCREW	MCCH0054501	SILICON RUBBER, FOLDER LIGHT	Gray	21
4	MCCH01	CAP,SCREW	MCCH0054601	SILICON RUBBER, FOLDER LEFT	Gray	22
4	MCCH02	CAP,SCREW	MCCH0054702		Green	30
4	MCCH03	CAP,SCREW	MCCH0054802		Green	28
4	MGAZ01	GASKET	MGAZ0022702		Gold	
4	MGAZ02	GASKET	MGAZ0022703		Gold	
4	MGAZ04	GASKET	MGAZ0022701		Gold	
4	MHFD00	HINGE,FOLDER	MHFD0011201		Without Color	39
4	MIDZ00	INSULATOR	MIDZ0056801		Without Color	
4	MIDZ02	INSULATOR	MIDZ0075001		Without Color	
4	MKAA00	KEYPAD,DIAL	MKAA0012602		Green	44
4	MLAC00	LABEL,BARCODE	MLAC0003401	EZ LOOKS(user for mechanical)	Without Color	
4	MSGB00	STOPPER,HINGE	MSGB0010901	PC	Without Color	48
4	MTAB00	TAPE,PROTECTION	MTAB0084901		Without Color	
4	MTAB01	TAPE,PROTECTION	MTAB0085001		Without Color	
6	ADCA00	DOME ASSY,METAL	ADCA0035201	FOLDER MOD BUTTON DOME ASSY	Without Color	11
3	ACGM00	COVER ASSY,REAR	ACGM0059602	REAR+CAMERA WINDOW ASS'Y	Green	
4	GMEY00	SCREW MACHINE,BIND	GMEY0009201	1.4 mm,3.5 mm,MSWR3(BK) ,B ,+ ,HEAD D=2.7mm	Black	20,63,77
4	MCCZ00	CAP	MCCZ0008903		White	
4	MCIA00	CONTACT,ANTENNA	MCIA0014801	PRESS, 0.15T	Gold	64
4	MCJN00	COVER,REAR	MCJN0037501	PC, UV	White	76
4	MDAD00	DECO,CAMERA	MDAD0013002		Green	70
4	MDAK00	DECO,REAR	MDAK0007202		Green	66
4	MGAD00	GASKET,SHIELD FORM	MGAD0096701	MAIN CONNECTOR	BROWN GOLD	61
4	MGAD01	GASKET,SHIELD FORM	MGAD0096901	LCD RIGHT	BROWN GOLD	75
4	MHGB00	HOLDER,CARD	MHGB0001401		Without Color	74
4	MLAB00	LABEL,A/S	MLAB0000601	HUMIDITY STICKER	Without Color	
4	MLAN00	LABEL,QUALCOMM	MLAN0000601	Black,95C	Transparent	
4	MPBT00	PAD,CAMERA	MPBT0019701		Black	

10. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	Part Number	Specification	Color	Remark
4	MPBZ00	PAD	MPBZ0101301		Black	
4	MTAA00	TAPE,DECO	MTAA0095101		Without Color	
4	MTAA01	TAPE,DECO	MTAA0095201		Without Color	69
4	MTAB00	TAPE,PROTECTION	MTAB0089201		Without Color	
4	MTAB01	TAPE,PROTECTION	MTAB0089301		Without Color	
4	MWAE00	WINDOW,CAMERA	MWAE0009301	0.8T, PMMA SHEET	Without Color	68
4	MWAH00	WINDOW,FLASH	MWAH0001601	PMMA	Transparent	67
4	SJMY00	VIBRATOR,MOTOR	SJMY0007007	3 V, .08 A,5*12.4 ,Cylinder Motor		62
3	ACGN00	COVER ASSY,CAMERA	ACGN0004501	CAMERA + BRACKET ASS'Y	Without Color	
4	ABFZ00	BRACKET ASSY	ABFZ0005701	MEGA CAMERA BRACKET ASS'Y	Without Color	
5	MBFP00	BRACKET,CAMERA	MBFP0003001	PC	Without Color	55
5	MTAZ00	TAPE	MTAZ0083001		Without Color	56
5	MTAZ01	TAPE	MTAZ0083201		Without Color	59
4	MGAD00	GASKET,SHIELD FORM	MGAD0102701		Without Color	60
3	GMEY00	SCREW MACHINE,BIND	GMEY0009201	1.4 mm,3.5 mm,MSWR3(BK) ,B ,+ ,HEAD D=2.7mm	Black	20,63,77
3	MCCF00	CAP,MOBILE SWITCH	MCCF0030501		White	73
3	MCCH00	CAP,SCREW	MCCH0054901	SILICON RUBBER, MAIN LEFT	White	71
3	MCCH01	CAP,SCREW	MCCH0055001	SILICON RUBBER, MAIN RIGHT	White	72
3	MFEA00	FRAME,SHIELD	MFEA0007801	PC	Without Color	53
3	MLAK00	LABEL,MODEL	MLAK0009001		Without Color	
5	ADCA00	DOME ASSY,METAL	ADCA0035301	MAIN BUTTON DOME ASSY	Without Color	47
5	MGAZ00	GASKET	MGAZ0022901		Gold	
5	MLAB00	LABEL,/A/S	MLAB0000601	HUMIDITY STICKER	Without Color	
5	MLAC00	LABEL,BARCODE	MLAC0003401	EZ LOOKS(user for mechanical)	Without Color	

10. EXPLODED VIEW & REPLACEMENT PART LIST

10.2 Replacement Parts <Main component>

Note: This Chapter is used for reference, Part order is ordered by SBOM standard on GCSC

Level	Location No.	Description	Part Number	Specification	Color	Remark
4	SACY00	PCB ASSY,FLEXIBLE	SACY0038001		Silver	12
5	SACB00	PCB ASSY, FLEXIBLE,INSERT	SACB0025501		Green	
5	SACE00	PCB ASSY,FLEXIBLE,SMT	SACE0033801		Silver	
6	SACC00	PCB ASSY,FLEXIBLE,SMT BOTTOM	SACC0018001		Silver	
7	C4	CAP,CERAMIC,CHIP	ECCH0000276	1 uF,10V,Z,Y5V,HD,1608,R/TP		
7	C5	CAP,CERAMIC,CHIP	ECCH0000276	1 uF,10V,Z,Y5V,HD,1608,R/TP		
7	CN3	CONNECTOR,BOARD TO BOARD	ENBY0019501	20 PIN,.4 mm,ETC , ,H=1.5, Socket		
7	LD1	DIODE,LED,CHIP	EDLH0006001	Blue ,1608 ,R/TP ,Blue SMD LED		
7	LD2	DIODE,LED,CHIP	EDLH0006001	Blue ,1608 ,R/TP ,Blue SMD LED		
7	R10	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
7	R11	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
7	R12	RES,CHIP	ERHY0000203	10 ohm,1/16W,J,1005,R/TP		
7	R3	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
7	R4	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
7	R6	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
7	R7	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	SACD00	PCB ASSY,FLEXIBLE,SMT TOP	SACD0026201		Silver	
7	CN1	CONNECTOR,BOARD TO BOARD	ENBY0020201	40 PIN,0.4 mm,ETC , ,H=0.9, Header		
7	CN2	CONNECTOR,BOARD TO BOARD	ENBY0022401	50 PIN,0.4 mm,ETC , ,H=0.9, Header		
7	R1	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP		
7	R9	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	SPCY00	PCB,FLEXIBLE	SPCY0057801	POLYI ,0.5 mm,MULTI-6 ,		
4	SURY00	RECEIVER	SURY0009501	ASSY ,107 dB,32 ohm,11*07 ,3T		24
4	SVCY00	CAMERA	SVCY0009101	CMOS ,VGA ,		23_1
4	SVLM00	LCD MODULE	SVLM0015201	MAIN ,M_220*220 S_128*160 ,M_46.5*52.3*4.3 S_7*4.3 ,.262k ,TFT ,TM ,(SOURCE)HD66781 (GATE)HD66783 ,SUB LCD:DRIVE IC(LGDP4511) ,		13
4	SNGF00	ANTENNA,GSM,FIXED	SNGF0011001	3.0 ,-2.0 dBd,Green ,GSM900+DCS1800+PCS1900+WCDMA2100,fixed		65
4	SACY00	PCB ASSY,FLEXIBLE	SACY0038101		Silver	58

10. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	Part Number	Specification	Color	Remark
5	SACE00	PCB ASSY,FLEXIBLE,SMT	SACE0033901		Silver	
6	SACD00	PCB ASSY,FLEXIBLE,SMT TOP	SACD0026301		Silver	
7	CN1	CONNECTOR,BOARD TO BOARD	ENBY0025201	26 PIN,0.4 mm,ETC , ,H=0.9, Header		
7	CN2	CONNECTOR,BOARD TO BOARD	ENBY0019101	24 PIN,0.4 mm,STRAIGHT , ,H1.5, MALE		
7	LD1	DIODE,LED,MODULE	EDLM0005502	White ,3 LED,3.5*2.8*1.8 ,R/TP ,Flash LED		
7	R1	RES,CHIP	ERHY0000214	51 ohm,1/16W,J,1005,R/TP		
6	SPCY00	PCB,FLEXIBLE	SPCY0058201	POLYI ,0.5 mm,BUILD-UP 6 ,FPCB-CAMERA		
4	SVCY00	CAMERA	SVCY0007701	CMOS ,MEGA ,1.3M ESS Sensor		57
3	SAEY00	PCB ASSY,KEYPAD	SAEY0044401		Silver	51
4	SAEB00	PCB ASSY,KEYPAD,INSERT	SAEB0011701		Silver	
5	SAKY00	PCB ASSY,SIDEKEY	SAKY0005401		Silver	
5	SUSY00	SPEAKER	SUSY0017501	ASSY ,8 ohm,90 dB,15 mm,*14mm, 3.7T		52
4	SAEE00	PCB ASSY,KEYPAD,SMT	SAEE0013301		Silver	
5	SAEC00	PCB ASSY,KEYPAD,SMT BOTTOM	SAEC0012701		Silver	
6	C1	CAP,CERAMIC,CHIP	ECCH0000110	10 pF,50V,D,NP0,TC,1005,R/TP		
6	C10	CAP,CERAMIC,CHIP	ECCH0000122	47 pF,50V,J,NP0,TC,1005,R/TP		
6	C2	CAP,CERAMIC,CHIP	ECCH0000182	0.1 uF,10V ,K ,X5R ,HD ,1005 ,R/TP		
6	C3	CAP,CERAMIC,CHIP	ECCH0000182	0.1 uF,10V ,K ,X5R ,HD ,1005 ,R/TP		
6	C7	CAP,CERAMIC,CHIP	ECCH0000122	47 pF,50V,J,NP0,TC,1005,R/TP		
6	C8	CAP,CERAMIC,CHIP	ECCH0000122	47 pF,50V,J,NP0,TC,1005,R/TP		
6	C9	CAP,CERAMIC,CHIP	ECCH0000122	47 pF,50V,J,NP0,TC,1005,R/TP		
6	CN1	CONNECTOR,BOARD TO BOARD	ENBY0002107	24 PIN,.5 mm,STRAIGHT ,SILVER ,		
6	CN3	CONNECTOR,BOARD TO BOARD	ENBY0001803	2 PIN,1.27 mm,STRAIGHT ,SILVER ,		
6	CN4	CONNECTOR,BOARD TO BOARD	ENBY0001803	2 PIN,1.27 mm,STRAIGHT ,SILVER ,		
6	D1	DIODE,SWITCHING	EDSY0010401	1-1G1A ,40 V,300 A,R/TP ,Silicon Epitaxial Schottky Barrier Type Diode		
6	FB1	FILTER,BEAD,CHIP	SFBH0007103	75 ohm,1005 ,CHIP BEAD, 300mA		
6	FB2	FILTER,BEAD,CHIP	SFBH0007103	75 ohm,1005 ,CHIP BEAD, 300mA		
6	FB3	FILTER,BEAD,CHIP	SFBH0007103	75 ohm,1005 ,CHIP BEAD, 300mA		
6	FB4	FILTER,BEAD,CHIP	SFBH0007103	75 ohm,1005 ,CHIP BEAD, 300mA		
6	R1	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP		

10. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	Part Number	Specification	Color	Remark
6	R11	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R12	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R13	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R16	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R17	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R18	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R19	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R20	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R21	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R22	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R24	RES,CHIP	ERHY0000233	470 ohm,1/16W,J,1005,R/TP		
6	R25	RES,CHIP	ERHY0000233	470 ohm,1/16W,J,1005,R/TP		
6	R27	RES,CHIP	ERHY0000233	470 ohm,1/16W,J,1005,R/TP		
6	R28	RES,CHIP	ERHY0000233	470 ohm,1/16W,J,1005,R/TP		
6	R7	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R8	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R9	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	TVS1	DIODE,TVS	EDTY0007301	SOD-523 ,5 V,240 W,R/TP ,SINGLE LINE TVS DIODE FOR ESD		
6	TVS2	DIODE,TVS	EDTY0007301	SOD-523 ,5 V,240 W,R/TP ,SINGLE LINE TVS DIODE FOR ESD		
6	TVS3	DIODE,TVS	EDTY0007301	SOD-523 ,5 V,240 W,R/TP ,SINGLE LINE TVS DIODE FOR ESD		
6	U1	IC	EUSY0200301	Leadless chip ,6 PIN,R/TP ,Hall S/W, Pb Free		
6	VA1	VARISTOR	SEVY0000702	14 V,10% ,SMD ,		
6	VA2	VARISTOR	SEVY0000702	14 V,10% ,SMD ,		
6	VA3	VARISTOR	SEVY0000702	14 V,10% ,SMD ,		
5	SAED00	PCB ASSY,KEYPAD,SMT TOP	SAED0012901		Silver	
6	LD1	DIODE,LED,CHIP	EDLH0006001	Blue ,1608 ,R/TP ,Blue SMD LED		
6	LD10	DIODE,LED,CHIP	EDLH0006001	Blue ,1608 ,R/TP ,Blue SMD LED		
6	LD11	DIODE,LED,CHIP	EDLH0006001	Blue ,1608 ,R/TP ,Blue SMD LED		
6	LD12	DIODE,LED,CHIP	EDLH0006001	Blue ,1608 ,R/TP ,Blue SMD LED		
6	LD13	DIODE,LED,CHIP	EDLH0006001	Blue ,1608 ,R/TP ,Blue SMD LED		
6	LD14	DIODE,LED,CHIP	EDLH0006001	Blue ,1608 ,R/TP ,Blue SMD LED		
6	LD15	DIODE,LED,CHIP	EDLH0006001	Blue ,1608 ,R/TP ,Blue SMD LED		
6	LD16	DIODE,LED,CHIP	EDLH0006001	Blue ,1608 ,R/TP ,Blue SMD LED		

10. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	Part Number	Specification	Color	Remark
6	LD17	DIODE,LED,CHIP	EDLH0006001	Blue ,1608 ,R/TP ,Blue SMD LED		
6	LD18	DIODE,LED,CHIP	EDLH0006001	Blue ,1608 ,R/TP ,Blue SMD LED		
6	LD19	DIODE,LED,CHIP	EDLH0006001	Blue ,1608 ,R/TP ,Blue SMD LED		
6	LD2	DIODE,LED,CHIP	EDLH0006001	Blue ,1608 ,R/TP ,Blue SMD LED		
6	LD3	DIODE,LED,CHIP	EDLH0006001	Blue ,1608 ,R/TP ,Blue SMD LED		
6	LD4	DIODE,LED,CHIP	EDLH0006001	Blue ,1608 ,R/TP ,Blue SMD LED		
6	LD5	DIODE,LED,CHIP	EDLH0006001	Blue ,1608 ,R/TP ,Blue SMD LED		
6	LD6	DIODE,LED,CHIP	EDLH0006001	Blue ,1608 ,R/TP ,Blue SMD LED		
6	LD7	DIODE,LED,CHIP	EDLH0006001	Blue ,1608 ,R/TP ,Blue SMD LED		
6	LD8	DIODE,LED,CHIP	EDLH0006001	Blue ,1608 ,R/TP ,Blue SMD LED		
6	LD9	DIODE,LED,CHIP	EDLH0006001	Blue ,1608 ,R/TP ,Blue SMD LED		
6	R10	RES,CHIP	ERHY0000223	150 ohm,1/16W,J,1005,R/TP		
6	R14	RES,CHIP	ERHY0000223	150 ohm,1/16W,J,1005,R/TP		
6	R15	RES,CHIP	ERHY0000223	150 ohm,1/16W,J,1005,R/TP		
6	R2	RES,CHIP	ERHY0000223	150 ohm,1/16W,J,1005,R/TP		
6	R23	RES,CHIP	ERHY0000223	150 ohm,1/16W,J,1005,R/TP		
6	R26	RES,CHIP	ERHY0000223	150 ohm,1/16W,J,1005,R/TP		
6	R29	RES,CHIP	ERHY0000223	150 ohm,1/16W,J,1005,R/TP		
6	R3	RES,CHIP	ERHY0000223	150 ohm,1/16W,J,1005,R/TP		
6	R30	RES,CHIP	ERHY0000223	150 ohm,1/16W,J,1005,R/TP		
6	R31	RES,CHIP	ERHY0000223	150 ohm,1/16W,J,1005,R/TP		
6	R35	RES,CHIP	ERHY0000223	150 ohm,1/16W,J,1005,R/TP		
6	R36	RES,CHIP	ERHY0000223	150 ohm,1/16W,J,1005,R/TP		
6	R37	RES,CHIP	ERHY0000223	150 ohm,1/16W,J,1005,R/TP		
6	R38	RES,CHIP	ERHY0000223	150 ohm,1/16W,J,1005,R/TP		
6	R39	RES,CHIP	ERHY0000223	150 ohm,1/16W,J,1005,R/TP		
6	R4	RES,CHIP	ERHY0000223	150 ohm,1/16W,J,1005,R/TP		
6	R40	RES,CHIP	ERHY0000223	150 ohm,1/16W,J,1005,R/TP		
6	R5	RES,CHIP	ERHY0000223	150 ohm,1/16W,J,1005,R/TP		
6	R6	RES,CHIP	ERHY0000223	150 ohm,1/16W,J,1005,R/TP		
6	TVS4	DIODE,TVS	EDTY0008501	TFSC ,5 V,50 W,R/TP ,small size		
6	TVS5	DIODE,TVS	EDTY0008501	TFSC ,5 V,50 W,R/TP ,small size		
6	TVS6	DIODE,TVS	EDTY0008501	TFSC ,5 V,50 W,R/TP ,small size		
5	SPEY00	PCB,KEYPAD	SPEY0035701	FR-4 ,0.5 mm,DOUBLE ,		

10. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	Part Number	Specification	Color	Remark
3	SAFY00	PCB ASSY,MAIN	SAFY0134601		Silver	54
4	SAFB00	PCB ASSY,MAIN,INSERT	SAFB0053501		Green	
5	SBCL00	BATTERY,CELL,LITHIUM	SBCL0001303	2 V,1 mAh,COIN ,SOLDER TYPE BACKUP BATTERY		
4	SAFF00	PCB ASSY,MAIN,SMT	SAFF0059401		Silver	
5	SAFC00	PCB ASSY,MAIN,SMT BOTTOM	SAFC0065801		Green	
6	ANT601	ANTENNA,GSM,FIXED	SNGF0008301	3.0 ,-2.0 dBd , ,bluetooth_chip, 9.0x3.0x1.5		
6	B201	X-TAL	EXXY0016801	13 MHz,19 PPM,10 pF,40 ohm,SMD ,5*3.20*0.7 ,		
6	C101	CAP,CERAMIC,CHIP	ECCH0000173	1.2 pF,16V ,B ,NP0 ,TC ,1005 ,R/TP		
6	C102	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP		
6	C103	CAP,CERAMIC,CHIP	ECCH0000186	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP		
6	C104	CAP,CERAMIC,CHIP	ECCH0000110	10 pF,50V,D,NP0,TC,1005,R/TP		
6	C105	CAP,CERAMIC,CHIP	ECCH0000110	10 pF,50V,D,NP0,TC,1005,R/TP		
6	C106	CAP,CERAMIC,CHIP	ECCH0000110	10 pF,50V,D,NP0,TC,1005,R/TP		
6	C107	CAP,CERAMIC,CHIP	ECCH0000110	10 pF,50V,D,NP0,TC,1005,R/TP		
6	C108	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP		
6	C109	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP		
6	C110	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP		
6	C112	CAP,CERAMIC,CHIP	ECCH0000161	33 nF,16V,K,X7R,HD,1005,R/TP		
6	C113	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C114	CAP,CERAMIC,CHIP	ECCH0005705	10 uF,6.3V ,K ,X5R ,HD ,2012 ,R/TP		
6	C117	CAP,CERAMIC,CHIP	ECCH0005705	10 uF,6.3V ,K ,X5R ,HD ,2012 ,R/TP		
6	C1899	CAP,CERAMIC,CHIP	ECCH0006201	4.7 uF,6.3V ,K ,X5R ,TC ,1608 ,R/TP		
6	C1915	CAP,CERAMIC,CHIP	ECCH0006201	4.7 uF,6.3V ,K ,X5R ,TC ,1608 ,R/TP		
6	C1916	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP		
6	C1917	CAP,CERAMIC,CHIP	ECCH0000276	1 uF,10V,Z,Y5V,HD,1608,R/TP		
6	C1918	CAP,CHIP,MAKER	ECZH0003501	1 uF,6.3V ,K ,X5R ,HD ,1608 ,R/TP		
6	C201	CAP,CERAMIC,CHIP	ECCH0000117	27 pF,50V,J,NP0,TC,1005,R/TP		
6	C202	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP		
6	C203	CAP,CERAMIC,CHIP	ECCH0000117	27 pF,50V,J,NP0,TC,1005,R/TP		
6	C204	CAP,CERAMIC,CHIP	ECCH0000147	2.2 nF,50V,K,X7R,HD,1005,R/TP		
6	C206	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		
6	C207	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		
6	C208	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		
6	C209	CAP,CERAMIC,CHIP	ECCH0000180	3.3 pF,50V ,C ,NP0 ,TC ,1005 ,R/TP		

10. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	Part Number	Specification	Color	Remark
6	C210	CAP,CERAMIC,CHIP	ECCH0000180	3.3 pF,50V ,C ,NP0 ,TC ,1005 ,R/TP		
6	C211	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		
6	C212	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		
6	C214	CAP,CERAMIC,CHIP	ECCH0000167	0.1 uF,6.3V,K,X5R,HD,1005,R/TP		
6	C215	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		
6	C216	CAP,CERAMIC,CHIP	ECCH0000138	390 pF,50V,K,X7R,HD,1005,R/TP		
6	C217	CAP,CERAMIC,CHIP	ECCH0000152	5.6 nF,25V,K,X7R,HD,1005,R/TP		
6	C218	CAP,CERAMIC,CHIP	ECCH0000147	2.2 nF,50V,K,X7R,HD,1005,R/TP		
6	C219	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP		
6	C220	CAP,CERAMIC,CHIP	ECCH0000701	1.2 pF,50V ,C ,NP0 ,TC ,1005 ,R/TP		
6	C221	CAP,CERAMIC,CHIP	ECCH0000127	82 pF,50V,J,NP0,TC,1005,R/TP		
6	C222	CAP,CERAMIC,CHIP	ECCH0000147	2.2 nF,50V,K,X7R,HD,1005,R/TP		
6	C223	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP		
6	C224	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP		
6	C225	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		
6	C226	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP		
6	C227	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP		
6	C228	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP		
6	C229	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP		
6	C230	CAP,CERAMIC,CHIP	ECCH0000137	330 pF,50V ,K ,X7R ,HD ,1005 ,R/TP		
6	C231	CAP,CERAMIC,CHIP	ECCH0000122	47 pF,50V,J,NP0,TC,1005,R/TP		
6	C232	CAP,CERAMIC,CHIP	ECCH0000181	4.7 pF,50V ,C ,NP0 ,TC ,1005 ,R/TP		
6	C233	CAP,CERAMIC,CHIP	ECCH0000124	56 pF,50V,J,NP0,TC,1005,R/TP		
6	C234	CAP,CERAMIC,CHIP	ECCH0000175	2.7 pF,50V ,B ,NP0 ,TC ,1005 ,R/TP		
6	C235	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		
6	C236	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		
6	C237	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP		
6	C238	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP		
6	C239	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		
6	C240	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		
6	C313	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP		
6	C314	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP		
6	C315	CAP,CERAMIC,CHIP	ECCH0000110	10 pF,50V,D,NP0,TC,1005,R/TP		
6	C316	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		

10. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	Part Number	Specification	Color	Remark
6	C317	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		
6	C318	CAP,CERAMIC,CHIP	ECCH0000128	100 pF,50V,J,NP0,TC,1005,R/TP		
6	C319	CAP,CERAMIC,CHIP	ECCH0000181	4.7 pF,50V ,C ,NP0 ,TC ,1005 ,R/TP		
6	C320	CAP,CERAMIC,CHIP	ECCH0000186	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP		
6	C321	CAP,CERAMIC,CHIP	ECCH0000186	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP		
6	C322	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP		
6	C323	CAP,CERAMIC,CHIP	ECCH0000110	10 pF,50V,D,NP0,TC,1005,R/TP		
6	C324	CAP,CERAMIC,CHIP	ECCH0000110	10 pF,50V,D,NP0,TC,1005,R/TP		
6	C325	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP		
6	C326	CAP,CERAMIC,CHIP	ECCH0000110	10 pF,50V,D,NP0,TC,1005,R/TP		
6	C327	CAP,CERAMIC,CHIP	ECCH0000105	4 pF,50V,C,NP0,TC,1005,R/TP		
6	C328	CAP,CERAMIC,CHIP	ECCH0000122	47 pF,50V,J,NP0,TC,1005,R/TP		
6	C330	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		
6	C331	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		
6	C332	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP		
6	C333	CAP,CERAMIC,CHIP	ECCH0000128	100 pF,50V,J,NP0,TC,1005,R/TP		
6	C334	CAP,CERAMIC,CHIP	ECCH0000130	150 pF,50V ,J ,SL ,TC ,1005 ,R/TP		
6	C335	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		
6	C336	CAP,CERAMIC,CHIP	ECCH0000149	3.3 nF,50V,K,X7R,HD,1005,R/TP		
6	C337	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP		
6	C401	CAP,CERAMIC,CHIP	ECCH0000130	150 pF,50V ,J ,SL ,TC ,1005 ,R/TP		
6	C402	CAP,CERAMIC,CHIP	ECCH0000128	100 pF,50V,J,NP0,TC,1005,R/TP		
6	C403	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		
6	C404	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		
6	C405	CAP,CERAMIC,CHIP	ECCH0000128	100 pF,50V,J,NP0,TC,1005,R/TP		
6	C406	CAP,CERAMIC,CHIP	ECCH0000186	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP		
6	C408	CAP,CERAMIC,CHIP	ECCH0000128	100 pF,50V,J,NP0,TC,1005,R/TP		
6	C410	CAP,CERAMIC,CHIP	ECCH0000186	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP		
6	C411	INDUCTOR,CHIP	ELCH0005001	2.2 nH,S ,1005 ,R/TP ,		
6	C412	CAP,CERAMIC,CHIP	ECCH0000186	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP		
6	C420	CAP,CERAMIC,CHIP	ECCH0005705	10 uF,6.3V ,K ,X5R ,HD ,2012 ,R/TP		
6	C422	CAP,CERAMIC,CHIP	ECCH0005705	10 uF,6.3V ,K ,X5R ,HD ,2012 ,R/TP		
6	C423	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		
6	C424	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP		

10. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	Part Number	Specification	Color	Remark
6	C507	CAP,CERAMIC,CHIP	ECCH0000122	47 pF,50V,J,NP0,TC,1005,R/TP		
6	C514	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		
6	C515	CAP,CERAMIC,CHIP	ECCH0000122	47 pF,50V,J,NP0,TC,1005,R/TP		
6	C516	CAP,CERAMIC,CHIP	ECCH0000165	68 nF,6.3V,K,X5R,HD,1005,R/TP		
6	C518	CAP,CERAMIC,CHIP	ECCH0000165	68 nF,6.3V,K,X5R,HD,1005,R/TP		
6	C520	CAP,CERAMIC,CHIP	ECCH0000122	47 pF,50V,J,NP0,TC,1005,R/TP		
6	C521	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		
6	C522	CAP,TANTAL,CHIP	ECTH0002702	1 uF,16V ,M ,STD ,1608 ,R/TP		
6	C523	CAP,CERAMIC,CHIP	ECCH0000279	0.47 uF,10V ,Z ,Y5V ,HD ,1608 ,R/TP		
6	C527	CAP,CHIP,MAKER	ECZH0026301	4.7 uF,6.3V ,Z ,Y5V ,HD ,1608 ,R/TP		
6	C531	CAP,CERAMIC,CHIP	ECCH0000276	1 uF,10V,Z,Y5V,HD,1608,R/TP		
6	C532	CAP,CERAMIC,CHIP	ECCH0000276	1 uF,10V,Z,Y5V,HD,1608,R/TP		
6	C533	CAP,CERAMIC,CHIP	ECCH0000276	1 uF,10V,Z,Y5V,HD,1608,R/TP		
6	C534	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C535	CAP,CERAMIC,CHIP	ECCH0000165	68 nF,6.3V,K,X5R,HD,1005,R/TP		
6	C536	CAP,CERAMIC,CHIP	ECCH0004903	1 uF,6.3V ,Z ,Y5V ,TC ,1005 ,R/TP		
6	C537	CAP,CERAMIC,CHIP	ECCH0000122	47 pF,50V,J,NP0,TC,1005,R/TP		
6	C538	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C539	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C541	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		
6	C542	CAP,CERAMIC,CHIP	ECCH0004903	1 uF,6.3V ,Z ,Y5V ,TC ,1005 ,R/TP		
6	C543	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		
6	C544	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C545	CAP,CERAMIC,CHIP	ECCH0004903	1 uF,6.3V ,Z ,Y5V ,TC ,1005 ,R/TP		
6	C546	CAP,CERAMIC,CHIP	ECCH0005705	10 uF,6.3V ,K ,X5R ,HD ,2012 ,R/TP		
6	C547	CAP,CERAMIC,CHIP	ECCH0004903	1 uF,6.3V ,Z ,Y5V ,TC ,1005 ,R/TP		
6	C548	CAP,CERAMIC,CHIP	ECCH0000110	10 pF,50V,D,NP0,TC,1005,R/TP		
6	C549	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C550	CAP,CERAMIC,CHIP	ECCH0005705	10 uF,6.3V ,K ,X5R ,HD ,2012 ,R/TP		
6	C551	CAP,CERAMIC,CHIP	ECCH0005705	10 uF,6.3V ,K ,X5R ,HD ,2012 ,R/TP		
6	C552	CAP,CERAMIC,CHIP	ECCH0000139	470 pF,50V,K,X7R,HD,1005,R/TP		
6	C553	CAP,CERAMIC,CHIP	ECCH0000276	1 uF,10V,Z,Y5V,HD,1608,R/TP		
6	C556	CAP,CERAMIC,CHIP	ECCH0000143	1 nF,50V,K,X7R,HD,1005,R/TP		
6	C557	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		

10. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	Part Number	Specification	Color	Remark
6	C576	CAP,CERAMIC,CHIP	ECCH0005801	2.2 uF,6.3V ,K ,X5R ,TC ,1608 ,R/TP		
6	C588	CAP,CERAMIC,CHIP	ECCH0005705	10 uF,6.3V ,K ,X5R ,HD ,2012 ,R/TP		
6	C591	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C595	CAP,CERAMIC,CHIP	ECCH0005705	10 uF,6.3V ,K ,X5R ,HD ,2012 ,R/TP		
6	C596	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C597	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C598	CAP,CERAMIC,CHIP	ECCH0000139	470 pF,50V,K,X7R,HD,1005,R/TP		
6	C599	CAP,CERAMIC,CHIP	ECCH0000110	10 pF,50V,D,NP0,TC,1005,R/TP		
6	C600	CAP,CERAMIC,CHIP	ECCH0005705	10 uF,6.3V ,K ,X5R ,HD ,2012 ,R/TP		
6	C640	CAP,CERAMIC,CHIP	ECCH0005705	10 uF,6.3V ,K ,X5R ,HD ,2012 ,R/TP		
6	C641	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C642	CAP,CERAMIC,CHIP	ECCH0000128	100 pF,50V,J,NP0,TC,1005,R/TP		
6	C643	CAP,CERAMIC,CHIP	ECCH0000128	100 pF,50V,J,NP0,TC,1005,R/TP		
6	C645	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C646	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C647	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		
6	C705	CAP,CERAMIC,CHIP	ECCH0000114	20 pF,50V,J,NP0,TC,1005,R/TP		
6	C706	CAP,CERAMIC,CHIP	ECCH0000114	20 pF,50V,J,NP0,TC,1005,R/TP		
6	C708	CAP,CERAMIC,CHIP	ECCH0005801	2.2 uF,6.3V ,K ,X5R ,TC ,1608 ,R/TP		
6	C709	CAP,CERAMIC,CHIP	ECCH0005801	2.2 uF,6.3V ,K ,X5R ,TC ,1608 ,R/TP		
6	C710	CAP,CERAMIC,CHIP	ECCH0004903	1 uF,6.3V ,Z ,Y5V ,TC ,1005 ,R/TP		
6	C711	CAP,CERAMIC,CHIP	ECCH0005801	2.2 uF,6.3V ,K ,X5R ,TC ,1608 ,R/TP		
6	C712	CAP,CERAMIC,CHIP	ECCH0005801	2.2 uF,6.3V ,K ,X5R ,TC ,1608 ,R/TP		
6	C713	CAP,CERAMIC,CHIP	ECCH0004903	1 uF,6.3V ,Z ,Y5V ,TC ,1005 ,R/TP		
6	C714	CAP,CERAMIC,CHIP	ECCH0004903	1 uF,6.3V ,Z ,Y5V ,TC ,1005 ,R/TP		
6	C715	CAP,CERAMIC,CHIP	ECCH0004903	1 uF,6.3V ,Z ,Y5V ,TC ,1005 ,R/TP		
6	C716	CAP,CERAMIC,CHIP	ECCH0004903	1 uF,6.3V ,Z ,Y5V ,TC ,1005 ,R/TP		
6	C717	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C718	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C719	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C720	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C721	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C722	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C723	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		

10. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	Part Number	Specification	Color	Remark
6	C724	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C725	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C726	CAP,CERAMIC,CHIP	ECCH0000122	47 pF,50V,J,NP0,TC,1005,R/TP		
6	C727	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C728	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C729	CAP,CERAMIC,CHIP	ECCH0000137	330 pF,50V ,K ,X7R ,HD ,1005 ,R/TP		
6	C730	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C731	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C732	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C733	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C734	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C735	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C736	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C737	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C738	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C740	CAP,TANTAL,CHIP,MAKER	ECTZ0000318	33 uF,10V ,M ,STD ,3216 ,R/TP		
6	C741	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C742	CAP,CERAMIC,CHIP	ECCH0000276	1 uF,10V,Z,Y5V,HD,1608,R/TP		
6	C743	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP		
6	CN601	CONN,RF SWITCH	ENWY0000401	STRAIGHT ,SMD ,0.1 dB,3*3*1.8 / 500 CYCLES		
6	CN701	CONNECTOR,BOARD TO BOARD	ENBY0022501	50 PIN,0.4 mm,ETC , ,H=0.9, Socket		
6	CN702	CONNECTOR,BOARD TO BOARD	ENBY0025501	26 PIN,0.4 mm,ETC , ,H=0.9, Socket		
6	D701	IC	EUSY0135201	u181 BGA ,181 PIN,R/TP ,ASIC / WCDMA AIR INTERFACE / WANDA		
6	D703	DIODE,SWITCHING	EDSY0009901	ESC ,80 V,300 A,R/TP ,1.6*0.8*0.6(t)		
6	FB501	FILTER,BEAD,CHIP	SFBH0008901	30 ohm,2012 ,3000mA, BEAD for LARGE CURRENT		
6	FB502	FILTER,BEAD,CHIP	SFBH0008901	30 ohm,2012 ,3000mA, BEAD for LARGE CURRENT		
6	FB503	FILTER,BEAD,CHIP	SFBH0008901	30 ohm,2012 ,3000mA, BEAD for LARGE CURRENT		
6	FB504	FILTER,BEAD,CHIP	SFBH0008901	30 ohm,2012 ,3000mA, BEAD for LARGE CURRENT		
6	FB505	FILTER,BEAD,CHIP	SFBH0002302	120 ohm,1608 ,CHIP BEAD, 2000mA		
6	FL101	FILTER,SEPERATOR	SFAY0004601	, , dB, dB, dB, dB,ETC ,16 PIN / 4.2*3.5*1.4 / GSM-WCDMA SP6T		
6	FL201	FILTER,SAW	SFSY0024402	2140 MHz,2.0*1.6*0.6 ,SMD ,6pin, Unbal-Bal, 50//200		
6	FL301	FILTER,SAW	SFSY0024401	1950 MHz,2.0*1.6*0.6 ,SMD ,6pin, Bal-Unbal, 200//50		
6	FL401	FILTER,EMI/POWER	SFEY0006501	SMD ,3 TERMINAL EMI FILTER		

10. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	Part Number	Specification	Color	Remark
6	FL702	FILTER,EMI/POWER	SFEY0006701	SMD ,CSP, 20 Ball 8ch EMI Filter /w ESD,Pb-free		
6	FL705	FILTER,EMI/POWER	SFEY0007801	SMD ,4ch(2.0*1.25), 200MHz, 1000Mohm, 10V, 100mA, (29nH,47pF)		
6	FL706	FILTER,EMI/POWER	SFEY0007801	SMD ,4ch(2.0*1.25), 200MHz, 1000Mohm, 10V, 100mA, (29nH,47pF)		
6	L101	INDUCTOR,CHIP	ELCH0005010	1.8 nH,S ,1005 ,R/TP ,		
6	L102	INDUCTOR,CHIP	ELCH0001030	8.2 nH,J ,1005 ,R/TP ,PB-FREE		
6	L103	FILTER,BEAD,CHIP	SFBH0007103	75 ohm,1005 ,CHIP BEAD, 300mA		
6	L104	FILTER,BEAD,CHIP	SFBH0007103	75 ohm,1005 ,CHIP BEAD, 300mA		
6	L105	FILTER,BEAD,CHIP	SFBH0007103	75 ohm,1005 ,CHIP BEAD, 300mA		
6	L201	INDUCTOR,CHIP	ELCH0001425	82 nH,J ,1005 ,R/TP ,PBFREE		
6	L202	INDUCTOR,CHIP	ELCH0001425	82 nH,J ,1005 ,R/TP ,PBFREE		
6	L203	INDUCTOR,CHIP	ELCH0001407	5.6 nH,S ,1005 ,R/TP ,PBFREE		
6	L204	INDUCTOR,CHIP	ELCH0005001	2.2 nH,S ,1005 ,R/TP ,		
6	L207	INDUCTOR,CHIP	ELCH0001511	100 nH,J ,1608 ,R/TP ,PBFREE		
6	L208	INDUCTOR,CHIP	ELCH0003811	1000 nH,K ,1608 ,R/TP ,COIL TYPE		
6	L305	FILTER,BEAD,CHIP	SFBH0007103	75 ohm,1005 ,CHIP BEAD, 300mA		
6	L307	INDUCTOR,CHIP	ELCH0001407	5.6 nH,S ,1005 ,R/TP ,PBFREE		
6	L308	INDUCTOR,CHIP	ELCH0001001	10 nH,J ,1005 ,R/TP ,Pb Free		
6	L309	INDUCTOR,CHIP	ELCH0001407	5.6 nH,S ,1005 ,R/TP ,PBFREE		
6	L310	INDUCTOR,CHIP	ELCH0001401	15 nH,J ,1005 ,R/TP ,Pb Free		
6	L311	INDUCTOR,CHIP	ELCH0001401	15 nH,J ,1005 ,R/TP ,Pb Free		
6	L401	FILTER,BEAD,CHIP	SFBH0008101	600 ohm,1005 ,		
6	L402	FILTER,BEAD,CHIP	SFBH0007103	75 ohm,1005 ,CHIP BEAD, 300mA		
6	L501	FILTER,BEAD,CHIP	SFBH0007103	75 ohm,1005 ,CHIP BEAD, 300mA		
6	L502	FILTER,BEAD,CHIP	SFBH0007103	75 ohm,1005 ,CHIP BEAD, 300mA		
6	L503	INDUCTOR,SMD,POWER	ELCP0009402	22 uH,M ,2.8*2.6*1.0 ,R/TP ,power inductor		
6	L601	INDUCTOR,CHIP	ELCH0005005	27 nH,J ,1005 ,R/TP ,		
6	L602	CAP,CERAMIC,CHIP	ECCH0000186	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP		
6	L701	IC	EUSY0163501	SOT323-6L ,6 PIN,R/TP ,EMI FILTER & LINE TERMINATION for USB		
6	L702	FILTER,BEAD,CHIP	SFBH0002302	120 ohm,1608 ,CHIP BEAD, 2000mA		
6	N101	IC	EUSY0122502	LLP-6 ,6 PIN,R/TP ,300mA CMOS LDO / 2.8V, Pb-free		
6	N201	IC	EUSY0133001	uBGA ,56 PIN,R/TP ,U8000 RF IC		
6	N304	IC	EUSY0132901	56 ,56 PIN,R/TP ,WCDMA TXIC Wivi		
6	N401	PAM	SMPY0007101	dBm, %, mA, dBc, dB,6*6*1.25 ,SMD ,PAM for TRI-BAND(EGSM/GPRS)		

10. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	Part Number	Specification	Color	Remark
6	N503	IC	EUSY0132701	u143 BGA ,143 PIN,R/TP ,ASIC / POWER MANAGEMENT IC / VINCENNE		
6	N702	IC	EUSY0153001	SOT23-5 ,5 PIN,R/TP ,150 mA LDO REGULATOR / 1.5V		
6	PT501	THERMISTOR	SETY0005701	NTC ,47000 ohm,SMD ,F, Pb Free		
6	Q501	TR,FET,P-CHANNEL	EQFP0005601	POWERPAK 1212-8 ,0.8 W,20 V,5.4 A,R/TP ,P-CHANNEL 20V (D-S) MOSFET		
6	Q502	TR,FET,P-CHANNEL	EQFP0003601	SOT-363 ,.27 W,20 V,.66 A,R/TP ,Dual(P-channel:PD=0.27W,VDS=-8V,ID=0.57, Pb free		
6	Q702	TR,BJT,NPN	EQBN0014901	SOT323 ,.2 W,R/TP ,NPN SWITCHING TR, Pb free		
6	Q703	TR,BJT,PNP	EQBP0003001	UMT6 ,.15 W,R/TP ,		
6	R101	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R102	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R103	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R104	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R105	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R106	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R201	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R202	RES,CHIP	ERHY0000250	3.3K ohm,1/16W,J,1005,R/TP		
6	R203	FILTER,BEAD,CHIP	SFBH0007103	75 ohm,1005 ,CHIP BEAD, 300mA		
6	R204	FILTER,BEAD,CHIP	SFBH0007103	75 ohm,1005 ,CHIP BEAD, 300mA		
6	R205	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R206	RES,CHIP	ERHY0000255	5.6K ohm,1/16W,J,1005,R/TP		
6	R207	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R208	RES,CHIP	ERHY0000220	100 ohm,1/16W,J,1005,R/TP		
6	R209	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R210	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R212	RES,CHIP	ERHY0000241	1K ohm,1/16W,J,1005,R/TP		
6	R2126	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R2127	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP		
6	R2129	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP		
6	R2132	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP		
6	R2135	RES,CHIP	ERHY0000160	180K ohm,1/16W,F,1005,R/TP		
6	R2138	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP		
6	R215	RES,CHIP	ERHY0000203	10 ohm,1/16W,J,1005,R/TP		
6	R2150	RES,CHIP	ERHY0000714	.51 ohm,1/4W ,J ,2012 ,R/TP		
6	R216	RES,CHIP	ERHY0000261	10K ohm,1/16W,J,1005,R/TP		

10. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	Part Number	Specification	Color	Remark
6	R217	RES,CHIP	ERHY0000261	10K ohm,1/16W,J,1005,R/TP		
6	R2171	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R2179	FILTER,BEAD,CHIP	SFBH0007103	75 ohm,1005 ,CHIP BEAD, 300mA		
6	R2186	FILTER,BEAD,CHIP	SFBH0007103	75 ohm,1005 ,CHIP BEAD, 300mA		
6	R2191	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R2192	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP		
6	R2194	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R2196	RES,CHIP	ERHY0000226	220 ohm,1/16W,J,1005,R/TP		
6	R2197	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R220	RES,CHIP	ERHY0000203	10 ohm,1/16W,J,1005,R/TP		
6	R2205	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R221	RES,CHIP	ERHY0000203	10 ohm,1/16W,J,1005,R/TP		
6	R2225	RES,CHIP	ERHY0008701	0.22 ohm,1/4W ,J ,2012 ,R/TP		
6	R2236	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R2237	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R2238	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R2239	RES,CHIP	ERHY0000261	10K ohm,1/16W,J,1005,R/TP		
6	R2251	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R309	RES,CHIP	ERHY0000203	10 ohm,1/16W,J,1005,R/TP		
6	R310	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R311	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R312	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R313	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R314	RES,CHIP	ERHY0000111	680 ohm,1/16W,F,1005,R/TP		
6	R315	RES,CHIP	ERHY0000111	680 ohm,1/16W,F,1005,R/TP		
6	R316	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R317	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R318	RES,CHIP	ERHY0000254	4.7K ohm,1/16W,J,1005,R/TP		
6	R319	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R320	RES,CHIP	ERHY0000203	10 ohm,1/16W,J,1005,R/TP		
6	R401	RES,CHIP	ERHY0000241	1K ohm,1/16W,J,1005,R/TP		
6	R402	RES,CHIP,MAKER	ERHZ0000459	3 Kohm,1/16W ,J ,1005 ,R/TP		
6	R403	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R407	RES,CHIP	ERHY0008601	0.05 ohm,1/4W ,J ,2012 ,R/TP		

10. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	Part Number	Specification	Color	Remark
6	R408	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R413	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R503	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R504	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP		
6	R505	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R506	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R510	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R511	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R512	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R516	RES,CHIP	ERHY0000220	100 ohm,1/16W,J,1005,R/TP		
6	R517	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R518	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R519	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R520	RES,CHIP	ERHY0000220	100 ohm,1/16W,J,1005,R/TP		
6	R521	RES,CHIP	ERHY0000266	22K ohm,1/16W,J,1005,R/TP		
6	R522	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R523	RES,CHIP	ERHY0000241	1K ohm,1/16W,J,1005,R/TP		
6	R526	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R527	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R528	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP		
6	R535	RES,CHIP	ERHY0000241	1K ohm,1/16W,J,1005,R/TP		
6	R536	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R538	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP		
6	R540	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R541	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R542	RES,CHIP	ERHY0000263	15K ohm,1/16W,J,1005,R/TP		
6	R543	RES,CHIP	ERHY0000213	47 ohm,1/16W,J,1005,R/TP		
6	R544	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R545	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R546	RES,CHIP	ERHY0000261	10K ohm,1/16W,J,1005,R/TP		
6	R547	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP		
6	R548	RES,CHIP	ERHY0000202	4.7 ohm,1/16W,J,1005,R/TP		
6	R549	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP		
6	R550	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP		

10. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	Part Number	Specification	Color	Remark
6	R551	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R552	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP		
6	R553	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R554	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R555	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R556	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R557	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP		
6	R558	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R559	RES,CHIP	ERHY0000266	22K ohm,1/16W,J,1005,R/TP		
6	R560	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R561	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R562	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP		
6	R563	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R564	RES,CHIP	ERHY0000401	0 ohm,1/16W,J,1608,R/TP		
6	R565	RES,CHIP,MAKER	ERHZ0000319	8200 ohm,1/16W ,F ,1005 ,R/TP		
6	R570	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R593	RES,CHIP	ERHY0008701	0.22 ohm,1/4W ,J ,2012 ,R/TP		
6	R599	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R600	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R648	RES,CHIP	ERHY0001302	1 ohm,1/8W,J,2012,R/TP		
6	R650	RES,CHIP	ERHY0000266	22K ohm,1/16W,J,1005,R/TP		
6	R651	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R652	RES,CHIP	ERHY0000282	120K ohm,1/16W,J,1005,R/TP		
6	R656	CAP,CERAMIC,CHIP	ECCH0000186	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP		
6	R701	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R702	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R704	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R706	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R708	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R714	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R715	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R716	RES,CHIP	ERHY0000214	51 ohm,1/16W,J,1005,R/TP		
6	R717	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R718	RES,CHIP	ERHY0000214	51 ohm,1/16W,J,1005,R/TP		

10. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	Part Number	Specification	Color	Remark
6	R721	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R724	RES,CHIP	ERHY0000261	10K ohm,1/16W,J,1005,R/TP		
6	R725	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R726	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R730	RES,CHIP	ERHY0000261	10K ohm,1/16W,J,1005,R/TP		
6	R731	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R732	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R733	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R735	RES,CHIP	ERHY0000262	12K ohm,1/16W,J,1005,R/TP		
6	R736	RES,CHIP,MAKER	ERHZ0000459	3 Kohm,1/16W ,J , 1005 ,R/TP		
6	R737	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R738	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R739	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R740	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R744	RES,CHIP	ERHY0000250	3.3K ohm,1/16W,J,1005,R/TP		
6	R745	RES,CHIP	ERHY0000249	2.7K ohm,1/16W,J,1005,R/TP		
6	R747	RES,CHIP	ERHY0000143	43K ohm,1/16W,F,1005,R/TP		
6	R748	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP		
6	R749	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP		
6	R752	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R753	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R754	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R755	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP		
6	R756	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R757	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP		
6	R758	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R843	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP		
6	R847	RES,CHIP	ERHY0008601	0.05 ohm,1/4W ,J ,2012 ,R/TP		
6	R875	RES,CHIP	ERHY0008601	0.05 ohm,1/4W ,J ,2012 ,R/TP		
6	R878	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP		
6	R899	RES,CHIP	ERHY0008602	0.1 ohm,1/4W ,J ,2012 ,R/TP		
6	U501	IC	EUSY0232802	sot 23-5 ,5 PIN,R/TP ,2.8V,150mA LDO		
6	U503	IC	EUSY0232802	sot 23-5 ,5 PIN,R/TP ,2.8V,150mA LDO		
6	U506	IC	EUSY0275401	SOT23-5 ,5 PIN,R/TP ,150mA, 2.4V, 80dB, LDO, PBFREE		

10. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	Part Number	Specification	Color	Remark
6	U510	IC	EUSY0232815	SOT23-5 ,5 PIN,R/TP ,2.85V,300mA,LDO,PBFFREE		
6	U604	IC	EUSY0212002	HVQFN ,52 PIN,R/TP ,BLUETOOTH RADIO MODULE WITH BASEBAND CONTROLLER_Pb free		
6	U701	IC	EUSY0188103	QFN ,24 PIN,R/TP ,MAIN+FLASH UPTO400mAcontinuous		
6	V201	DIODE,VARIABLE CAP	EDVY0001801	SCD80 ,0.09 pF,R/TP ,		
6	V501	DIODE,TVS	EDTY0007001	SOT23-6 ,9 V , W,R/TP ,TVS DIODE ARRAY		
6	V502	DIODE,SWITCHING	EDSY0011901	EMD2 ,30 V,1 A,R/TP ,VF=1.5V(IF=200mA) , IR=30uA(VR=10V)		
6	V503	DIODE,SWITCHING	EDSY0011901	EMD2 ,30 V,1 A,R/TP ,VF=1.5V(IF=200mA) , IR=30uA(VR=10V)		
6	V701	DIODE,TVS	EDTY0006401	SC70-6L ,5 V,100 W,R/TP ,PB-FREE		
6	W101	CONN,RF SWITCH	ENWY0003301	,SMD ,0.4 dB,		
6	X502	CONN,SOCKET	ENSY0009901	8 PIN,ETC ,SMD ,2.54 mm,2.2T UIM CONNECTOR WITH BRIDGE		
6	X701	CONN,RECEPTACLE	ENEY0004101	24 PIN,3 , ,25.3*10*(3+1.5)T		
6	Z201	FILTER,SAW	SFSY0012502	190 MHz,3.8*3.8*1.2 ,SMD ,6pin, Bal-Bal, 1000//1000		
5	SAFD00	PCB ASSY,MAIN,SMT TOP	SAFD0064901			
6	B301	IC	EUSY0067201	MAA05A ,5 PIN,R/TP ,2.4V,10uA, TEMP SENSOR(Pb Free)		
6	B601	X-TAL	EXXY0004602	.032768 MHz,20 PPM,12.5 pF,65000 ohm,SMD ,6.9*1.4*1.3 ,		
6	C111	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		
6	C115	CAP,CERAMIC,CHIP	ECCH0005705	10 uF,6.3V ,K ,X5R ,HD ,2012 ,R/TP		
6	C116	CAP,CERAMIC,CHIP	ECCH0005705	10 uF,6.3V ,K ,X5R ,HD ,2012 ,R/TP		
6	C1930	CAP,CERAMIC,CHIP	ECCH0000110	10 pF,50V,D,NP0,TC,1005,R/TP		
6	C1931	CAP,CERAMIC,CHIP	ECCH0000110	10 pF,50V,D,NP0,TC,1005,R/TP		
6	C1932	CAP,CERAMIC,CHIP	ECCH0000110	10 pF,50V,D,NP0,TC,1005,R/TP		
6	C1933	CAP,CERAMIC,CHIP	ECCH0000110	10 pF,50V,D,NP0,TC,1005,R/TP		
6	C301	CAP,CERAMIC,CHIP	ECCH0000137	330 pF,50V ,K ,X7R ,HD ,1005 ,R/TP		
6	C302	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		
6	C303	CAP,CERAMIC,CHIP	ECCH0005705	10 uF,6.3V ,K ,X5R ,HD ,2012 ,R/TP		
6	C304	CAP,CERAMIC,CHIP	ECCH0005705	10 uF,6.3V ,K ,X5R ,HD ,2012 ,R/TP		
6	C305	CAP,CERAMIC,CHIP	ECCH0005705	10 uF,6.3V ,K ,X5R ,HD ,2012 ,R/TP		
6	C306	CAP,CERAMIC,CHIP	ECCH0000143	1 nF,50V,K,X7R,HD,1005,R/TP		
6	C307	CAP,CERAMIC,CHIP	ECCH0000186	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP		
6	C308	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP		
6	C309	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		

10. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	Part Number	Specification	Color	Remark
6	C310	CAP,CERAMIC,CHIP	ECCH0000167	0.1 uF,6.3V,K,X5R,HD,1005,R/TP		
6	C311	CAP,CERAMIC,CHIP	ECCH0000110	10 pF,50V,D,NP0,TC,1005,R/TP		
6	C312	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		
6	C413	CAP,CERAMIC,CHIP	ECCH0000165	68 nF,6.3V,K,X5R,HD,1005,R/TP		
6	C414	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP		
6	C415	CAP,CERAMIC,CHIP	ECCH0000165	68 nF,6.3V,K,X5R,HD,1005,R/TP		
6	C416	CAP,CERAMIC,CHIP	ECCH0000165	68 nF,6.3V,K,X5R,HD,1005,R/TP		
6	C417	CAP,CERAMIC,CHIP	ECCH0000165	68 nF,6.3V,K,X5R,HD,1005,R/TP		
6	C418	CAP,CERAMIC,CHIP	ECCH0000165	68 nF,6.3V,K,X5R,HD,1005,R/TP		
6	C419	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP		
6	C425	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		
6	C426	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		
6	C427	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		
6	C428	CAP,CERAMIC,CHIP	ECCH0000111	12 pF,50V,J,NP0,TC,1005,R/TP		
6	C429	CAP,CERAMIC,CHIP	ECCH0000186	33 pF,50V,J,NP0,TC,1005,R/TP		
6	C430	CAP,CERAMIC,CHIP	ECCH0000901	2.2 pF,50V,C,NP0,TC,1005,R/TP		
6	C431	CAP,CERAMIC,CHIP	ECCH0000186	33 pF,50V,J,NP0,TC,1005,R/TP		
6	C432	CAP,CERAMIC,CHIP	ECCH0000901	2.2 pF,50V,C,NP0,TC,1005,R/TP		
6	C433	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		
6	C434	CAP,CERAMIC,CHIP	ECCH0000110	10 pF,50V,D,NP0,TC,1005,R/TP		
6	C435	CAP,CERAMIC,CHIP	ECCH0000175	2.7 pF,50V,B,NP0,TC,1005,R/TP		
6	C436	CAP,CERAMIC,CHIP	ECCH0000175	2.7 pF,50V,B,NP0,TC,1005,R/TP		
6	C437	INDUCTOR,CHIP	ELCH0001033	1.5 nH,S,1005,R/TP,PBFREE		
6	C438	CAP,CERAMIC,CHIP	ECCH0000110	10 pF,50V,D,NP0,TC,1005,R/TP		
6	C439	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP		
6	C440	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		
6	C441	CAP,CERAMIC,CHIP	ECCH0000143	1 nF,50V,K,X7R,HD,1005,R/TP		
6	C442	CAP,CERAMIC,CHIP	ECCH0000143	1 nF,50V,K,X7R,HD,1005,R/TP		
6	C443	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP		
6	C444	CAP,CERAMIC,CHIP	ECCH0000146	1.8 nF,50V,K,X7R,HD,1005,R/TP		
6	C445	CAP,CERAMIC,CHIP	ECCH0000144	1.2 nF,50V,K,X7R,HD,1005,R/TP		
6	C447	CAP,CERAMIC,CHIP	ECCH0000140	560 pF,50V,K,X7R,HD,1005,R/TP		
6	C448	CAP,CERAMIC,CHIP	ECCH0000137	330 pF,50V,K,X7R,HD,1005,R/TP		
6	C449	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP		

10. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	Part Number	Specification	Color	Remark
6	C450	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		
6	C451	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		
6	C452	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP		
6	C453	CAP,CERAMIC,CHIP	ECCH0000186	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP		
6	C454	CAP,CERAMIC,CHIP	ECCH0000186	33 pF,50V ,J ,NP0 ,TC ,1005 ,R/TP		
6	C501	CAP,TANTAL,CHIP	ECTH0002702	1 uF,16V ,M ,STD ,1608 ,R/TP		
6	C502	CAP,TANTAL,CHIP	ECTH0002702	1 uF,16V ,M ,STD ,1608 ,R/TP		
6	C503	CAP,CERAMIC,CHIP	ECCH0000279	0.47 uF,10V ,Z ,Y5V ,HD ,1608 ,R/TP		
6	C504	CAP,CERAMIC,CHIP	ECCH0005801	2.2 uF,6.3V ,K ,X5R ,TC ,1608 ,R/TP		
6	C508	CAP,CERAMIC,CHIP	ECCH0006201	4.7 uF,6.3V ,K ,X5R ,TC ,1608 ,R/TP		
6	C509	CAP,CERAMIC,CHIP	ECCH0000128	100 pF,50V,J,NP0,TC,1005,R/TP		
6	C510	CAP,CERAMIC,CHIP	ECCH0005801	2.2 uF,6.3V ,K ,X5R ,TC ,1608 ,R/TP		
6	C511	CAP,CERAMIC,CHIP	ECCH0000155	10 nF,16V,K,X7R,HD,1005,R/TP		
6	C512	CAP,CERAMIC,CHIP	ECCH0000276	1 uF,10V,Z,Y5V,HD,1608,R/TP		
6	C513	CAP,CHIP,MAKER	ECZH0003501	1 uF,6.3V ,K ,X5R ,HD ,1608 ,R/TP		
6	C517	CAP,CERAMIC,CHIP	ECCH0004903	1 uF,6.3V ,Z ,Y5V ,TC ,1005 ,R/TP		
6	C519	CAP,CERAMIC,CHIP	ECCH0004903	1 uF,6.3V ,Z ,Y5V ,TC ,1005 ,R/TP		
6	C524	CAP,CERAMIC,CHIP	ECCH0002003	33 nF,16V ,K ,B ,TC ,1005 ,R/TP		
6	C525	CAP,CERAMIC,CHIP	ECCH0000126	68 pF,50V,J,NP0,TC,1005,R/TP		
6	C526	CAP,CERAMIC,CHIP	ECCH0002003	33 nF,16V ,K ,B ,TC ,1005 ,R/TP		
6	C528	CAP,CERAMIC,CHIP	ECCH0002003	33 nF,16V ,K ,B ,TC ,1005 ,R/TP		
6	C529	CAP,CERAMIC,CHIP	ECCH0000126	68 pF,50V,J,NP0,TC,1005,R/TP		
6	C554	CAP,CERAMIC,CHIP	ECCH0004903	1 uF,6.3V ,Z ,Y5V ,TC ,1005 ,R/TP		
6	C555	CAP,CERAMIC,CHIP	ECCH0000110	10 pF,50V,D,NP0,TC,1005,R/TP		
6	C558	CAP,CERAMIC,CHIP	ECCH0000122	47 pF,50V,J,NP0,TC,1005,R/TP		
6	C559	CAP,CERAMIC,CHIP	ECCH0000122	47 pF,50V,J,NP0,TC,1005,R/TP		
6	C560	CAP,CERAMIC,CHIP	ECCH0002003	33 nF,16V ,K ,B ,TC ,1005 ,R/TP		
6	C561	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C562	CAP,CERAMIC,CHIP	ECCH0004903	1 uF,6.3V ,Z ,Y5V ,TC ,1005 ,R/TP		
6	C563	CAP,CERAMIC,CHIP	ECCH0005705	10 uF,6.3V ,K ,X5R ,HD ,2012 ,R/TP		
6	C564	CAP,CERAMIC,CHIP	ECCH0005705	10 uF,6.3V ,K ,X5R ,HD ,2012 ,R/TP		
6	C566	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		
6	C567	CAP,CERAMIC,CHIP	ECCH0000165	68 nF,6.3V,K,X5R,HD,1005,R/TP		
6	C568	CAP,CERAMIC,CHIP	ECCH0000165	68 nF,6.3V,K,X5R,HD,1005,R/TP		

10. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	Part Number	Specification	Color	Remark
6	C570	CAP,CERAMIC,CHIP	ECCH0000126	68 pF,50V,J,NP0,TC,1005,R/TP		
6	C571	CAP,CERAMIC,CHIP	ECCH0000126	68 pF,50V,J,NP0,TC,1005,R/TP		
6	C572	CAP,TANTAL,CHIP	ECTH0002702	1 uF,16V ,M ,STD ,1608 ,R/TP		
6	C573	CAP,TANTAL,CHIP	ECTH0002702	1 uF,16V ,M ,STD ,1608 ,R/TP		
6	C574	CAP,CERAMIC,CHIP	ECCH0000276	1 uF,10V,Z,Y5V,HD,1608,R/TP		
6	C575	CAP,CERAMIC,CHIP	ECCH0004903	1 uF,6.3V ,Z ,Y5V ,TC ,1005 ,R/TP		
6	C577	CAP,CERAMIC,CHIP	ECCH0004903	1 uF,6.3V ,Z ,Y5V ,TC ,1005 ,R/TP		
6	C578	CAP,CERAMIC,CHIP	ECCH0000148	2.7 nF,50V,K,X7R,HD,1005,R/TP		
6	C579	CAP,CERAMIC,CHIP	ECCH0000149	3.3 nF,50V,K,X7R,HD,1005,R/TP		
6	C580	CAP,CHIP,MAKER	ECZH0003501	1 uF,6.3V ,K ,X5R ,HD ,1608 ,R/TP		
6	C581	CAP,CERAMIC,CHIP	ECCH0000122	47 pF,50V,J,NP0,TC,1005,R/TP		
6	C582	CAP,CERAMIC,CHIP	ECCH0000151	4.7 nF,25V,K,X7R,HD,1005,R/TP		
6	C584	CAP,TANTAL,CHIP,MAKER	ECTZ0005501	100 uF,6.3V ,M ,STD ,ETC ,R/TP		
6	C585	CAP,TANTAL,CHIP,MAKER	ECTZ0005501	100 uF,6.3V ,M ,STD ,ETC ,R/TP		
6	C587	CAP,CERAMIC,CHIP	ECCH0000149	3.3 nF,50V,K,X7R,HD,1005,R/TP		
6	C589	CAP,CERAMIC,CHIP	ECCH0000151	4.7 nF,25V,K,X7R,HD,1005,R/TP		
6	C590	CAP,CERAMIC,CHIP	ECCH0005705	10 uF,6.3V ,K ,X5R ,HD ,2012 ,R/TP		
6	C592	CAP,TANTAL,CHIP,MAKER	ECTZ0005501	100 uF,6.3V ,M ,STD ,ETC ,R/TP		
6	C593	CAP,TANTAL,CHIP,MAKER	ECTZ0005501	100 uF,6.3V ,M ,STD ,ETC ,R/TP		
6	C601	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C602	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C603	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C604	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C605	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C606	CAP,CERAMIC,CHIP	ECCH0000137	330 pF,50V ,K ,X7R ,HD ,1005 ,R/TP		
6	C607	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		
6	C608	CAP,CERAMIC,CHIP	ECCH0000115	22 pF,50V,J,NP0,TC,1005,R/TP		
6	C609	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C610	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C611	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C612	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C613	CAP,CERAMIC,CHIP	ECCH0000143	1 nF,50V,K,X7R,HD,1005,R/TP		
6	C614	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C615	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		

10. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	Part Number	Specification	Color	Remark
6	C616	CAP,CERAMIC,CHIP	ECCH0000182	0.1 uF,10V ,K ,X5R ,HD ,1005 ,R/TP		
6	C617	CAP,CERAMIC,CHIP	ECCH0000182	0.1 uF,10V ,K ,X5R ,HD ,1005 ,R/TP		
6	C618	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C619	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C620	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C621	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C622	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C623	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C624	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C625	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C626	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C627	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C628	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C629	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C630	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C631	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C632	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C633	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C634	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C635	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C636	CAP,CERAMIC,CHIP	ECCH0000276	1 uF,10V,Z,Y5V,HD,1608,R/TP		
6	C637	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C638	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C639	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C644	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	C739	CAP,CERAMIC,CHIP	ECCH0000168	0.1 uF,16V,Z,Y5V,HD,1005,R/TP		
6	CN502	CONN,JACK/PLUG,EARPHONE	ENJE0003603	12 ,12 PIN,MMIC CONN.12P		
6	CN703	CONNECTOR,BOARD TO BOARD	ENBY0002103	24 PIN,.5 mm,STRAIGHT ,SILVER ,		
6	D501	DIODE,SWITCHING	EDSY0011901	EMD2 ,30 V,1 A,R/TP ,VF=1.5V(IF=200mA) , IR=30uA(VR=10V)		
6	D601	IC	EUSY0135001	u289 BGA ,289 PIN,R/TP ,ASIC / BASEBAND CONTROLLER / MARITA		
6	D702	DIODE,TVS	EDTY0006401	SC70-6L ,5 V,100 W,R/TP ,PB-FREE		
6	FB701	RES,CHIP,MAKER	ERHZ0000608	10 ohm,1/10W ,F ,1608 ,R/TP		
6	FB702	FILTER,BEAD,CHIP	SFBH0002302	120 ohm,1608 ,CHIP BEAD, 2000mA		

10. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	Part Number	Specification	Color	Remark
6	FL102	DUPLEXER,IMT	SDMY0000701	1950 MHz,2140 MHz,1.45 dB,1.60 dB,41 dB,50 dB,5.4*5.0*1.6 ,SMD ,		
6	FL402	FILTER,SAW	SFSY0024302	1842.5 MHz,1.4*1.1*0.6 ,SMD ,5pin, Unbal-Bal, 50//150		
6	FL403	FILTER,SAW	SFSY0024303	1960 MHz,1.4*1.1*0.6 ,SMD ,5pin, Unbal-Bal, 50//150		
6	FL701	VARISTOR	SEVY0005501	18 V ,SMD ,4ch. R-Varistor Array(100Ohm,15pF)		
6	FL703	VARISTOR	SEVY0005501	18 V ,SMD ,4ch. R-Varistor Array(100Ohm,15pF)		
6	FL704	VARISTOR	SEVY0005501	18 V ,SMD ,4ch. R-Varistor Array(100Ohm,15pF)		
6	L199	INDUCTOR,CHIP	ELCH0005009	100 nH,J ,1005 ,R/TP ,		
6	L301	FILTER,BEAD,CHIP	SFBH0002302	120 ohm,1608 ,CHIP BEAD, 2000mA		
6	L302	FILTER,BEAD,CHIP	SFBH0002302	120 ohm,1608 ,CHIP BEAD, 2000mA		
6	L303	FILTER,BEAD,CHIP	SFBH0002302	120 ohm,1608 ,CHIP BEAD, 2000mA		
6	L304	INDUCTOR,SMD,POWER	ELCP0009401	4.7 uH,M ,2.8*2.6*1.0 ,R/TP ,		
6	L403	FILTER,BEAD,CHIP	SFBH0007103	75 ohm,1005 ,CHIP BEAD, 300mA		
6	L404	FILTER,BEAD,CHIP	SFBH0007103	75 ohm,1005 ,CHIP BEAD, 300mA		
6	L405	INDUCTOR,CHIP	ELCH0001413	22 nH,J ,1005 ,R/TP ,PBFREE		
6	L406	INDUCTOR,CHIP	ELCH0005006	33 nH,J ,1005 ,R/TP ,		
6	L407	INDUCTOR,CHIP	ELCH0005013	4.7 nH,S ,1005 ,R/TP ,		
6	L408	INDUCTOR,CHIP	ELCH0001408	6.8 nH,J ,1005 ,R/TP ,Pb Free		
6	L409	INDUCTOR,CHIP	ELCH0005013	4.7 nH,S ,1005 ,R/TP ,		
6	L410	INDUCTOR,CHIP	ELCH0001401	15 nH,J ,1005 ,R/TP ,Pb Free		
6	L411	FILTER,BEAD,CHIP	SFBH0007103	75 ohm,1005 ,CHIP BEAD, 300mA		
6	L412	INDUCTOR,CHIP	ELCH0007404	5.6 uH,K ,1608 ,R/TP ,		
6	L413	INDUCTOR,CHIP	ELCH0007403	100 uH,K ,2012 ,R/TP ,		
6	L414	FILTER,BEAD,CHIP	SFBH0007103	75 ohm,1005 ,CHIP BEAD, 300mA		
6	L415	INDUCTOR,CHIP	ELCH0001402	18 nH,J ,1005 ,R/TP ,Pb Free		
6	L416	FILTER,BEAD,CHIP	SFBH0007103	75 ohm,1005 ,CHIP BEAD, 300mA		
6	N301	IC	EUSY0136001	3 X 4 UCSP ,10 PIN,R/TP ,600 mA BUCK REGULATORS / DYNAMIC OUTPUT VOLTAGE,PBFREE		
6	N302	PAM	SMPY0002801	26 dBm,40 % ,83 A,-58 dBc,23.5 dB,8.0*6.0*1.4 ,SMD ,		
6	N303	ISOLATOR,IMT	SQMY0001001	1950 MHz,3.2*3.2*1.5 ,SMD ,1920~1980MHz		
6	N402	IC	EUSY0133103	BGA ,64 PIN,R/TP ,6*6 mm, lead-free, Analog Baseband ASIC		
6	N403	TRANSFORMER,MATCHING	STMY0018401	6 PIN,SMD ,DCS TX BALUN		
6	N404	TRANSFORMER,MATCHING	STMY0018402	6 PIN,SMD ,GSM Tx Balun		
6	N405	IC	EUSY0132801	56 ball ,56 PIN,R/TP ,RFIC		

10. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	Part Number	Specification	Color	Remark
6	N501	IC	EUSY0171302	SOT-23 ,5 PIN,R/TP ,150mA 3.3V LDO, Pb-free		
6	N502	IC	EUSY0153001	SOT23-5 ,5 PIN,R/TP ,150 mA LDO REGULATOR / 1.5V		
6	N504	IC	EUSY0171201	CSP ,25 PIN,R/TP ,6 CHANNEL ESD FILTER, EMP SOLUTION, Pb-free		
6	N701	IC	EUSY0171401	CSP ,20 PIN,R/TP ,7 CHANNEL ESD FILTER ARRAY, KNATTE, Pb-free		
6	Q601	TR,BJT,NPN	EQBN0014901	SOT323 ,.2 W,R/TP ,NPN SWITCHING TR, Pb free		
6	Q602	TR,BJT,NPN	EQBN0013301	2-2H1A ,.1 W,R/TP ,VEBO=6V, Pb free		
6	Q701	TR,BJT,NPN	EQBN0013701	EMT6 ,150 mW,R/TP ,DUAL TRANSISTORS		
6	R2130	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R2131	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R2241	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R2248	RES,CHIP	ERHY0000216	68 ohm,1/16W,J,1005,R/TP		
6	R2249	RES,CHIP	ERHY0000216	68 ohm,1/16W,J,1005,R/TP		
6	R2250	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R2252	RES,CHIP	ERHY0000261	10K ohm,1/16W,J,1005,R/TP		
6	R2253	RES,CHIP	ERHY0000261	10K ohm,1/16W,J,1005,R/TP		
6	R301	RES,CHIP	ERHY0000138	33K ohm,1/16W,F,1005,R/TP		
6	R302	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP		
6	R303	RES,CHIP	ERHY0000271	39K ohm,1/16W,J,1005,R/TP		
6	R306	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R307	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R308	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R404	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R405	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP		
6	R406	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R409	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R410	RES,CHIP	ERHY0000220	100 ohm,1/16W,J,1005,R/TP		
6	R411	RES,CHIP	ERHY0000220	100 ohm,1/16W,J,1005,R/TP		
6	R412	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R414	RES,CHIP	ERHY0000206	18 ohm,1/16W,J,1005,R/TP		
6	R415	RES,CHIP	ERHY0000228	270 ohm,1/16W,J,1005,R/TP		
6	R416	RES,CHIP	ERHY0000228	270 ohm,1/16W,J,1005,R/TP		
6	R417	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R418	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		

10. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	Part Number	Specification	Color	Remark
6	R420	INDUCTOR,CHIP	ELCH0005015	6.8 nH,S ,1005 ,R/TP ,		
6	R421	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R422	INDUCTOR,CHIP	ELCH0005015	6.8 nH,S ,1005 ,R/TP ,		
6	R423	RES,CHIP	ERHY0000220	100 ohm,1/16W,J,1005,R/TP		
6	R424	RES,CHIP	ERHY0000220	100 ohm,1/16W,J,1005,R/TP		
6	R425	RES,CHIP	ERHY0000235	560 ohm,1/16W,J,1005,R/TP		
6	R426	RES,CHIP	ERHY0000222	120 ohm,1/16W,J,1005,R/TP		
6	R427	RES,CHIP	ERHY0000231	390 ohm,1/16W,J,1005,R/TP		
6	R428	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R429	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R430	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R431	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R501	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R502	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R507	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP		
6	R508	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R509	RES,CHIP	ERHY0000241	1K ohm,1/16W,J,1005,R/TP		
6	R513	RES,CHIP	ERHY0000274	51K ohm,1/16W,J,1005,R/TP		
6	R514	RES,CHIP	ERHY0000261	10K ohm,1/16W,J,1005,R/TP		
6	R515	RES,CHIP	ERHY0000261	10K ohm,1/16W,J,1005,R/TP		
6	R524	RES,CHIP	ERHY0000241	1K ohm,1/16W,J,1005,R/TP		
6	R525	RES,CHIP	ERHY0000241	1K ohm,1/16W,J,1005,R/TP		
6	R529	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP		
6	R530	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R531	RES,CHIP	ERHY0000264	18K ohm,1/16W,J,1005,R/TP		
6	R532	RES,CHIP	ERHY0000264	18K ohm,1/16W,J,1005,R/TP		
6	R533	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R534	RES,CHIP	ERHY0000264	18K ohm,1/16W,J,1005,R/TP		
6	R537	RES,CHIP	ERHY0000264	18K ohm,1/16W,J,1005,R/TP		
6	R539	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R566	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R567	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP		
6	R569	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R572	RES,CHIP	ERHY0000236	620 ohm,1/16W,J,1005,R/TP		

10. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	Part Number	Specification	Color	Remark
6	R573	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R574	RES,CHIP	ERHY0000236	620 ohm,1/16W,J,1005,R/TP		
6	R576	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R577	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R578	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R579	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R580	CAP,CERAMIC,CHIP	ECCH0002003	33 nF,16V ,K ,B ,TC ,1005 ,R/TP		
6	R581	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R582	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R583	CAP,CERAMIC,CHIP	ECCH0002003	33 nF,16V ,K ,B ,TC ,1005 ,R/TP		
6	R584	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R585	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R586	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP		
6	R587	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R588	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R589	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP		
6	R590	RES,CHIP	ERHY0000259	8.2K ohm,1/16W,J,1005,R/TP		
6	R591	RES,CHIP	ERHY0000282	120K ohm,1/16W,J,1005,R/TP		
6	R592	RES,CHIP	ERHY0000282	120K ohm,1/16W,J,1005,R/TP		
6	R594	RES,CHIP	ERHY0000254	4.7K ohm,1/16W,J,1005,R/TP		
6	R595	RES,CHIP	ERHY0000261	10K ohm,1/16W,J,1005,R/TP		
6	R596	RES,CHIP	ERHY0000282	120K ohm,1/16W,J,1005,R/TP		
6	R597	RES,CHIP	ERHY0000282	120K ohm,1/16W,J,1005,R/TP		
6	R598	RES,CHIP	ERHY0000254	4.7K ohm,1/16W,J,1005,R/TP		
6	R601	RES,CHIP	ERHY0000254	4.7K ohm,1/16W,J,1005,R/TP		
6	R602	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP		
6	R604	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R606	RES,CHIP	ERHY0000213	47 ohm,1/16W,J,1005,R/TP		
6	R608	RES,CHIP	ERHY0000250	3.3K ohm,1/16W,J,1005,R/TP		
6	R609	RES,CHIP	ERHY0000250	3.3K ohm,1/16W,J,1005,R/TP		
6	R610	RES,CHIP	ERHY0000243	1.2K ohm,1/16W,J,1005,R/TP		
6	R613	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP		
6	R614	RES,CHIP	ERHY0000233	470 ohm,1/16W,J,1005,R/TP		
6	R615	RES,CHIP	ERHY0000283	130K ohm,1/16W,J,1005,R/TP		

10. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	Part Number	Specification	Color	Remark
6	R616	RES,CHIP	ERHY0000213	47 ohm,1/16W,J,1005,R/TP		
6	R617	RES,CHIP	ERHY0000275	56K ohm,1/16W,J,1005,R/TP		
6	R618	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP		
6	R619	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP		
6	R620	RES,CHIP	ERHY0000275	56K ohm,1/16W,J,1005,R/TP		
6	R621	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP		
6	R626	RES,CHIP	ERHY0000241	1K ohm,1/16W,J,1005,R/TP		
6	R627	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R628	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP		
6	R629	RES,CHIP	ERHY0000201	0 ohm,1/16W,J,1005,R/TP		
6	R630	RES,CHIP	ERHY0000250	3.3K ohm,1/16W,J,1005,R/TP		
6	R631	RES,CHIP	ERHY0000220	100 ohm,1/16W,J,1005,R/TP		
6	R634	RES,CHIP	ERHY0000282	120K ohm,1/16W,J,1005,R/TP		
6	R636	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP		
6	R641	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP		
6	R653	RES,CHIP	ERHY0000292	470K ohm,1/16W,J,1005,R/TP		
6	R654	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP		
6	R655	RES,CHIP	ERHY0000280	100K ohm,1/16W,J,1005,R/TP		
6	R727	RES,CHIP	ERHY0000204	12 ohm,1/16W,J,1005,R/TP		
6	R741	RES,CHIP	ERHY0000249	2.7K ohm,1/16W,J,1005,R/TP		
6	R742	RES,CHIP	ERHY0000204	12 ohm,1/16W,J,1005,R/TP		
6	S601	CONN,SOCKET	ENSY0014101	8 PIN,ETC , ,1.1 mm,T-Flash Memory Socket		
6	U502	IC	EUSY0232807	sot 23-5 ,5 PIN,R/TP ,1.8V,150mA LDO		
6	U504	IC	EUSY0160001	MicroStar Junior ,15 PIN,R/TP ,1.1W Class-D Mono Audio AMP		
6	U505	IC	EUSY0160001	MicroStar Junior ,15 PIN,R/TP ,1.1W Class-D Mono Audio AMP		
6	U507	IC	EUSY0175001	FFP16 ,16 PIN,R/TP ,3D SURROUND AUDIO PROCESSOR		
6	U508	IC	EUSY0188601	MICROBUMP ,10 PIN,R/TP ,Dual SPDT Analog switch(Pb Free)		
6	U509	IC	EUSY0142501	LLP ,8 PIN,R/TP ,Dual 105mW Headphone Amplifier		
6	U601	IC	EUSY0163901	uCSP ,10 PIN,R/TP ,Dual Analog Switch, 300MHz Bandwidth		
6	U602	IC	EUSY0163901	uCSP ,10 PIN,R/TP ,Dual Analog Switch, 300MHz Bandwidth		
6	U603	IC	EUSY0211101	SCSP ,88 PIN,ETC ,512M(256*2) MLC NOR +128M (64*2) PS/ 1.8V/ PB FREE		

10. EXPLODED VIEW & REPLACEMENT PART LIST

Level	Location No.	Description	Part Number	Specification	Color	Remark
6	Z401	FILTER,SAW	SFSY0024301	942.5 MHz,1.4*1.1*0.6 ,SMD ,5pin, Unbal-Bal, 50//150		
5	SPFY	PCB,MAIN	SPFY0106301	FR-4 ,0.8 mm,STAGGERED-8 ,		
3	SUMY00	MICROPHONE	SUMY0010702	UNIT ,44 dB,4*1.5 ,spring type		

10. EXPLODED VIEW & REPLACEMENT PART LIST

10.3 Accessory

Note: This Chapter is used for reference, Part order is ordered by SBOM standard on GCSC

Level	Location No.	Description	Part Number	Specification	Color	Remark
3	MHBY00	HANDSTRAP	MHBY0000404	Hand Strap 135mm	Black	
3	SBPL00	BATTERY PACK,LI-ION	SBPL0072221	3.7 V,1400 mAh,1 CELL,PRISMATIC ,U8130 BATTERY(Li-Polymer) 1400mA(Typical)	Silver	
3	SGDY00	DATA CABLE	SGDY0005601	DK-40G ,K8000 24PIN I/O + USB A TYPE		
3	SGEY00	EAR PHONE/EAR MIKE SET	SGEY0003707	U880,8550 ,GRAY-AIR CAP,2.0TMMI12P		49
3	SSAD00	ADAPTOR,AC-DC	SSAD0007848	FREE ,50 Hz,4.6 V,0.8 A,CE ,3G		